TI Designs：TIDA-01584
采用负载开关的功率排序参考设计

说明

此参考设计使用负载开关演示各种电源定序配置。对于必须按特定顺序开启的电压轨，电源时序是确保安全及可靠运行的关键。电源轨定序还有助于错开通电过程中的浪涌电流，这将降低系统压力并防止意外达到反向偏置条件。通过使用集成的负载开关，无需大量的处理器干预或外部数字组件，即可独立调整每个电压轨的时序。通过用于调整上升时间的计时电容 (C_T) 引脚和用于调整下降时间的快速输出放电 (QOD) 引脚，可控制负载开关时序。此设计非常适合 用于多功能打印机 (MFP) 和机顶盒 (STB) 等应用，此类应用需要使用特定的时序来开启各种子系统和处理器轨。

资源

TIDA-01584	设计文件夹
TPS22918	产品文件夹
TPS22810	产品文件夹
TPS22917	产品文件夹
TPS22975	产品文件夹

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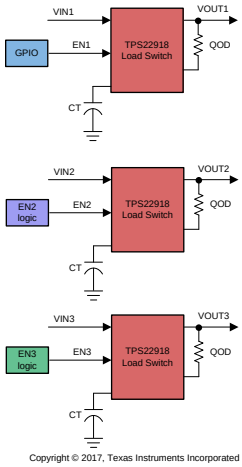
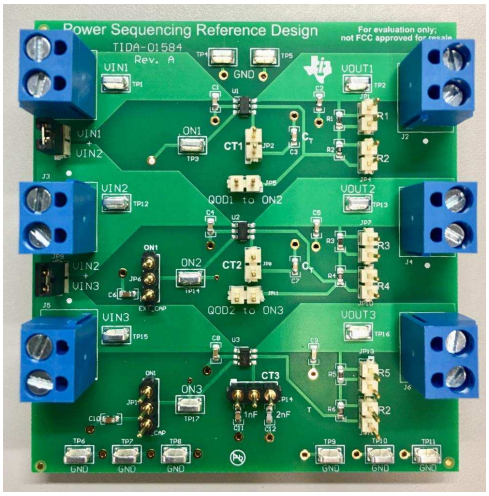
特性

- 三种不同的电源定序配置：CT 配置、QOD 配置和独立 GPIO 配置
- 使用 CT 控制上升时间以及使用 QOD 控制断电时间的可调定时阈值
- 引脚对引脚封装方式允许根据不同的电压、电流和 R_{ON} 要求在多个负载开关之间交换
- 在系统发生意外功率损耗的情况下，正常关闭定序
- 负载开关可帮助实现较分立式 MOSFET 解决方案更小的解决方案尺寸和更少的组件数量

应用

- 多功能打印机 (MFP)
- 机顶盒 (STB)
- 远端射频单元
- 基带装置





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1 System Description

Many applications require controlled power-up and power-down sequences to properly operate subsystems and downstream components. This reference design showcases three different power-sequencing configurations that use integrated load switches. Power sequencing can be achieved by connecting various jumpers, resistors, and capacitors on the board. Because timing constraints vary greatly between different applications and processor-to-processor communications, this design is not limited to specific timing constraints or sequences. Instead, the design allows the user to configure multiple timing configurations to fit their unique system specifications. Using load switches ensures that subsystems will power up and down in a safe and reliable fashion while housing a smaller footprint in comparison to a discrete MOSFET implementation.

The first power-sequencing configuration routes a single GPIO to the enable (ON) pin of the three load switches. When the GPIO (ON1) is enabled, the three load switches turn on at the same time. By adjusting the capacitance on the timing capacitance pin (CT pin), the voltages on the different channels ramp up at different times . A larger capacitance on the CT pin results in a longer ramp-up time. The ramp-up time is measured by changing the slope of the rise time, called the *slew rate*. An example of this configuration is shown in 图 1.

The second power-sequencing configuration also contains a single GPIO, but the configuration is only connected to the first load switch. On the output of the first load switch, QOD is connected to the enable pin of the second load switch, effectively *daisy-chaining* the devices together. QOD pulls V_{OUT} to ground whenever the device is turned off, which prevents the output from *floating* or entering an undetermined state. Connecting various resistors to the QOD pin changes the rate that the output is falls to ground. By connecting QOD to the enable pin of the next load switch in parallel to an external capacitor, this connection creates an RC delay. This connection creates a power sequencing configuration that is dependent on the timing of an external RC delay. The CT pins on all three load switches can be connected to the same capacitance value, which ensures that each voltage rail ramps up with the same slew rate. The block diagram in 图 3 explains the configuration in more detail.

The third power-sequencing configuration leaves the three load switch channels independent, which requires external control signals to control the timing sequence. Some of these external devices can include digital timing ICs, supply voltage supervisors (SVS), or external oscillators. The CT pin can be used alongside the external timing component to further customize timing windows.

In each of the three power-sequencing configurations, power-down sequencing is achieved by adjusting the resistance on the QOD pin. By increasing the external resistance from VOUT to QOD, the current decreases into the QOD pin and increases the time for the rail to power off.

1.1 Key System Specifications

表 **1. Key System Specifications Using TPS22918(1)**

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range(1)	V_{IN}	1 V to 5.5 V
Output voltage range(1)	V_{OUT}	1 V to 5.5 V
Maximum load current(1)	I_{OUT}	2 A
Number of power rails	—	Three channels
Typical TPS22918 turn-on time	t_{ON}	135 µs
Output capacitance	C_{OUT}	10 µF
Internal QOD resistance	R_{PD}	24 Ω

(1) Input voltage range, output voltage range, maximum load current, and R_{ON} can be adjusted by using a different load switch.

表 1. Key System Specifications Using TPS22918[(1)] (continued)

PARAMETER	SPECIFICATIONS	DETAILS
External QOD resistance	R_{QOD}	0 Ω, 300 Ω, and 500 Ω
On-resistance	R_{ON}	52 mΩ

2 System Overview

2.1 Block Diagram

图 1 describes the CT configuration. Power-sequencing timing is achieved by changing the capacitance value on the CT pin. A larger capacitance on the CT pin results in a slower slew rate and rise time. Power-down Sequencing is achieved with the QOD pin; adjusting the QOD resistance will vary the rate at which the output decays. 图 2 shows the expected behavior of this configuration.

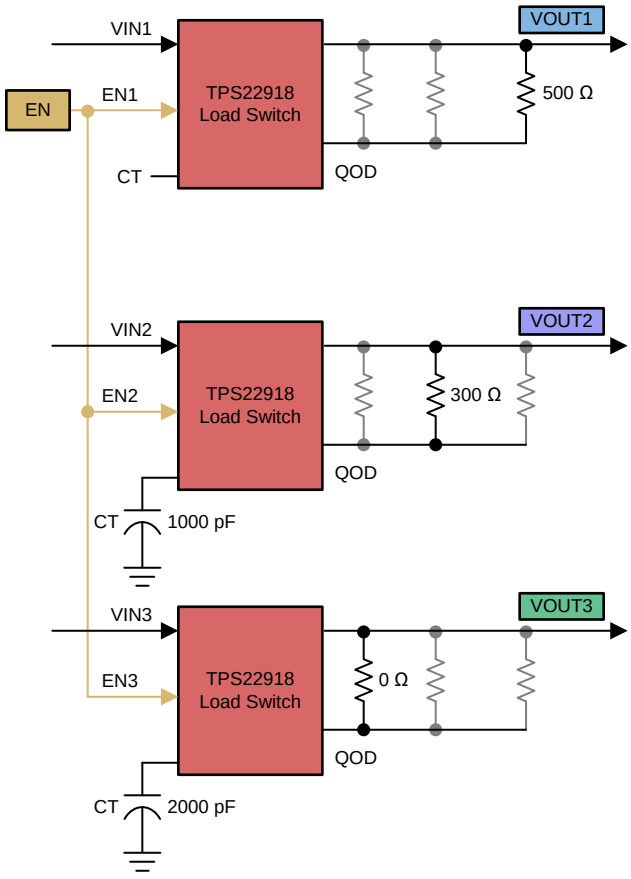

图 1. TIDA-01584 CT Configuration Block Diagram

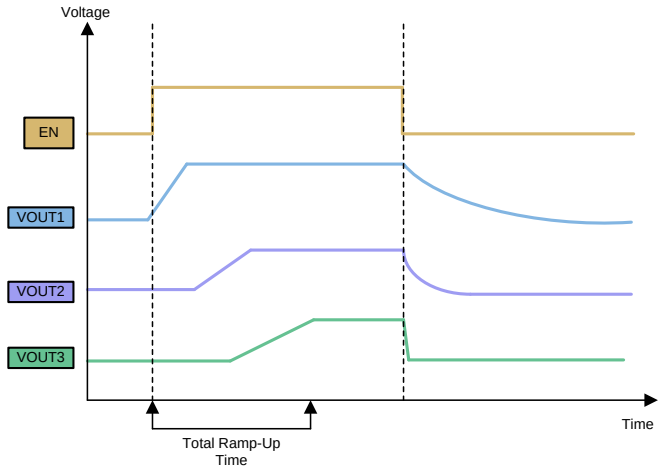

图 2. CT Configuration Expected Behavior

图 3 describes the QOD configuration. Power-up timing is achieved by connecting QOD of the previous switch to the enable pin of the next switch. The timing delay is created by changing an external RC delay capacitor (10µF on 图 3). A larger external capacitor increases the delay between voltage rails. The slew rate of the rails can remain the same by using the same capacitance on the CT pin, but different capacitances across the switches can be used for different slew rates, similar to the CT configuration. Power-down sequencing is achieved with the QOD pin. 图 4 shows the expected behavior of this configuration.

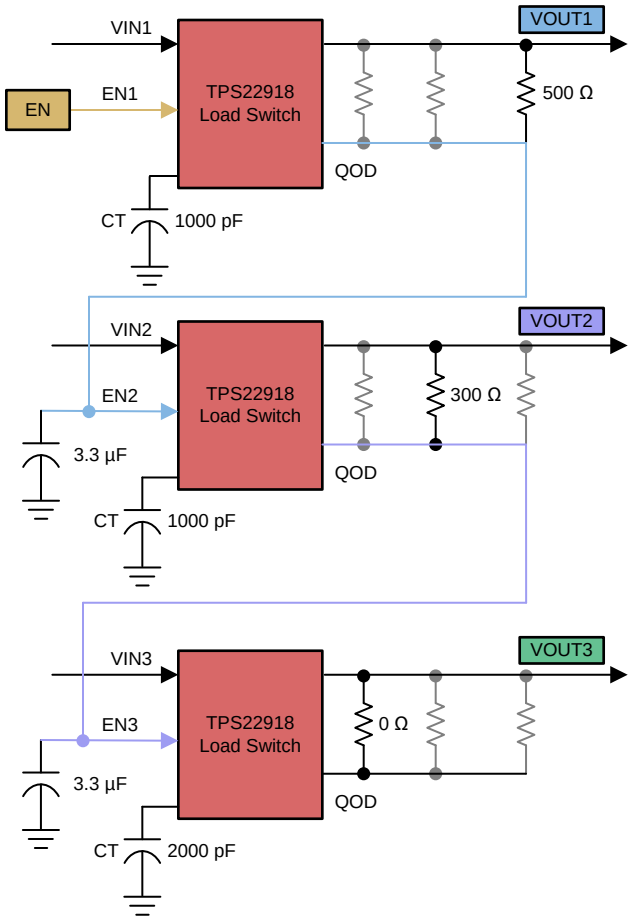

图 3. TIDA-01584 QOD Configuration Block Diagram

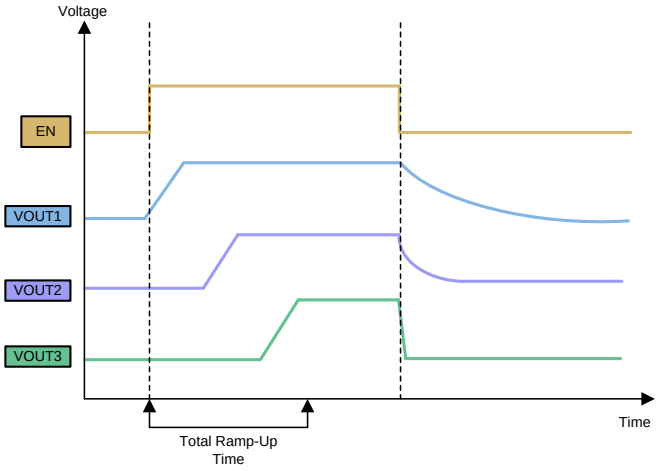

图 4. QOD Configuration Expected Behavior

图 5 shows the independent GPIO configuration. All three voltage channels are kept separated, and power-up timing is achieved by using separate control signals for each switch.

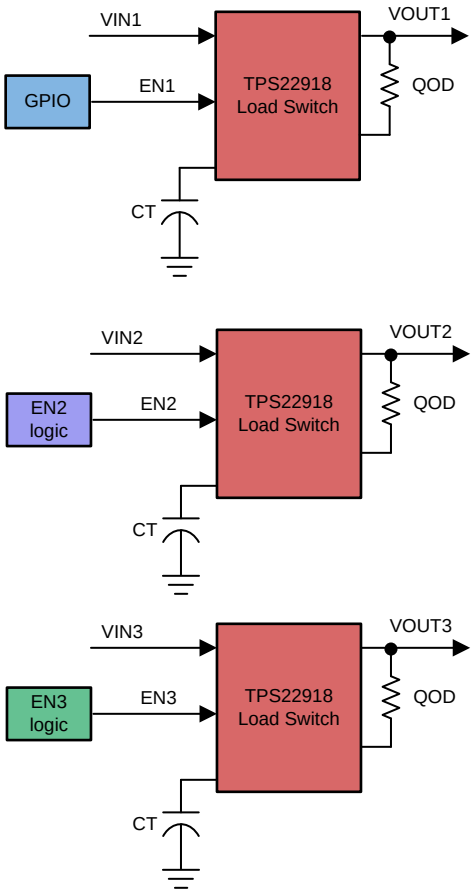

图 5. TIDA-01584 Independent GPIO Configuration Block Diagram

2.2 Design Considerations

2.2.1 Configurable Timing Adjustments

This section gives general calculations for determining timing parameters. Note that the specific timing parameters of load switches can vary depending on the *operating conditions of the system* and *load specifications*. To learn more about other timing considerations and specifications, refer to *Timing of Load Switches Application Report*[2].

For the CT configuration, the start-up sequencing can be changed by adjusting the CT capacitance of each load switch. The CT capacitor charges up shortly after the switch is turned on and remains high until V_{OUT} becomes stable. Once V_{OUT} reaches a stable value, the capacitor discharges to ground. Using the TPS22918, the approximate formula for the relationship between C_T and the slew rate is shown in 公式 1.

$$SR = 0.55 \times CT + 30 \quad (1)$$

Where:

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)

- The units for the constant 30 are µs/V.
- The units for the constant 0.55 are µs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. Rise time is defined as the total time it takes for the output voltage to rise from 10% to 90% of its final value. The slew rate equation accounts for this percentage, so no additional calculations are necessary. 表 2 contains test data measured on a TPS22918.

表 2. Rise Time Table for TPS22918(1)

CT (pF)	RISE TIME (µs) 10% to 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1 V
0	135	95	75	60	50	45	40
220	650	455	350	260	220	185	160
470	1260	850	655	480	415	340	300
1000	2540	1680	1300	960	810	660	560
2200	5435	3580	2760	2020	1715	1390	1220
4700	12050	7980	6135	4485	3790	3120	2735
10000	26550	17505	13460	9790	8320	6815	5950

(1) Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on C_T.

The QOD configuration highlights another way to change the ramp-up time. Introducing an external RC delay between each of the load switches allows each voltage rail to ramp up with the same slew rate though delayed. The reference uses 10-µF external capacitors to control the RC delay, but these capacitors can be changed to fit different timing parameters. The voltage on the external RC capacitor, and in turn, the voltage on the enable pin of the next load switch can be calculated by 公式 2.

$$V_{ON\_2} = V_{OUT\_1} \times e^{\frac{-t}{T}} \quad (2)$$

Where:

- V_{ON_2} is the voltage across the enable pin of the next load switch (V)
- V_{OUT_1} is the voltage on the output of the first load switch (V)
- t = time since previous output rail reached 90%
- T = time constant equal to $R_{QOD\_1} \times C_{external(3.3µ)}$

The power down timing is controlled by adjusting the QOD resistor. The QOD pin contains an internal resistor that connects to ground whenever the switch is disabled. If an external resistor is connected between the QOD pin and V_{OUT}, the discharge rate becomes based upon the added resistance. The fall times of the device depend on many factors, including the total QOD resistance, V_{IN} voltage, and the output capacitance. The approximate fall time of V_{OUT} can be calculated by using 公式 3.

$$V_{OUT} = V_{IN} \times e^{\frac{-t}{T}} \quad (3)$$

Where:

- V_{OUT} is the output voltage of the load switch (V)
- t = time since enable disconnect
- T = time constant equal to $R_{QOD} \times C_{LOAD}$

表 3. QOD Fall Times for TPS22918(1)

V_{IN}(V)	FALL TIME (µs) 90% to 10%, C_{IN} = 1 µF, I_{OUT} = 0 A , V_{ON} = 0 V, T_A = 25°C		
	C_L = 1 µF	C_L = 10 µF	C_L = 100 µF
5.5	42	190	1880
5	43	200	1905
3.3	47	230	2150
2.5	58	300	2790
1.8	75	430	4165
1.2	135	955	9910
1	230	1830	19625

(1) Typical values with QOD shorted to V_{OUT}.

During unexpected system power loss, load switches can maintain graceful power down sequencing. QOD dissipates power when Vin is unexpectedly grounded. If ON is also disabled when Vin is removed, the body diode in the load switch dissipates power. When selecting the appropriate C_{OUT} and R_{QOD} values for the sequence, be sure to check if there are voltage or timing margins that must be maintained during power down. Refer to 资源 data sheets for more information about power sequencing timing parameters.

2.2.2 Design Flexibility

Although the reference design testing was completed using the TPS22918, power sequencing can still be achieved by using other pin-to-pin load switches. Timing constraints are different for each load switch due to input voltage, internal resistance, current range, internal QOD, and other factors.

If the application requires higher voltage rails up to 18 V, the TPS22918 can be swapped for the TPS22810. Because both devices are pin-to-pin compatible, the device can easily be swapped out to achieve higher voltage application.

If the power sequencing application requires higher current power rails, the TPS22975 can be used. Although the TPS22975 does not contain an adjustable QOD pin, power-down sequencing can still be achieved with the internal 230-Ω resistor. The TPS22975 can support higher current up to 6 A.

The TPS22917 contains similar features as the TPS22918 with the added benefit of reverse current protection. Current protection ensures that no current can flow from the load back to the power supply during a short or fault event. The TPS22917 also contains a PMOS architecture and low leakage current (quiescent current). This makes the TPS22917 ideal for power sequencing solutions with battery operation or for applications with a goal of power loss reduction.

表 4. Load Switches for Power Sequencing

DEVICE	RECOMMENDED VOLTAGE RANGE	MAXIMUM CURRENT	R_{ON}	ADJUSTABLE QUICK OUTPUT DISCHARGE	REVERSE CURRENT BLOCKING
TPS22918	1 V to 5.5 V	2 A	52 mΩ at 5 V	✓	—
TPS22810	2.7 V to 18 V	2 A	79 mΩ at 12 V	✓	—
TPS22975	0.6 V to 5.7 V	6 A	16 mΩ at 5 V	—	—
TPS22917	1 V to 5.5 V	2 A	80 mΩ at 5 V	✓	✓

2.2.3 Total Solution Size and GPIO Control

As designs are continually getting smaller and sleeker, designs require a more space-conscious layout. By using integrated load switches for power sequencing, the system remains as compact and space efficient as possible. *Selecting a Load Switch to Replace a Discrete Solution Application Report*[3] provides a comparison between discrete and integrated load switches and highlights differences in size comparison and protection features.

Power sequencing traditionally requires processor intervention to control multiple enable pins or external oscillators to sequence multiple power rails. Some designs also contain external SVSs or digital clocks to enable each power rail. This reference design can sequence power rails with a single enable pin and a few resistors and capacitors, which reduces the solution size, cost, and number of GPIO inputs.

2.3 Highlighted Products

2.3.1 TPS22918

The TPS22918 is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high-current rails, the device implements a low-resistance N-channel MOSFET, which reduces the dropout voltage across the device. The device has a configurable slew rate that reduces or eliminates power supply droop due to large inrush currents. The device also features a QOD pin, which allows for the configuration of the discharge rate of VOUT. QOD occurs when the switch is disabled. The device has very-low leakage currents during shutdown, which also helps mitigate leakage for downstream modules during standby. The integrated control logic, driver, charge pump, and output discharge field-effect transistor (FET) eliminates the requirement for any external components, which reduces solution size and bill of materials (BOM) count.

2.3.2 TPS22810

The TPS22918 is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device. The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the requirement for any external components, which reduces solution size and BOM count.

2.3.3 TPS22975

The TPS22975 device is a single-channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an N-channel MOSFET. The device has a configurable slew rate for applications that require a specific rise-time. The device prevents downstream circuits from pulling high standby current from the supply by limiting the leakage current of the device when it is disabled. The integrated control logic, driver, power supply, and output discharge FET eliminates the requirement for any external components, which reduces solution size and BOM count.

2.3.4 TPS22917

The TPS22917 is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance P-channel MOSFET which reduces the drop out voltage across the device. The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the requirement for any external components, which reduces solution size and BOM count.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 System Overview

The different modes of operation in the power sequencing reference design can accommodate different system requirements. The CT configuration is a space-conscious layout that only uses external CT and QOD components to achieve power sequencing. The QOD configuration enables faster switching configurations. The external RC delay can be adjusted across a large range of values without impacting the slew rate of the voltage rail. This is useful in applications where one power rail needs to be fully on before the second rail starts turning on.

The terminal connectors on the left side of the board serve as input voltage connections for the three load switches. Test points TP1, TP12, and TP15 can also be used to supply voltage to each load switch. Jumpers JP3 and JP9 can be inserted to enable the same voltage level across all three load switches. The TPS22918 can support input voltages from 1 V to 5.5V, but the switches can be swapped out for the TPS22810 to support higher voltage applications.

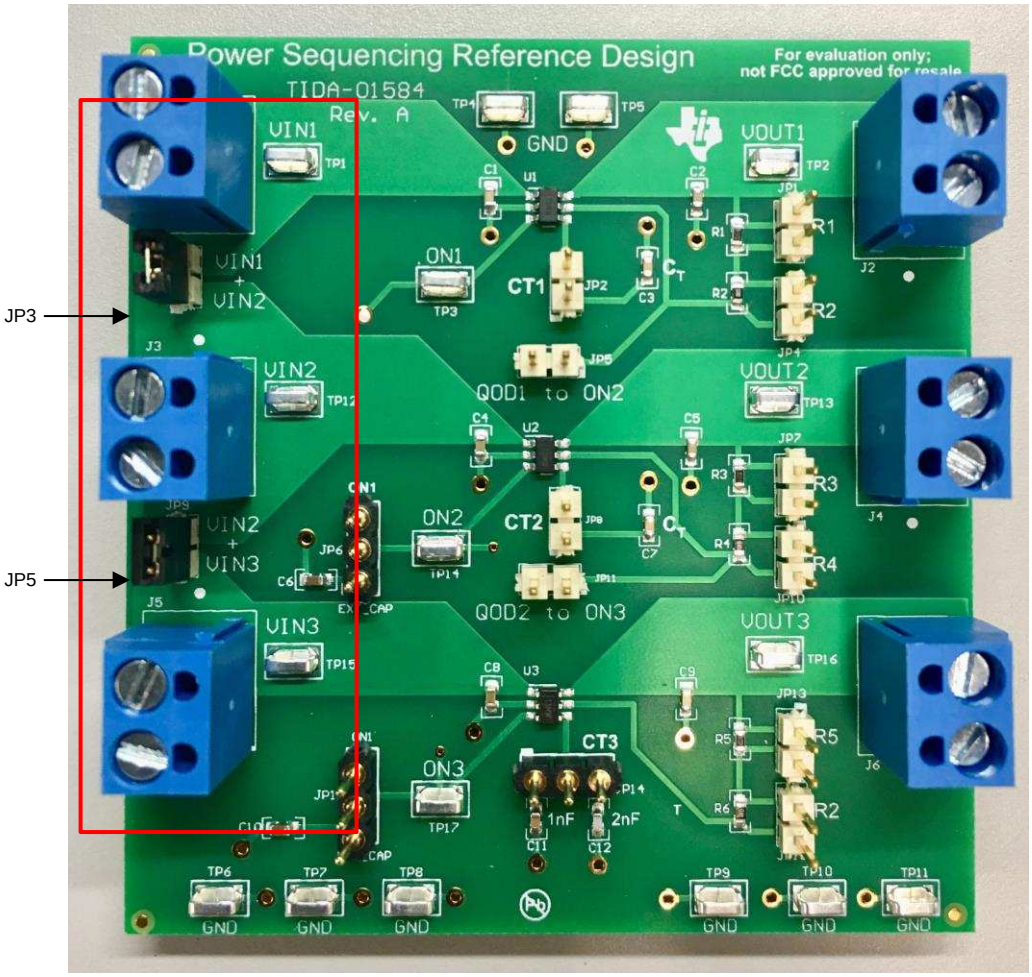

图 6. Input Connections

The terminal connectors on the right side of the board serve as output load connections for the three load switches. 图 7 the test points TP2, TP13, and TP16 that can also be used as VOUT connections. An external 10-µF capacitor was connected to each output during testing to replicate load capacitance.

Test points TP3, TP14, and TP17 are connected to the ON pins of the load switches. ON is an active high enable for each load switch that activates with standard GPIO logic thresholds. The pin can be driven with input above 1 V for the TPS22918 and TPS22917 or 1.2 V for the TPS22975 and TPS22810.

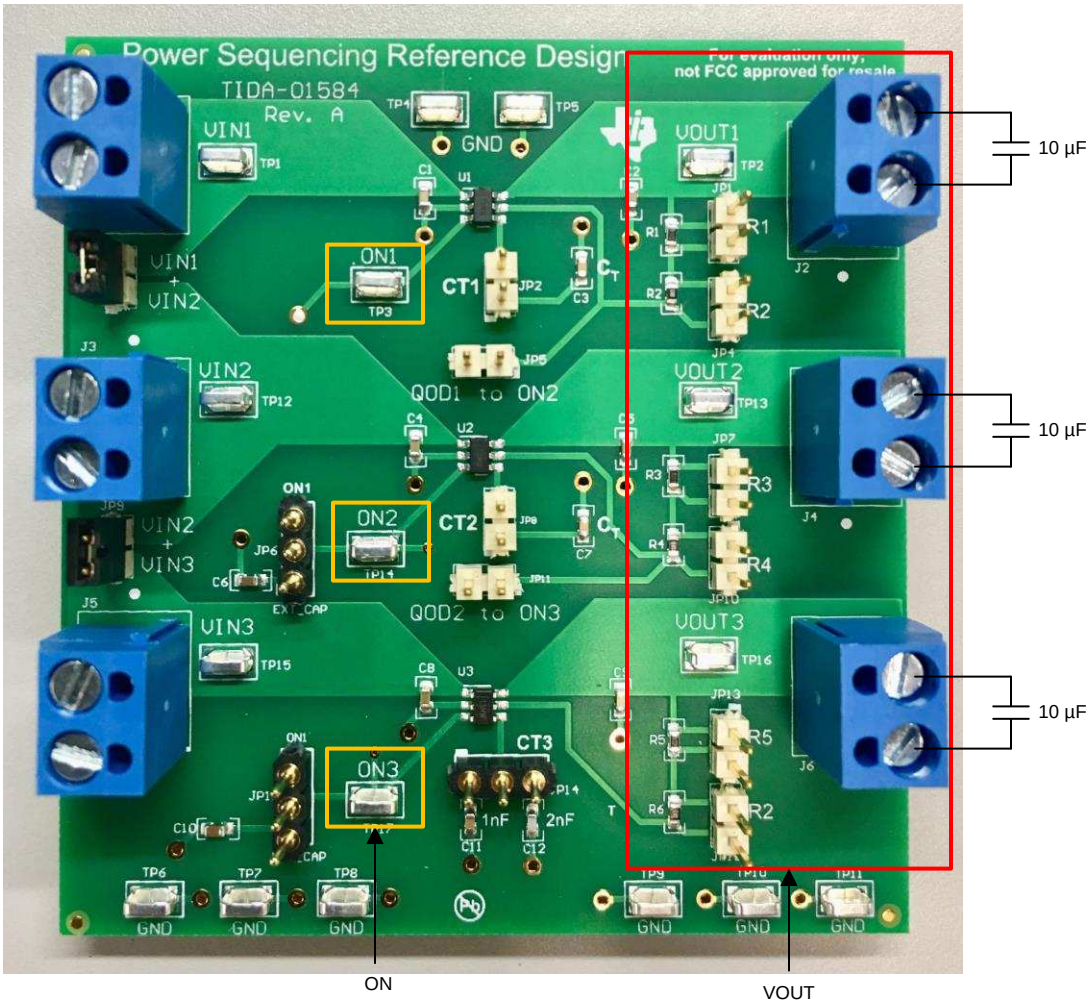

图 **7. Output Connections and Enables**

The CT jumpers, located at JP2, JP8, and JP14, control the CT capacitance of the three load switches. The top two load switches can be connected to 1000-pF capacitors, and the bottom load switch can be connected to 1000-pF or 2000-pF capacitors, which are useful for the CT configuration of power sequencing. These values can be changed by re-soldering different capacitors onto the board.

QOD pulls the output to ground whenever the device is turned off. The TPS22918, TPS22810, and TPS22917 contain adjustable QOD resistance by connecting an external resistor to VOUT. The total QOD resistance is the external value plus the internal QOD resistance. In 图 8, the external QOD resistance is 500 Ω if the top jumper is connected. If the bottom jumper is connected, the external QOD resistance is 300 Ω. If both jumpers are connected, neither external resistor is used, and the overall QOD resistance is the internal QOD resistance.

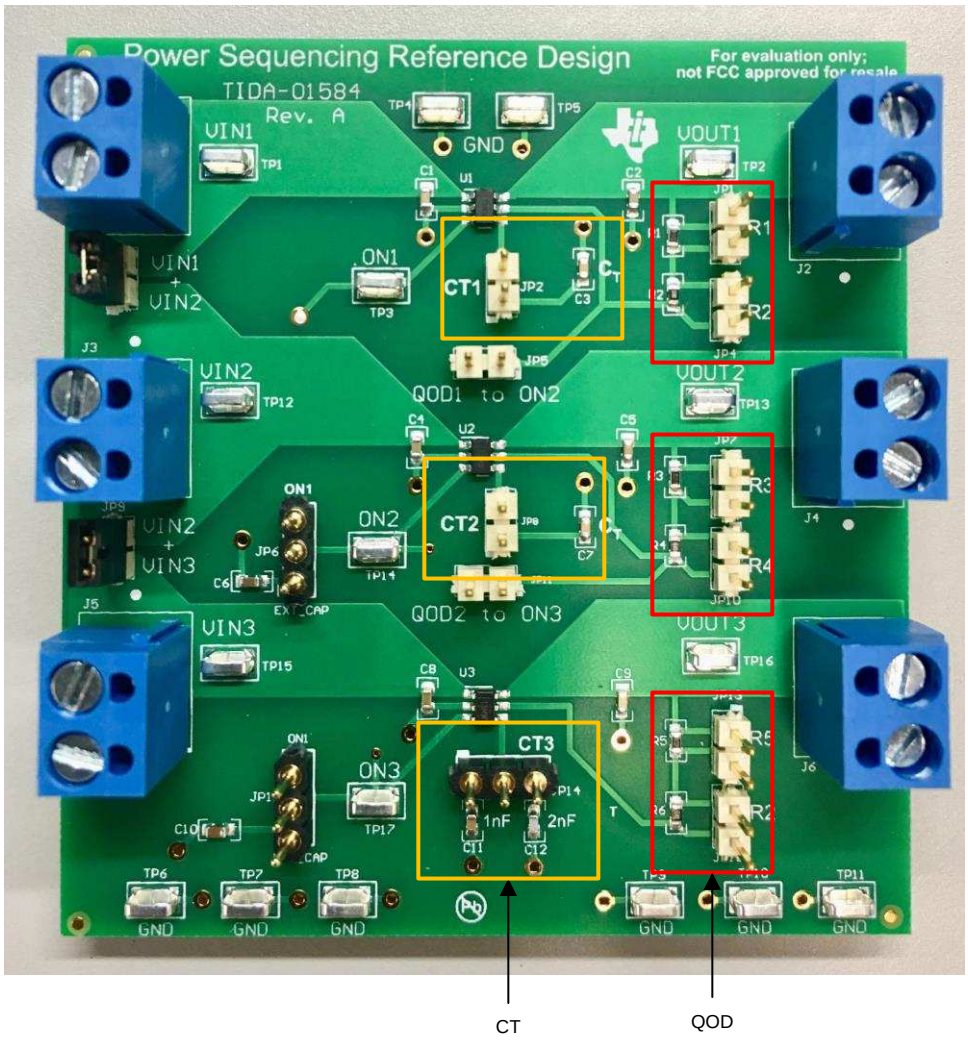

图 8. CT and External QOD Pins

JP5 and JP11 on 图 9 can be used to enable the QOD configuration. Connecting these jumpers routes the QOD output of the previous load switch into the ON pin of the next load switch.

JP6 and JP12 are 3-pin connectors. By connecting jumpers in the top position in the CT configuration, the ON pins of the load switches connect together. By connecting jumpers in the bottom position in the QOD configuration, the ON pin routes to an external capacitor.

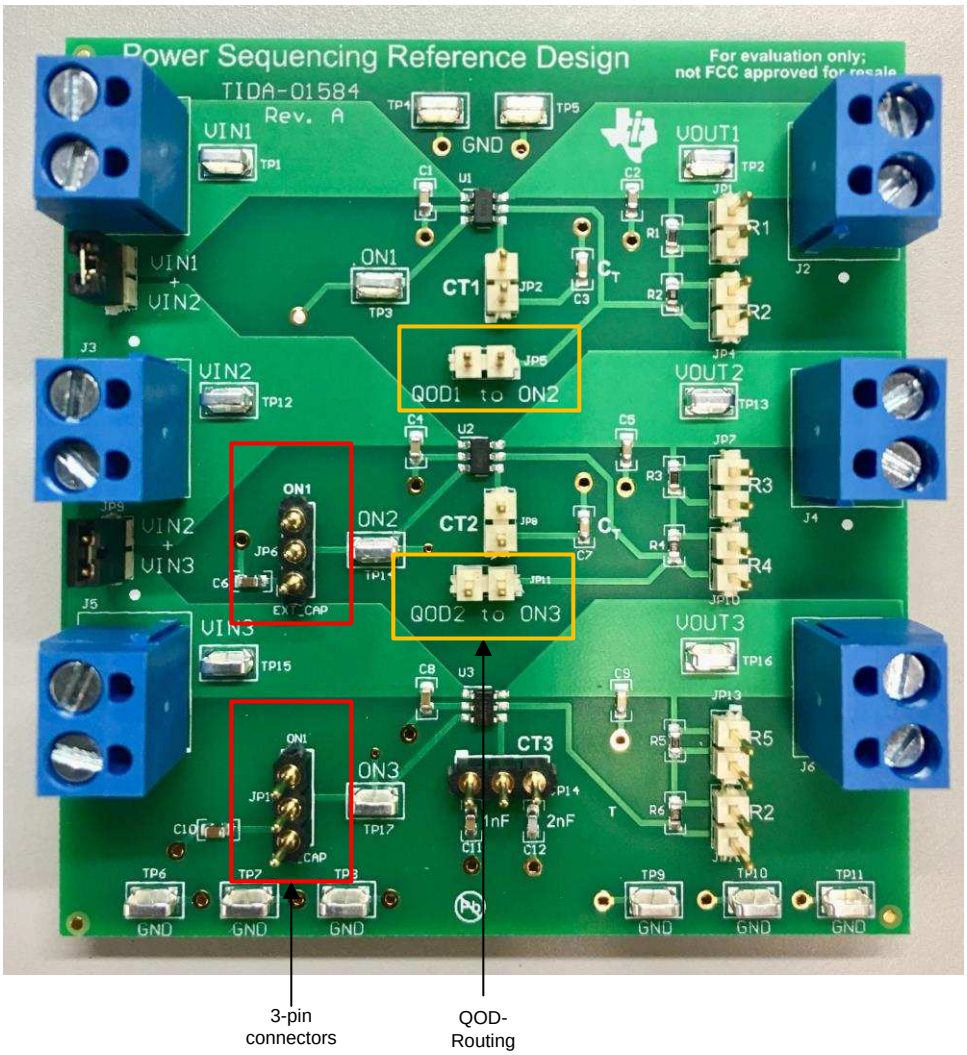

图 9. QOD Routing and External Cap Jumpers

3.1.1.2 Configuration Setup

3.1.1.2.1 CT Configuration

To configure the reference in the CT configuration, connect the jumpers as shown in 图 10. Make sure that the jumpers on the 3-pin headers are in the top position to connect the enables together and that the CT jumpers are configured as shown to achieve different rise times.

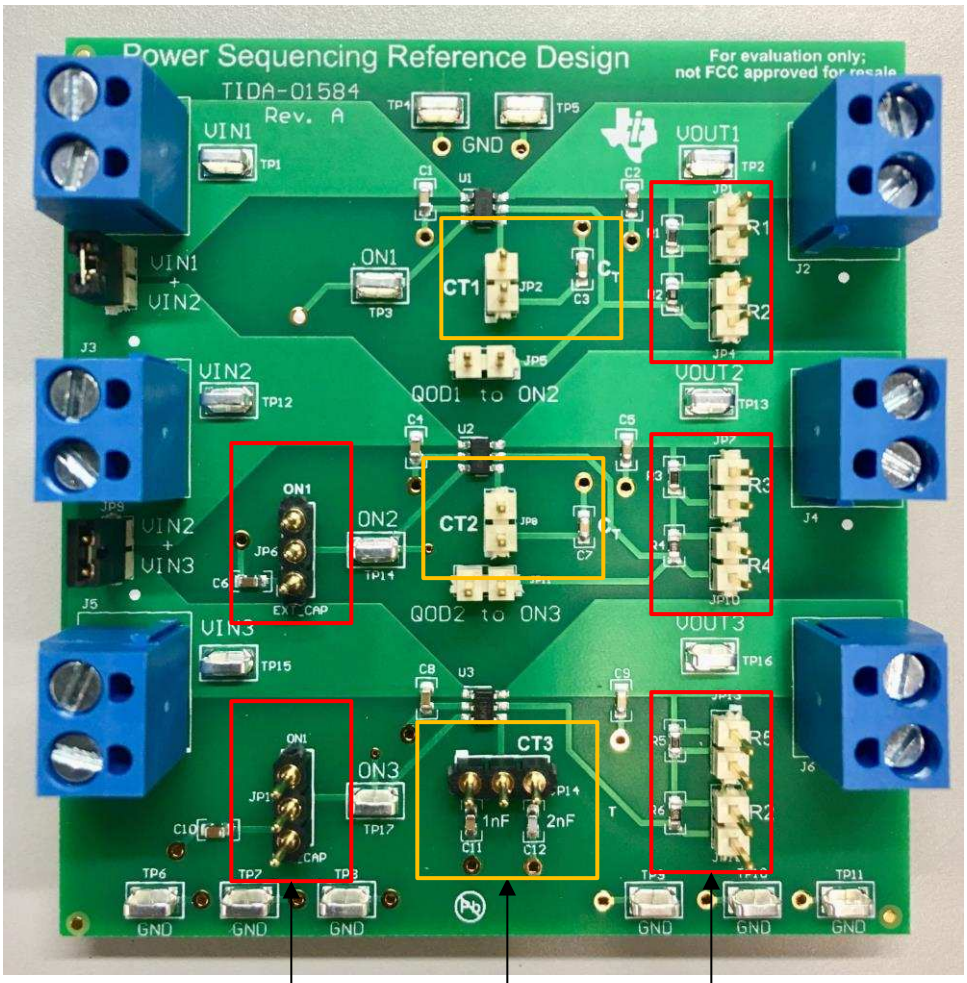

图 10. CT Jumper Configuration

3.1.1.2.2 QOD Configuration

To configure the reference design in the QOD configuration, connect the jumpers as shown in 图 11. Make sure that the jumpers on the 3-pin headers are in the bottom position to connect the ON pins to the external charging capacitors. Connect the QOD-routing jumpers to enable the RC delay between the load switches. Finally, connect the CT pins to the correct jumpers to enable the same rise time across all three load switches.

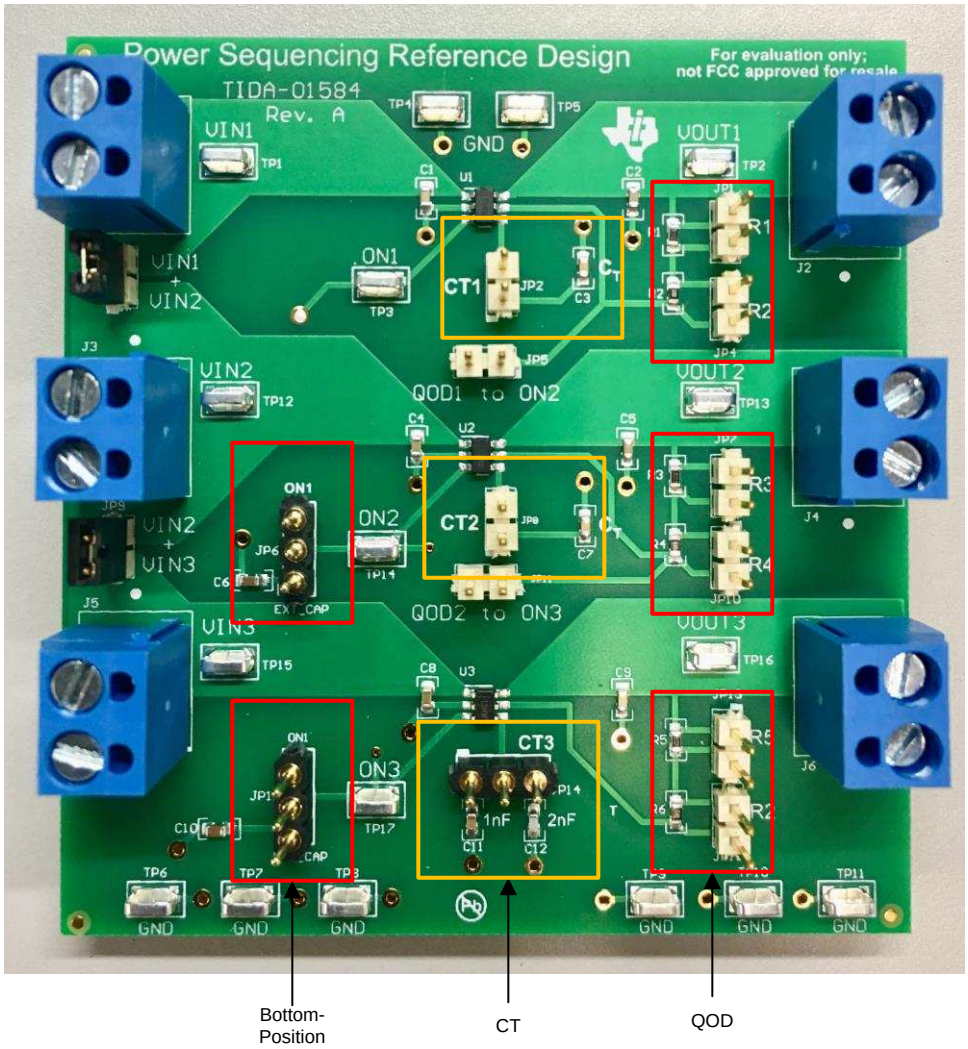

图 11. QOD Jumper Configuration

表 5. Jumpers or Connectors Summary(1)

DESCRIPTION	JUMPER OR CONNECTOR	CT CONFIGURATION	QOD CONFIGURATION
CT capacitors	JP2, JP8, JP14	OFF, ON, ON (right Position)	ON, ON, ON (left position)
QOD routing jumpers	JP5, JP11	OFF	ON
External three-pin jumper	JP6, JP12	ON (top position)	ON (bottom position)
QOD resistors	R1, R2, R3, R4, R5, R6	—	—
VIN voltage bridge jumpers	J3, J9	—	—

(1) — is not dependent on configuration

3.2 Testing and Results

3.2.1 Test Setup

Testing was completed in a lab using a power supply and oscilloscope. The ON pin was toggled using a function generator pulse, and 10-µF capacitors were used as output load capacitance. The rise time of the voltage rail was taken by measuring the time between 10% to 90% of the final value. Fall time was measured in the same manner. For power-down sequencing, external resistors were connected to the QOD pins. The first load switch contained 524 Ω (500-Ω external + 24-Ω internal pulldown), the second load switch contained 324 Ω, and last load switch only used the internal 24-Ω pulldown.

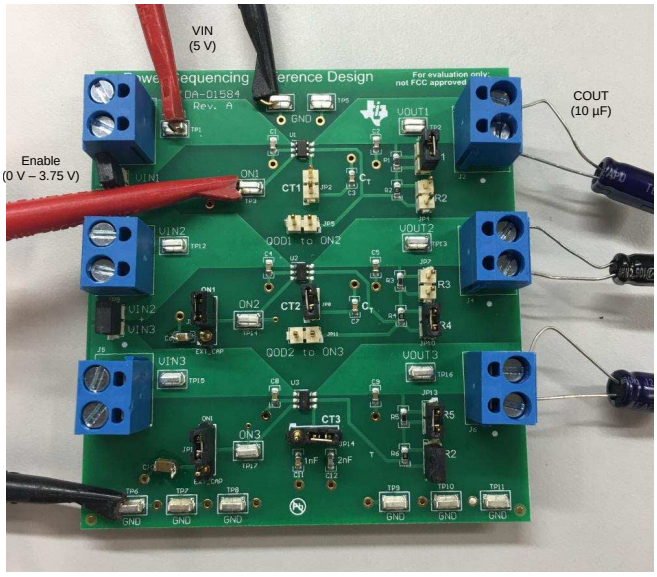

图 12. Input Connections for CT Configuration

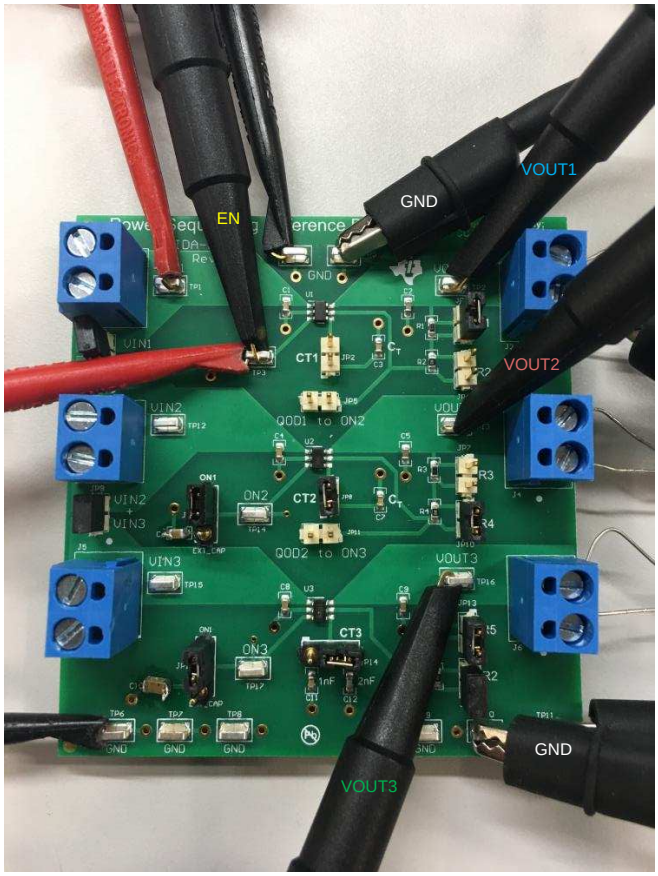

图 13. Oscilloscope Connections for CT Configuration

表 6. Test Conditions

TEST CONDITION	PARAMETER VALUE
Input voltage	5 V
ON pin voltage	0 V to 3.75 V square pulse
Ambient temperature	20°C
C_{OUT}	10 µF per channel
Output QOD resistance	524 Ω, 324 Ω, 24 Ω
Oscilloscope channel one	ON (yellow)
Oscilloscope channel two	VOUT1 (blue)
Oscilloscope channel three	VOUT2 (purple)
Oscilloscope channel four	VOUT3 (green)

3.2.2 Test Results

3.2.2.1 CT Configuration Results

In the CT configuration, the first load switch uses no CT capacitor, the second load switch uses a 1-nF capacitor, and the third load switch uses a 4.7-nF capacitor. The first load switch, without the CT pin, turned on in around 160 µs. The second load switch turned on in 3 ms, and the last load switch ramped up in 14 ms. Although all three of the load switches were enabled at the same time, the difference in slew rates created the differentiation in rise times.

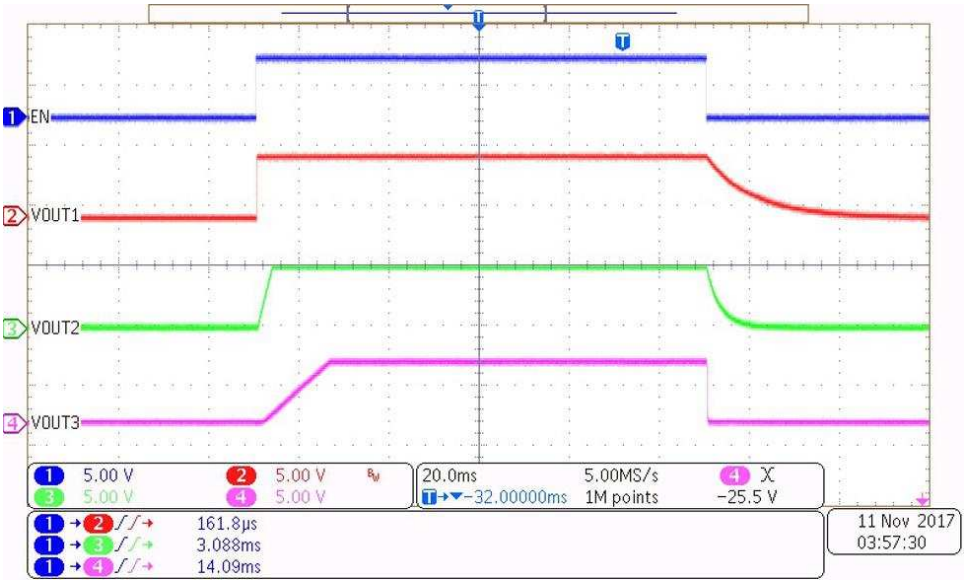

图 **14. CT Configuration Sequencing Event**

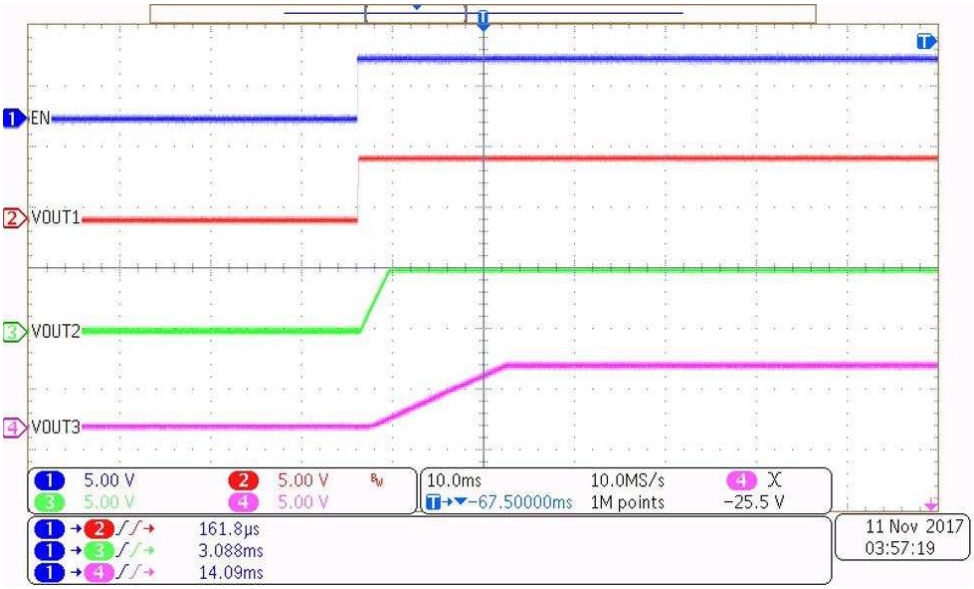

图 **15. CT Configuration Power-On Sequence**

3.2.2.2 CT Configuration Analysis

For space-constrained power sequencing applications, this configuration offers a compact sequencing design that does not require external ICs. By connecting the enable pins of the load switches together, this configuration offers a simple and smaller footprint. The linear slew rate control prevents inrush current from damaging downstream components. The slew rate equation is also easier to calculate; the timing delay increases linearly as the CT capacitance increases. By also controlling the timing with the CT capacitance, this keeps the timing parameters independent on the output load resistance and capacitance.

3.2.2.3 QOD Configuration Results

In the QOD configuration, all three load switches use a 1-nF capacitor on the CT pin, which keeps the slew rates the same. For the external RC delay, the first RC delay uses a 3.3-µF capacitor, and the second RC delay uses a 10-µF capacitor.

The first load switch, without any external RC delay, turned on in around 2.9 ms. The second load switch, with the 3.3-µF delay, turned on in 6.7 ms. The third load switch, with the external 10-µF capacitor, turned on in 9.1 ms.

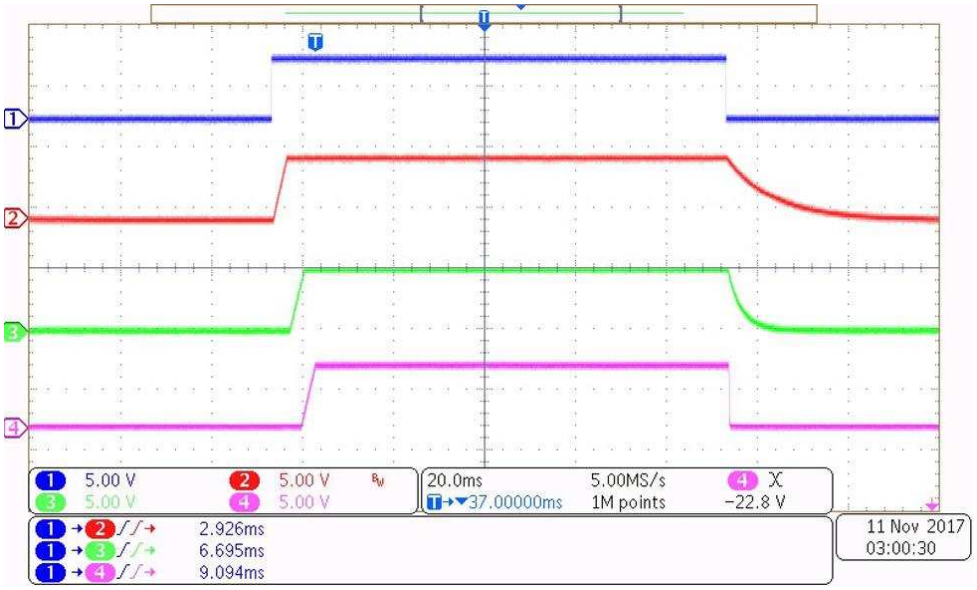

图 **16. QOD Configuration Sequencing Event**

图 17 shows that the previous voltage rail fully ramps up before the next voltage rail starts turning on.

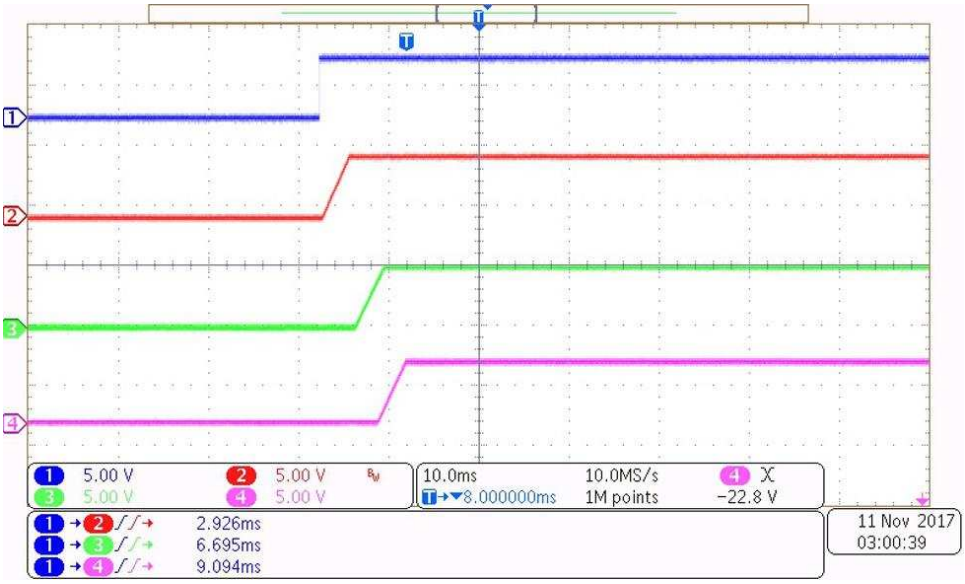

图 17. QOD Configuration Power-On Sequence

3.2.2.4 QOD Configuration Analysis

The external RC delay can be fine-tuned for precise timing adjustments or be configured to allow one voltage rail to turn on fully before the next voltage rail starts ramping up. These times can be critical in devices where one subsystem must fully turn on before the second subsystem can be turned on. The external RC delay also frees the C_T pin, which allows greater range on slew rate control. The configuration does not require an external IC or supervisor and only requires a single GPIO from the processor to sequence the power rails.

3.2.2.5 Power-Down Sequencing Results

Power-down sequences are not dependent on either turn-on sequence. By staying independent, the voltage rails and downstream subsystems can turn off in a different sequence than the turn-on sequence. This indepence allows for unique power sequencing arrangements. For example in 图 16, the QOD configuration is configured so VOUT3 voltage rail (green trace) turns on last but also turns off first.

图 18 shows a scope shot of a power-down sequence. The first load switch (VOUT1) connects a 500-Ω external resistor to the QOD pin, which contains an internal 24-Ω resistor. The second load switch (VOUT2) contains 324 Ω overall, and the third load switch, VOUT3, uses the internal 24-Ω resistor. As the resistance on the QOD pin increases, the time it takes for the voltage rail to power down increases.

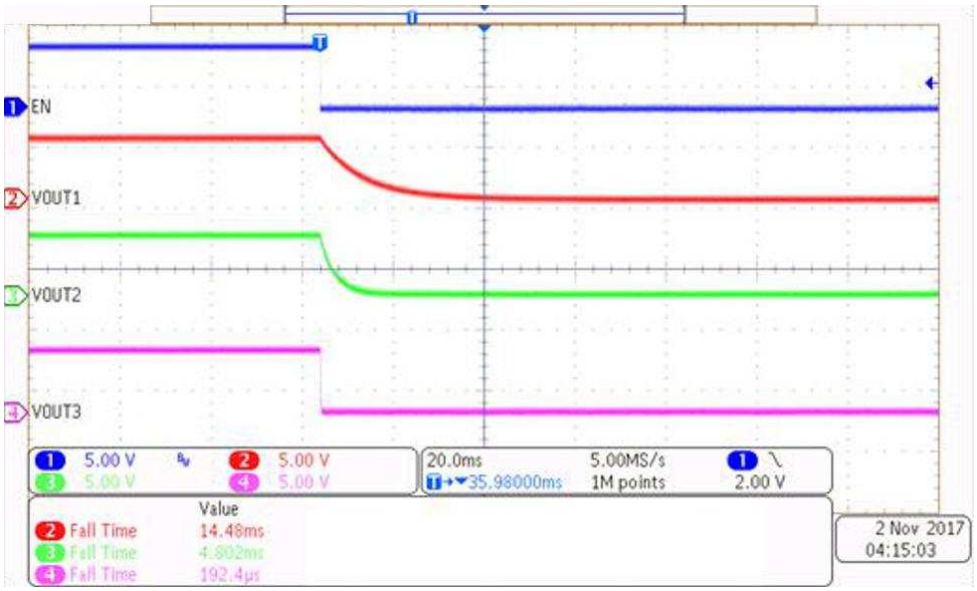

图 **18. Power Down Sequencing**

3.2.2.6 Further Tests

This design allows users to configure multiple power sequencing configurations that are not limited to just the CT configuration and QOD configuration. The jumpers can be configured to sequence rails in other configurations, such as the ones shown in 图 19 and 图 20.

In 图 19 the first rail is sequenced using the QOD configuration, and the last two load switches are sequenced using the CT configuration. All three load switches contain the same CT value, but the switches are sequenced so the first load switch turns on before the second and third load switches turn on in parallel. This configuration only requires one GPIO and can be expanded to incorporate more load switches.

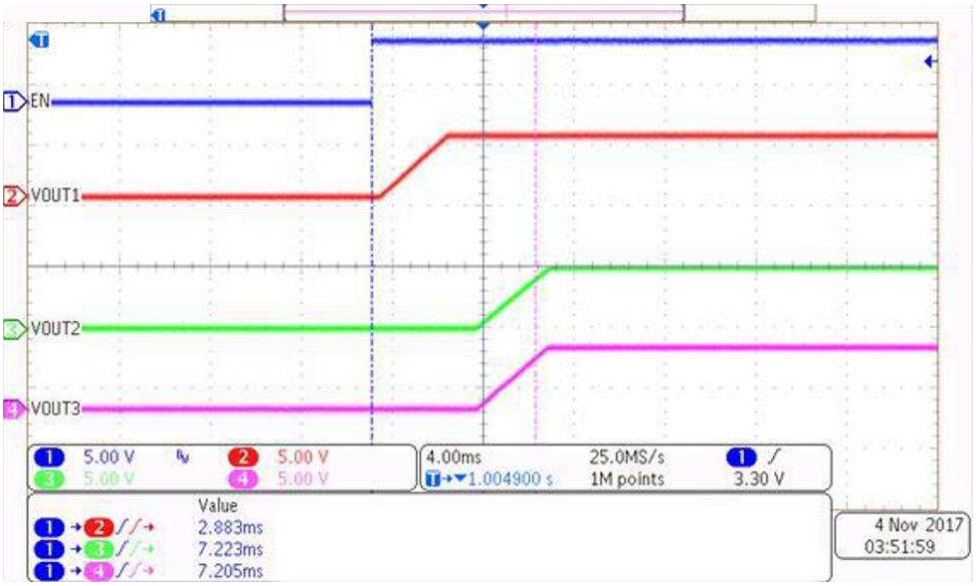

图 **19. Parallel Configuration One**

In 图 20 the first two load switches are connected with the CT configuration, and the third load switch is connected with the QOD configuration. Putting both designs together makes it possible to sequence load switches in many combinations depending on design specifications. Some voltage rails can turn on in parallel with each another while other rails turns on before or afterwards. This sequence can all be achieved by using a single GPIO, which frees up board space, processor intervention, and external ICs.

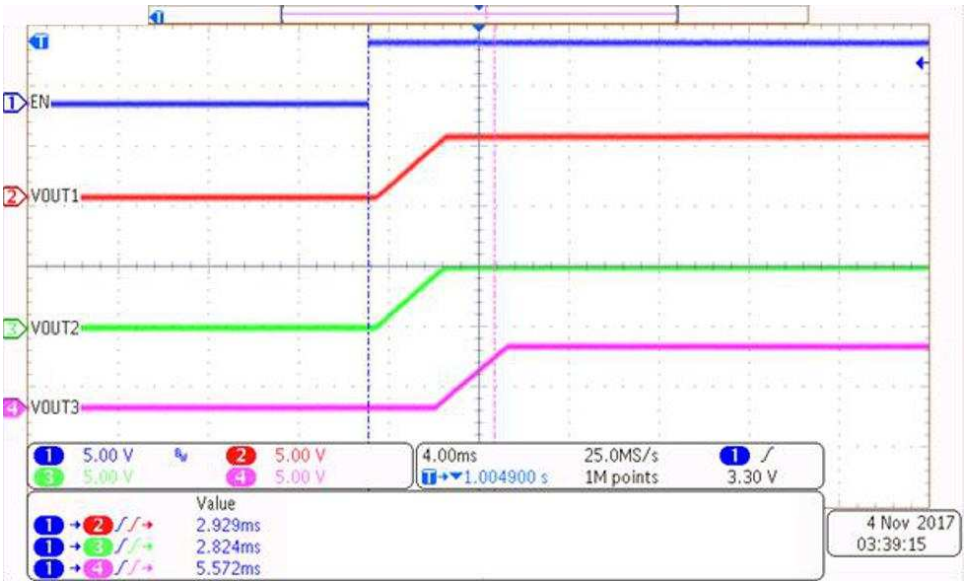

图 20. Parallel Configuration Two

Although most of the lab testing was completed using the TPS22918, power sequencing can still be achieved using other load switches. The reference design allows other pin-to-pin load switches to be used instead of the TPS22918. In 图 21 the testing was completed using the TPS22810 load switch. Timing will be different for the TPS22810, consult the device's data sheet for more specific information about timing requirements.

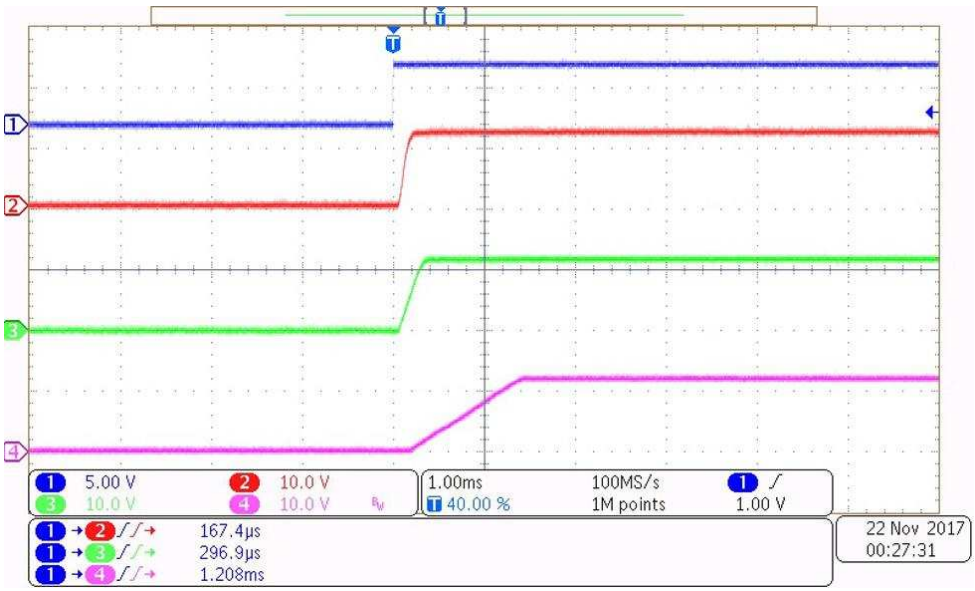

图 21. Power Sequencing Using TPS22810

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01584.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01584.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01584.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01584.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01584.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01584.

5 Software Files

To download the software files, see the design files at TIDA-01584.

6 Related Documentation

1. Texas Instruments, *Simple power-rail sequencing solutions for complex multi-rail systems*
2. Texas Instruments, *Timing of Load Switches Application Report*
3. Texas Instruments, *Selecting a Load Switch to Replace a Discrete Solution Application Report*

6.1 商标

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