TI Designs：TIDA-01056
*用于在最大限度地减小 **EMI** 的同时优化供电效率的 **20** 位 **1MSPS DAQ** 参考设计*

说明

该高性能数据采集 (DAQ) 系统参考设计优化了功率级，以降低功耗并最大程度地减小电磁干扰 (EMI) 的影响。通过使用 LMS3635-Q1 降压转换器，该设计实现了高效率（即使在轻负载情况下也是如此）和极低的 EMI（由于利用对称或蝴蝶布局的 HotRod™封装）。此外，由于 LMS3635-Q1 具有更低的开关频率，设计人员可以通过采用低压降线性稳压器 (LDO) 更有效地滤除输出电压纹波。与 LM53635 降压转换器相比，该参考设计可在轻负载电流下将效率提高 7.2%，从而实现 125.25dB 的无杂散动态范围 (SFDR)、99dB 的信噪比 (SNR) 和 16.1 的有效位数 (ENOB)。

资源

TIDA-01056	设计文件夹
LMS3635-Q1	产品文件夹
TPS7A47	产品文件夹

TI E2E™ Community

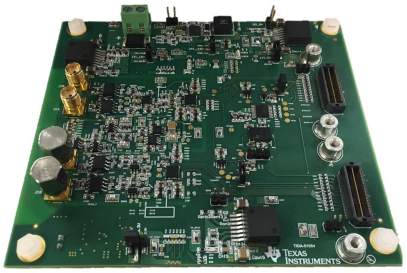
咨询我们的 E2E 专家

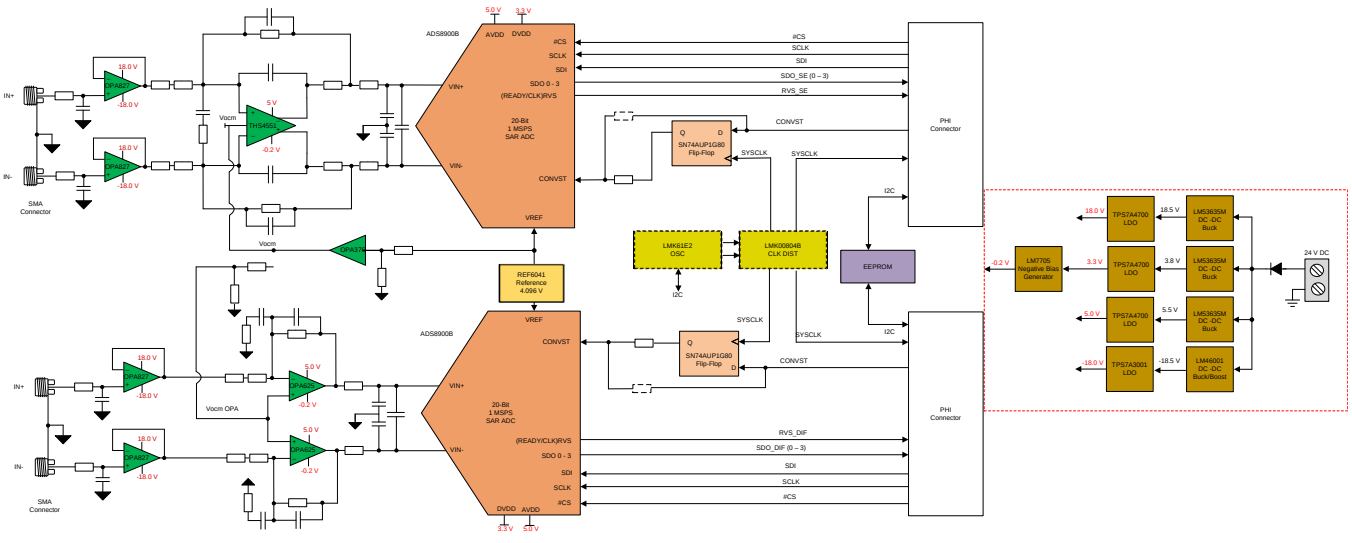
特性

- 电源设计可最大程度地减小直流/直流 EMI 对系统性能的影响
- 两个 20 位 SAR 模数转换器 (ADC) 通道
- 适用于高通道数系统（可重复）的模块化前端参考设计
- 高达 ±4V 的输入信号（$8V_{PP}$ 差动）

应用

- 数据采集 (DAQ)
- 半导体测试设备
- LCD 测试设备
- 实验室仪表
- 电池测试





1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for applications such as semiconductor tests, memory tests, liquid-crystal display (LCD) tests, and battery tests. In these systems, often hundreds or thousands of data channels are required; thus, maximizing SNR performance while minimizing power, component count, and cost are all key design criteria. These systems have some type of power generator that typically includes DC-to-DC converters to provide the voltage levels required to power each device in the analog front end (AFE). These converters have switching components that cause EMI emission and harm the system performance.

图 1 shows a block diagram of a generic AFE circuit.

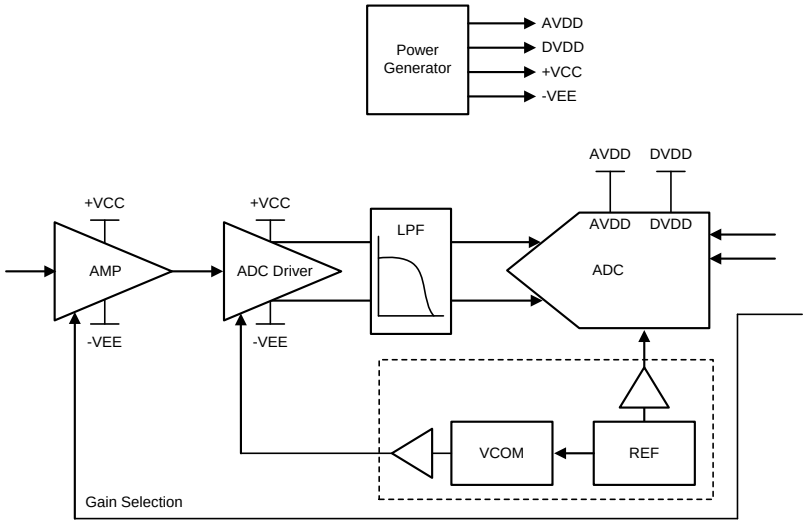


图 1. Generic AFE

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASUREMENT
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	8-V_{PP} fully differential	8-V_{PP} fully differential
Resolution	20 bits	20 bits
SNR	> 96 dB	99 dB
THD	< –120 dB	–126.7 dB
ENOB	> 16 bit	16.16 bits
System power	< 2.5 W	1.92 W
Form factor (L × W)	120 mm × 100 mm	112.98 × 99.82 mm

2 System Overview

2.1 Block Diagram

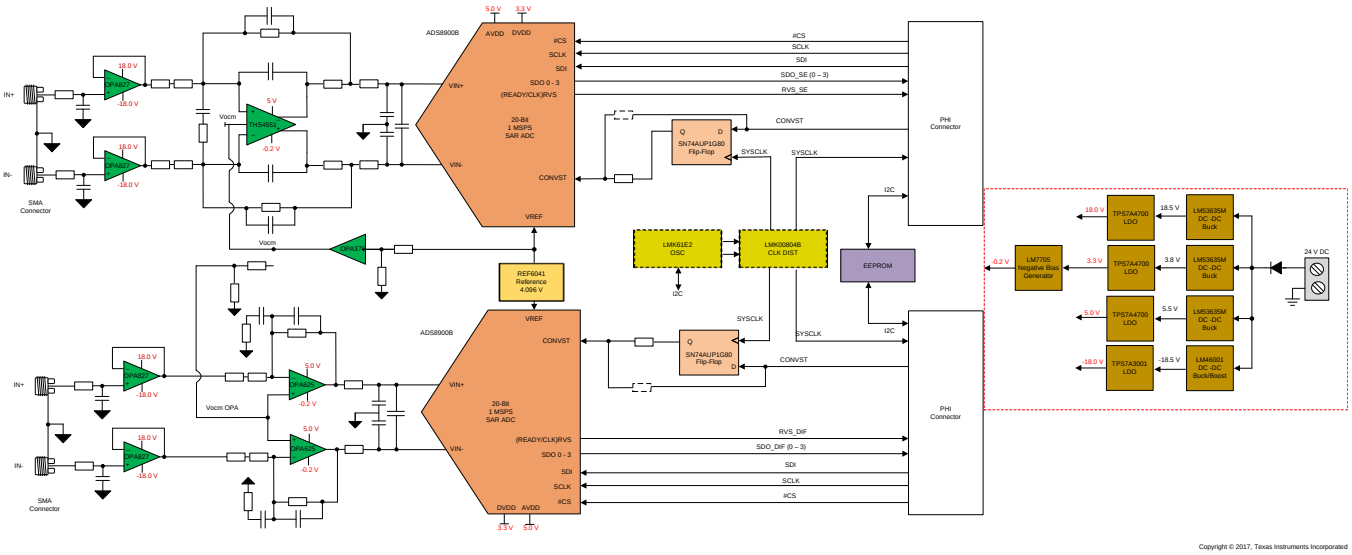


图 **2. TIDA-01056 System Block Diagram**

This reference design focuses on optimizing power supply efficiency while minimizing the effect of the EMI generated from the system buck converters powering the AFE and 20-bit, 1-MSPS successive approximation register (SAR) ADC. This design compares the efficiency of the LM53635 buck converter, which switches at 2.1 MHz and is used in this reference design, to the LMS3635 buck converter, which has a 400-kHz switching frequency. As both devices use the HotRod™ package and butterfly layout, designers can directly observe the effects of switching frequency on both EMI and efficiency.

2.2 Highlighted Products

2.2.1 LMS3635-Q1

The function of the LMS3635M in this design is to bring the 24-V input voltage down to 3.8 V, 5.5 V, and 18.5 V in a highly efficient manner. This part is selected based on its superior efficiency at light load, low switching frequency, excellent EMI performance, and compact printed-circuit board (PCB) layout. The automotive-qualified HotRod QFN package reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering EMI. Seamless transition between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) modes, along with a low quiescent current, ensures high efficiency and superior transient responses at all loads.

2.2.2 TPS7A47

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

2.3 System Design Theory

High-performance DAQ systems require low-power consumption while minimizing EMI from switching regulators to prevent from impacting the performance of high-resolution ADCs. The following subsection describes optimizing the power supply stage using the LMS3635-Q1 and provides measurement results and a comparison of the efficiency, SNR, total harmonic distortion (THD), and SFDR.

2.3.1 AFE and SAR ADC

This reference design consists of an AFE with two channels. Both channels are similar, with the exception of the ADC driver architecture. The first channel uses the THS4551, a fully differential amplifier specifically designed to be used with high-performance SAR ADCs. The second channel uses dual OPA625 amplifiers, which are wired to work as a fully differential amplifier. These amplifiers drive the ADS8900B SAR ADC, a 20-bit, high-precision, high-speed data converter. The AFE and SAR ADC are the key aspects of this design for working with DAQ systems; however, these devices are not the main focus of this design. To learn more about the design theory of the AFE and SAR ADC, see *ADC Driver Reference Design Improving Full-Scale THD Using Negative Supply*.

2.3.2 Power Structure

This system requires a wide variety of voltage rails to meet the specification of the reference design. The input voltage required for the system is 24-V DC. The power tree in 图 3 highlights the distribution of the power into the different required rails. To create these rails, this design contains the LMS3635-Q1 high-efficiency buck converter. This solution is compared to the LM53635 to show the improvement in efficiency.

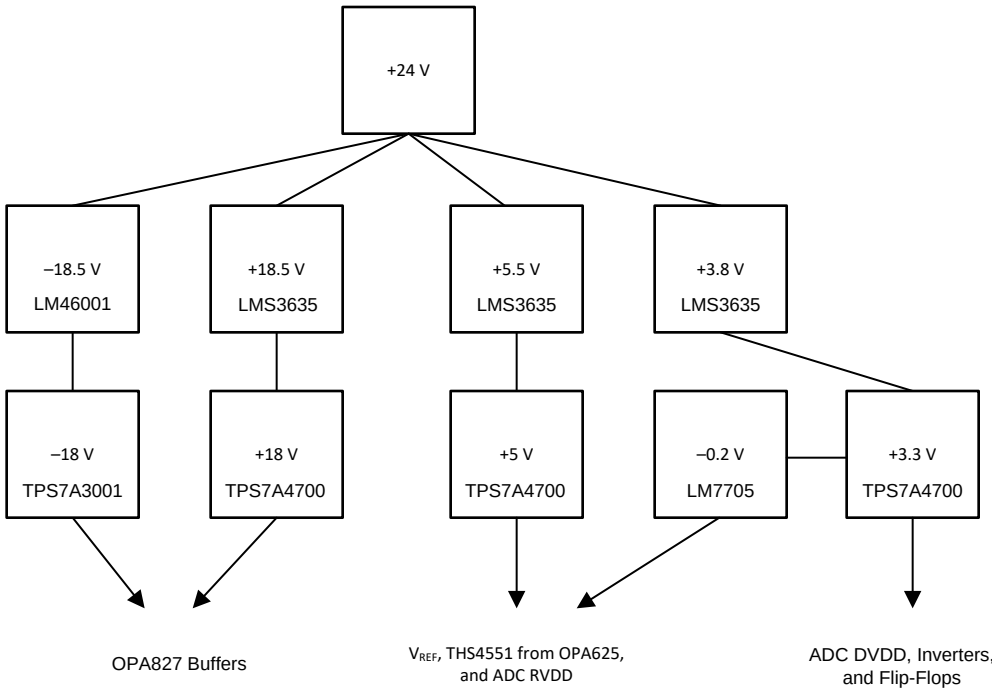


图 3. System Power Tree

2.3.2.1 LMS3635-Q1 Circuitry

图 4 shows the 18-V rail circuitry with the LMS3635-Q1; each rail is structured the same way, with the only difference being the different passive component values. The input of the buck is connected to the 24-V supply by a two-pin header. This header allows the user to leave unused bucks powered off, which is critical to the testing performed on the reference design. The buck converter is followed by an LDO to remove the switching noise. The input of the LDO is connected to a three-pin header. The other two pins of this header are connected to the outputs of both buck converter options. This header is used in conjunction with the two-pin header to properly connect the buck, for which the intention is to use with the LDO. The three-pin header allows the use of only one LDO for each rail, which improves space efficiency and also helps with certain aspects of testing and debugging.

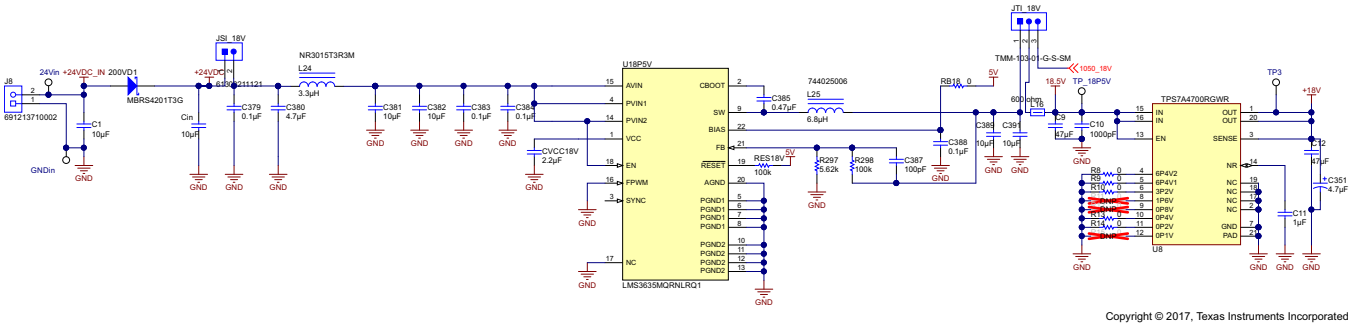


图 4. LMS3635-Q1 Schematic

2.3.3 LMS3635-Q1 Switching Noise

Buck converters produce output voltage ripple, which is also known as switching noise. Many different factors involving the switching regulator determine the amplitude of this ripple, which can be high enough to cause issues with devices powered by this buck converter. Because this reference design uses noise-sensitive devices such as the 20-bit ADC, a high-voltage ripple can have a detrimental effect on signal integrity. An LDO is placed at the output of the switching regulator to remove the switching noise and circumvent such an occurrence.

The following calculations and simulations show the importance of connecting the LDO to remove the switching frequency. The output voltage ripple and switching frequency (f_S) for the buck in the 5-V rail (the rail powering the RVDD of the ADC, V_{REF}, OPA625, and THS4551) was measured to be approximately 30 mV and 30 kHz (see 图 5 and 图 6, respectively).

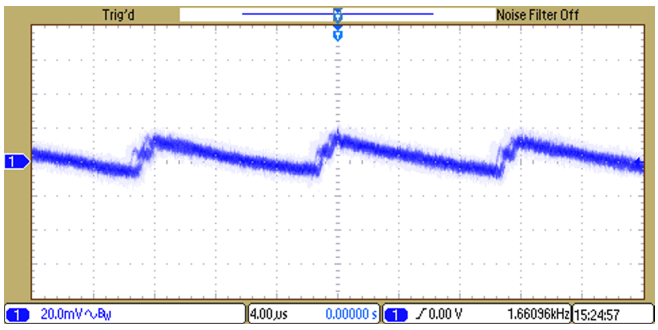


图 5. Output Ripple of LMS3635-Q1 (5-V Rail)

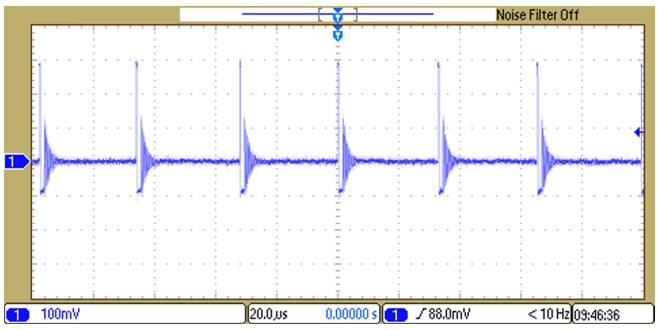


图 6. Switching Waveform of LMS3635-Q1 (5-V Rail)

The buck is designed to output 5.5 V, which is just above the dropout of the LDO, to minimize the efficiency loss. A TINA-TI™ simulation model is created for the TPS7A4700 LDO with a 5.5-V DC level and a sine wave input of 30 mV_{pk-pk}, 30 kHz (simulating the output of the LMS3635 device with ripple). A steady-state analysis provided the output of the LDO, which 图 7 shows.

As for the LM53635—because the output current of the 5.5-V rail is measured as 20 mA—its switching frequency must be around 70 kHz, as evidenced from the *Switching Frequency vs Load Current* graph in *LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter*. 图 8 shows the LDO simulation result, which was obtained under the same DC level and amplitude as the LMS3635 device.

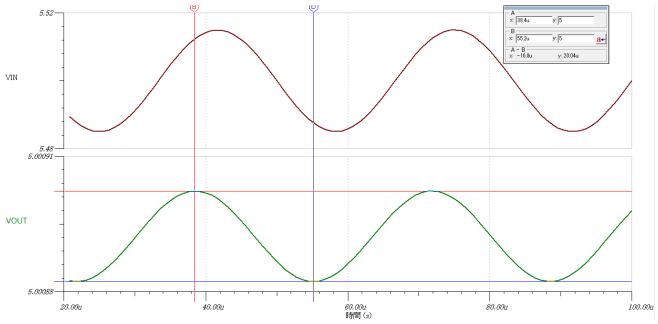


图 7. LDO Simulation V_{IN} from LMS3635 for 5-V Rail

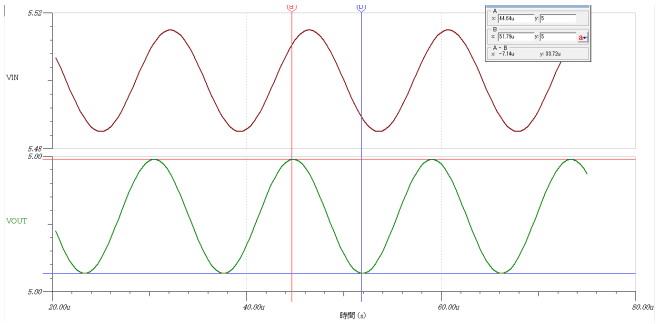


图 8. LDO Simulation V_{IN} from LM53635 for 5-V Rail

After the LDO, the peak-to-peak switching noise of the LMS3635-Q1 and LM53635 are 20.04 µV and 33.72 µV, respectively. Because the LDO has an improved power supply rejection ratio (PSRR) at lower frequencies (see 图 9), the ripple rejection of the LMS3635-Q1 (30-kHz switching) is 41% superior to the LM53635 (70-kHz switching). Thus, from a ripple and EMI perspective, the LMS3635-Q1 is more suitable for high-accuracy DAQ.

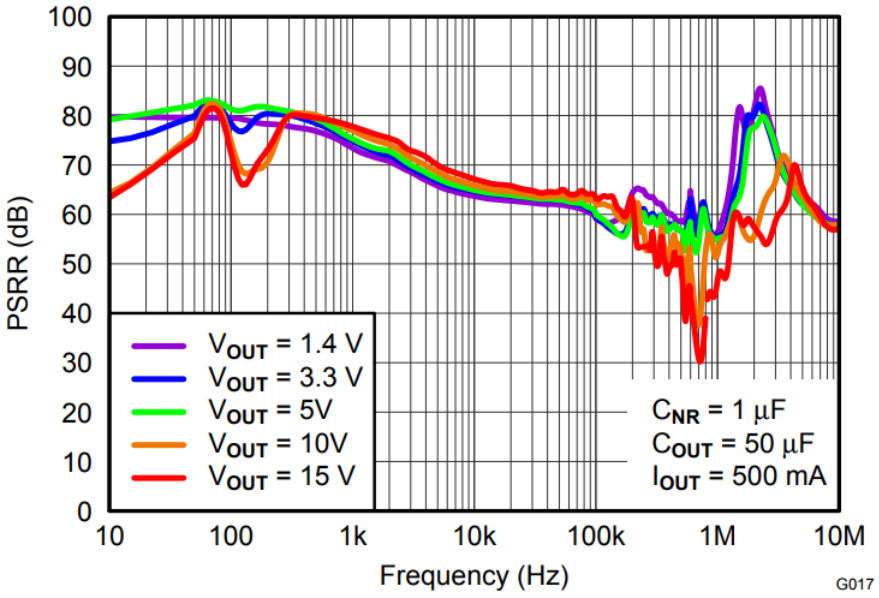


图 9. PSRR of TPS7A47x

The LDO effectively reduces the switching ripple noise by a factor of 1497. Further calculations are made to observe the noise present at the ADC using the output voltage ripple of the LMS3635-Q1 device. Compare this result to the result of using the output voltage ripple of the TPS7A4700 in the same calculations. This ripple voltage without the LDO goes to both the OPA625 and THS4551 devices. The THS4551 has a PSRR of 110 dB at 30 kHz and a gain of 1. 公式 1 shows that the PSRR is equal to:

$$PSSR(dB) = -20\log_{10}\left(\frac{\Delta V_{OS}}{\Delta V_{SUPPLY}}\right) \quad (1)$$

Because this system has a gain of 1, the total noise gain on the non-inverting terminal is 1 + 1. This is a gain of 6 dB. The total PSRR for the THS4551 is approximately 104 dB for this system. This value is equal to 0.00000631 V/V. The amount of power supply noise coupled to the ADC data lines is calculated using 公式 2:

$$30\ mV \times 0.00000631 = 189.3\ nV \quad (2)$$

Compare this noise value to the least significant bit (LSB) value of the ADC to observe the effect it has on signal integrity. Calculate the value of 1 LSB for a 20-bit differential input ADC with 4.096 V as a reference voltage using 公式 3 and 公式 4:

$$\frac{2 \times 4.096}{2^{20}} = 7.812\ \mu V \quad (3)$$

$$\frac{189.3\ nV}{7.812\ \mu V} \times 100 = 2.42\%\ LSB \quad (4)$$

Because the ADS8900B has a differential input, the full-scale input range (FSR) is twice the reference voltage. To determine the LSB of the differential input ADC, see the section regarding the *ADC Transfer Function* in *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features*. The OPA625 has a power supply rejection ratio of 77 dB at 30 kHz. At a gain of 1, the PSRR is equal to 71 dB. This value is equivalent to 0.00028 V/V. 公式 5 and 公式 6 calculate the power supply noise present at the ADC driven by the OPA625 device:

$$30\ mV \times 0.00028 = 8.46\ \mu V \quad (5)$$

$$\frac{8.46\ \mu V}{7.812\ \mu V} \times 100 = 108\%\ LSB \quad (6)$$

With a 2.42% LSB present at the ADC, the THS4551 signal chain is not greatly impacted by excluding the LDO. However, the OPA625 signal chain has more than 1 LSB of power supply noise present at the ADC without the LDO. This above 1 LSB noise value causes missing code and creates a huge negative impact on the output data of the ADC. Using the LDO output ripple of 20.04 µV and the same equations, the amount of power supply noise coupled to the ADC data lines for the ADC driven by the THS4551 is:

$$20.04\ \mu V \times 0.00000631 = 126.4\ pV \quad (7)$$

$$\frac{126.4\ pV}{7.812\ \mu V} \times 100 = 0.0016\%\ LSB \quad (8)$$

This highlights that the amount of noise on the 5-V rail is much less than 1% of the LSB value of the ADC. The amount of power supply noise present at the ADC of the OPA625 is:

$$20.04\ \mu V \times 0.00028 = 5.65\ nV \quad (9)$$

$$\frac{5.65\,\text{nV}}{7.812\,\mu\text{V}} \times 100 = 0.072\%\,\text{LSB} \tag{10}$$

When using the LDO, both the THS4551 and OPA625 signal chain ADCs have much less than 1% LSB of noise present at their power supply inputs. This specification ensures that there is no negative impact on signal integrity with the LDO present in the system. This test concludes that the LDO is necessary in the power rail circuits to generally remove any system performance degradation as a result of switching noise.

2.3.4 LMS3635-Q1 EMI

One of the goals for this design is to eliminate any system performance degradation due to EMI for high-performance DAQ systems. Buck converters are the main source of unwanted spur production throughout the spectrum due to their harsh switching components. The LMS3635-Q1 is a great solution for this problem because many of its features focus on reducing EMI.

2.3.4.1 HotRod™ Packaging

The biggest factor that helps the LMS3635-Q1 reduce EMI is the HotRod Flip-Chip-on-Leadframe (FCOL) packaging, which 图 11 shows. This package style flips the die over and uses copper bumps to connect directly to the leads, thus eliminating the requirement for a wire bond (see 图 10). Removing this wire bond reduces the parasitics, which dramatically lowers the switch node ringing. This ringing is a major source of EMI for buck converters using the standard wire-bond packaging.

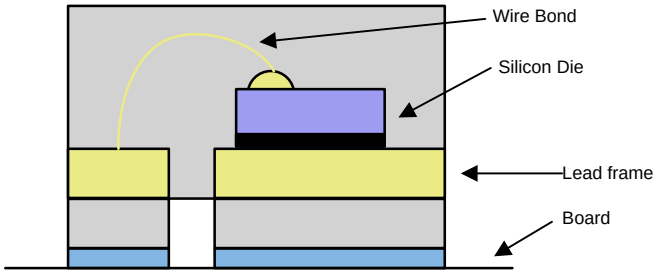


图 **10. Standard Wire-Bond QFN**

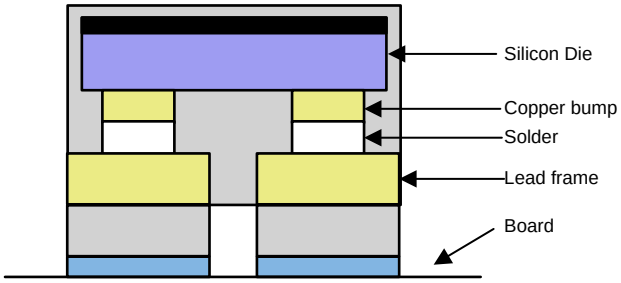


图 **11. HotRod™ FCOL QFN**

图 12 and 图 13 show the difference between switch node ringing for a wire-bond package and a HotRod package. The ringing overshoot reduces from 9 V to 0 V, which lowers the overall EMI and noise. The HotRod packaging helps to reduce EMI and allows for a smaller size and reduced R_{DS_ON}, which improves the efficiency.

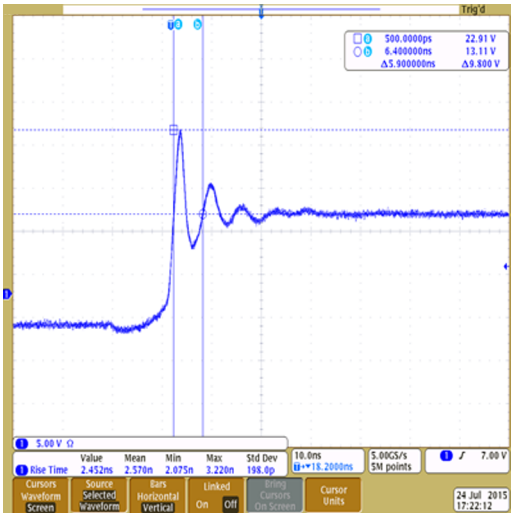


图 **12. LM53603 TSSOP**

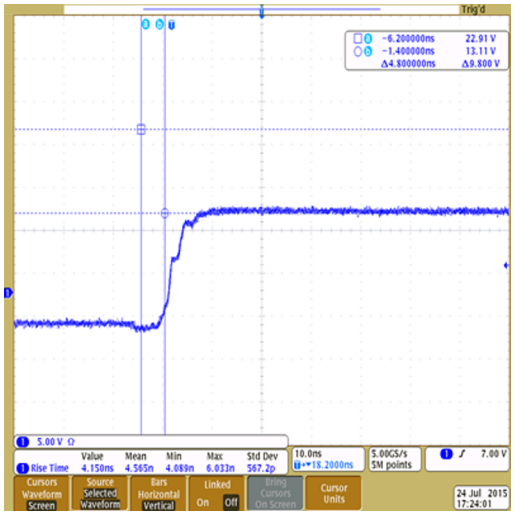


图 **13. LM53635-Q1 FCOL**

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

This section outlines the information for getting the board up and running quickly. To learn about the precision host interface (PHI) board or the onboard clocking and jitter cleaner, see *Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters*. Take care when moving jumper pins to avoid possible damage to the components.

3.1.1 Jumper Configuration

This system has several configurable power options. These options are selectable through using two-pin and three-pin jumpers. 表 2 highlights the purpose of each jumper and assists in changing the configuration to fit the user requirements.

表 2. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
JSI_18V	Power to LMS3635-Q1 18-V rail	—	Short
JTI_18V	Connects LMS3635-Q1 to TPS7A700 for 18-V rail	Connects LMZ14201 to TPS7A700 for 18-V rail	Short pins 1 and 2
JSI_5V	Power to LMS3635-Q1 5-V rail	—	Short
JTI_5V	Connects LMS3635-Q1 to TPS7A700 for 5-V rail	Connects LMZ14203 to TPS7A700 for 5-V rail	Short pins 1 and 2
JSI_3.3V	Power to LMS3635-Q1 3.3-V rail	—	Short
JTI_3.3V	Connects LMS3635-Q1 to TPS7A700 for 3.3-V rail	Connects LMZ14202 to TPS7A700 for 3.3-V rail	Short pins 1 and 2
JPRI_–18V	Power to LM46001 –18-V rail	—	Short
JTI_–18V	Connects LM46001 to TPS7A3001 for –18-V rail	Connects LM5574 to TPS7A3001 for –18-V rail	Short pins 1 and 2
JMTI_–18V	Power to LM5574 –18-V rail	—	Open
JZI_18V	Power to LMZ14201 18-V rail	—	Open
JZI_3.3V	Power to LMZ14202 3.3-V rail	—	Open
JZI_5V	Power to LMZ14203 5-V rail	—	Open
J39	Connects –0.2-V rail to OPA625 and THS4551	Shorts –0.2-V rail to ground	Short pins 1 and 2

3.2 Testing and Results

3.2.1 Efficiency

The efficiency of each buck converter (3.8 V, 5.5 V, and 18.5 V) was evaluated with those devices implemented on the system board. Because the LMS3635-Q1 is capable of superior light load mode, it has an overall better efficiency than the LM53635. Specifically, at a 15.7-mA output current (see 表 3), the efficiency improved by 7.2% (89/83-1).

表 3. Efficiency Evaluation Results

VOLTAGE SOURCE	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)	INPUT VOLTAGE (V)	INPUT CURRENT (mA)	EFFICIENCY (%)
LMS3635-Q1	3.804	184	24	33	88
	5.488	20.1	24	5.26	87
	19.077	15.7	24	14	89
LM53635-Q1	3.813	184	24	34	86
	5.492	20.1	24	5.26	87
	19.093	15.7	24	15	83

3.2.2 EMI Matters

An Audio Precision 2700 series signal generator is used as the signal source to test the AFE and ADC performance. The noise and THD of the AP2700 have adequate performance and do not limit measurements or system performance. A generic DC power supply is used to generate the 24-V DC input voltage.

A PHI controller board is used to connect the TIDA-01056 board to the host PC, where the ADS8900B EVM GUI functions. This software allows the designer to measure SNR, THD, SFDR, signal-to-noise and distortion ratio (SINAD), and ENOB for the ADC by running a spectral analysis. The AP2700 is set to output a 2-kHz 8-V_{pk-pk} sinusoid. A value of 2 kHz is chosen because it is the standard frequency when measuring noise and THD, and 8-V_{pk-pk} grants full range on the THS4551 or OPA625 devices, thus granting a full range of 0 to the V_{REF} for the ADC.

AC performance was measured for both the LMS3635-Q1 and LM53635-Q1 devices (see 图 14 and 图 15). The LMS3635 slightly outperformed the LM53635 by almost 1 dB in SFDR. According to *Multi-Rail Power Reference Design for Eliminating EMI Effects in High-Performance DAQ Systems*, the LM53635 gives a comparable performance to the same system with external power supplies. Thus, the LMS3635 device can reduce power consumption and reduce voltage ripple while minimizing the effect of EMI from switching noise.

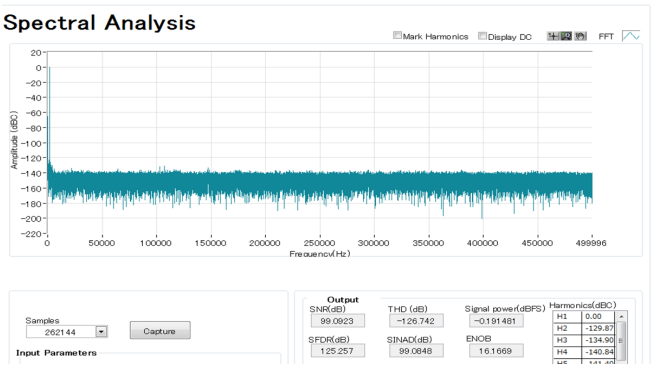


图 14. AC Performance with LMS3635

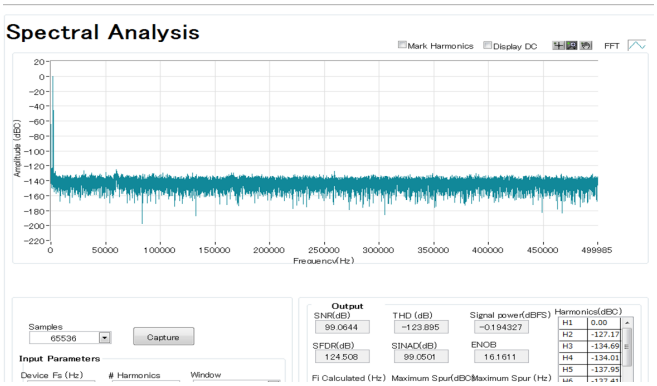


图 15. AC Performance with LM53635

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01056.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01056.

4.3 PCB Layout Recommendations

The LMS3635-Q1 has certain layout guidelines that help to reduce EMI. 图 16 shows how the LMS3635-Q1 and its additional components must be placed in the layout.

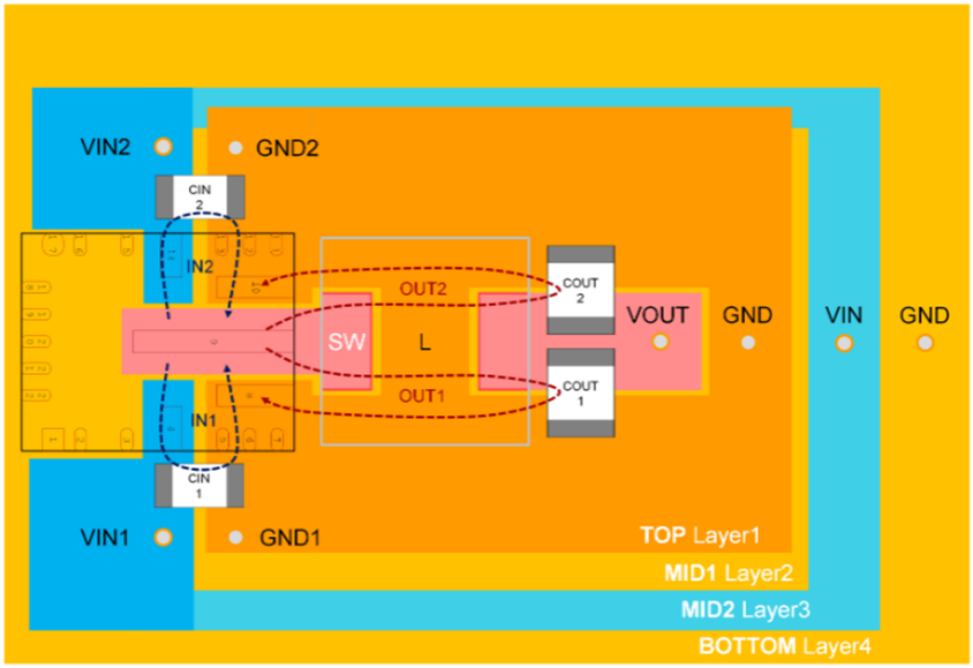


图 16. LMS3635-Q1 Layout Guidelines

Putting the input and output capacitors in this configuration creates parallel capacitance loops, thus minimizing the inductance. This placement then reduces the switch node ringing and lowers the overall EMI emissions. TI also recommends leaving the ground plane unbroken under the device. This placement provides the shortest return path possible, minimizing EMI generated by the loop. For more layout recommendations regarding the AFE or SAR ADC, see *Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters*.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01056.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01056.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01056.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01056.

5 Software Files

To download the software files, see the design files at TIDA-01056.

6 Related Documentation

1. Texas Instruments, *ADC Driver Reference Design Improving Full-Scale THD Using Negative Supply*
2. Texas Instruments, *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features*
3. Texas Instruments, *Multi-Rail Power Reference Design for Eliminating EMI Effects in High-Performance DAQ Systems*
4. Texas Instruments, *Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters*

6.1 商标

7 About the Authors

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