TI Designs：TIDA-01573
适用于激光雷达的纳秒激光驱动器参考设计

说明

此激光雷达（光距离和范围探测）参考设计展示了一款低侧纳秒级 GaN 栅极驱动器 LMG1020，该驱动器能够驱动 FET 产生功率超过 100W 的 1ns 激光光脉冲。

资源

TIDA-01573	设计文件夹
LMG1020	产品文件夹

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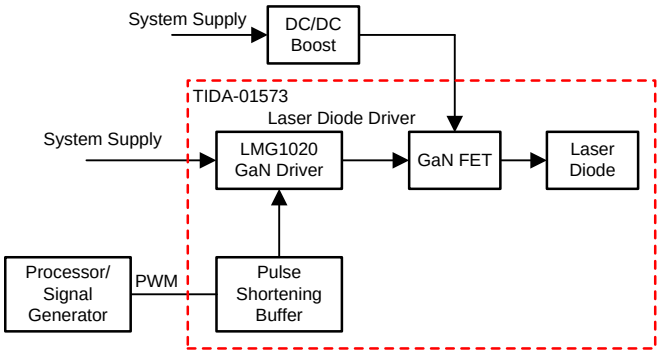
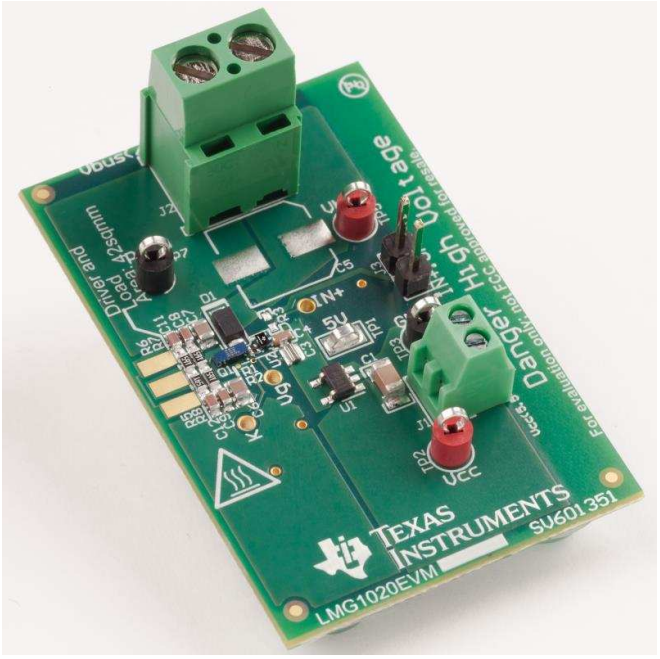
特性

- 电路可提供 60A、1ns 电流脉冲
- 具有用于安装和测试激光二极管的灵活平台
- 最新的 GaN FET 驱动器技术 LMG1020
- 先进的极低电感布局

应用

- 3D 成图激光雷达
- 非汽车自主驾驶车辆激光雷达
- 测距激光雷达
- 激光扫描仪
- 光纤集成仪器





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1 System Description

With the increased popularity of LiDAR applications, the required specifications are constantly improving, especially for resolution and distance. For high-speed applications, the detection desired specification hovers around 300 m for a 30-cm object with 10% reflectivity. This specification translates into a solution that requires 100 W to 200 W of light power and a repetition rate of up to 1 MHz to fill a front facing field of vision (100º × 25º with a 0.1º resolution) and allow for a 20-Hz to 60-Hz refresh rate.

With the popularity of near infrared (IR) wavelength at around 905 nm, there is an eye safety energy limit of 250 nJ that must be met. If the range of power has to increase, and to increase the resolution the repetition frequency has to increase, the only way to maintain emission under the safety limit is to have extremely high energy pulses for an extremely short amount of time (and low duty cycle).

The requirement then comes to 100 W to 200 W for 1 ns to 2 ns at a 1-MHz to 2-MHz repetition rate.

This reference design uses the LMG1020EVM-006 to provide a LiDAR driver capable of this performance and guides through the consideration and specifications necessary to replicate such performance.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	30 to 75	VDC
Input current	0.1	A
Bias voltage	6 to 18	VDC
Switching frequency	0.1 to 1	MHz
Peak pulse current	60	A

2 System Overview

2.1 Block Diagram

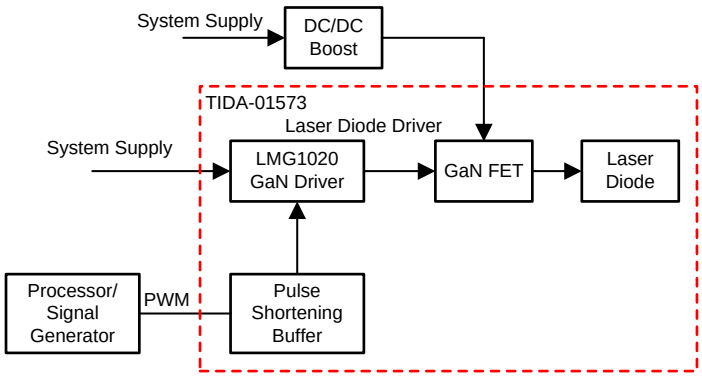

图 1. TIDA-01573 Block Diagram

2.2 Design Considerations

2.2.1 Capacitor Selection

Due to the extremely fast nature of this application, the selection, placement, and value of the bypass capacitance is critical for both the gate and the main power loops.

2.2.1.1 Gate Loop Capacitors

The bypass capacitor for the LMG1020 must be located on the top layer with ground return on the layer immediately adjacent and minimal spacing (5 mils recommended). Place the capacitor as close as possible to the device, and connect it to both VDD and GND using large power planes. This bypass capacitor has to be at least 0.1 µF (up to 1 µF) with a temperature coefficient of X7R or better.

For this particular application, it is highly recommended to use low inductance body types such as LICC, IDC, feed-though, and LGA.

图 2 shows the feed-though type, which allows for the fastest rise times because it minimizes the parasitic inductance.

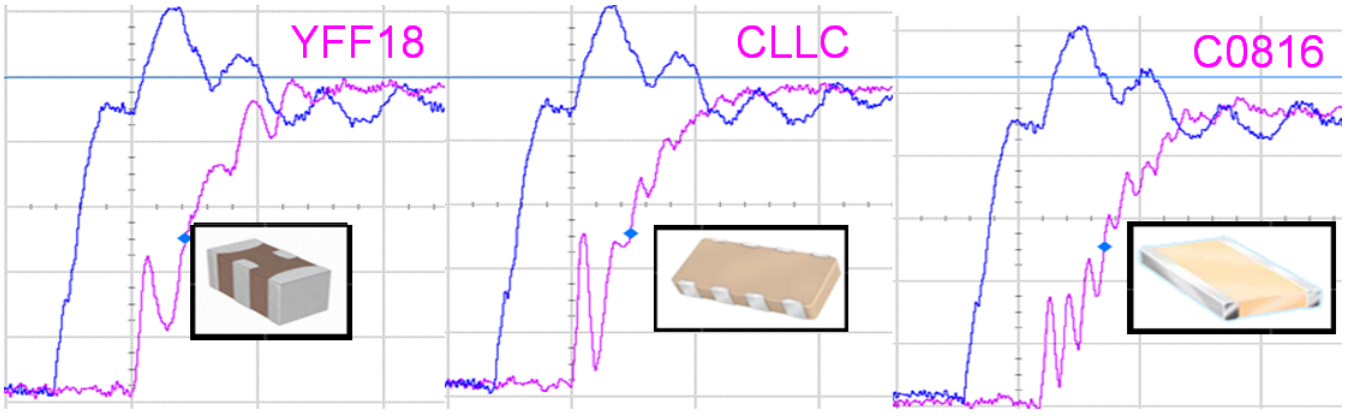

图 2. Low-Inductance Bypass Capacitors

Finally, place an additional 1-µF capacitor as close to the device as possible.

2.2.1.2 Power Loop Capacitors

High-frequency capacitors for the power loop must provide currents in excess of 60 A with a rise time of ≈ 300 ps (200 A/ns). The inductance of the loop is the main limiting element when dealing with those speeds. The capacitors must be selected to allow for the maximum bus voltage. These capacitors must provide both enough charge to sustain the current and a minimal inductive path.

X7R or better material is needed to provide stability and low ESR; a mix of 0603 and 0805 is necessary, where the smaller capacitors are in the closest proximity to the power loop and the 0805 are adjacent to those first capacitors. These materials are preferred if low-inductance, wide-body packages become available.

The total value for the capacitance depends on the pulse repetition and pulse duration—in this case, a 1-MHz repetition frequency for a 60-A, 1-ns pulse and a 40-V bus. To ensure the peak current is reached, do not let the capacitor bank discharge more than 5% during the first half of the pulse.

$$\frac{60\ \text{A} \times 1\,\text{ns}}{2\ \text{V}} = 30\text{-nF capacitance} \tag{1}$$

The layout of this section is critical and is discussed in 节 2.2.4 and 节 2.2.5.

2.2.2 FET Selection

The specifications to select the correct FET for a LiDAR application are different than for normal power conversion applications.

To ensure the capability of reaching high currents in a nanosecond delay, the FET must fully turn on extremely fast. GaN HEMTs are a better candidate because of their high conductance characteristic (Gm).

表 2 compares the advantages of a GaN HEMT for nanosecond applications with respect to a Silicon FET.

表 2. GaN vs Silicon Advantages

PARAMETER	BSP318S (SILICON 60 V)	EPC2019 (GaN 200 V)	UNIT	GaN ADVANTAGE	P_{SAVE} (TOTAL ≈ 2 W)
B_{VDSS}	60	200	V	More robust	
$R_{DS(on)}$	70 (90)	36 (50)	mΩ		
$V_{DS(on)}$	2.1 (2.7)	1.1 (1.5)	V at 30 A	50% conduction losses	35 mW
Ciss	300	200	pF		
gm(25C)	5.5	26	S	Faster turnon (20% of VI losses)	2.25 W
V_{TH}	1.6	1.4	V		
Vplateau	7.1	2.6	V at 30 A	Faster turnon	
Q_G	14	1.8	nC	Shorter pulse capable	
Q_{GD}		0.35	nC at 100 V		
Q_{GD}	3.6	0.28	nC at 30 V	Shorter pulse capable	
Qoss		18	nC at 100 V		
Qoss	3.88	8.9	nC at 30 V	Twice the Coss losses	–250 mW

The selected FET can be sized significantly smaller than the full load current rating because this is a pulsed application.

Note that the peak current of the FET represents the saturation of the channel, and the $R_{DS(on)}$ increases rapidly beyond that specified current level, which means that the highest current possible in the system is ultimately limited by the maximal FET peak current.

图 3 shows the difference in switched current through the channel (ultimately available to the laser diode). The silicon FET peak current for a 2-ns pulse is 1/3 of a GaN FET. Below 2 ns, the peak current for the Si FET reduces rapidly.

In the 5-ns comparison, the half-power width for the GaN is ≈ 3 ns versus 5 ns for the silicon case, and the actual energy used is very similar but with a peak power of roughly half. The GaN FET solution would increase the application range by 80% and by 30%, respectively.

Following 公式 2:

$$R \times \frac{1}{\sqrt{P}} \quad (2)$$

where:

- R is distance
- P is the light output power of the laser

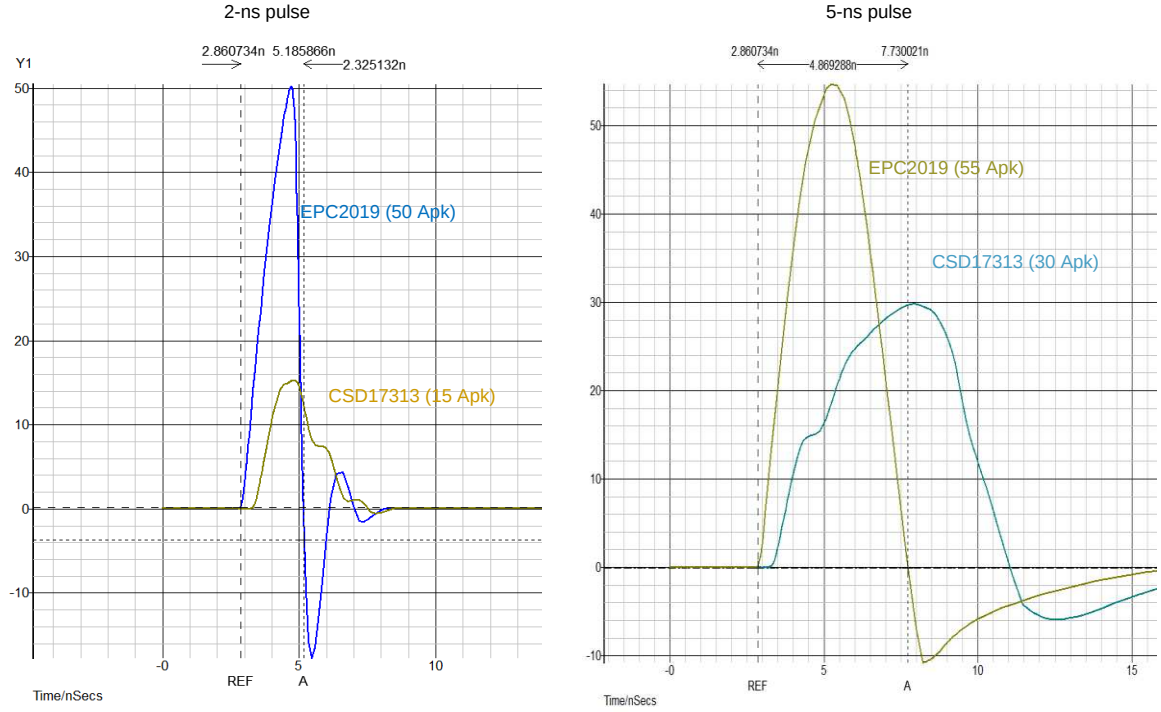

图 3. GaN FET vs MOSFET Pulse Comparison

Finally, because of the extremely high di/dt and the ground lifting that occurs as a direct consequence, if the gate loop and power loop ground returns are tied together, the gate would detect a reduction in its relative voltage, effectively pinching the gate off. This reduction causes a negative feedback that slows down the turnon process of the FET.

To mitigate this effect, a split path for the two returns is necessary. Use a FET with a dedicated Kelvin gate ground return connection.

The last consideration while selecting the FET is its capability to withstand the inductive voltage overshoot that appears when the FET turns off, especially if operating without clamping.

The initial target this reference design is to reach 40 A and with a maximal bus voltage of 100 V. The FET this design uses is the EPC2019 because of its dedicated gate Kelvin connection. The 200-V breakdown voltage rating assures the reliability of the part; a 40-A peak rating for 300 µs is sufficient.

On a 1-ns pulse, the current must be able to ramp up to 60 A, although it is possible to observe a rapid degradation in the system output efficiency in part due to the elevated current density though the FET.

Note that it is recommended to follow the curve of the safe operating region (SOA) from the manufacturer, and if exceeded for short amount of time, the factory would have to approve its use in an application.

2.2.3 Kelvin Gate

Ground lifting issues are associated with very high di/dt of the main power loop. To avoid these issues, the gate signal must be decoupled completely by providing its separate ground return path, thus ensuring no power current flow where the gate current flows.

To ensure this flow, with the correct selection of the FET, it is possible to have a dedicated pin to serve as the connection point to the signal ground.

The power and the signal ground are connected internally to the FET, are kept completely separated on the board, and are named as two different nets.

Avoiding the ground to lifts ensures a much faster and smoother turnon characteristic of the FET. With a ground lift on a common source, the V_{GS} would be reduced by the source voltage rising and effectively starting to turn off the FET.

2.2.4 Ground Return

Due to the very high currents and high speed of this application, take all the layout considerations into account.

In this reference design, all ground returns are done on the layer immediately adjacent with a minimized spacing of 5 mil. This layout minimizes the inductance by providing a coupled return path as close as possible for the currents loops.

Furthermore, the power loop ground and the gate loop grounds are separated and tied together at the single tie point inside the FET. This combination ensures that no current from the power loop flows through the gate loop and causing a ground lift.

This reference design also uses micro-vias in pads to:

- Further reduce the parasitic inductances
- Improve the vertical current extraction from components
- Keep the return loops as short as possible

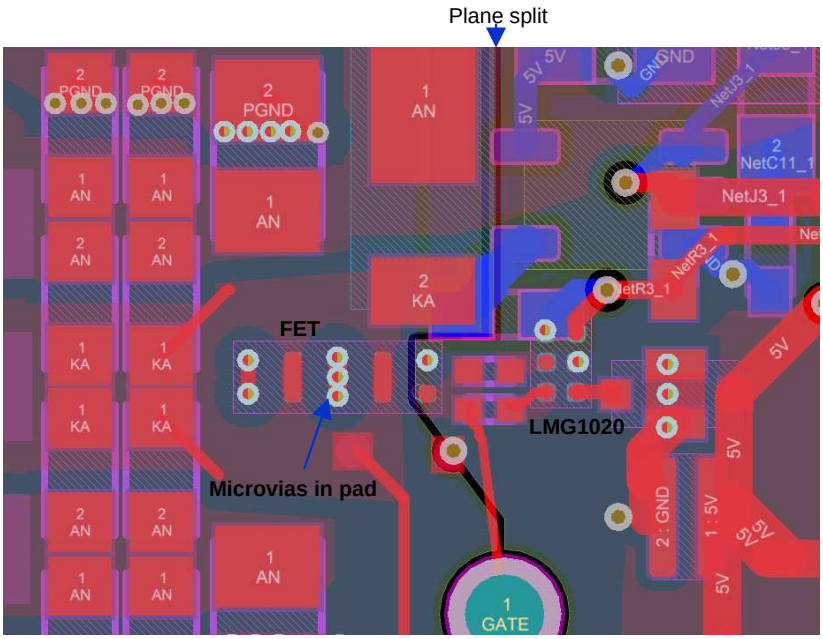

图 **4. Split Ground Planes**

2.2.5 Split Power Loop

Due to the high speed of the design, there is a heavy focus on minimizing the parasitic inductances. This focus is extremely important on the highest current loop in the circuit, which is the laser power loop.

To achieve this, the board is designed with a split power loop, where bypass capacitors are placed on both sides of the laser diode.

Splitting the loop offers several advantages:

- As the two loops are symmetrical and have the same inductance, splitting is equivalent of putting two inductances in parallel, thus halving the effective inductance and sharing the current into the two separate branches. If one loop alone has inductance L and current I, by adding a second loop of inductance L, each loop would have a ramp time divided by two as if the inductance was half of one single loop.
- As the currents in the two loops flow in opposite directions, the magnetic flux has a tendency to cancel itself out, which reduces coupling losses and interference on the board, thus reducing both stray impedance and improving the immunity of the surrounding circuitry. This reduction is theoretical; in the near field, the cancellation is only partial and appreciable at the mid-point.

图 5 shows how current flows in the two power loops.

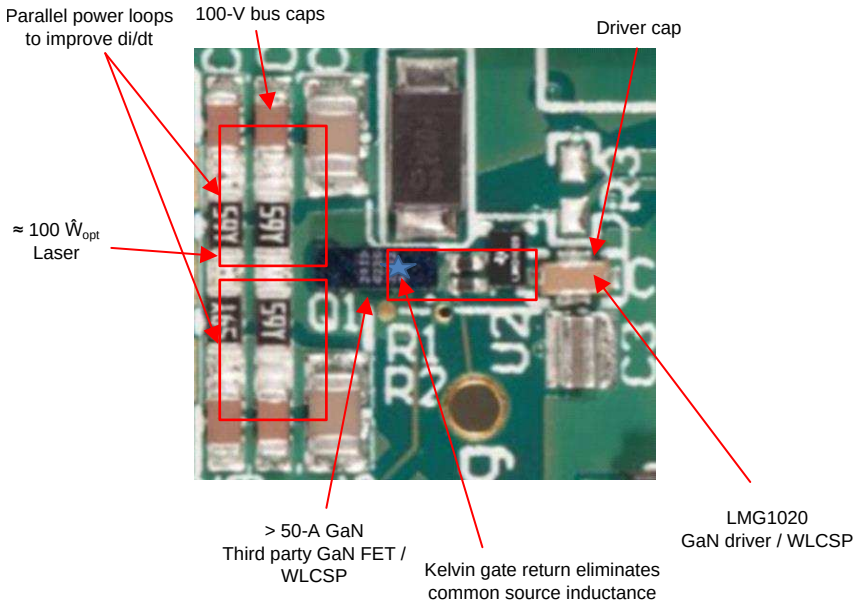

图 **5. Parallel Power Loops**

2.2.6 Inductive Overshoot

When switching tens of Amperes over less than a nanosecond, the parasitic inductances play an major role in shaping the voltage waveform. In this case, the best practices are applied in minimizing such inductance. However, because of the magnitude of the current and the timing involved, across the few hundreds of picohenries, it is possible to develop several tens of volts.

More precisely, following 公式 3, it is possible to visualize the magnitude of such overshoots. Considering that the entire energy in the parasitic inductance will resonate into the FET capacitance:

$$\frac{1}{2}V^2C = \frac{1}{2}I^2L$$
$$V = I\sqrt{\frac{L}{C}} \quad (3)$$

In 公式 3, by subsittuting L = 325 pH, C = C_{OSS} = 200 pF, and I = 57 A, this yields 73 V.

This phenomenon is also easily observed in when capturing the V_{DS} as shown in 图 6.

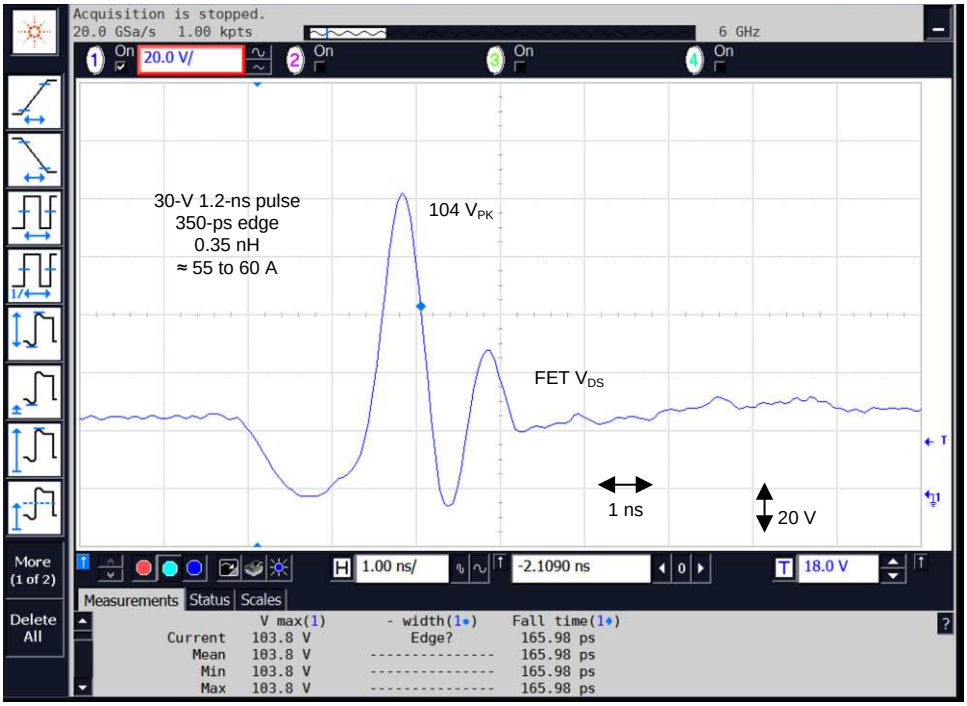

图 6. Inductive Overshoot on Driving FET After Turnoff

This overshoot can cause overstress at the driving FET, which has to be selected appropriately to withstand such surges.

The second concern is the stresses caused on the cathode of the laser diode. The BV of each junction is in units of amperes, 2 V to 6 V typically for older generations and 10 V to 15 V for later generations, yielding for a triple-stacked diode a range between 6 V and 45 V.

Examining this issue closer, it is necessary to consider how much stress will actually be present at the junction of the laser diode and how much of the voltage drop will appear across the parasitic inductance.

Using the extracted value of 50 pH between the junction and the measurable board waveform, no or very little stress appear across the junction as shown in 图 7.

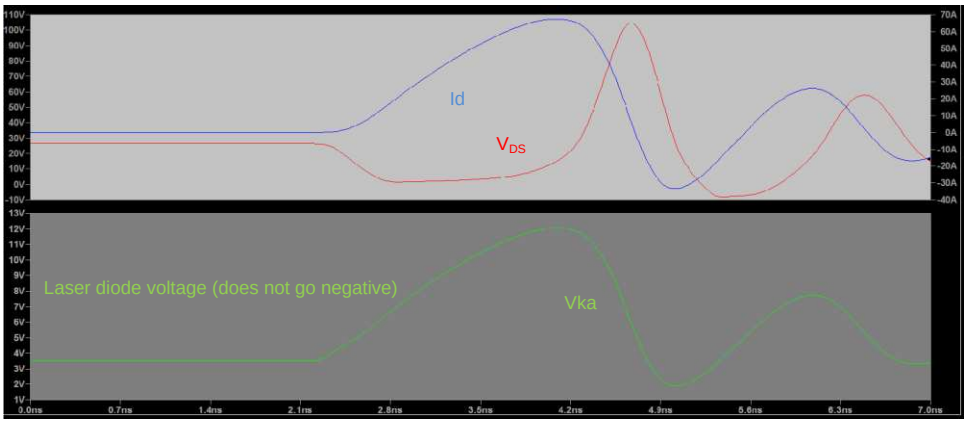

图 7. Simulation of Voltage Stress on the Cathode of Laser Diode

2.2.7 Clamping Diode

The inductive overshoot can cause stresses in the system that can be mitigated, possibly to size components closer to operation. To mitigate this stress, add an anti-parallel conduction path to the laser diode to avoid the large voltages experienced by an unclamped circuit.

The clamp can be provided by either a diode or a FET with the gate connected to source (active only in the third quadrant). When selecting the clamping device, consider the following:

- Package inductance: The package must be as small and with low inductance as possible because this will be in parallel with the inductance in the laser diode. If the clamp inductance is much larger than the laser diode, this solution will quickly lose effectiveness (as most of the current would still flow through the laser diode).
- Board layout: The proximity of the clamp is key to shunting the current away from the laser diode because the current will be favoring the path of least impedance. Unfortunately, the placement will always be challenging and slightly sub-optimal because one cannot optimize for both the laser conduction and the clamp shunt path.
- Device capacitance and junction charges: This capacitance appears across the laser diode, causing some of the switched current bypass the laser diode, thus slowing the turnon performance and peak currents. Furthermore, a PN junction with a reverse recovery charge results in a recovery loss, causing the system efficiency to drop.

The following figures show the voltage spike reduction associated with the clamp. On a 25-V bus, the unclamped circuit has a voltage overshoot of 12 V, while the clamp keeps it at 3 V (the current is ≈ 10 A, in this case).

图 **8. Overshoot Voltage With Clamping Diode**

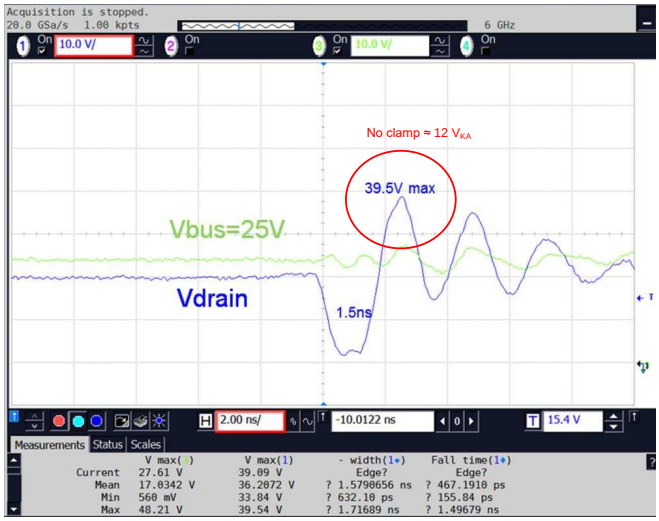

图 **9. Overshoot Voltage Without Clamping Diode**

From these figures, optimal performance is achieved when using a GaN HEMT because this has the minimal amount of charge, does not suffer recovery losses, and has minimal inductance as it is an unpackaged device.

2.2.8 LDO and Supply Selection

Due to the limits imposed both by the LMG1020 driver and the EPC FET, the power supply for this solution must maintain the output voltage below 5.25 V and nominally at 5 V.

2.2.9 Buffer Selection

This portion is optional depending on what the application and driving logic is used.

The board used as reference in this design guide features a pulse-shortening buffer. In an full system application, which most likely is a FPGA-type controller with LVDS type output, it is recommended to use as a buffer an LVDS to CMOS receiver such as DS90LV028A.

2.3 Highlighted Products

2.3.1 LMG1020

The LMG1020 is a single, low-side driver targeted at driving enhancement-mode GaN FETs and logic-level silicon FETs in high-speed applications. The simple structure of the device allows for extremely fast propagation delays of 2.5 ns of signals as short as 1 ns. The high drive strength for the pullup (7 A) and pulldown (5 A) can be independently adjusted thanks to the split output configuration.

The driver features undervoltage lockout (UVLO) and overtemperature protection (OTP) to ensure the device is not damaged in overload or fault conditions.

The LMG1020 is provided in an extremely compact, low-inductance WCSP package to meet the form-factor and gate loop inductance requirements of new GaN-based applications.

The LMG1020 has the following features and specifications:

- Single low-side, ultra-fast driver for 5-V drive GaN and silicon FETs
- Single 5-V supply
- Schmitt-trigger type CMOS inputs for robustness
- 2.5-ns typical, 4.5-ns max propagation delay
- 210-ps typical rise and fall time
- Protects against UVLO and overtemperature
- Minimum footprint 2×3 ball WCSP minimizes gate loop inductance and maximizes power density

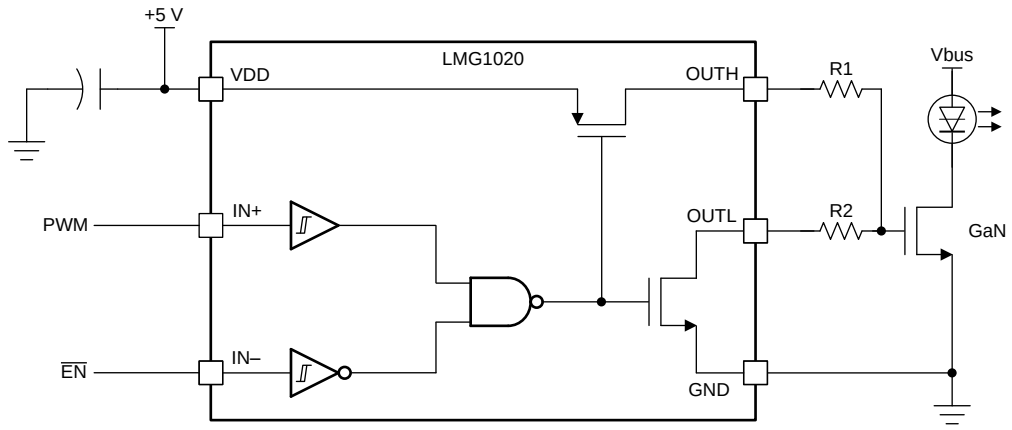

图 **10. LMG1020 Block Diagram**

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

- DC voltage source: Capable of supplying the input of the EVM up to 75-V DC as desired; capable of supplying 100 mA and supports current limiting
- DC bias source: Capable of 6-V to 18-V DC output at up to 100 mA
- Oscilloscope: Capable of operating at least 1 GHz (6 GHz recommended), using oscilloscope probes with a "pigtail" spring ground clip instead of the standard alligator clip
- DC multimeters: Capable of 100-V measurement, suitable for determining operation and efficiency (if desired)
- Function generator: Single output capable of at least 0-V to 3-V DC pulse signal (operating maximum digital input is 5-V DC), 1-MHz frequency or higher, 50-ns minimum pulse or smaller

3.2 Testing and Results

3.2.1 Test Setup

To obtain and measure nanosecond pulses at the output:

1. Connect the input (J2) and bias supplies (J1) as shown in 图 5, but do not power them on yet.
2. Power up the DC bias supply (J1), maintaining it in the 5.5-V to 15-V range and setting the current limit to 0.1 A.
3. Connect the function generator and apply the following settings:
   - Frequency: 100 kHz
   - Signal range: 0 V to 3 V
   - Pulse width: 100 ns
   - Enable the output
4. Power up the input supply (J2) (as shown in 图 5) and set to the desired input voltage, but no higher than 75-V DC. Set the current limit to 0.2 A.

   It is recommended to begin measurements at a lower voltage such as 10 V to ensure the correct waveforms are being captured.
5. Tune the length of the pulse on the function generator so that the cathode voltage pulse is reduced to the desired width (approximately 1 ns to 2 ns). Notice that if the onboard resistive load is being used, the rising edge of the pulse is given by the RC constant of the load in series with the COSS of the FET.
6. Perform the desired measurements.

3.2.2 Test Results

The most accessible point to get a direct measurement of the performance for this reference design is to measure the V_{DS} of the FET.

Looking at the behavior of the system from the input through the signal chain, it is possible to better understand the functionality and capability of this design. 图 11 shows how the input signal is treated if the input buffer is used. Note that it is possible to bypass this altogether and feed a signal directly to the LMG1020.

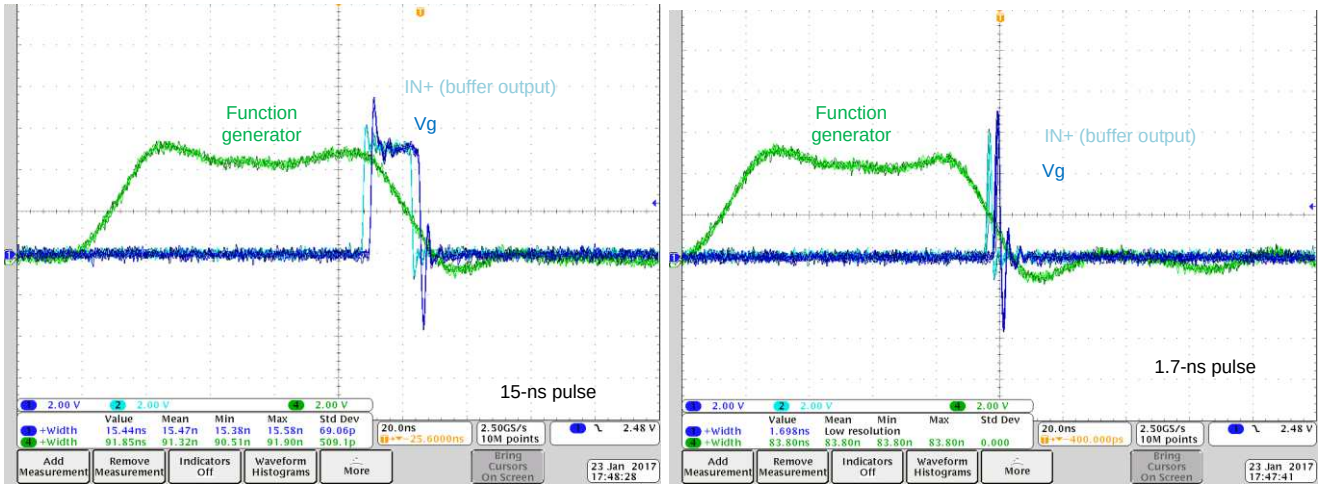

图 **11. Input Signal**

Adding the stitched node, it is possible to see the V_{DS} waveform, as shown in 图 12.

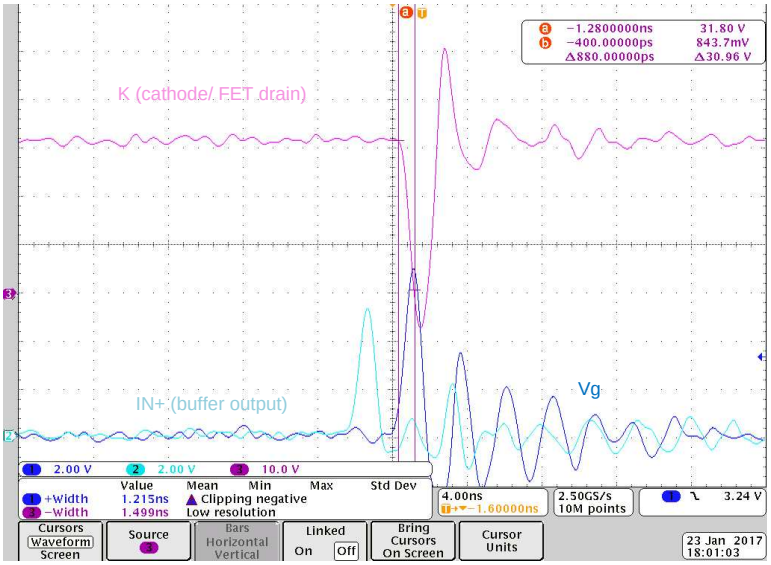

图 **12. Input and V_{DS} Signals**

The oscilloscope screenshot shown in 图 13 is taken with a 500-MHz oscilloscope to show typical operation waveforms. On the (K) waveform, it is possible to see a 20-V overshoot, which is due to the inductance in the power loop.

V_G seems to be oscillating, but this is caused by pickup noise, which is inevitable even when using a spring ground connection. The expected resonant frequency for the gate loop is ≈ 70 MHz to 90 MHz (given a gate capacitance of ≈ 10 nF and a gate inductance of 3 nH to 5 nH). The oscillation observed is at 250 MHz, which implies a gate loop inductance of ≈ 40 pH. Therefore, there is pickup noise.

It is possible to observe the pulse width generated and the inductive voltage overshoot after the rising edge.

图 13 shows the speed at which the combination of the LMG1020 and a GaN FET can turn on. With a 300-ps turnon time, it is possible to reach a current of 60 A through the channel and the laser diode and turn it back off in less than 1.5 ns.

图 13. V_{DS} for 1.5-ns Pulse With 40 V of Bus Voltage

Because of the speed and the particular care that is taken to minimize the loop inductance, there is no direct method to measure the current directly.

There are two indirect methods to measure current:

- Create a model to include the parasitic inductances of the components, connections, and PCB traces.
- Measure the power from the from the light pulses generated by the laser.

The next direct measurement that it is possible to make is the light pulse using first an single-photon avalanche diode (SPAD) matrix receiver (MicroFC-SMA-10010 Silicon Photo multiplier).

图 14 shows that the resulting light pulse captured has a 300-ps rising edge and a width at 50% of its amplitude (half-power) of 1 ns.

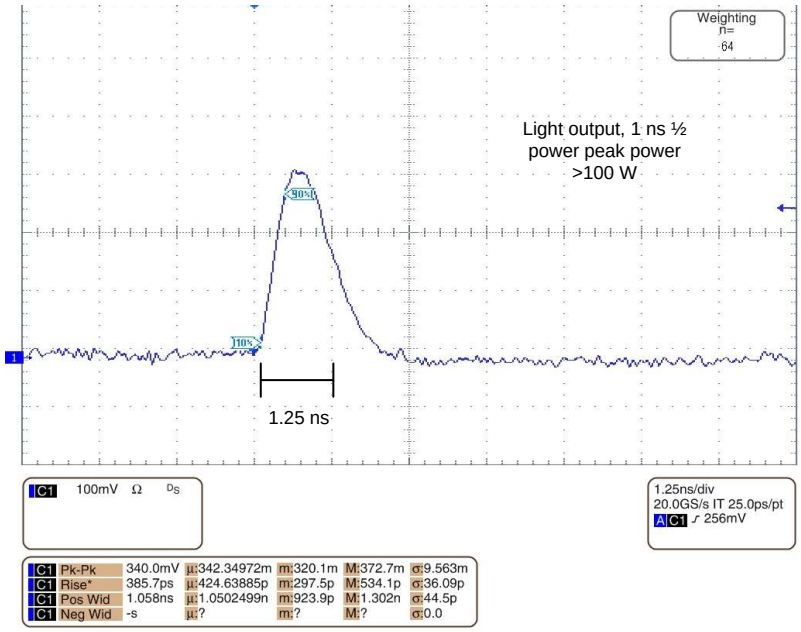

图 14. 100-W, 1-ns Light Pulse

Note that this type of receiver has a finite percentage (≈ 14% in this case) of a cell responding to an incident photon. For a high intensity laser, the cells can be depleted quickly. This generates a very quick rising edge, but can fail to capture the full shape of the curve as the time constant for current quenching and recovery is longer than 10 µs. A very high light intensity would trigger all the cells instantaneously (saturating the receiver), thus giving the impression of a very sharp and short pulse.

A possible solution to this issue is to use a screen to de-amplify the light pulse until it is possible to observe a direct change in the amplitude of the peak of the light pulse as a function of the bus voltage.

To validate this result, a 80-µm PIN receiver with an 8GHz bandwidth (Thorlabs DET08C) is used to observe the change directly.

图 15 shows how output power varies in proportion with the pulse width. Because this is a fast transition, the main limiting element is presented by the impedance form the parasitic inductances. By increasing the width of the pulse, it is possible to observe a distinct increase in the amplitude of the pulse.

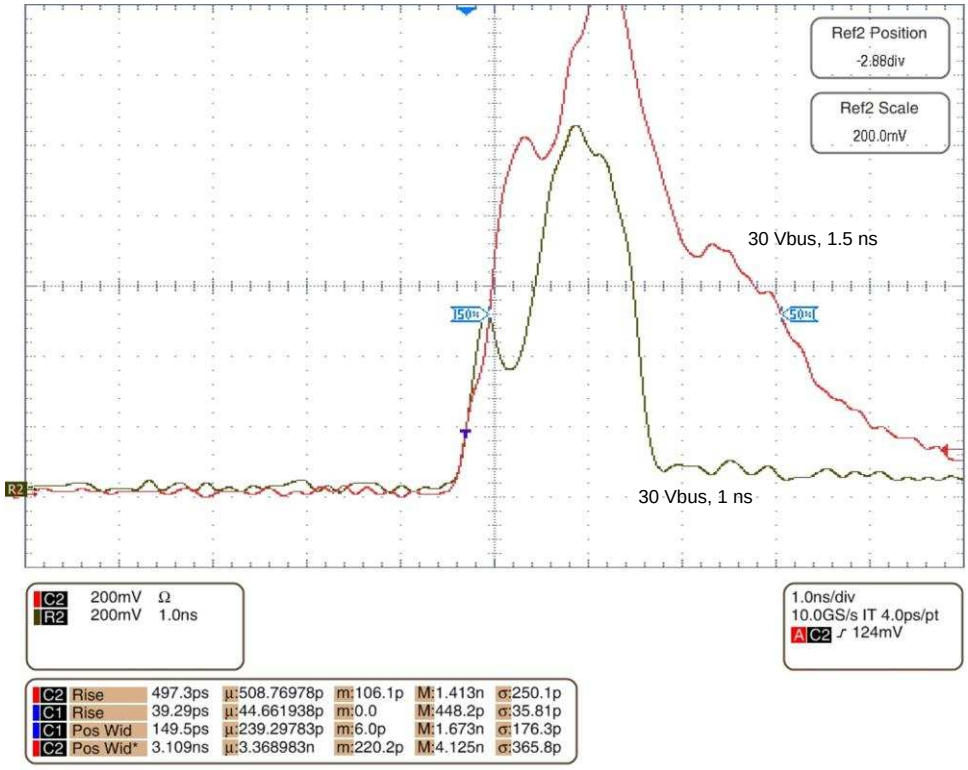

图 15. 1-ns and 1.5-ns Light Pulse Comparison at 30 V

The amplitude of the pulse is proportional to the output light power but does not indicate the dimension. Conversion from light back to electrical signal depends on the coupling, angle of incidence, and diffraction.

To measure the intensity of the pulse captured by the optical receiver, measure the power in the entire pulse and derive the dimension of the pulse from measuring the power and mathematically calculate the equivalence.

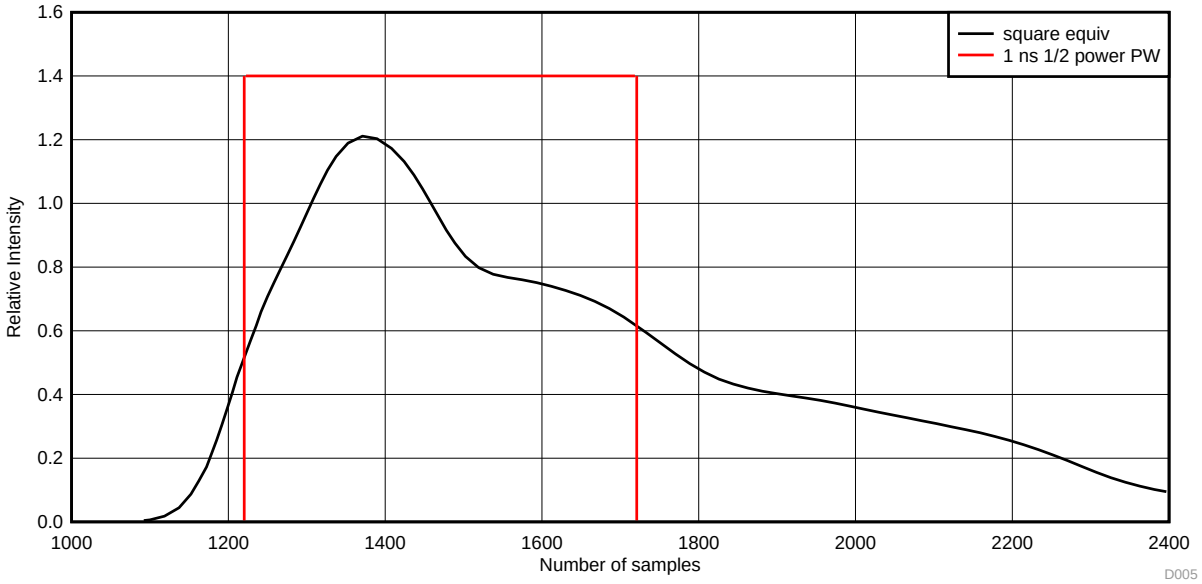

图 **16. Light Pulse Square Equivalents**

Using an optical power meter (similar to Thorlabs PDA150A), it is possible to measure the total energy transmitted by the light pulse (area under the red curve) to get a scaling for the peak power in the pulse. It is necessary to do some numerical manipulation.

Considering a square pulse with the same width of the 1-ns half-power optical width (in this case, 1 ns), for the energy be equivalent to the energy contained in the optical pulse, it is necessary to:

- Integrate the area under the red curve (optical pulse), this will be equivalent to the energy measured by the light meter.
- Find the peak value for the red curve (equivalent pulse) that gives the equivalent area
- Extrapolate the proportion of the two peaks between the power measured by the instrument and the peak power of the light pulse.

For this particular case, the parameters are as follows (rounded for simplicity):

- Sample interval: 2 ps
- Measured power: 510 µW (on a 10-kHz, 0.98-ns pulse)
- Adjusted power per pulse: 52 W
- Integral energy: 700 (these are relative units of energy as the amplitude of the pulse is not scaled) for the light pulse (over 2500 samples)
- 1-ns equivalent (over 500 samples) peak: 1.39
- Light peak: 1.22
- Proportion: 0.874
- Peak power: 45.5 W

With this adjusted calculation, 图 17 represents the extracted power outputs for different types of diodes. Note that with an optimized package and a bus voltage of 60 V, it is possible to get close to a 200-W peak light output for a 1.5-ns pulse.

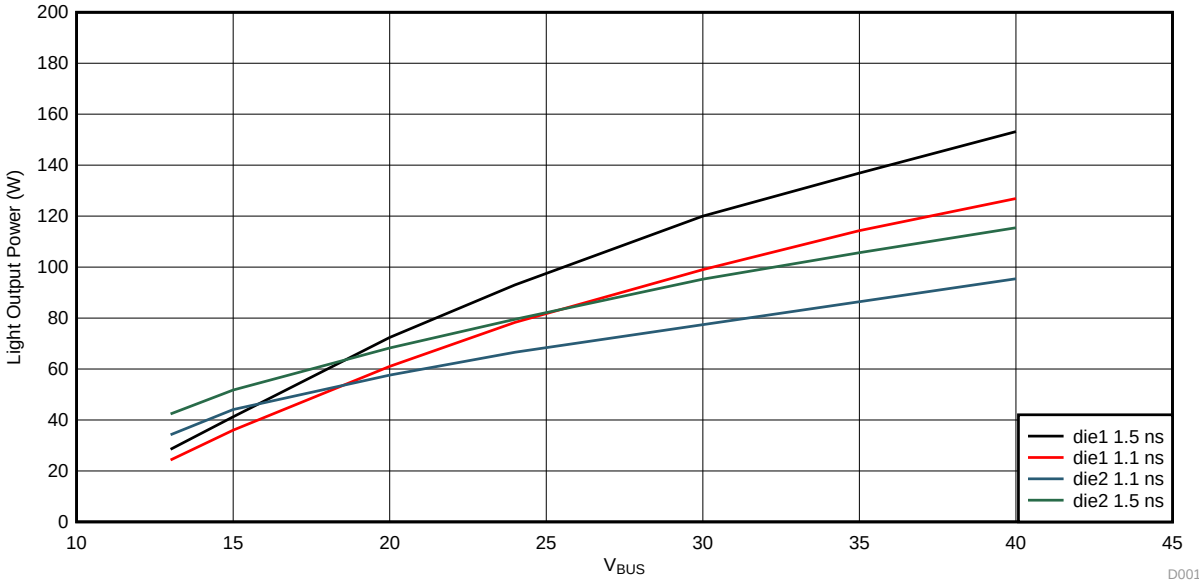

图 17. Bare Laser Die Luminescent Power Output Curves vs Bus Voltage

This first set of measurements is taken on a setup with the bare die attached directly to the board and wire-bonged (as it would be in a package). This setup is not practical for manufacturing but a good exploration to uncover the potential limits of an optimized system.

The two laser diodes in consideration are both 905-nm, 75-W rated, but it is possible to notice a large performance difference. Be sure to test devices that have similar specifications before selecting one for the design.

To account for a more manufacturable solution, compare the performance of the bare die with the same laser diode in an SMT package. 图 18 shows the results of such a comparison.

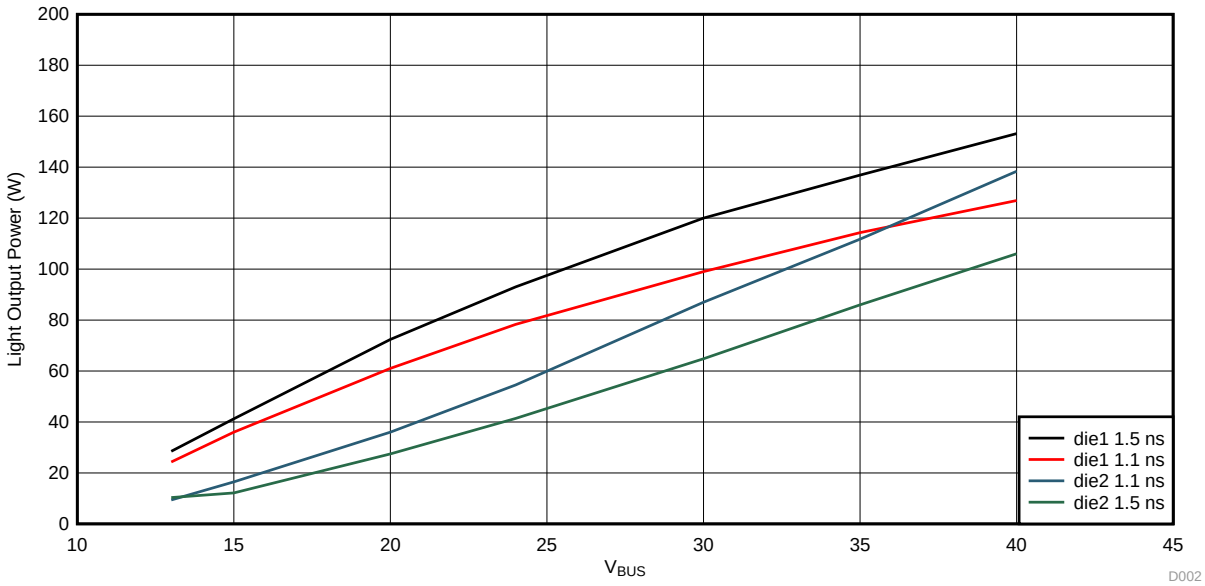

图 18. Bare Die vs SMT Laser Diode Luminescent Power Output Curves

The performance for short pulses is inferior in the SMT packaged laser (as in this case it adds almost 1 nH of parasitic inductance), but it is still possible to achieve a peak output in excess of 100 W with only 40 V as bus voltage. Remember that these are 75-W, triple-stacked, with a forward drop of ≈ 12 V. This setup also explains why 图 19 is not available below 12 V).

Per manufacturers the SOA of the laser is rated at 100% for 100 ns, and increase logarithmically as the pulse shortens, yielding a max of > 500% at 1 ns.

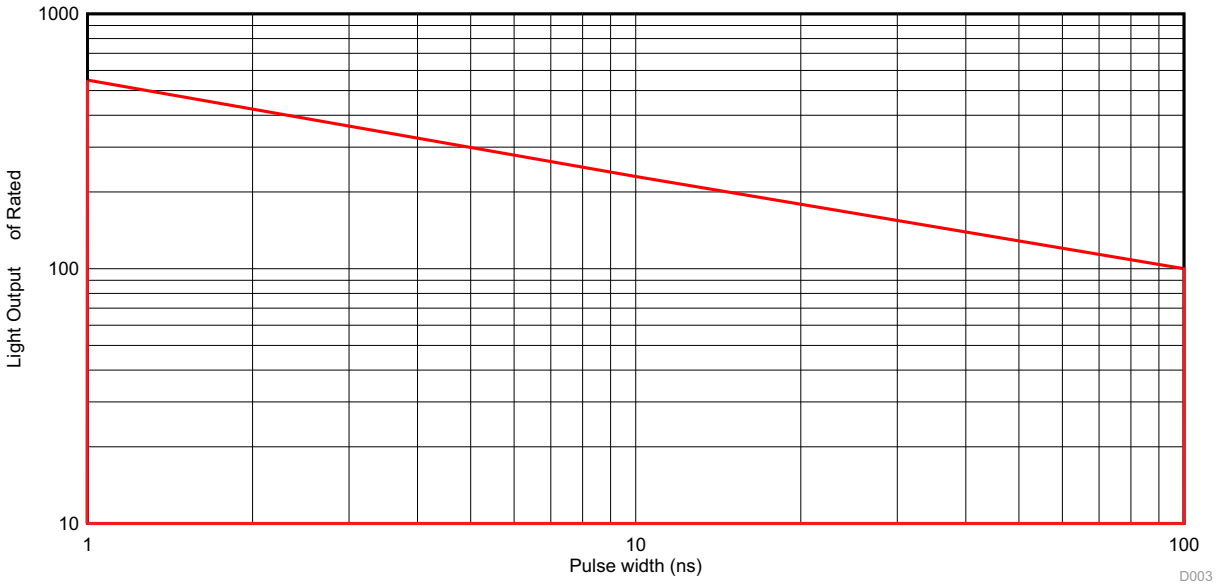

图 **19. Laser Diode Output Luminescence SOA**

Given these power levels, it is possible to trace back the peak current flowing though the laser diode by using an extrapolation from 图 20 that correlates current to output light power.

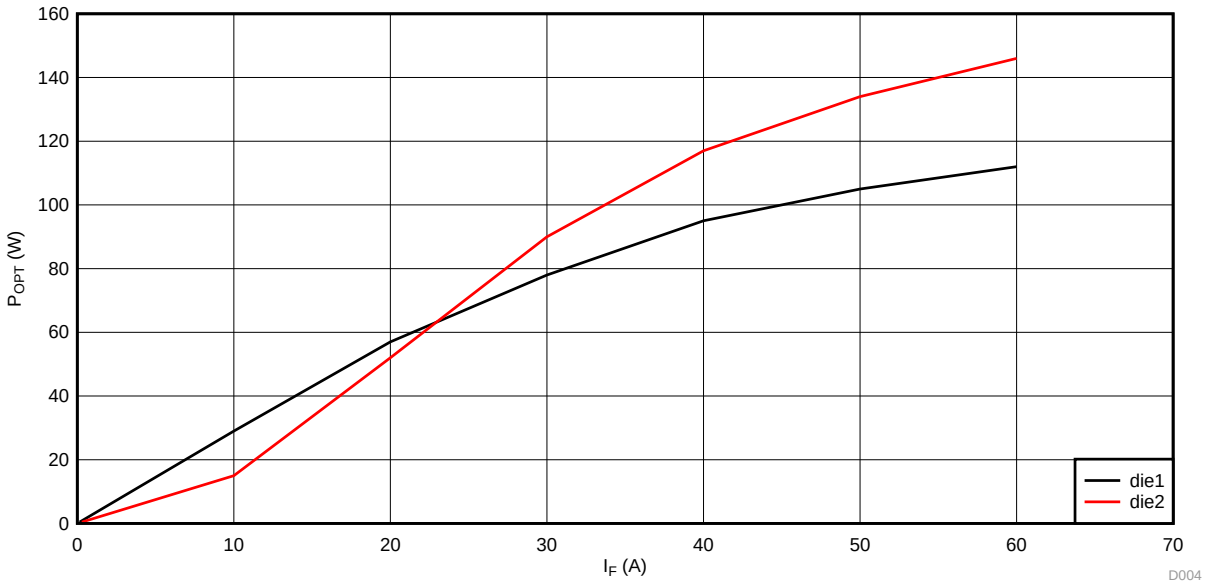

图 **20. Relative Rated Luminescence vs Channel Current**

Notice that with the configuration used as a reference, this reference design can exceed peak currents of 60 A.

Regarding the effective power distribution, given a 12-V_F drop at 60 A, the input power to the diode is ≈ 720 W and only ≈ 120 W comes out as light. The emitting efficiency of such lasers is only 15% to 20%.

This is an important aspect to consider in a design as the rest of the power is dissipated as heat in the die (600 W per pulse, according to the calculation). By running a short pulse (a few ns) and a duty cycle of less than 1%, it is possible to maintain the thermal within the operating limits.

One final advantage of using an active LiDAR configuration (where the FET switching causes directly the diode to switching) is that it is possible to pulse the laser several times within a short duration, which can be a desired feature for pattern recognition.

图 21 shows a double 1.5-ns pulse at 5 ns of separation.

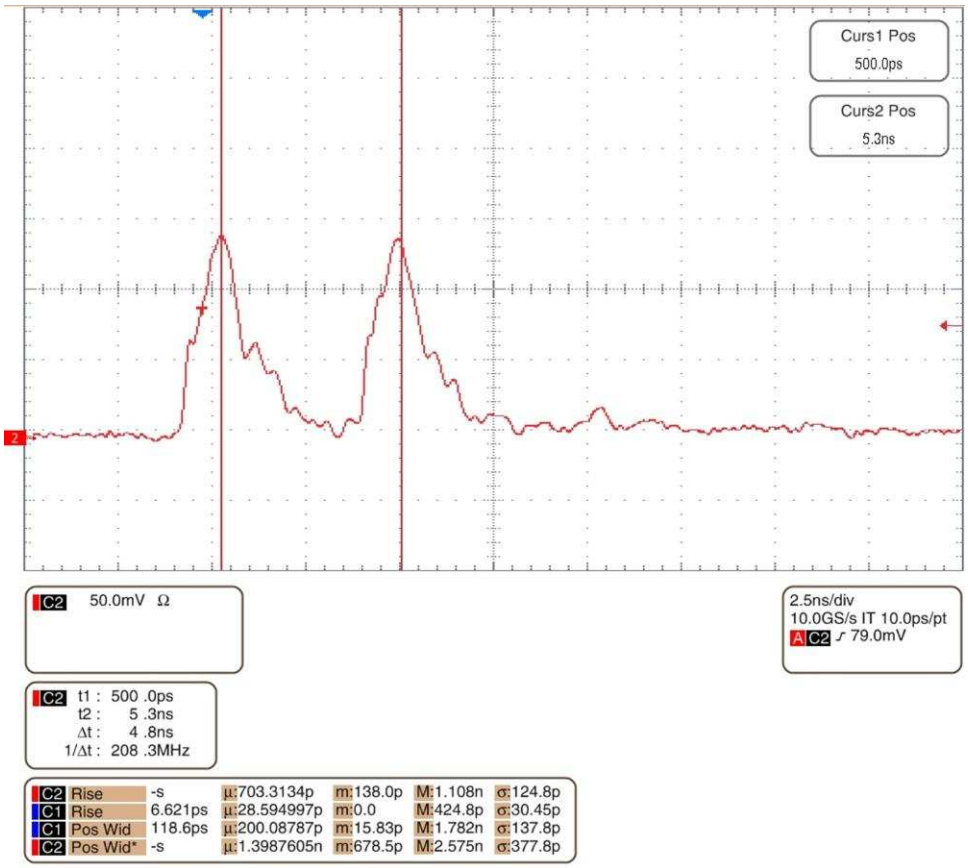

图 21. Double Light Pulse: Two 1.3-ns Pulses at 5-ns Separation

4 Design Files

4.1 Schematics

To download the schematics, see the design files a TIDA-01573.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01573.

4.3 PCB Layout

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01573.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01573.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01573.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01573.

5 Related Documentation

1. Texas Instruments, *Using the LMG1020-EVM Nano-second LiDAR EVM User's Guide*

5.1 商标

6 About the Author

ALBERTO DORONZO is a systems and applications power engineer for the high-voltage power business within Texas Instruments. Alberto earned a master degree in electrical and electronics engineering at Imperial College London in 2006.

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