

TI Designs: TIDA-050000

适用于 Xilinx® Zynq®-7、Spartan®-7 和 Zynq®-7000 FPGA 的集成电源参考设计



说明

此参考设计是一款可扩展电源，用于为 Xilinx® Artix® 7、Spartan®7 和 Zynq®-7000 系列 FPGA 器件供电。此设计接收来自标准直流电源的电源，并通过明确的 Samtec 插座端子板连接方式为 Xilinx 芯片组和 DDR 存储器的所有电源轨供电。此设计具有可扩展性，能够支持最基本的 Spartan-7 FPGA 器件和配备千兆位级收发器 (MGT) 的更复杂 Artix-7 FPGA，最高可支持配备双核 Arm® Cortex®-A9 处理器的 Zynq-7000。由于其设计可扩展性以及 Xilinx 系列器件相似性，该参考设计基于面向 Xilinx Zynq UltraScale+ MPSoC 器件的 TIDA-01480 电源参考设计而构建。

资源

TIDA-050000	设计文件夹
TPS65023	产品文件夹
TPS568215	产品文件夹
TPS62067	产品文件夹
TPS51200	产品文件夹

特性

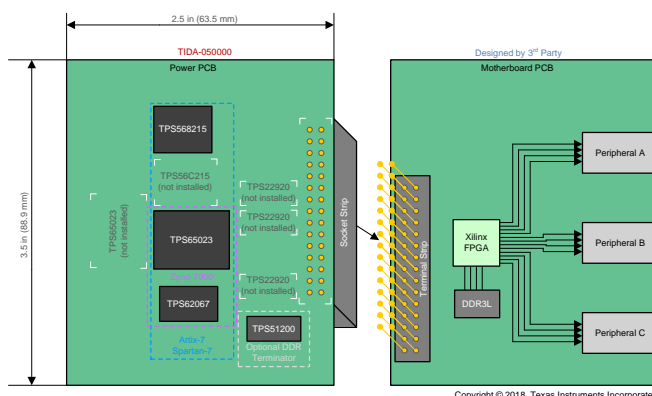
- 13 个可通过硬件配置的电源轨：
 - 八个降压转换器、四个 LDO、一个 DDR 终端
- 轻松更改硬件中的任何输出电压
 - 无需软件或定制 EEPROM/OTP
- 只需 1 个输入电压：5V/6A (30W)
- 堪称适用于以下 Xilinx 产品的理想电源：
 - Artix-7 和 Spartan-7 FPGA、Zynq-7000 和 Zynq-7000S SoC
- 小型 3.5 英寸 x 2.5 英寸 PCB，适合作为原型设计工具使用

应用

- 工业 - 工厂自动化与控制：
 - 可编程逻辑控制器 (PLC)：CPU (PLC 控制器)
 - 机器视觉：视觉计算机
 - 工业机器人：CPU 板
- 工业 - 医疗、保健与健身：
 - 成像：超声波扫描仪
- 个人电子产品 - 电视：4K 超高清电视



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1 System Description

This reference design is intended to be used as a prototyping tool for developing innovative applications using the Xilinx Artix-7 FPGA, Spartan-7 FPGA, and Zynq-7000 SoC devices.

This reference design is based on the TIDA-01480 power supply reference design for Xilinx Zynq UltraScale+ (ZU+) MPSoC devices. The ZU+ devices are more complex and require more power than the Artix-7, Spartan-7, and Zynq-7000 devices. As a result, not all devices shown on the PCB are assembled in this reference design and the solution sizes are smaller. All of the variants in the reference design can be derived from TIDA-01480 and encourage re-use of power products already approved by Xilinx for a more complex design.

The flexibility of the Xilinx FPGA and SoC devices can be overwhelming to a designer who wants to develop rapid prototypes of new products. This reference design is designed specifically to solve the problem of designing a power supply for the flexible yet complex FPGA and SoC devices. Board designers can focus on routing critical high-speed data and peripheral connections to the FPGA or SoC and let this reference design resolve concerns related to power supply design for the many required rails of the Xilinx device. The board on which the Xilinx device is mounted, or the *motherboard*, simply needs to use the specified Samtec connectors and the designer can wire his or her PCB using Xilinx terminology. The designer can combine this reference design with their newly designed Xilinx FPGA or SoC motherboard prototype, plug in an AC/DC (5 V, 6 A out) adapter to the barrel jack of this reference design, and begin testing.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER ⁽¹⁾	SPECIFICATIONS	DETAILS
Input power source	DC 5 V, 6 A (30 W); applied by a 2.5-mm ID, 5.5-mm OD barrel jack or screw terminals	YU0506 (3.1 节)
VCCINT, VCCBRAM ⁽²⁾	0.95 V/1 V, ±3%, ≤ 6.1 A	TPS568215 (3.2.2 节)
VCC_DDR, VDD ⁽³⁾ , VDDQ ⁽³⁾	1.35 V to 1.5 V (user-defined), ±V _{DDR} %, 500 mA < I _{LOAD} < 2 A	TPS62067 (3.3 节)
VMGTAVTT ⁽²⁾	1.2 V, ±3%, up to 1 A	TPS65023 DCDC1 (3.1 节)
VCCAUX, VCCADC	1.8 V, ±5%, up to 0.35 A	TPS65023 DCDC2 (3.1 节)
VMGTAVCC ⁽²⁾	1.0 V, ±2.5%, up to 0.4 A	TPS65023 DCDC3 (3.1 节)
VCC_IO	1.8 V or 3.3 V, ±5%, < 200 mA	TPS65023 LDO2 (3.1 节)
VCCO[0..]	1.2 V to 3.3 V (user-defined), ±3 %, ≤ 500 mA	Multiple options
VTT, VREFCA (VDDQ/2)	Mid-rail reference voltage for DDR memory	TPS51200 ⁽⁴⁾ (3.4 节)
Operating temperature	-40°C to +85°C	2.3 节
Solution size (area) ⁽⁴⁾	Variants 006 and 007: 1.008 in ² (650 mm ²); Variant 008: 0.723 in ² (466 mm ²)	2.1 节
Form factor (x-y dimensions)	2.5 in x 3.5 in (63.5 mm x 88.9 mm) PCB	2.2 节

(1) Parameters are listed for Variant 006. All other variants combine rails together or do not require certain rails.

(2) For some Xilinx product variants, this parameter is additionally required or cannot be combined. These modifications depend on the feature set used in the application.

(3) VDD and VDDQ are common names for the primary DDR memory power supply and not connections on the Xilinx device.

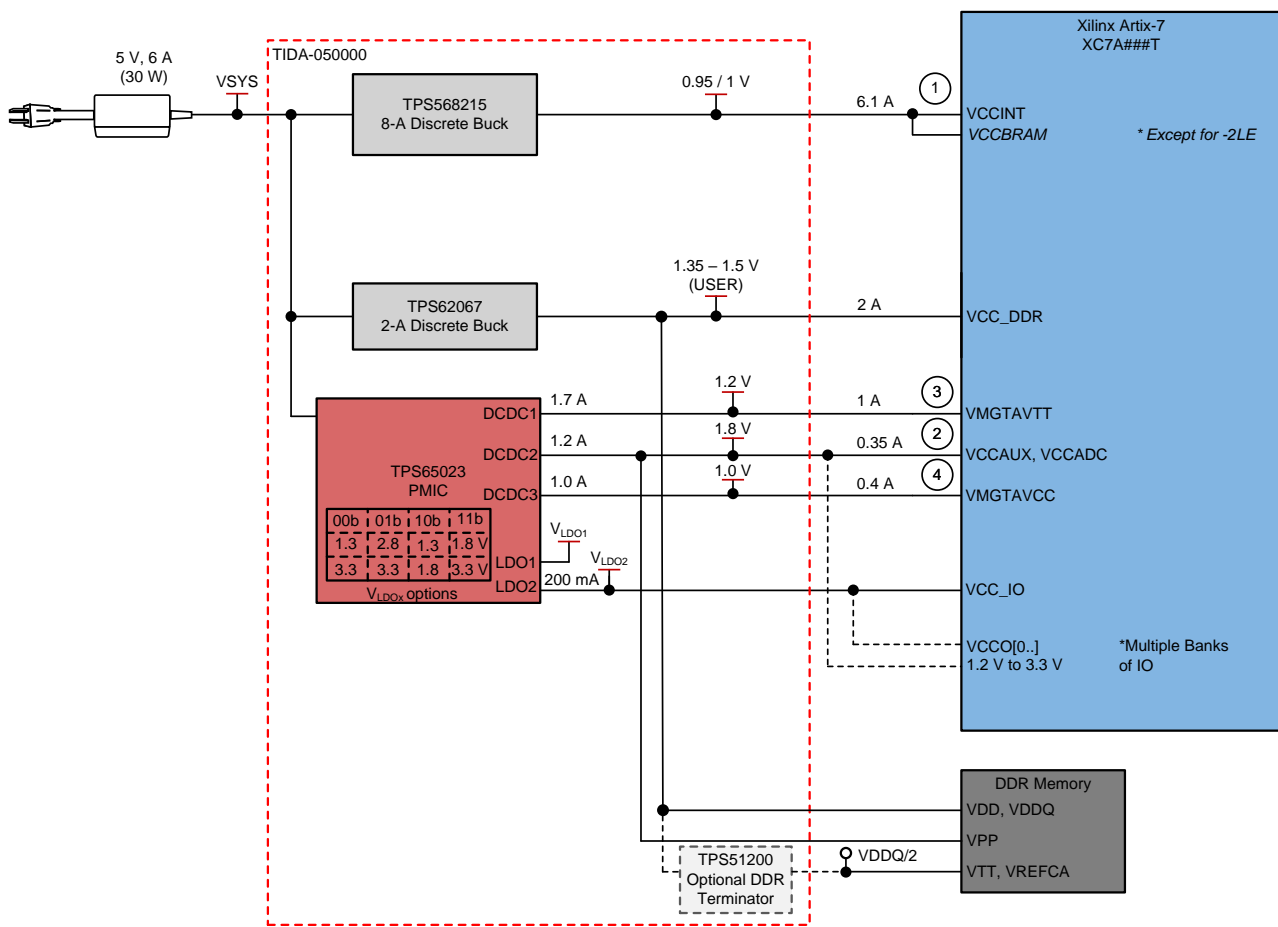
(4) A DDR terminator is optional and a voltage divider can be substituted depending on the DDR memory IC used. The TPS51200 is not included in solution size measurements.

2 System Overview

2.1 Block Diagrams

There are three (3) assembly variants of this reference design. This design is based on TIDA-01480, so the first five (5) variants are for the Zynq UltraScale+ family and are not included in this design guide. The sixth variant is for the Artix-7 FPGA (shown in 图 1), the seventh is for the Spartan-7 FPGA (shown in 图 2), and the eighth is for the Zynq-7000 SoC (shown in 图 3). The approximate solution size for each variant is listed for each respective block diagram, along with notable differences between the variants. The names used for these board variants are consistent with Xilinx nomenclature. For additional information, refer to the Xilinx references in 5 节.

2.1.1 Variant 006: Artix-7 FPGA



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图 1. Block Diagram of Design Variant 006

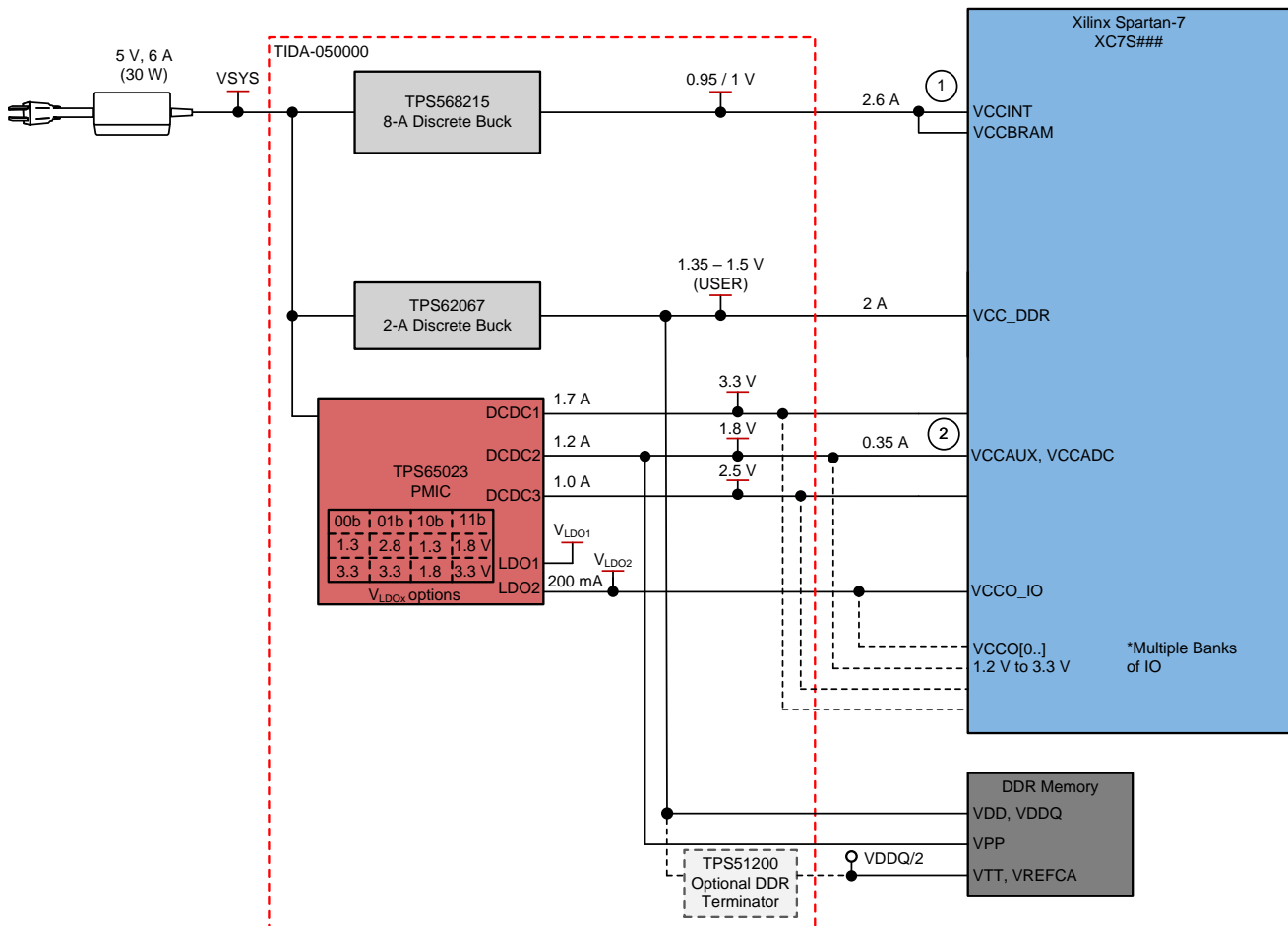
Notes about Variant 006:

- A second TPS65023 PMIC and the 12-A TPS5C215 are not required in this reference design.
- This variant of the reference design is modified for the Artix-7 FPGA and uses similar nomenclature for Xilinx power rails. Power rail names that are not matched in the schematic must be re-mapped by changing net names on the Xilinx motherboard.
- This variant of the reference design for Artix-7 is most similar to Variant 001 in TIDA-01480 for the ZU+

device family.

- Solution size = 1.008 in² (650 mm²)

2.1.2 Variant 007: Spartan-7 FPGA



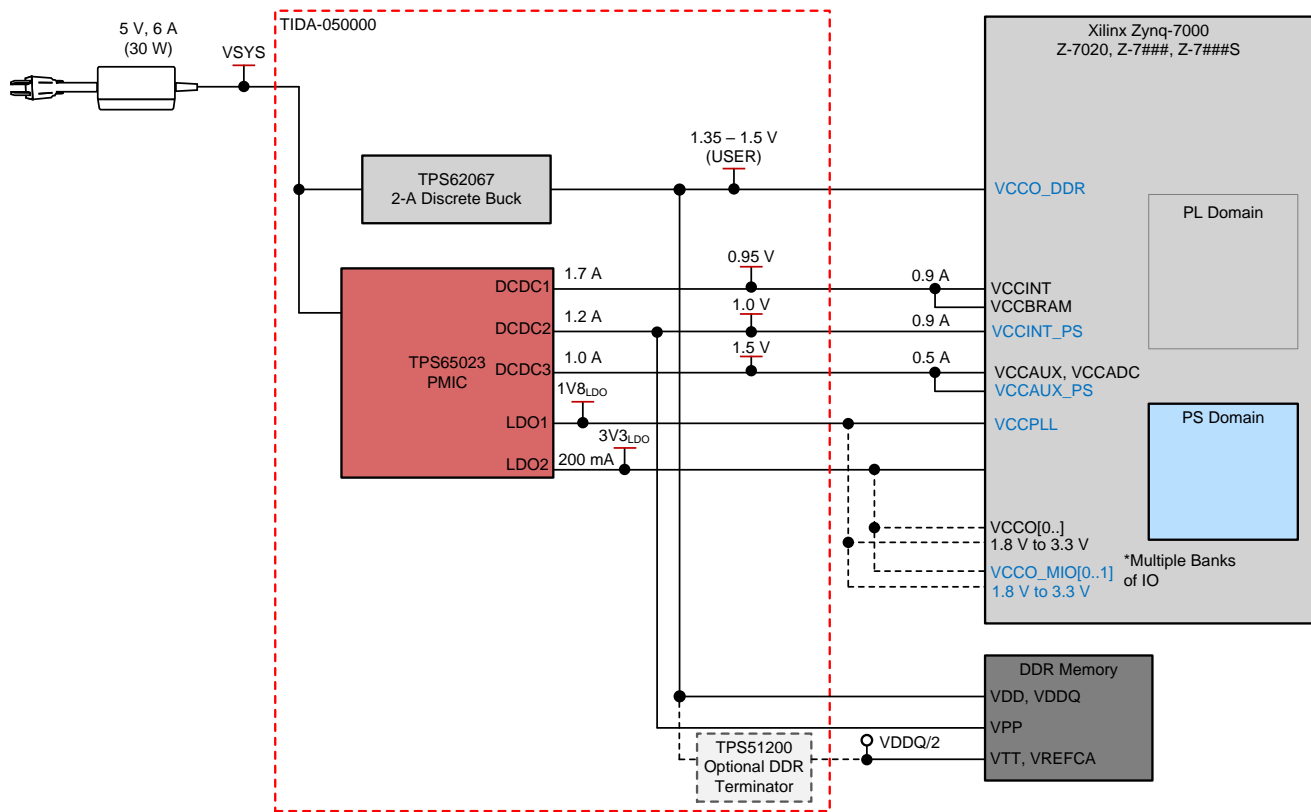
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图 2. Block Diagram of Design Variant 007

Notes about Variant 007:

- This design uses the same components as Variant 006 but has more spare rails to power I/Os of the Spartan-7 device and peripherals.
- The TPS568215 supports a load current of 8 A. The [TPS54218](#) (2 A), [TPS54418](#) (4 A), [TPS54618](#) (6 A), or [TPS54719](#) (7 A) can be substituted in the final design if lower current is required by the FPGA. The TPS54x18/TPS54x19 devices are pin-to-pin compatible with each other but not pin-to-pin compatible with the TPS568215.
- Solution size = 1.008 in² (650 mm²)

2.1.3 Variant 008: Zynq-7000 SoC



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图 3. Block Diagram of Design Variant 008

Notes about Variant 008:

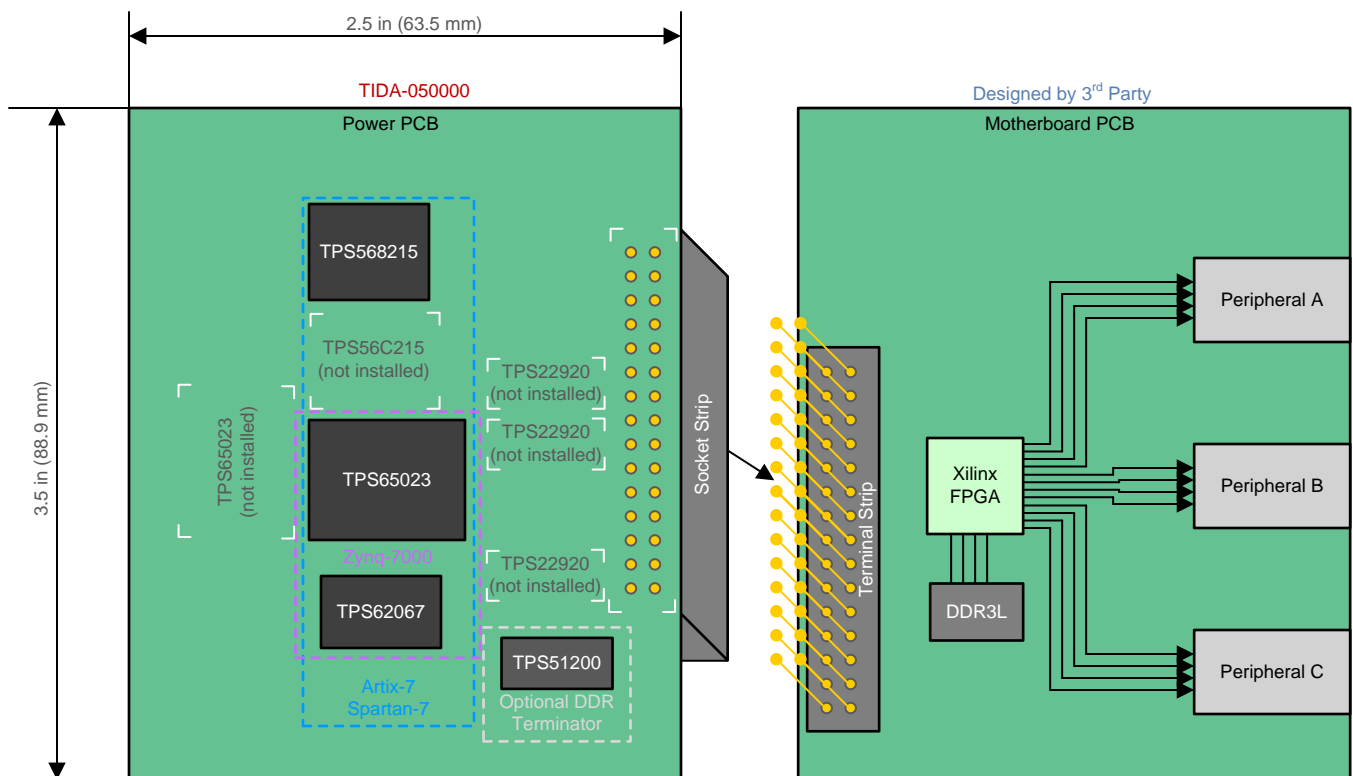
- The Zynq-7000 SoC can be the most power-optimized device targeted by this reference design. As a result, the high current 8-A TPS568215 is not included in this variant.
- In applications where up to 10 A is required by the core rail, VCCINT, the [TPS56C215](#) can be assembled on the PCB by modifying the Altium project variants. The DCDC1 rail of the TPS65023B can then be modified to an IO voltage ranging from 1.8 V to 3.3 V.
- Solution size = 0.723 in² (466 mm²)

2.2 Design Considerations

This reference design is intended to be used during the prototyping phase for any application of a Xilinx Artix-7, Spartan-7, or Zynq-7000 device. To begin prototyping, first select the part in the Xilinx product family of devices that meets the needs of the application. The next step is to design a motherboard PCB containing the Xilinx FPGA or SoC and the correct Samtec connectors to mate with this reference design. When the motherboard PCB is built, connect the two boards through the Samtec connectors and apply a barrel jack to this reference design to use it as a power supply for the motherboard. Refer to 3.1 节 for more details on the Samtec connectors.

Although intended for prototyping, the overall solution size can be critical for designers. As a result, the entire reference design (including power devices, passive components, connectors, and indicator LEDs) fits on a 3.5-in x 2.5-in PCB. The design is scalable to meet the needs of a variety of Xilinx power profiles; as a result, close attention is paid to silkscreen labeling, highlighting the area used by each device block, and top-side placement of critical power components.

For the solution size of each variant, see 2.1 节.



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图 4. Conceptual Drawing of TIDA-050000 Form Factor

2.3 Highlighted Products

2.3.1 TPS65023

The TPS65023 device is an integrated power management device for applications that require multiple power rails (see 图 5). The TPS65023 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O, and memory rails in a processor-based system. The core converter allows for on-the-fly voltage changes through a serial interface, allowing the system to implement dynamic power savings. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

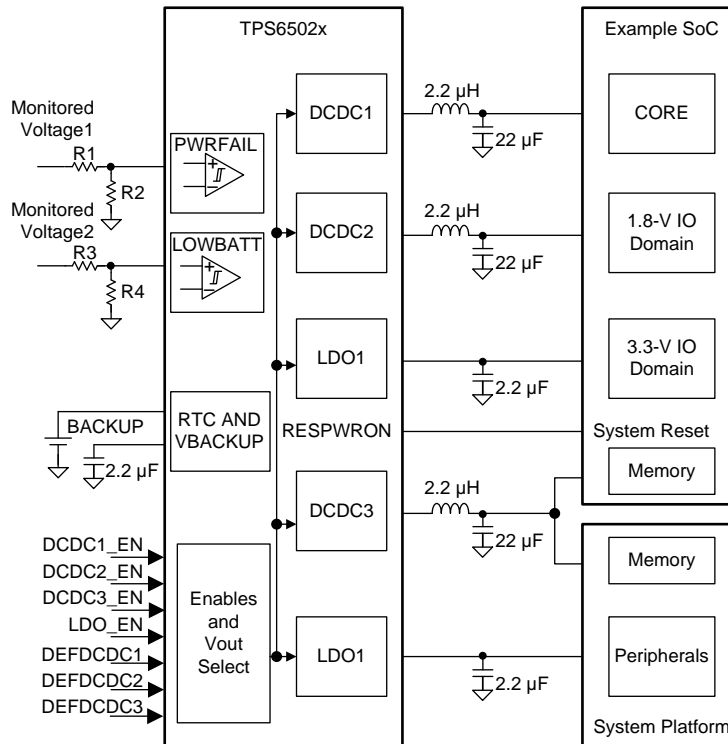


图 5. TPS65023 Simplified Application Circuit

The TPS65023 is chosen for this reference design because it is a densely integrated power management device that provides a high number of power rails in a small package, which is critical to achieve the desired solution size. The Xilinx FPGAs and SoCs are flexible and can be used in a variety of applications, and the TPS65023 output voltages can be set in hardware for scalability and flexibility in the power supply.

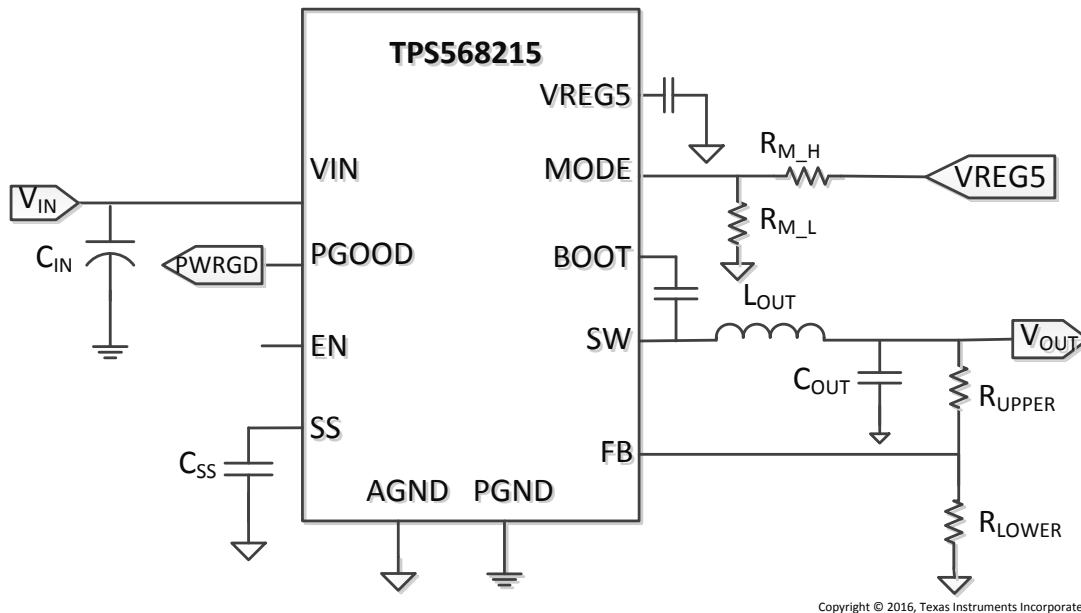
This reference design uses Revision B of the TPS65023, [TPS65023B](#), for its improved I²C performance over the previous version of the device.

For automotive applications requiring AEC-Q100 qualification, consider using the [TPS65023-Q1](#) in the assembly of this design.

For more relevant information on this device, see [TPS65023x Power Management IC for Li-Ion and Li-Polymer Powered Systems](#).

2.3.2 TPS568215

The TPS568215 is TI's smallest monolithic, 8-A synchronous buck converter with an adaptive on-time D-CAP3™ Control Mode (see 图 6). The device integrates low $R_{DS(on)}$ power MOSFETs that enable high efficiency and offer ease-of-use with a minimum external component count for space-conscious power systems. Competitive features include a very accurate reference voltage, fast load transient response, auto-skip mode operation for light load efficiency, adjustable current limit, and no requirement for external compensation. A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS568215 is available in a thermally enhanced 18-pin HotRod™ QFN package.



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图 6. TPS56C215 Simplified Application Circuit

The TPS56C215 is chosen for this design to deliver high current (up to 12 A) to the core rail of the Xilinx FPGAs. The core rail, VCCINT, requires up to 6.1 A of current for the Artix-7 variant. When a Spartan-7 Xilinx device is used, a TPS54x18 or TPS54719 device can be used instead to reduce overall cost, but this change in the final design will result in layout changes to create the PCB. The schematic of this reference design includes one TPS568215 and one TPS56C215. The end designer can use any combination of one or two TPS5x215 devices required to meet the current needs of the application because the two buck converters are pin-to-pin equivalent.

The C in TPS56C215 is hexadecimal notation, where 0xC converts to decimal 12, meaning that the TPS56C215 is rated for up to 12 A of current at the output. The TPS568215 has an identical simplified application circuit, and the TPS568215 data sheet indicates that this device rated for up to 8 A of current at the output. The circuitry for both devices in this reference design is the same, except that the TPS56C215 requires a physically larger inductor for lower DC resistance and a higher rated current capability. As a result, only the device designated as U5 on this reference design can deliver up to 12 A of continuous current.

For more relevant information on this device, see [TPS568215 4.5-V to 17-V Input , 8-A Synchronous Step-Down SWIFT™ Converter](#).

2.3.3 TPS62067

The TPS62067 is a highly efficient, synchronous step-down DC/DC converter (see 图 7). This device provides up to 2 A of output current. With an input voltage range of 2.9 V to 6 V, the device is a perfect fit for power conversion from a 5-V or 3.3-V system supply rail. The TPS62067 operates at a 3-MHz fixed frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range. The power save mode is optimized for low output voltage ripple. The TPS62067 provides an open drain power good output. The TPS62067 converter is optimized for operation with a tiny 1- μ H inductor and a small 10- μ F output capacitor to achieve smallest solution size and high regulation performance.

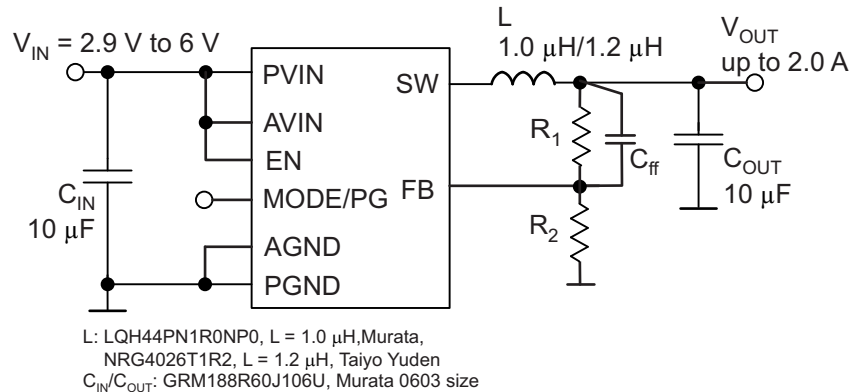


图 7. TPS62067 Simplified Application Circuit

All variants of this reference design use a dedicated rail to provide power to DDR memory's VDD (VDDQ) power input. For these applications, the TPS62067 is chosen to supply up to 2 A of current with a hardware-configurable output voltage to support DDR2, LP-DDR2, DDR3, DDR3L, or LP-DDR3. The default assembly of this reference design sets this voltage to 1.35 V for DDR3L.

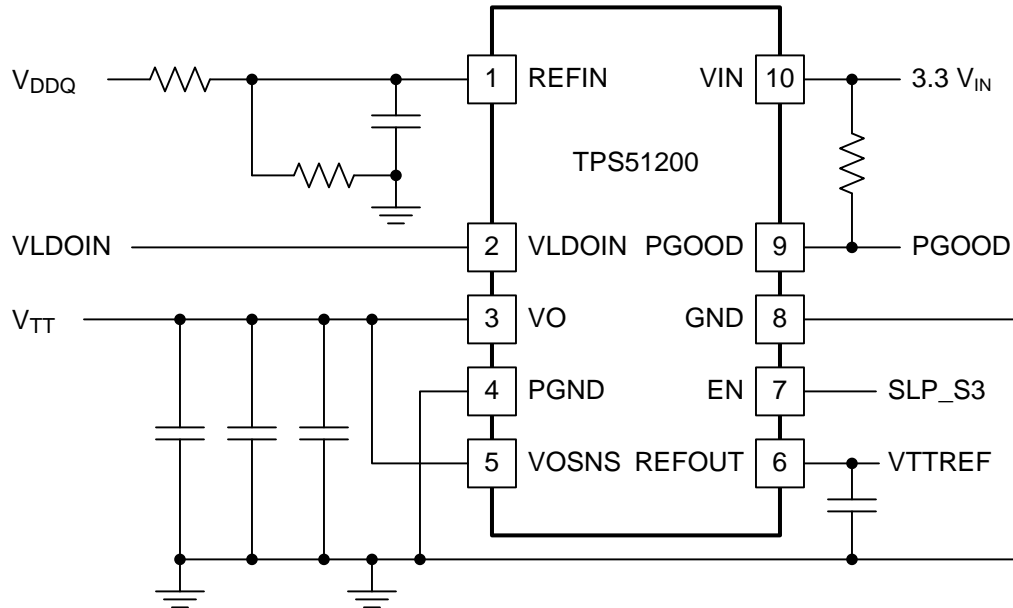
For automotive applications requiring AEC-Q100 qualification, consider using the [TPS62067-Q1](#) in the assembly of this design.

The TPS62067 features the power-good (PG) output function on pin 6 and is used in this reference design. To use the MODE function (input) on pin 6 to force PWM at a fixed switching frequency (instead of the PG ability), use the [TPS62065](#) and modify the schematic accordingly to change the wiring of the PG output to an input for MODE selection. The AEC-Q100 automotive qualified version of this device, [TPS62065-Q1](#), is also available.

For more relevant information on this device, see [TPS6206x 3-MHz, 2-A, Step-Down Converter in 2-mm x 2-mm SON Package](#).

2.3.4 TPS51200

The TPS51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration (see 图 8). The TPS51200 maintains a fast transient response and requires a minimum output capacitance of only 20 μF . The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT bus termination. In addition, the TPS51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.



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图 8. TPS51200 Simplified DDR Application Circuit

If a DDR terminator is required by the application, the TPS51200 is used in the reference design because it simply and reliably produces an output voltage at the VO pin (V_{TT} node) that is equal to the voltage at the REFIN pin (half of the voltage labeled VDDQ) by either sinking or sourcing current into the V_{TT} node.

For more relevant information on this device, see [TPS51200 Sink and Source DDR Termination Regulator](#).

2.4 System Design Theory

2.4.1 Buck Converter Output Voltages

All DC/DC buck converters set the output voltage using the same principle. A resistor divider is connected from the output voltage to GND, and the center node of the two resistors is connected to the feedback pin of the converter. Although the name of the feedback pin and the terminology for its voltage can differ from device to device, the same general equation is used to set the voltage for all of the buck converters in this reference design.

The feedback voltage (commonly referred to as V_{FB} or V_{REF}) is a constant for each buck converter and can easily be found in the data sheet for that device. For the TPS65023, the feedback voltage for the DC/DC buck converters is called $V_{DEFDCDCx}$. V_{OUT} is the desired output voltage for the buck converter. Generally speaking, R_2 is selected first and is treated as a constant to solve for R_1 using 公式 1.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} \right) - R_2 \quad (1)$$

After two resistors are selected from the component library and placed in the schematic, the output voltage can be calculated using 公式 2 to ensure the voltage is within the desired supply voltage range.

$$V_{OUT} = V_{FB} \times \left(\frac{R_1 + R_2}{R_2} \right) \quad (2)$$

图 9 shows an example of how to set the output voltage for DCDC3 of the TPS65023 using an external resistor divider. This example is shown because wiring the TPS65023 is the most complex in this reference design and the same theory is used for all buck converters.

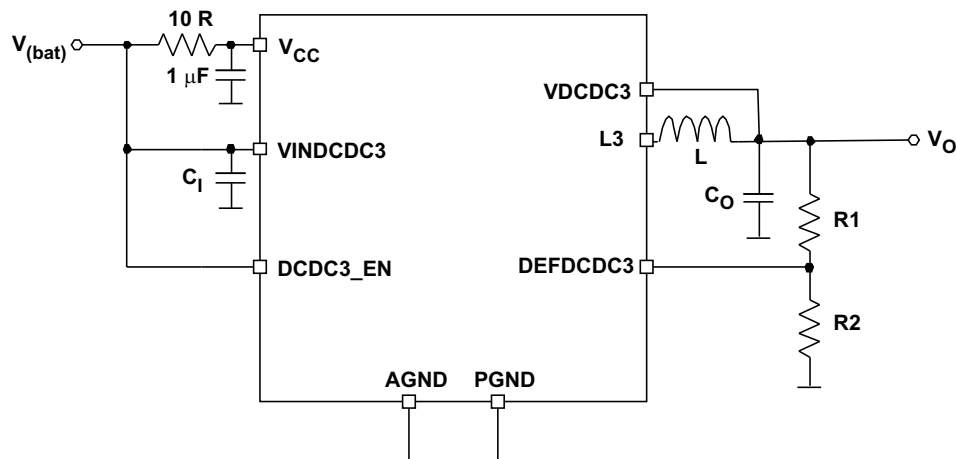


图 9. TPS65023 External Resistor Divider for DCDC3

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

The only hardware required to power on this reference design at full load is a DC power supply capable of delivering 5 V at a current of at least 6 A. The simplest way to apply this power is by connecting a barrel jack plug of an AC/DC adapter into the receptacle J1 with an inner diameter (ID) of 2.5 mm and an outer diameter (OD) of 5.5 mm, where the internal *tip* has positive (+) polarity and the external *sleeve* has negative (–) polarity. An AC/DC adapter with generic part number *YU0506* is commonly available and meets these requirements.

If an AC/DC adapter meeting these specific requirements is not available, a DC power supply in a lab can be connected to screw terminal J2 by connecting the "+" terminal to pin 1, labeled *5V IN*, and the "-" terminal to pin 2, labeled *GND*.

When the design is used for prototyping an application of the Xilinx Artix-7 FPGA, Spartan-7 FPGA, or Zynq-7000 SoC, the mating Samtec connectors for J6 and J7 must be used and must be mounted with relative positions to each other matching the placement of J6 and J7 on the bottom of this board.

- J6 (MPS-04-7.70-01-L-V) mates with MPT-04-6.30-01-L-V:
 - Pin 1 of J6 has X,Y coordinates of 1900 mil, 2472 mil (48.26 mm, 62.789 mm)
- J7 (BSE-060-01-L-D-A) mates with BTE-060-09-L-D-A:
 - Pin 1 of J7 has X,Y coordinates of 1944.25 mil, 197 mil (49.383 mm, 5.004 mm)

The distance from the center of pin 1 on J6 to the center of pin 1 on J7 is +44.74 mil (1.136 mm) horizontally on the X-axis and –2275 mil (57.785 mm) vertically on the Y-axis.

3.2 Testing and Results

The tests performed in this section are completed on the fully populated TIDA-01480 PCB, which contains some components not included in any or all variants of this reference design. The tests required for this reference design are a subset of the tests completed and documented in this section.

3.2.1 Test Setup

A handheld digital multimeter measures the DC output voltages of each power rail output provided by this reference design. 图 10 shows the setup for this test and highlights the measurement locations probed with the multimeter.

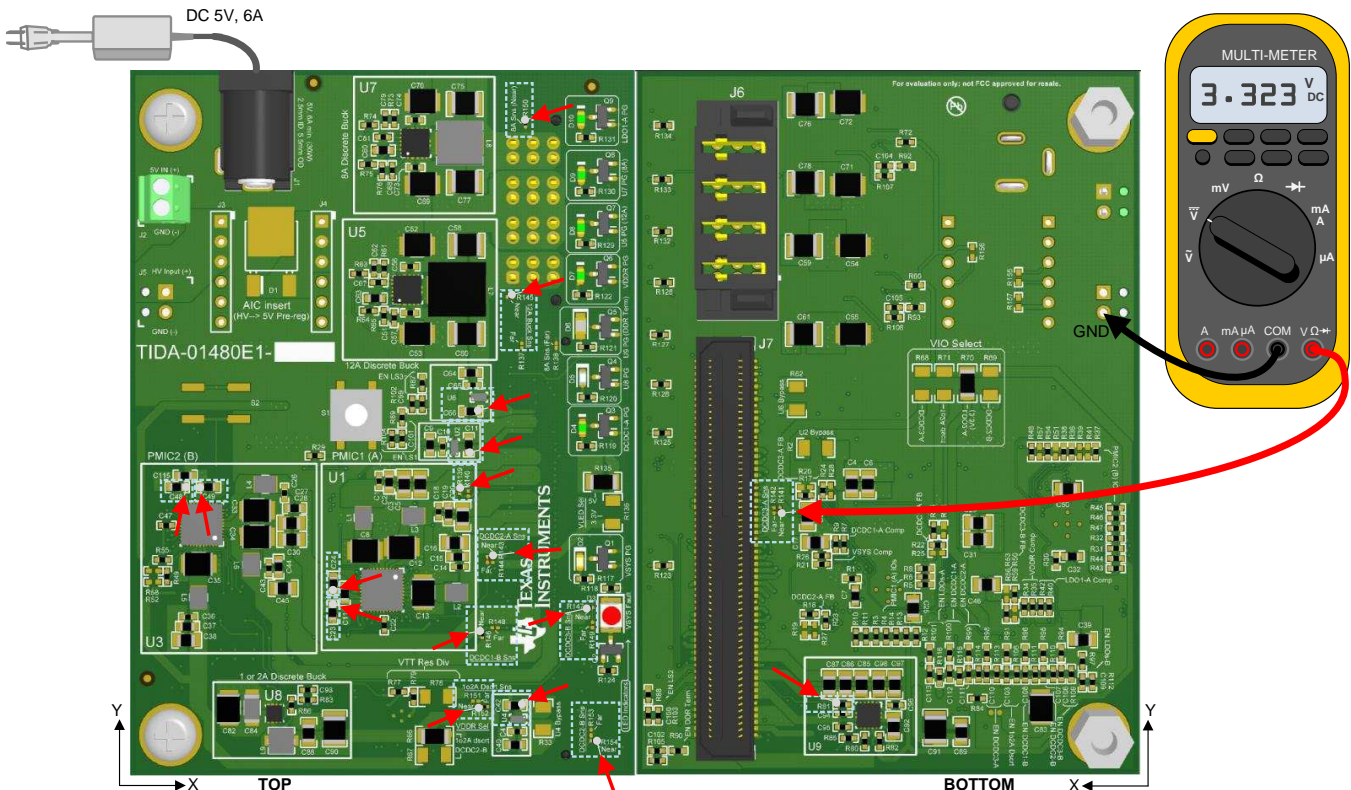


图 10. Setup and Measurement Locations for DC Voltage Measurements

表 2 lists the results of these simple measurements.

A standard DC power supply, an electronic load, and an oscilloscope are used to take load measurements on the output power rails. The voltage is measured at the output capacitor of the DC/DC switching regulator where the output voltage is being sensed by the device. 图 11 shows the setup for these tests. The VCC_12A rail provided by the TPS56C215 is shown as an example of how the load is applied and how the measurement is taken with the oscilloscope probe. A current probe (not depicted) is also used to monitor the load current and slew rate during load steps.

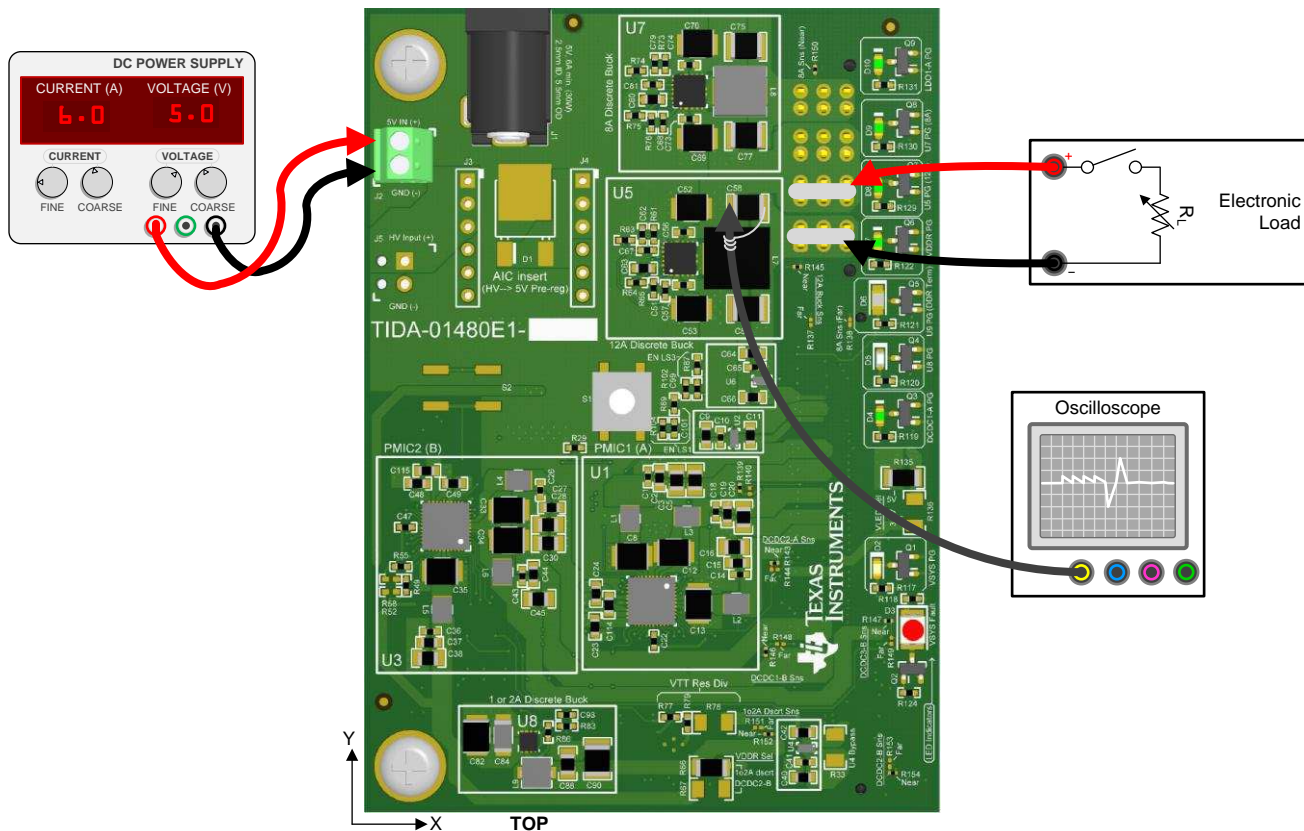


图 11. Setup for Measuring Output Voltages with Load Applied

3.2.2 Test Results

表 2 lists the power rails measured for DC output voltage using the default component values populated on this reference design. The measurements are done at no load with a handheld multimeter and the component designator, where the measurement is taken, is also listed.

表 2. DC Output Voltage Measurements

POWER RAIL NAME	DEVICE COMPONENT DESIGNATOR	MEASUREMENT COMPONENT DESIGNATOR	DESIRED VOLTAGE (V)	MEASURED VOLTAGE (V)
VDCDC1_A	U1	R139	1.2	1.204
VDCDC2_A	U1	R143	1.8	1.804
VDCDC3_A	U1	R141	3.3	3.323
VLDO1A_1V8	U1	C23	1.8	1.802
VLDO2A_3V3	U1	C24	3.3	3.301
VDCDC1_B	U3	R146	0.9	0.902
VDCDC2_B	U3	R154	1.8	1.806
VDCDC3_B	U3	R147	0.85	0.862
VLDO1_B	U3	C48	1.8	1.797
VLDO2_B	U3	C49	3.3	3.293
VDCDC1_A_LS1	U2	C11	1.2	1.204
VDCDC2_B_LS2	U4	C42	1.8	1.806
VCC_12A	U5	R145	0.9	0.896
VCC_8A	U7	R150	0.9	0.894
VCC_1or2A	U8	R152	1.36	1.378
VCC_12A_LS3	U6	C66	0.9	0.896
VTT_DDR	U9	R81	0.68	0.689

图 12 shows the test results measuring the output voltage of VDCDC1_A with no load applied. Note that PFM mode is entered automatically by the TPS65023B device. This feature can be disabled by writing to the device with I²C commands.

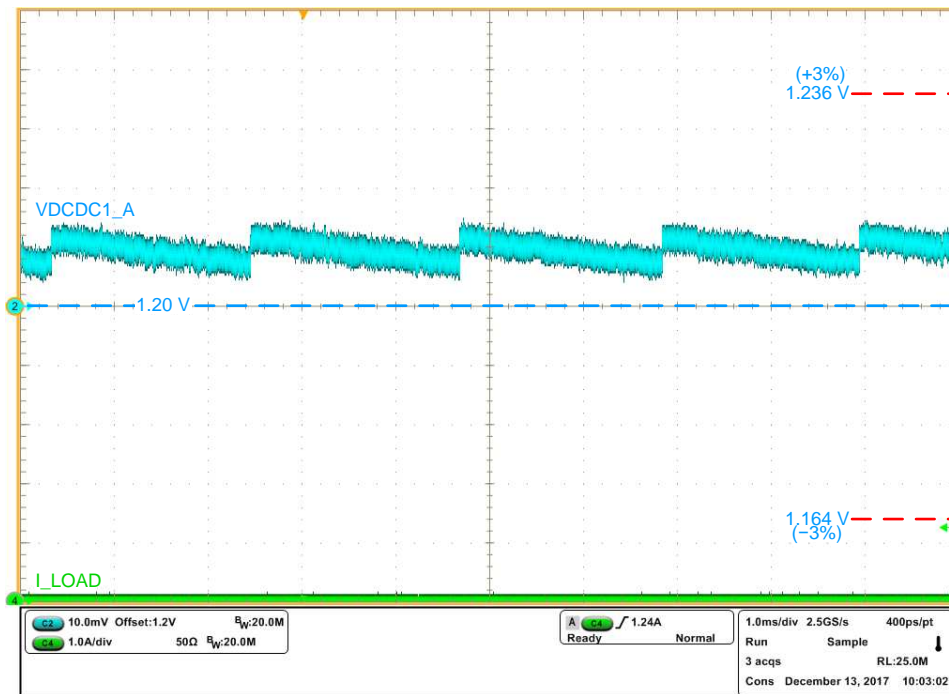


图 12. VDCDC1_A No Load Test

图 13 shows the test results measuring the output voltage of VDCDC1_A with a full load of 1.7 A applied. Note that the TPS65023B device is in PWM and switching continuously.

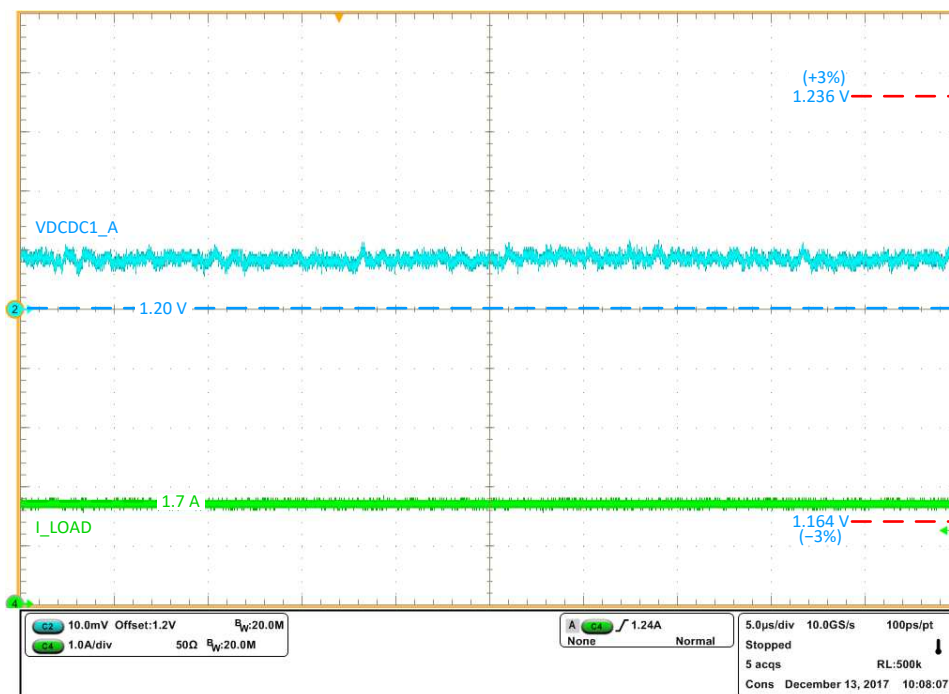


图 13. VDCDC1_A Full Load Test

图 14 显示了测试结果，测量 VDCDC1_A 的输出电压，负载从 0 A 到 1.7 A (100%) 应用。请注意，电子负载设置为最大 slew 率为 25 A/μs，但此 slew 率并未完全实现，因为 TPS65023B 设备的软启动功能和电源轨的大输出电容。

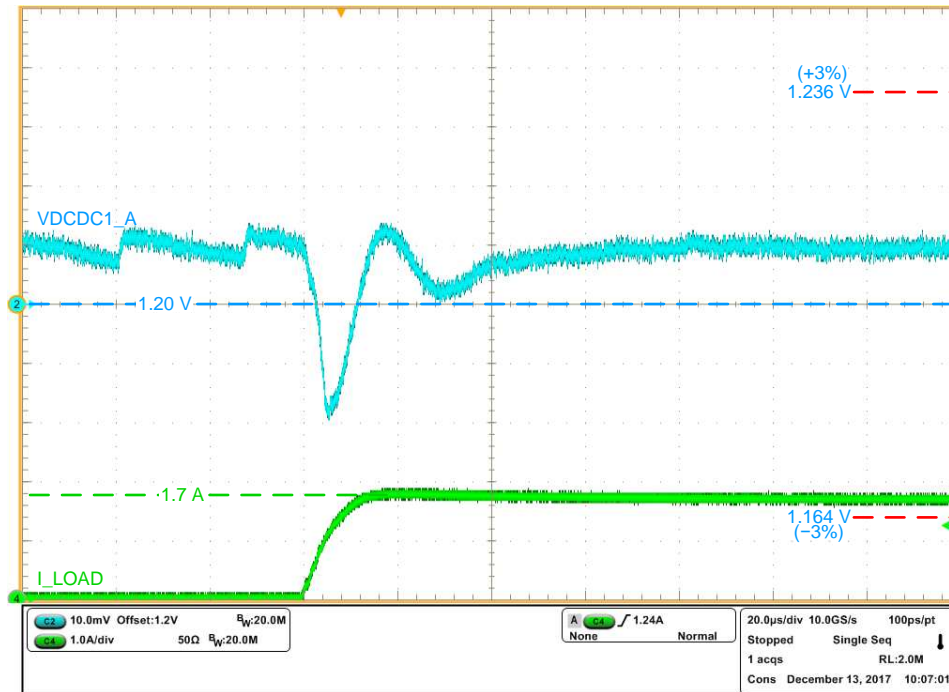


图 14. VDCDC1_A Load Step Test

图 15 显示了测试结果，测量 VCC_8A 的输出电压，无负载应用。请注意，TPS568215 设备会自动进入 PFM 模式。此功能可以通过更改连接到设备 MODE 引脚的电阻分压器来禁用。

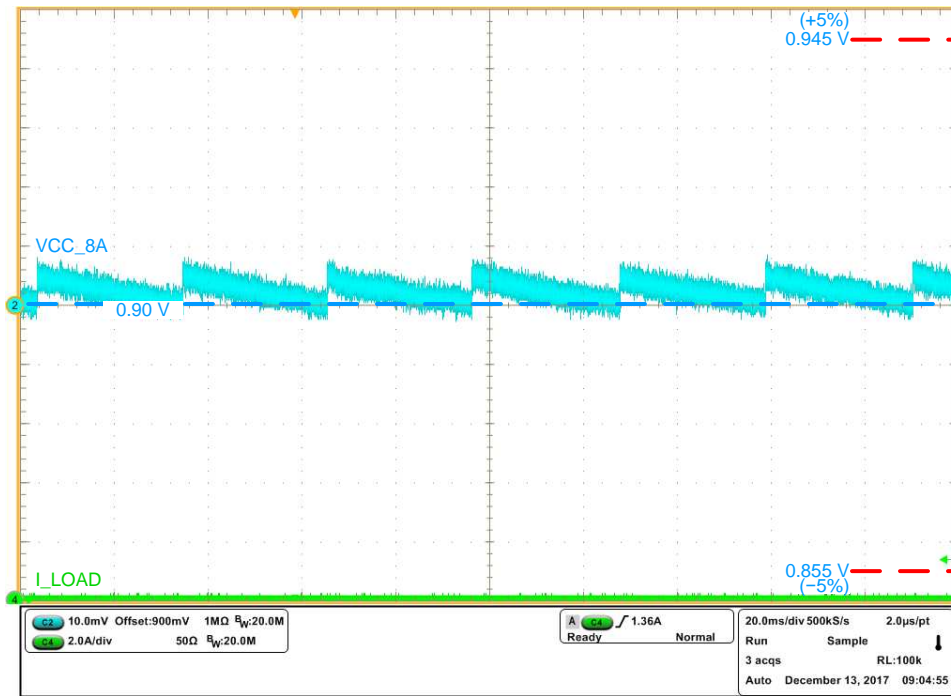


图 15. VCC_8A No Load Test

图 16 shows the test results measuring the output voltage of VCC_8A with a full load of 6.55 A applied as required by the application. Note that the TPS568215 device is in PWM and switching continuously.

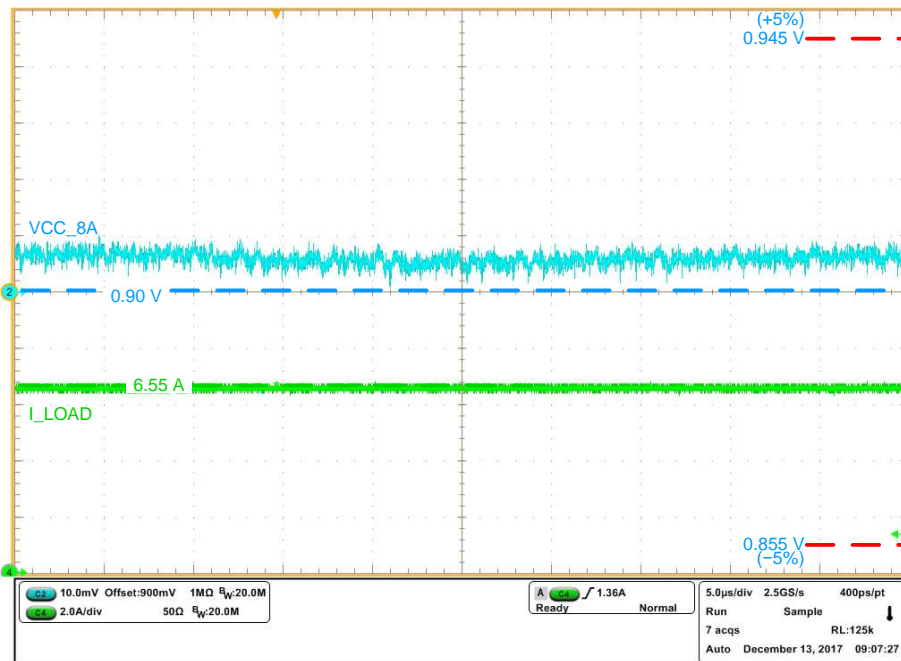


图 16. VCC_8A Full Load Test

图 17 显示了测试结果，测量 VCC_8A 的输出电压，负载从 0 A 到 6.55 A (100%) 应用。该应用只需要 25% 的全负载，但 TPS568215 能够在 100% 负载步骤中保持调节。请注意，电子负载设置为最大 slew 率 25 A/ μ s，但这个 slew 率没有完全实现，因为 TPS568215 设备的软启动功能和电源轨的大输出电容。

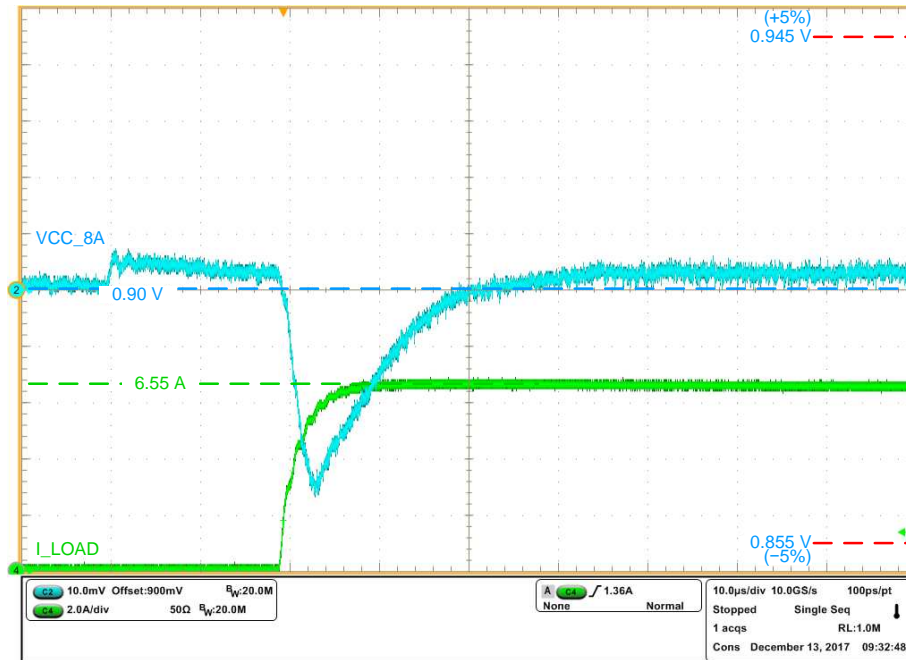


图 17. VCC_8A Load Step Test

图 18 显示了测试结果，测量 VCC_12A 的输出电压，没有负载应用。请注意，TPS56C215 设备会自动进入 PFM 模式。此功能可以通过更改连接到设备 MODE 引脚的电阻分压器来禁用。

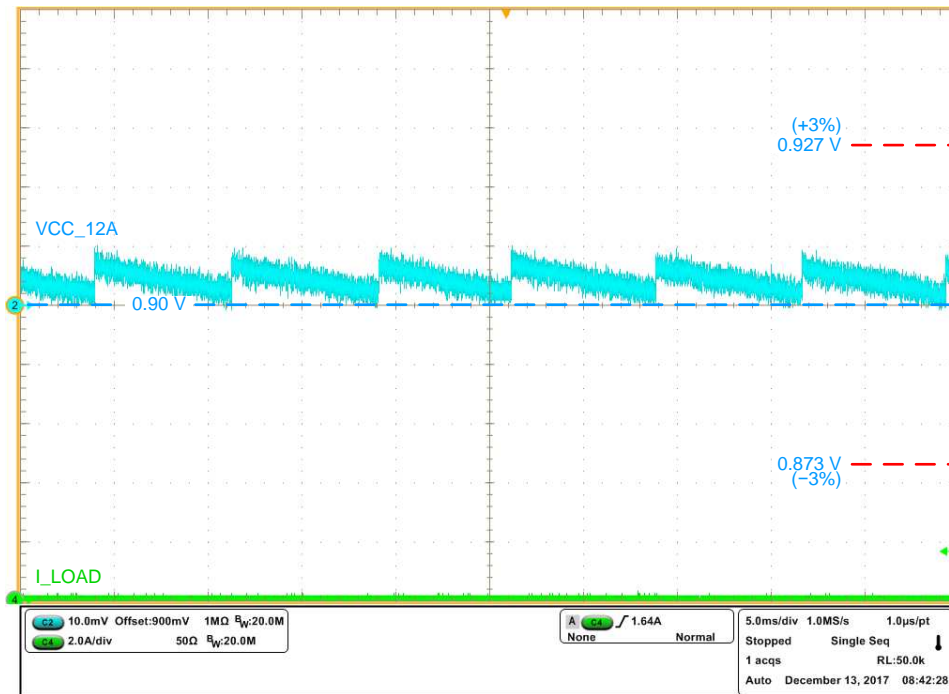


图 18. VCC_12A No Load Test

图 19 shows the test results measuring the output voltage of VCC_12A with a full load of 9.1 A applied as required by the application. Note that the TPS56C215 device is in PWM and switching continuously.

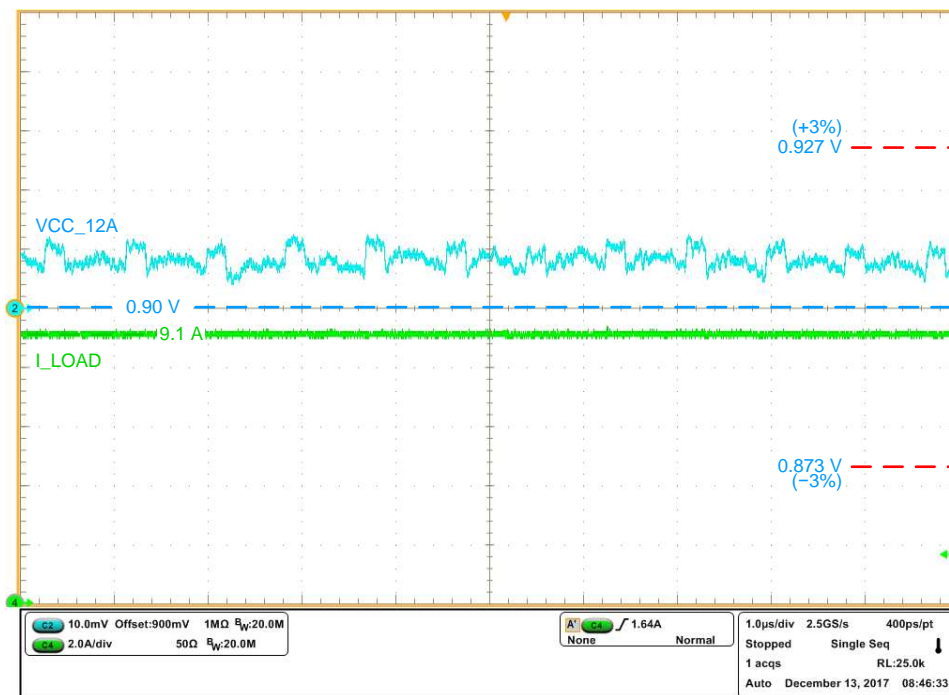


图 19. VCC_12A Full Load Test

图 20 显示了测试结果，测量了 VCC_12A 的输出电压，负载从 5.28 A 到 9.1 A (58% 到 100%) 应用。该应用只需要满负载的 25%，负载步骤测量所描绘的范围是始终满足输出电压所需的 3% 公差的最大范围。请注意，电子负载设置为最大 slew 率为 25 A/μs，但此 slew 率并未完全实现，因为 TPS56C215 器件的软启动特性和电源轨的大输出电容。

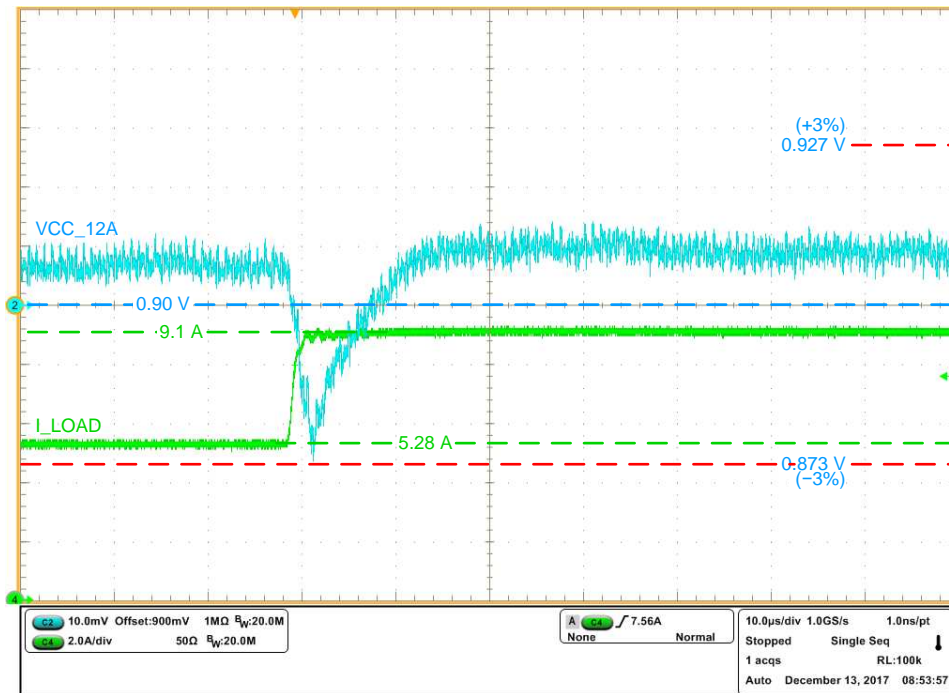


图 20. VCC_12A Load Step Test

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-050000](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-050000](#).

4.3 PCB Layout Recommendations

The layout guidelines in each device's data sheet are used as a starting point for placement of critical components for the respective buck converter. For additional guidance on layout, see the EVM User's Guides consulted in 5 节.

This reference design is a six (6) layer PCB with 1-oz copper thickness and a total thickness of 62 mils. The top (first) and bottom (sixth) layers are used for component placement and for routing signals and power. The second and fifth layers are solid copper GND planes. The innermost layers (third and fourth) are reserved for routing low-speed digital signals and low-current power traces. An example of a low-current power trace would be any of the 200-mA LDOs for the two TPS65023 devices, which have an average trace width of 30 mils.

The shortest routing distance from input to output is for the TPS56C215 12-A converter and for the TPS568215 8-A converter. For these two high-current rails, the input power from VSYS is connected by a solid copper polygonal pour directly to both sets of input capacitors with an approximate distance of 750 mils (19 mm). The output inductor is connected by a solid copper pour directly to the blade of J6 with an approximate distance of 150 mils (3.8 mm). The total worst-case distance from input (VSYs) to output (VCC_12A or VCC_8A), including the device, is less than 2 inches with all routing on the top layer.

All buck converters have at least one pin named AGND, and all components that must connect to AGND (sensitive analog signals such as feedback resistors, comparator resistors, and mode selection resistors) are connected to the AGND pin of the device using a *star-point* connection. These AGND star-points connect to the GND plane with a single via connected to the GND net and these vias are located near an AGND pin for each device (five AGND-to-GND vias total, one for each device designated as U1, U3, U5, U7, and U8).

To save space, large bypass capacitors that appear in sets of two (2, 4, 6, or 8) alternate placement on top and bottom layers of the PCB with multiple vias placed around the capacitor pad to allow current flow to and from opposite layers of the board. For example, U5 (TPS56C215) requires four output bypass capacitors. C58 and C60 are placed on the top layer while C59 and C61 are placed on the bottom layer with five vias surrounding each pad.

Other than thermal relief vias for devices and drill holes for through-hole components, all vias have a hole size of 7.9 mils and a 14-mil diameter (3-mil annular ring). The minimum trace width for low-speed low-current signal routing is 4 mils around the TPS65023 devices and 6 mils anywhere else on the board.

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-050000](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-050000](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-050000](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-050000](#).

5 Related Documentation

1. Texas Instruments, [TPS65023B/TPS650231EVM User's Guide](#)
2. Texas Instruments, [TPS568215EVM-762 8-A, SWIFT™ Regulator Evaluation Module User's Guide](#)
3. Texas Instruments, [TPS62065/TPS6206567EVM User's Guide](#)
4. Texas Instruments, [Using the TPS51200 EVM Sink/Source DDR Termination Regulator User's Guide](#)
5. Xilinx, [XILINX ARTIX-7 FPGAS: New Performance and Bandwidth Standards for Power-Limited, Cost-Sensitive Markets](#)
6. Xilinx, [Cost-Optimized Product Selection Guide](#)

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6 About the Author

BRIAN BERNER joined Texas Instruments as an applications engineer in 2011 after earning his bachelor of science and master of science degrees in electrical engineering from Lehigh University. Prior to joining the Integrated Power Management team, Brian worked as an applications engineer supporting customers using the [TPS6598x](#) family of USB Type-C and PD Port Controllers while developing technical content to aid in product development.

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