TI Designs：TIDA-060020
支持 HART 的 PLC 模拟输入模块参考设计

说明

此参考设计是一个单通道、4mA 至 20mA 的模拟输入模块，支持高速可寻址远程传感器 (HART) 通信协议，可实现场发射器和可编程逻辑控制器 (PLC) 之间的双向数字通信。代表主要变量的回路电流流经电流感应电阻器，产生与之成正比的电压，该电压由精度 Δ-Σ 模数转换器 (ADC) (ADS1260) 进行数字化。DAC8740H HART®调制解调器用于此设计中，以在整个电流回路中实现 HART 通信。ADS1260 和 DAC8740H 与一个外部微控制器相连接，该微控制器控制着 ADS1260 采样，并包含支持 HART 协议的 HART 软件栈。该设计还 具有 数字隔离、宽电源电压范围和用于 ADC 的高精度外部电压基准。

资源

TIDA-060020	设计文件夹
DAC8740H	产品文件夹
ADS1260	产品文件夹
REF3425	产品文件夹
TLV760	产品文件夹
ISO7741	产品文件夹
ISO7742	产品文件夹

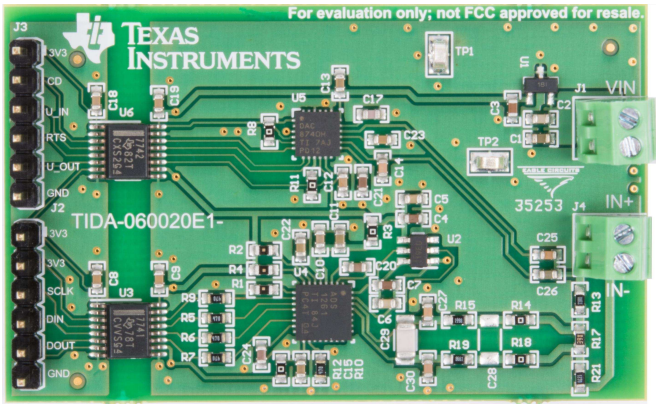
TI E2E™ Community 咨询我们的 E2E™ 专家

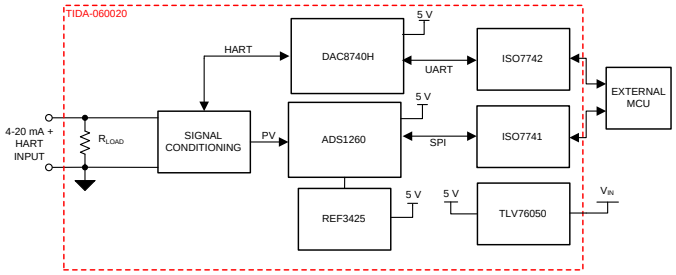
特性

- 采用 HART 调制解调器的 4mA 至 20mA 模拟输入
- 高精度回路电流测量 < 0.05% FSR TUE
- 已经过 HART 物理层合规性测试
- 6V 至 28V 电源输入
- 20 有效位数的分辨率可进行回路电流测量

应用

- 工厂自动化与控制
- 楼宇自动化





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

This analog input module reference design accepts traditional 4-mA to 20-mA inputs and supports HART enabled transmitters with the HART communication protocol. The key components are the ADS1260 for sensing the loop current and the DAC8740H HART modem, which provides digital frequency shift key (FSK) communication over the current loop. The input module acts as the HART master and requests data from the field transmitter (i.e. the HART slave). The ADC and HART modem are supported by a low-dropout (LDO) power supply, a precision voltage reference, and digital isolators. These components, along with the ADC and HART modem, create a complete system-level design for HART-enabled analog input modules. This design guide covers the key considerations to achieve HART compliance with highly accurate loop-current measurements.

1.1 Key System Specifications

表 1 lists key specifications for this reference design.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Supply input voltage	6 V - 28 V	节 2.3.4
Load resistance	260 Ω	节 2.2.2
ADC effective resolution	20 bits	节 3.2.2.9
ADC sampling rate	20 SPS	节 2.2.3
Total unadjusted error (DC loop current)	<0.05% FSR at 25°C	节 2.2.2
Current input range	3.5 mA - 23.5 mA	节 2.2.2
Power consumption	220 mW at 24 V	节 2.3.4
Board dimensions	58 mm × 36 mm	节 4.3.1
HART signal amplitude	400 mV_{PP} to 800 mV_{PP}	节 3.2.2.1
HART FSK frequencies	1200 Hz ±1%, 2200 Hz ±1%	节 3.2.2.1
HART PHY compliance	Physical layer tests completed for low impedance device	节 3.2.1.1

2 System Overview

2.1 Block Diagram

图 1 shows a block diagram of this reference design.

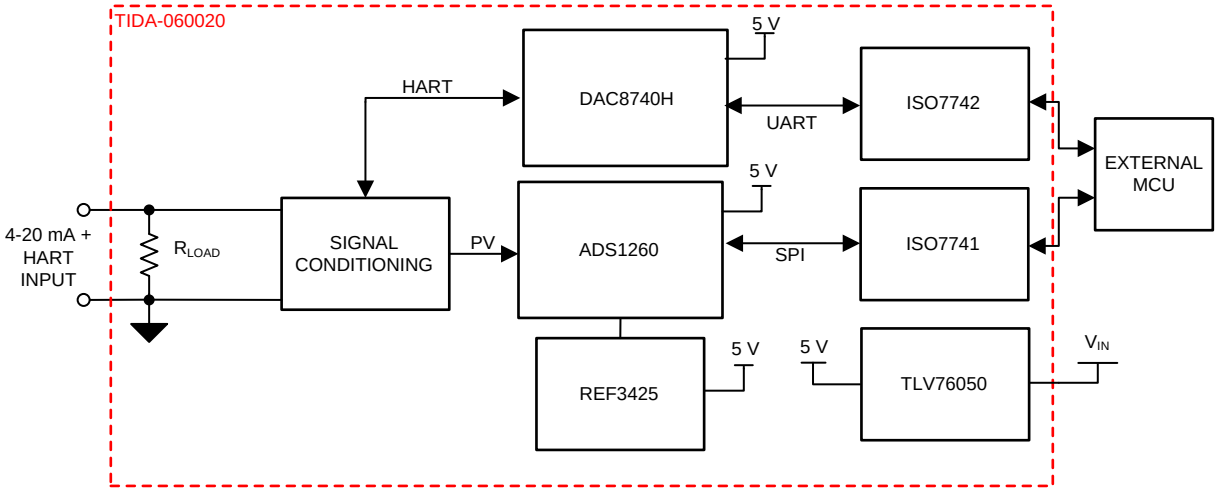


图 1. TIDA-060020 Block Diagram

2.2 Design Considerations

2.2.1 Overview of a HART Enabled Analog Input Module

In 4-mA to 20-mA systems, the analog input module is responsible for digitizing the loop current value by sensing the voltage across a known load resistor. The value of the DC loop current represents the primary variable and the transmitter regulates this current based on the measurement of a sensor. The analog input module can be used with both 2-wire and 3-wire loop current transmitters.

图 2 shows a simplified circuit diagram of a HART enabled analog input module. When the current flows across the load resistor, R1, a proportional voltage is induced across R1. This voltage is equal to the loop current multiplied by the load resistance. The ADC samples and converts this voltage into a digital value that can be read by a microcontroller. R2 and C1 form a simple low-pass filter to remove out-of-band noise present at the ADC input. C2 and C3 isolate the DC from the modem input and output to the high side of the load resistor.

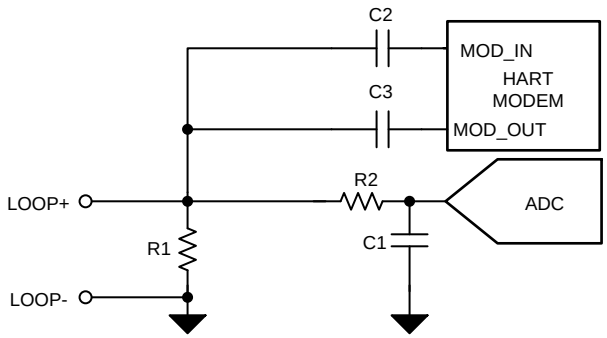


图 2. Simplified Analog Input Module

Because the transmitter regulates the loop current, the HART signal is transmitted as a 1-mA_{PP} current waveform that is AC-coupled to the DC loop current value. The input module directly couples the HART voltage signal across the load resistor when the input module is transmitting HART. The HART modem demodulates the voltage signal created across R1 by the 1-mA_{PP} HART current waveform.

Specific filtering is required to separate the analog signal from the HART signal at the analog input module. The analog signal is restricted to very low frequency, imposing a restriction on the transmitter analog rate of change. The HART modem requires a band-pass filter to remove both the analog signal and limit high frequency noise. 图 3 shows a simplified illustration of the analog and HART signal bands.

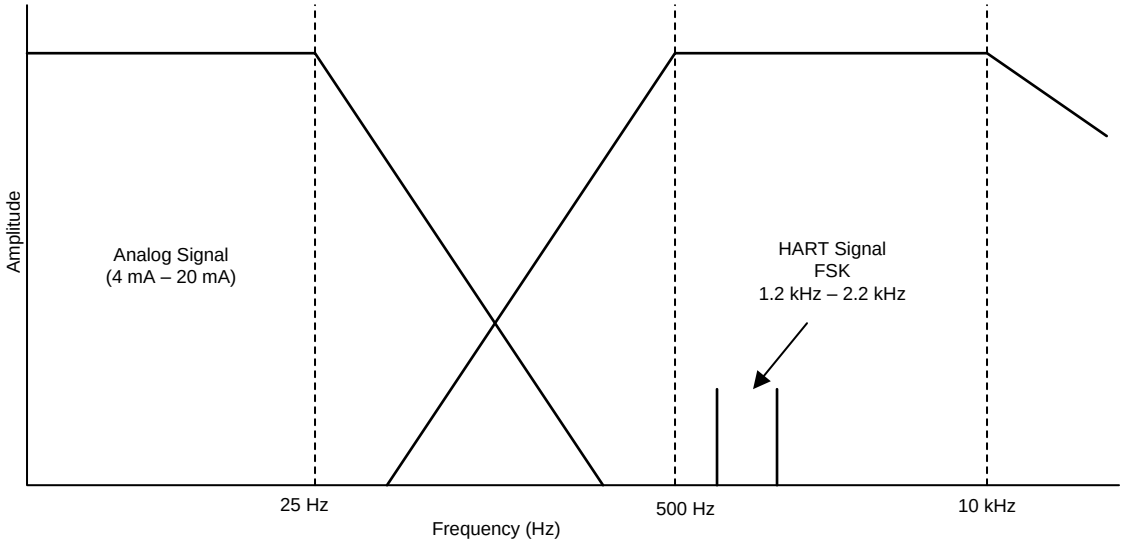


图 3. Analog Signal and HART Frequency Bands

2.2.2 Load Resistor Considerations

The load resistor is used both for sensing the loop current and for converting the HART current waveform into a voltage signal. The HART specification requires a load resistance between 230 Ω and 600 Ω. The simplified configuration illustrated in 图 2 uses a single load resistor but, at full-scale current, creates a high voltage at the input of the ADC that may exceed the absolute input range. At a 23.5-mA input, the voltage at LOOP+ is 250 Ω × 23.5 mA = 5.875 V, which is above the voltage range of many precision ADC inputs. The solution is to split the load resistance across multiple resistors in order to limit the voltage at the ADC inputs, but still maintain the total load resistance required for HART communication.

图 4 illustrates the load resistance split across three discrete resistors: R1, R2, and R3. In this configuration, the HART signal and the loop current are both present across the total load resistance (R1 + R2 + R3). The ADS1260 only measures the voltage across R2; therefore, R2 is the only resistor that requires high precision. Because of the high input impedance presented by the internal PGA, the high and low sides of R2 can be connected to the ADS1260 through only a discrete low-pass antialiasing filter. The amplifier characteristics of the PGA impose specific voltage range limitations in order to maintain linear operation. The combination of three resistors allows the design to adapt to varying load currents and input voltage requirements.

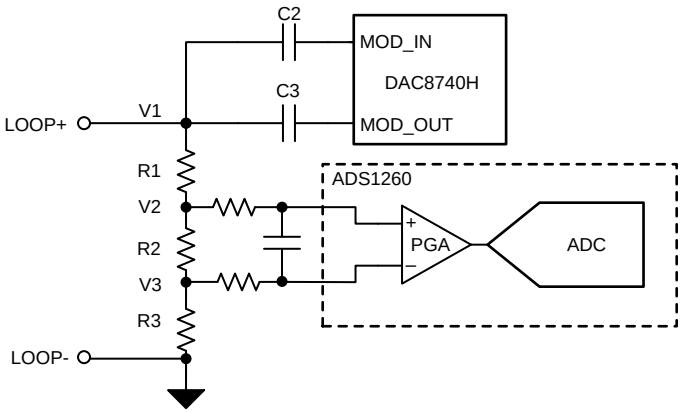


图 **4. Schematic With Split Load Resistors**

In addition to providing a high input impedance, the PGA is used to add gain to the differential input voltage before being converted by the ADC. This process ensures that the design uses most of the ADC full-scale range. Using the PGA also allows for a smaller sense resistor (R2), giving more flexibility when choosing R1 and R3 to meet the device input voltage requirements. 图 5 shows the relationship between the voltages at the positive and negative PGA inputs (V_{AINP} and V_{AINN}) and their respective outputs (V_{OUTP} and V_{OUTN}). The outputs of the PGA amplifiers are limited to 300 mV away from each supply rail, which translates to a limitation on the absolute input voltage, differential input voltage, and usable PGA gain.

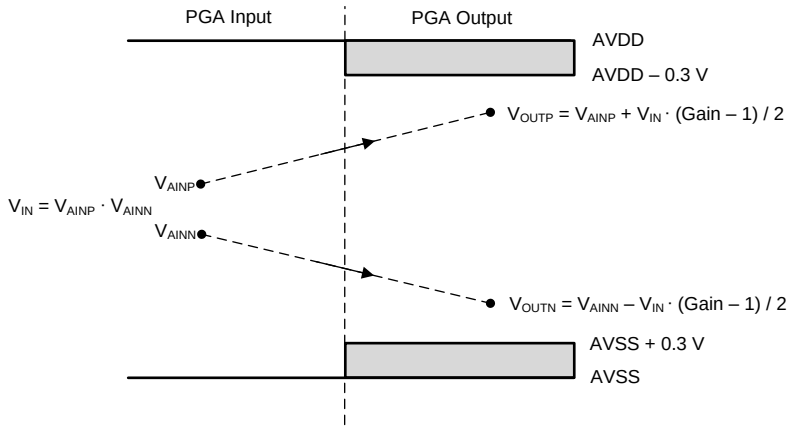


图 **5. PGA Input and Output Range**

The first step in determining R1, R2, and R3 is to determine the full-scale input range of the ADC. For most precision delta-sigma ADCs, the full-scale range depends on the reference voltage, V_{REF}. The ADS1260 can convert differential input voltages between $–V_{REF}$ and $+V_{REF}$. For devices with an internal PGA, the full-scale range must be referred to the input as $–V_{REF}$ / Gain to $+V_{REF}$ / Gain. Select the PGA gain and R2 resistance value to span most of the full-scale range over the desired input current range. Using a PGA gain greater than 1 V/V not only reduces the required sense resistor value, but also reduces the input-referred noise of the ADC. The main advantage of using the PGA gain is reducing the sense resistance required, thus reducing self-heating and drift that contributes to error. 公式 1 shows the differential input voltage to the ADC after the internal PGA as a function of loop current.

$$V_{ADC} = I_{LOOP} \times R2 \times GAIN \quad (1)$$

This design uses a mid-supply reference voltage of 2.5 V from a REF3425. In order to support the maximum expected current of 23.5 mA, R2 must be less than 2.5 V / 23.5 mA = 106.4 Ω. Increasing the PGA gain to 4 V/V decreases the minimum R2 value to 26.6 Ω, and also reduces the input-referred noise of the ADS1260. R2 is set to 24.9 Ω to allow for some headroom, resulting in a span of 348.6 mV to 2.34 V into the ADC.

When the sense resistor is chosen, R3 must be selected based on 图 5 to satisfy the PGA input requirements. 公式 2 calculates the absolute input voltage requirements for both PGA inputs (V_{AINP}, V_{AINN}). These limits are based on the analog supply rails (AVDD, AVSS), the differential input voltage (V_{IN} = Loop Current × R2), and the gain of the PGA. The voltage at the negative PGA input (V_{AINN}) is equal to R3 times the loop current. The voltage at the positive PGA input is equal to V_{AINN} + V_{IN}. 公式 3 calculates the input limits for the minimum input current of 3.5 mA and 公式 4 calculates the input limits for the maximum input current of 23.5 mA.

$$AVSS + 0.3\ V + V_{IN} \times \frac{Gain - 1}{2} < V_{AINP,}\ V_{AINN} < AVDD - 0.3\ V - V_{IN} \times \frac{Gain - 1}{2} \quad (2)$$

$$0.4307\ V < V_{AINP,}\ A_{AINN}\left(3.5\ mA\right) < 4.569\ V \quad (3)$$

$$1.178\ V < V_{AINP,}\ V_{AINN}\left(23.5\ mA\right) < 3.804\ V \quad (4)$$

R3 is selected to ensure the voltage A_{INN} is above the lower limit at the minimum loop current of 3.5 mA. 公式 5 calculates the minimum R3 value as 430.7 mV / 3.5 mA = 123 Ω. A value of 127 Ω allows for additional margin in the design. 公式 6 shows the voltage at the minimum loop current for the chosen resistance value of 127 Ω. This value satisfies the minimum PGA requirement. R1 is finally selected to ensure the sum of the resistance is greater than 230 Ω to meet the HART specification. 公式 7 shows the voltage at V2 based on R2, R3, and the maximum loop current. R1 must be at least 78 Ω to account for the remaining required load resistance in order to comply with the HART protocol, 110 Ω is therefore selected.

$$R3 \geq \frac{0.4307\ V}{3.5\ mA} \quad (5)$$

$$V3\left(3.5\ mA\right) = 3.5\ mA \times 127\ \Omega = 0.4445\ V \quad (6)$$

$$1.178\ V < V_{AINP,}\ V_{AINN}\left(23.5\ mA\right) < 3.804\ V \quad (7)$$

The PGA inputs must stay within the limits set by 公式 2 across the entire current input range. Checking the corner cases ensures that the minimum PGA input is not violated at the minimum input current and that the maximum PGA input is not violated at the maximum input current. 图 6 illustrates A_{INN}, A_{INP}, and the PGA input limitations over the input current range. 图 6 shows that the inputs are within range during all conditions.

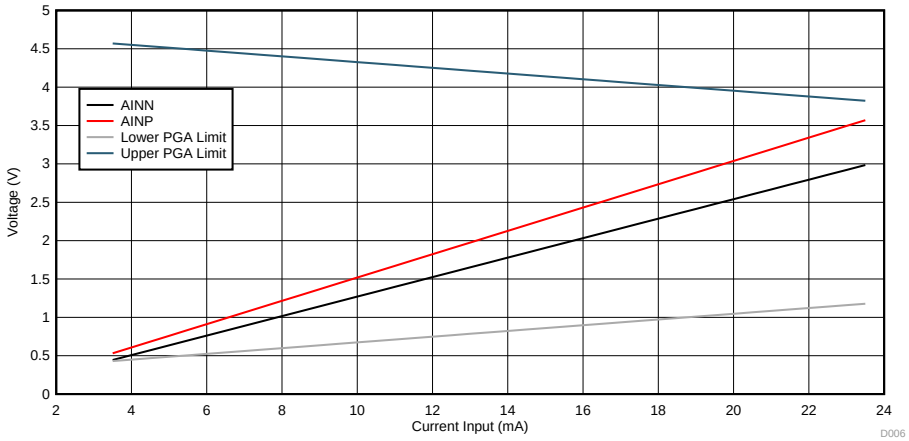


图 **6. PGA Inputs vs Loop Current**

2.2.3 ADC Input Filter and Internal Sinc Filter

The loop-current measurement encompasses two types of signal filtering: a discrete antialiasing filter and a digital decimation filter. The digital filter is responsible for low-pass filtering and decimating the samples from the delta-sigma modulator into a high-resolution result. The ADS1260 offers multiple sinc and finite impulse response (FIR) filter options with a variable frequency response based on the data rate, filter order, and clock frequency. The response of the digital filter returns to unity gain at multiples of the modulator sampling frequency, f_{MOD}.

The filter type and filter order both offer a tradeoff between conversion latency and stop-band attenuation. Lower latency allows for multiple sensors to be multiplexed into a single ADC with less delay, whereas lower stop-band attenuation reduces the level out-of-band signals that alias into the pass band, thus improving the noise performance of the system. In addition to noise, the filter in this design must reject the 1.2-kHz and 2.2-kHz FSK signals imposed onto the current loop by the field transmitter. Increasing the filter order to a second order lowers the stop-band attenuation to at least –80 dB at those frequencies and adds only one additional sample of conversion latency. Finally, the loop current is nearly a DC signal, which requires minimal signal bandwidth. This design uses an output data rate (f_{DR}) of 20 samples-per-second (SPS), yielding a –3-dB bandwidth of 6.3 Hz. 图 7 shows the frequency response of the sinc2 filter with a data rate of 20 SPS.

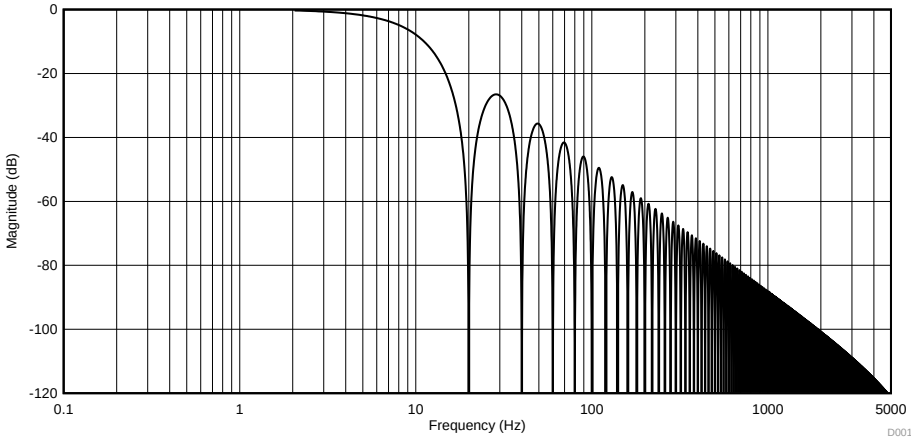


图 **7. Frequency Response of ADS1260 Sinc2 Filter at 20 SPS**

An analog antialiasing filter supplements the attenuation of the digital filter by rejecting both differential and common-mode noise. The second lobe of the sinc2 frequency response reaches approximately –36 dB and continues to roll off until f_{MOD} / 2 where the response repeats. At f_{MOD}, the digital filter response returns to unity gain, providing no attenuation. Because the stop-band rejection of the sinc2 filter is high, the discrete antialiasing filter has almost six decades in frequency before it is needed to attenuate noise around f_{MOD}. A single-pole, low-pass filter with a –3-dB cutoff frequency conservatively placed around 100 Hz yields nearly –80 dB of rejection at a modulator frequency of 921.6 kHz, which is more than sufficient in this design. Common-mode capacitors that are each ten times smaller than the differential capacitor can be added from each channel input to ground to help filter common-mode noise without affecting the system common-mode rejection. 图 8 illustrates the simulation schematic used to simulate the frequency response of the antialiasing filter at the input of the ADS1260 PGA (labeled *VIN*) and 图 9 illustrates the resulting frequency response. The analog antialias filter formed at the PGA output contributes an additional 24-dB rejection at f_{MOD}.

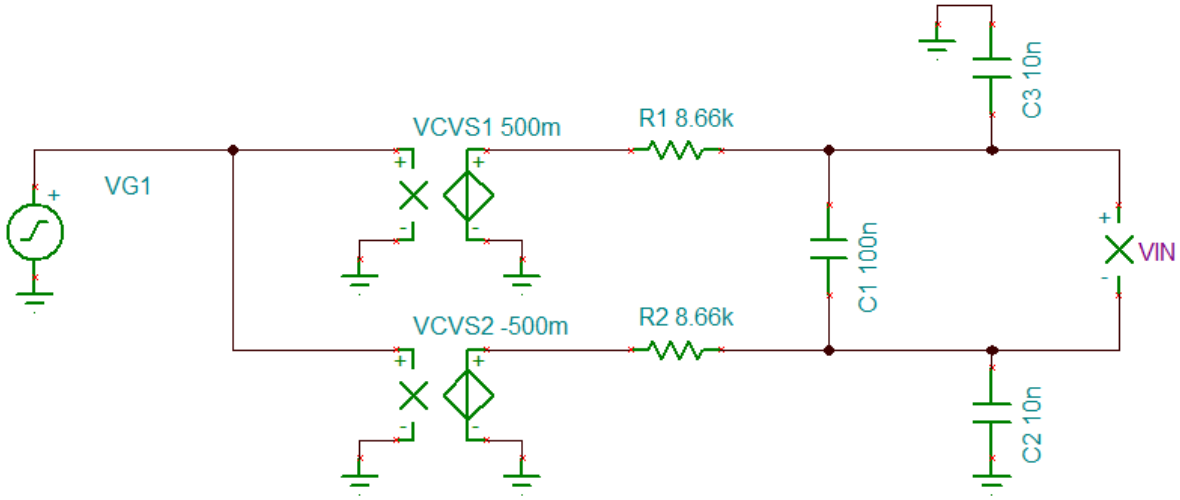


图 8. TINA-TI™ Simulation Schematic for Antialiasing Filters

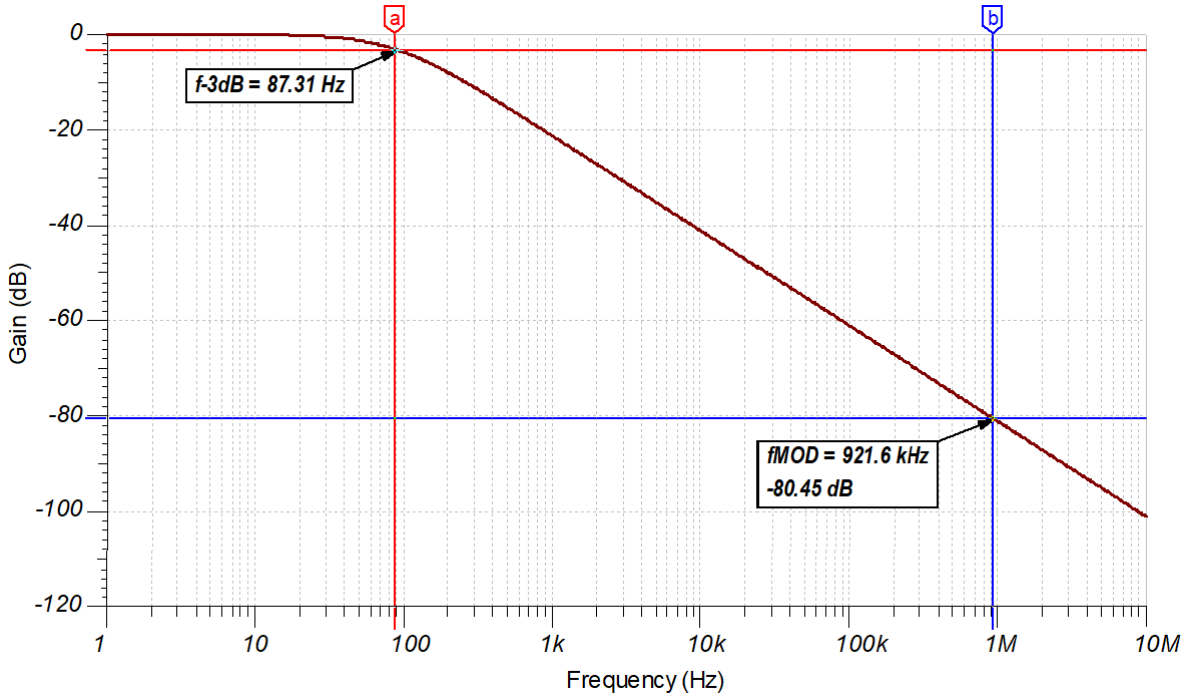


图 9. Low-Pass Antialiasing Filter Frequency Response

2.2.4 HART Considerations

The highway addressable remote transducer (HART) send and receive signals are AC-coupled directly to the load resistor. The input module receives the HART signal as a 1-mA_{PP} current waveform that is converted to voltage by the sense resistor and AC-coupled to the HART modem. Alternatively, when the input module transmits HART data a voltage signal is coupled across the sense resistor and the modulation of loop voltage is detected by the transmitter. The HART protocol is a half-duplex communication scheme and the devices have a master and slave relationship. The input module is the HART master and is responsible for requesting HART data from the current transmitter or slave device.

图 10 illustrates how the DAC8740H is connected in this input module design. MOD_OUT is coupled to the load resistor with a large capacitance value to avoid attenuating the HART signal. C1 and RL form a high-pass filter that can attenuate the HART signal if the cutoff frequency is too high. The cutoff frequency can be calculated based on the RC time constant formed by RL and C1.

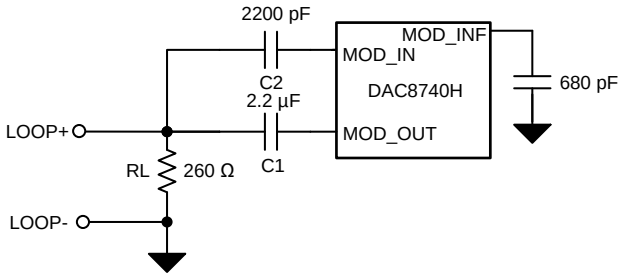


图 10. DAC8740H Input Module Coupling

The input HART signal is coupled to the DAC8740H MOD_IN pin by C2. The recommended value for C2 is 2200 pF because this capacitor affects the DAC8740H input filter response. 图 11 shows the band-pass filter (BPF) formed by the AC-coupling capacitor internal resistors and the 680 pF on the MOD_INF pin. 图 12 shows the passive filter response. This passive filter is followed by an internal second-order active high-pass filter (HPF) to meet the requirements for filtering the analog signal and high-frequency noise. The resulting filter has a 3rd-order, high-pass response below 500 Hz and a 1st-order, low-pass response above 10 kHz. The DAC8740H minimizes the external filtering components and filter design with this internal band-pass filter and ensures the HART filtering requirements are met.

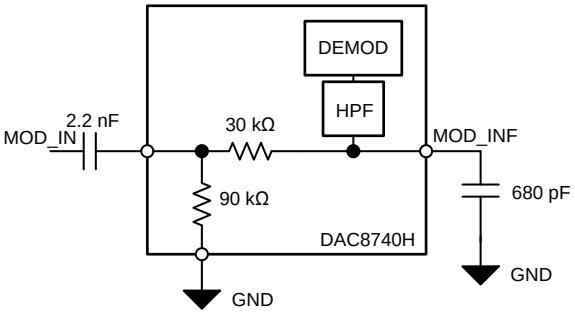


图 11. DAC8740H Internal Filter

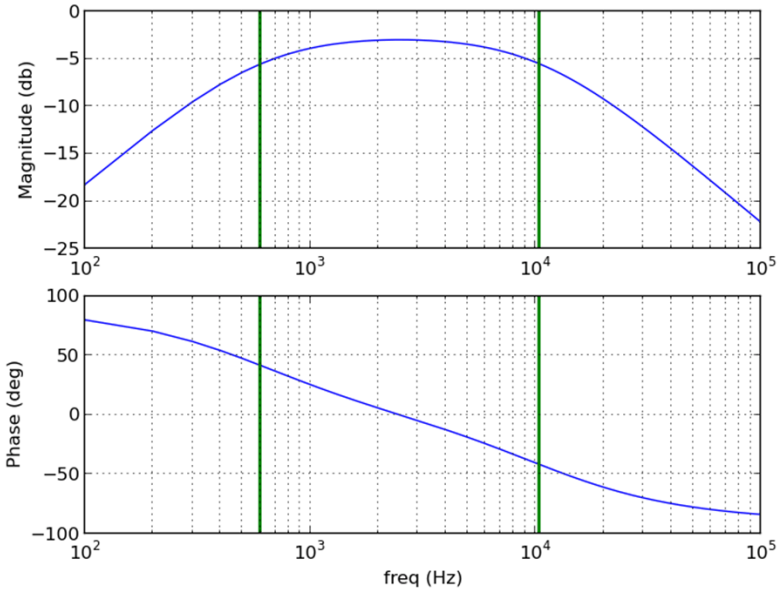


图 **12. Passive BPF Response**

The DAC8740H acts as a UART-to-HART direct feedthrough converter. The device transmits HART when the RTS ("Request-To-Send") pin is held low and interrupts the host processor with the CD pin when HART RX data are detected. In this design, an external TI MSP430FR5969 LaunchPad™ development kit is used to interface with the HART modem over the universal asynchronous receiver/transmitter (UART).

2.3 Highlighted Products

2.3.1 DAC8740H

The DAC8740H is a HART physical layer compliant modem with a UART interface. The DAC8740H integrates all required circuitry to operate as the physical layer HART modem in both slave and master configurations. The device features an internal reference, oscillator, and HART input filter requiring only a few passive components and a host processor for operation. The DAC874xH family of devices also function as FOUNDATION Fieldbus™ and Profibus PA modems.

2.3.2 ADS1260

The ADS1260 is a precision, 40-kSPS, delta-sigma, analog-to-digital converter with an integrated programmable gain amplifier (PGA) and internal fault monitors. The ADCs are comprised of an input signal multiplexer, a low-nose PGA providing a gain from 1 to 128, a 24-bit delta-sigma modulator, and a programmable digital filter. The high-impedance PGA inputs reduce measurement error caused by sensor loading. The ADS1260 supports three differential or five single-ended inputs. The ADS1260B integrates a 9-ppm/°C reference over a temperature range of 0°C to +85°C.

2.3.3 REF3425

The REF3425 device is a low temperature drift (6 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy and low operating current with power consumption less than 95 µA. This device also offers very low output noise of 3.8 μV_{PP}/V, which enables its ability to maintain high signal integrity with high-resolution data converters in noise-critical systems. With a small SOT-23 package, the REF3425 offers enhanced specifications and a pin-to-pin replacement for the MAX607x and ADR34xx devices. This reference was chosen because the REF3425 has better drift performance than the ADC internal reference. The REF3425 provides a balance between cost, accuracy, and drift.

2.3.4 TLV760

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the maximum 100-mA load across operating temperature. Standard packaging for the TLV760 is the 3-pin, SOT-23 package. The TLV760 is available in 3.3-V, 5-V, 12-V, and 15-V options. The SOT-23 packaging of the TLV760 series allows the device to be used in space-constrained applications. The TLV760 is a small size alternative to the LM78Lxx series and similar devices.

2.3.5 ISO774X

The ISO774x devices are high-performance, quad-channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV, and CQC. The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This reference design features multiple headers to externally interface the onboard DAC8740H HART modem and the ADS1260 ADC through digital isolators. The ADS1260EVM is used to interface with the ADC to test the input current measurement aspects of the design. The DAC8740H is interfaced with both the DAC8740HEVM and an MSP430FR5969 LaunchPad™ containing a HART software stack to conduct the physical layer HART testing. The additional external test equipment required includes an oscilloscope, 8.5 digit digital multimeter (DMM), precision current source, HART filter tools, and HART test modem.

3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 HART Physical Layer Test Setup

图 13 shows the test setup for most physical layer HART test cases. This test setup is used to evaluate the reference design. Any waveform measurements or scope captures are taken across the test load. The current source and DC offset are set to replicate 4-mA to 20-mA operating conditions. 节 3.2.2 specifies if another test setup is used.

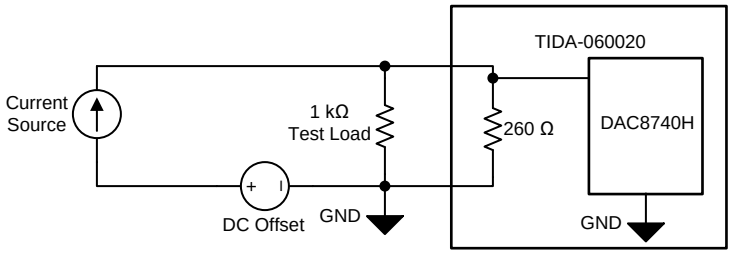


图 13. HART Current Input Device Test Setup

3.2.1.2 DC Current Test Setup (ADC)

图 14 shows how the ADC is tested. The DAC8760EVM is used as a precision DC current source to produce the loop current through the load resistors. An 8.5 digit DMM is used to measure the voltage across the current-sense resistor and calculate the loop current from the measured sense resistance. The sense resistor was measured using a 4-wire measurement for accuracy. This measured current value is compared to the value sampled by the ADC, producing a total unadjusted error (TUE) curve. Using the DAC8760EVM allows the HART signal to be coupled, thus ensuring the HART waveform does not impact the DC current measurement by the ADC.

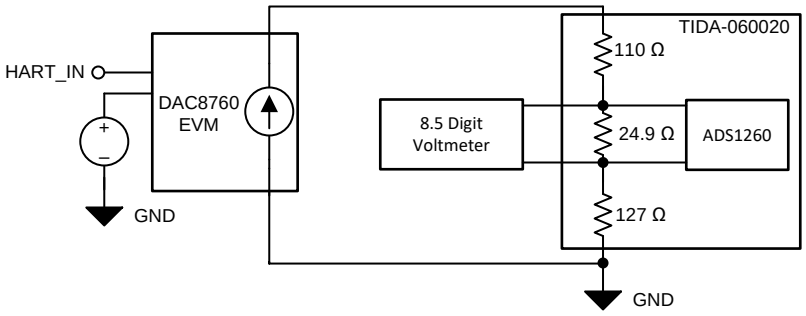


图 **14. ADC Test Setup**

3.2.2 Test Results

This section contains the test results for the HART physical layer tests and the ADC DC current measurements.

3.2.2.1 HART Waveform Test Results

图 15 and 图 16 show the measured waveforms across the test load for both the 1200-Hz and 2200-Hz HART signals, respectively. 表 2 shows the measured amplitude and frequency compared to the pass criteria for a low impedance device.

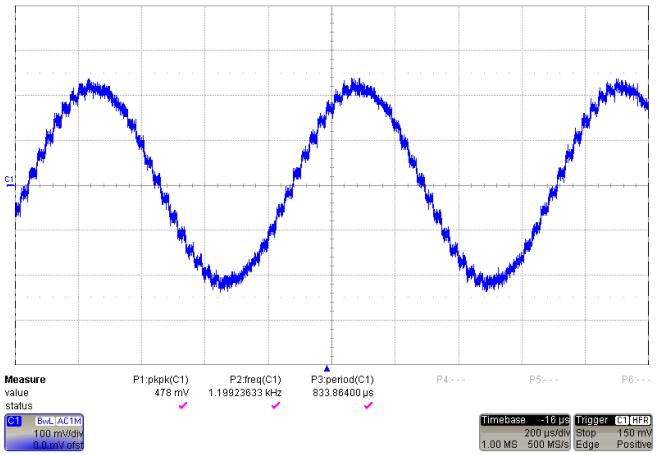


图 **15. 1200-Hz Waveform**

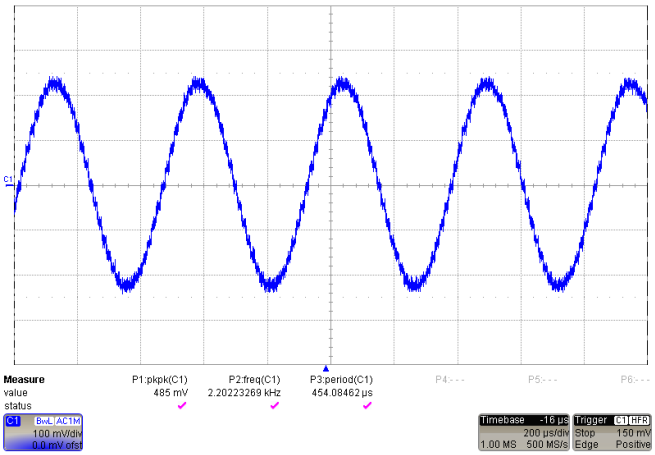


图 **16. 2200-Hz Waveform**

表 **2. HART Waveform Test Results**

TEST	MEASURED	PASS CRITERIA
1200-Hz waveform amplitude	478 mV	400 mV - 800 mV; low Z
2200-Hz waveform amplitude	485 mV	400 mV - 800 mV; low Z
1200-Hz waveform frequency	1199.2 Hz	1188 Hz - 1212 Hz
2200-Hz waveform frequency	2202.2 Hz	2179 Hz - 2222 Hz

3.2.2.2 HART Carrier Start, Stop, Decay Test Results

The carrier must start within 5 bit times (1 bit time = 1 period at 1200 Hz), stop within 3 bit times, and decay within 6 bit times. The carrier is tested at both 1200 Hz and 2200 Hz. 图 17 and 图 18 show an example of the start and stop results with a 1200-Hz carrier waveform. Channel 1 is measured at the test load and channel 2 is the RTS signal. For both carrier frequencies, the stop, start, and decay tests were less than 1 bit time, satisfying the requirement.

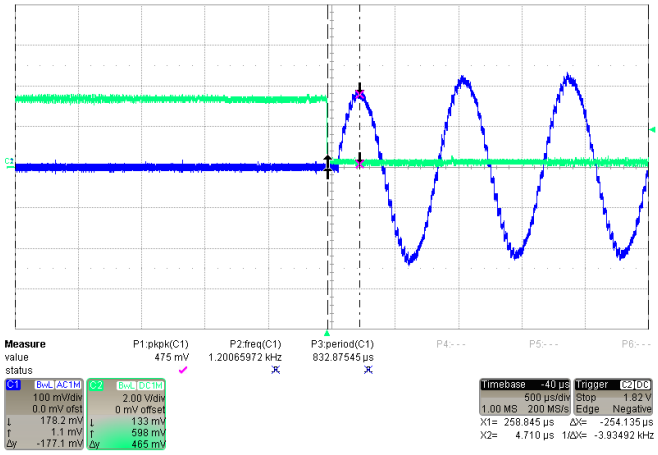


图 17. 1200-Hz Start Test

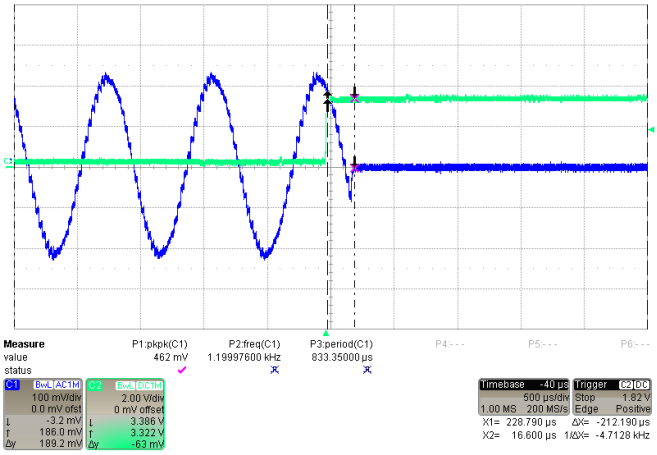


图 18. 1200-Hz Stop and Decay Test

3.2.2.3 Carrier Start and Stop Transient Test Results

The carrier start and stop transient test ensures that a large spike does not occur in the analog signal domain when the HART communication begins and ends. 图 19 shows the test setup. The analog test filter is connected to the reference design and the output is displayed on the oscilloscope. The output through the filter must not create a spike greater than 100 mV. 图 20 and 图 21 illustrate the start and stop transients. There is no noticeable transient at the output of the analog test filter. Channel 1 is measured across the test load, channel 2 is the RTS pin, and channel 3 is the voltage after the analog filter.

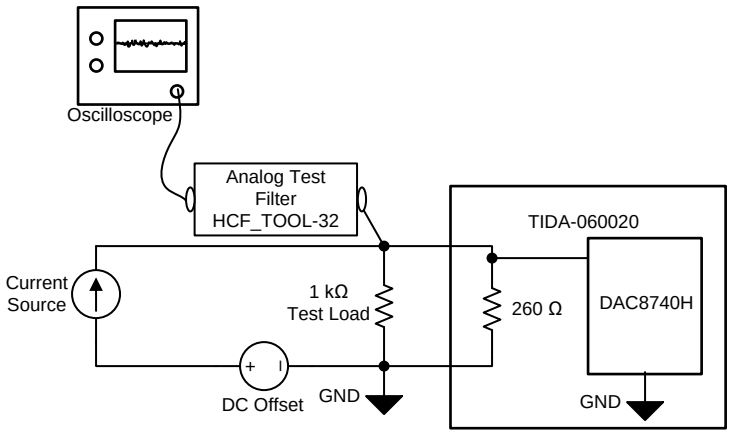


图 19. Carrier Start and Stop Transient Test Setup

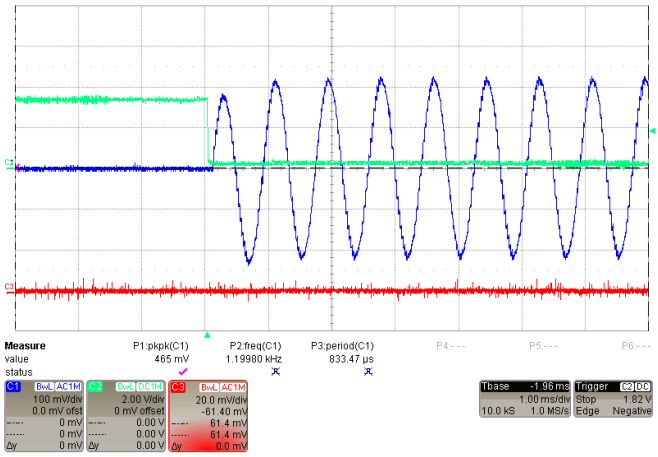


图 20. Carrier Start Transient

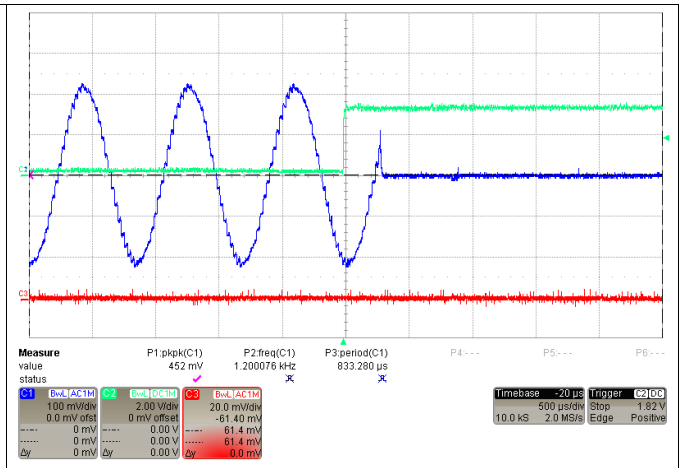


图 21. Carrier Stop Transient

3.2.2.4 HART Output Noise During Silence Test Results

The output noise during silence test ensures that the input module does not contribute unacceptable noise levels to the loop when HART is not being transmitted. 图 22 shows the test setup. The TIDA-060020 is configured in an inactive state. No loop current is flowing to ensure the measured noise is the only contribution from the TIDA-060020 circuitry. First, the oscilloscope is connected to the reference design directly to measure broadband noise levels. Then the oscilloscope is connected through a digital test filter to measure in-band noise levels. 图 23 illustrates the scope capture of the noise. Channel 1 shows the broadband noise without the digital test filter and channel 2 shows the in-band noise with the digital test filter. If the measured broadband noise without the filter is less than 2.2mV$_{RMS}$, then measuring the in-band noise through the digital test filter is not required. 表 3 illustrates the measured noise results compared to the pass criteria.

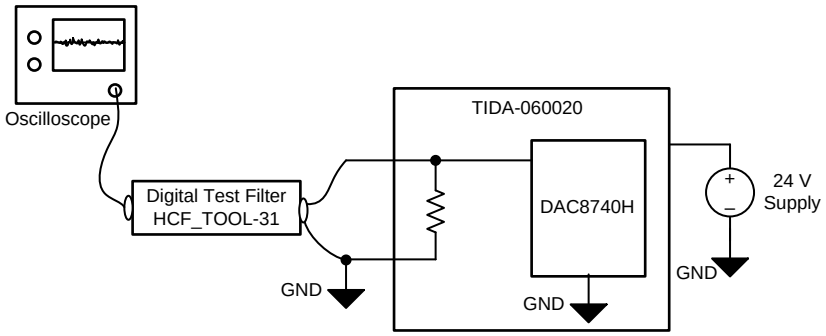


图 22. Output Noise During Silence Test Setup

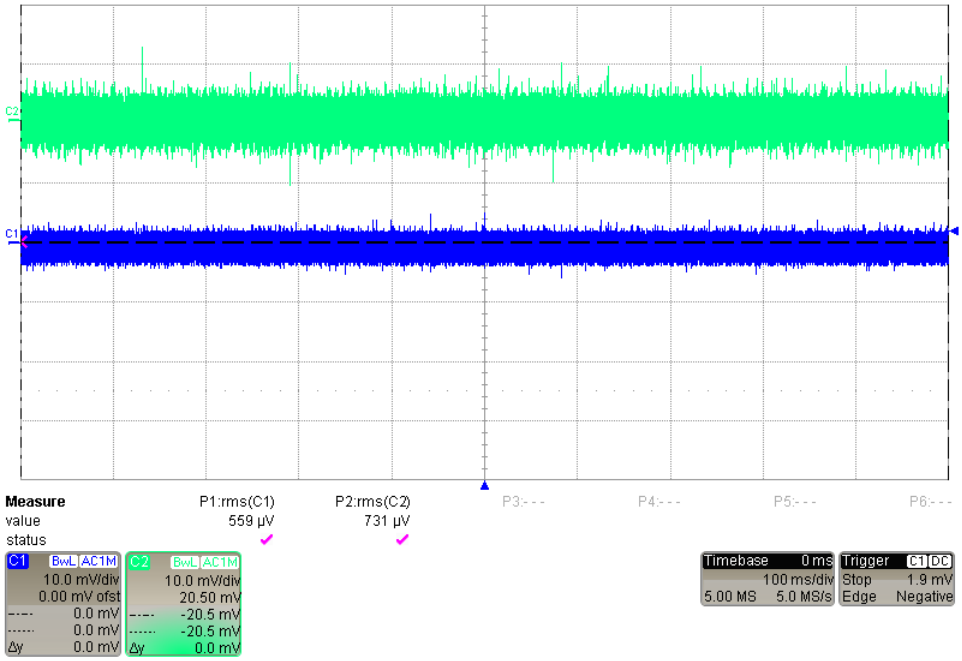


图 **23. Output Noise During Silence Scope Capture**

表 **3. Output Noise During Silence Test Results**

TEST	MEASURED	PASS CRITERIA
Broadband noise (no filter)	559 μV_{RMS}	138 mV_{RMS} max
In-band noise (500 Hz to 10 kHz) digital test filter (10x gain)	731 μV_{RMS}	22 mV_{RMS} max

3.2.2.5 HART Receive Impedance Test Results

The receive impedance is the input impedance of the tested device. The impedance affects the HART signal integrity and can reduce the distance over which HART can be used. 图 24 shows the test setup for receive impedance. A sinusoidal AC source generates a voltage and the amplitude is measured twice: first across a 250-Ωtest load (Va) and again across the input of the TIDA-060020 (Vb). The impedance is calculated by Z = (250 Ω / Va) × Vb. 表 4 lists the measured values of Va, Vb, and the calculation of Z at the required frequencies. 图 25 illustrates a plot of the receive impedance. A parallel combination of R = 261 Ω and C = 13 nF approximates the receive impedance of TIDA-060020.

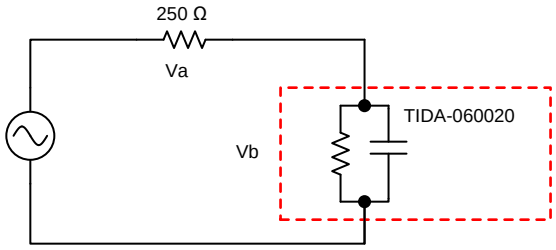


图 **24. Receive Impedance Test Setup**

表 **4. Receive Impedance Measurements**

FREQUENCY (Hz)	Va (V RMS)	Vb (V RMS)	Z (Ω)
500	0.3529	0.3710	261.0
950	0.3534	0.3704	260.2
1.6k	0.3542	0.3695	259.0
2.5k	0.3550	0.3686	257.8
5k	0.3567	0.3671	255.5
10k	0.3600	0.3560	251.7
20k	0.3704	0.3594	240.9
50k	0.4217	0.3318	195.4

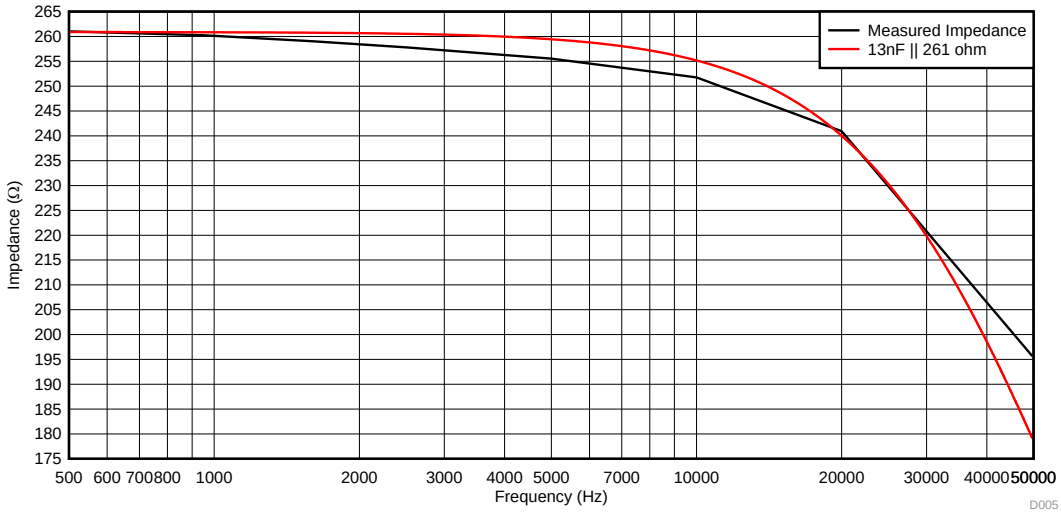


图 **25. Receive Impedance vs Frequency**

The receive impedance must be between 230 Ω and 600 Ω between 950 Hz and 2500 Hz. The receive impedance over the extended frequency band of 500 Hz to 10 kHz must have a difference between the maximum and minimum value difference less than 6 dB (factor of 2). The receive impedance of the TIDA-060020 decreases by 9.3 Ω over the extended frequency band.

3.2.2.6 Send Impedance Test Results

图 26 shows the send impedance test setup. The output of the TIDA-060020 is connected to an external test load resistor and the 1200-Hz and 2200-Hz waveforms are produced by the DAC8740H. The test is repeated for two load resistance values. V1 is the voltage measured across a 10-kΩ test load and V2 is the voltage measured across a 1-kΩ test load. 公式 8 calculates the send impedance as the change in voltage across the test load (ΔV) divided by the change in current (ΔI). 表 5 shows the results for the 1200-Hz and 2200-Hz tests. The send impedance is required to be less than 80 percent of the receive impedance.

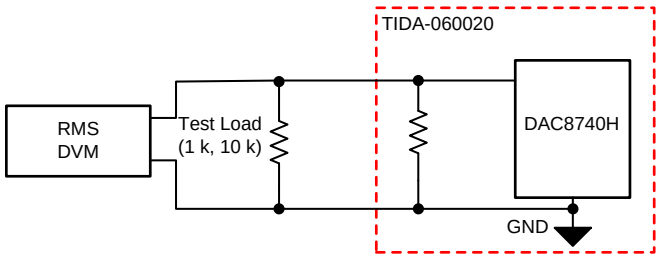


图 **26. Send Impedance Test Setup**

$$Z_{OUT} = \frac{\Delta V}{\Delta I} = \frac{V1 - V2}{\left(\frac{V2}{1k\Omega}\right) - \left(\frac{V1}{10\,k\Omega}\right)} \quad (8)$$

表 **5. Send Impedance Measurements**

TEST	RMS VOLTAGE (V_{RMS})	FREQUENCY (Hz)	Z_{OUT} (Ω)
10 kΩ, 1200 Hz (V1)	0.1573	1200	32.5
10 kΩ, 2200 Hz (V1)	0.1624		
1 kΩ, 1200 Hz (V2)	0.1528	2200	18.9
1 kΩ, 2200 Hz (V2)	0.1597		

3.2.2.7 Noise Sensitivity Test Results

图 27 shows the noise sensitivity test setup. This test is designed to ensure HART communication can still occur with noise added to the loop. Noise of different frequencies is injected by a signal generator and adjusted so the specified amplitude is detected across the load resistor of the TIDA-060020. A HART test modem is then used with a waveform amplitude of 175 mV_{PP} to generate 100 consecutive response request exchanges with the noise on the loop. No bit errors occurred in this testing of the TIDA-060020. 表 6 lists the noise sensitivity levels. In the case of the 29-Hz and 63-Hz frequency levels, the amplitude is restricted to 0.9 V so as not to exceed the minimum HART-enabled operating current of 3 mA. 图 28 illustrates an example of setting the sinusoidal noise level across the load resistor before generating the response and request sequence.

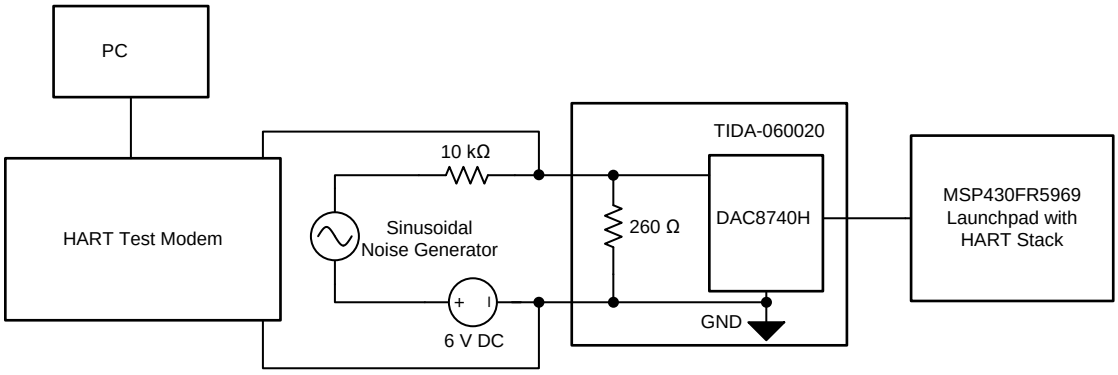


图 **27. Noise Sensitivity Test Setup**

表 **6. Noise Sensitivity Levels**

AMPLITUDE	FREQUENCY
55 mV_{PP}	1.7 kHz
220 mV_{PP}	250 Hz
880 mV_{PP}	125 Hz
3.52 V_{PP} (limited to 0.9 V_{PP})	63 Hz
16 V_{PP} (limited to 0.9 V_{PP})	29 Hz

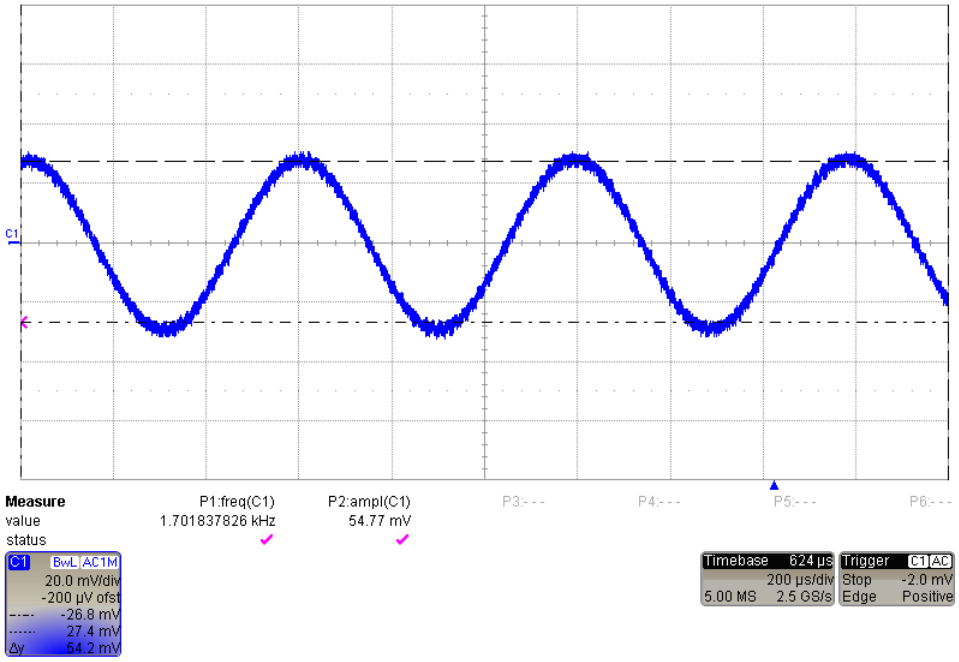


图 **28. Example of Setting the Noise Level Across R_{LOAD}**

3.2.2.8 Carrier Detect Tests

The carrier detect tests ensure that the modem does not attempt to demodulate a HART signal below 80 mV_{PP} and always demodulates HART signals above 120 mV_{PP}. To perform this test, the setup from the noise sensitivity test setup is used and the test modem is set to an amplitude of 80 mV_{PP} and 120 mV_{PP}. The carrier detect pin is monitored and is not asserted in the 80-mV_{PP} case but is asserted in the 120-mV_{PP} case. The time from the carrier on to the carrier detect assertion and the time from the carrier off to the carrier detect deassertion must be no more than 6 bit times.

图 29 shows that the carrier detect is not asserted when the test is run with a HART signal amplitude of 80 mV_{PP}. 图 31 shows that the carrier detect is asserted after applying a HART signal amplitude of 120 mV_{PP}. 图 30 shows that the carrier detect is deasserted after same 120 mV_{PP}carrier is turned off. Both 图 31 and 图 30demonstrate approximately a 1 bit time delay.

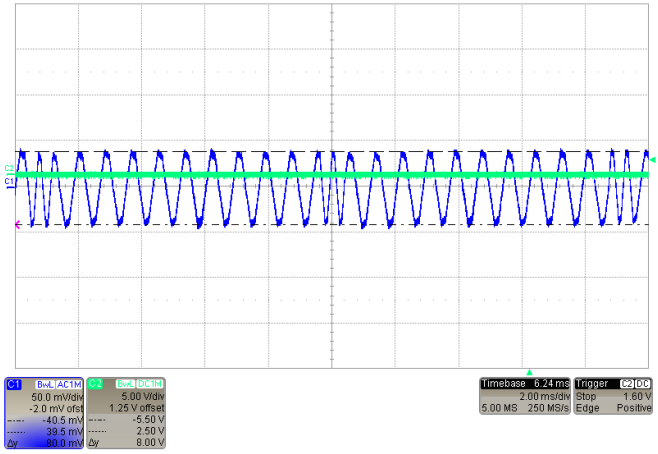


图 29. Carrier Detect With 80-mV_{PP} HART Signal, Carrier Not Asserted

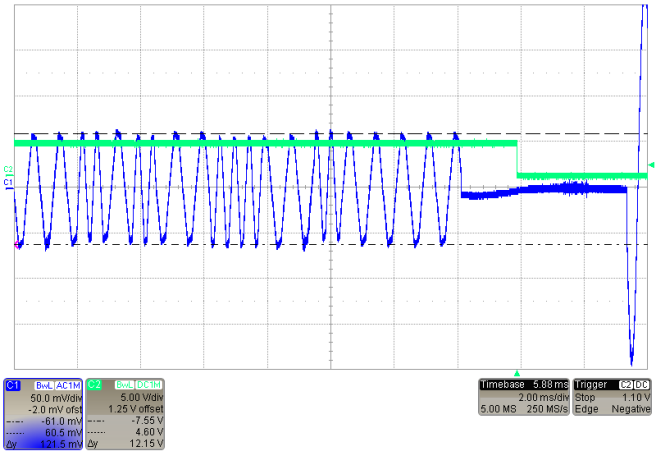


图 30. Carrier Detect With 120-mV_{PP} HART Signal, Carrier Deasserted

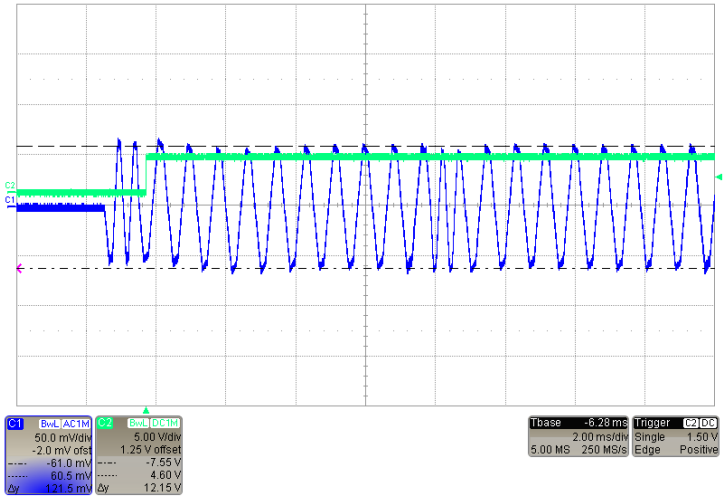


图 31. Carrier Detect With 120-mV_{PP} HART Signal, Carrier Asserted

3.2.2.9 DC Current Measurement Test Setup (ADC)

To measure the accuracy of the ADC DC loop current measurement, the test setup shown in 节 3.2.1.2 is used. The DAC8760 sets the DC loop current in steps of 500 µA. The voltage across the sense resistor is measured by both the 8.5 digit DMM and the ADC. The TUE is calculated based on 公式 9, where $I_{LOOP,ADC}$ is the current calculated from the ADC voltage reading and $I_{LOOP,DMM}$ is the current calculated from the voltage measured by the 8.5 digit DMM. 图 32 plots the TUE over the input current range of the design. The maximum error is 0.007% of the full-scale range (FSR) at room temperature.

$$\text{TUE}(\%\text{FSR}) = \frac{I_{LOOP,\,ADC} - I_{LOOP,\,DMM}}{23.5\ \text{mA} - 3.5\ \text{mA}} \times 100 \tag{9}$$

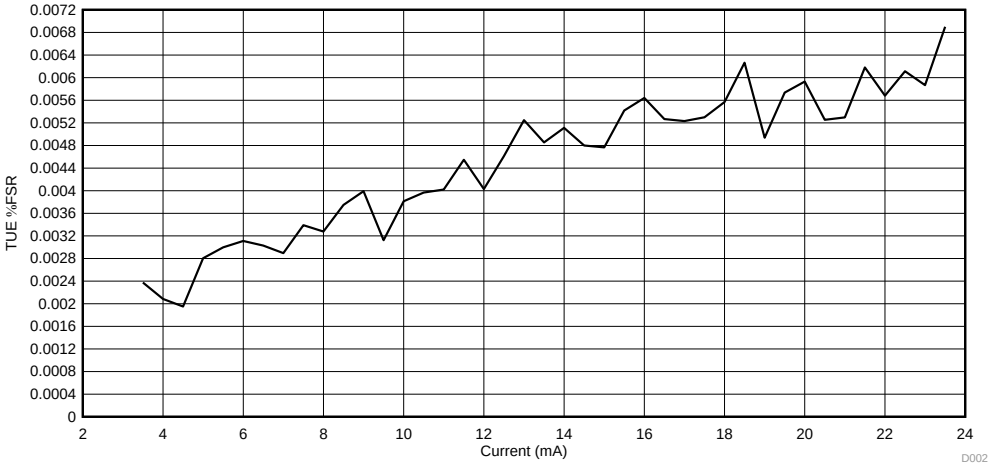


图 **32. Current TUE vs Loop Current**

The ADC performance was evaluated by taking 1024 samples of the voltage across the sense resistor with the loop current set to mid-scale (i.e. 12 mA). This evaluation is first done with HART disabled and then repeated with the HART enabled.. This process ensures that the HART signal which is superimposed on the loop current is being filtered out effectively and is not affecting the DC current measurement. 图 33 and 图 34 plot a histogram of the DC measurements taken with HART disabled and with HART enabled, respectively. No significant difference is observed when the HART is enabled, confirming that the combination of analog and digital filtering sufficiently attenuates the HART signal from the loop current.

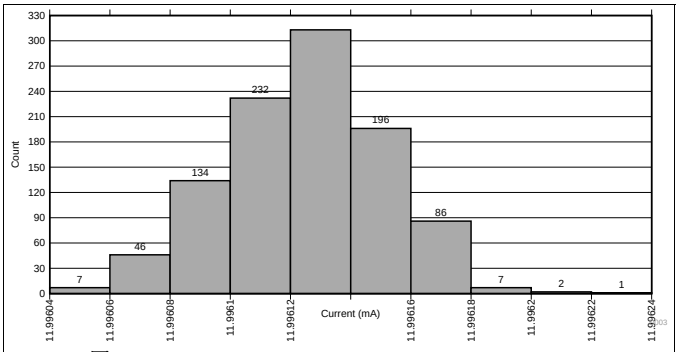


图 **33. Histogram of ADC Samples With HART Disabled (ENOB = 20.847 Bits, NFB = 18.022 Bits, Peak-to-Peak Codes = 63 LSB)**

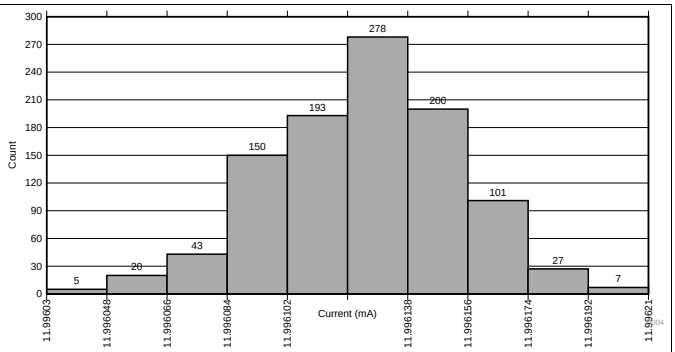


图 **34. Histogram of ADC Samples With HART Enabled (ENOB = 20.789 Bits, NFB = 18.167 Bits, Peak-to-Peak Codes = 57 LSB)**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060020

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060020.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060020.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060020.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060020.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060020.

5 Software Files

To download the software files, see the design files at TIDA-060020.

6 Related Documentation

1. TI Designs: TIDA-01504*Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter with HART Modem Reference Design*

6.1 商标

7 About the Author

GARRETT SATTERFIELD is an applications engineer in the Precision Digital-to-Analog Converters product line at Texas Instruments, where he supports industrial products and applications. Garrett received his BS in Electrical Engineering from the Georgia Institute of Technology.

RYAN ANDREWS is an applications engineer with the Precision ADC product line at Texas Instruments, where he supports industrial and medical products and applications. Ryan received his BS in Biomedical Engineering and his BA in Spanish from the University of Rhode Island.

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