设计指南：TIDA-070005
3V 至 7V 输入电压、24A 输出电流、0.95V 输出电压、航空级电流共享负载点 (POL) 参考设计

说明

部分新型航空级 FPGA 和 ASIC 需要低电压和高电流来满足其核心功耗要求，因此促生了对航空级直流/直流电源转换负载点 POL 电源的需求，该电源可提供低电压输出和高电流以满足其核心功耗要求。此参考设计提供了使用四 (4) 个正交 TPS50601A-SP 直流/直流转换器以生成 24A 电源的 POL 硬件示例，另外，此参考设计指南还提供了有关如何正确配置和评估参考设计硬件并对其进行计时的详细信息，参考设计硬件包含一块母板和四个子板。

资源

TIDA-070005	设计文件夹
TPS50601A-SP	产品文件夹
INA901-SP	产品文件夹
TPS7A4501-SP	产品文件夹
SE555-SP	产品文件夹
SN54HC74-SP	产品文件夹
SN54HC04-SP	产品文件夹
SN74AHC1G04	产品文件夹

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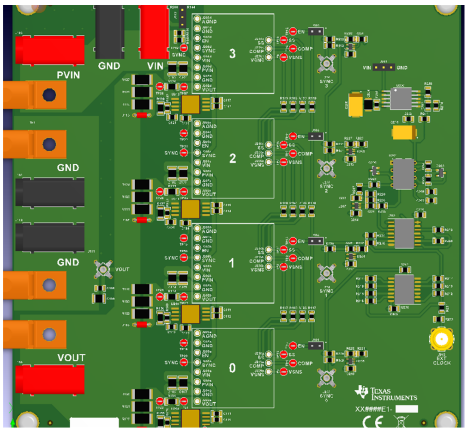
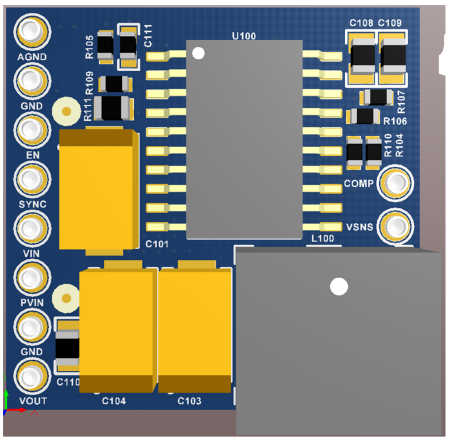
特性

- 独立航空级时钟生成功能
- 内置电流检测监控功能
- 可通过多种配置来评估 2 个、3 个或 4 个 TPS50601A-SP POL 的电流共享
- 适用于控制逻辑和时钟的内置航空级稳压电源
- 对母板和子板提供硬件支持
- 外部时钟生成和使用功能
- 易于进行设计互换的双板解决方案
- 提供设计细节指导，支持构建满足系统需求的个性化解决方案

应用

- 命令和数据处理
- 卫星电力系统 (EPS)
- 光学成像有效载荷
- 雷达成像有效载荷
- 通信有效载荷





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1 System Description

The TIDA-070005 is a reference hardware example of a 24-A DC/DC power solution for space grade applications. The newest space grade FPGAs and ASICs require high currents for their core power consumption. These high current requirements drive a need for space grade DC/DC power conversion circuitry. The TIDA-070005 design showcases the use of four TPS50601A-SP DC/DC converters in quadrature to generate a 24-A supply. This design guide provides details on how to properly configure, clock, and evaluate the TIDA-070005 which includes one mother board and four daughter boards.

The TPS50601A-SP DC/DC radiation hardened buck regulator is a 7-V, 6-A synchronous converter that can be configured in master-slave mode to provide up to 12 A of output current using the sync pin while sharing SS (soft-start), COMP (compensation), and EN (enable) pins.

The TIDA-070005 is a hardware reference design for the TPS50601A-SP. The design is intended to be used as an example of how build and operate a solution with four TPS50601A-SP converters working in quadrature to achieve a 24-A power solution while sharing the SS, COMP, and EN pins as described in the TPS50601A-SP datasheet similar to parallel operation.

The TIDA-070005 hardware consists of two separate printed-circuit boards (PCBs). The first board is referred to as the Mother Board and the second board is referred to as the daughter board. The Mother board consists of the power management, clocking, and current sense capabilities on the design. The daughter board consists of the TPS50601A-SP POL (point of load) buck converter, Vout settings, and compensation networks for the design. In application four daughter boards connect to one mother board via a set of individual headers for each board.

The design allows for a user to select between six different configurations to showcase the versatility of combining the TPS50601A-SP in parallel and quadrature to generate a number of high current rails. The TPS7A4501-SP LDO regulator provides the control circuitry power to the POL as well as the clocking Integrated Circuits (IC) on the motherboard. The SE555-SP and 2 SN54HC74-SP work together to generate a digital phase splitter, the digital phase splitter generates four clock signals all 90 degrees out of phase to minimize noise in the system as well as maximize stability of the output current.

Current TI space rated solution only provide up to 6 A of output current. Large currents are needed to drive future space grade FPGAs. This design provides a complete solution for providing up to 24 A of current for the next gen FPGAs

1.1 Key System Specifications

表 **1. Mother Board Key System Specifications**

PARAMETER	DESCRIPTION	SPECIFICATION
PVin	Input power for the output stage of the switching regulators	3 to 7 V
Vin	Input power for the control circuitry of the switching regulators	3 to 7 V
Vin_LDO_6V	TPS7A4501-SP input power	2.5 to 20 V
Iout	Load current	6 A/device - 24-A total

表 **2. Daughter Board Key System Specifications**

PARAMETER	DESCRIPTION	SPECIFICATION
PVin	Input power for the output stage of the switching regulators	3 to 7 V
Vin	Input power for the control circuitry of the switching regulators	3 to 7 V
Iout	Load current	6 A

1.2 Design Benefits

- Scalability
  - Hardware can be used for evaluation of 1, 2, 3 or 4 buck regulators working together or separately in multiple configurations.
  - Hardware example can be scaled to greater current configurations with proper design and testing
- High Level of Integration
  - All evaluation can be done with TIDA-070005 hardware, and external power supply/load
  - Integrated current sense monitoring
  - Integrated clocking and power management solution
- Multiple Clocking Options
  - System design allows for externally generated clocking solutions
  - System design allows for internally generated clocking solutions

2 System Overview

2.1 Block Diagram

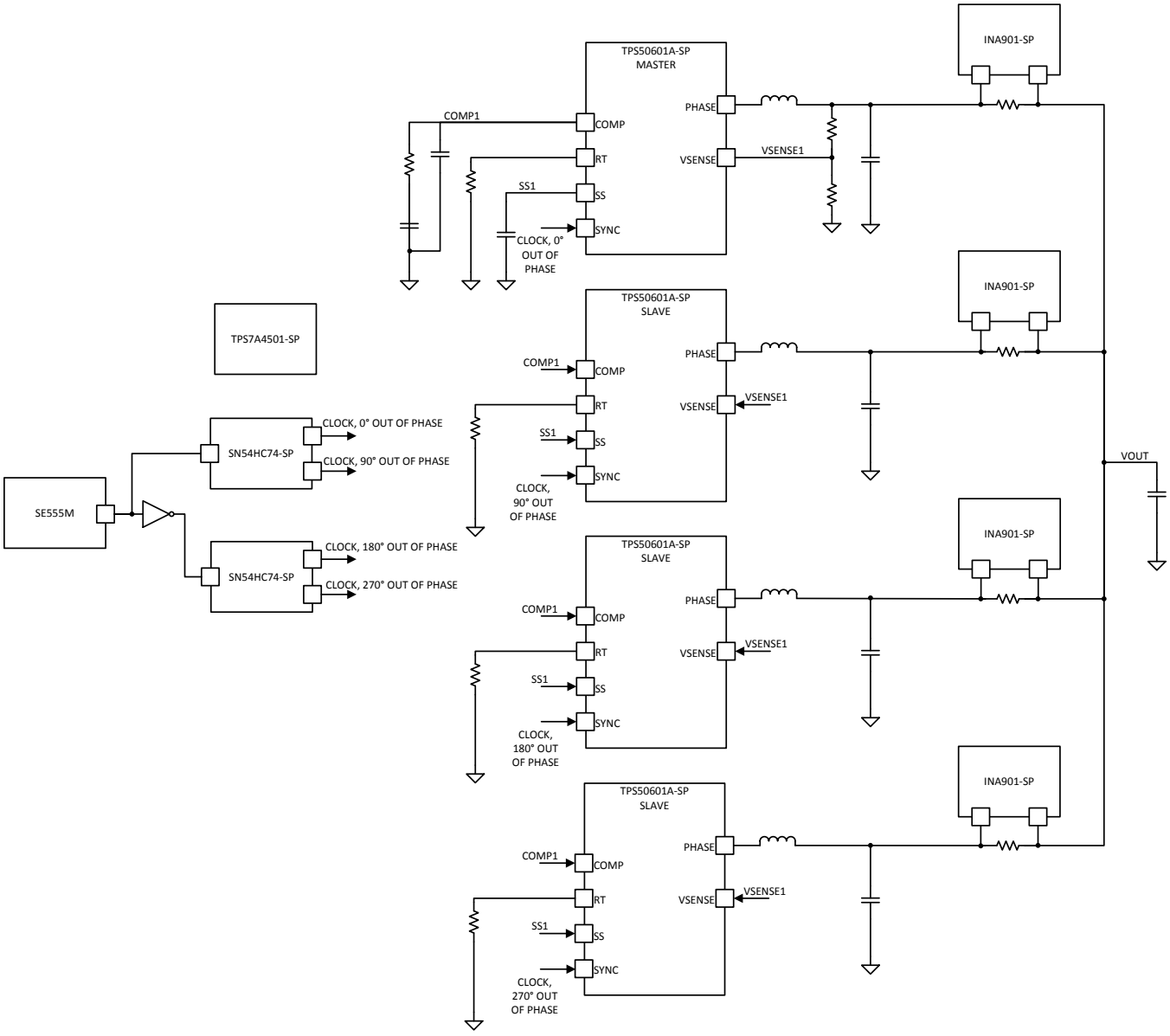

图 **1. TIDA-070005 Block Diagram**

2.2 Design Considerations

When using the TPS50601A-SP in master-slave mode (with either 1, 2 or 3 slaves), particular attention must be paid to the passive component values calculation for the EN, SS and COMP pins. This is because there is only set of passives (placed closely to the master) but they are connected to the respective pins of all slave devices. Therefore, this factor (2, 3 or 4) must be taken into account depending on the number of devices used in the configuration.

2.3 Highlighted Products

The following section describes the important ICs that make up the TIDA-070005 24-A solution.

2.3.1 TPS50601A-SP

The TPS50601A-SP is a radiation hardened, 7-V, 6-A synchronous step-down converter, which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. The device is offered in an ultra small, thermally enhanced 20-pin ceramic flatpack package.

The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins. In addition, the TPS50601A-SP can be configured in master-slave mode to provide up to 12 A of output current.

Cycle-by-cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

2.3.2 TPS7A4501-SP

The TPS7A4501-SP is a low-dropout (LDO) regulator optimized for fast-transient response. The 5962-1222402VHA can supply 750 mA of output current with a dropout voltage of 300 mV. The 5962R1222403VXC can supply 1.5 A of output current with a dropout voltage of 320 mV. Quiescent current is well controlled; it does not rise in dropout, as with many other regulators. In addition to fast transient response, the TPS7A4501-SP regulator has very-low output noise, which makes it ideal for sensitive RF supply applications.

Output voltage range is from 1.21 to 20 V. The TPS7A4501-SP is stable with output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection. The device is available as an adjustable device with a 1.21-V reference voltage. The 5962-1222402VHA is available in 10-pin CFP (U) package and 5962R1222403VXC is available in thermally-enhanced 10-pin CFP (HKU) package. Known good die (KGD) option is available for both 5962-1222402V9A for non-RHA version and 5962R1222403V9A for RHA

2.3.3 INA901-SP

The INA901-SP is a voltage-output, current-sense amplifier that can sense drops across shunt resistors at common-mode voltages from –16 V to +80 V, independent of the supply voltage. The INA901-SP operates from a single 2.7-V to 18-V supply, drawing 700 µA (typical) of supply current.

The gain of the INA901-SP is 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops. The pinouts readily enable filtering.

The device is specified over the extended operating temperature range of –55°C to 125°C and is offered in an 8-pin CFP package.

2.3.4 SE555-SP

The SE555-SP is a precision timing circuit capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of VCC. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 100 mA. Operation is specified for supplies of 4.5 to 16.5 V. With a 5-V supply, output levels are compatible with TTL inputs.

2.3.5 SN54HC74-SP

The SNx4HC74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs

2.3.6 SN54HC04-SP

The SNx4HC04 devices contain six independent inverters. They perform the Boolean function Y = A in positive logic

2.3.7 SN74AHC1G04DCKR

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function Y = A.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

The TIDA-070005 consists of two boards, a mother board and 4 daughter boards. To get started with using the hardware, see 3.2 节.

3.1.1 Hardware

3.1.1.1 Mother Board

The mother board consists of the system power, clocking circuitry, and current sense monitoring. The mother board has four sockets in which four independent daughter boards can plug into via headers on the board to be configured as desired by the user. The below sections detail the different subsystems within the mother board.

3.1.1.1.1 System Power

The power stage of the mother board provides three different settings, each is described in the below sections. The power stage is responsible for distributing three separate power rails. The first power rail is PVin which is the input power rail to the output stage of the TPS50601A-SP DC/DC buck reg. The second power rail is Vin which is the input power to the control logic for the TPS50601A-SP. The third power stage is the input power rail to the output power stage of the TPS7A4501-SP LDO; the LDO's output powers the ICs that make up the clocking stage of the mother board as well as the INA901-SP current sense monitor.

表 **3. Mother Board Power Settings**

Jumper	Power Option 1	Power Option 1	Power Option 1
R143	Y	Y	DNP
R116	Y	Y	DNP
R144	Y	DNP	DNP
R200	Y	DNP	DNP

3.1.1.1.1.1 Pvin == Vin == Vin_LDO_6V = 6 V

In the simplest configuration R143, R116, R144, and R200 are all populated and a 6-V supply and its respective ground is connected to the board via J100 and J103. The 6-V supply then powers the PVIn and Vin of all TPS50601A-SP POLs on each daughter board plugged into the mother board. The 6-V rail also supplies power to the TPS7A4501-SP and the downstream clocking ICs on the mother board

3.1.1.1.1.2 PVin == Vin = Desired Input Voltage to POL; Vin_LDO_6V = 6 V

In the second configuration R143 and R116 are populated and R144 and R200 are DNP (Do Not Populate). This configuration allows for more flexibility as the input voltage to the POLs in the system can now be altered to specific design specifications for evaluation. The range for PVin and Vin is 3- to 7-V DC. A power supply and its respective ground is connected to the board by J100 and J10 to provide the power to PVin and Vin via banana cables. A 6-V power supply is then connected to J113 for power to the TPS7A4501-SP with the positive and negative terminals connected to pin 1 and pin 2, respectively.

3.1.1.1.3 All Rails Independently Powered

In the third configuration each of the three power rails are independently supplied their respected power and R143, R116, R144, and R200 are all DNP. In this configuration banana cables are connected to J100 and J103 for the PVin power of the converters. Pins 4 and 3 are Vin and GND for the POL converters respectively and should be connected to a power supply. Pins 1 and 2 are Vin_LDO_6V and GND respectively for the inputs to the TPS7A4501-SP and will also need their own power supply.

图 2 shows the configuration of the TPS7A4501-SP in the system.

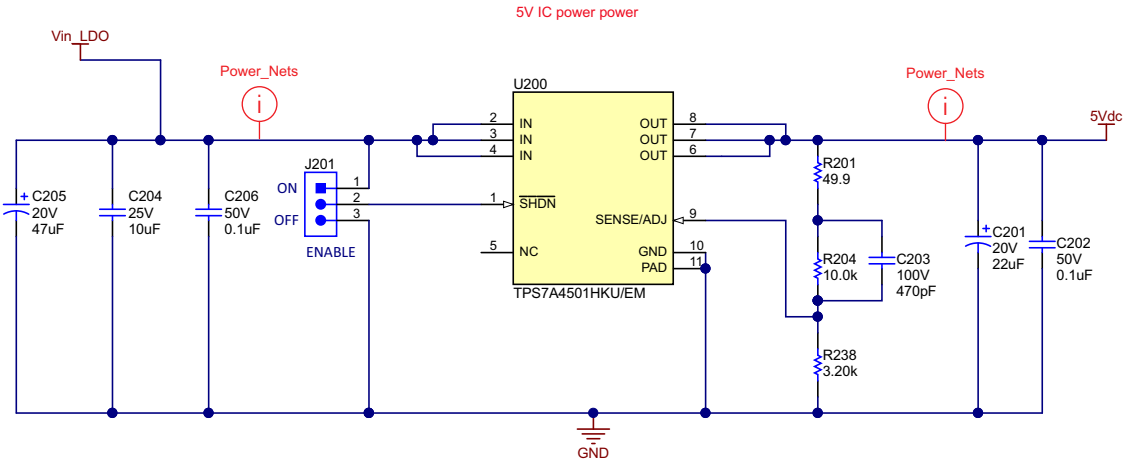

图 2. TPS7A4501-SP Design Schematic

The TPS7A4501-SP has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors, R1 and R2, as shown in the device datasheet. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. Calculate the output voltage using Equation 2 of the datasheet shown below.

The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.

3.1.1.1.2 System Clocking

There are three clocking configurations available in the TIDA-070005 discussed as follows.

3.1.1.1.2.1 Quadrature Clocking

This configuration implements a digital phase splitter to generate the quadrature clock. A 555 timer must be set to output at 2×f the desired end switching frequency of the POL. With the output connected to the gate terminal of an N type FET, we can capture two square wave clock signals operating at 2×f and 180° out of phase with one another. These signals are called 555_clock_2fa and 555_clock2fb as shown in 图 3. Both of these signals are fed to two separate D flip flops. Note that the D flip flops only latch on the rising edge of the clock. The clock 2×f frequency that is 180° out of phase with another generates two individual rising clock signals to the two respective D flip flops 90° shifted with respect to the desired frequency of the POLs which is 1/2 the 2×f frequency being fed to the flip flops. Capturing the Q and Qnot output of each of the D flip flops will then result in 4 outputs 90° out of phase with one another and operating at the desired switching frequency of the POLs as shown in 2.2 节.

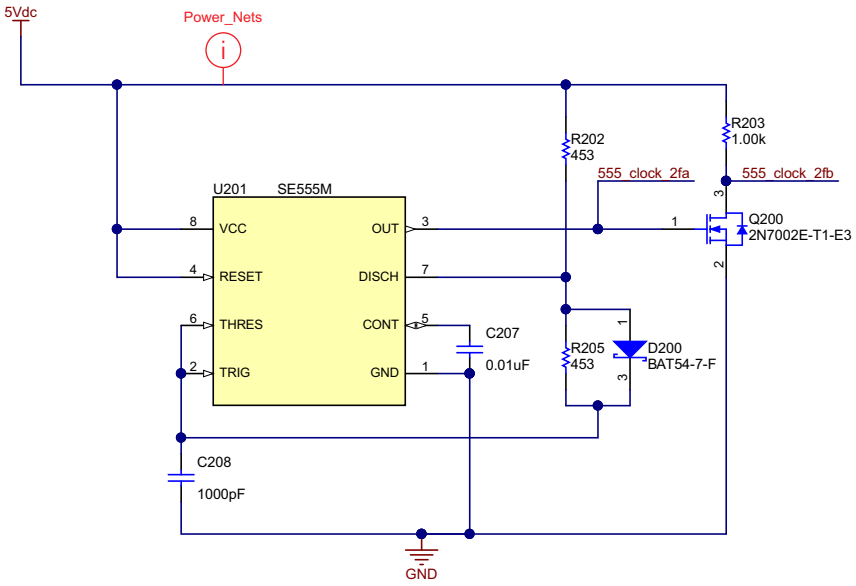

图 3. SE555-SP Design Schematic

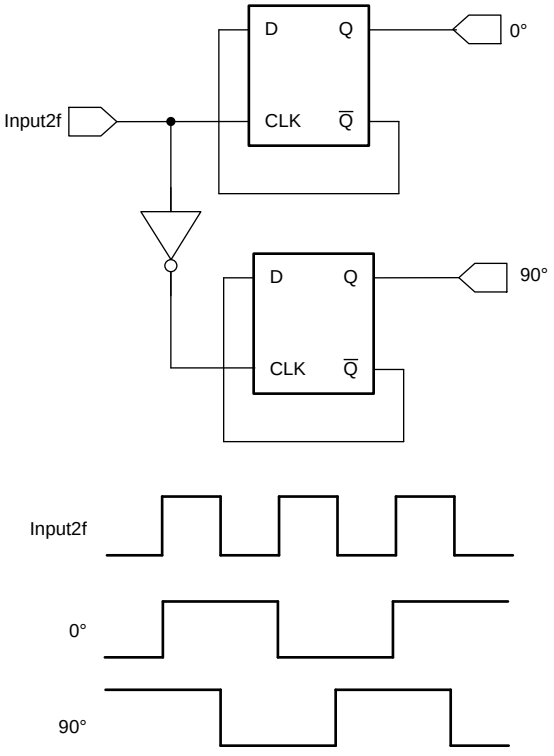

图 4. Quadrature Clock

As shown in 图 3, adding R205 to the circuit and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C208 charges through R202 and R205 and then discharges through R205 only. Therefore, the duty cycle is controlled by the values of R202 and R205

This astable connection results in capacitor C208 charging and discharging between the threshold-voltage level (×0.67 × VCC) and the trigger-voltage level (⨯0.33 × VCC). As in the monostable circuit of the datasheet for the SE555-SP, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage. Please refer to the SE555-SP datasheet to for equations to help with component selection

图 5 shows the configuration SN54HC74-SP in the system.

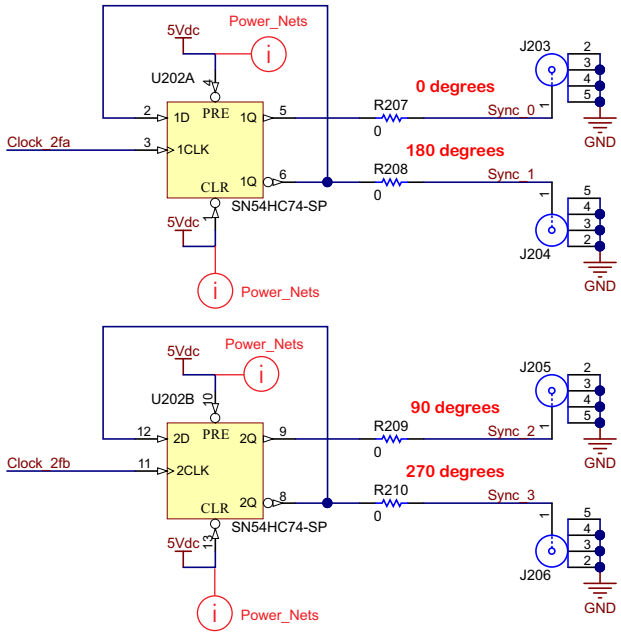

图 5. SN54HC74-SP Design Schematic

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. The resistor and capacitor at the CLR pin are optional. If they are not used, the CLR pin should be connected directly to VCC to be inactive.

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs may be combined to produce higher drive, but the high drive will also create faster edges into light loads. Because of this, routing and load conditions should be considered to prevent ringing.

3.1.1.1.2.2 Parallel Clocking Hex Converter

Clocking configuration two requires an external clock and uses the hex inverter to generate two sets of 180° phase shift clocks. This clocking configuration best shows the parallel capabilities of the TPS50601A-SP devices. This option also allows for completely independent rails while still maintaining a level of synchronization in the system that fits the desired design.

图 6 shows the configuration of the SN54HC04-SP in the system.

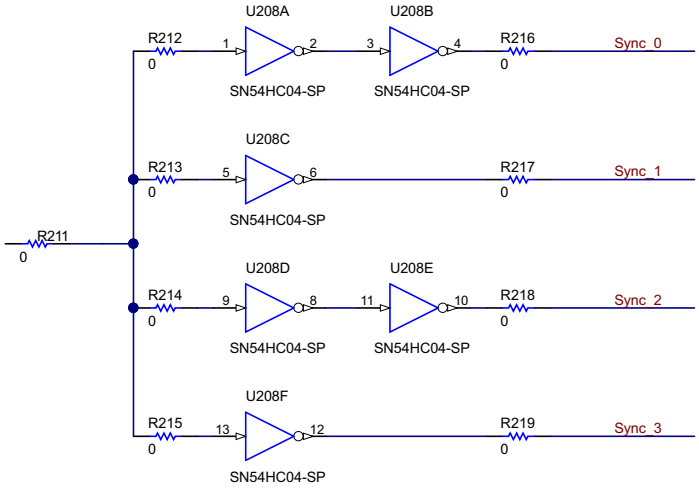

图 **6. SN54HC04-SP Design Schematic**

3.1.1.1.2.3 Customizable Phase Shifts Single Inverters

The third clocking configuration allows for the user to select any number of 180° phase shifts in clocking by using or not using the SN74AHC1G04 inverter IC. By using and external clock users can populate or depopulate the SN74AHC1G04 indenters. This clocking option allows for the buck regulators to operate independently of one another (not in master slave mode) while still current sharing in parallel if desired. This option also allows for completely independent rails while still maintaining a level of synchronization in the system that fits the desired design.

3.1.1.1.3 Current Monitoring

There are four INA901-SP current sense amplifiers on the mother board. Each one monitors the current out of each POL for evaluation. 图 7 shows the configuration of the INA901-SP in the system.

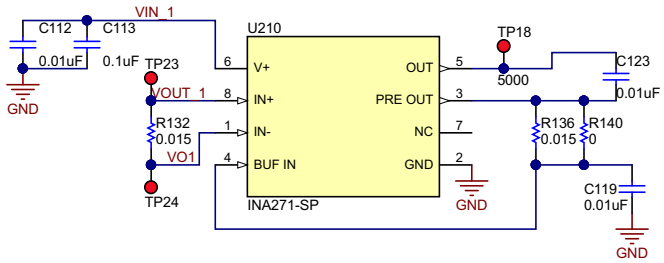

图 **7. INA901-SP Design Schematic**

Setting the Rs of the INA901-SP. (R131, R132, R133, R134)

The value chosen for the shunt resistor, RS, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of RS provide better accuracy at lower currents by minimizing the effects of offset, while low values of RS minimize voltage loss in the supply line. For most applications, best performance is attained with an RS value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (VS – 0.2) / Gain.

3.1.1.1.4 Operation Modes

表 4. Operation Modes

Operation Mode		Variant 001 – Quadrature operation 555 timer	Variant 002 – Quadrature operation external clock used	Variant 003 – Parallel operation master slave	Variant 004 – Two parallel master slave two individually synchronized	Variant 005 – All Individual rails external clock synchronized 180° phase shift	Variant 006 – All Individual rails external clock synchronized selectable phase shift
# of separate power rails		1	1	2	3	4	4
PWR	R116	Y	Y	Y	Y	Y	Y
	R143	Y	Y	Y	Y	Y	Y
	R144	DNP	DNP	DNP	DNP	DNP	DNP
	R200	DNP	DNP	DNP	DNP	DNP	DNP
Sync	R100	DNP	DNP	Y	Y	DNP	DNP
	R101	DNP	DNP	DNP	DNP	DNP	DNP
	R102	DNP	DNP	Y	DNP	DNP	DNP
Comp	R103	Y	Y	Y	Y	DNP	DNP
	R104	Y	Y	DNP	DNP	DNP	DNP
	R105	Y	Y	Y	DNP	DNP	DNP
Vsns	R107	Y	Y	Y	Y	DNP	DNP
	R108	Y	Y	DNP	DNP	DNP	DNP
	R109	Y	Y	Y	DNP	DNP	DNP
En	R117	Y	Y	Y	Y	DNP	DNP
	R118	Y	Y	DNP	DNP	DNP	DNP
	R119	Y	Y	Y	DNP	DNP	DNP
SS	R128	Y	Y	Y	Y	DNP	DNP
	R129	Y	Y	DNP	DNP	DNP	DNP
	R130	Y	Y	Y	DNP	DNP	DNP
Individual Inverters	R220	DNP	DNP	DNP	DNP	Y	DNP
	R225	DNP	DNP	DNP	DNP	DNP	DNP
	R229	DNP	DNP	DNP	DNP	Y	DNP
	R226	DNP	DNP	DNP	DNP	DNP	DNP
	R230	DNP	DNP	DNP	DNP	Y	DNP
	R227	DNP	DNP	DNP	DNP	DNP	DNP
	R231	DNP	DNP	DNP	DNP	Y	DNP
	R228	DNP	DNP	DNP	DNP	DNP	DNP
	R232	DNP	DNP	DNP	DNP	Y	DNP
	R221	Y	Y	Y	Y	Y	Y
	R222	Y	Y	Y	Y	Y	Y
	R223	Y	Y	Y	Y	Y	Y
	R224	Y	Y	Y	Y	Y	Y
Hex Inverter	R211	DNP	DNP	Y	Y	Y	DNP
	R216	DNP	DNP	Y	Y	Y	DNP
	R217	DNP	DNP	Y	Y	Y	DNP
	R218	DNP	DNP	Y	Y	Y	DNP
	R219	DNP	DNP	Y	Y	Y	DNP

表 4. Operation Modes (continued)

Operation Mode		Variant 001 – Quadrature operation 555 timer	Variant 002 – Quadrature operation external clock used	Variant 003 – Parallel operation master slave	Variant 004 – Two parallel master slave two individually synchronized	Variant 005 – All Individual rails external clock synchronized 180° phase shift	Variant 006 – All Individual rails external clock synchronized selectable phase shift
Quadrature Clock Selection	R206	DNP	Y	DNP	DNP	DNP	DNP
	R234	DNP	Y	DNP	DNP	DNP	DNP
	R235	Y	DNP	DNP	DNP	DNP	DNP
	R236	DNP	Y	DNP	DNP	DNP	DNP
	R237	Y	DNP	DNP	DNP	DNP	DNP
Flip Flops	R207	Y	Y	DNP	DNP	DNP	DNP
	R208	Y	Y	DNP	DNP	DNP	DNP
	R209	Y	Y	DNP	DNP	DNP	DNP
	R210	Y	Y	DNP	DNP	DNP	DNP
Power Resistors	R106	Y	Y	DNP	DNP	DNP	DNP
	R110	Y	Y	DNP	DNP	DNP	DNP
	R111	Y	Y	DNP	DNP	DNP	DNP
	R115	Y	Y	DNP	DNP	DNP	DNP
	R120	Y	Y	DNP	DNP	DNP	DNP
	R121	Y	Y	DNP	DNP	DNP	DNP
	R122	Y	Y	DNP	DNP	DNP	DNP
	R123	Y	Y	DNP	DNP	DNP	DNP
	R124	Y	Y	DNP	DNP	DNP	DNP
	R125	Y	Y	DNP	DNP	DNP	DNP
	R126	Y	Y	DNP	DNP	DNP	DNP
	R127	Y	Y	DNP	DNP	DNP	DNP
Power Jumpers	J102	DNP	DNP	DNP	DNP	DNP	DNP
	J105	DNP	DNP	DNP	DNP	DNP	DNP
	J107	DNP	DNP	DNP	DNP	DNP	DNP
	J110	DNP	DNP	DNP	DNP	DNP	DNP

3.1.1.1.4.1 Variant 001 – Quadrature operation 555 timer

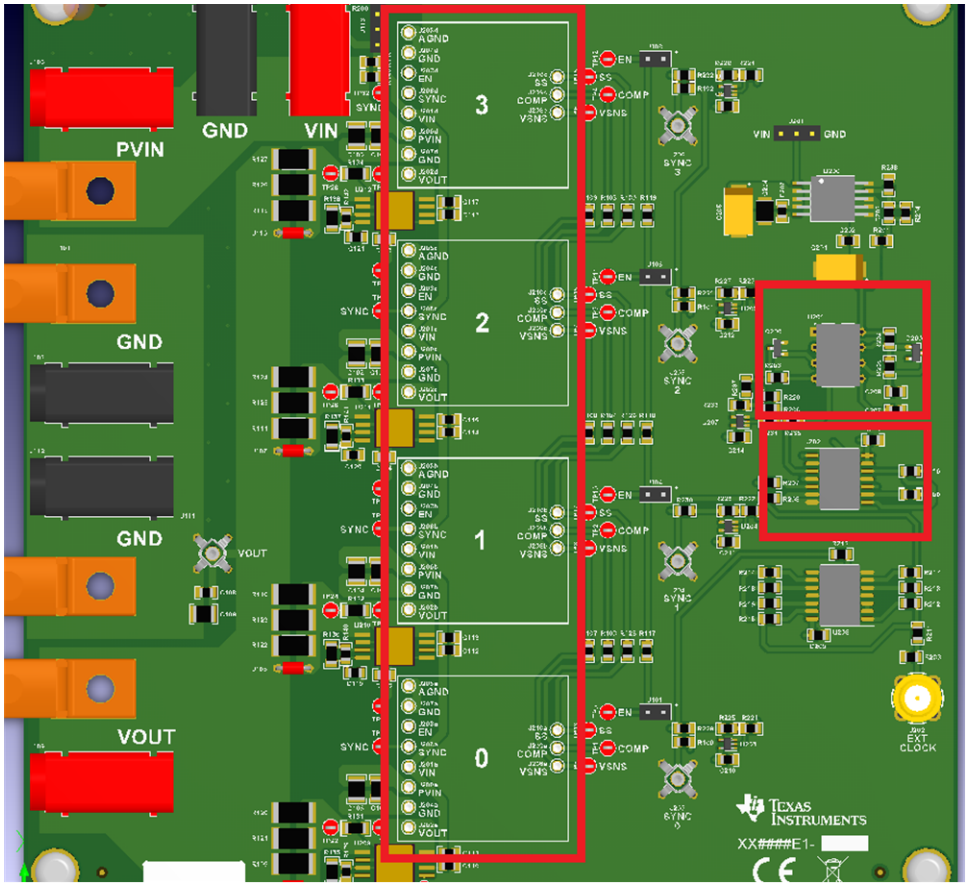

图 **8. Variant 001**

图 8 shows variant 001 of the TIDA-070005. Variant 001 showcases the quadrature operation of the TIDA-070005 in which all four TPS50601A-SP are clocked 90° out of phase with each other via the digital phase splitter circuitry where the 2f input is generated by the drain and gate voltages of the N type FET on the output of the SE555 555 timer.

3.1.1.1.4.2 Variant 002 – Quadrature operation external clock used

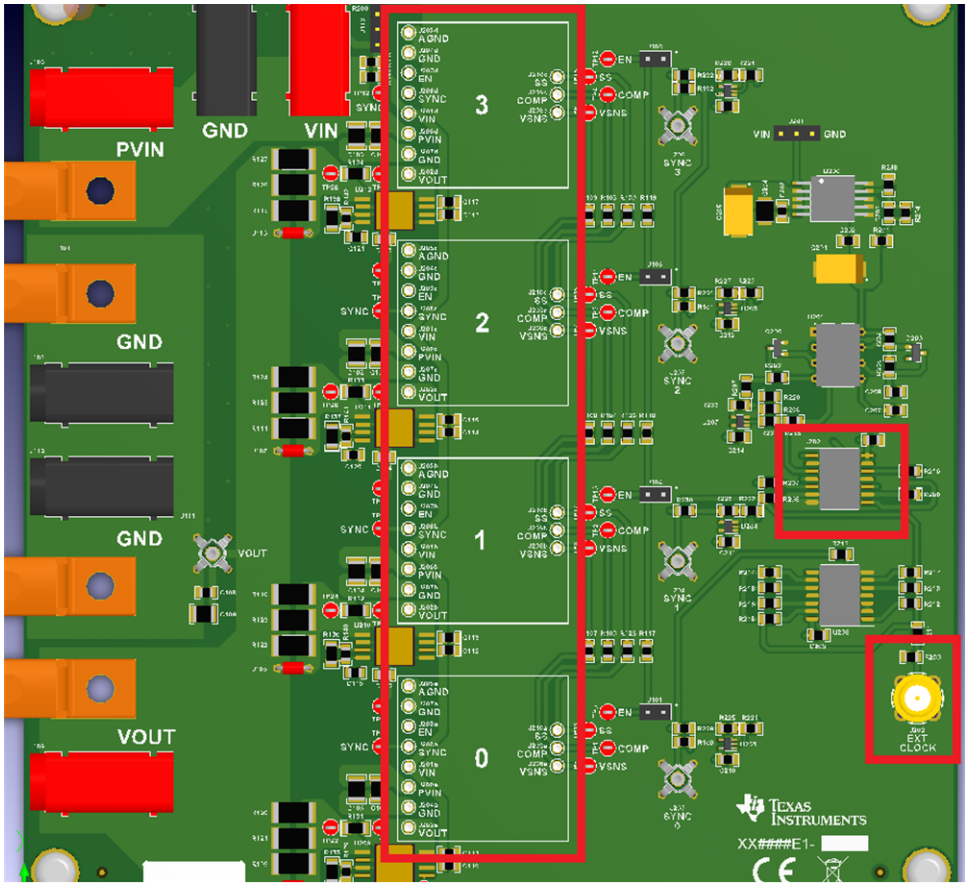

图 **9. Variant 002**

图 9 shows variant 002 of the TIDA-070005. Variant 002 showcases the quadrature operation of the TIDA-070005 in which all four TPS50601A-SP are clocked 90° out of phase with each other via an externally generated clock signal that is 2 times the frequency of the POL switching frequency.

3.1.1.1.4.3 Variant 003 – Parallel operation master slave

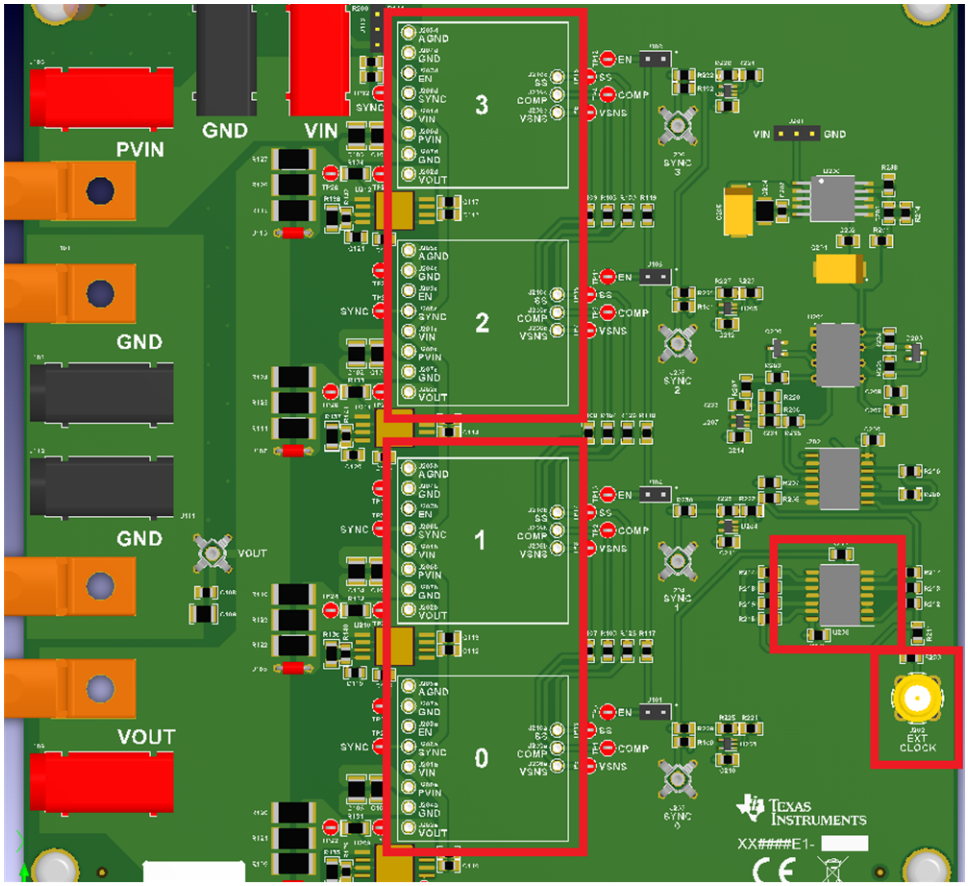

图 **10. Variant 003**

图 10 shows variant 003 of the TIDA-070005. Variant 0003 showcases the ability to have two sets of parallel POLs to generate two different power rails each having the capabilities of producing up to 12 A of current. This configuration uses an externally generated clocking signal and the hex inverter to generate the 180°out of phase clocks for each set of parallel operating POLs. POL 0 and 1 are in parallel and POL 2 and 3 are in parallel in this configuration

3.1.1.1.4.4 Variant 004 – Two parallel master slave two individually synchronized

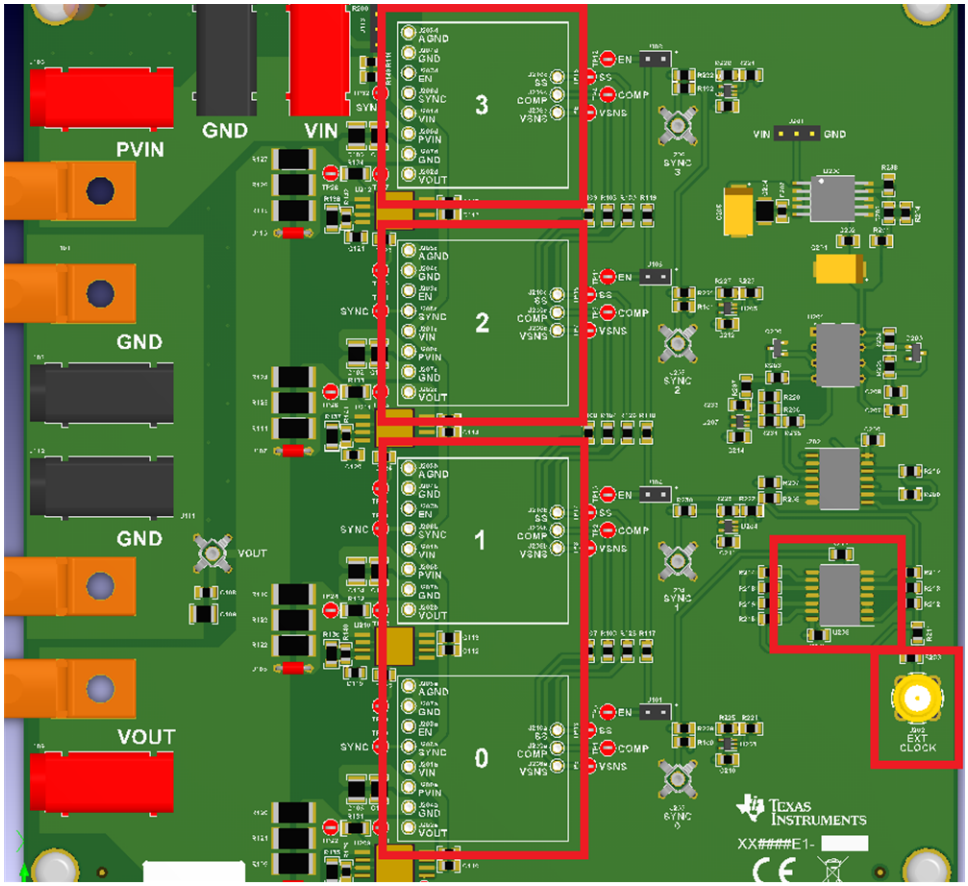

图 **11. Variant 004**

图 11 shows variant 004 of the TIDA-070005. Variant 004 showcases the ability to generate one high current rail by operating POL 0 and 1 in parallel to generate 12 A and then operating POLs 2 and 3 independently to generate 2 individual rails each with 6-A capability.

3.1.1.1.4.5 Variant 005 – All Individual rails external clock synchronized 180° phase shift

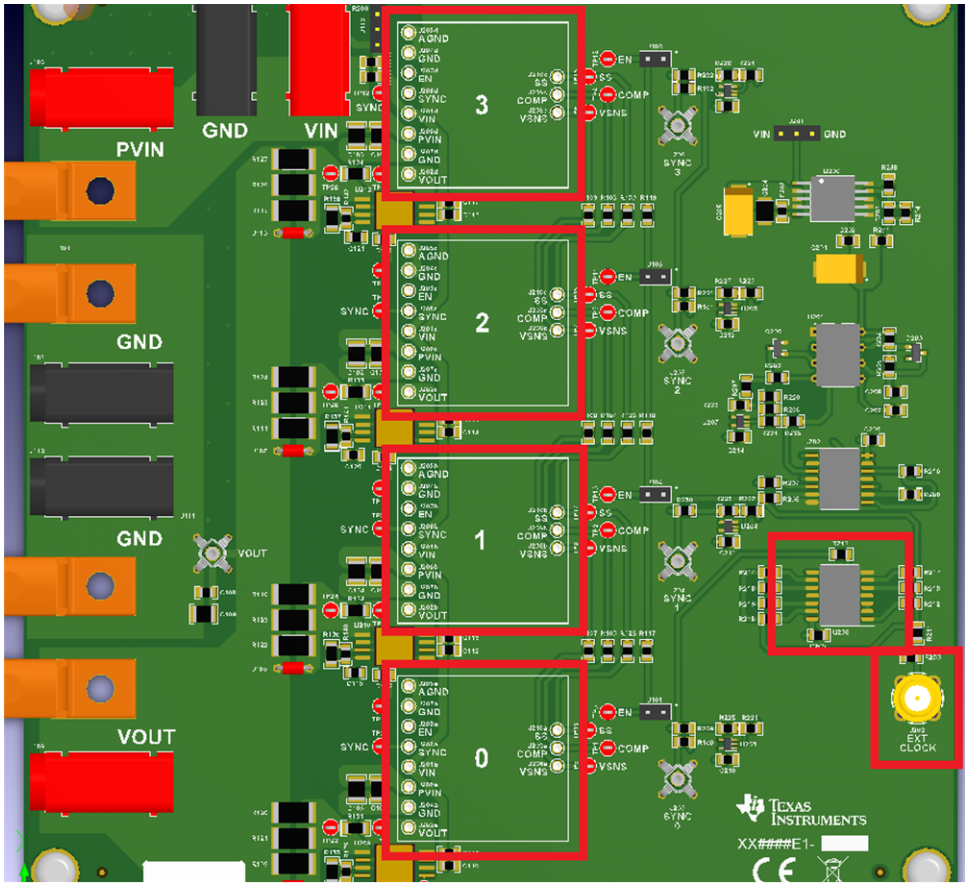

图 **12. Variant 005**

图 12 shows variant 005 of the TIDA-070005. Variant 005 showcases the ability to operate all 4 POLs independently from one another with having POLs 0 and 1 operate at 180° out of phase with one another as well as POLs 2 and 3 operating 180° out of phase with one another.

3.1.1.1.4.6 Variant 006 – All Individual rails external clock synchronized selectable phase shift

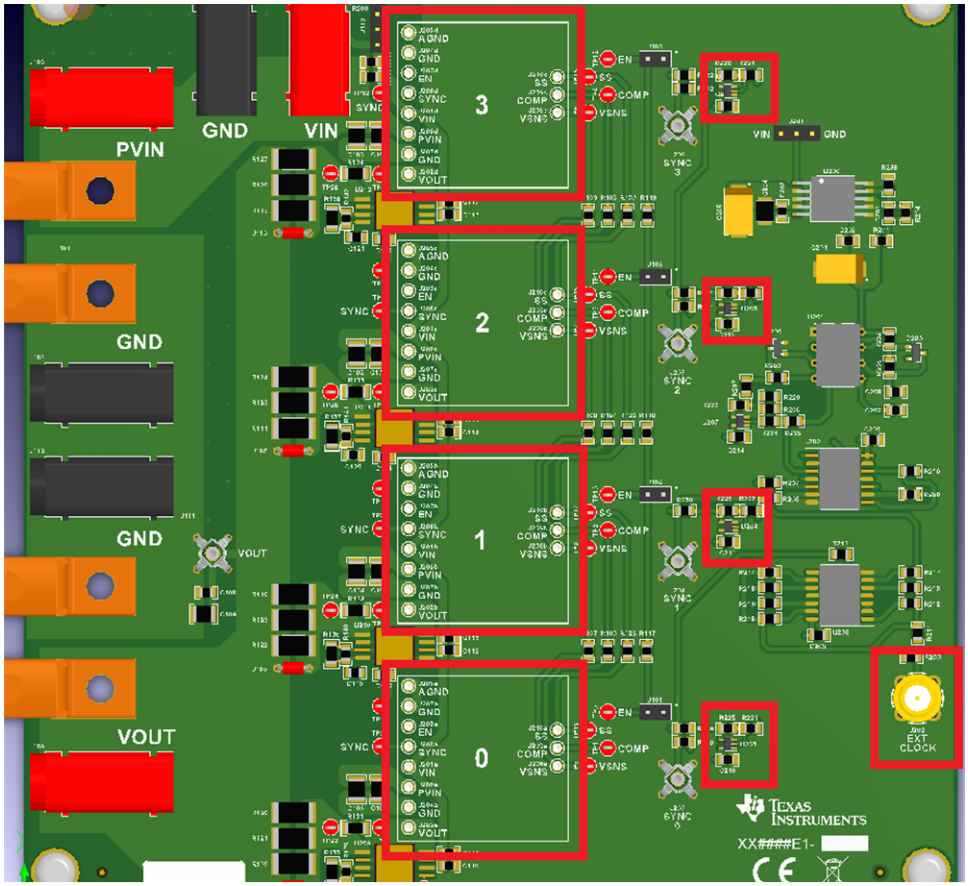

图 **13. Variant 006**

图 13 shows variant 006 of the TIDA-070005. Variant 006 showcases the ability to operate all 4 POLs independently from one another while allowing the user to select any combination of converters to operate in phase or 180° out of phase with the external clock and individual inverters. This is using the third clocking option.

3.1.1.2 Daughter Board

The daughter board is shown in 图 14 and its schematic is shown in 图 15. Four of these boards will plug into the mother board for normal operation.

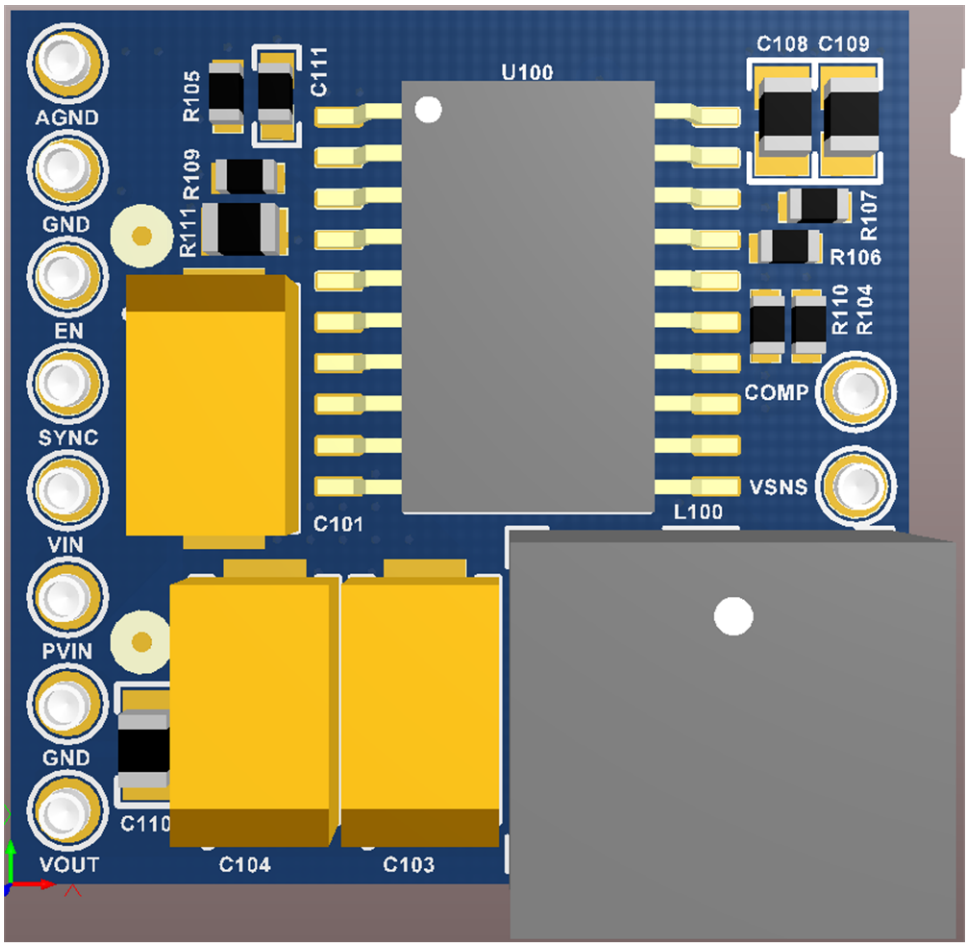

图 **14. Daughter Board Top View**

- R109 is the RT resistor. this must be set to the desired switching frequency of the POLs (1/2 the switching frequency generated by the SE555-SP timer).
- R107, C108, and C109 are the passives for the compensation network. *Note in current sharing mode only one TPS50601A-SP POL will have these passives populated*.
- R104, F106, R110, and C107 make up the feedback network that sets the voltage to the VSENSE pin. *Note in current sharing mode only one TPS50601A-SP POL will have these passives populated*.

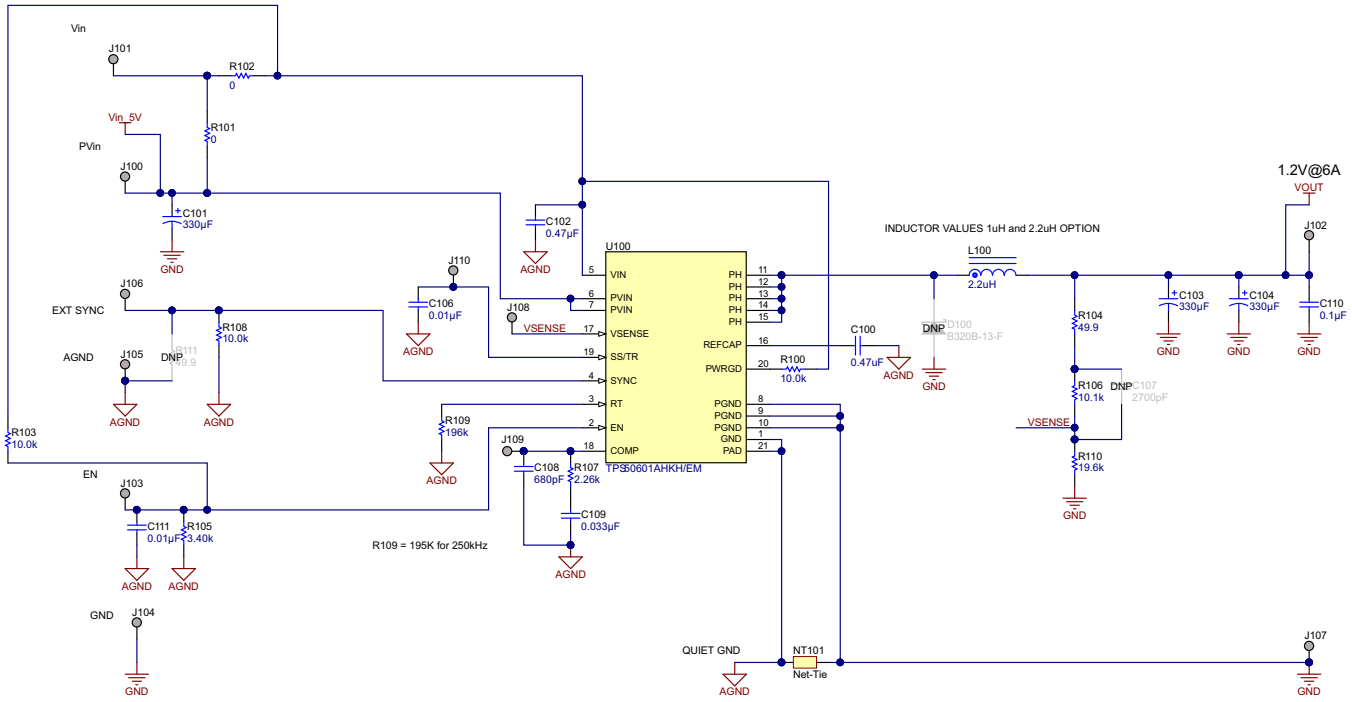

图 **15. TPS50601A-SP Design Schematic**

The switching frequency of the device supports three modes of operations. The modes of operation are set by the conditions on the RT and SYNC pins. At a high level, these modes can be described as master, internal oscillator, and external synchronization modes. In master mode, the RT pin should be left floating; the internal oscillator is set to 500 kHz, and the SYNC pin is set as an output clock. The SYNC output is in phase with respect to the internal oscillator. SYNC out signal level is the same as VIN level with 50% duty cycle. SYNC signal feeding the slave module, which is in phase with the master clock, gets internally inverted (180° out of phase with the master clock) internally in the slave module. In internal oscillator mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a 10-kΩ resistor to GND for this mode to be effective. The switching frequency of the device is adjustable from 100 kHz to 1 MHz by placing a maximum of 510 kΩ and a minimum of 47 kΩ, respectively. To determine the RT resistance for a given switching frequency, please refer to the TPS50601A-SP datasheet.

When operating the converter in internal oscillator mode (internal oscillator determines the switching frequency (500 kHz) default), the synchronous pin becomes the output and there is a phase inversion. When trying to parallel with another converter, the RT pin of the second (slave) converter must have its RT pin populated such that the converter frequency of the slave converter must be within ±5% of the master converter. This is required because the RT pin also sets the proper operation of slope compensation.

In external synchronization mode, a resistor is connected between the RT pin and GND. The SYNC pin requires a toggling signal for this mode to be effective. The switching frequency of the device goes 1:1 with that of SYNC pin. External system clock-user supplied sync clock signal determines the switching frequency. If no external clock signal is detected for 20 µs, then TPS50601A-SP transitions to its internal clock, which is typically 500 kHz. An external synchronization using an inverter to obtain phase inversion is necessary. RT values of the master and slave converter must be within ±5% of the external synchronization frequency. This is necessary for proper slope compensation. A resistance in the RT pin is required for proper operation of the slope compensation circuit. To determine the RT resistance for a given switching frequency, please refer to the TPS50601A-SP datasheet.

There are several industry techniques used to compensate DC-DC regulators. For this design, type 2B compensation is used as shown in the *Small Signal Model for Frequency Compensation* section of the device datasheet. First, the modulator pole, fpmod, and the RESR zero, fzmod must be calculated using the equations in the datasheet. A starting point for the closed loop crossover frequency fco, can also be calculated as indicated in the datasheet and then the required compensation components may be derived.

The TPS50601A-SP output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends to use 1% tolerance or better resistors. Start with a 10 kΩ for RTOP and use Equation 1 in the device datasheet to calculate RBOTTOM. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

3.2 Quick Start Guide

The below provides quick steps to Starting up the TIDA-70005 using Operating Mode Variant 001 which uses the stand alone on board quadrature clock generating circuitry and Power Option 2.

1. Without powering on: Connect a 6-V power supply and its ground return to J114 and J115 respectively - this is the power to the TPS7A4501-SP and the downstream clocking ICs
2. Without powering on: Connect a 5-V power supply and its ground return to J100 and J103 respectively - this is the PVin and Vin to the TPS50601A-SP POLs on the board
3. Without powering on: Connect an electronic load capable of sinking up to 25-A DC to J109 and J112
4. Power on the 6-V supply to the TPS7A4501-SP
5. Confirm the quadrature clocks are properly being generated by probing J203, J204, J205, J206
6. Power of the 5-V supply to the POLs
7. Confirm that the POLs are properly regulated to the correct voltage by validating on any jumper J102, J105, J107, J110
8. Set the electronic load to 1 A and turn on
9. Verify that the POLs are properly regulating and supplying current
10. Increase the electronic loads current consumption to design specifications, that do not exceed 24 A

3.3 Testing and Results

3.3.1 Test Setup

Pictures of the test setup used to evaluate the TIDA-070005 are shown in 图 16, 图 17, 图 18 and 图 19.

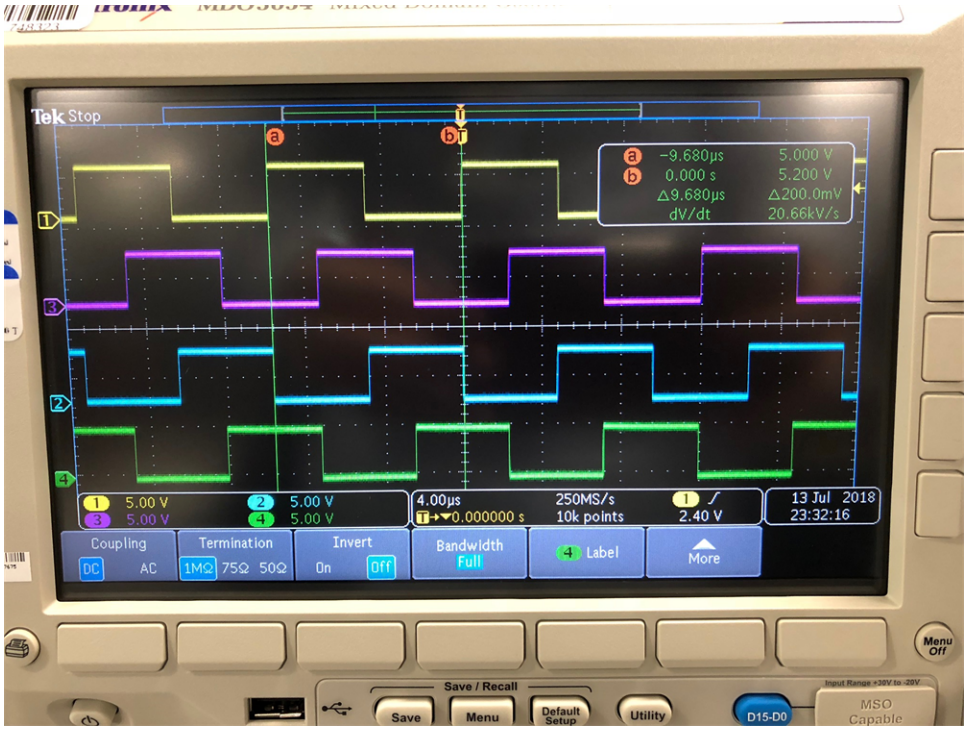

图 16. Quadrature Clock Verification

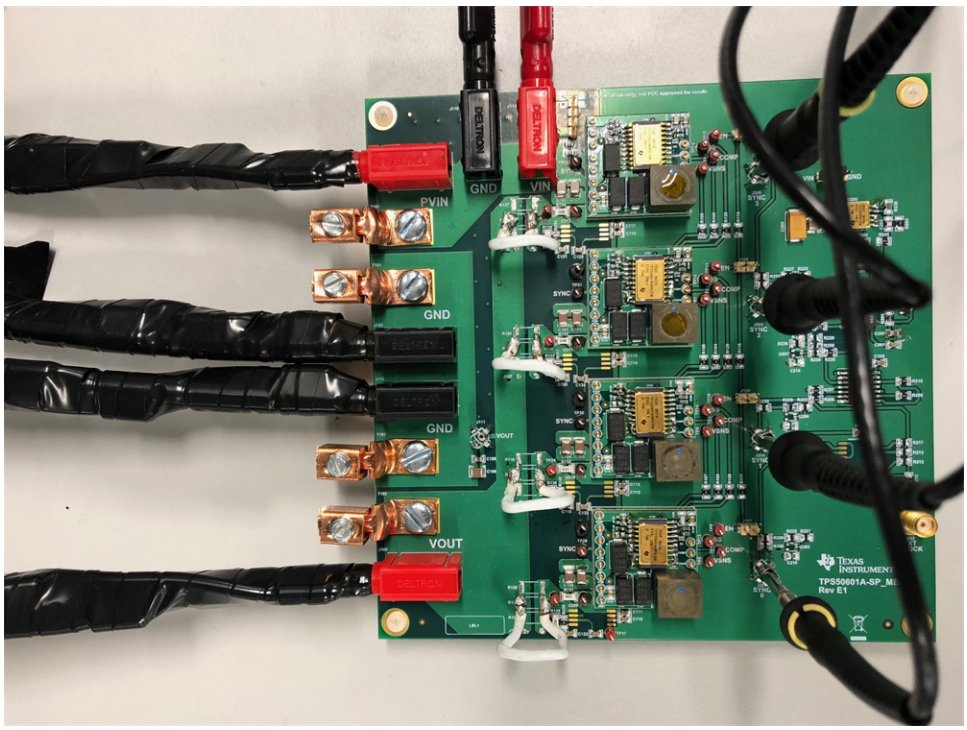

图 17. PVin and Vin Power Connections (Power Option 2)

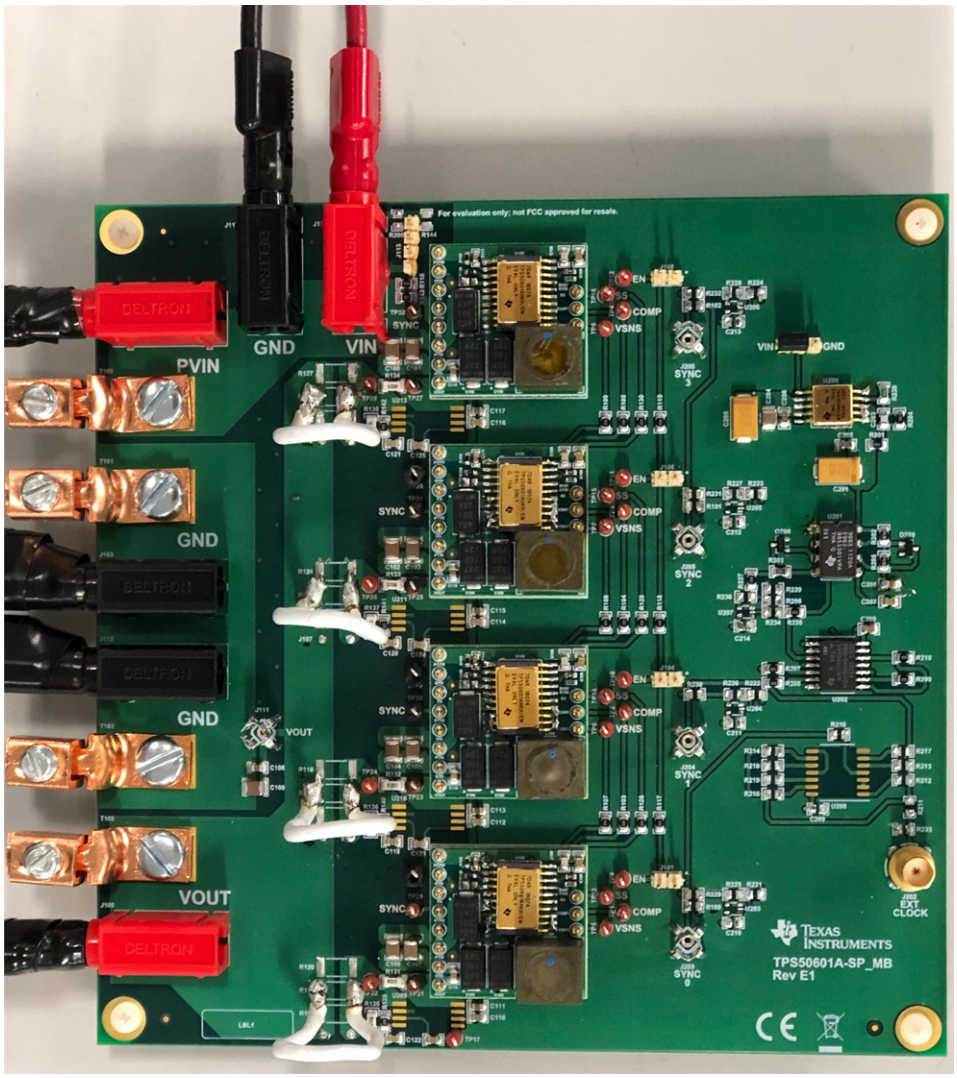

图 **18. Vin_LDO_6V Power Connections (Power Option 2)**

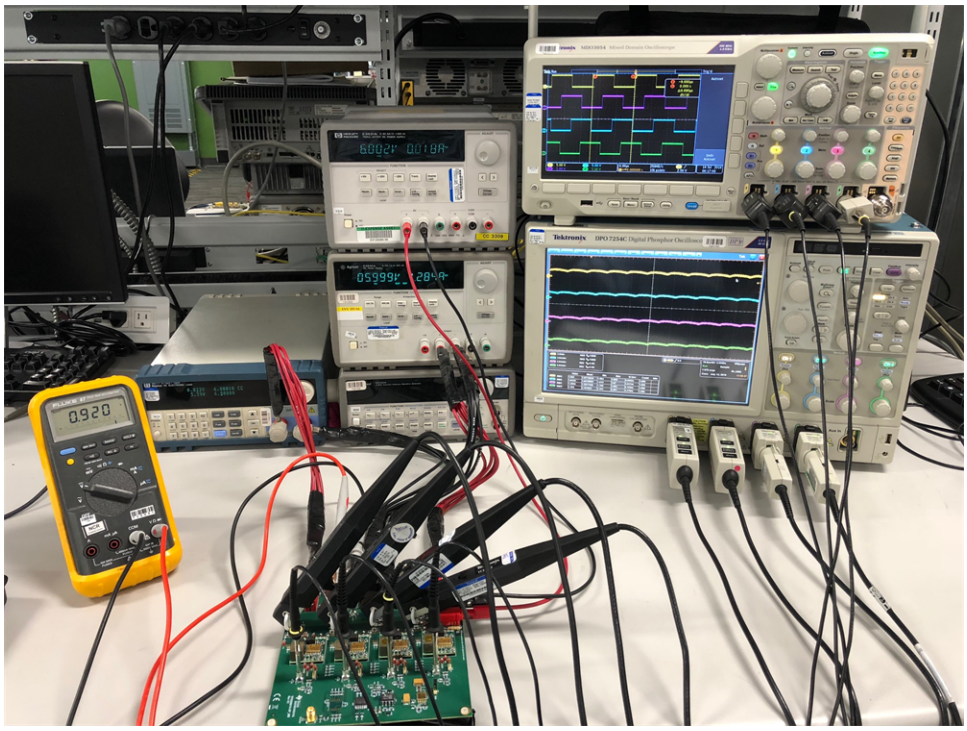

图 **19. Test Setup and Operation at 6-A Load**

3.3.2 Test Results

The TIDA-70005 was tested under the following conditions:

- VIN = 5 V
- VOUT = 0.95 V
- f_{SW} = 100 kHz
- T = 25°C

图 20 shows the data collected under these conditions.

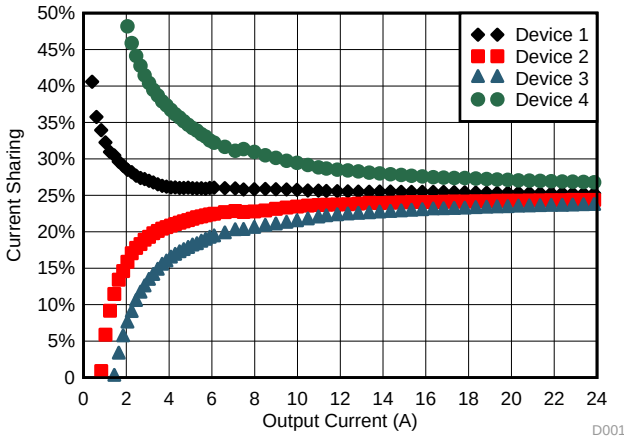

图 **20. Current Sharing Results Out to 24 A in Quadrature Operation**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-070005.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-070005.

4.3 PCB Layout Recommendations

The main concern with the mother board is to keep all TPS50601A-SP as close as possible so that the common output is close to each of them. The layout for the daughter boards has more constraints as it involves the switching node and the analog sensitive signals of each TPS50601A-SP. The main recommendations follow the ones described in the TPS50601A-SP datasheet as follows:

- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor and the output filter capacitor.
- Thermal pad can be electrically floating or connected externally. If electrically connected externally then it must be connected to GND. Customer should evaluate their system performance when thermal pad is electrically isolated and thermally conductive.
- The PVIN and VIN pins should be bypassed to ground with ceramic capacitors placed as close as possible to the pins.
- Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The RT, REFCAP, and COMP pins are sensitive to noise so the respective components should be located as close as possible to the IC and routed with minimal lengths of trace.
- The feedback voltage signal VSENSE should be routed away from the switching node.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-070005.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-070005.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-070005.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-070005.

5 Related Documentation

1. *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter*, SLVSDF5
2. *TPS7A4501-SP Low-Dropout Voltage Regulator*, SLVSC31
3. *INA901-SP Radiation Hardened, –16-V to 80-V Common Mode, Unidirectional Current-Shunt Monitor*, SBOS938

4. *SE555-SP QML CLASS V PRECISION TIMER*, SGLS401
5. *SNx4HC74-SP Dual D-Type Positive-Edge-Triggered Flip-Flops With Clear and Preset*, SCLS094
6. *SNx4HC04-SP Hex Inverters*, SCLS078
7. *SN74AHC1G04 Single Inverter Gate*, SCLS318
8. *TI Space Rated Power Solution for Microsemi® RTG4™ FPGA*, SLVA857

5.1 商标

5.2 Third-Party Products Disclaimer

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (Debember 2018) to A Revision **Page**

- 已更改 将标题从“24A 航空级负载点参考设计”更改为“3V 至 7V 输入电压、24A 输出电流、0.95V 输出电压、航空级电流共享负载点 (POL) 参考设计” 1
- 已添加 添加了“命令和数据处理；卫星电力系统 (EPS)；光学成像有效载荷；雷达成像有效载荷以及通信有效载荷 应用”.. 1

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