TI Designs：TIDA-010026
*适用于 **EnDat 2.2** 绝对编码器的稳定接口参考设计*

说明

该参考设计展示了 EnDat 2.2 编码器的稳定接口。这其中展示了 EMC 抗扰性，尤其是逆变器开关噪声等快速瞬变抗扰性。编码器电源电压是可配置的并集成了短路保护，以防止由于电缆短路或误接线而造成的损坏，还集成了诊断反馈以检测故障。逻辑接口支持 3.3V 至 1.8V 的 I/O。该设计与 TI LaunchPad™开发套件兼容，从而能够轻松地使用 C2000™MCU 来评估 EnDat 2.2。该设计已使用最长 100m 的电缆针对多个 EnDat 2.2 编码器进行了测试。

资源

TIDA-010026	设计文件夹
THVD1450	产品文件夹
TPS62125	产品文件夹
TPS82150	产品文件夹
SN74LVC2T45	产品文件夹
TVS1401	产品文件夹
Launchxl-f28379d	产品文件夹

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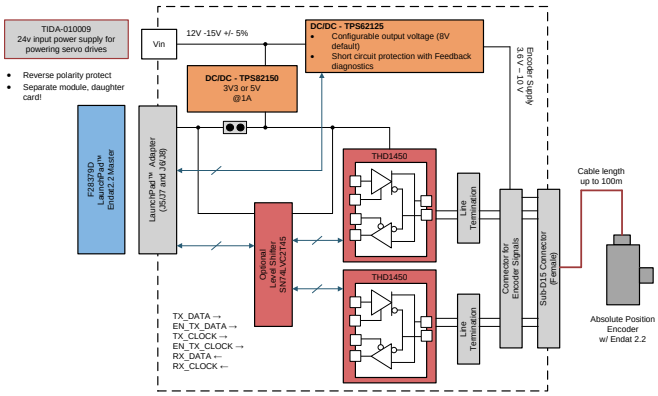
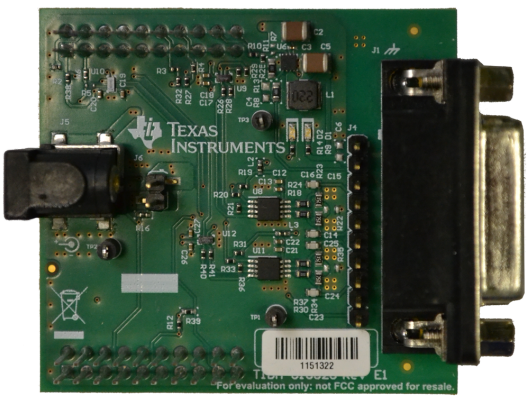
特性

- 电缆长度达 20m 时超过 16MHz 的 HEIDENHAIN EnDat 2.2 时钟频率，电缆长度达 100m 时超过 8MHz 的时钟频率
- 高度稳定的接口，凭借 3.3V 至 5V 的宽电源范围、半双工 RS-485 收发器 (THVD1450)、50 兆波特以及 ±15V 的共模范围、16kV 的 IEC-ESD 和 4kV 的 EFT，可实现高 EMC 抗扰性
- 设计经测试可满足 ESD (IEC61000-4-2)、EFT (IEC61000-4-4) 和浪涌 (IEC61000-4-5) 的 EMC 抗扰性要求，并达到 IEC61800-3 规定的级别和通过标准
- 可配置编码器电压默认为 8V，具有低纹波 (< 50mVpp)，输出符合 Endat 2.2 规格
- 编码器电源标称输出电流为 250mA，具有短路保护功能和电源正常状态反馈（用于诊断）
- 逻辑接口默认采用 3.3V I/O，以连接到运行 EnDat 2.2 主软件的主机处理器（如 C2000 MCU 或 Sitara ™处理器）

应用

- 伺服 CNC 和机器人
- 交流逆变器和 VF 驱动器
- 伺服驱动器位置传感器
- 工业机器人





1 System Description

Absolute digital encoders are used to get absolute position or rotary angle and feedback typically in industrial drives, like servo drives, CNC, and robotics EE.

There are multiple protocol standards, based on RS-485, RS-422 with synchronous or asynchronous communication and protocol-specific encoder supply voltage range. Drive customers are looking for a universal RS-485 digital interface to enable their drive to support the absolute encoder which fits best to the system.

The trend is for more precise and robust control of motors, additional safety features as well as predictive maintenance for lesser or complete avoidance of shutdown time.

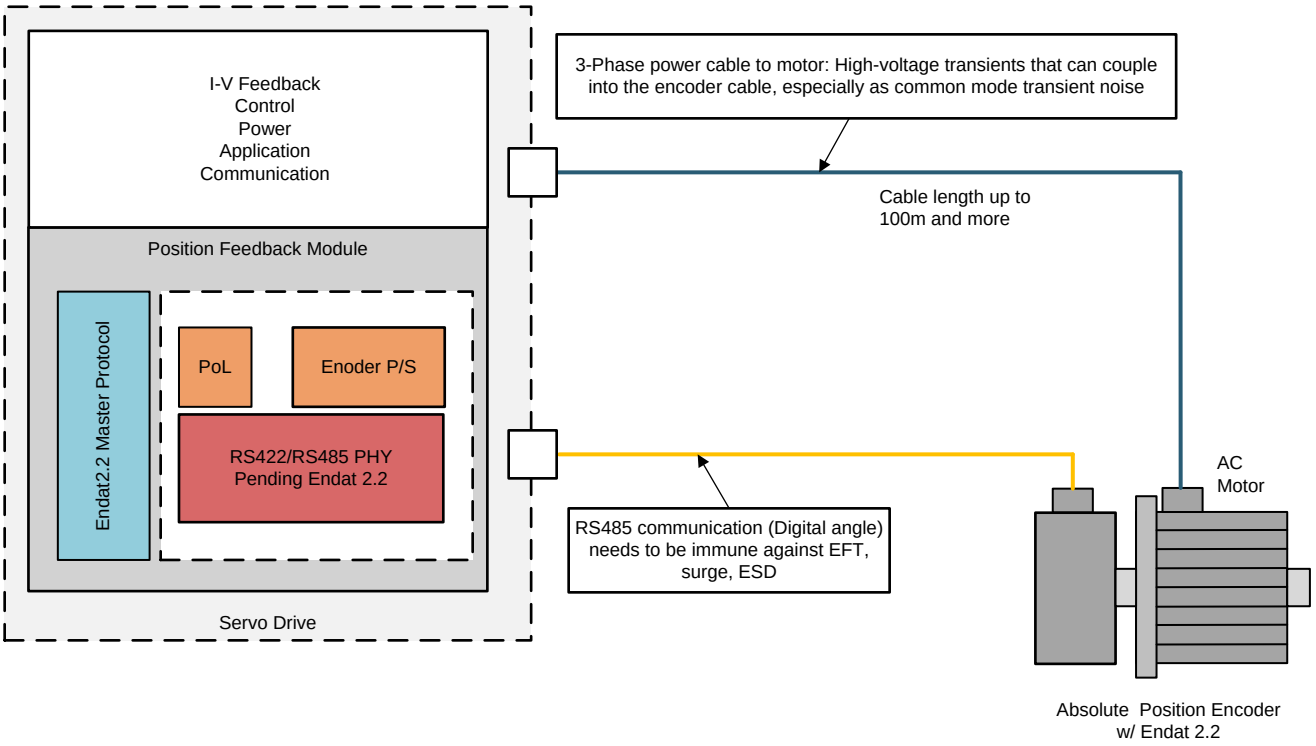
Robustness against harsh industrial environments yield higher reliability and less down-time

- In real drives, the most critical noise is PWM switching noise coupled into the shield of the power cable during the high-voltage PWM switching transients. These transients can be 10 kV/µs with IGBT and up to 50 to 100 kV/µs with SiC, in the future. These transients can couple typically as AC common-mode transients into the RS-485 differential signals. EFT and INS common-mode noise are the closest to real impulse noise in drives.
- Corrupt communication (bit errors) – despite being detected with CRC error – make the current position or angle read data invalid and can or will impact the performance of the drives. In the worst case, the drive must be shut down due to lack of angle correct information.

It is expected that much more attention also from the EMEA/U.S. drive and encoder customers is given to RS-485 immunity against ESD, surge, and especially EFT and INS. The trend to faster-switching GaN and especially SiC with higher impulse noise than existing IGBTs will further increase the importance of the RS-485 transceiver with high EMC (EFT) immunity.

图 1 shows a simplified system block of a hardware interface module supporting digital absolute position encoders. The design is shown as a subsystem of an industrial servo drive connected to the absolute position encoder. 图 1 shows that the RS-485 transceiver is needed in both the encoder and the drive.

图 1. Industrial Drive With Digital Interface to Absolute Position Encoders



1.1 IEC61800-3 EMC Immunity Standard

When building an industrial drive, the customer must pass the compliance test of the IEC61800-3 EMC standards. For more details on the IEC61800-3 standard, see this blog link or see this video link. The blog shows that there are several interfaces which must be tested.

For this design only, the “Port for process measurement control lines” is tested. On this interface ESD, EFT and surge immunity is tested as part of the IEC61800-3 standard for industrial drives.

表 1. IEC618000-3 EMC Immunity Requirements for Second Environment and Measured Voltage Levels and Class

REQUIREMENTS				
PORT	**PHENOMENON**	**BASIC STANDARD**	**LEVEL**	**PERFORMANCE (ACCEPTANCE) CRITERION**
Port for process measurement control lines	Electrostatic Discharge (ESD)	IEC61000-4-2	±4 kV CD or 8 kV AD, if CD not possible	B
Port for process measurement control lines	Fast transient Burst (EFT)	IEC61000-4-4	±2 kV / 5 kHz or 100 kHz, capacitive clamp	B
Port for process measurement control lines	Surge	IEC61000-4-5	±1 kV; since shielded cable > 20-m, direct coupling to shield (2 Ω, 500 A)	B

表 2 shows the performance (acceptance) criterion definitions.

表 2. Performance Criterion Definitions

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module continues to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module continues to operate as intended without manual intervention.
C	During the test, loss of functions is accepted, but no destruction of hardware or software. After the test, the module continues to operate as intended automatically, after manual restart, or power off, or power on.

Depending on where in the world the drive is EMC tested, there are other IEC standards for *Electrical Fast* transients. For example, Japan specifies an additional standard – the NECA TR-28 for impulse noise (INS), this design was tested against IEC61000-4-4.

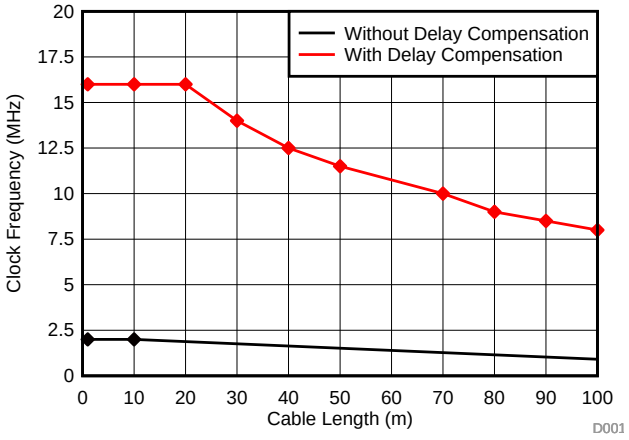
1.2 TI Design Overview

The major building blocks of this TI hardware design are the bidirectional 4-wire RS-485 interface, protected encoder power supply as well as a 3.3-V digital interface to a host processor to run the Endat 2.2 master protocol. The host processor that runs Endat 2.2 master protocol is not part of this design.

The position encoder with Endat 2.2 is connected to the subsequent electronics, for example, in the servo drive the encoder cable connection is typically a single, 8-wire shielded cable, as 图 1 shows. Only four signal lines are required. Two lines are for the bidirectional differential data (DATA+ and DATA–) and are transmitted in half-duplex mode. The other two lines are for the differential clock signal (CLOCK+ and CLOCK–). From the remaining wires, two wires are used for the encoder power supply. The other two wires are used for battery buffering or for parallel power-supply lines to reduce the cables losses.

EnDat 2.2 specifies differential line transmitter and receiver according to EIA standard RS-485 for the differential signals CLOCK+, CLOCK–, DATA+ and DATA–. The clock frequency is variable. The maximum clock frequency depends on the cable length, as outlined in 图 2.

图 2. Maximum Clock Frequencies Versus Cable Length up to 100 m for EnDat 2.2



With propagation-delay compensation in the ‘EnDat 2.2 Master’ the clock frequency can be from 100 kHz up to 16 MHz, and up to 100 m with 8 MHz. HEIDENHAIN cables must be used.

The data is transmitted and received synchronous to the clock signal, which is generated by the EnDat 2.2 Master. On the EnDat 2.2 Master, the transmit data changes on the falling edge clock edge. Without delay compensation on the *Master*, the receive data is latched on the rising clock edge. The clock remains high, when there is neither data transmitted or received.

1.3 Key System Specifications

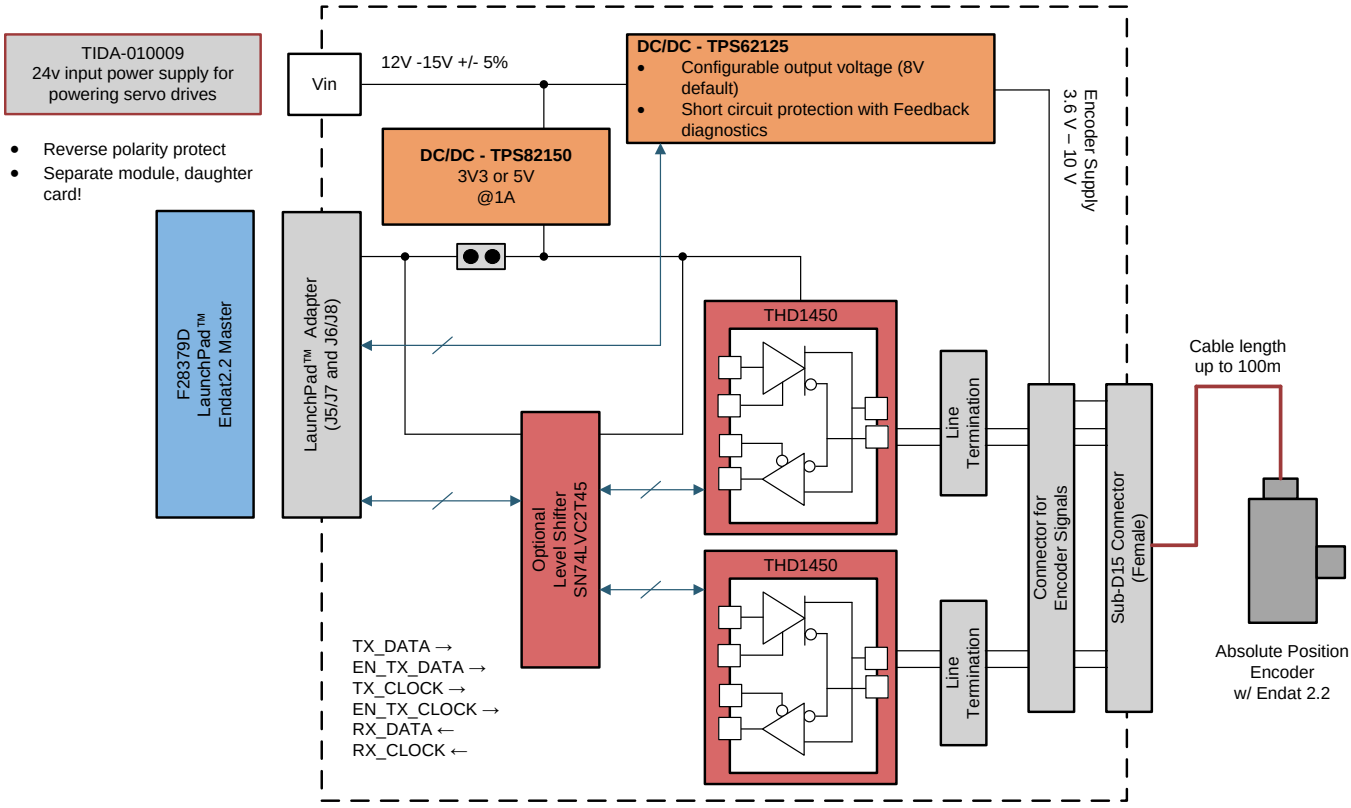
表 3. TIDA-010026 Specifications

PARAMETER	VALUE (TYPICAL)	COMMENT
Encoder standard	Endat 2.2	• HW: Compliant to Endat 2.2 standard • SW: Endat 2.2 Master for C2000 LaunchPad, see *Position Manager* software packet. • For further details about *Position Manager Software,* ask on TI's E2E forum.
Encoder connector	Sub D-15 or 10-pin header	Compatible to HEIDENHAIN adapter ID 524599-xx
DC input voltage	12 V to 15 V ±10%	2.1-mm ID, 5.5-mm ODM barrel DC jack. 15-V Input to supply the board.
RS-485 interface	2-channel half-duplex 5-V RS-485 transceiver	Can be configured for use in both Encoder and drive interface.
RS-485 Transceiver power supply	3.3 V or 5 V	Flexible power supply for 3.3 V or 5 V versions of RS-485 transceivers. The default 3.3 V.
RS-485 Baud rate	50 MBaud	Baud Rate exceeds Endat 2.2 specification for additional margin for better data rates for longer cable lengths.
Configurable encoder power supply	8-V Default 3.6 V to 10 V	Endat 2.2 specification is between 3.6 V and 14 V. For voltage above 10 V, see TIDA-00172 for power supply reference
Endat 2.2 ripple	< 50 mVpp	Exceeds Endat 2.2 specification
Encoder power supply protection	Short-circuit protection with Fault feedback	
Logic connector	2 × 20 Header	BoosterPack™ compliant for Launchxl-f28379d. For pin assignment, see 表 10.
I/O interface signaling voltage	3.3-V default	Also provides 3.3 V, 1-A rail to power a host processor such as the TMS320F28379D device.
PCB	4 Layer	
Temperature range [Ambient]	–40°C to 85°C	Industrial temperature range –40°C to 85°C. No heat sink required.
Electromagnetic compatibility (EMC)	According to IEC61800-3	Designed to exceed IEC61800-3, EMC levels and pass criterion for ESD, EFT and Surge according to test method described in: • IEC61000-4-2 • IEC61000-4-4 • IEC61000-4-5

2 System Overview

2.1 Block Diagram

图 3. TIDA-010026 System Block Diagram



2.2 Design Considerations

For this design, a 12- to 15-V input rail is used, and the latest RS-485 transceivers. This design supports an encoder using 2 power-supply wires and 2 RS-485 transceivers; one for clock and one for data transfer.

For more details on the different TI Designs supporting the Endat 2.2 standard, see TI designs listed in 表 4, per protocol.

表 4. Absolute Position Encoder Digital Interface TI Designs Supporting Endat 2.2

ENCODER PROTOCOL	TI DESIGN
Endat 2.2	TIDA-00172, TIDA-00179, TIDA-01401, TIDA-010026, TIDM-1008

Each of these Endat 2.2 TI Designs has different configurations of power supply requirements and functionality.

2.2.1 TI Design Hardware Considerations

RS-485 Transceiver Circuits

The Endat 2.2 protocol is a synchronous communication which runs up to a maximum of 16-MHz frequency on the clock communication path.

表 5 lists parameters with regards to RS-485 transceivers taken into consideration.

表 5. RS-485 Parameters From Corresponding Data Sheets (SLLSEY3)

PARAMETER	THVD1450
Supply voltage	3.3 V – 5 V
Baud rate (maximum)	50 Mbps
Receiver propagation delay (maximum)	40 ns
Driver propagation delay (maximum)	20 ns
Differential Input Voltage	±15 V
IEC61000-4-4 EFT (absolute maximum ratings)	±4 kV

Using this information, the RS-485 device selected is the THVD1450.

RS-485 Termination and Transient Protection

Instead of single 120-Ω, 0.1-W resistors, two smaller resistors 0603 in series 0.1 W each are chosen. A pulse-proof resistor is provisioned at the A and B bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up. In this design, these resistors are replaced with 0-Ω resistors to show the robustness of the THVD1450 device.

To further improve immunity against common-mode noise, two different circuit choices are shown.

Option 1: 330-pF bypass capacitors are added from each differential RS-485 outputs A and B to GND. See C14 and C25 in 图 4; these capacitors need to be high-quality capacitors (NP0, C0G).

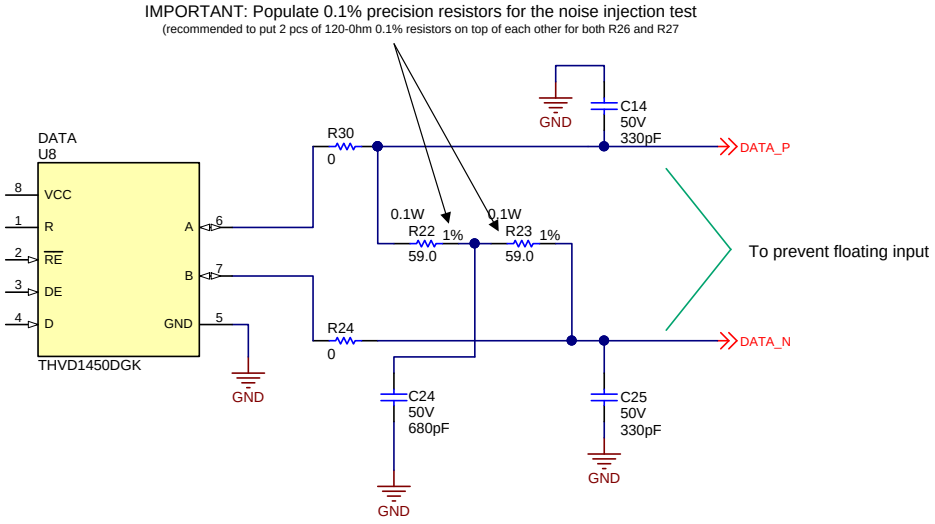
Option 2: 680-pF bypass capacitor C15 is added at the center point of the termination resistors R22 and R23.

This bypass capacitor removes the need to match the capacitors to have the same effect on the common mode during an event. The difference of the resistor values affects the equal distribution of an event. The capacitor must be a high-quality capacitor (NP0, C0G).

Option 1 is the HEIDENHAIN default recommendation for termination. For more details, see *EnDat 2.2 – Bidirectional Interface for Position Encoders*. This option is chosen as default for the Altium project for this design.

The bus terminals of the THVD14xx transceiver family possess on-chip ESD protection against ±30-kV human body model (HBM), ±16-kV IEC61000-4-2 contact discharge, and ±4-kV IEC61000-4-4 *Fast Transient Burst* meaning that no further protection is required when using shielded cables.

图 4. TIDA-010026 Schematic of Data Transceiver Circuit



For the data circuit, the resistors mentioned are R22, R23, and R33 and the capacitors are C14, C15, and C16.

5-V to 3.3-V Level shifter

Since the THVD1450 device is a 3.3-V to 5-V RS-485 transceiver, level translation may be needed. This level shifter must have propagation delay because this affects the system performance at long cable lengths. The SN74LVC2T45 device is chosen. With this device, 3 ICs are needed using two for transmitting data and one for receiving data. To ensure the same propagation delay, select VCCB to always support the RS-485 power rail and VCCA always supports the Endat 2.2 Master processor. With this configuration and the voltage levels chosen that the propagation delay on the level shifter is always the same.

表 6. Maximum Propagation Delay for 3.3-V to 5-V Level Translation From Corresponding Data Sheets (SCES516)

VCCA	VCCB	DIRECTION	PROPAGATION DELAY [t_{PLH} / t_{PHL}]
3.3 V	5 V	B to A	5.4 ns / 4.5 ns
5 V	3.3 V	B to A	3.9 ns / 3.5 ns

For other voltage-rail configurations, see the *SN74LVC2T45 Dual-bit dual-supply bus transceiver with configurable voltage translation* data sheet.

2.2.2 Host Processor Interface

Select the processor interface to work for the Launchxl-f28379d; this is implemented using the header J2 to J3 of the TI Design. For more details on the interface, see 节 3.1.1.3 in this design guide.

2.2.3 System Power Supply

The power supply for this design is defined from a 12-V or 15-V intermediate rail. This rail is typically available in a industrial drive. This rail is then supplying the digital interface and the Encoder Voltage.

To support a system with space constraints, the following considerations were done on the two rails:

- To reduce size of the Encoder voltage supply, a DC/DC with integrated enable, current limit and power

good signal was considered for a solution.

- To reduce size of the 3v3 rail, a DC/DC with integrated inductor was considered for a solution.

Self-heating of the IC must still be within the temperature specification of 85°C ambient.

Power supply for digital interface

表 7 shows the estimated worst-case current consumption of the LaunchPad and RS-485 transceivers.

表 7. Worst-Case Power Consumption

PARAMETER	POWER CONSUMPTION	CURRENT ON 3.3 V	LOSSES ON MODULE WITH 85% EFFICIENCY
LaunchPad (TMS320F28379D datasheet)	1.9305 W	585 mA	87.75 mA
THVD1450 Pd (worst case)	330 mW × 2	200 mA	30 mA
			117.75 mA

This would pull a 785-mA current from the 3.3-V rail; this value is not close to the reality for this design. In this case, the TIDA-010026 most likely requires around 30% of this value.

With this in mind, a 1-A DC/DC power supply is needed with an efficiency of at least 85%. This power supply also must support the temperature requirement of 85°C ambient without cooling.

The DC/DC module, which is including the inductor, was considered as a feasible choice for the solution with the high efficiency requirement in mind. Since the TPS82150 device has this feature, it is selected - if the temperature performance fits. This choice is explained in detail in this section.

The junction temperature uses the EVM Junction-to-Case thermal resistance to calculate the worst-case junction temperature of the TPS82150 device, see 公式 1:

$$T_{increase} = 58.2 \frac{°C}{W} \times 0.389\ W = 22.61°C \quad (1)$$

The device can operate at an ambient temperature up to 125°C – 22.61 = 102°C, taking the worst-case self-heating condition of the device into account. Due to this, the TPS82150 device was selected.

To get the 3.3-V output of the TPS82150 device, the equation from the *Setting the Output Voltage* section of the TPS82150 data sheet is used to generate the formula in 公式 2. This is used to calculate the output voltage feedback resistor divider setting.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.8\ V} - 1 \right) = \frac{100\ k\Omega}{\left(\frac{3.3\ V}{0.8\ V} - 1 \right)} \approx 316\ k\Omega \tag{2}$$

R2 is chosen to be 100 kΩ which gives a R2 of 316 kΩ.

Protected Power Supply for the Encoder

The input voltage specification of an Endat 2.2 Encoder is between 3.6 V and 14 V, from a drive perspective an Encoder is typically supplied with voltage range between a 5-V and 10-V supply, needing up to 250-mA current. The 8-V default is chosen for the design – a typical choice in drives, this enables support of longer cables without having to consider the voltage drop of the cable, when powering the encoder.

To add additional fault protection and diagnostics, a specification of the design is also to find a DC/DC power supply which enables integrated short-circuit protection and fault diagnostics. This enables the lowest system cost for the encoder interface.

The DC/DC power supply must support low ripple output voltage, this is needed for the sophisticated electronics of the Encoder.

The TPS62125 device is a good choice with the previous considerations, it has a 750-mA (typical) high-side current limit and diagnostic feedback, it supports the input voltage range and uses control methods which are optimized for a low ripple output voltage. With the high-side current limit feature, it is possible to detect short circuits while not drawing excess current on the Encoder rail. This is tested in 节 3.2.2.2.3.

To get the 8-V output voltage of the equation in the *Output Voltage Setting* section of the TPS62125 data sheet, the formula in 公式 3 is used to calculate the output voltage feedback resistor divider setting.

$$R_2 = \frac{R_1}{\left(\frac{V_{OUT}}{0.8\ V} - 1 \right)} = \frac{1\ M\Omega}{\left(\frac{8\ V}{0.8\ V} - 1 \right)} \approx 110\ k\Omega \tag{3}$$

R1 is chosen to be 1 MΩ which gives a R2 of 110 kΩ.

One limit of this device is the 85°C ambient temperature as the device is only used for the encoder with around 100-mA current consumption. This temperature can go higher but consideration must be made when calculating the T_J estimation. 公式 4 is used for an initial consideration taking 250-mA current consumption.

$$T_{increase} = 65.2 \frac{°C}{W} \times 0.25\ A \times 0.15 \times 8\ V = 19.56°C \tag{4}$$

This means that the device can operate at an ambient temperature up to 125°C – 19.56 = 105°C taking the worst-case self-heating condition of the device into account. The data sheet limit states that the device can only work up to 85°C which limits the device temperature operation range.

2.2.4 TI Design Hardware Updates

This design is an update of the TIDA-00172. The design uses a different approach of implementing the power supply and includes a higher-performing RS-485 transceiver.

2.2.5 TI Design Software Design

The C2000 microcontroller is selected to test this design. This is done using the SW library “Position manager” which enables the use of the Endat 2.2 protocol.

To generate this example software, the controlSUITE™ software package is needed.

The position manager libraries enable many different digital and analog Encoder interfaces. For more information on the Position Manager from C2000, see the following link:

www.ti.com/C2000Drives

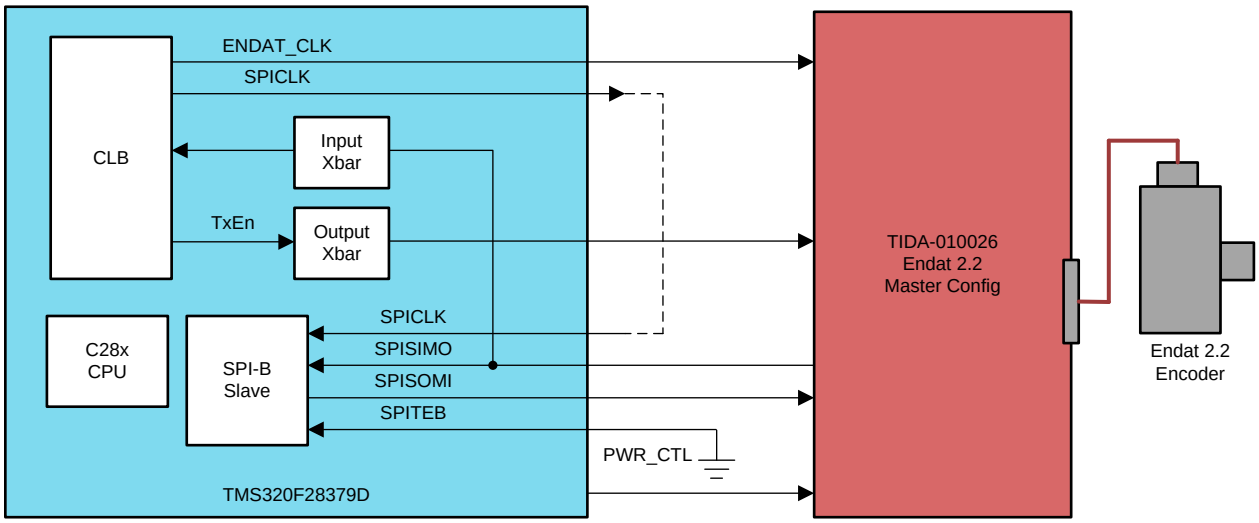
For the tests of this design, two types of software were built. One needed to test an Endat 2.2 interface and the other is used to generate eye diagrams and bit error tests. The Endat 2.2 software example is found in controlSUITE. To download controlSUITE, use the following link www.ti.com/ControlSuite

The software used for the tests is a demonstration version showing an Endat 2.2 connection giving the result back in a virtual com port. This is done combining two examples from ControlSuite, the first example shows the Endat 2.2 protocol, the second software shows a UART implementation using the C2000 MCU.

For questions on ControlSuite visit the e2e forum: https://e2e.ti.com/support/microcontrollers/c2000/

See the *C2000™ position manager EnDat22 library module* user's guide for Endat 2.2 documentation for the C2000. 图 5 shows how the software connects to the TIDA-010026 board. This figure is based on the *EnDat Implementation Diagram Inside TMS320F28379D* image in the *C2000™ position manager EnDat22 library module*.

图 5. Endat 2.2 Master C2000 Pin Connections



2.3 Highlighted Products

2.3.1 THVD1450

The THVD14xx devices are a family of noise-immune RS-485/RS- 422 transceivers designed to operate in rugged industrial environments. The bus pins of these devices are robust to high levels of IEC electrical fast transients (EFT) and IEC electrostatic discharge (ESD) events, eliminating the need for additional system level protection components.

Each of these devices operates from a single supply between 3 V and 5.5 V. The devices in this family feature an extended common-mode voltage range which makes them suitable for multi-point applications over long cable runs.

The THVD14xx family of devices is available in small VSON and VSSOP packages for space constrained applications. These devices are characterized over ambient free-air temperatures from –40°C to 125°C.

Features:

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3 V to 5.5 V supply voltage
- Extended operational common-mode range: ±15 V
- Bus I/O protection
  - ± 30 kV HBM
  - ± 18 kV IEC61000-4-2 contact discharge
  - ± 18 kV IEC61000-4-2 air-gap discharge
  - ± 4 kV IEC61000-4-4 fast transient burst
- Extended industrial temperature range: –40°C to 125°C
- Low power consumption
  - Low standby supply current: <1 μA
  - Current during operation: <3 mA
- Glitch-free power-up, power-down for hot plug-in capability
- Open, short, and idle bus failsafe
- 1/8 unit load options (up to 256 bus nodes)
- Small-size VSSOP packages save board space or SOIC for drop-in compatibility
- Low EMI 500 kbps 50 Mbps data rates

2.3.2 TPS62125

The TPS62125 device is a high-efficiency synchronous step-down converter optimized for low and ultra-low power applications providing up to 300-mA output current. With this feature, the converter can generate a power supply rail by extracting energy from a storage capacitor fed from high impedance sources such as solar panels or current loops. With its DCS-Control scheme the converter provides power-save mode operation to maintain highest efficiency over the entire load current range. At light loads

the converter operates in pulse frequency modulation (PFM) mode and transitions seamlessly and automatically in pulse width modulation (PWM) mode at higher load currents. The DCS-Control™ scheme is optimized for low-output ripple voltage in PFM mode to reduce output noise to a minimum and features excellent AC load regulation. An open-drain power good output indicates once the output voltage is in regulation.

Features:

- Wide input voltage range 3 V to 17 V
- Wide output voltage range 1.2 V to 10 V
- Low output ripple voltage
- Up to 1-MHz switching frequency
- Highest efficiency over wide VIN and VOUT range
- Pin-to-pin compatible with the TPS62160 and TPS62170 devices
- 100% duty cycle mode
- Power Good open drain output
- Output discharge function
- Small 2-mm × 2-mm 8-pin WSON package

2.3.3 TPS82150

The TPS82150 is a 17-V input 1-A step-down converter MicroSiP™ power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2.0 MHz and automatically enters Power Save Mode operation at light load currents. In Power Save Mode, the device operates with typically 20-µA quiescent current. Using the DCS-Control™ topology, the device achieves excellent load transient performance and accurate output voltage regulation.

Features:

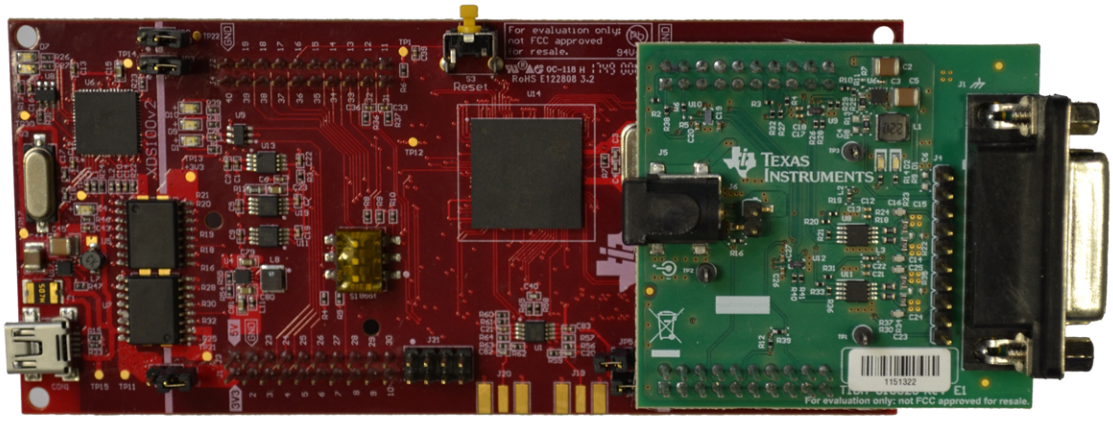
- 3.0-mm × 2.8-mm × 1.5-mm MicroSiP™ package
- 3.0-V to 17-V input range
- 1-A continuous output current
- DCS-Control™ topology
- 0.9-V to 6-V adjustable output voltage
- 100% duty cycle for lowest dropout
- Power Good output
- Programmable soft startup with tracking
- Thermal shutdown protection
- Pin-to-pin compatible with the TPS82130 (2 A) and TPS82140 (3 A) devices
- –40°C to 125°C operating temperature range

3 Hardware and Test Results

3.1 Hardware

图 6 shows the top side of the TIDA-010026 PCB with the Launchxl-f28379d. The headers and default jumper settings are explained in 表 9.

图 6. LaunchPad™ and TIDA-010026 (Top View)



3.1.1 Hardware Getting Started

3.1.1.1 Prerequisites

The following hardware equipment and software is required for the evaluation of the TIDA-010026 TI Design.

表 8. Prerequisites

EQUIPMENT	COMMENT
15-V DC power supply	15-V output power brick with at least 2-A output current capability 2.1-mm ID/5.5-mm OD mating barrel connector
TIDA-010026 hardware	With the default jumper settings per 节 3.1.1.2.
C2000 Endat 2.2 Master Software	Download ControlSuite, see 节 2.2.5.
F28379D LaunchPad	Available through TI eStore
Code Composer Studio 6	Download from https://www.ti.com
HEIDENHAIN shielded cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1 m	524599-1
Encoder	ROQ 437, EQN 1337, ROC 425

3.1.1.2 Default Resistor and Jumper Configuration

Prior to working with the TIDA-010026 board, make sure that the correct resistor settings are applied. 表 9 shows the default jumper configuration on the board.

表 9. Default Resistor and Jumper Settings

HEADER, RESISTOR	JUMPER, RESISTOR SETTING
R5, R6	Master(R5) or slave(R6 - Default) configuration for C2000 SPI data signals
R27, R32	Master(see layout guide lines 节 4.3.2) or slave (R27, R32 - Default) configuration for C2000 SPI data signals

3.1.1.3 Host Processor Interface

表 10 shows the signals the TIDA-010026 BoosterPack uses to communicate with the C2000 LaunchPad.

表 10. Pinout of J2 and J3 Host Processor Interface

LAUNCHXL-F28379D				TIDA-010026 REVISION E1			
J1	J3	J4	J2	J2		J3	
3V3	5V	PWM1A	GND	3V3	NC(5V)	ENC_CLK	GND
GPIO32	GND	PWM1B	SPIACS, GPIO61		GND	SPICLK	SPISTE
SCIB_RX	ADCIN14	PWM2A	GPIO123				
SCIB TX	ADCINC3	PWM2B	GPIO122	AUX_PG		EN_TX_DATA	
GPIO67	ADCINB3	PWM3A	RESETn	ENC_PG			
GPIO111	ADCINA3	PWM3B	SPIASIMO				SPISIMO
SPIACLK	ADCINC2	GPIO24	SPIASOMI	SPICLK, GPIO65			SPISOMI
GPIO22	ADCINB2	GPIO16	GPIO124				
GPIO105	ADCINA2	DAC1	GPIO125	EN_TX_CLK			ENC_PS_EN
GPIO104	ADCINA0	DAC2	GPIO29				

3.2 Testing and Results

The tests are taken at room temperature (around 28°C) with a 16-kHz RS-485 data package repetition. These tests characterize each individual functional block as well as the entire board. The following tests were conducted:

- Digital interface signal tests
- Power management
- System performance
- EMC tests

The tests are done at room temperature (around 28°C) with a 16-kHz Endat 2.2 protocol repetition rate, this the same repetition rate as in a typical drive.

3.2.1 Test Setup

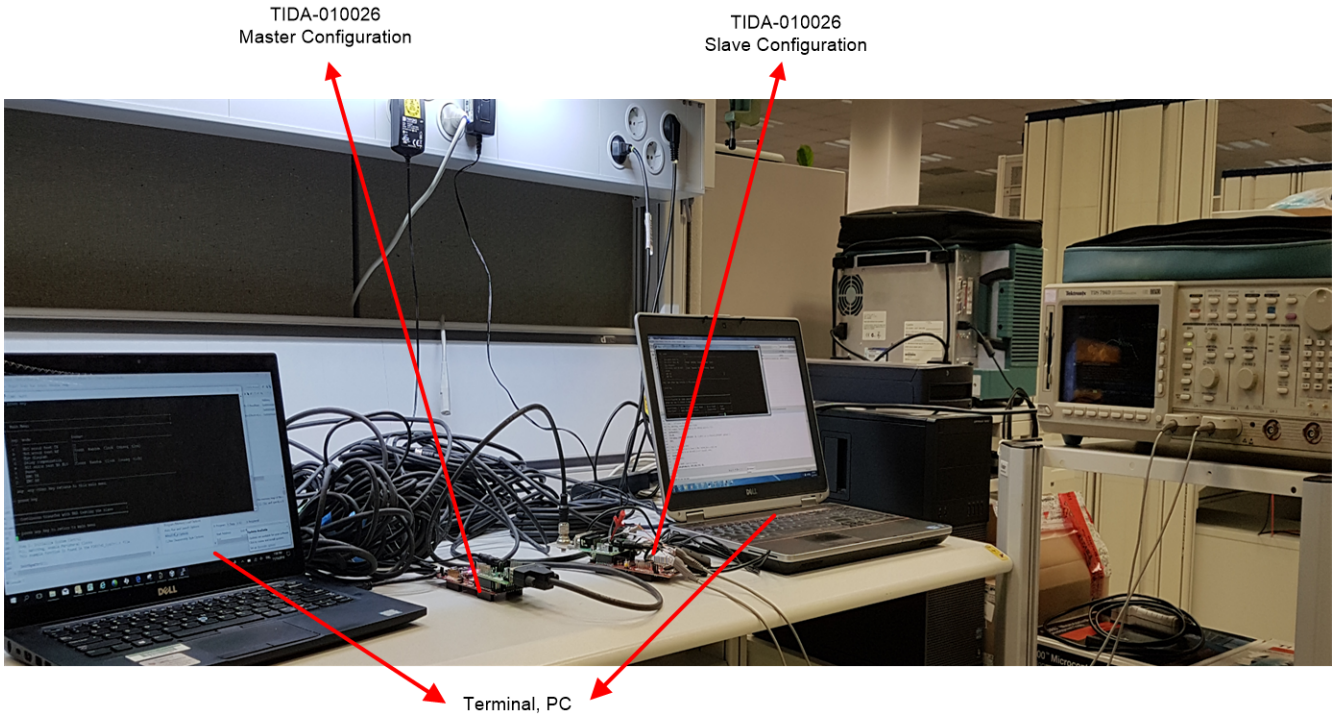
The following equipment is used for the TIDA-010026 testing session:

表 11. Test Equipment for TIDA-010026 Performance Tests

TEST EQUIPMENT	PART NUMBER
High-speed oscilloscope	Tektronix TDS784C
Differential probes	Tektronix P6630
Single-ended probes	Tektronix P6139A
HEIDENHAIN shielded cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1 m	524599-1
C2000 based random pattern generator and bit error analyzer (1–25 MHz) via SPI	Launchxl-f28379d
Thermal camera	Fluke TI40
HEIDENHAIN shielded cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1 m	524599-1
Encoder	ROQ 437, EQN 1337, ROC 425
Multimeter	Fluke 179

For the different tests the equipment used is listed in 表 11. 图 7 shows the test setup used for RS-485 performance tests.

图 7. TIDA-010026 Test Setup for RS-485 Cable Length and Eye Diagram Tests



Per the test section, different setups were used and are described with a diagram in the test section.

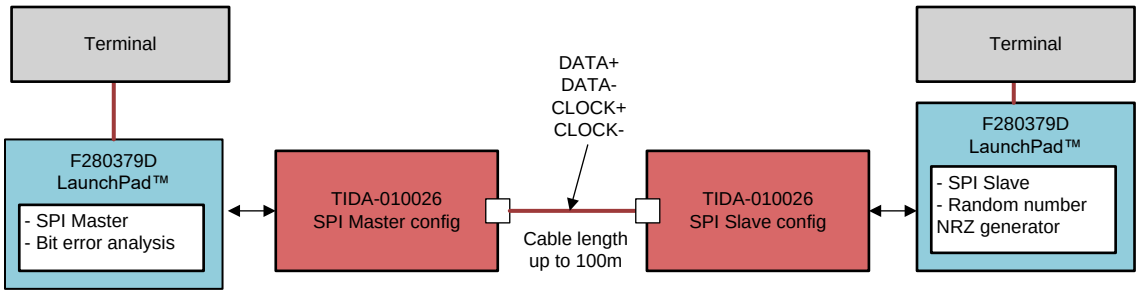
A test was conducted for the individual subsystems like RS-485 and power supply, as well as an application test with EnDat 2.2 position encoders. The RS-485 data and clock transceiver section was tested for maximum error free data rate versus cable length, signal integrity (eye diagram, transceiver propagation delay) and power supply. On the power supply, the following test was conducted power up and down.

The following system tests were conducted testing protection features and different HEIDENHAIN Endat 2.2 position encoders. An Endat 2.2 Master software implementation on TI's C2000 TMS320F28379D was used to conduct the application tests. Finally, we tested the immunity of this design according to IEC61800-3, for IEC61000-4-2 (ESD), IEC61000-4-4 (Fast Transient Burst) and IEC61000-4-5 (Surge).

图 8 shows the functional block diagram of the test setup. The TMS320F28379D MCU is used to implement a high-speed SPI Master (with delay compensation) and another MCU to implement an SPI Slave interface to control and analyze the synchronous data communication through the half-duplex interface. Master and slave were connected through HEIDENHAIN cables (4 × 0.14-mm^2 for RS-485, 4 × 0.34-mm^2 for supply lines) with 1 m, 9 m, 2 × 20 m, and 50 m yielding a total length of 100 m.

The SPI Master was connected to the TIDA-010026. The SPI Master clock was configurable from 1 MHz up to 50 MHz. The SPI Slave was connected to a **modified** version of the TIDA-010026 with only 120-Ω termination and the RS-485 clock transceiver configured in receive mode.

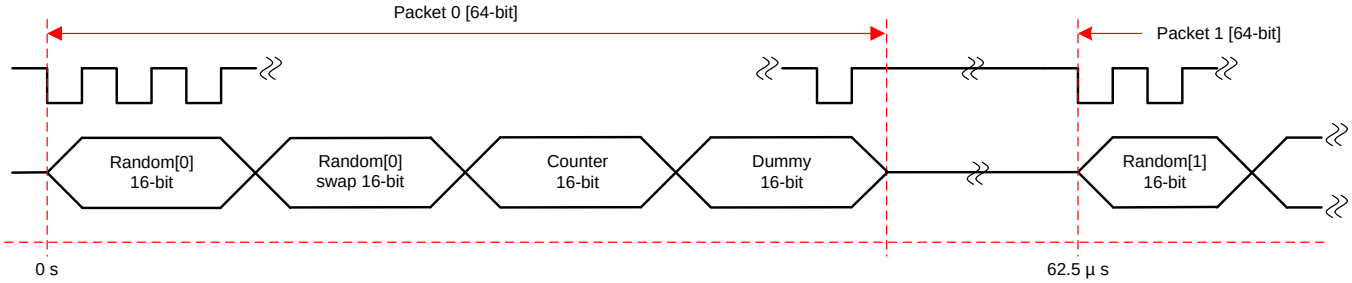
图 8. System Diagram of the Test Setup for TIDA-010026 RS-485 Performance Tests



The data communicated through the RS-485 half-duplex synchronous mode link was generated in software on TMS320F28379D MCU too.

In test mode, "MAXCLOCK", a new data packet was send at a 16-kHz rate. Each packet was 64-bit, with the first 16-bit being the random number, the second word the byte swapped random number, the third word being the packet counter and a dummy byte, as 图 9 shows. The random number was generated using the C function rand(). Test mode "MAXCLOCK" was used for the maximum clock frequency versus cable length. To measure the maximum bit error free data rate (clock rate) on either the received data on slave side or on the received data on master side, the frame counter and the swapped random number where analyzed for bit errors and an error counter was increased accordingly. If only a single error occurred within 60 seconds, the tests failed. This scenario should simulate the inner current control loop (FOC) of a typical servo drive running at 16 kHz, for example, and requesting a new angle position through Endat 2.2. 图 9 shows a diagram of the packet definition.

图 9. Test Pattern Transmitted Over RS-485 Link



In test mode EYEDIAGRAM a 16-bit random number is generated and continuously sent the 16-bit NRZ code at a configurable SPI Master clock from 1–25 MHz. We used the SPI Master clock to trigger the receive data after the end of the cable on the slave side with 120-Ω termination.

3.2.2 Test Results

3.2.2.1 RS-485 Transceiver Performance

3.2.2.1.1 RS-485 Clock Frequencies Versus Cable Length

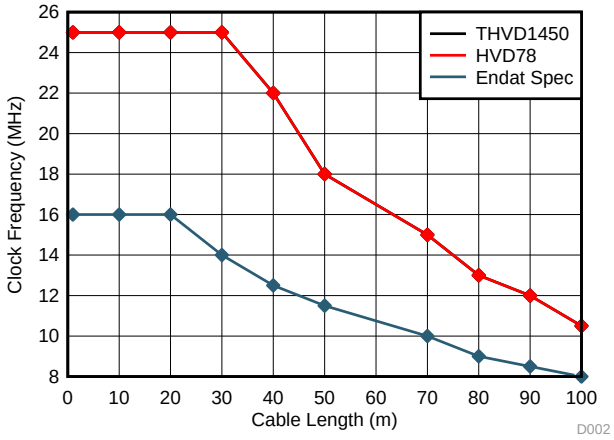
图 10 shows the maximum clock frequency versus cable length. It equals the synchronous data rate in half-duplex mode without any bit errors, as specified previously. This performance can show that the device can support Endat 2.2 specification with different cable lengths up to 100 m.

Remember that the maximum baud rate to which the RS-485 transceiver specified must be twice the Endat 2.2 clock rate, as Endat 2.2 transmits new data at the clock rate. Hence, for a clock rate of 16 MHz, the minimum baud rate needed to be 32 Mbps. The THVD1450 and SN65HVD78 devices are tested. The maximum recommended baud rate for both of them are 50 Mbps; therefore, tests were conducted only up to the respective maximum clock rates, which is 25 MHz for both the THVD1450 and SN65HVD78. Data was shifted out on the master side on the falling clock edge.

图 10 compares the maximum clock rates with zero bit error of the RS-485 transceivers in the THVD1450 versus the SN65HVD78 in the default configuration with a bypass capacitor at the differential outputs to GND. According to the real application, the results are measured at the master receiver. See 3.2 节 for the test setup.

From the result, with a cable length up to 100 m, the THVD1450 device has the same performance with the SN65HVD78 device. Both of them have an enough margin when compared to the Endat 2.2 specification.

图 10. Maximum Clock Frequencies vs Cable Length With Zero Bit Error for THVD1450 or SN65HVD78 at Master Receiver

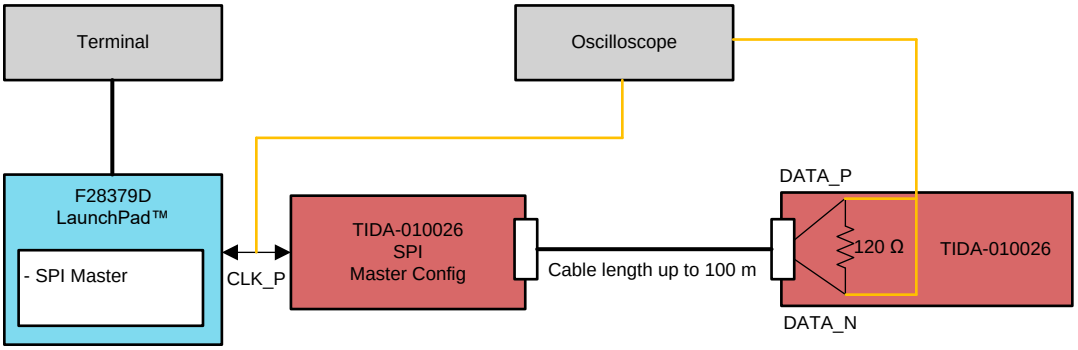


3.2.2.1.2 RS-485 Eye Diagram Versus Cable Length

Eye diagrams provide a quick and accurate way to visually analyze and evaluate the quality of a transmitted signal. The device under test was the master transceiver. The following pictures show the eye diagrams using random NRZ data measured differentially with 120-Ω termination at the cable end (slave receive side) with a differential Tektronix probe. The master transmitter clock rate was connected to channel 1 of the scope to trigger sampling of the differential data at the far cable end. 图 11 shows the setup block diagram.

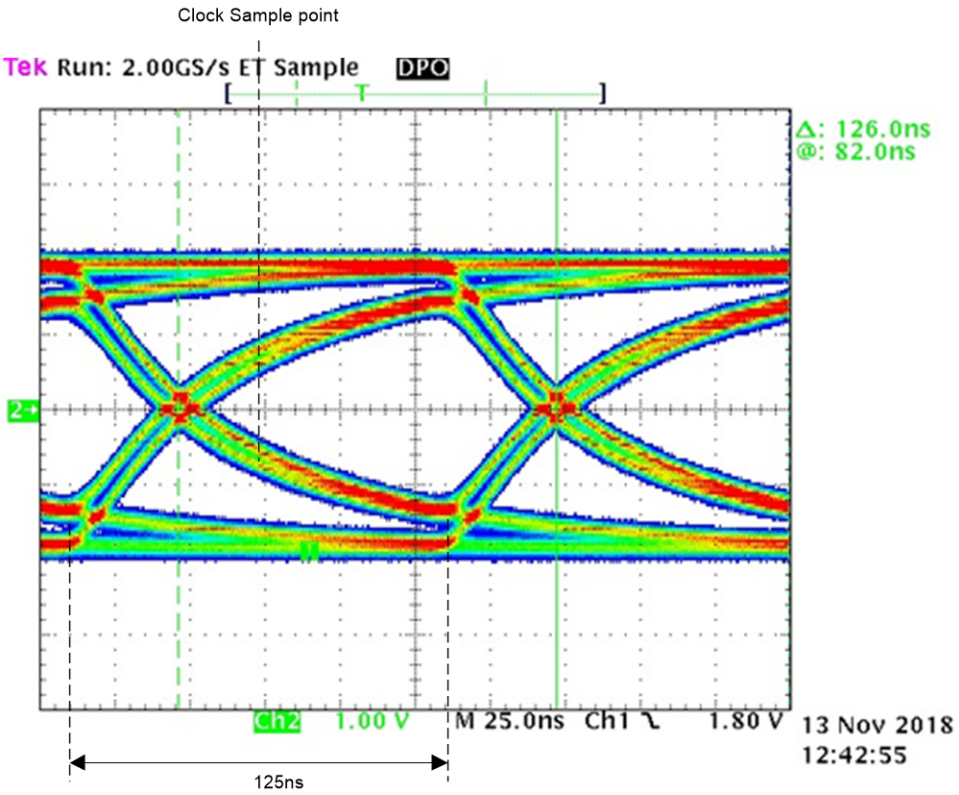
Measurements were conducted at cable length 100 m and 20 m with maximum data rate as specified per Endat 2.2 for the THVD1450 device with bypass capacitors on the master differential clock and data outputs.

图 11. Block Diagram of Test Setup Used for Eye Diagram Tests



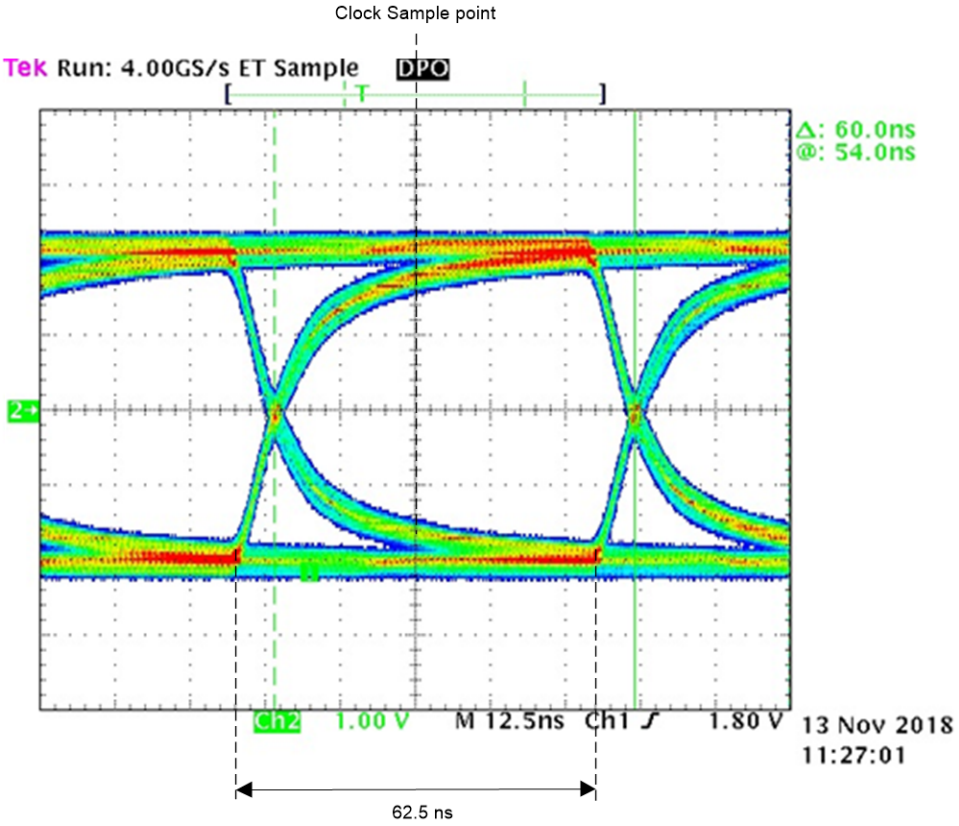
The clear eye diagrams shown in 图 12 and 图 13 show that the device can ensure a high quality of transmitted signal.

图 12. Eye Diagram THVD1450, 100-m Cable, 8-MHz Data Rate



The jitter of the received differential data at the 100-m cable far end with 120-Ω termination at the maximum EnDat 2.2. clock frequency is around 10% (0.9 UI-open), the steady state differential voltage is around ±1.8 V (3.6 Vpp). However, the rise or fall time from 10% to 90% is exactly one clock cycle (see 图 12). Taking into account that the receive data is sampled at the falling clock edge (in the 'middle' of the clock cycle) the effective worst-case differential voltage is around ±0.8 V.

图 13. Eye Diagram THVD1450, 20-m Cable, 16-MHz Data Rate



The jitter of the received differential data at the 100-m cable far end with 120-Ω termination at the maximum EnDat 2.2. clock frequency is around 10% (0.9 UI-open), the steady state differential voltage is around ±1.8 V (3.6 Vpp). However the rise or fall time from 10% to 90% is exactly one clock cycle (see 图 13). Taking into account that the receive data is sampled at the falling clock edge (in the 'middle' of the clock cycle), the effective worst-case differential voltage is around ±1.6 V.

3.2.2.1.3 RS-485 Transceiver Propagation Delay

Another aspect to look at is the RS-485 driver and receiver propagation delay especially to the configuration where no delay compensation is implemented. See the red curve in 图 2. The maximum frequency without delay compensation is 2 MHz. Therefore, the hardware must not contribute to more than 250 ns (border condition). The critical delay is the delay between the master clock and the receive data at the master. The following blocks contribute to this delay:

- EnDat Master serial port (transmit, receive)
- If added: buffer, level shifter (transmit, receive)
- RS-485 master (driver, receiver)
- Cable (two-times the length) typically 5 ns/m in one direction
- Encoder (slave receive to transmit delay, including RS-485)

With respect to the master implementation on TIDA-10026: 图 14 shows the rise- and fall-time propagation delay of the SN74LVC2T device level shifter and THVD1450 RS-485 with 120-Ω termination at driver and receiver. It is measured from logic input to differential output for the driver and vice versa for the receiver. The driver propagation delay measured is around 15 ns, the receiver propagation delay is around 36 ns. The RS-485 master transceiver only contributes to 51 ns to the overall loop delay, which is well below the critical threshold for the configuration without delay compensation.

图 14. Block Diagram of Test Setup Used for TIDA-10026 System Transmit Propagation Delay

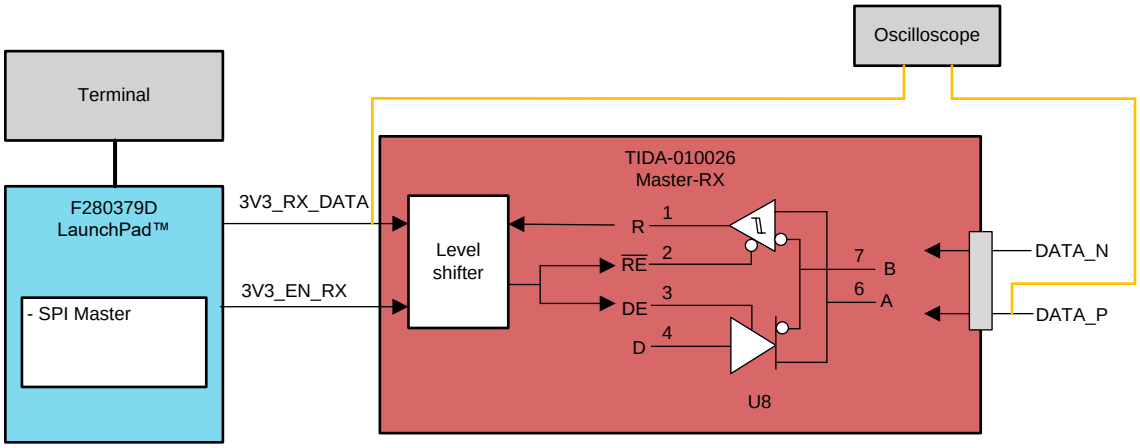
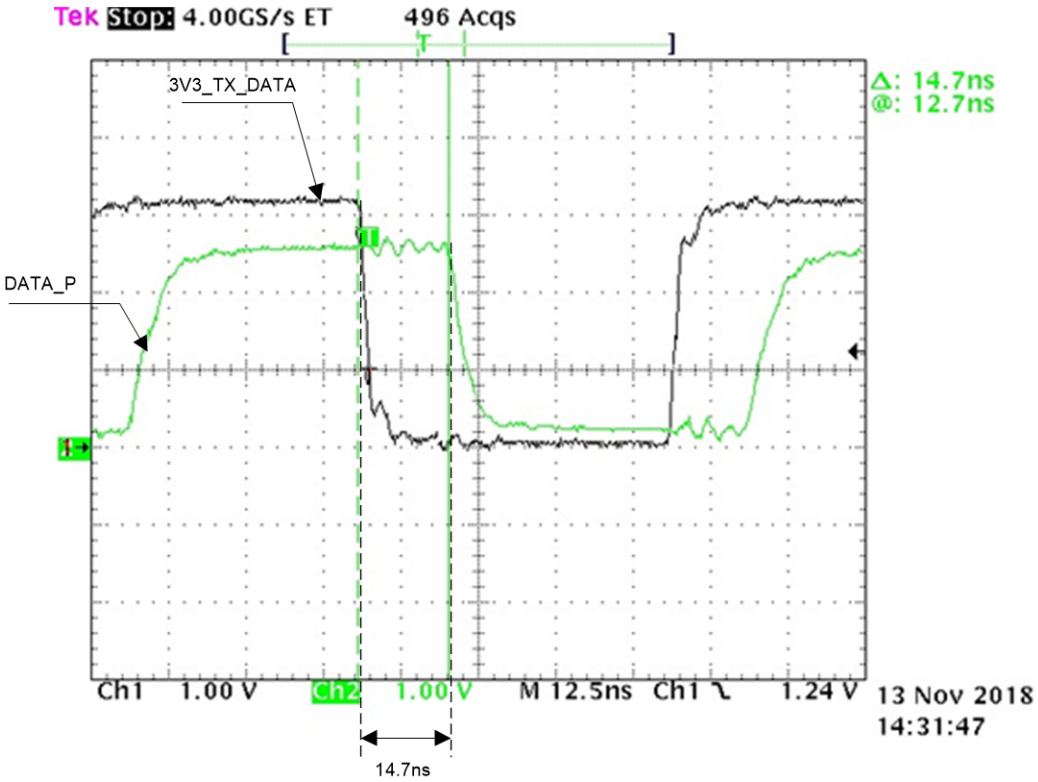


图 15. TIDA-10026 System Transmit Propagation Delay



The propagation delay of the THVD1450 is within the specification of the device. The maximum delay of the driver, transmitter is 20 ns.

图 16. Block Diagram of Test Setup Used for TIDA-10026 System Receive Propagation Delay

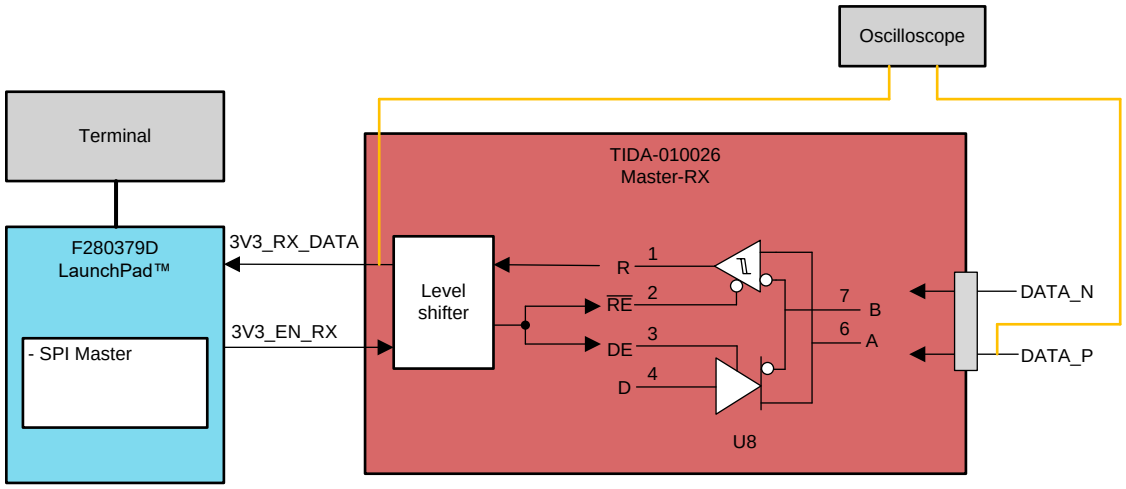
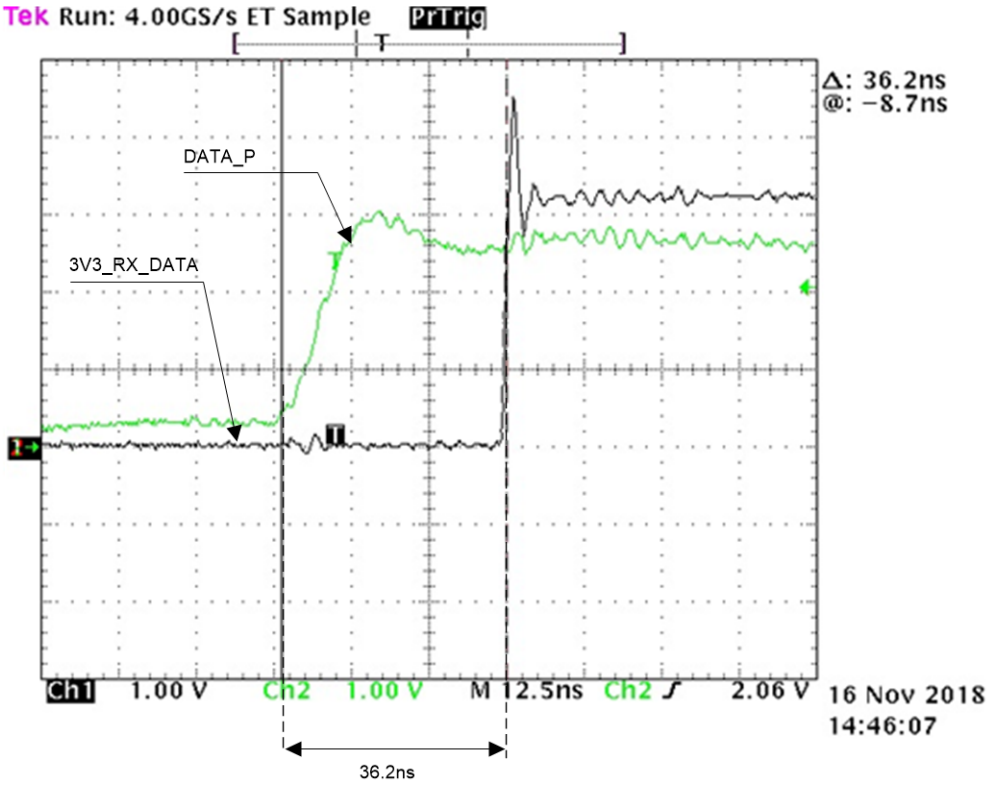
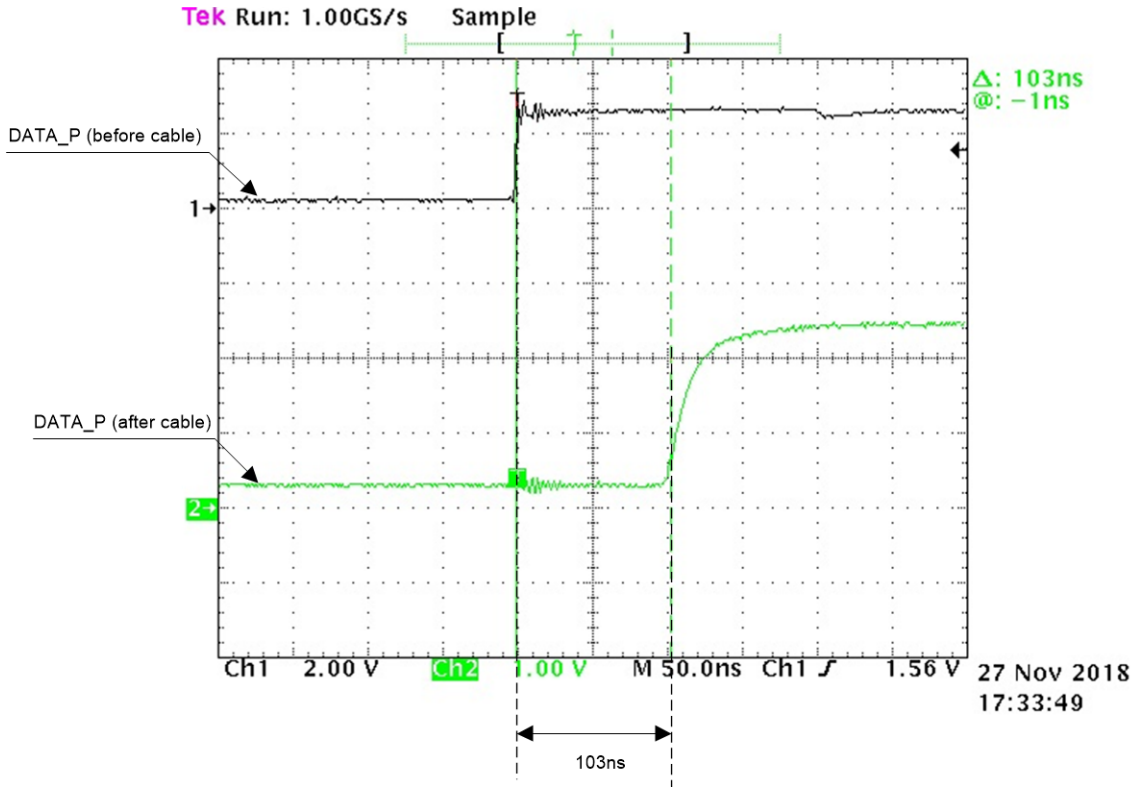


图 17. TIDA-10026 System Receive Propagation Delay



The propagation delay of the THVD1450 is within the specification of the device. The maximum delay of the receiver is 40 ns.

图 18. Propagation Delay Through 20-m Cable



To know the cable delay through the HEIDENHAIN cable, the differential transmit signal was measured at the start and end of the cable. 表 12 and 图 18 show the results of this measurement.

表 12. System Propagation Delay (One Direction)

CABLE LENGTH	PROPAGATION DELAY THROUGH HEIDENHAIN CABLE	TOTAL PROPAGATION DELAY THROUGH BOARD AND CABLE	BOARD DELAY IN % OF TOTAL DELAY
21 m	103 ns	154 ns	Approximately 33%
100 m	502 ns	553 ns	Approximately 10%

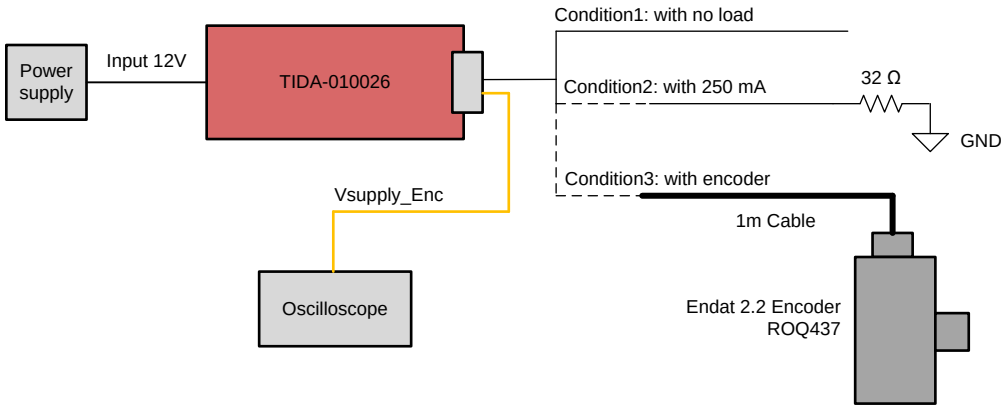
The cable propagation delay for 21 m and 100 m are dominant versus the RS-485 transceiver and level shifter. For an 8-MHz clock frequency the entire loop delay will be approximately 1.1 µs. At 8-MHz clock, this equals 9 clock periods, or, in other words the data is delayed by 9-bits at the master receiver side. This is not taking into account the electronics delay of the Encoder.

3.2.2.2 Power Supply Performance

3.2.2.2.1 Start-up and Shutdown

According to the schematics, by connecting J6.1 and J6.2 while connecting J3.18 with J4.9, both the C2000 LaunchPad and enable pin for Vsupply_Enc are powered by U7. According to 表 3, the minimum operating voltage for Endat running is 3.6 V. Referring to the schematic, the results are measured at “Vsupply_Enc” and “3v3”.

图 19. Block Diagram of Test Setup Used for Output Ripple Performance Test



From 图 20 and 图 21, the start-up time of the output voltage at the encoder connector is around 46 ms, while the shut-down time is around 100 ms. It can also be seen that the Encoder stops working at 3.4 V which is below the EnDat 2.2 specification. See 6 节 for details on the EnDat 2.2 specification

图 20. Power Rail Startup Sequence

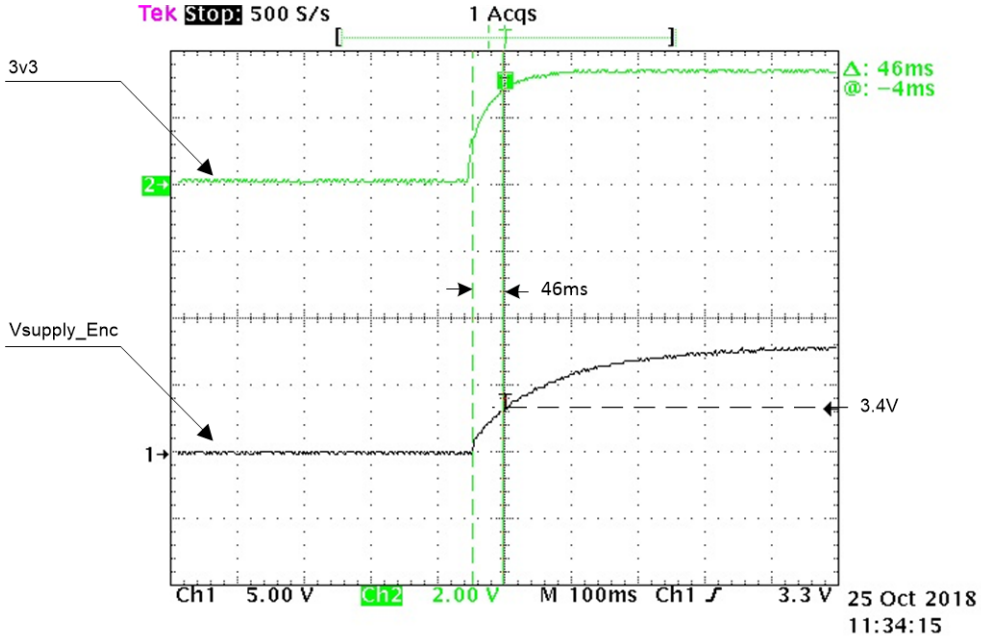
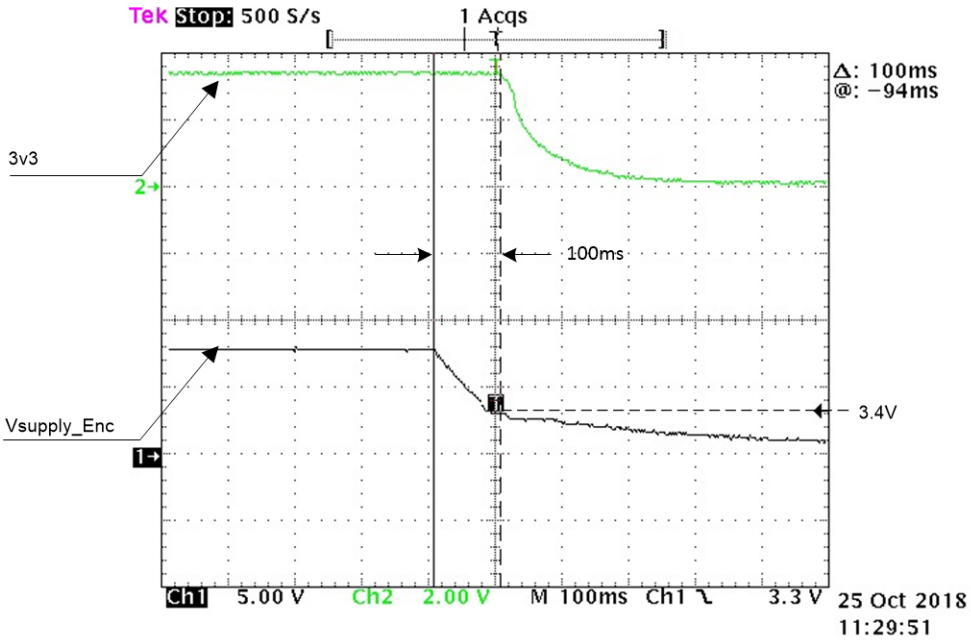


图 21. Power Rail Shutdown Sequence



3.2.2.2.2 Encoder Voltage Output Ripple

图 22 shows the block diagram of the test setup for power-supply performance. According to 表 3, the requirement for the output ripple is to have less than 100 mVpp of ripple on the output voltage. 图 23 to 图 25 show that the power supply meets this requirement with different loads. According to the encoder data sheet (ROQ 437, HEIDENHAIN), the current consumption of the encoder without load is 105 mA. The output voltage is measured at Vsupply_Enc.

图 22. Block Diagram of Test Setup Used for Output Ripple Performance Test

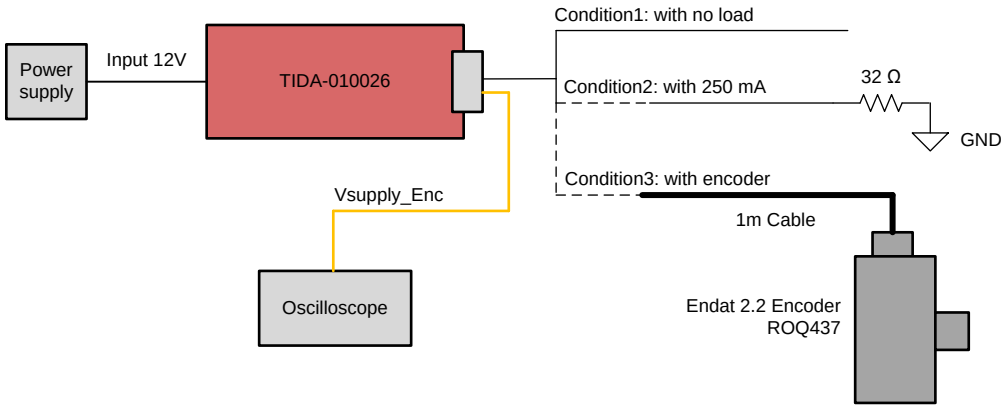


图 23. Encoder Voltage Output Ripple Performance With no Load (Condition 1)

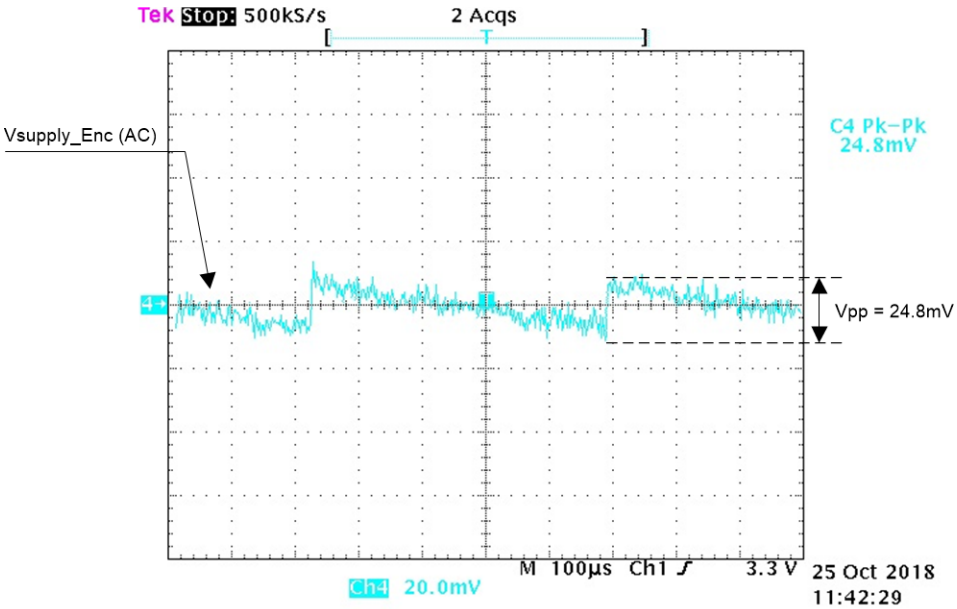


图 24. Encoder Voltage Output Ripple Performance With 250-mA Load (Condition 2)

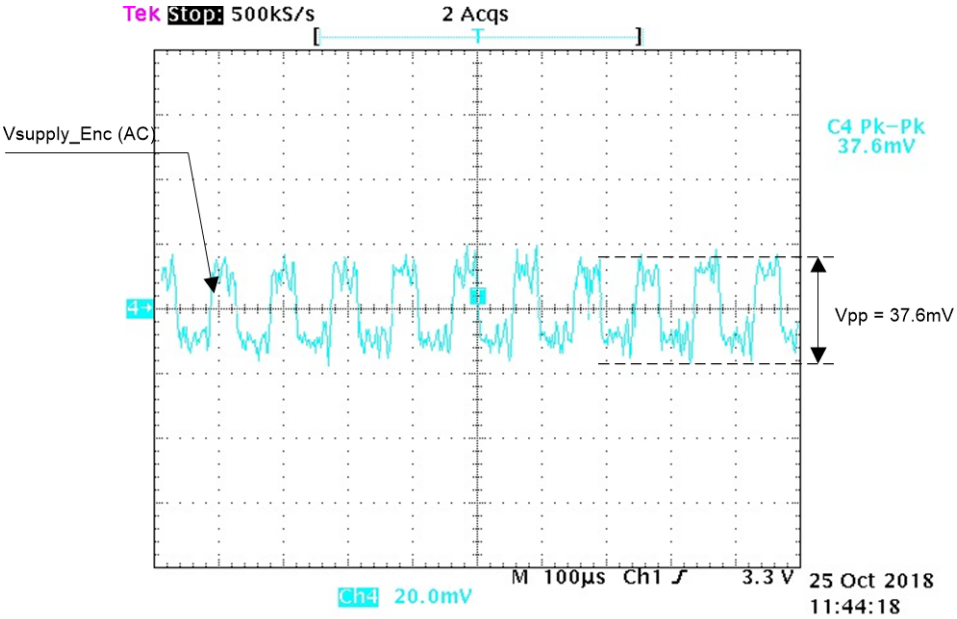
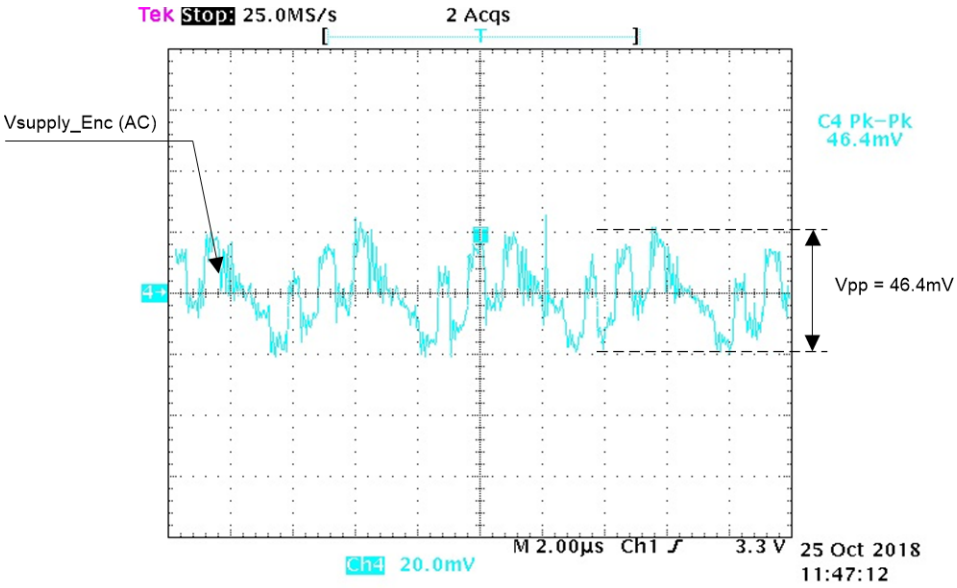


图 25. Encoder Voltage Output Ripple Performance With Encoder (Condition 3)



3.2.2.2.3 Short-Circuit Protection on Encoder Power Supply

To protect the drive short-circuit protection is built into the encoder power supply. This section is testing this protection under different load conditions.

图 26 shows 3 different load conditions and the measured signals:

- Condition 1: short circuit during startup
- Condition 2: sudden short circuit during normal operation
- Condition 3: Hot plug of an Encoder during normal operation

图 26. Block Diagram of Test Setup Used for Short-Circuit Protection Test

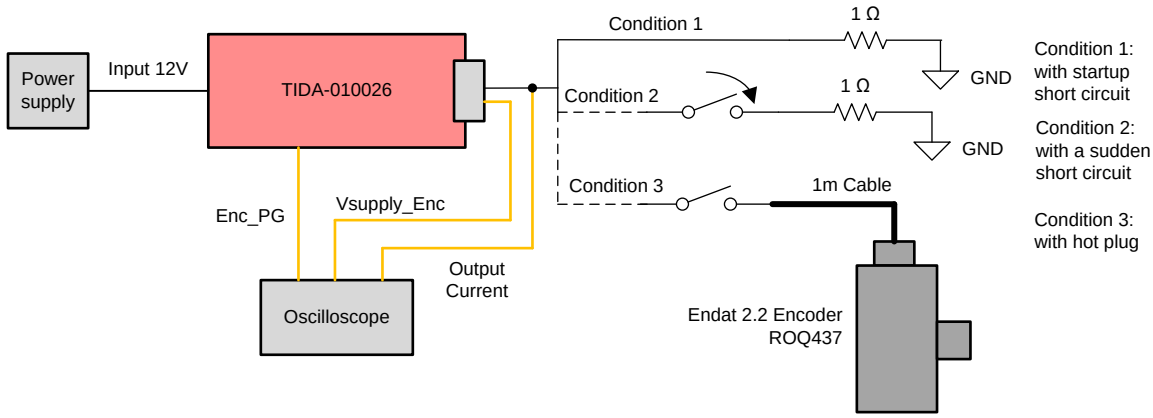


图 27 shows that during startup, the Encoder supply never starts to pull current as the short circuit is detected. The Host processor can read the ENC_PG and detect the short circuit. Thereafter, the host processor can turn off the power supply.

图 27. Encoder Supply With Start-up Short-Circuit Option 1

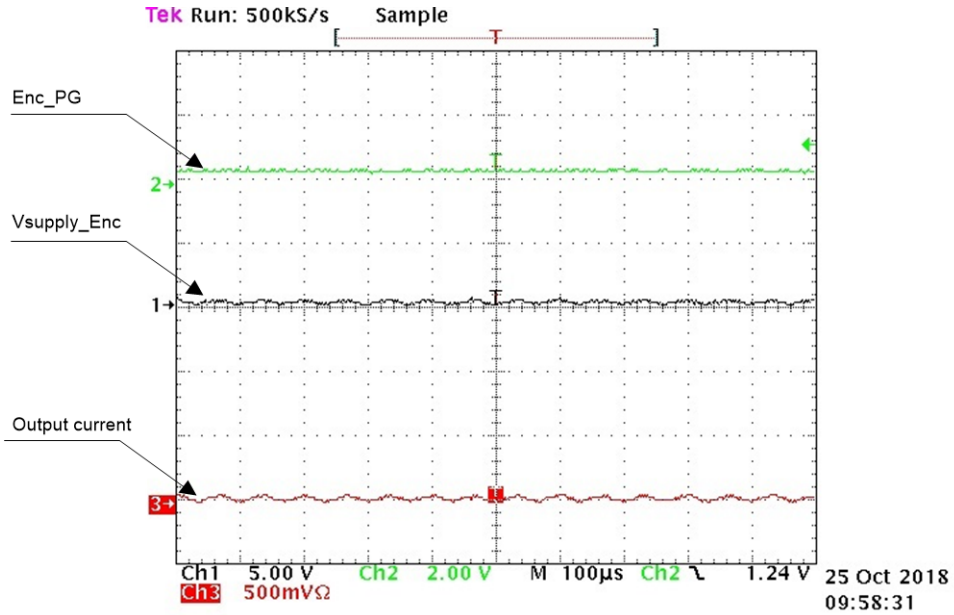


图 28 shows that the power supply detects the short circuit and turns off the power supply, after current have discharged the power supply will continue trying to start up again, with the short circuit still there the power supply stays off.

图 28. Encoder Supply With a Sudden Short-Circuit Option 2

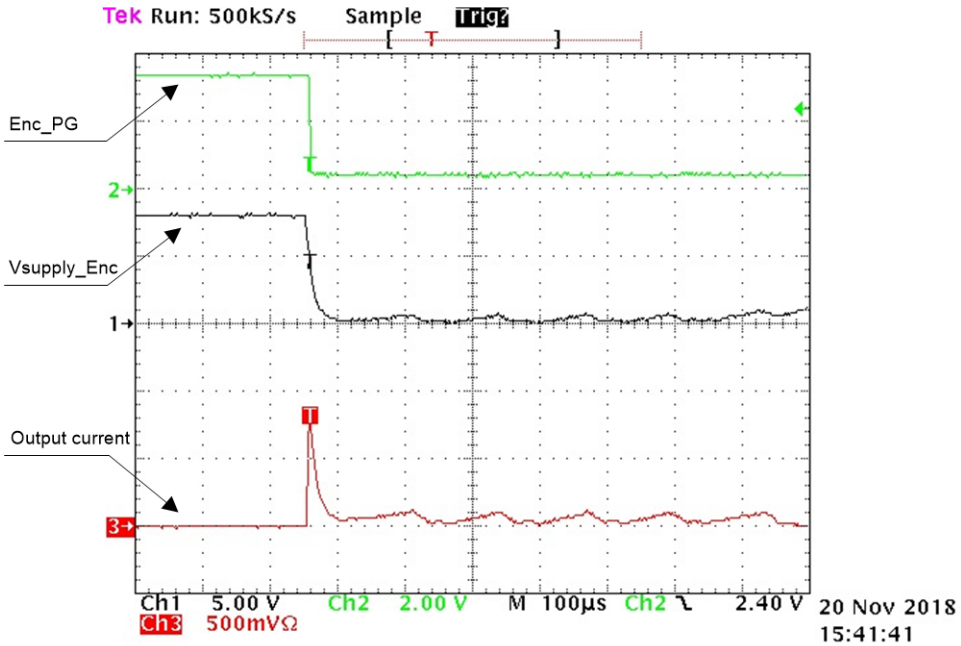
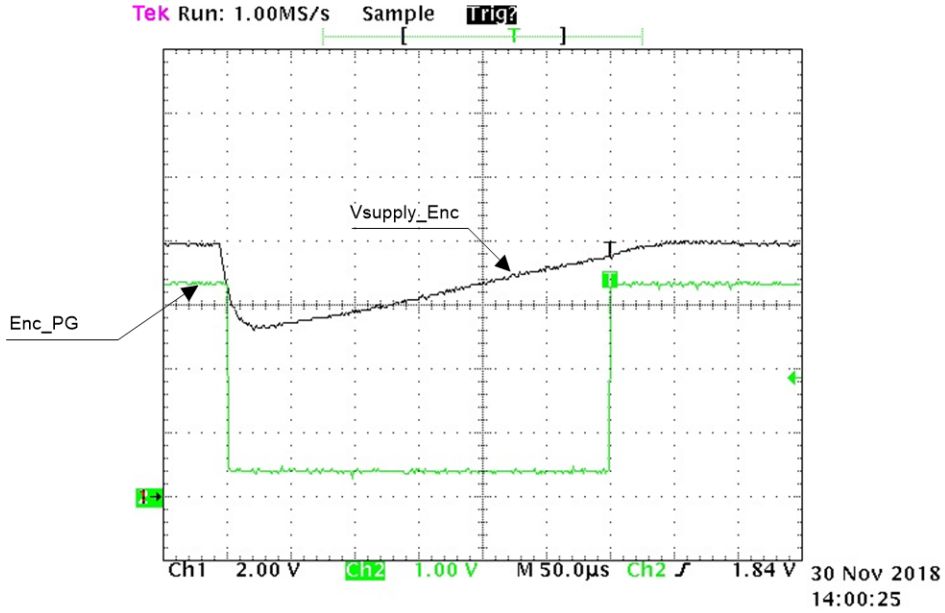


图 29 shows that the power supply detects the inrush current needed to supply the encoder, after the initial inrush current is done the power supply detects again that the encoder voltage is back in normal operation. This is detected using the host processor and the system can detect the hot plug of the Encoder.

图 29. Encoder Supply Showing Hot-Plug Capability Option 3



3.2.2.2.4 Current Consumption of RS-485

图 30 shows the test setup for current consumption, compared to the previous test, the C2000 LaunchPad is required. In this case, disconnect J3.18 with J4.9 and the enable signal is given by the C2000. For measuring the current consumption, the two resistors between power supply and RS-485 are replaced by two multimeters. In idle mode, both of two RS-485 devices are disabled; when Endat 2.2 is running, one of RS-485 transmits clock signal all the way while another one transmits data signal occasionally. Add the two current values from multimeters to get the total current consumption. 表 13 shows the results.

图 30. Block Diagram of Test Setup Used for Current Consumption

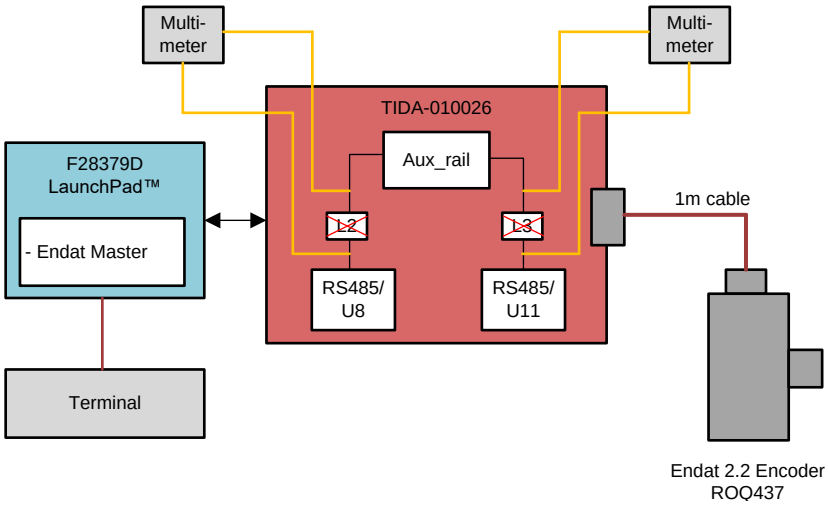


表 13. Current Consumption of RS-485

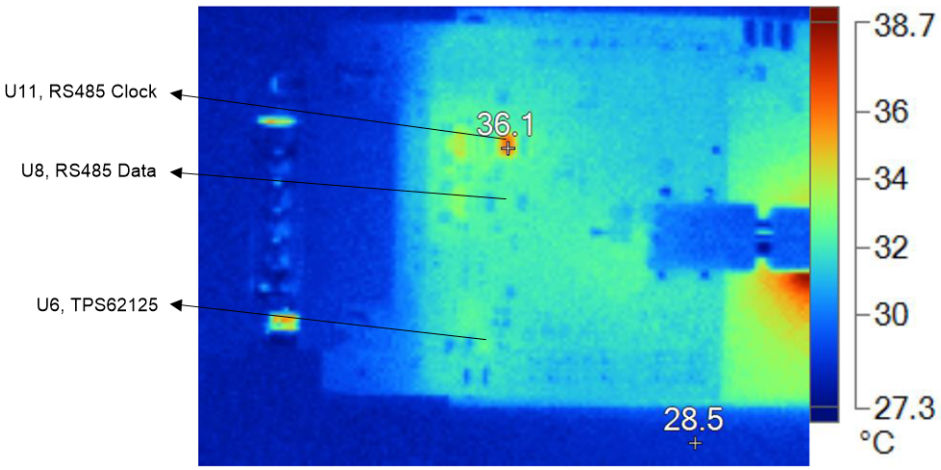
TASK	RS-485 FOR DATA, U8	RS-485 FOR CLOCK, U11	RS-485 TOTAL
Idle (TX disabled, RX enabled)	0.61 mA	0.61 mA	1.22 mA
Endat at 8.33 MHz	2.27 mA	41.45 mA	43.72 mA

The power consumption is measured with the reference design running an Endat 2.2 encoder at a 8.33-MHz clock frequency with a 16-kHz update rate.

3.2.2.2.5 Thermal Image

As a result of the efficiency seen previously, the board does not heat up much. This is the thermal image taken at 28.5°C room temperature, with an input of 15 V and an output of 8 V with encoder. The hottest point on TIDA-010026 is the THVD1450 device which transmits the clock signal all the time. The hottest temperature is 36°C, 7.5°C higher than the ambient temperature.

图 31. TIDA-010026 Thermal Image While Running Endat 2.2



3.2.2.3 System Performance

3.2.2.3.1 Test Setup

The LaunchPad-F28379D was used to perform system tests with the TIDA-010026 analog interface with an Endat 2.2 position encoder. This includes an Endat 2.2 Master implementation which was set to a 8.33-MHz Endat 2.2 clock rate and a 16-kHz repetition rate.

图 32. Test Setup for TIDA-010026 Test With Endat 2.2 Encoders

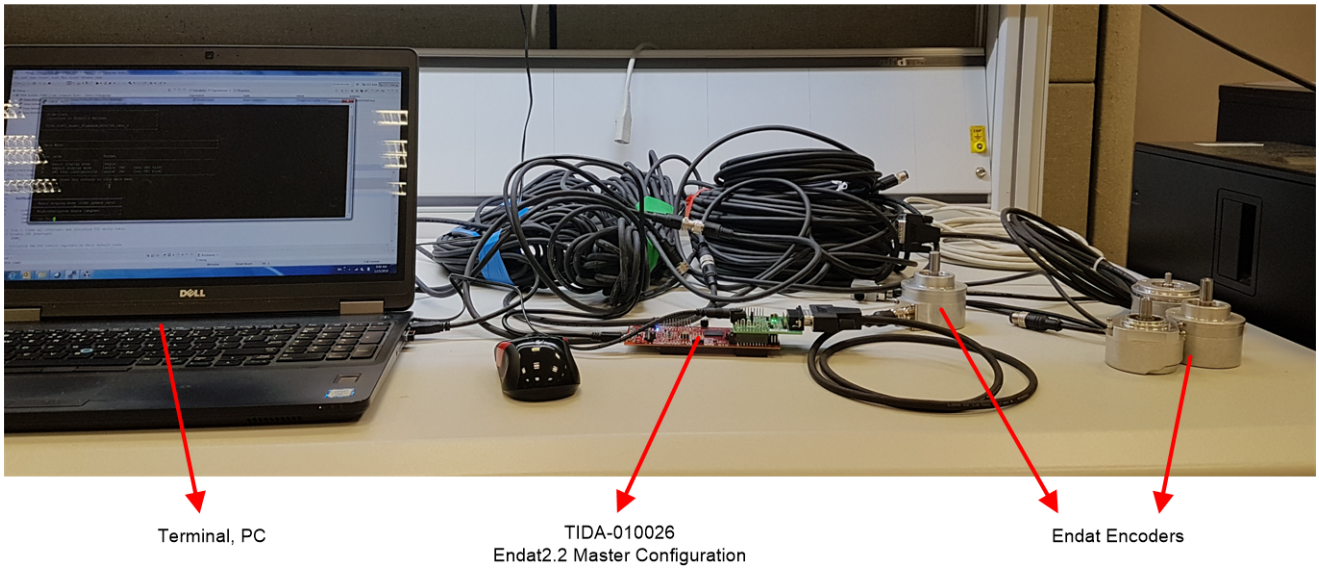


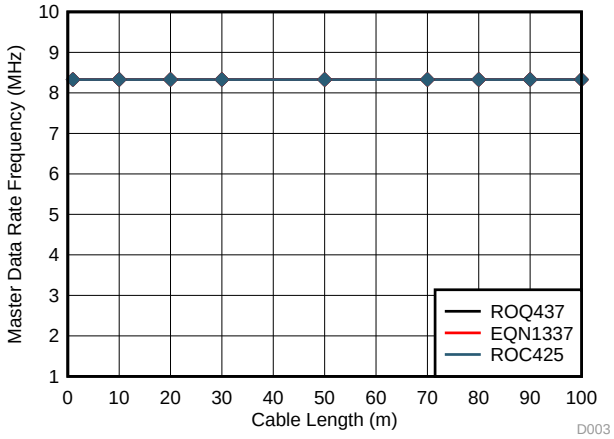
表 14. System Test Equipment

TEST EQUIPMENT	PART NUMBER
HEIDENHAIN EnDat 2.2 position encoders	ROQ 437, ROQ 1035, ROC 425
HEIDENHAIN shielded EnDat cables, PUR (4 × 0.14 mm^2, 4 × 0.34 mm^2), 10, 20 m, 20 m, 50 m	368330-xx, xx = cable length
HEIDENHAIN M12/Sub-D15 male adapter cable 1 m	524599-1
EnDat 2.2 Master (TI software from Position Manager)	Launchxl-f28379d
Endat 2.2 analog hardware	TIDA-010026

3.2.2.3.2 Endat 2.2 Cable Length Tests

Measurements were taken with the four previously-listed HEIDENHAIN EnDat 2.2 encoders to verify error-free communication at a maximum 8.33-MHz clock rate, which was the maximum specified clock frequency of these position encoders.

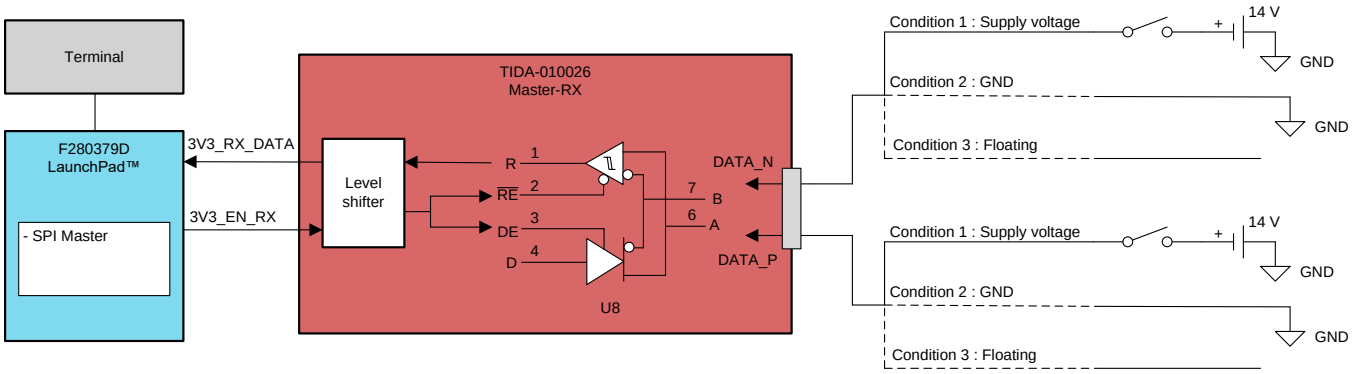
图 33. Cable Length Versus Master Clock Frequency With EnDat 2.2 Encoders With Zero CRC Errors



注: The 8.33-MHz frequency of the Endat 2.2 master clock is a limit of the LaunchPad used, this can be changed to 8.00 MHz, changing the default crystal frequency of the LaunchPad.

3.2.2.3.3 Miswiring Fault on the RS-485 Transceiver

图 34. Block Diagram of Test Setup Used for Miss Wiring



This test is conducted to test the THVD1450 device in a miss wire condition. This can happen during installation of the Encoder to the Encoder interface of the drive. For Endat 2.2 as the specification of the Encoder voltage is from 3.6 V to 14 V. The THVD1450 device is tested with a 14-V external signal on the A and B pins. After the voltage is applied to the pin, the Endat 2.2 protocol is tested on the TIDA-010026, if it is working.

表 15. Miswiring Test Results

A INPUT	B INPUT	Endat 2.2 RUNNING AFTERWARDS
Floating	14 V	Yes
14 V	Floating	Yes
GND	14 V	Yes
14 V	GND	Yes

With this test it is seen that the THVD1450 device can function after a miss wire of up to 14 V, which correlates with the data sheet – there the common mode of the A and B pin is a maximum ±18 V.

3.2.2.3.4 Hot-Plug Test of an Endat 2.2 Encoder

This system test is documented in 节 3.2.2.2.3 of the design guide.

3.2.2.4 EMC Test Results

The TIDA-010026 TI design is for tested for IEC61000-4-2, 4-4 and 4-5 (ESD, EFT and Surge) with test levels and performance criterion specified in the standard IEC 61800-3 “EMC immunity requirements and specific test methods applicable in adjustable speed, electrical-power drive systems”.

The design is compliant to these standards and exceeds the voltage requirements according to IEC61800-3 EMC immunity requirements. 表 16 and 表 17 show a summary, with more details in the following sections. The performance criterion A is often customer-specific and the expected accuracy depends on the system requirements.

表 16. IEC618000-3 EMC Immunity Test Results Summary

REQUIREMENTS					TIDA-010026 MEASUREMENTS		
PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION	LEVEL	PERFORMANCE (ACHIEVED) CRITERION	TEST
Port for process measurement control lines	Electrostatic Discharge (ESD)	IEC61000-4-2	±4 kV CD or 8 kV AD, if CD not possible	B	±8 kV CD	B	PASS (EXCEED)
Port for process measurement control lines	Fast transient Burst (EFT)	IEC61000-4-4	±2 kV / 5 kHz or 100 kHz, capacitive clamp	B	±4 kV	B	PASS (EXCEED)
Port for process measurement control lines	Surge	IEC61000-4-5	±1 kV; since shielded cable > 20 m, direct coupling to shield (2 Ω, 500 A)	B	±2 kV	A	PASS (EXCEED)

The performance (acceptance) criterion is defined, as follows:

表 17. Performance Criterion Definitions

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module continues to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module continues to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module continues to operate as intended automatically, after manual restart, or power off, or power on.

For all tests, an Endat 2.2 Master software was used to transmit an Endat 2.2 get angle command with a 16-kHz repetition. This means 1920000 packets transmitted during the 2 minutes of the test, with this value the Packet Error Rate is calculated.

3.2.2.4.1 EFT Immunity Applied on the Signal Ports

On the test for the signal port, the test was done using the Encoder as slave as seen with both image and diagram of the test setup in 图 35 and 图 36.

图 35. TIDA-010026 Test Setup for EFT Immunity Tests Using Encoder

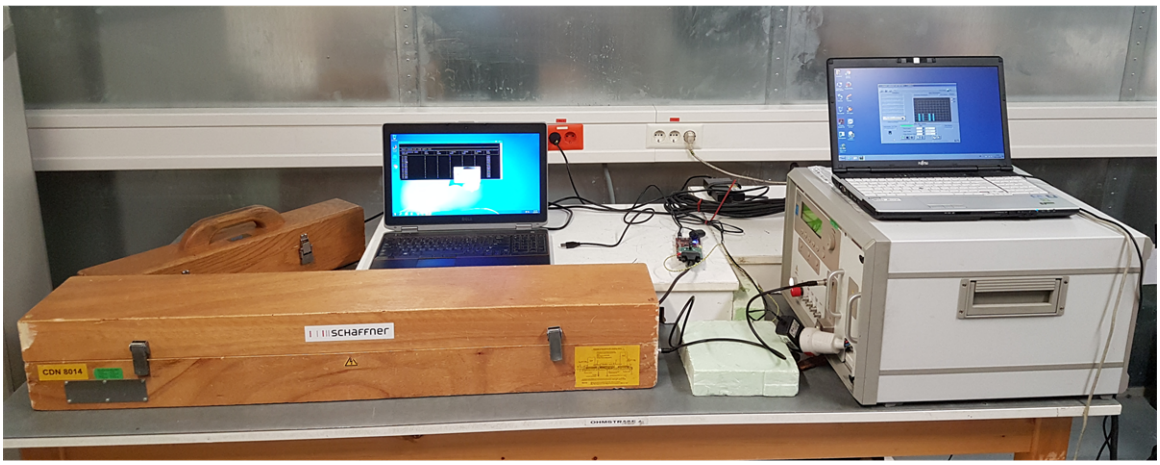
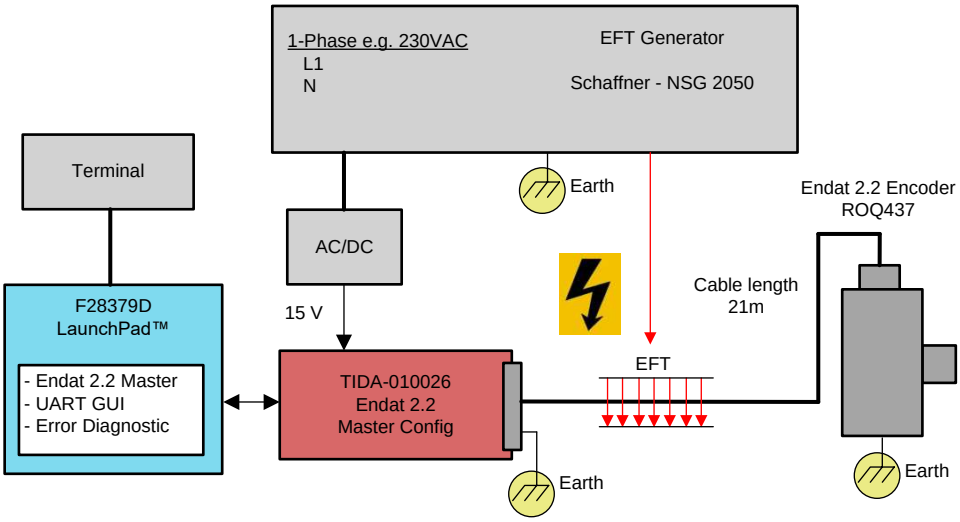


图 36. TIDA-010026 Diagram of Test Setup for EMC Immunity Tests on the Signal Port Using an Encoder



One issue of doing this test is that the encoder is a black box with an unknown RS-485 transceiver, this transceiver can influence the performance of the of the DuT. Several tests were committed with different considerations testing the RS-485 transceiver performance.

图 37 and 图 38 show the performance of the THVD1450 device compared to the other transceivers, the Earth (1 nF and 10 MΩ), and capacitive termination (330 pF).

图 37. TIDA-010026 Test Result of the EFT at 5-kHz Test With RS-485 Transceivers

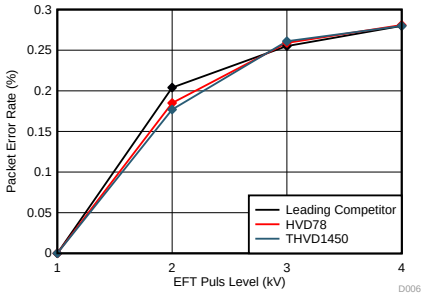
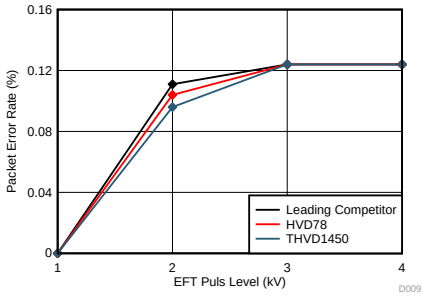


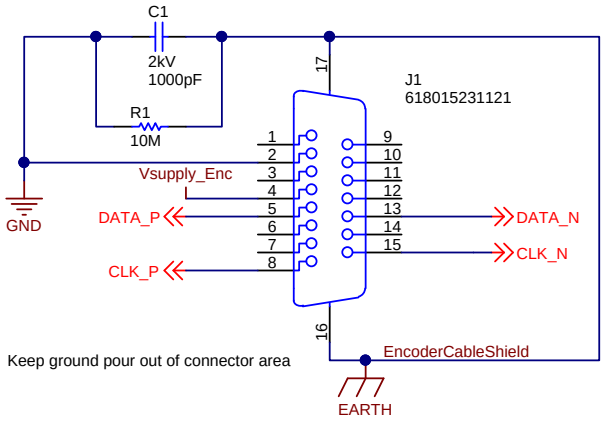
图 38. TIDA-010026 Test Result of the EFT at 100-kHz Test With RS-485 Transceivers



Note that the THVD1450 device performs slightly better than other high-immunity RS-485 transceivers from completion and TI at standard levels.

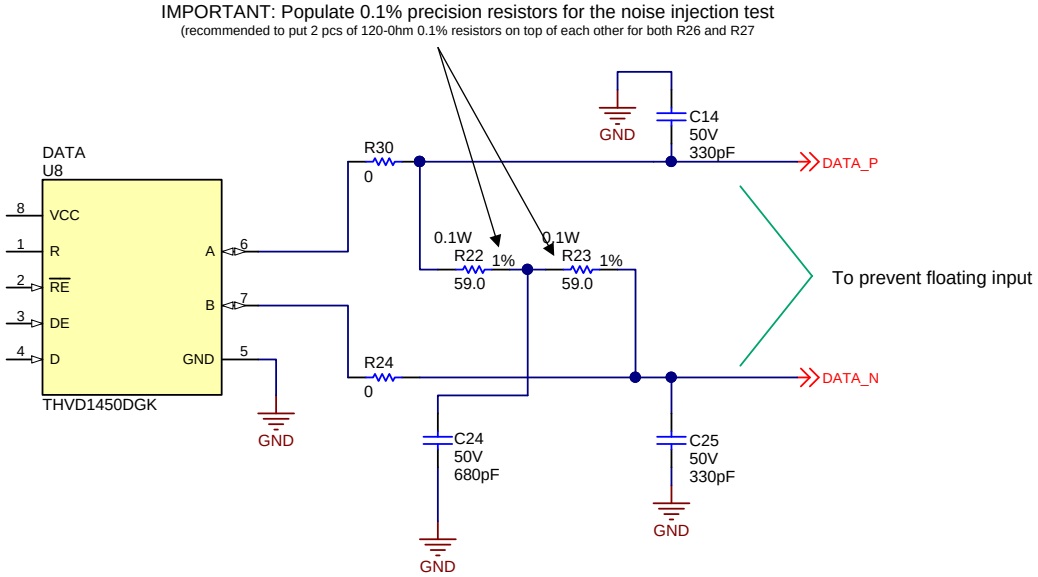
图 39 shows the EARTH connection and the capacitive termination influence of the system.

图 39. TIDA-010026 Schematic of Logic GND to Earth Decoupling



The termination test shows that if a capacitive termination of the differential signals can improve the signal integrity, 图 40 shows a schematic of the different options of signals.

图 40. TIDA-010026 Schematic of Data Transceiver Circuit



The termination capacitors are C15 or C16, and C14.

The earth connection test shows if a resistive, capacitive connection between earth and digital ground improves the signal integrity.

图 41. TIDA-010026 Test Result of the EFT at 5-kHz Test With Different Earth Connections

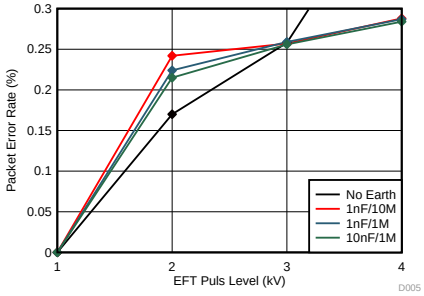
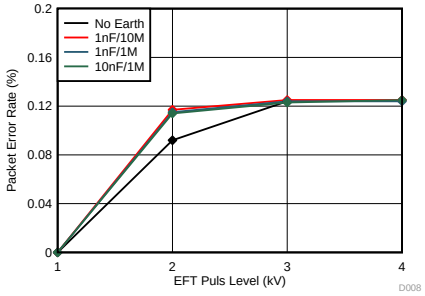


图 42. TIDA-010026 Test Result of the EFT at 100-kHz Test With Different Earth Connections



In 图 41 and 图 42 the earth connection was tested with different resistor and capacitor values, as soon as 4 kV was applied, the earth connection improves the signals significantly. The *No Earth* termination has a packet error rate of 0.47% at 5-kHz EFT and 26.90% at 100-kHz EFT.

These results show that depending on what frequency is injected, the choice of earth connection can be different.

图 43. TIDA-010026 Test Result of the EFT at 5-kHz Test With Different Capacitive Termination

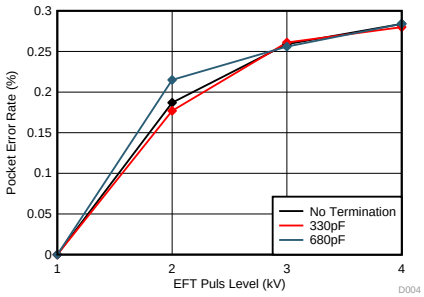
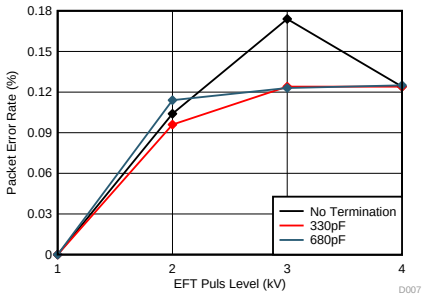


图 44. TIDA-010026 Test Result of the EFT at 100-kHz Test With Different Capacitive Termination



These results show that there is not a significant change in the results, still showing that the 330-pF termination is best.

3.2.2.4.2 Surge Immunity Applied on the Signal Ports

On the test for the signal port, the test was done using the Encoder as slave as 图 45 and 图 46 show.

图 45. TIDA-010026 Test Setup for Surge Immunity Tests Using Encoder

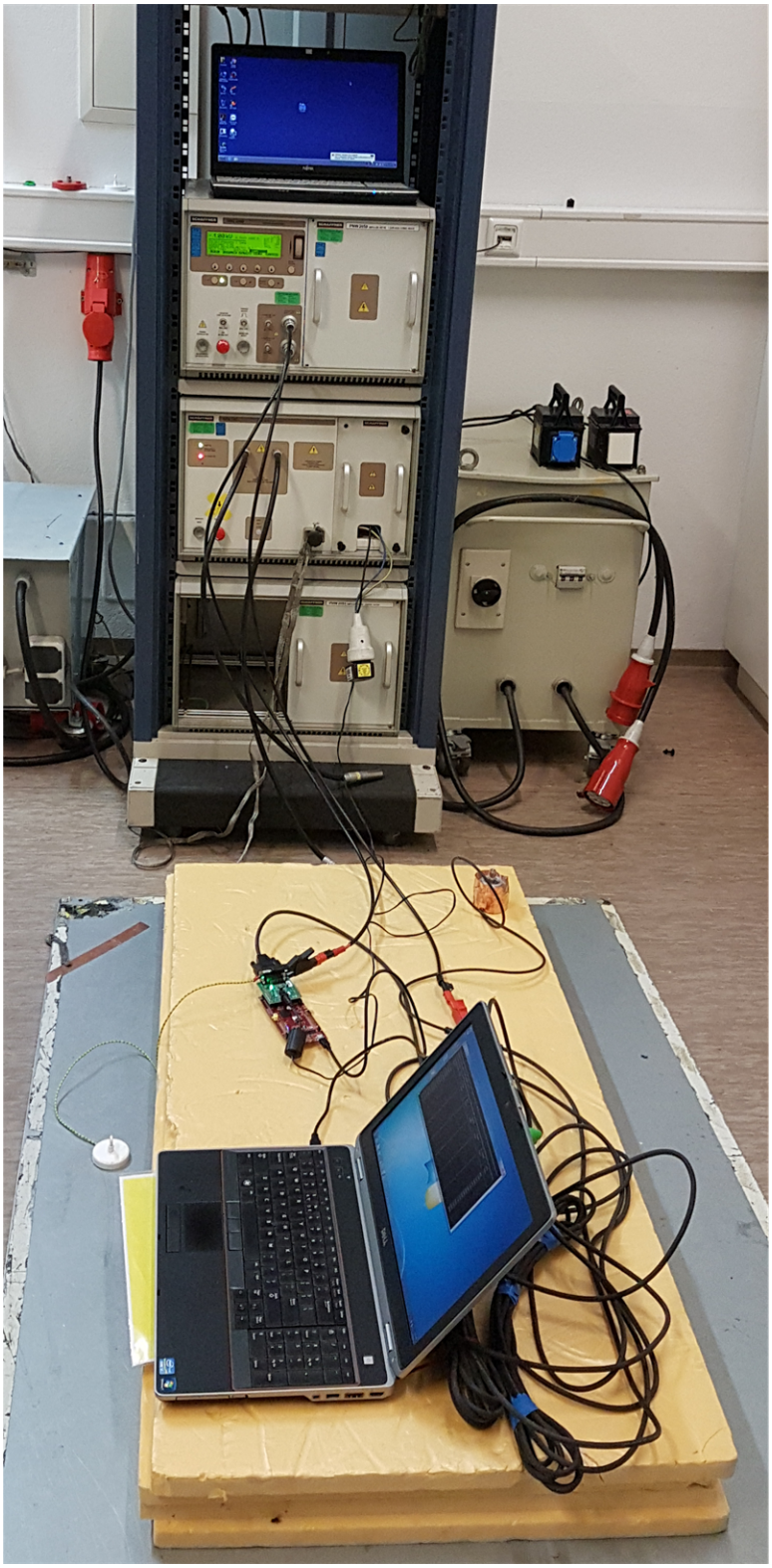


图 46. TIDA-010026 Diagram of Test Setup for Surge Immunity Tests on the Signal Port

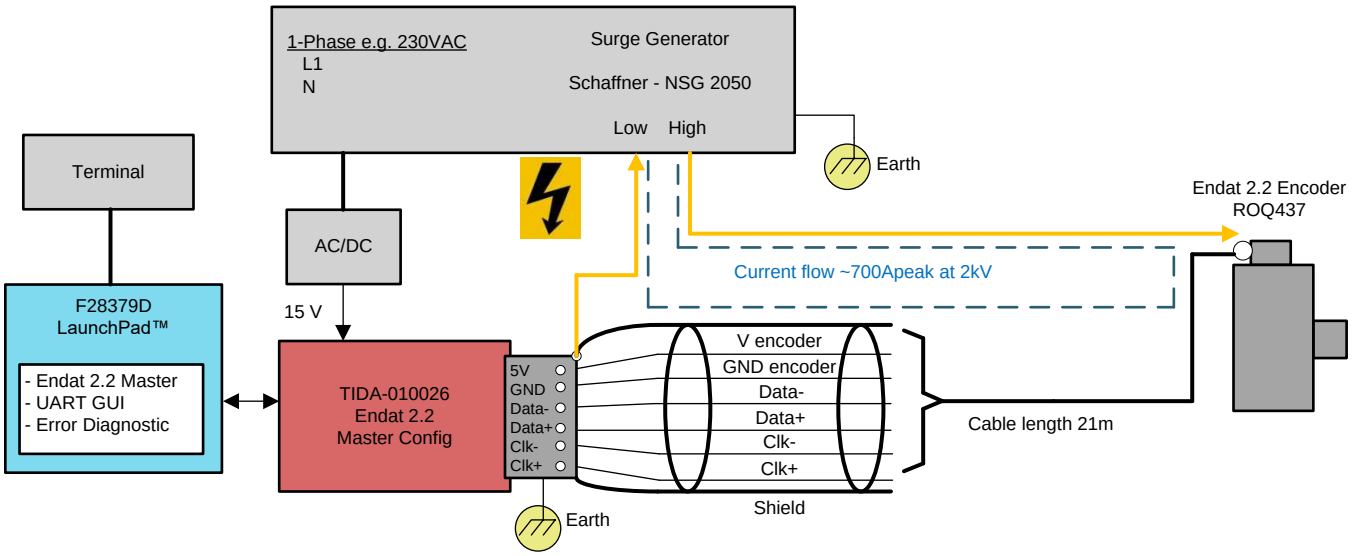


表 18 shows the results for the Surge test on the power port.

表 18. TIDA-010026 Test Result of the Surge Test

REQUIREMENTS					TIDA-010026 MEASUREMENTS		
PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION	LEVEL	PERFORMANCE (ACHIEVED) CRITERION	TEST
Port for process measurement control lines	Surge	IEC61000-4-5	±1 kV; since shielded cable > 20 m, direct coupling to shield (2 Ω, 500 A)	B	±0.5 kV	A	PASS (EXCEED)
Port for process measurement control lines	Surge	IEC61000-4-5	±1 kV; since shielded cable > 20 m, direct coupling to shield (2 Ω, 500 A)	B	±1 kV	A	PASS (EXCEED)
Port for process measurement control lines	Surge	IEC61000-4-5	±1 kV; since shielded cable > 20 m, direct coupling to shield (2 Ω, 500 A)	B	±2 kV	A	PASS (EXCEED)

This test shows that the THVD1450 exceeds the IEC61000-4-5 specification.

3.2.2.4.3 ESD Immunity Applied on the Signal Ports

The signal port test was done using the Encoder as slave, as 图 47 and 图 48 show.

图 47. TIDA-010026 Diagram of Test Setup for ESD Immunity Tests on the Signal Port

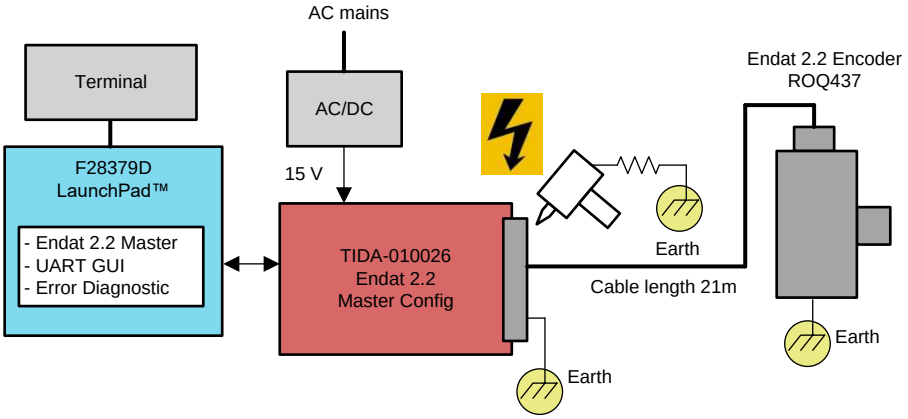


图 48. TIDA-010026 Test Setup for ESD Immunity Tests Using Encoder

This testing used the data communication from the master to the slave.

The results in 表 19 were achieved for the ESD test on the power port.

表 19. TIDA-010026 Test Result of the ESD Test

REQUIREMENTS					TIDA-010026 MEASUREMENTS		
PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION	LEVEL	PERFORMANCE (ACHIEVED) CRITERION	TEST
Port for process measurement control lines	Electrostatic Discharge (ESD)	IEC61000-4-2	± 4-kV CD or ± 8-kV AD, if CD not possible	B	±4 kV CD	B	PASS (EXCEED)
Port for process measurement control lines	Electrostatic Discharge (ESD)	IEC61000-4-2	± 4-kV CD or ± 8-kV AD, if CD not possible	B	±8 kV CD	B	PASS (EXCEED)

This test shows that the THVD1450 exceeds the IEC61000-4-2 specification.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010026.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010026.

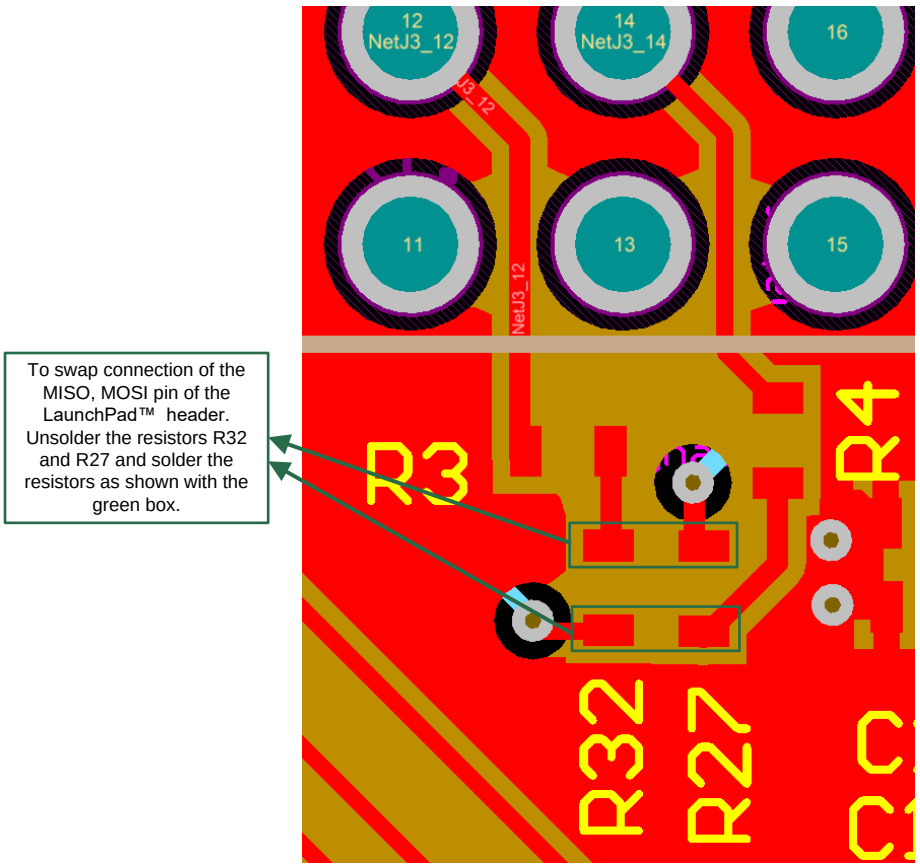
4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010026.

4.3.2 Layout Guidelines

图 49. How to Change Direction of MISO, MOSI Signal to the LaunchPad™ Pins



4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010026.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010026.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010026.

5 Software Files

To download the software files, see the design files at ControlSuite.

6 Related Documentation

1. HEIDENHAIN, *EnDat 2.2 – Bidirectional Interface for Position Encoders*
2. Texas Instruments, *C2000™ Position manager EnDat22 library module user's guide*
3. Texas Instruments, *Reference design for an interface to a position encoder with EnDat 2.2 design guide*
4. Texas Instruments, *Universal digital interface to absolute position encoders reference design*
5. Texas Instruments, *EnDat 2.2 system reference design*

6.1 商标

6.2 Third-Party Products Disclaimer

7 Terminology

EFT— Electrical Fast Transient

ESD— ElectroStatic Discharge

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