

MAXWELL CUSTOMER PROCESSOR BOARD

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REV	E4
VER	1.0

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	3rd JUN 2019	Drafted from "PROC062E3_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	26th JUN 2019	Updated REV E4 schematic as per change list document.	Mistral Design Team	AJIT MB	AJIT MB
0.3	28th JUN 2019	Updated test automation power section and LCD adpater board load switch.	Mistral Design Team	AJIT MB	AJIT MB
0.4	3rd JUL 2019	Updated variants	Mistral Design Team	AJIT MB	AJIT MB
0.5	13rd AUG 2019	Updated VDD_CORE regulator section	Mistral Design Team	AJIT MB	AJIT MB
0.6	22 AUG 2019	Updated VDD_1V0 and VDD_DLL section	Mistral Design Team	AJIT MB	AJIT MB
1.0	28 AUG 2019	Baselined			

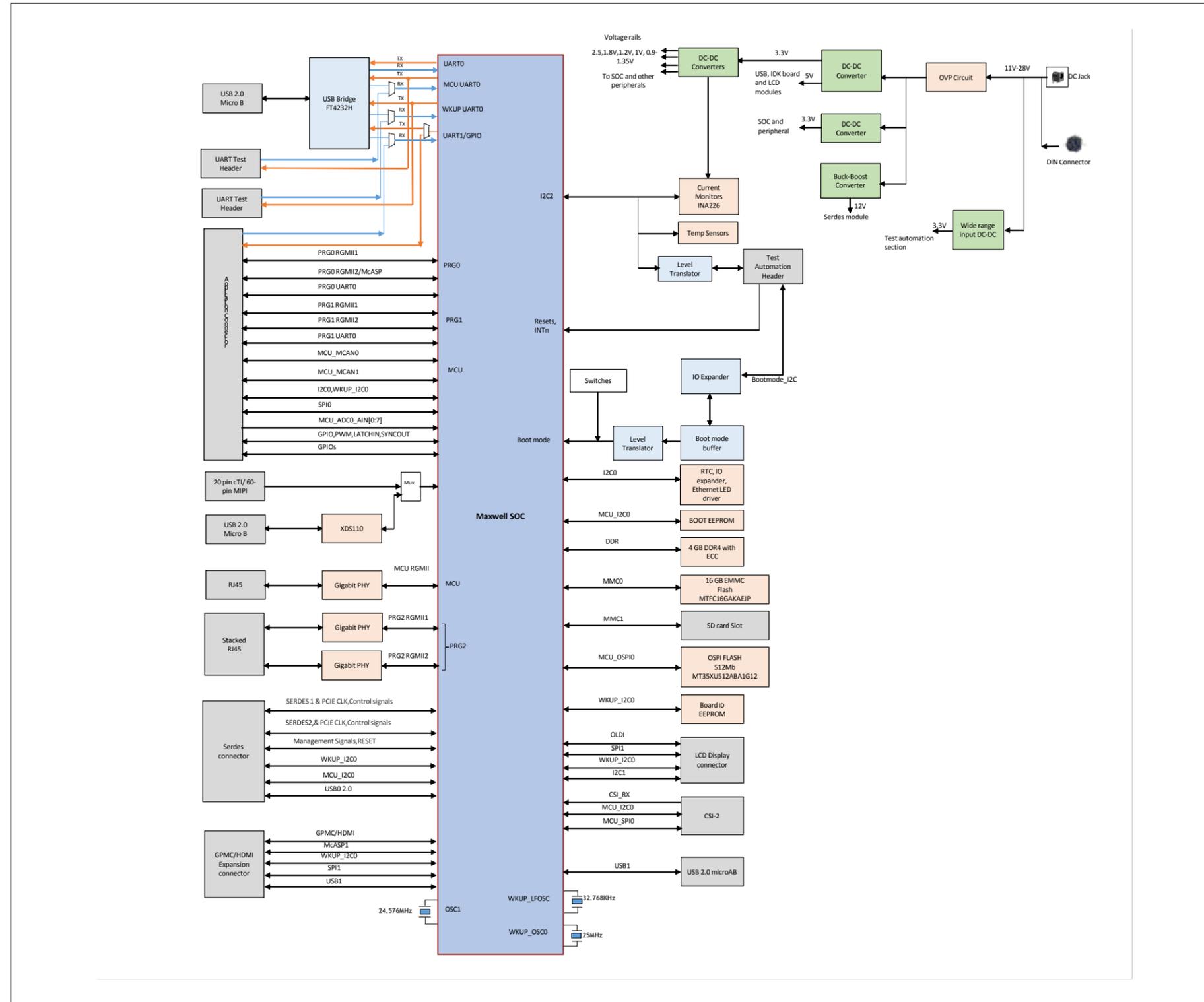
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Title REVISION HISTORY

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 2 of 44

BLOCK DIAGRAM_CP BOARD



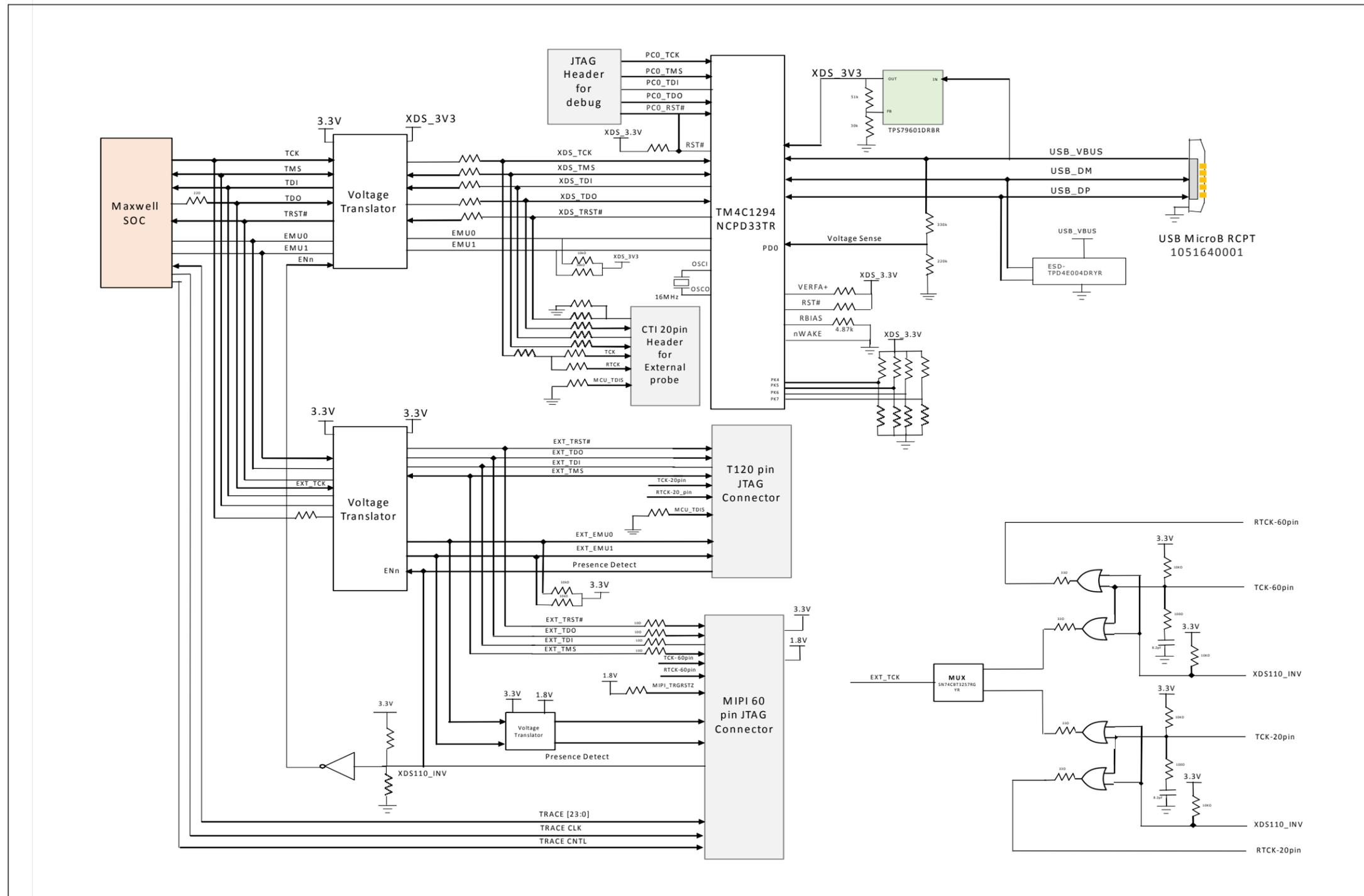
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Title BLOCK DIAGRAM_CP BOARD

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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BLOCK DIAGRAM_XDS110

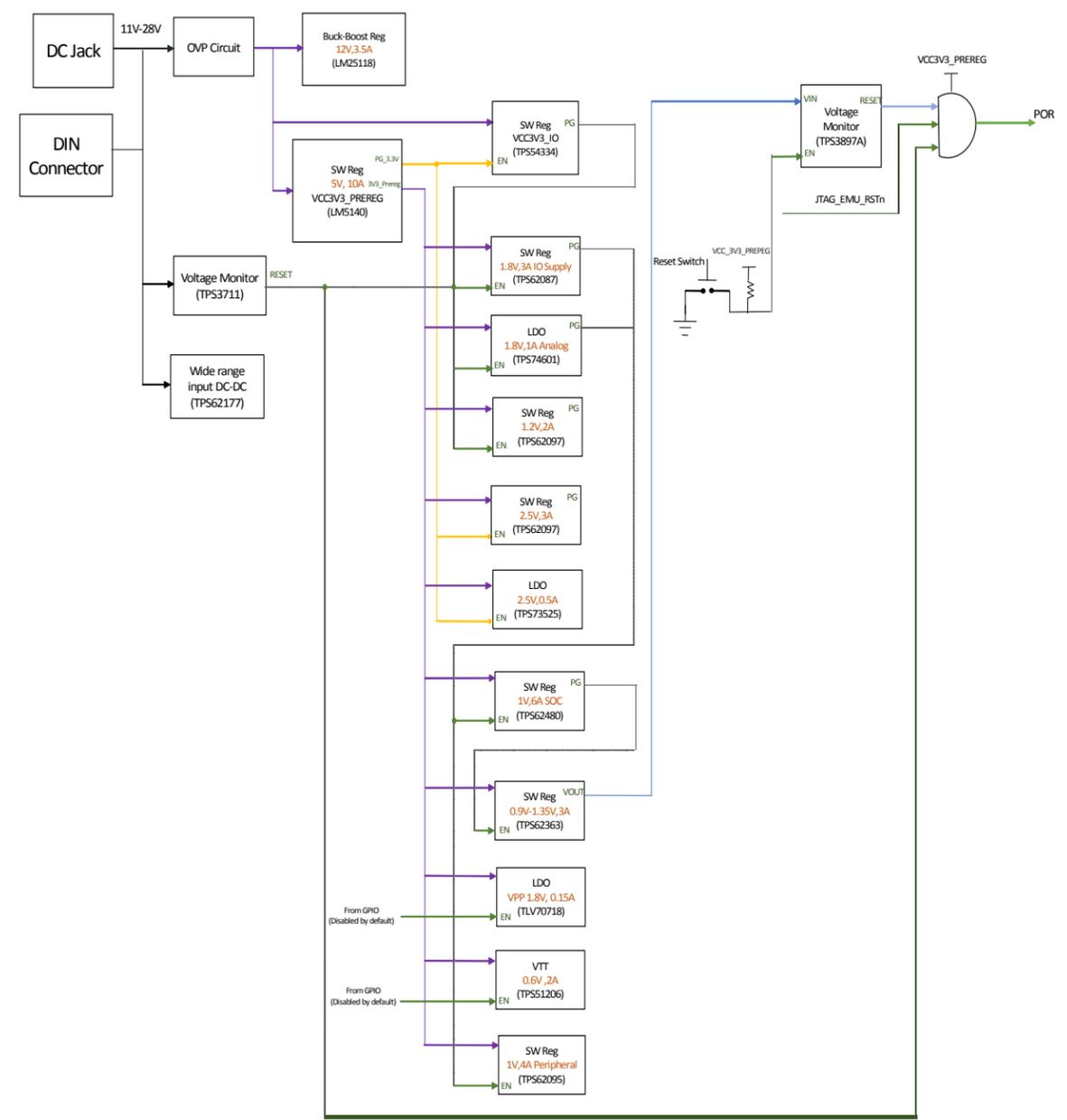
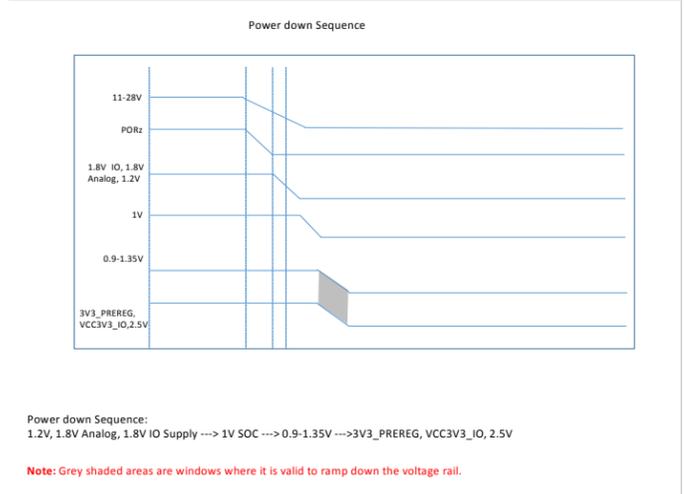
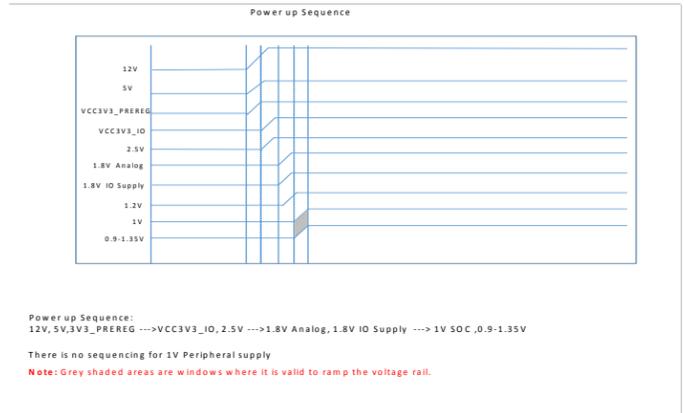


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Title		BLOCK DIAGRAM_XDS110	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E4
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POWER SEQUENCE



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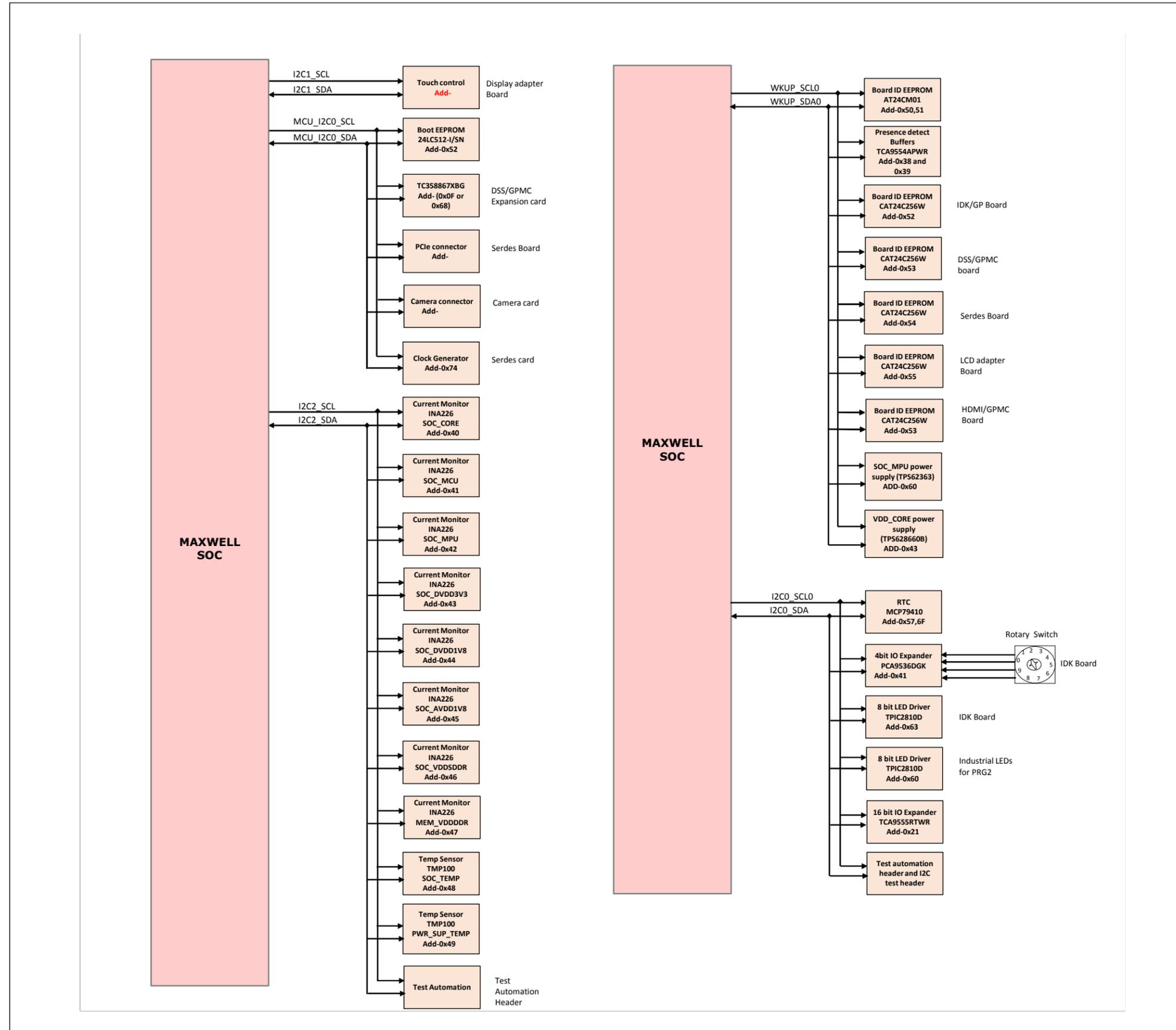


Title POWER SEQUENCE		
Size C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E4
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GPIO MAPPING TABLE

Total No of GPIOs Required from Maxwell SoC								
SI No	GPIO Description	Required on	FUNCTIONALITY	GPIO Number	SoC Muxed Signal name	Direction WRT CTRL	Default state	Active state
1	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_24	MCU_OSPIO_CSN1	Input	High	Low
2	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_27	MCU_OSPI1_DQS	Input	High	Low
3	eMMC Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
4	OSPI flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
5	SPI NOR flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
6	ICSSG_PRG2_Ethernet PHY Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
7	ICSSG_PRG2_Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_87	EXT_REFCLK1	Input/Output	High	Low
8	ICSSG_Ethernet PHY_1 Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	WKUP_GPIO0_50	MCU_SPIO_D1	Input	Low	High
9	ICSSG_Ethernet PHY_2 Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	WKUP_GPIO0_8	WKUP_GPIO0_8	Input	Low	High
10	MCU domain Ethernet PHY Reset Control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
11	MCU domain Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_80	MMC1_SDWP	Input/Output	High	Low
12	Three GPIO's are required to control the Mux select between UART test header RX , Application board & FT4232_ UART_RX	Customer Processor Board	Mux Selection	I2C GPIO Expander		Output	High	Low
13				I2C GPIO Expander		Output	High	Low
14				I2C GPIO Expander		Output	High	Low
15	VPP LDO enable	Customer Processor Board	VPP_EN	WKUP_GPIO0_26	MCU_OSPI1_LBCLKO	Output	Low	High
16	One WKUP_GPIO for VTT Regulator Enable	Customer Processor Board	VTT_EN	WKUP_GPIO0_28	MCU_OSPI1_DO	Output	Low	High
17	GPIO0 to drive PRG2 LED0	Customer Processor Board	LEDs	I2C GPIO Expander		Output	Low	High
18	GPIO1 to drive PRG2 LED1	Customer Processor Board	LEDs	I2C GPIO Expander		Output	Low	High
19	GPIO2 to drive PRG2 LED2	Customer Processor Board	LEDs	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	Low	High
20	GPIO3 to drive PRG2 LED3	Customer Processor Board	LEDs	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	Low	High
21	SOC MPU regulator reset control	Customer Processor Board	RESET_SoC_MPU	I2C GPIO Expander		Output	High	Low
22	SD card load switch enable control	Customer Processor Board	MMC1_SD_EN	I2C GPIO Expander		Output	High	Low
23	IDK_ICSSG_PRG0_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO1_58	PRG0_PRU1_GPO9	Output	High	Low
24	IDK_ICSSG_PRG0_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO1_39	PRG0_PRU0_GPO10	Input/Output	High	Low
25	IDK_ICSSG_PRG1_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO1_38	PRG0_PRU0_GPO9	Output	High	Low
26	IDK_ICSSG_PRG1_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO1_59	PRG0_PRU1_GPO10	Output	High	Low
27	IDK_ICSSG_Ethernet PHY_1 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO1_36/GPIO1_37	PRG0_PRU0_GPO7/PRG0_PRU0_GPO8	Input	Low	High
28	IDK_ICSSG_Ethernet PHY_2 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO1_56/GPIO1_57	PRG0_PRU1_GPO7/PRG0_PRU1_GPO8	Input	Low	High
29	IDK_ICSSG_Ethernet PHY_3 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO0_63/GPIO0_64	PRG1_PRU0_GPO7/PRG1_PRU0_GPO8	Input	Low	High
30	IDK_ICSSG_Ethernet PHY_4 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO0_83/GPIO0_84	PRG1_PRU1_GPO7/PRG1_PRU1_GPO8	Input	Low	High
31	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_46	PRG0_PRU0_GPO17	Output	Low	High
32	IDK_ICSSG0_Ethernet LED1	IDK /GP Application board	LEDs	GPIO1_66	PRG0_PRU1_GPO17	Output	Low	High
33	IDK_ICSSG0_Ethernet LED2	IDK /GP Application board	LEDs	GPIO1_48	PRG0_PRU0_GPO19	Output	Low	High
34	IDK_ICSSG0_Ethernet LED3	IDK /GP Application board	LEDs	GPIO1_68	PRG0_PRU1_GPO19	Output	Low	High
35	IDK_ICSSG0_Ethernet LED4	IDK /GP Application board	LEDs	GPIO0_73	PRG1_PRU0_GPO17	Output	Low	High
36	IDK_ICSSG0_Ethernet LED5	IDK /GP Application board	LEDs	GPIO0_93	PRG1_PRU1_GPO17	Output	Low	High
37	IDK_ICSSG0_Ethernet LED6	IDK /GP Application board	LEDs	GPIO0_75	PRG1_PRU0_GPO19	Output	Low	High
38	IDK_ICSSG0_Ethernet LED7	IDK /GP Application board	LEDs	GPIO0_95	PRG1_PRU1_GPO19	Output	Low	High
39	Touch Reset Control GPIO	LCD Adapter Board	Reset	I2C GPIO Expander		Output	High	Low
40	Touch Interrupt GPIO	LCD Adapter Board	Interrupt	I2C GPIO Expander		Input	Low	High
41	LCD Display Enable GPIO	LCD Adapter Board	LCD_EN	I2C GPIO Expander		Output	High	Low
42	CSI Camera Module Reset Control GPIO	CSI Connector	Reset	I2C GPIO Expander		Output	High	Low
43	Display_Power_Down GPIO	HDMI / GPMC Daughter Card	Display_PowerDown	I2C GPIO Expander		Output	High	Low
44	Touch Event GPIO	HDMI / GPMC Daughter Card	Interrupt	I2C GPIO Expander		Input	High	Low
45	SGMII PHY reset control	Serdes Modules	Reset	I2C GPIO Expander		Output	High	Low
46	SGMII PHY Interrupt	Serdes Modules	Interrupt	GPIO1_81	NMIN	Input/Output	High	Low

I2C TREE



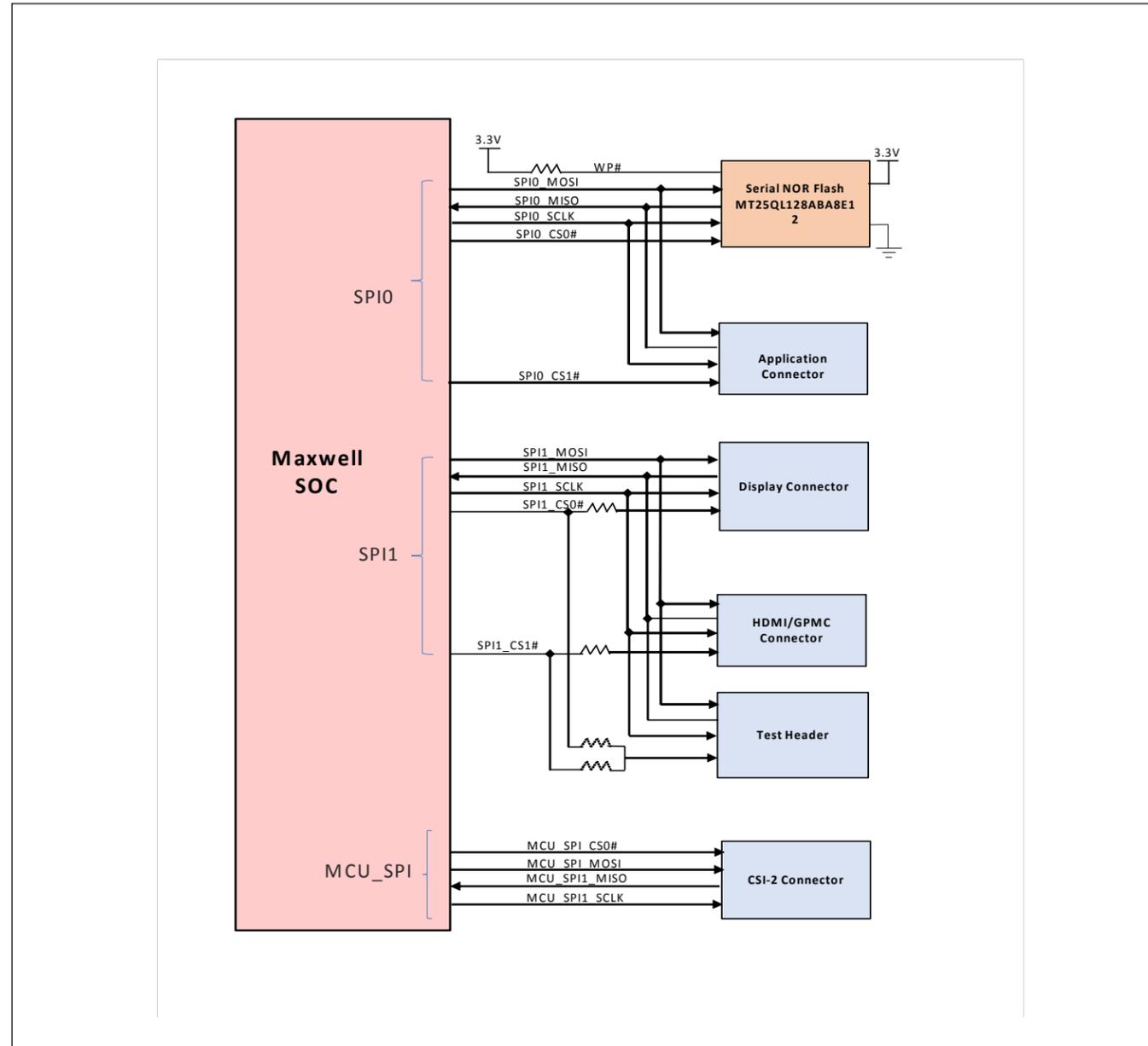
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Title I2C TREE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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SPI TREE



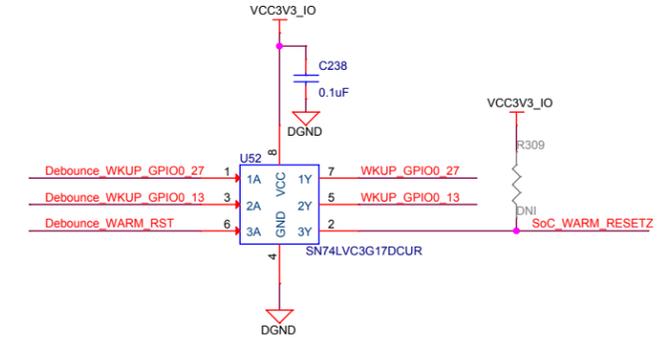
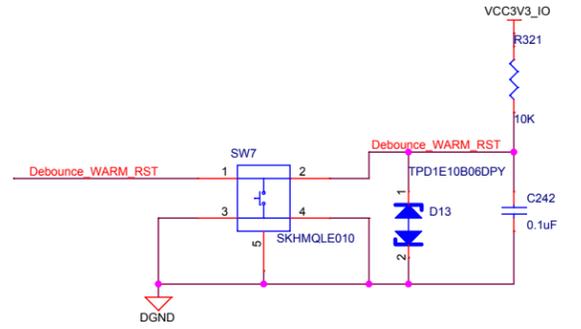
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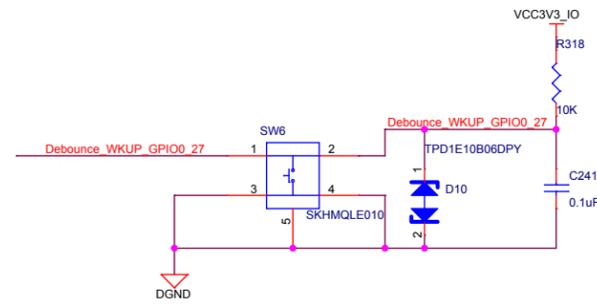
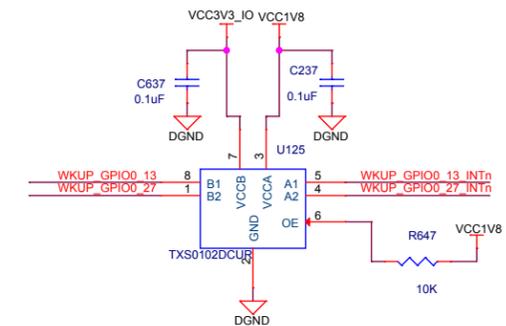
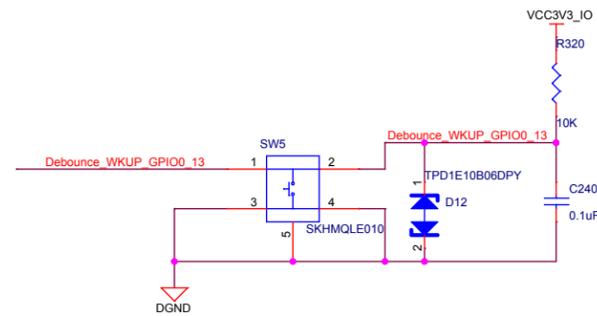
Title SPI TREE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
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SoC WARM_RST

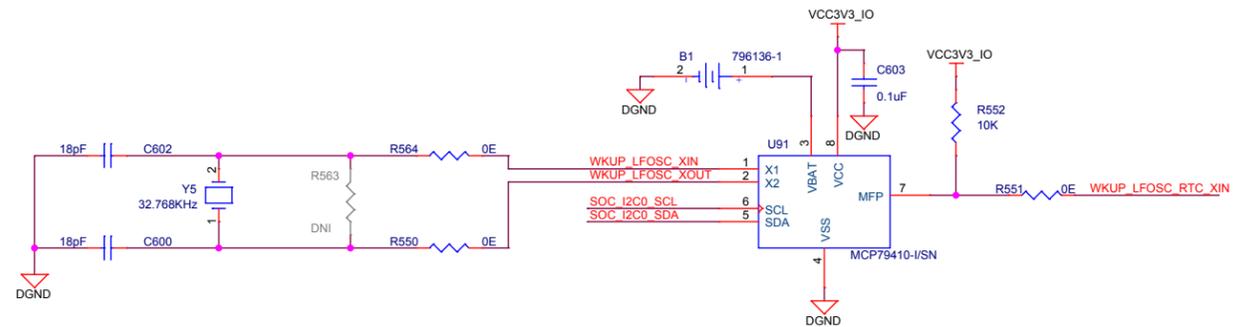
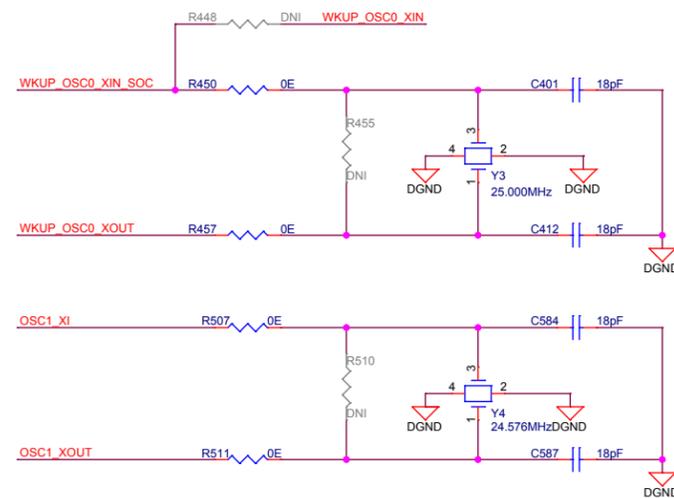


MCU_PUSH BUTTONS



- 36 WKUP_OSC0_XIN >> WKUP_OSC0_XIN
- 33 SoC_WARM_RESETZ << SoC_WARM_RESETZ
- 18 WKUP_GPIO0_13_INTn >> WKUP_GPIO0_13_INTn
- 18 WKUP_GPIO0_27_INTn >> WKUP_GPIO0_27_INTn
- 33 WKUP_OSC0_XIN_SOC >> WKUP_OSC0_XIN_SOC
- 33 WKUP_OSC0_XOUT >> WKUP_OSC0_XOUT
- 33 OSC1_XI >> OSC1_XI
- 33 OSC1_XOUT >> OSC1_XOUT
- 33 WKUP_LFOSC_RTC_XIN >> WKUP_LFOSC_RTC_XIN
- 32,33,37,38 SOC_I2C0_SCL >> SOC_I2C0_SCL
- 32,33,37,38 SOC_I2C0_SDA >> SOC_I2C0_SDA

SoC CLOCK



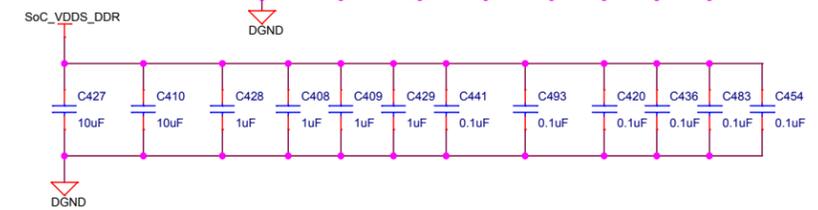
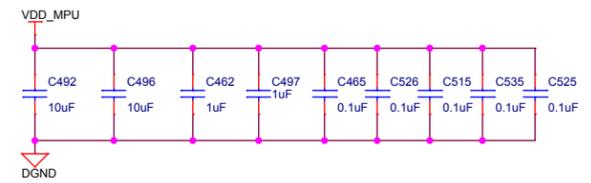
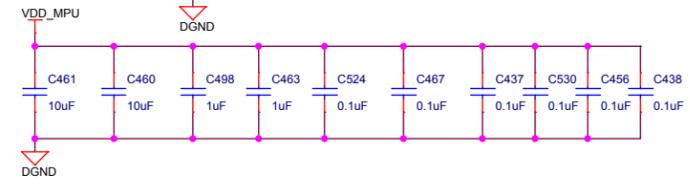
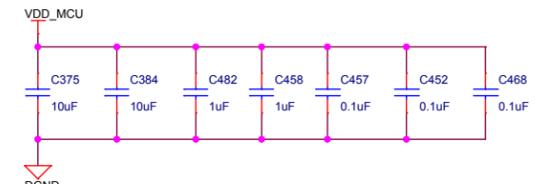
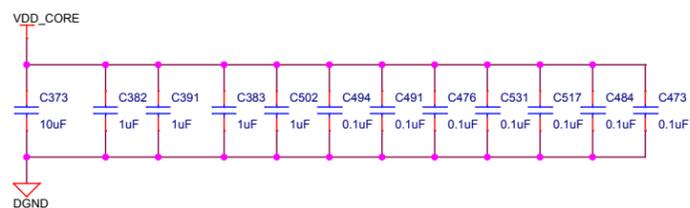
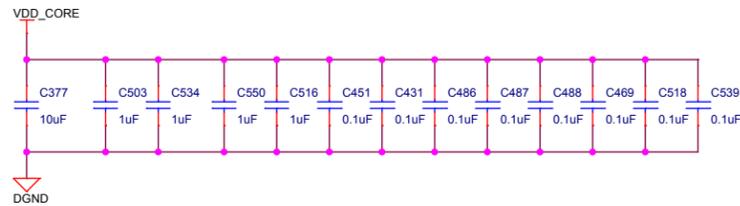
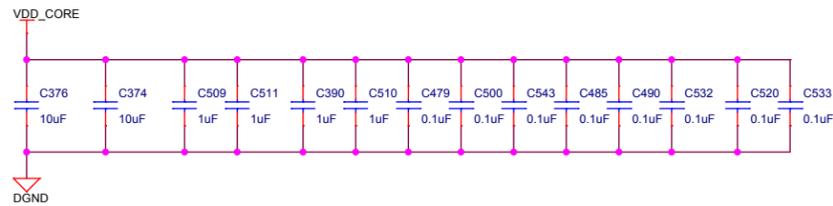
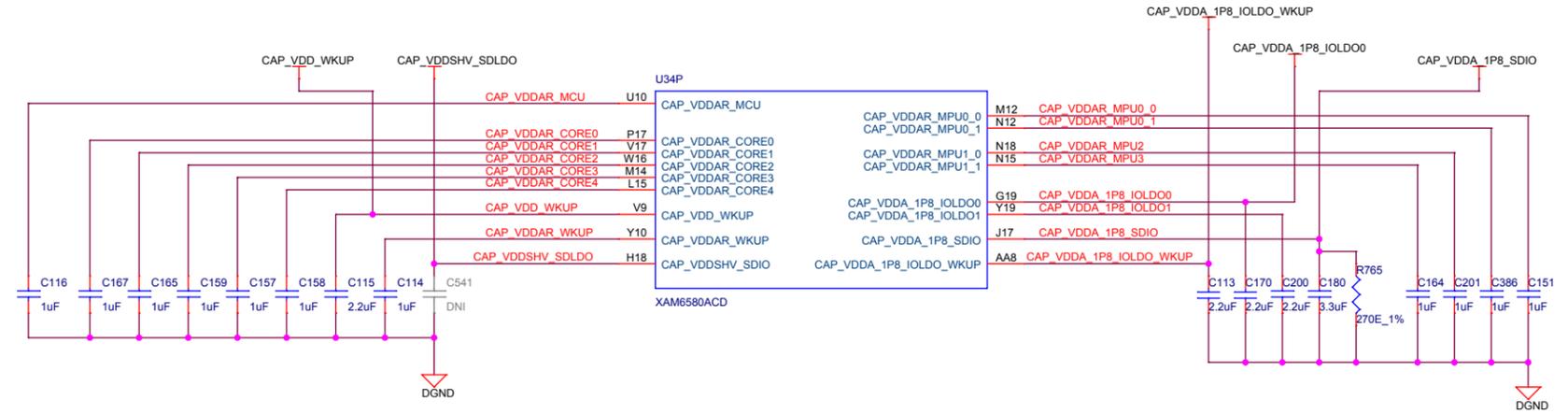
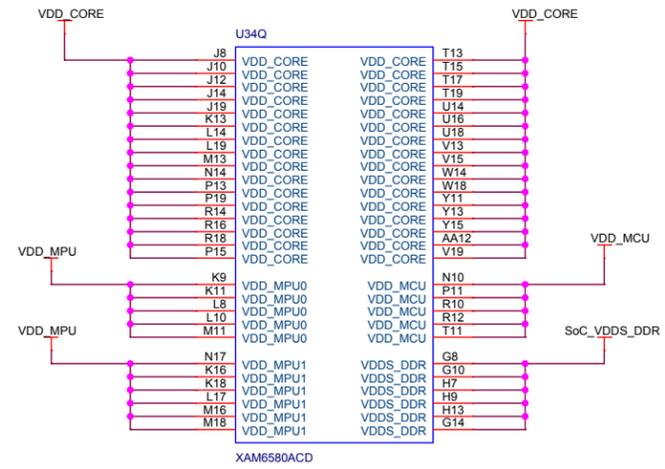
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Title SoC CLOCK & RESET

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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PROCESSOR POWER & DECAPS



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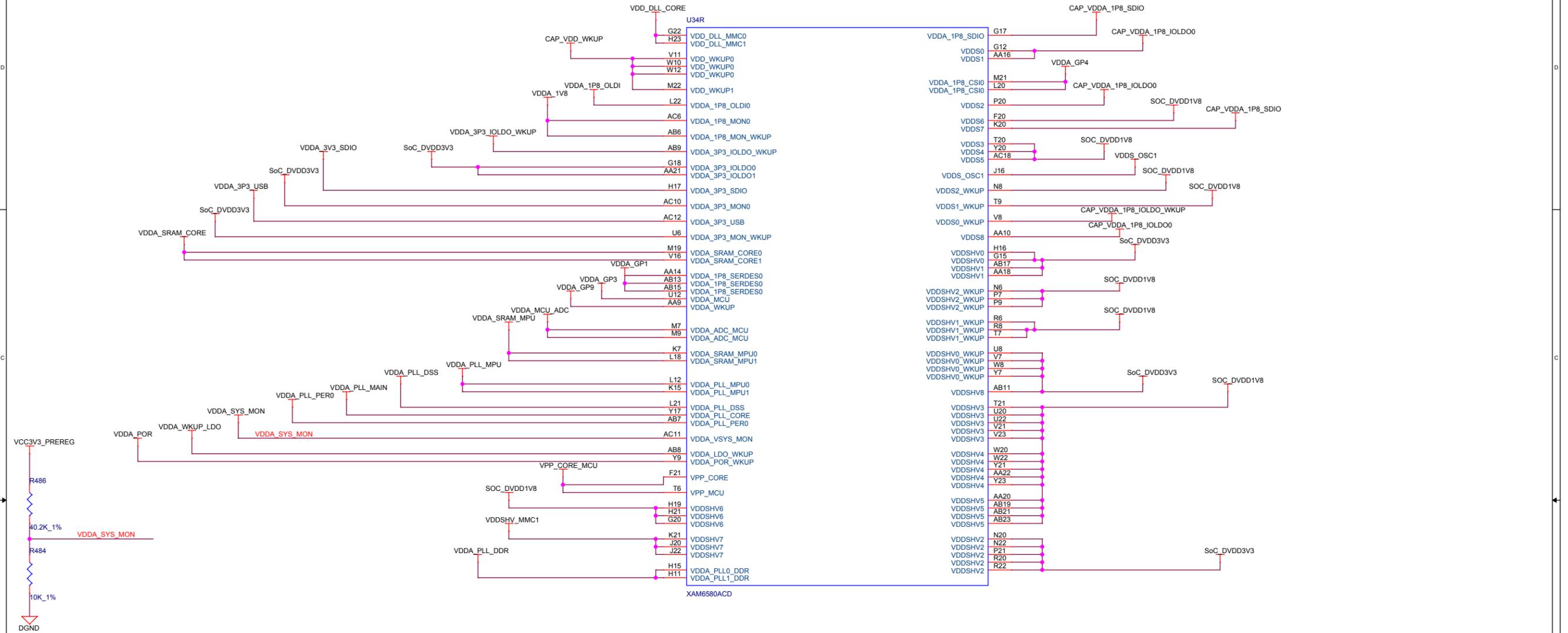


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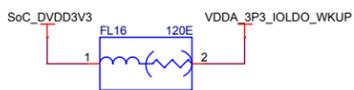
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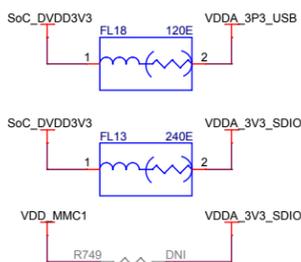
SoC POWER



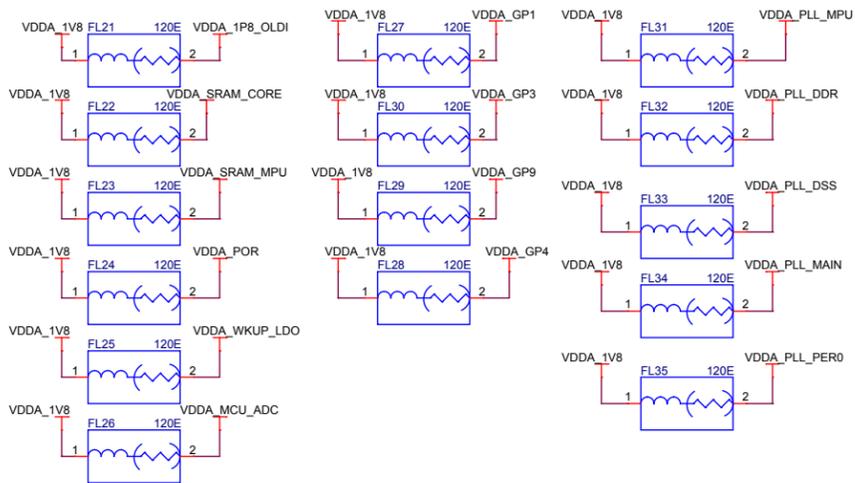
3.3V IO SUPPLY



3.3V ANALOG SUPPLY



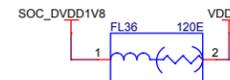
1.8V Analog SUPPLY



VPP SUPPLY



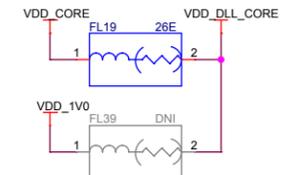
OSCILLATOR SUPPLY



MMC1 IO SUPPLY



CORE SUPPLY



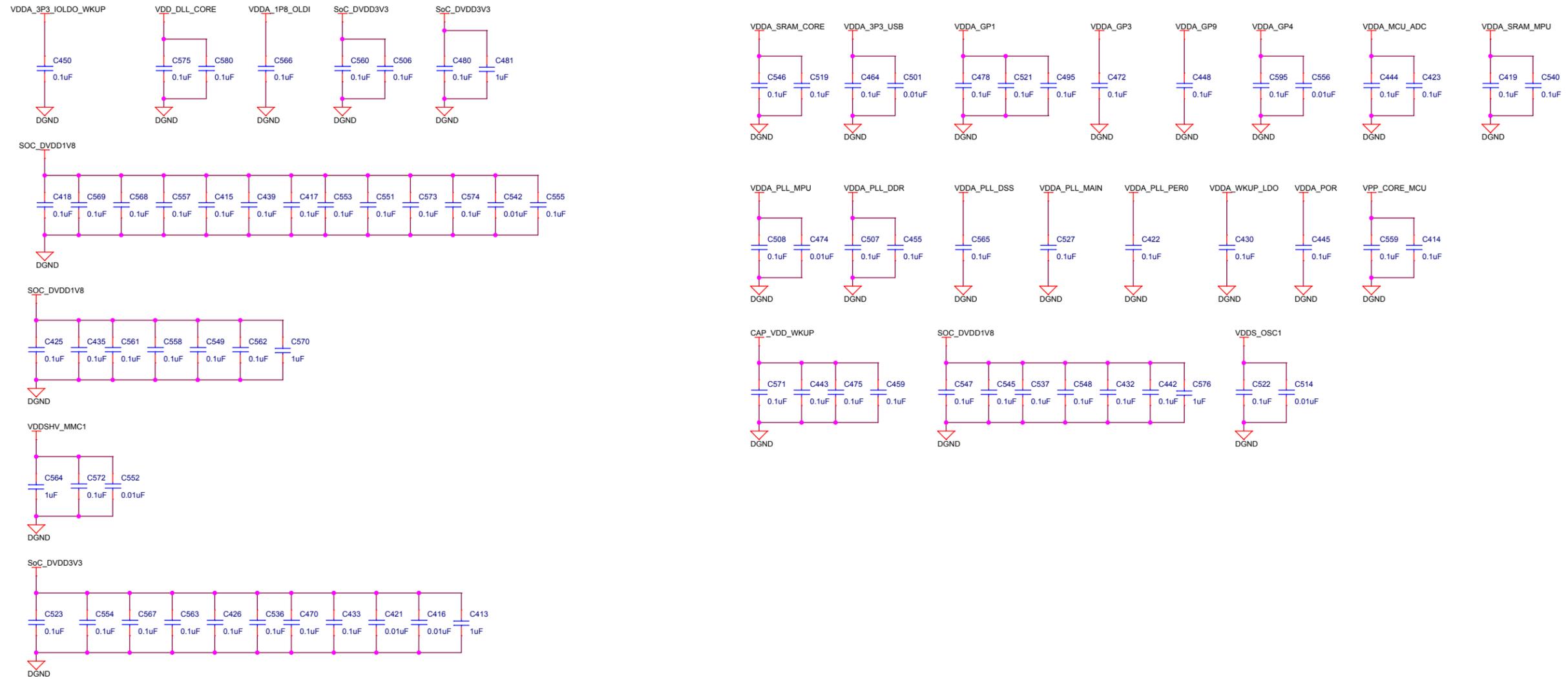
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Title SoC POWER2

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 12 of 44

PROCESSOR DECAPS



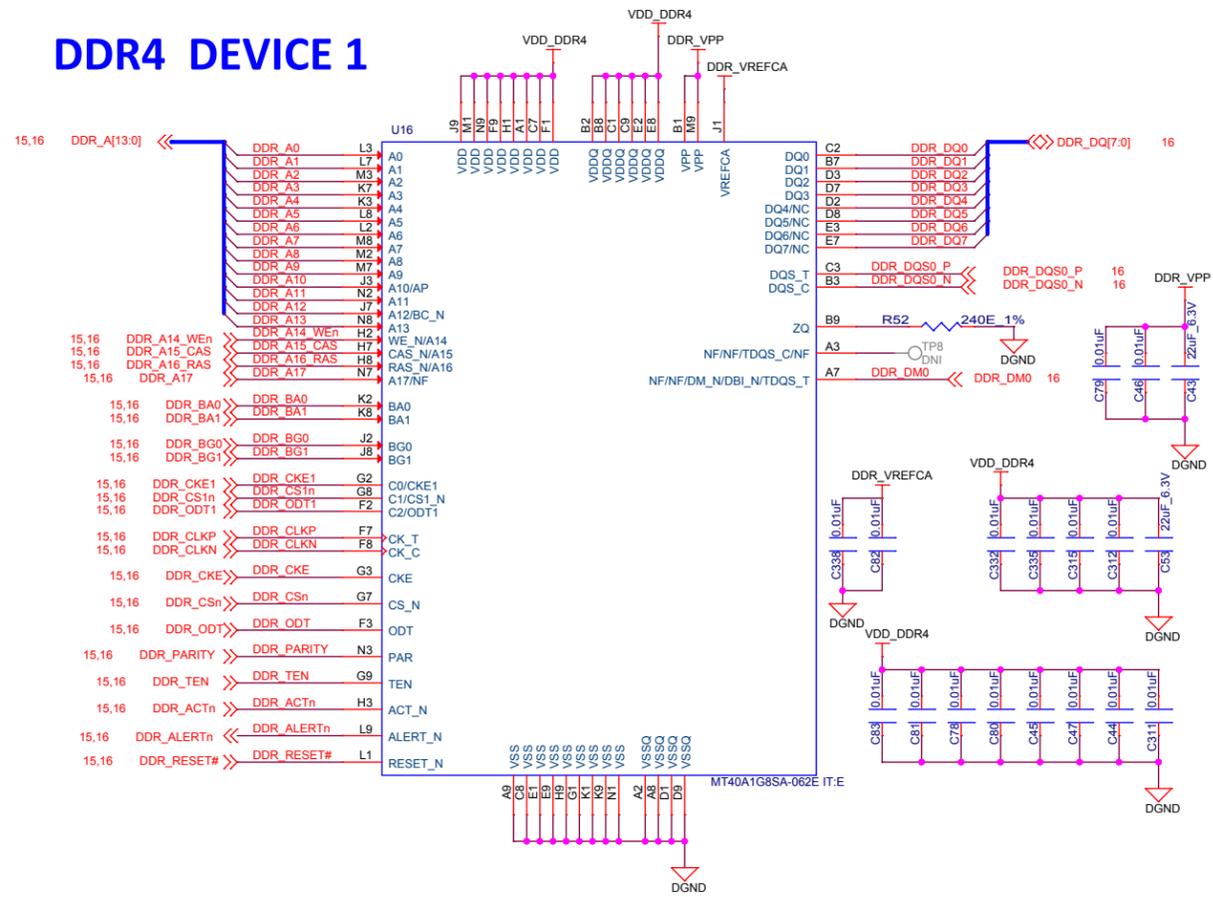
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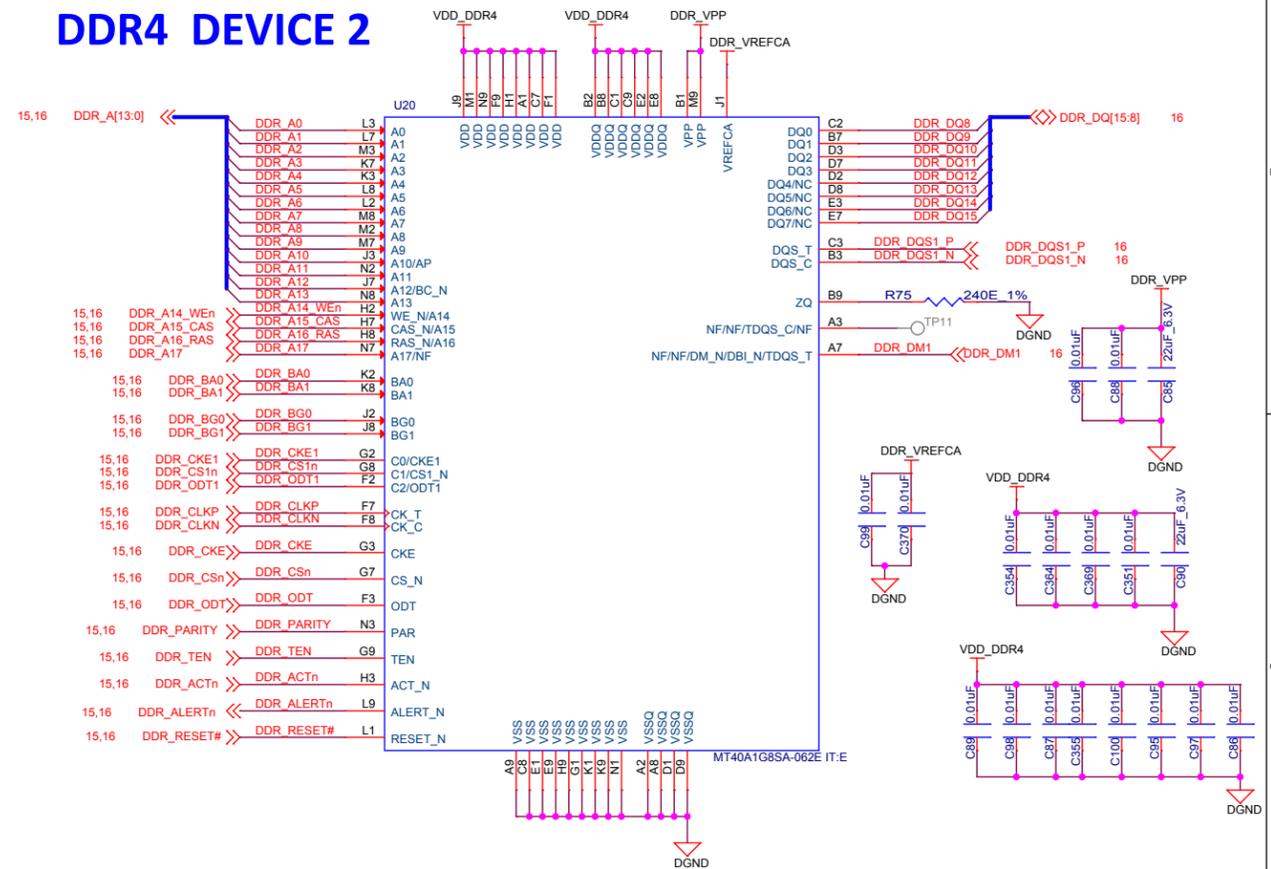
Title SoC POWER3

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 13 of 44

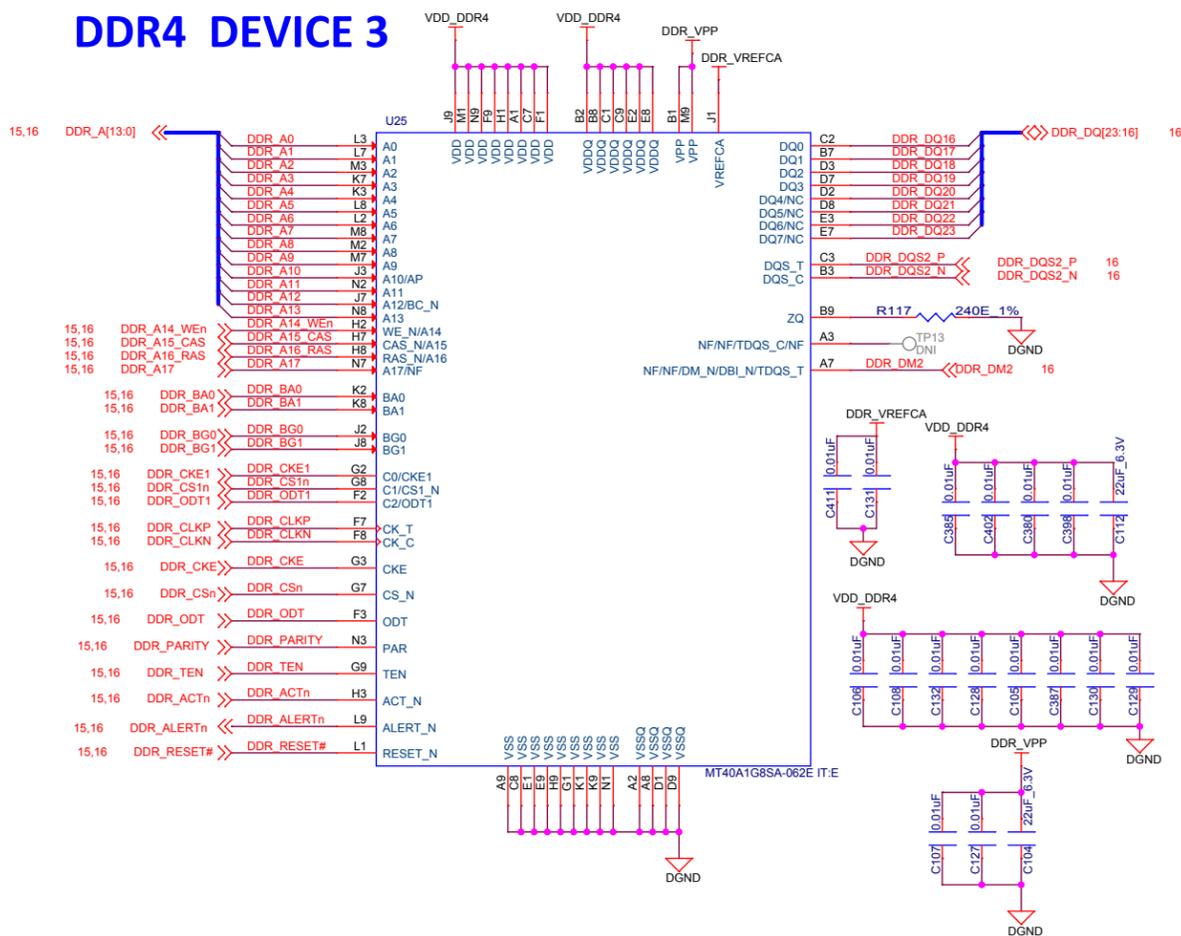
DDR4 DEVICE 1



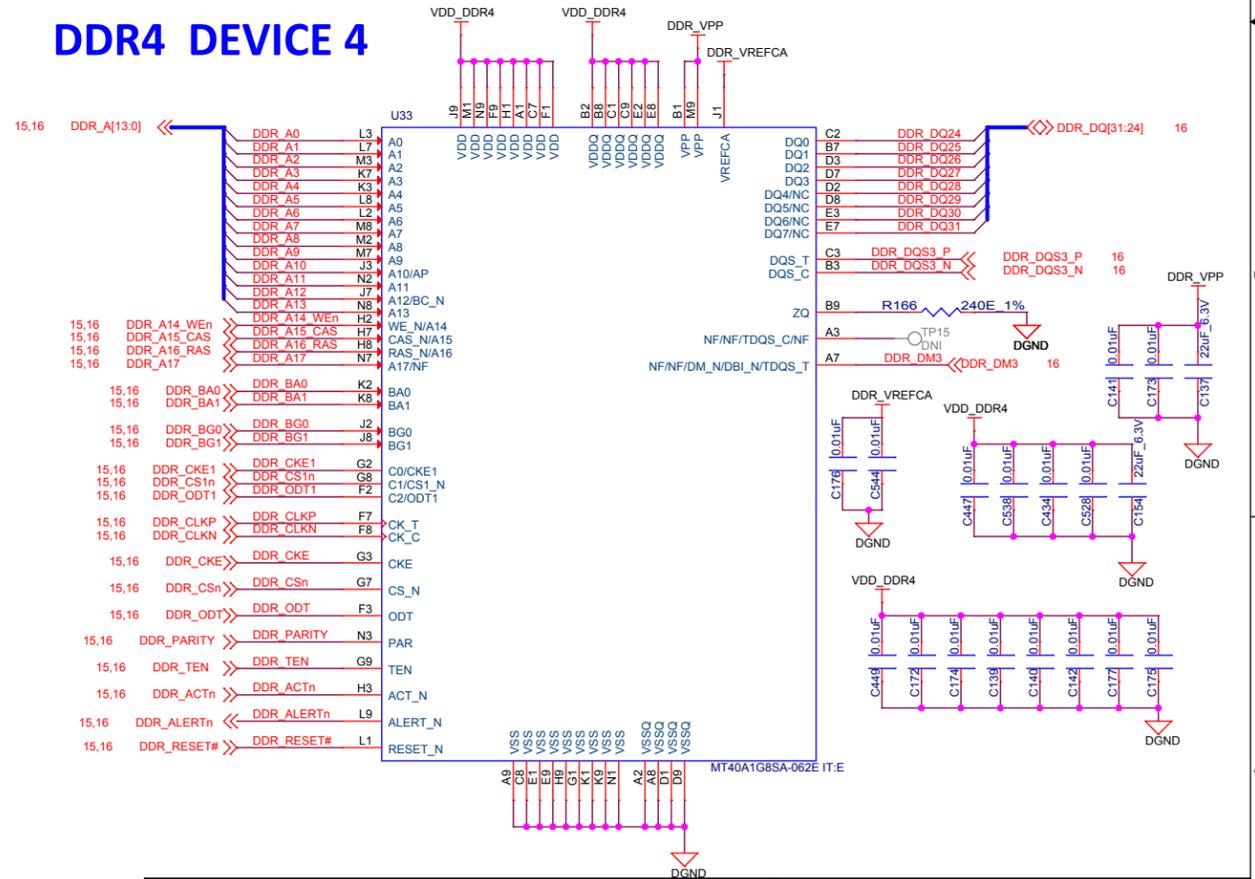
DDR4 DEVICE 2



DDR4 DEVICE 3



DDR4 DEVICE 4

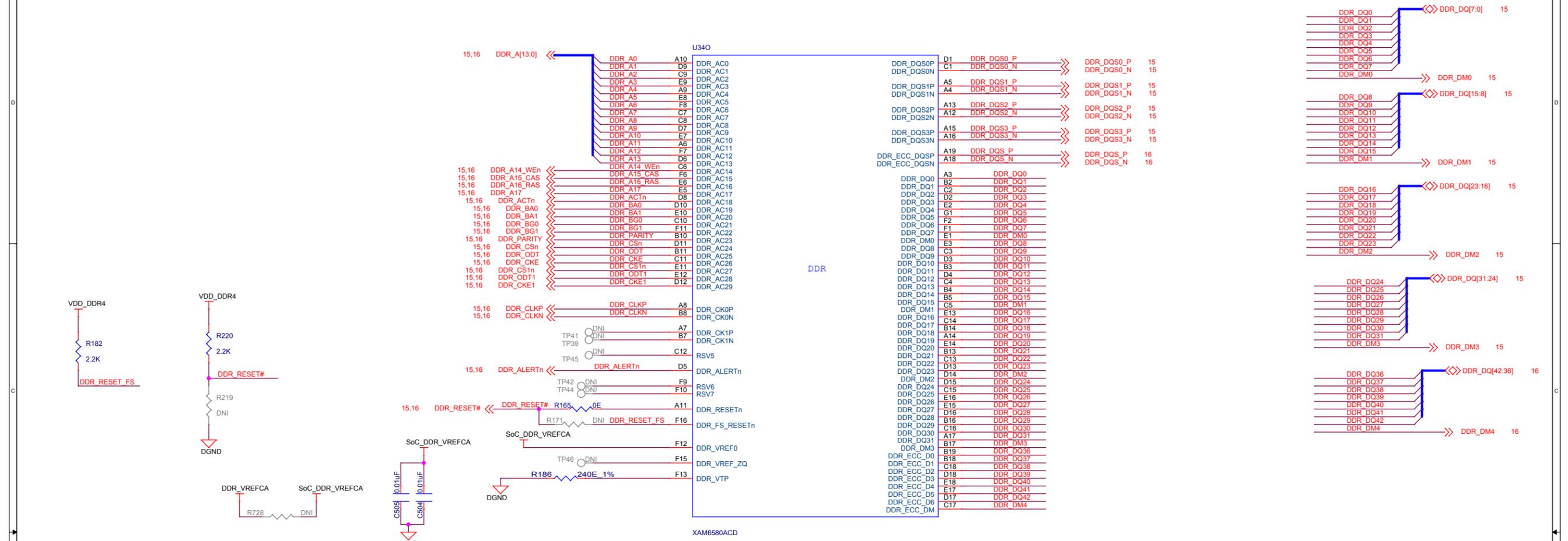


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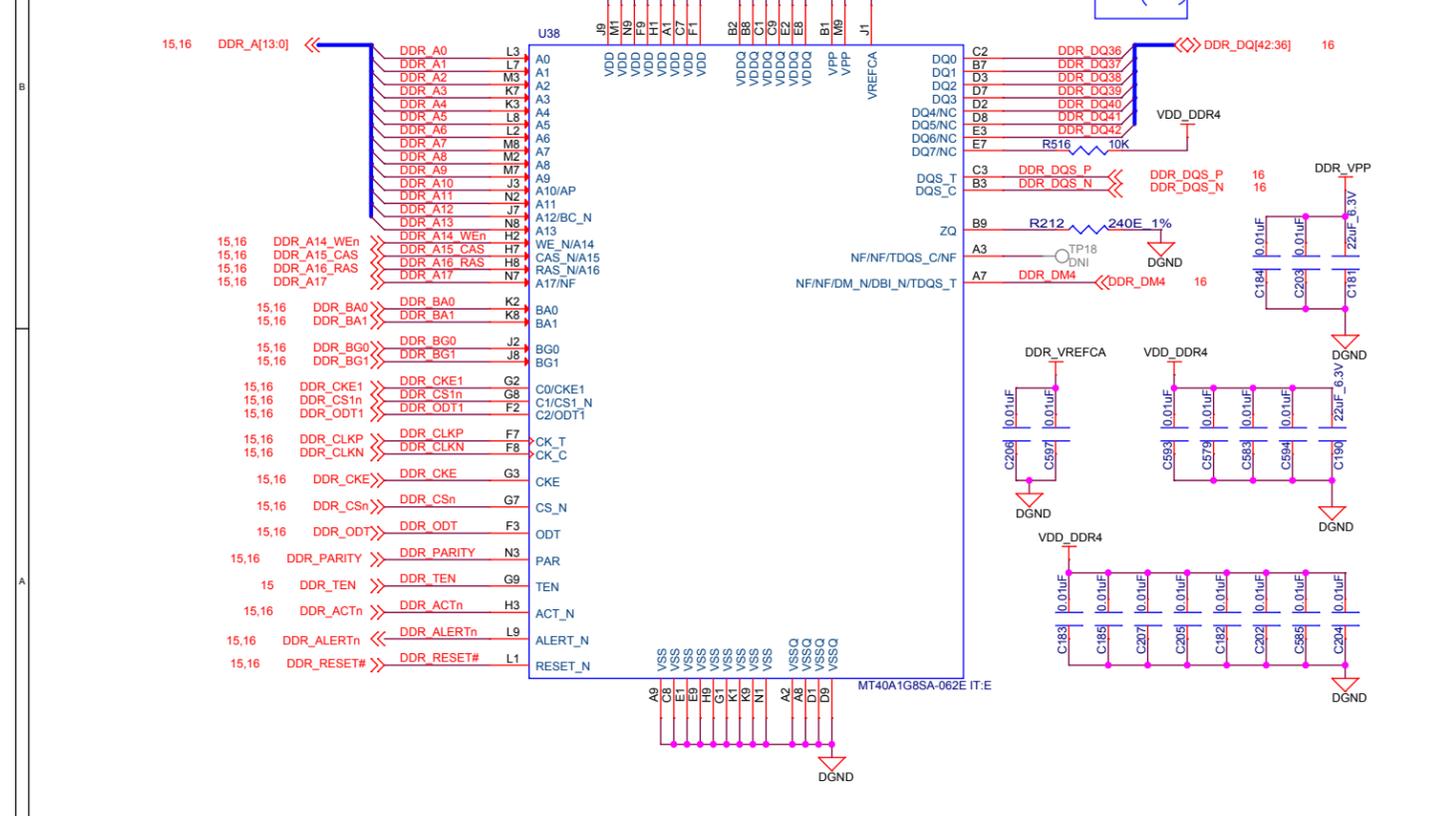


Title		DDR4 DEVICES	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E4
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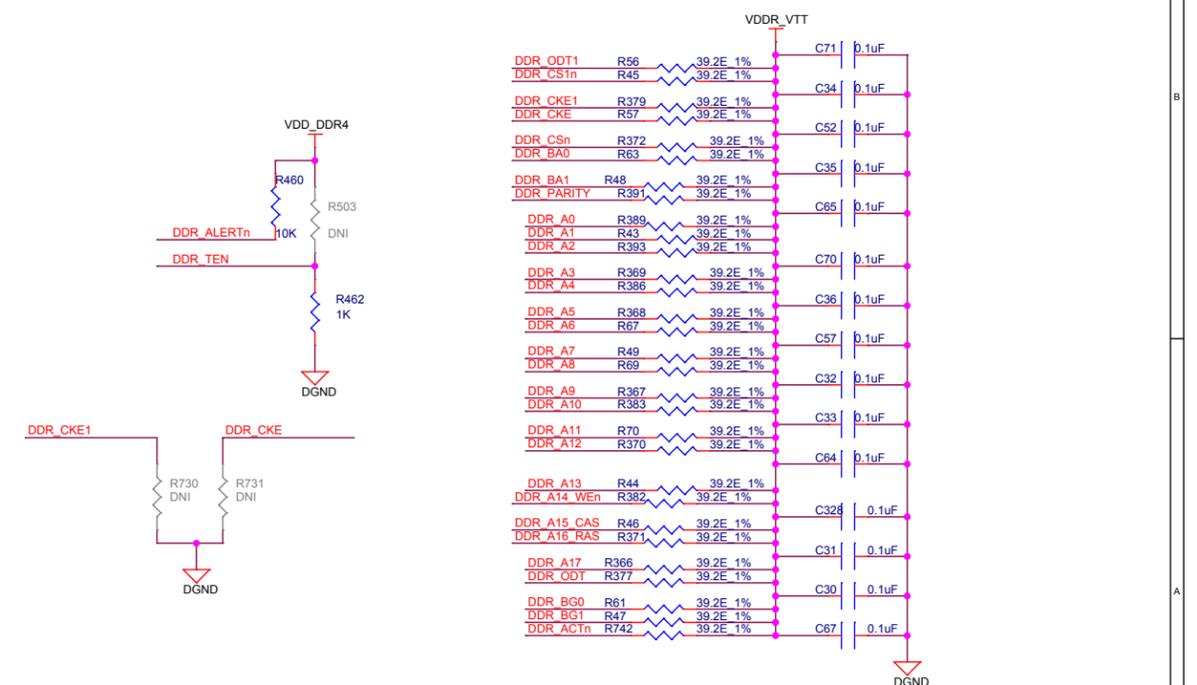
SoC DDR INTERFACE



ECC DEVICE



DDR TERMINATION

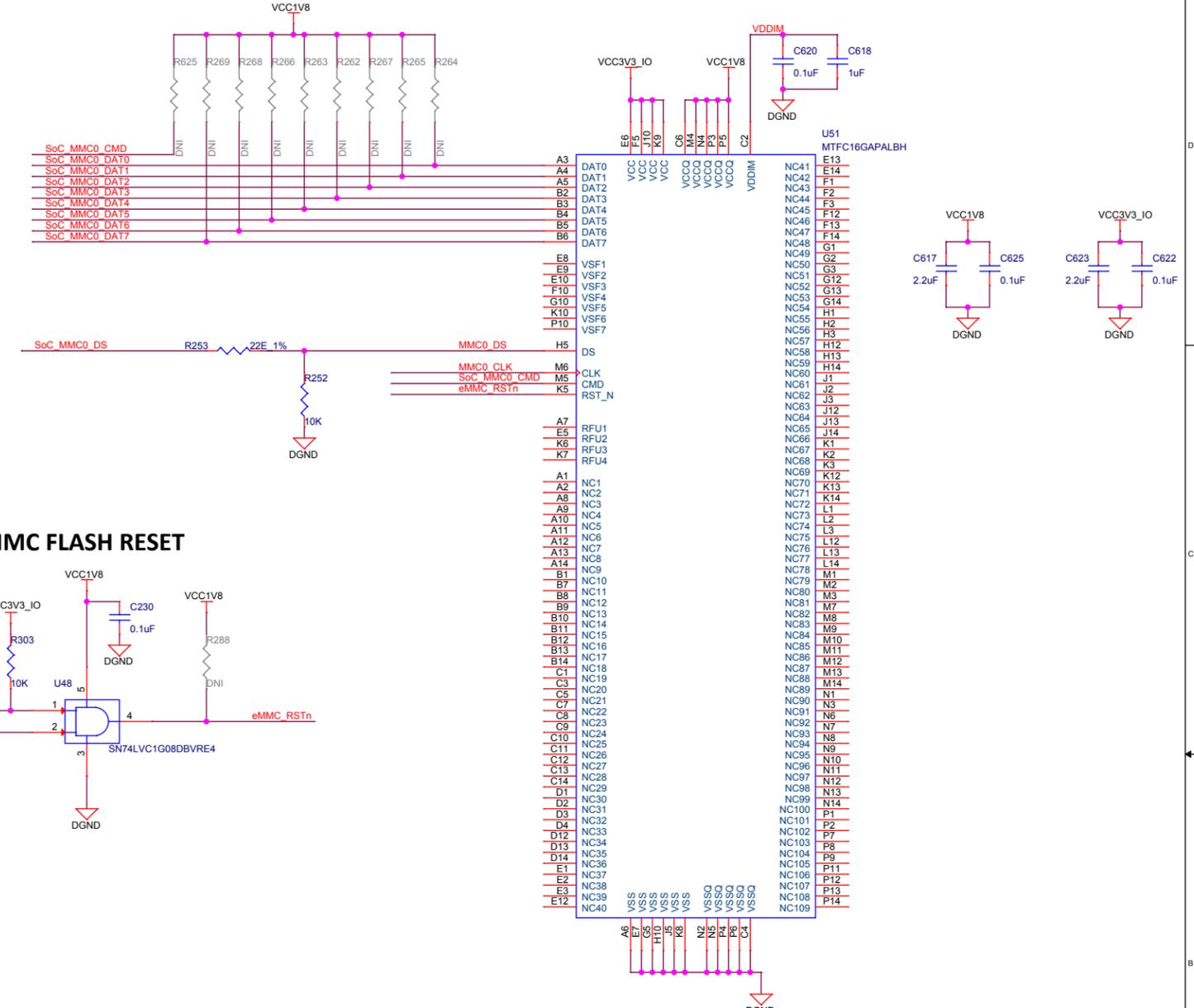
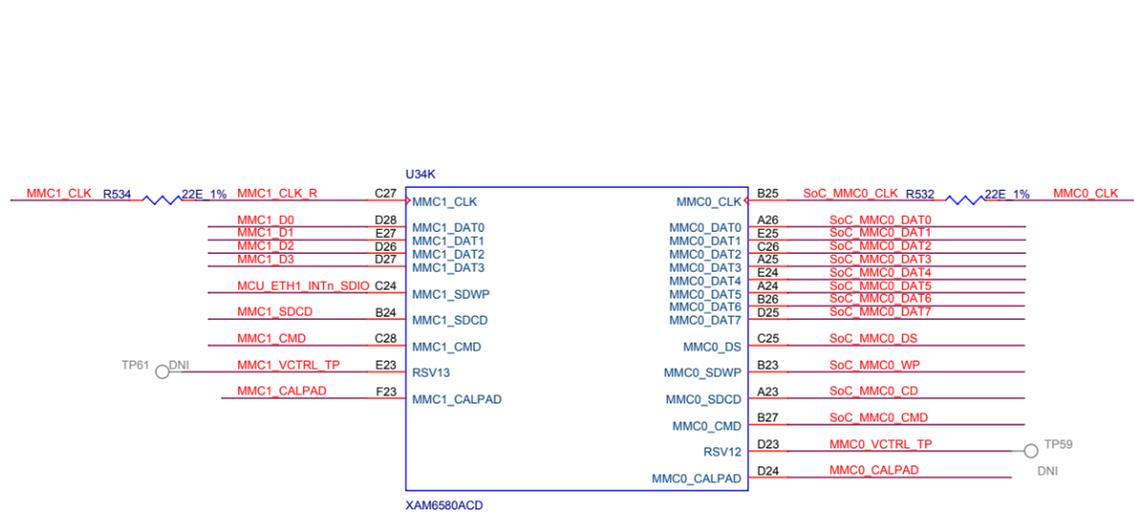


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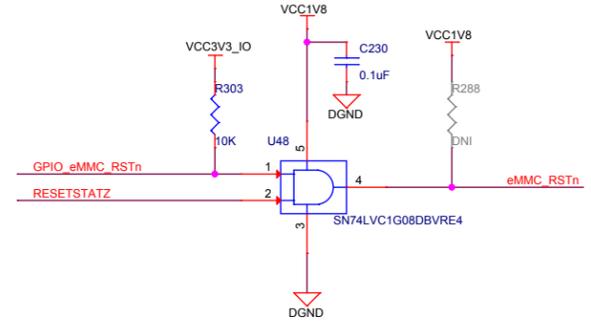


Title		
DDR4 ECC & TERMINATIONS		
Size	Rev	
C	E4	Variant Name = PROC082 001 OPN#TMDX654IDKEVM
Date:	Sheet	of
Thursday, August 22, 2019	16	44

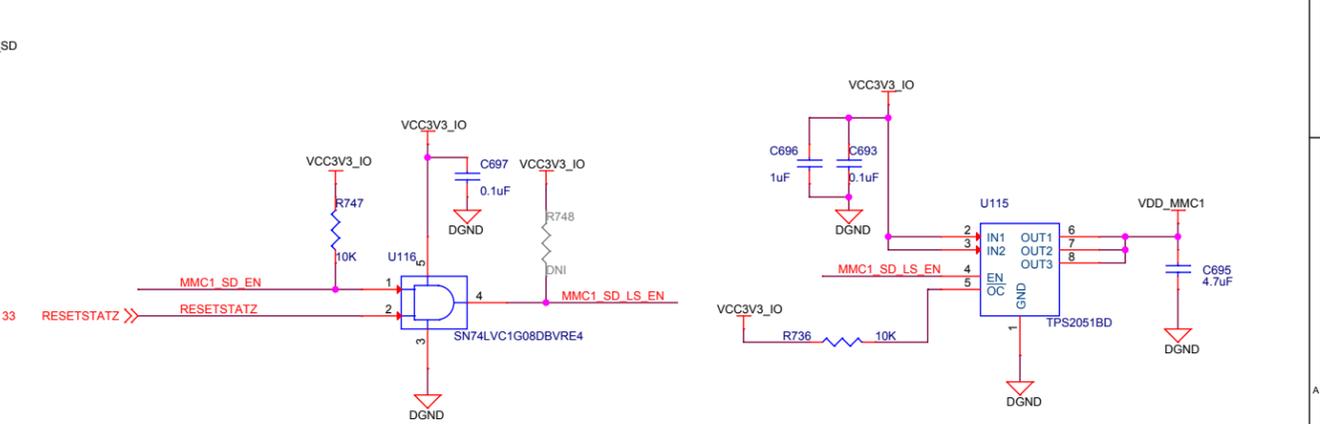
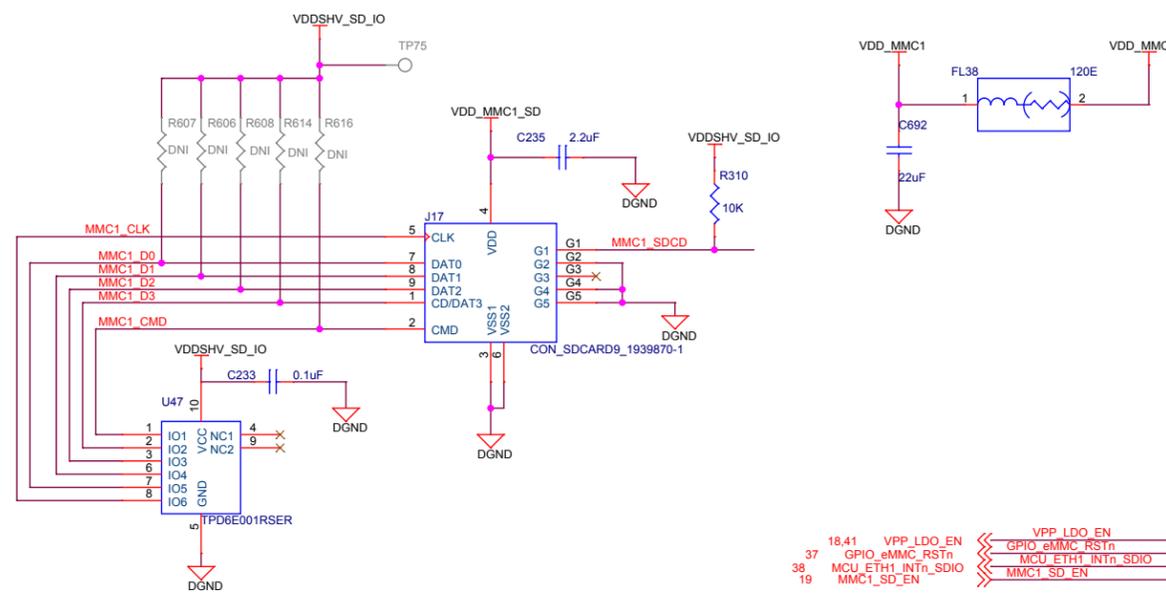
eMMC FLASH



eMMC FLASH RESET



SD CARD INTERFACE



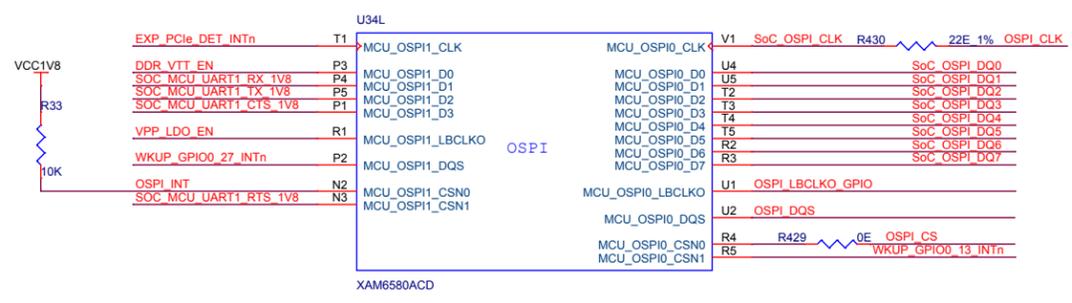
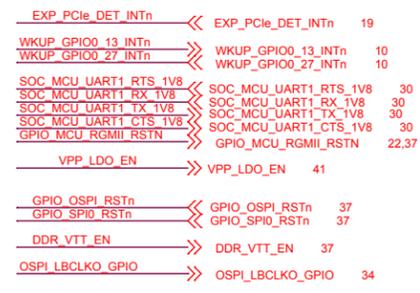
- 18.41 VPP_LDO_EN <<< VPP_LDO_EN
- 37 GPIO_eMMC_RSTn <<< GPIO_eMMC_RSTn
- 38 MCU_ETH1_INTrn_SDIO <<< MCU_ETH1_INTrn_SDIO
- 19 MMC1_SD_EN <<< MMC1_SD_EN

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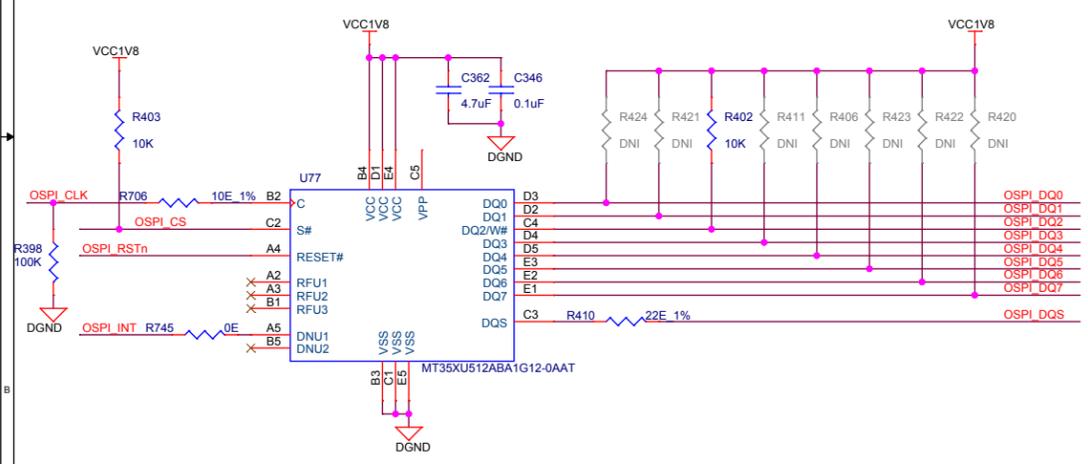
TEXAS INSTRUMENTS **MISTRAL**

Title: eMMC FLASH_SDCARD INTERFACE		Rev: E4
Size: C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev: E4
Date: Wednesday, August 28, 2019	Sheet: 17 of 44	

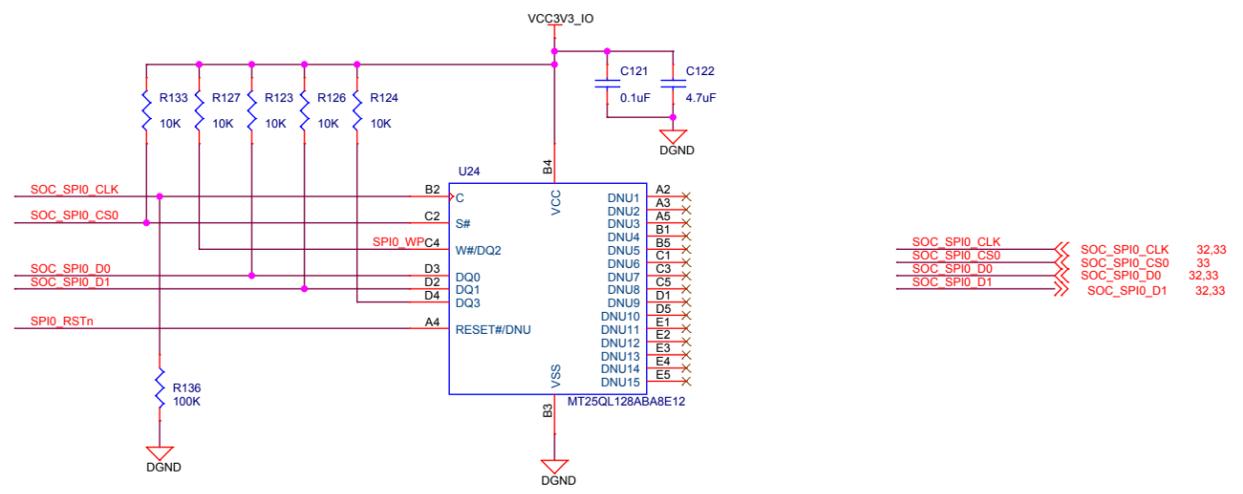
SOC OSPI INTERFACE



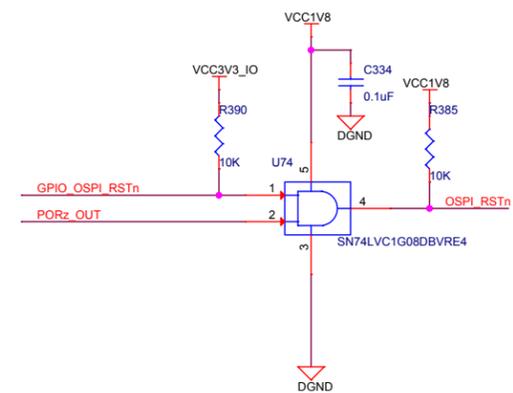
OSPI FLASH



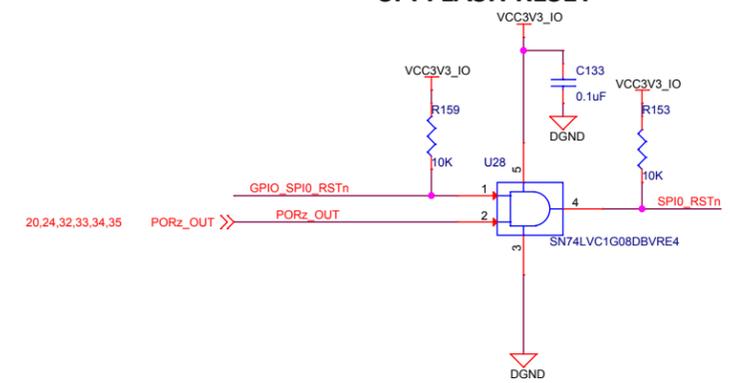
SPI NOR Flash



OSPI FLASH RESET



SPI FLASH RESET

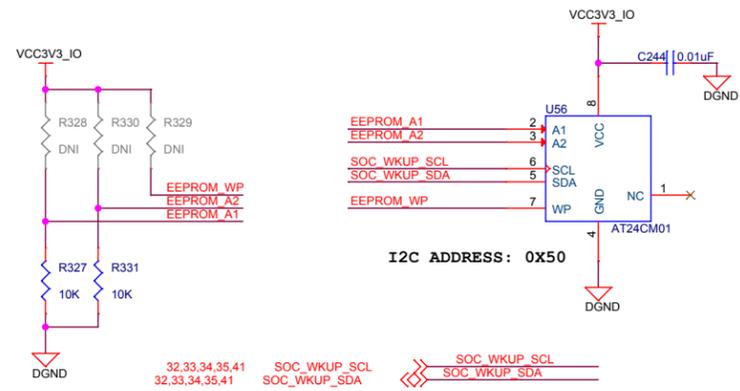


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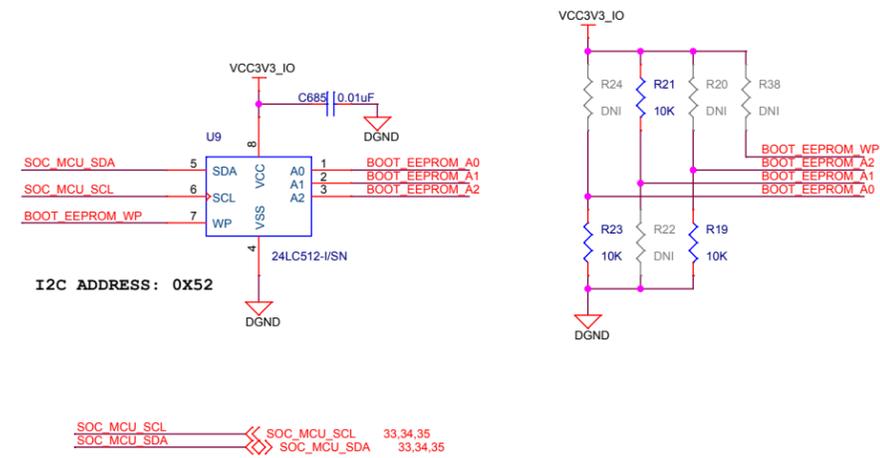


Title OSPI FLASH & SPI NOR FLASH		
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E4
Date: Thursday, August 29, 2019	Sheet 18 of 44	

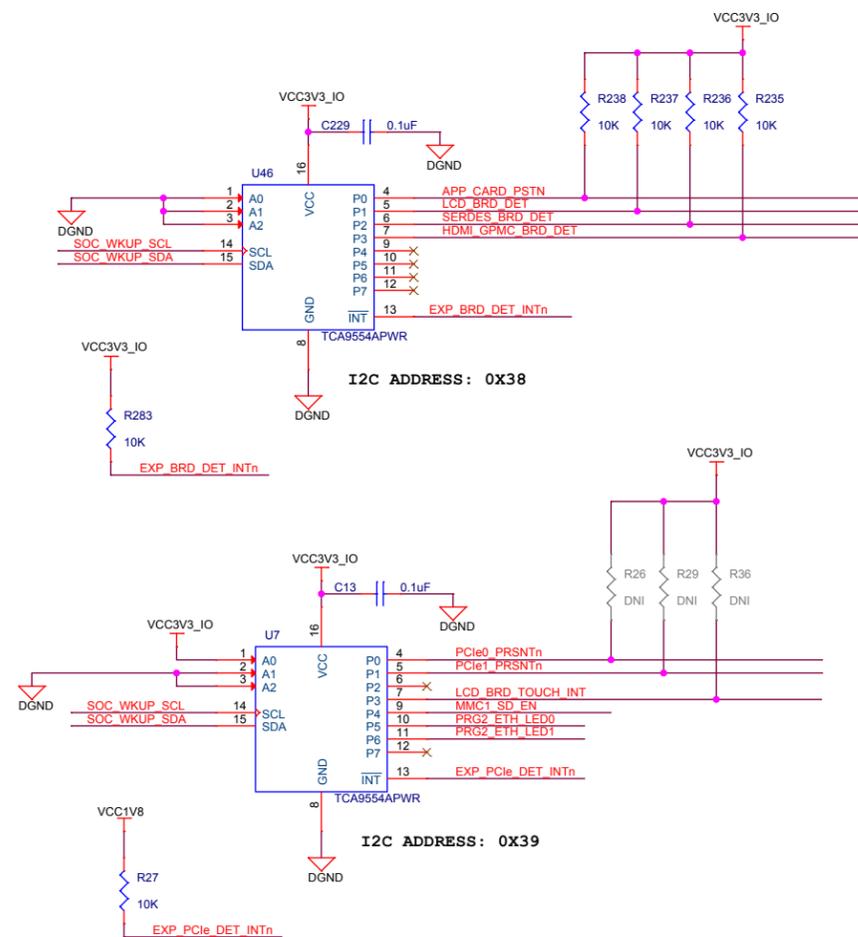
BOARD ID EEPROM



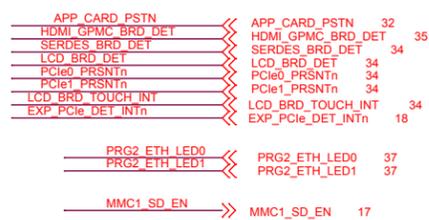
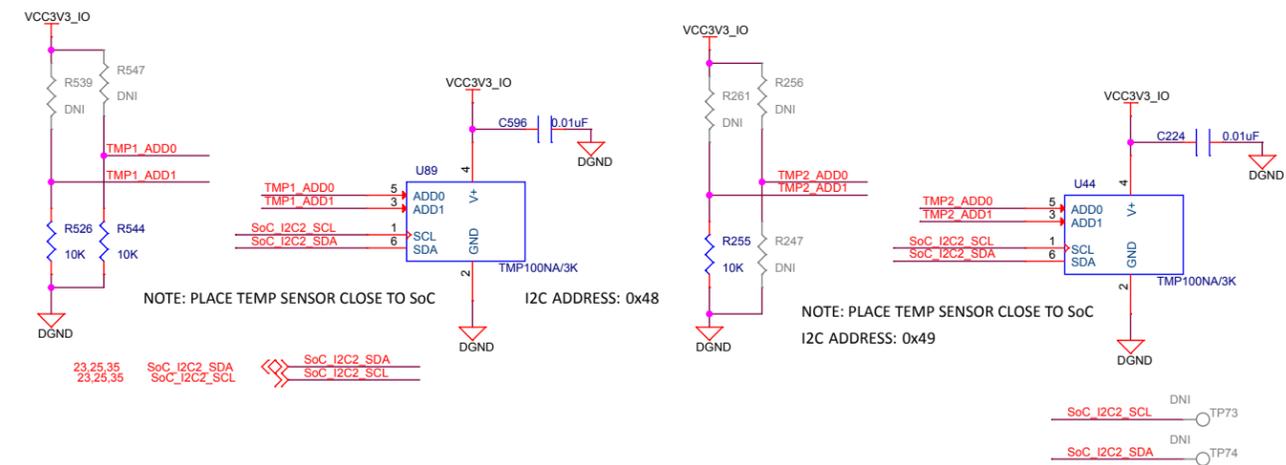
BOOT EEPROM



BOARD PRESENCE DETECT CIRCUIT



TEMPERATURE SENSOR

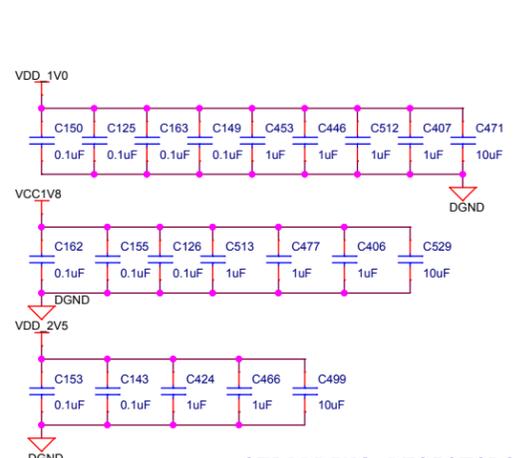


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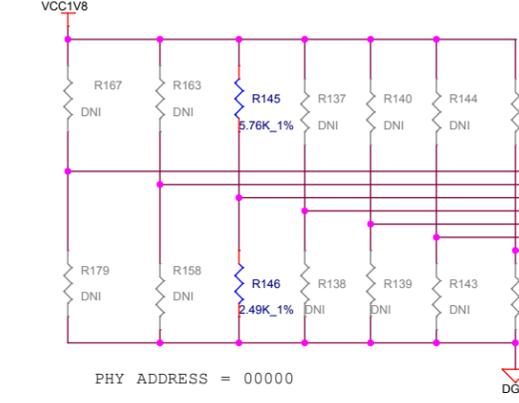


Title EEPROM,PRESENCE DETECTION & TEMP SENSOR

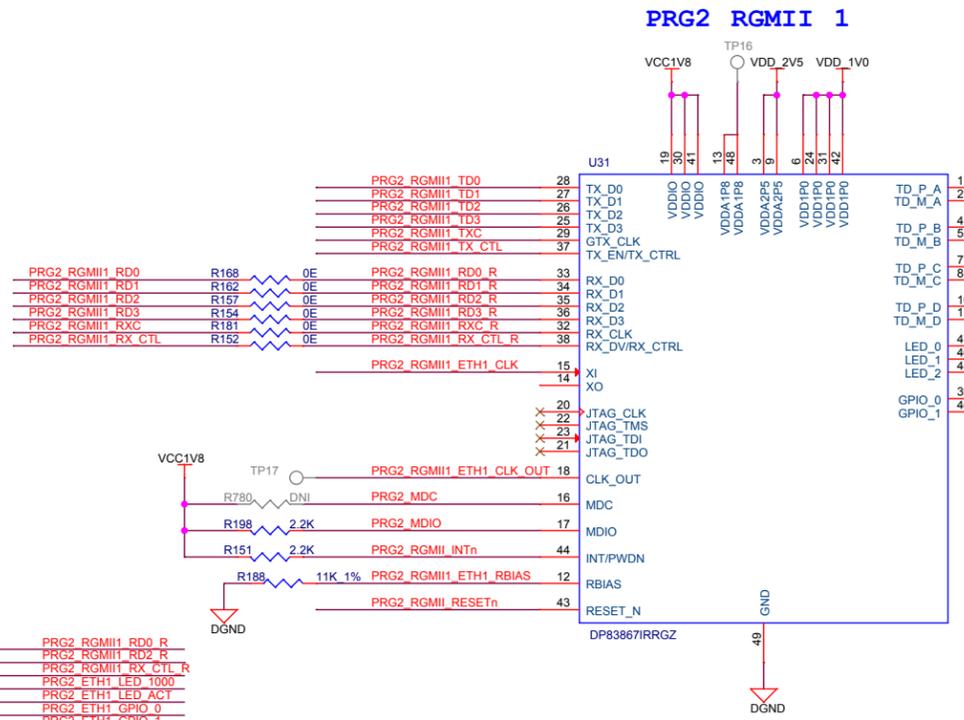
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Thursday, August 29, 2019	Sheet 19 of 44



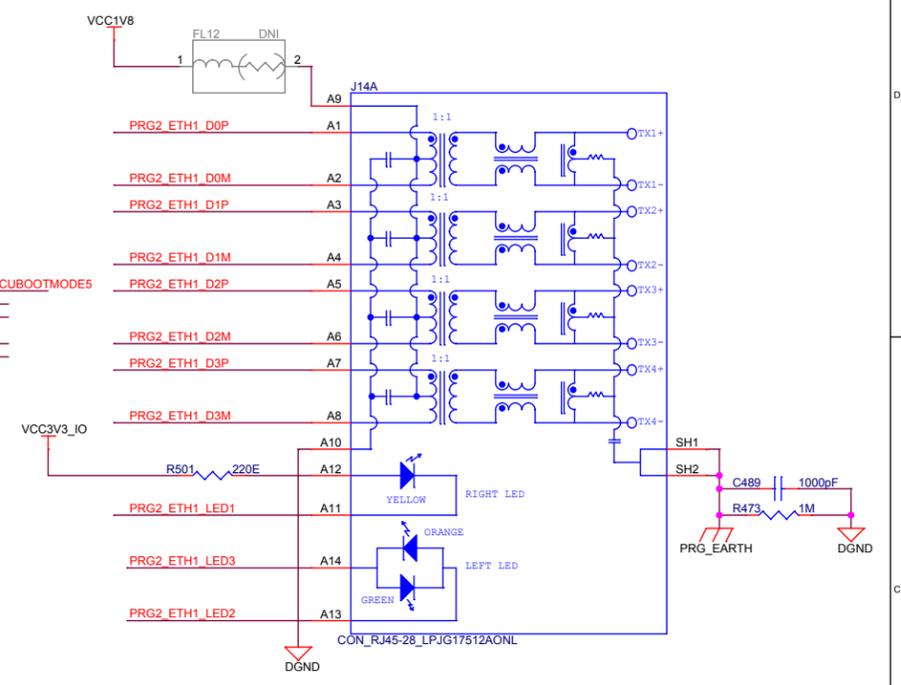
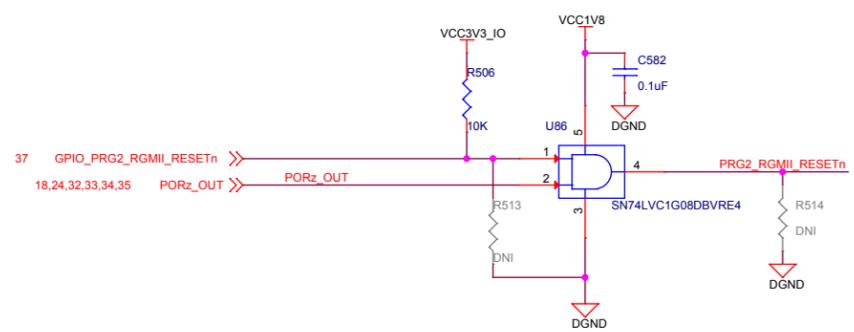
STRAPPING RESISTORS



PHY ADDRESS = 00000

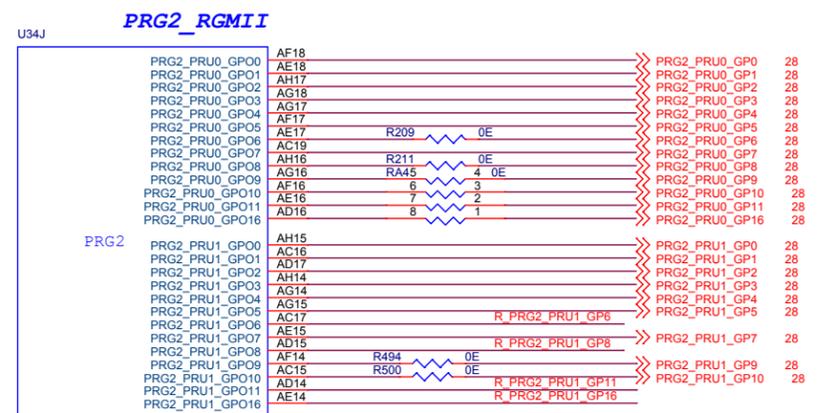


PRG2 PHY1 RESET



21,38	PRG2_RGMII_INTn	PRG2_RGMII_INTn
36	PRG2_RGMII_ETH1_CLK	PRG2_RGMII_ETH1_CLK
28	PRG2_RGMII_TD0	PRG2_RGMII_TD0
28	PRG2_RGMII_TD1	PRG2_RGMII_TD2
28	PRG2_RGMII_TD2	PRG2_RGMII_TD3
28	PRG2_RGMII_TD3	PRG2_RGMII_TXC
28	PRG2_RGMII_TXC	PRG2_RGMII_TX_CTL
28	PRG2_RGMII_TX_CTL	
28	PRG2_RGMII_RD0	PRG2_RGMII_RD0
28	PRG2_RGMII_RD1	PRG2_RGMII_RD2
28	PRG2_RGMII_RD2	PRG2_RGMII_RD3
28	PRG2_RGMII_RD3	PRG2_RGMII_RXC
28	PRG2_RGMII_RXC	PRG2_RGMII_RX_CTL
28	PRG2_RGMII_RX_CTL	
21,28,34	PRG2_MDC	PRG2_MDC
21,28,34	PRG2_MDIO	PRG2_MDIO
21	PRG2_RGMII_RESETn	PRG2_RGMII_RESETn
24,33	PRG2_ETH1_LED_LINK/MCUBOOTMODE5	PRG2_ETH1_LED_LINK/MCUBOOTMODE5

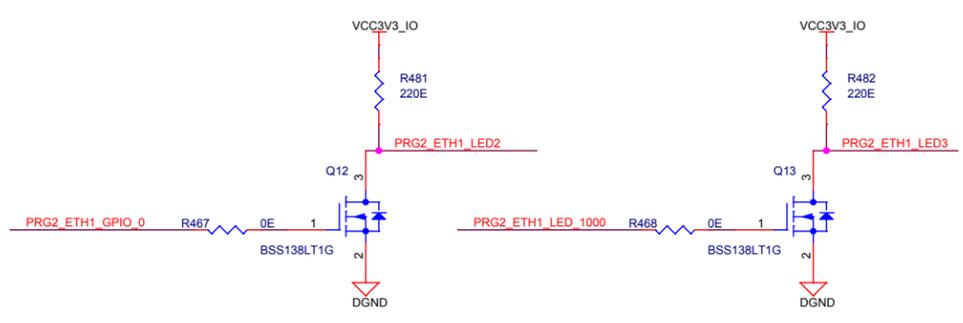
RGMII ETHERNET PHY - ICSSG



XAM6580ACD

R PRG2_PRU1_GP11	RA2	8	1	0E	PRG2_PRU1_GP11
R PRG2_PRU1_GP16	7	2	PRG2_PRU1_GP16		
R PRG2_PRU1_GP6	6	3	PRG2_PRU1_GP6		
R PRG2_PRU1_GP8	5	4	PRG2_PRU1_GP8		
PRG2_PRU1_GP6			PRG2_PRU1_GP6	28	
PRG2_PRU1_GP8			PRG2_PRU1_GP8	28	
PRG2_PRU1_GP11			PRG2_PRU1_GP11	28	
PRG2_PRU1_GP16			PRG2_PRU1_GP16	28	

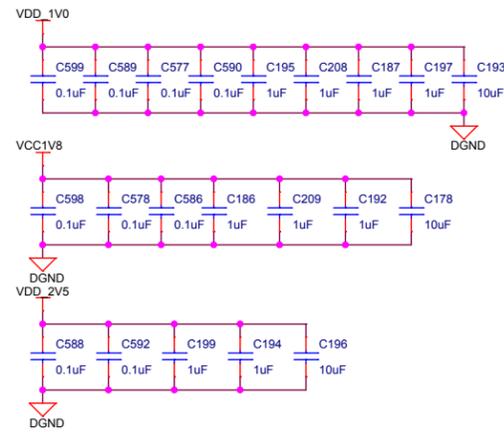
PRG2_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS



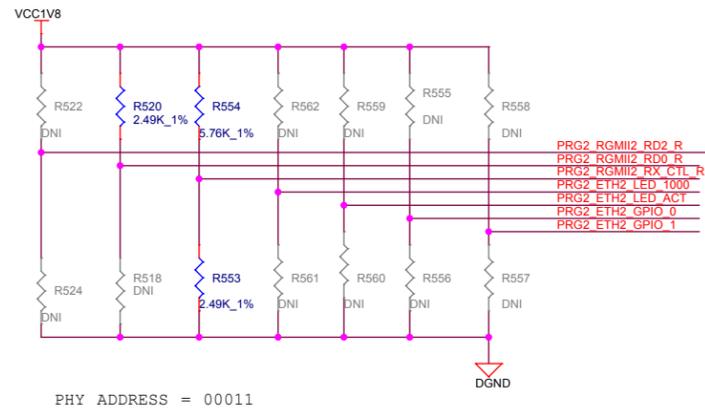
Designed for TI by Mistral Solutions Pvt Ltd

Title		RGMII ETHERNET PHY - ICSSG PRG2_PRU0	
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev	
C		E4	
Date:	Thursday, August 22, 2019	Sheet	20 of 44

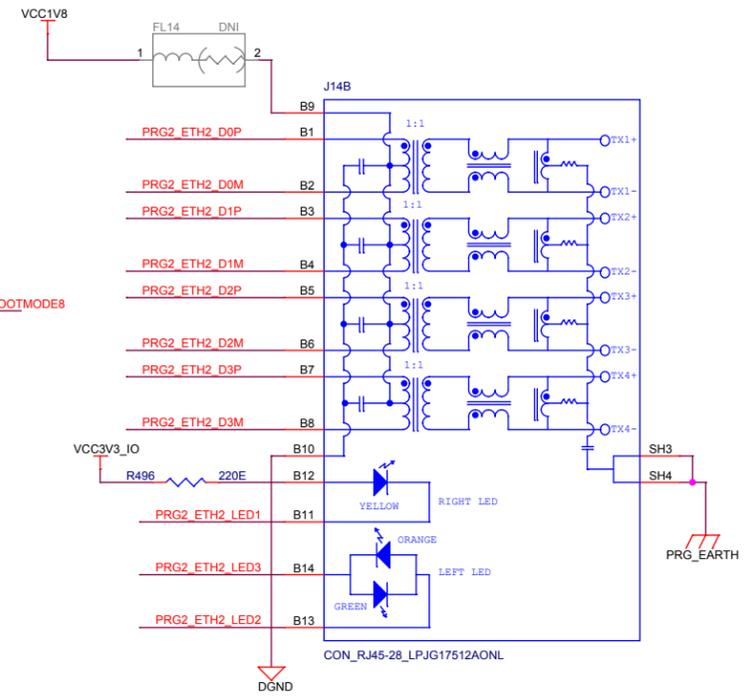
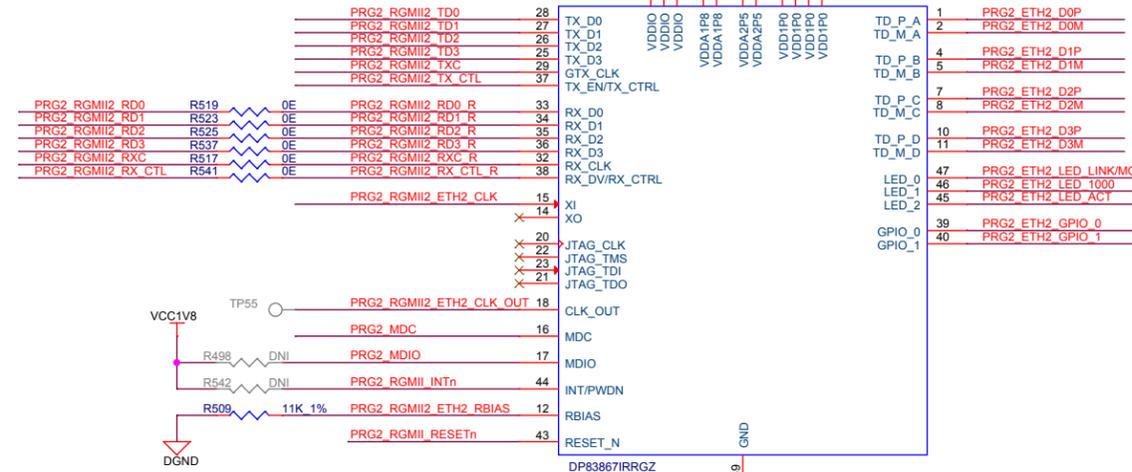
PRG2 RGMII 2



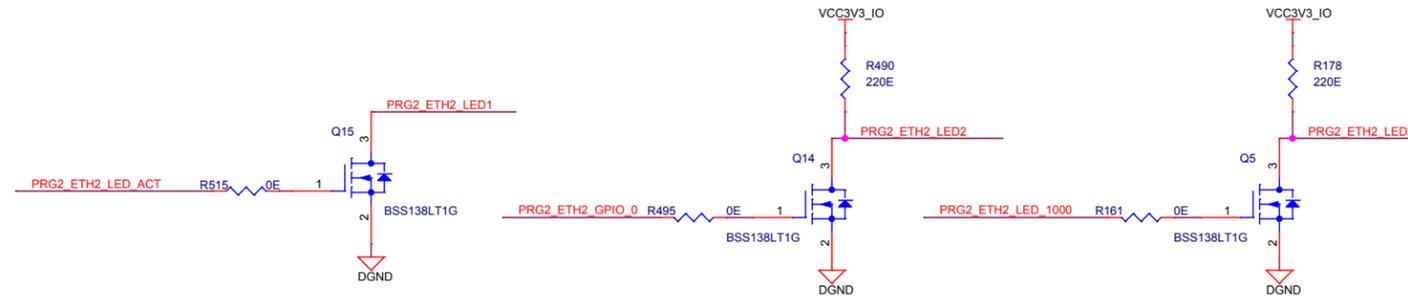
STRAPPING RESISTORS



PHY ADDRESS = 00011



PRG2_ETHERNET - 2 SPEED & ACTIVITY LED 'S DRIVERS



20	PRG2_RGMII_RESETn	PRG2_RGMII_RESETn
20,38	PRG2_RGMII_INTn	PRG2_RGMII_INTn
24,33	PRG2_ETH2_LED_LINK/MCUBOOTMODE8	PRG2_ETH2_LED_LINK/MCUBOOTMODE8
36	PRG2_RGMII2_ETH2_CLK	PRG2_RGMII2_ETH2_CLK
28	PRG2_RGMII2_TD0	PRG2_RGMII2_TD0
28	PRG2_RGMII2_TD1	PRG2_RGMII2_TD1
28	PRG2_RGMII2_TD2	PRG2_RGMII2_TD2
28	PRG2_RGMII2_TD3	PRG2_RGMII2_TD3
28	PRG2_RGMII2_TXC	PRG2_RGMII2_TXC
28	PRG2_RGMII2_TX_CTL	PRG2_RGMII2_TX_CTL
28	PRG2_RGMII2_RD0	PRG2_RGMII2_RD0
28	PRG2_RGMII2_RD1	PRG2_RGMII2_RD1
28	PRG2_RGMII2_RD2	PRG2_RGMII2_RD2
28	PRG2_RGMII2_RD3	PRG2_RGMII2_RD3
28	PRG2_RGMII2_RXC	PRG2_RGMII2_RXC
28	PRG2_RGMII2_RX_CTL	PRG2_RGMII2_RX_CTL
20,28,34	PRG2_MDIO	PRG2_MDIO
20,28,34	PRG2_MDC	PRG2_MDC

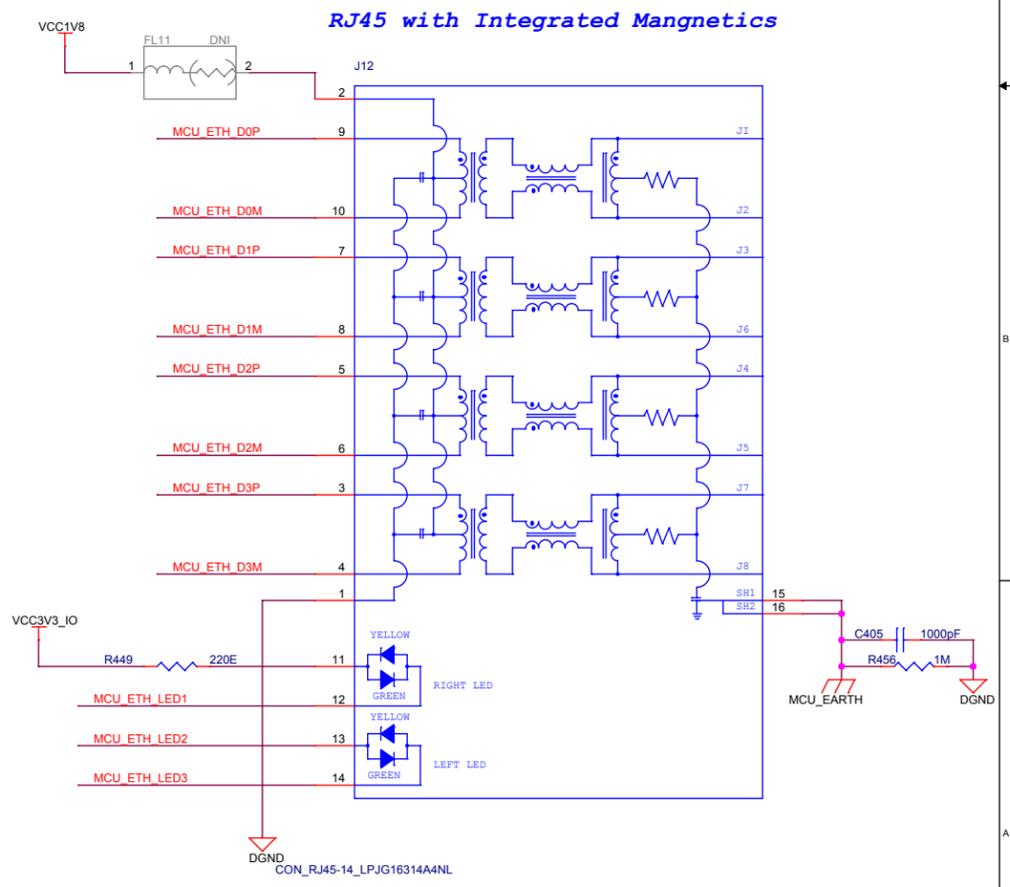
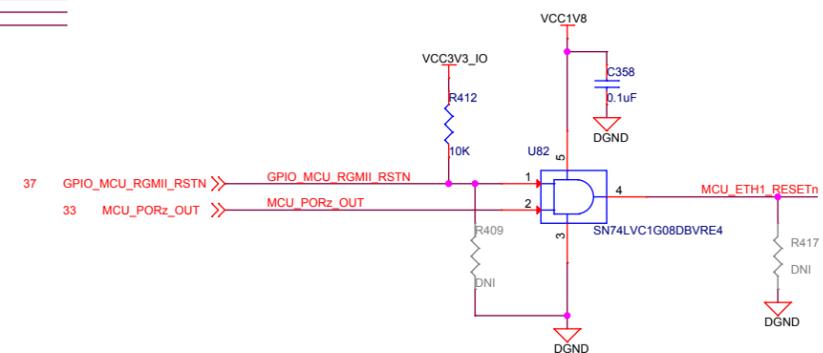
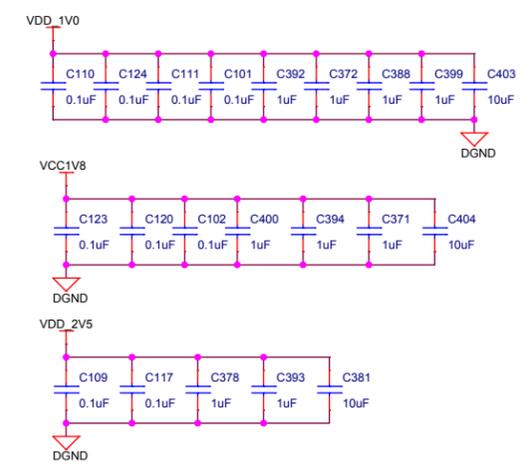
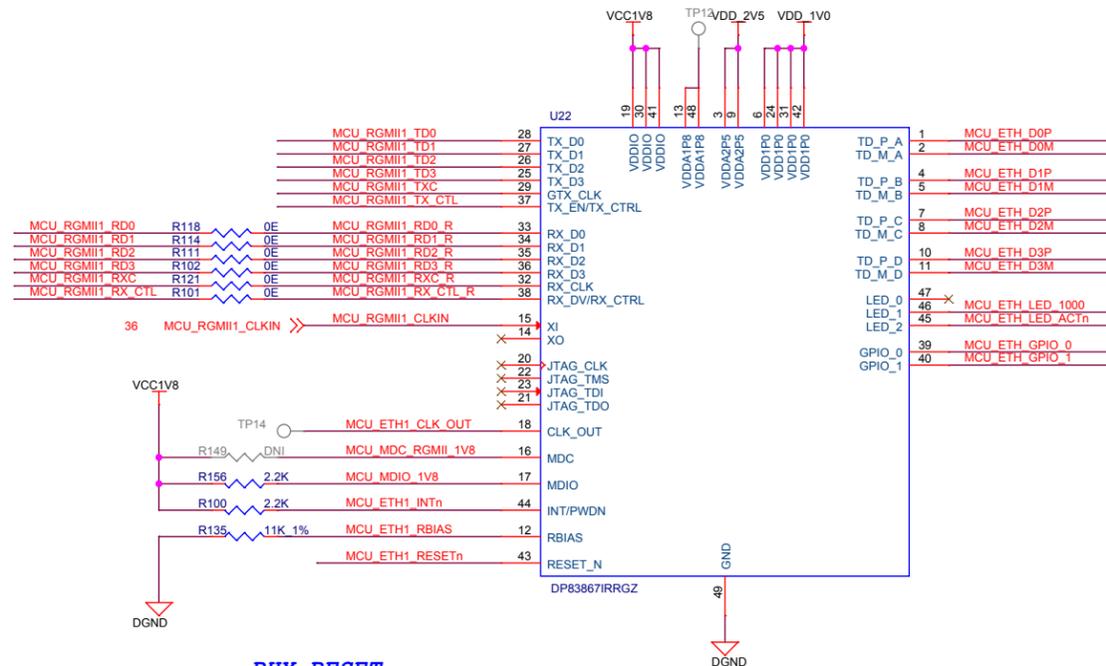
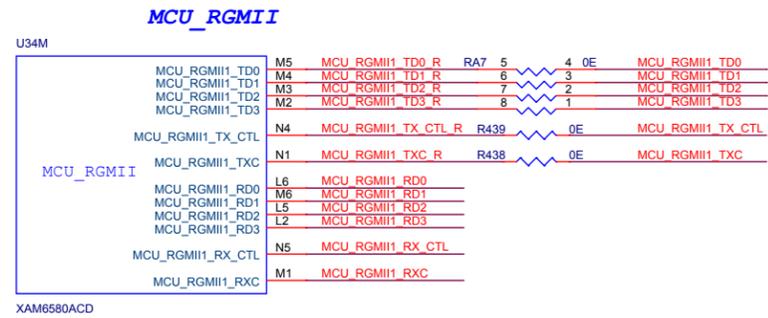
Designed for TI by Mistral Solutions Pvt Ltd



Title RGMII ETHERNET PHY - ICSSG PRG2_PRU1

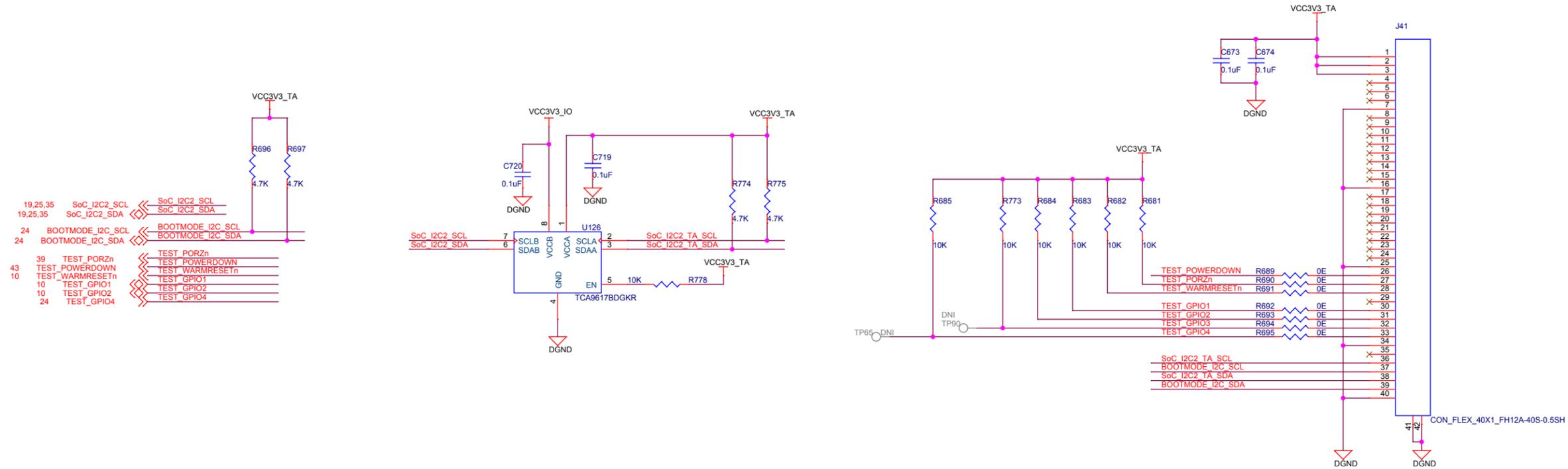
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev	E4
Date:	Thursday, August 29, 2019	Sheet	21 of 44

RGMII ETHERNET PHY - MCU



TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETrn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on WKUP_GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Used to Generate the interrupt on WKUP_GPIO0_27_INTn	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

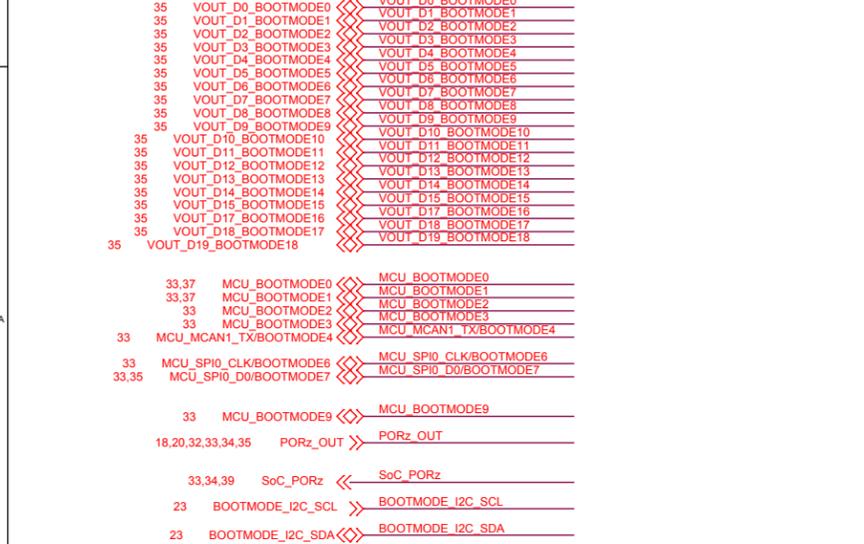
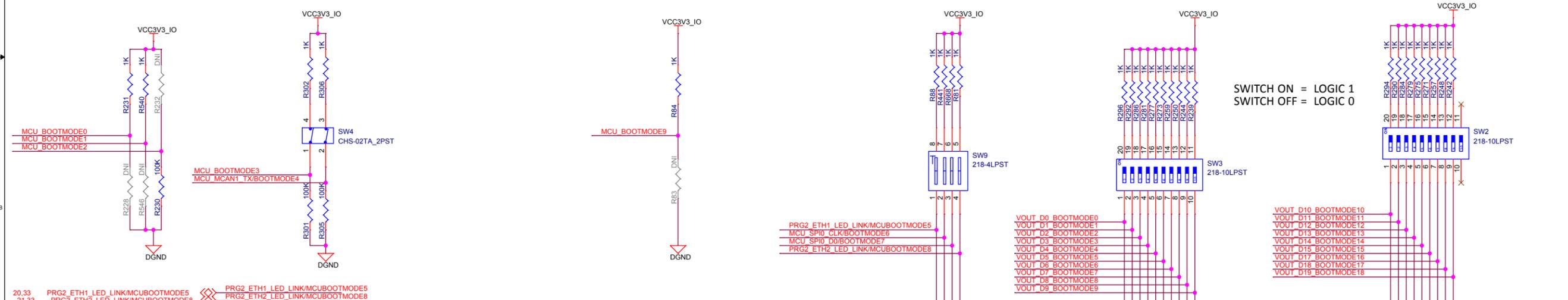
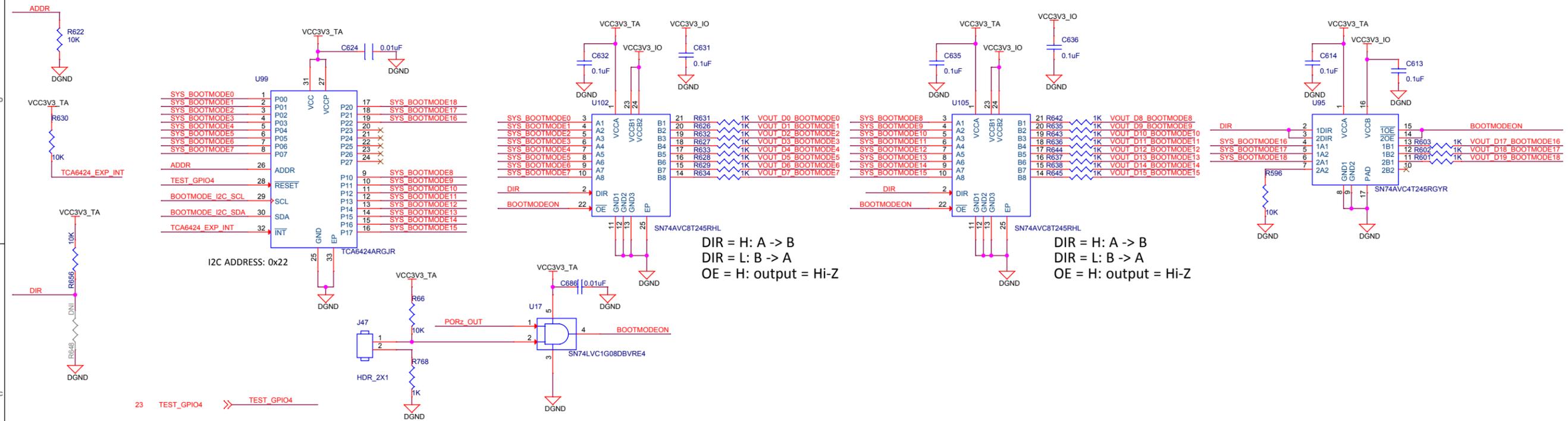
Designed for TI by Mistral Solutions Pvt Ltd



Title TEST AUTOMATION

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 23 of 44

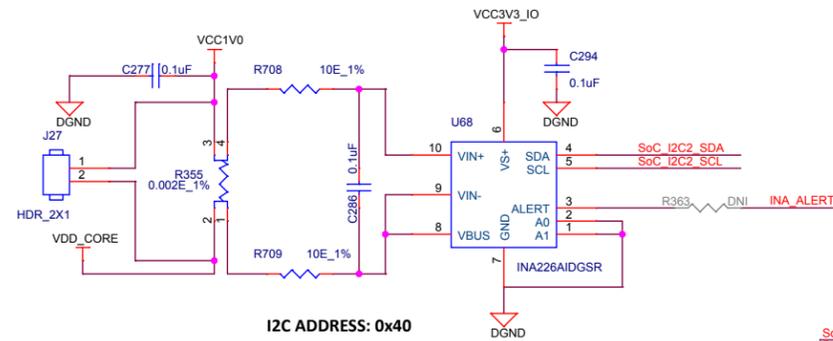
BOOT MODE BUFFER & SWITCHES



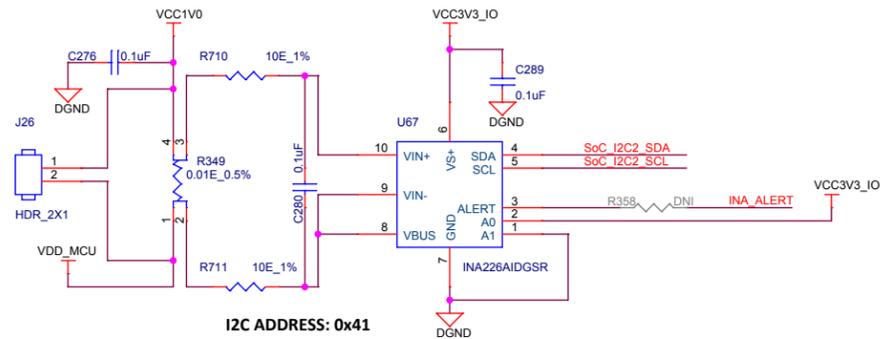
- ### BOOT MODES SUPPORTED
1. OSPI
 2. MMC1 - SD CARD
 3. MMC0 - eMMC
 4. PCIE (endpoint)
 5. CPSW Ethernet Slave
 6. USB Host
 7. USB Device

CURRENT MONITORING DEVICES

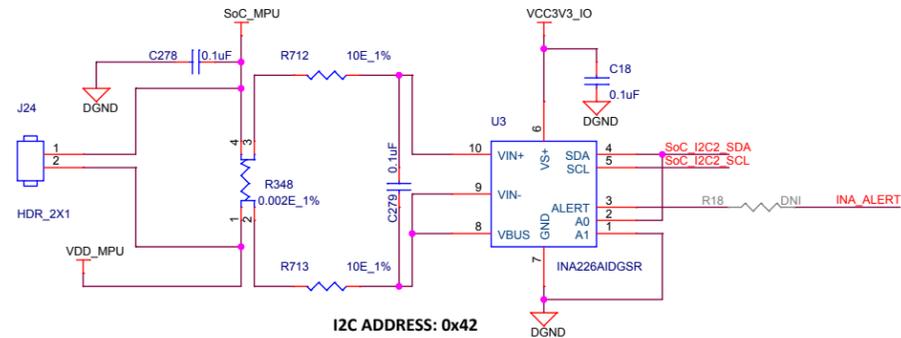
VDD_CORE



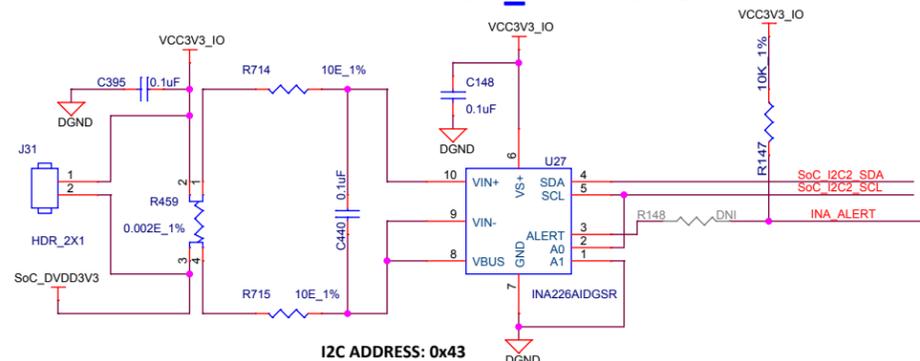
VDD_MCU



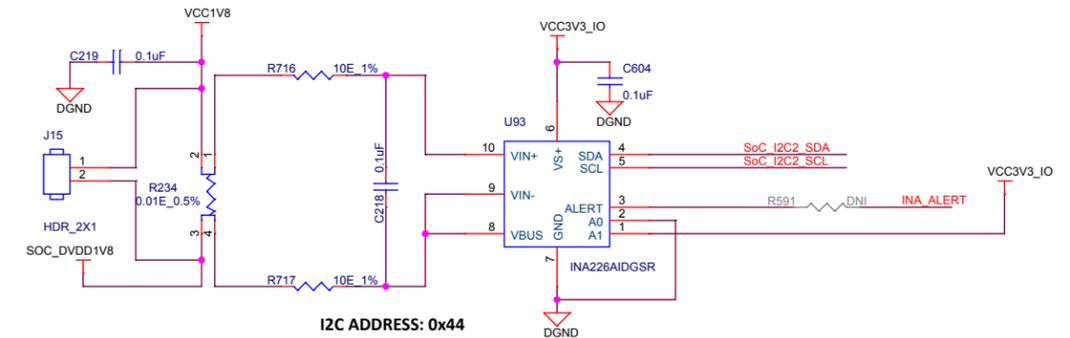
VDD_MPU



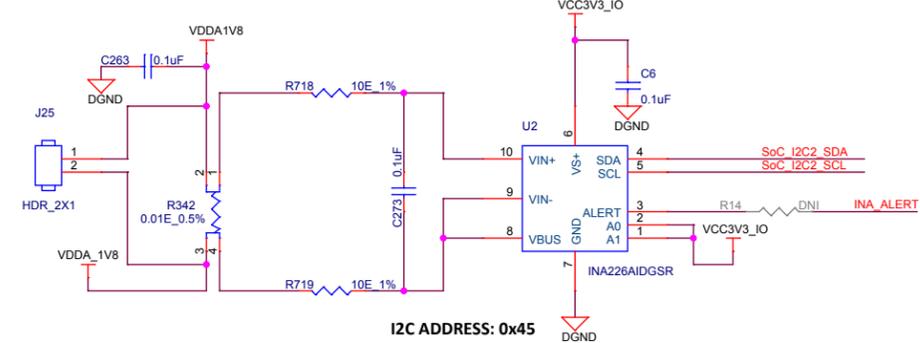
SoC_DVDD3V3



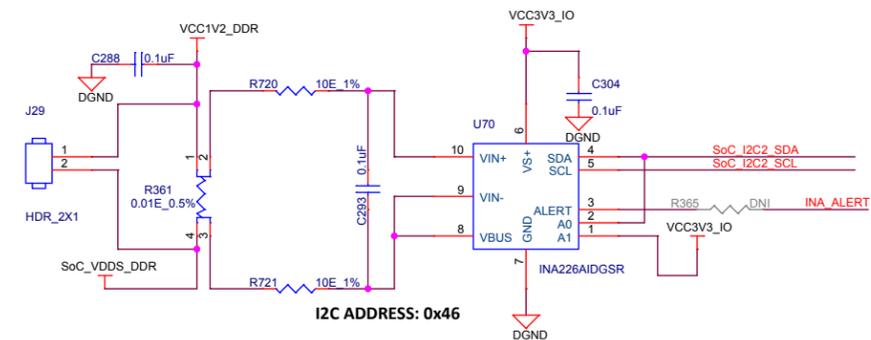
SoC_DVDD1V8



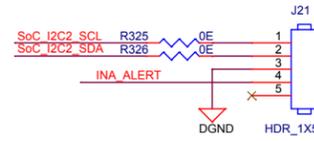
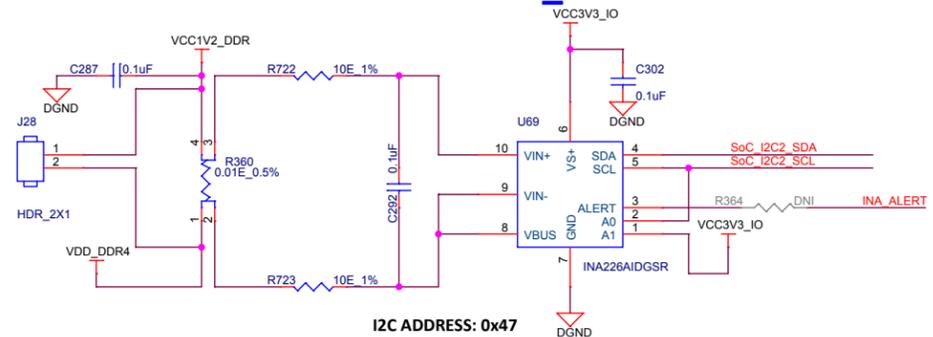
SoC_AVDD1V8



SoC_VDDS_DDR



VDD_DDR



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC1V0	VDD_CORE	40
VCC1V0	VDD_MCU	41
SoC_MPU	VDD_MPU	42
VCC3V3_IO	SoC_DVDD3V3	43
VCC1V8	SoC_DVDD1V8	44
VDDA1V8	SoC_AVDD1V8	45
VCC1V2_DDR	SoC_VDDS_DDR	46
VCC1V2_DDR	VDD_DDR	47

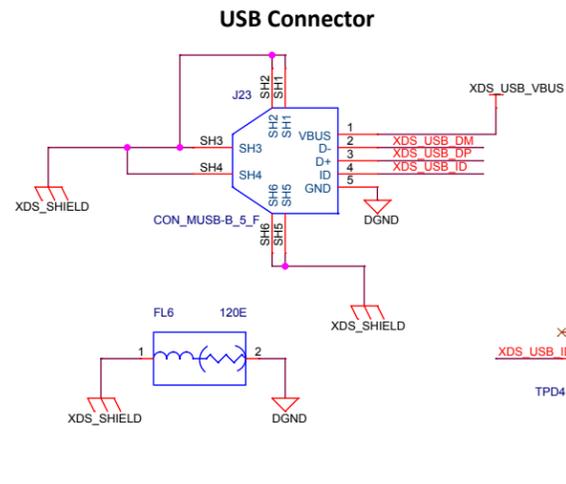


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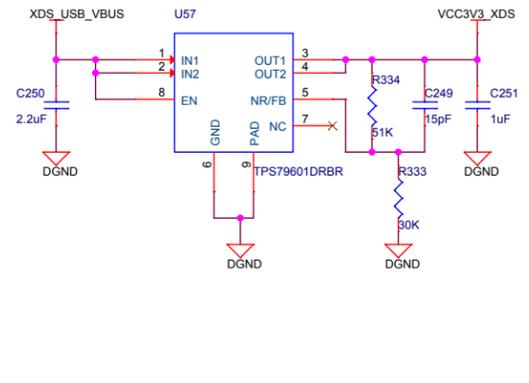


Title CURRENT MONITORING DEVICES

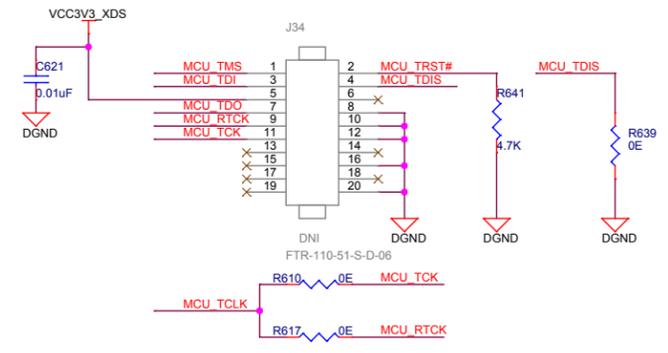
Size
C Variant Name = PROC082 001 OPN#TMDX654IDKEVM Rev E4
Date: Wednesday, August 28, 2019 Sheet 25 of 44



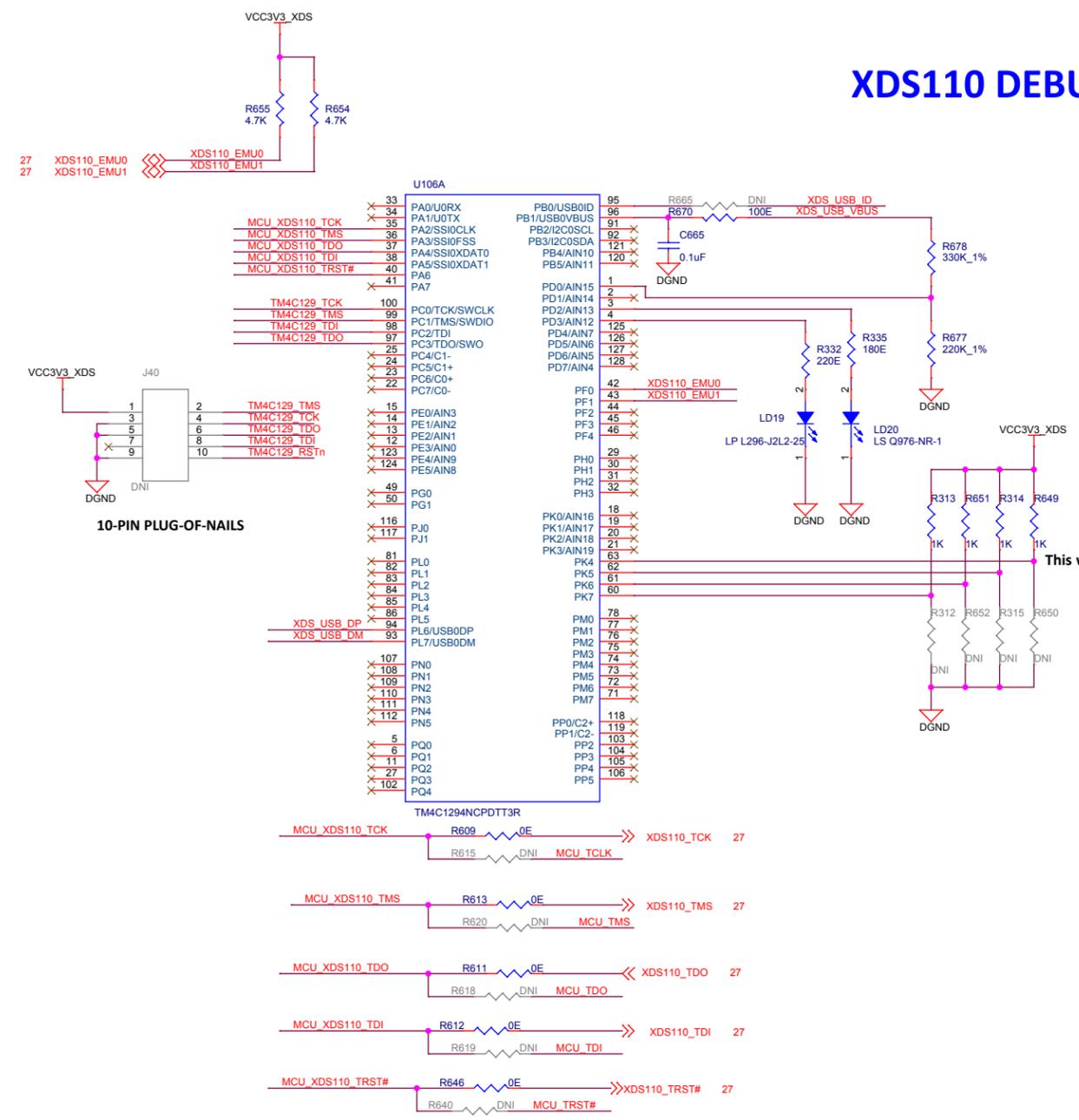
XDS110 POWER



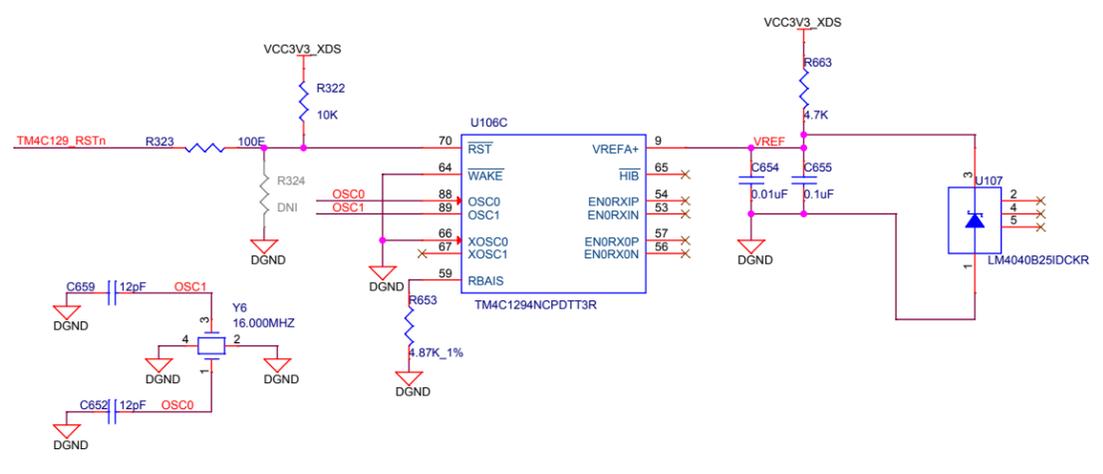
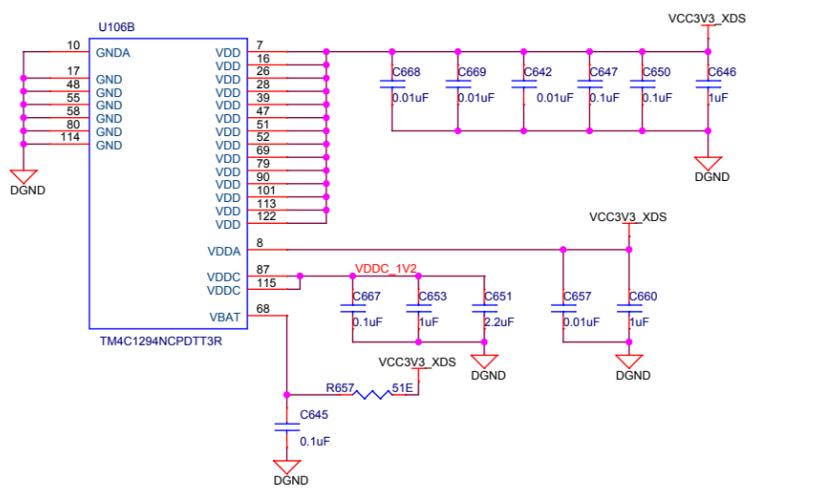
CTI 20 Pin Header external probe



XDS110 DEBUGGER



This will indicate the unique ID of the Debugger



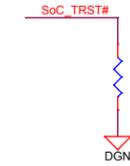
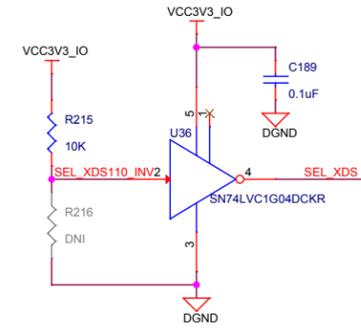
0- Ohm Res MUX between XDS110 JTAG and MCU cTI 20 pin connector.
 -For XDS110 JTAG R609,R613,R611,R612 and R646 Should be installed and R615,R620,R618,R619 and R640 Should be DNI'd.
 -For MCU cTI 20 pin , R615,R620,R618,R619 and R640 Should be Installed and R609,R613,R611,R612 and R646 Should be DNI'd.

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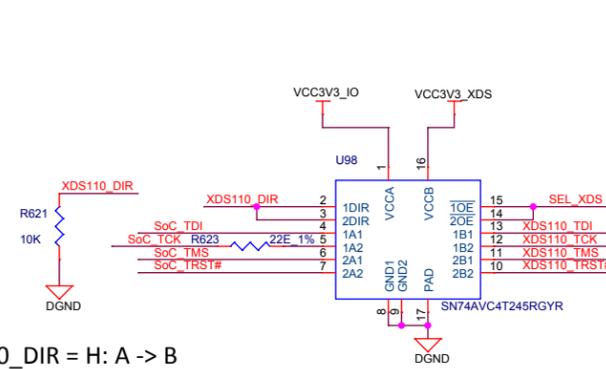
Title		XDS110 DEBUGGER
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 26 of 44

JTAG BUFFER

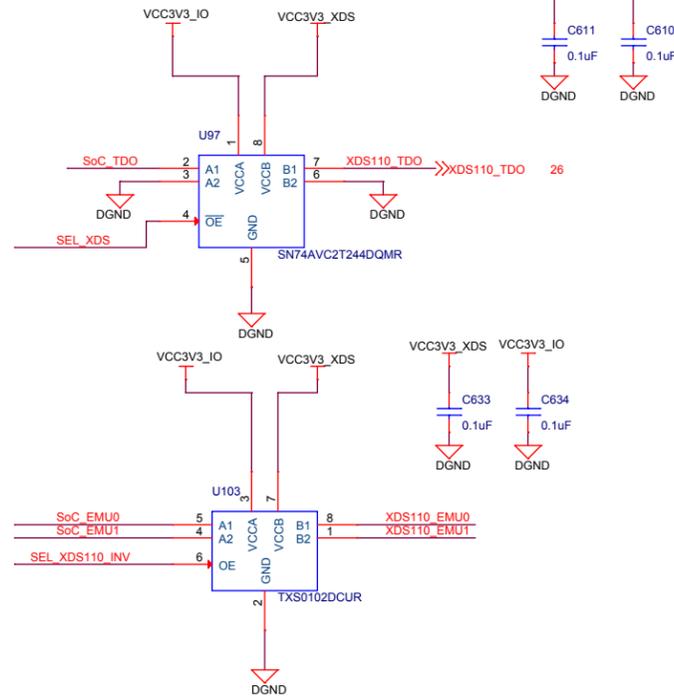


28	SEL_XDS110_INV	SEL_XDS110_INV
28	JTAG_EMU0	JTAG_EMU0
28	JTAG_EMU1	JTAG_EMU1
26	XDS110_TDI	XDS110_TDI
26	XDS110_TCK	XDS110_TCK
26	XDS110_TMS	XDS110_TMS
28	XDS110_TRST#	XDS110_TRST#
28	JTAG_TDI	JTAG_TDI
28	JTAG_TCK	JTAG_TCK
28	JTAG_TMS	JTAG_TMS
28	JTAG_TRST#	JTAG_TRST#
28	JTAG_TDO	JTAG_TDO
28	XDS110_EMU0	XDS110_EMU0
26	XDS110_EMU1	XDS110_EMU1
33	SoC_TDI	SoC_TDI
33	SoC_TDO	SoC_TDO
33	SoC_TMS	SoC_TMS
33	SoC_TCK	SoC_TCK
33	SoC_TRST#	SoC_TRST#
33	SoC_EMU1	SoC_EMU1
33	SoC_EMU0	SoC_EMU0

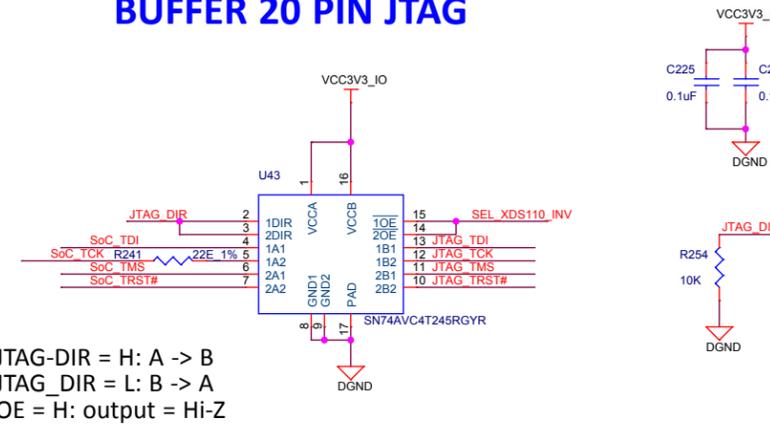
BUFFER XDS110



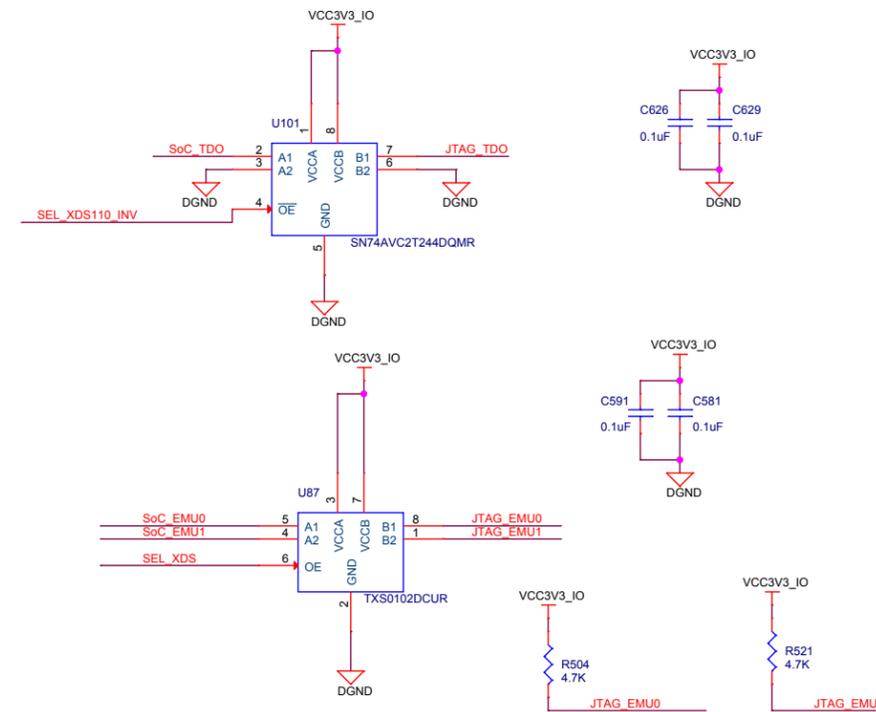
XDS110_DIR = H: A -> B
 XDS110_DIR = L: B -> A
 OE = H: output = Hi-Z



BUFFER 20 PIN JTAG



JTAG_DIR = H: A -> B
 JTAG_DIR = L: B -> A
 OE = H: output = Hi-Z



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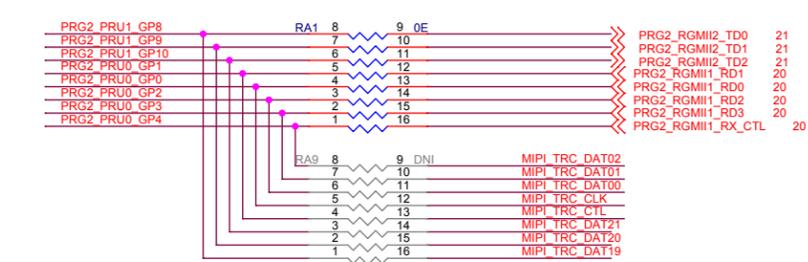
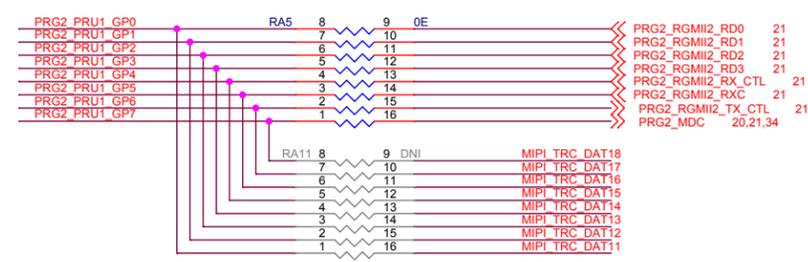
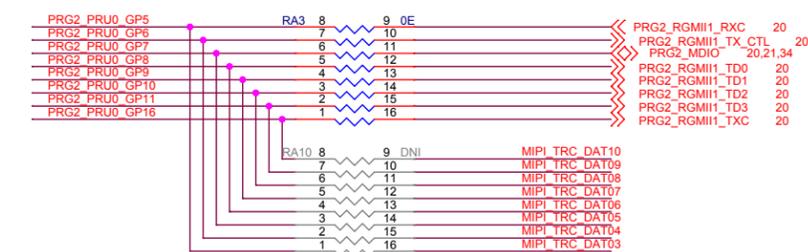
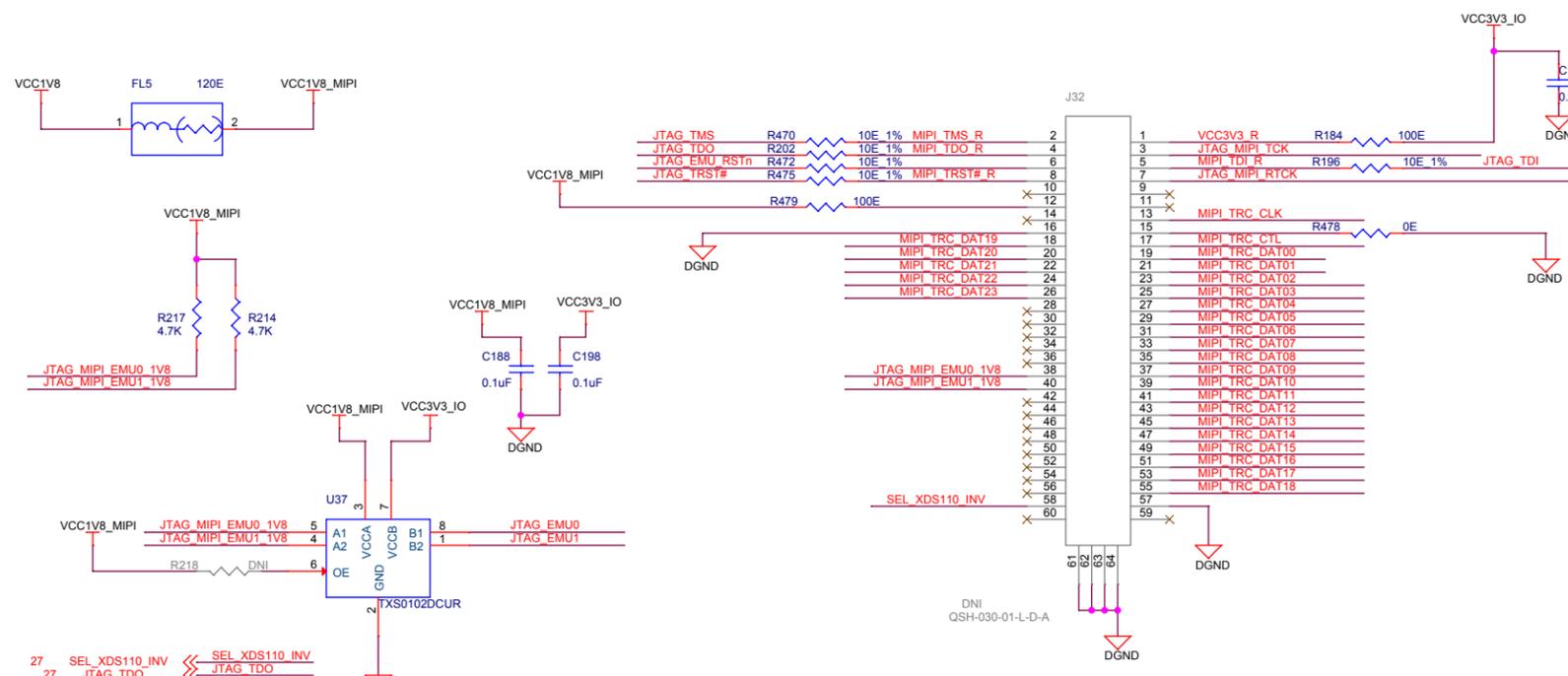


Title JTAG BUFFER

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 27 of 44

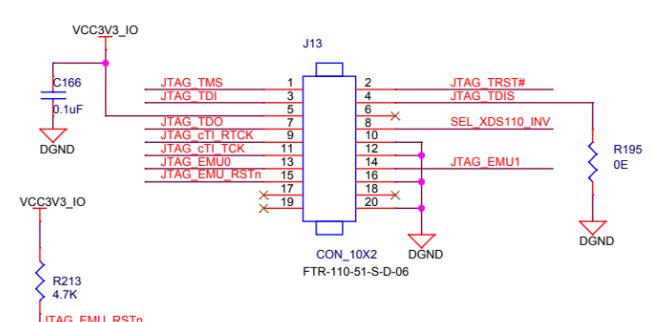
MIPI 60 PIN CONNECTOR

0- Ohm Res MUX between PRG2_Ethernet PHY (CP Board PHY) and JTAG TRACE Functionality
 -For PRG2_Ethernet PHY RA3, RA5, RA1, R180 & R183 Should be installed and RA10, RA11, RA9, R466 & R463 Should be DNI'd.
 -For TRACE RA10, RA11, RA9, R466 & R463 Should be Installed and RA3, RA5, RA1, R180 & R183 Should be DNI'd.

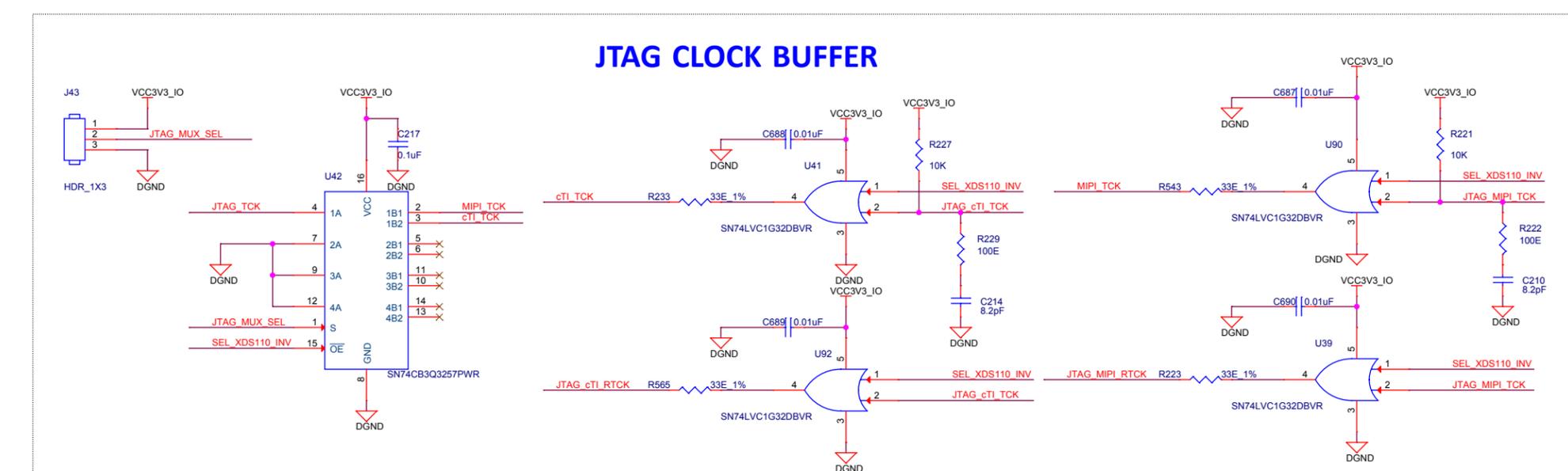


JTAG 20 PIN cTI CONNECTOR

27	SEL_XDS110_INV	SEL_XDS110_INV
27	JTAG_TDO	JTAG_TDO
27	JTAG_EMU0	JTAG_EMU0
27	JTAG_EMU1	JTAG_TDI
27	JTAG_TDI	JTAG_TCK
27	JTAG_TCK	JTAG_TMS
27	JTAG_TMS	JTAG_TRST#
27	JTAG_TRST#	JTAG_TRST#
20	PRG2_PRU0_GP0	PRG2_PRU0_GP0
20	PRG2_PRU0_GP1	PRG2_PRU0_GP1
20	PRG2_PRU0_GP2	PRG2_PRU0_GP2
20	PRG2_PRU0_GP3	PRG2_PRU0_GP3
20	PRG2_PRU0_GP4	PRG2_PRU0_GP4
20	PRG2_PRU0_GP5	PRG2_PRU0_GP5
20	PRG2_PRU0_GP6	PRG2_PRU0_GP6
20	PRG2_PRU0_GP7	PRG2_PRU0_GP7
20	PRG2_PRU0_GP8	PRG2_PRU0_GP8
20	PRG2_PRU0_GP9	PRG2_PRU0_GP9
20	PRG2_PRU0_GP10	PRG2_PRU0_GP10
20	PRG2_PRU0_GP11	PRG2_PRU0_GP11
20	PRG2_PRU0_GP16	PRG2_PRU0_GP16
20	PRG2_PRU1_GP0	PRG2_PRU1_GP0
20	PRG2_PRU1_GP1	PRG2_PRU1_GP1
20	PRG2_PRU1_GP2	PRG2_PRU1_GP2
20	PRG2_PRU1_GP3	PRG2_PRU1_GP3
20	PRG2_PRU1_GP4	PRG2_PRU1_GP4
20	PRG2_PRU1_GP5	PRG2_PRU1_GP5
20	PRG2_PRU1_GP6	PRG2_PRU1_GP6
20	PRG2_PRU1_GP7	PRG2_PRU1_GP7
20	PRG2_PRU1_GP8	PRG2_PRU1_GP8
20	PRG2_PRU1_GP9	PRG2_PRU1_GP9
20	PRG2_PRU1_GP10	PRG2_PRU1_GP10
20	PRG2_PRU1_GP11	PRG2_PRU1_GP11
20	PRG2_PRU1_GP16	PRG2_PRU1_GP16
39	JTAG_EMU_RSTn	JTAG_EMU_RSTn



JTAG CLOCK BUFFER

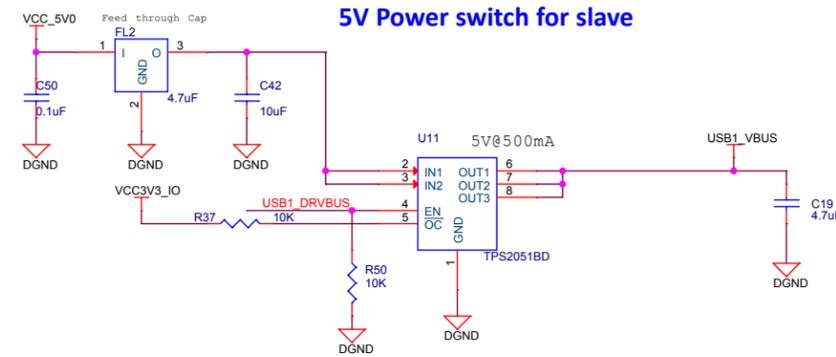
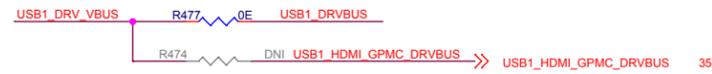
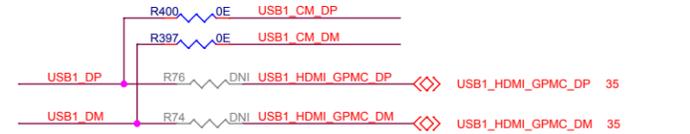
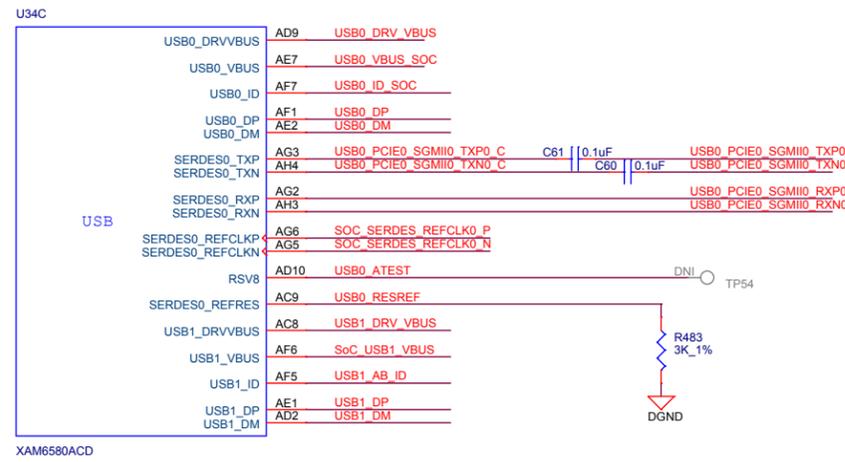


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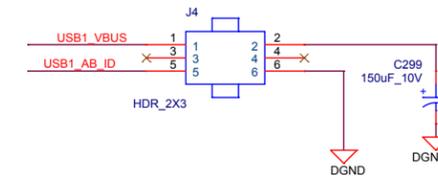


Title			MIPI 60 PIN CONNECTOR
Size	Variant Name = PROC082 001 OP#FTMDX654IDKEVM		Rev
C			E4
Date:	Monday, September 30, 2019	Sheet	28 of 44

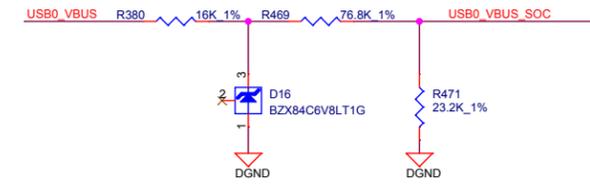
USB 2.0 INTERFACE



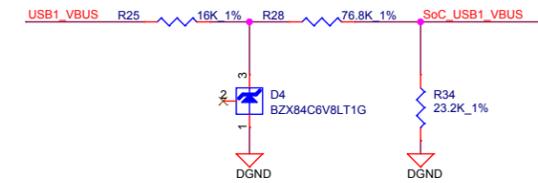
2X3 header to enable bulk capacitance on USB1_VBUS in host mode and to ground USB_AB_ID pin, if a non standard cable is used



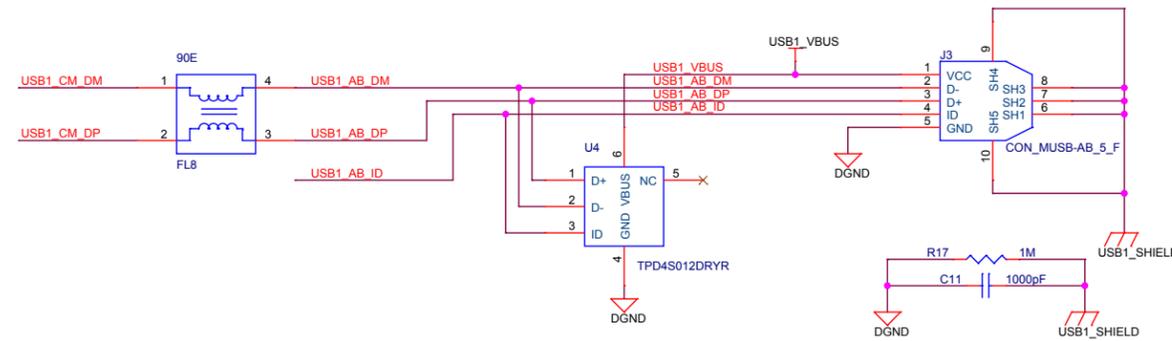
Resistor divider on SOC_VBUS



Resistor divider on SOC_VBUS



Micro USB 2.0 AB Connector



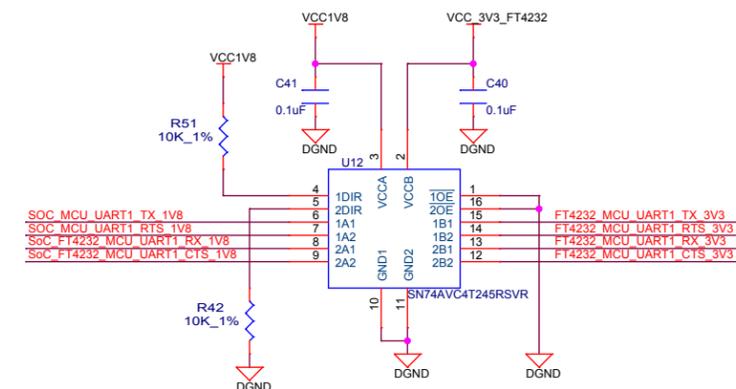
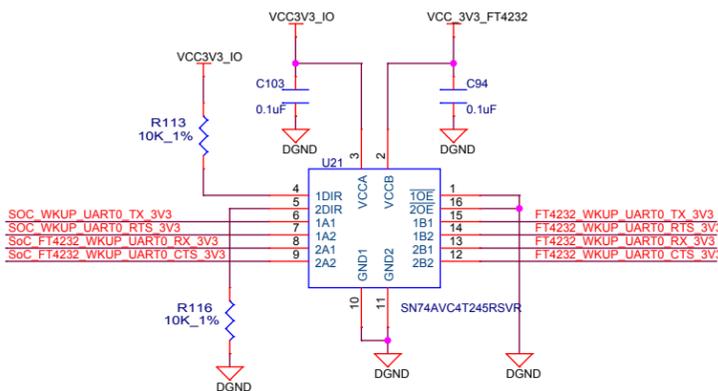
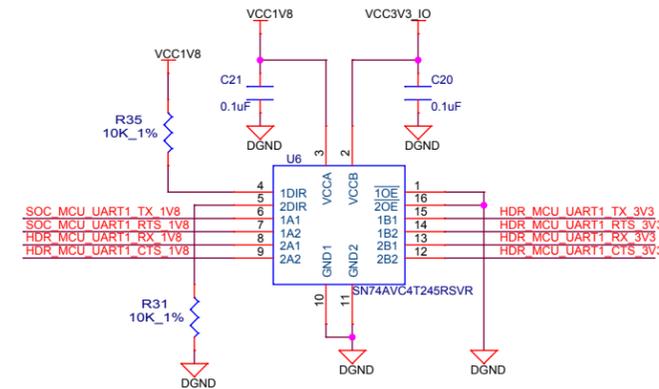
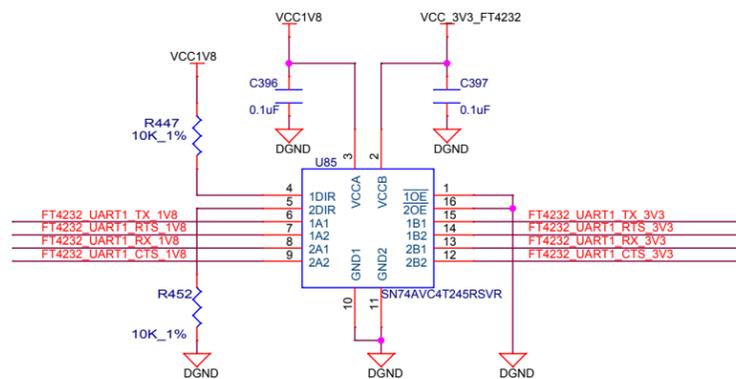
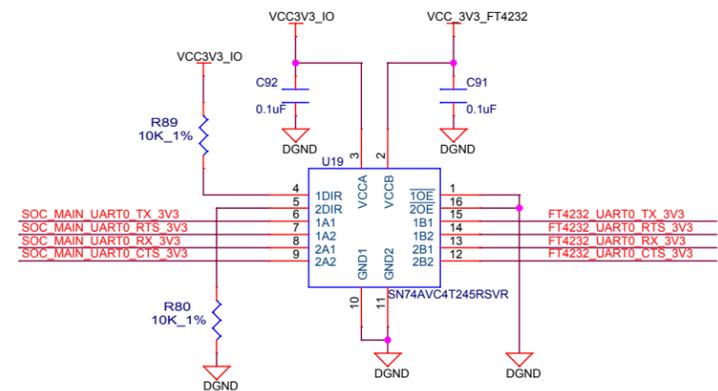
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Title: USB 2.0 INTERFACE

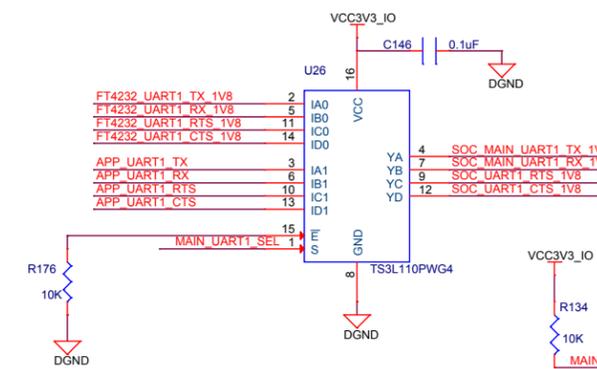
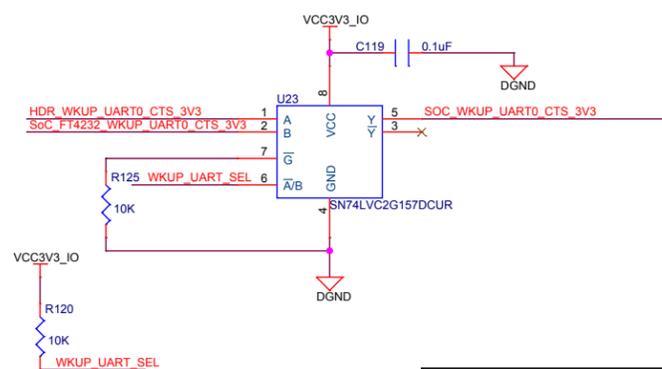
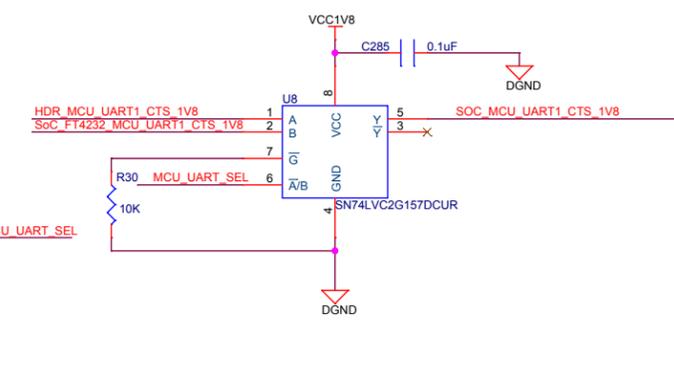
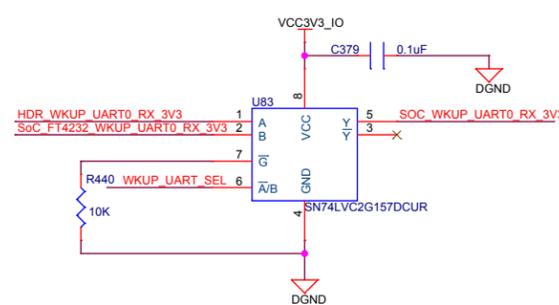
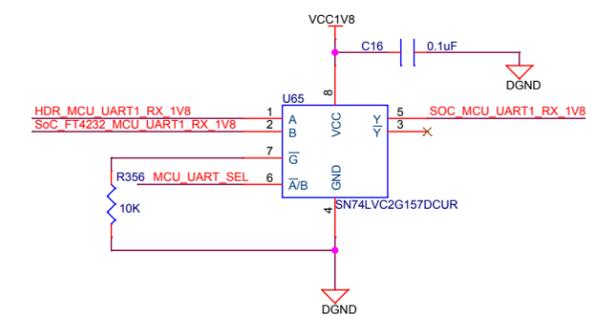
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 29 of 44

FT4232 LEVEL TRANSLATOR



MCU_UART_SEL	<<	MCU_UART_SEL	37
WKUP_UART_SEL	<<	WKUP_UART_SEL	37
MAIN_UART1_SEL	<<	MAIN_UART1_SEL	37
SOC_MAIN_UART0_RX_3V3	<<	SOC_MAIN_UART0_RX_3V3	33
SOC_MAIN_UART0_TX_3V3	<<	SOC_MAIN_UART0_TX_3V3	33
SOC_MAIN_UART0_RTS_3V3	<<	SOC_MAIN_UART0_RTS_3V3	33
SOC_MAIN_UART0_CTS_3V3	<<	SOC_MAIN_UART0_CTS_3V3	33
SOC_WKUP_UART0_RX_3V3	<<	SOC_WKUP_UART0_RX_3V3	33
SOC_WKUP_UART0_TX_3V3	<<	SOC_WKUP_UART0_TX_3V3	33,38
SOC_WKUP_UART0_RTS_3V3	<<	SOC_WKUP_UART0_RTS_3V3	33,38
SOC_WKUP_UART0_CTS_3V3	<<	SOC_WKUP_UART0_CTS_3V3	33,38
SOC_MCU_UART1_RX_1V8	<<	SOC_MCU_UART1_RX_1V8	18
SOC_MCU_UART1_TX_1V8	<<	SOC_MCU_UART1_TX_1V8	18
SOC_MCU_UART1_RTS_1V8	<<	SOC_MCU_UART1_RTS_1V8	18
SOC_MCU_UART1_CTS_1V8	<<	SOC_MCU_UART1_CTS_1V8	18
SOC_MAIN_UART1_RX_1V8	<<	SOC_MAIN_UART1_RX_1V8	32
SOC_MAIN_UART1_TX_1V8	<<	SOC_MAIN_UART1_TX_1V8	32
SOC_UART1_RTS_1V8	<<	SOC_UART1_RTS_1V8	32
SOC_UART1_CTS_1V8	<<	SOC_UART1_CTS_1V8	32
APP_UART1_CTS	<<	APP_UART1_CTS	32
APP_UART1_RTS	<<	APP_UART1_RTS	32
APP_UART1_RX	<<	APP_UART1_RX	32
APP_UART1_TX	<<	APP_UART1_TX	32
HDR_MCU_UART1_RTS_3V3	<<	HDR_MCU_UART1_RTS_3V3	38
HDR_MCU_UART1_CTS_3V3	<<	HDR_MCU_UART1_CTS_3V3	38
HDR_MCU_UART1_TX_3V3	<<	HDR_MCU_UART1_TX_3V3	38
HDR_MCU_UART1_RX_3V3	<<	HDR_MCU_UART1_RX_3V3	38
HDR_WKUP_UART0_RX_3V3	<<	HDR_WKUP_UART0_RX_3V3	38
HDR_WKUP_UART0_CTS_3V3	<<	HDR_WKUP_UART0_CTS_3V3	38
FT4232_UART0_TX_3V3	<<	FT4232_UART0_TX_3V3	31
FT4232_UART0_RTS_3V3	<<	FT4232_UART0_RTS_3V3	31
FT4232_UART0_RX_3V3	<<	FT4232_UART0_RX_3V3	31
FT4232_UART0_CTS_3V3	<<	FT4232_UART0_CTS_3V3	31
FT4232_UART1_TX_3V3	<<	FT4232_UART1_TX_3V3	31
FT4232_UART1_RTS_3V3	<<	FT4232_UART1_RTS_3V3	31
FT4232_UART1_RX_3V3	<<	FT4232_UART1_RX_3V3	31
FT4232_UART1_CTS_3V3	<<	FT4232_UART1_CTS_3V3	31
FT4232_WKUP_UART0_TX_3V3	<<	FT4232_WKUP_UART0_TX_3V3	31
FT4232_WKUP_UART0_RTS_3V3	<<	FT4232_WKUP_UART0_RTS_3V3	31
FT4232_WKUP_UART0_RX_3V3	<<	FT4232_WKUP_UART0_RX_3V3	31
FT4232_WKUP_UART0_CTS_3V3	<<	FT4232_WKUP_UART0_CTS_3V3	31
FT4232_MCU_UART1_TX_3V3	<<	FT4232_MCU_UART1_TX_3V3	31
FT4232_MCU_UART1_RTS_3V3	<<	FT4232_MCU_UART1_RTS_3V3	31
FT4232_MCU_UART1_RX_3V3	<<	FT4232_MCU_UART1_RX_3V3	31
FT4232_MCU_UART1_CTS_3V3	<<	FT4232_MCU_UART1_CTS_3V3	31

2:1 MUX

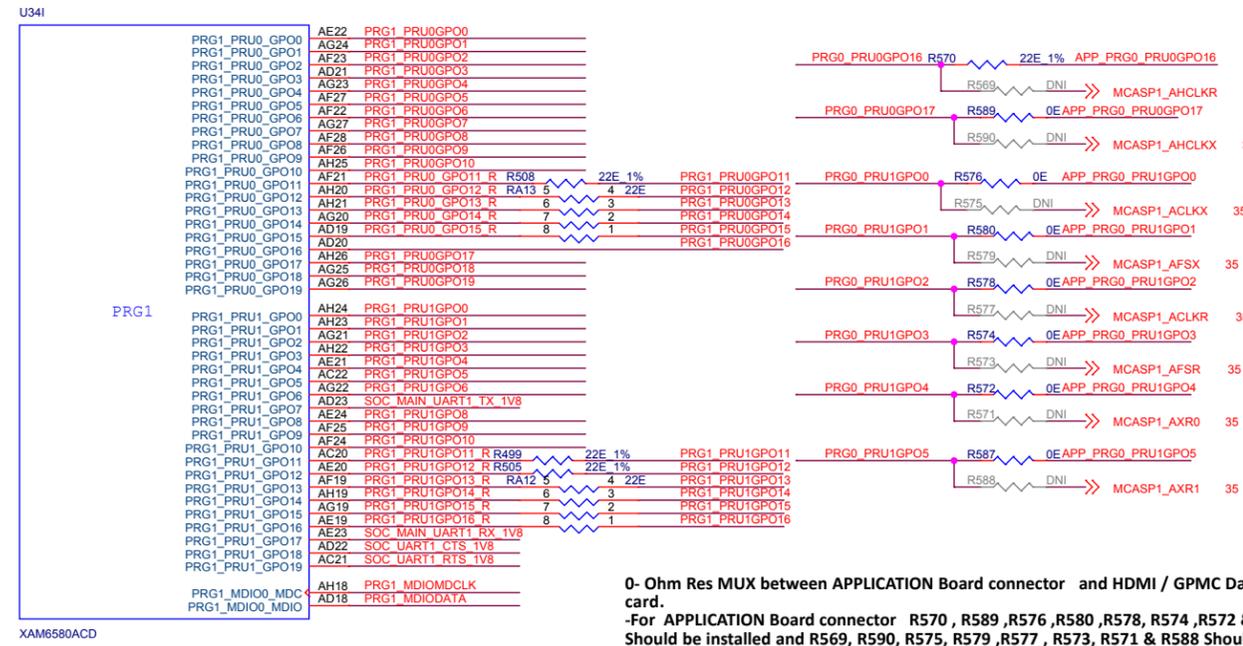
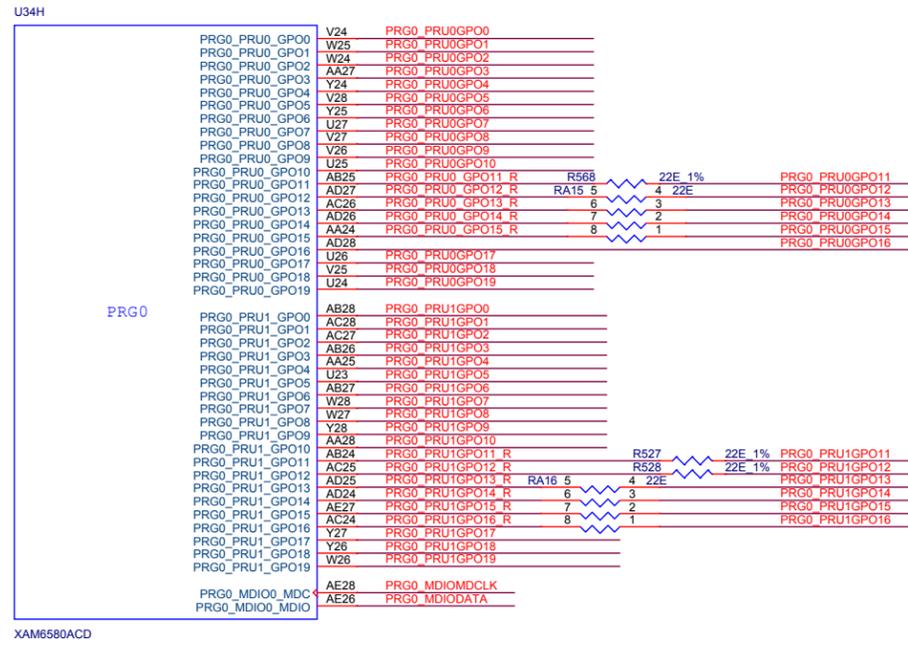


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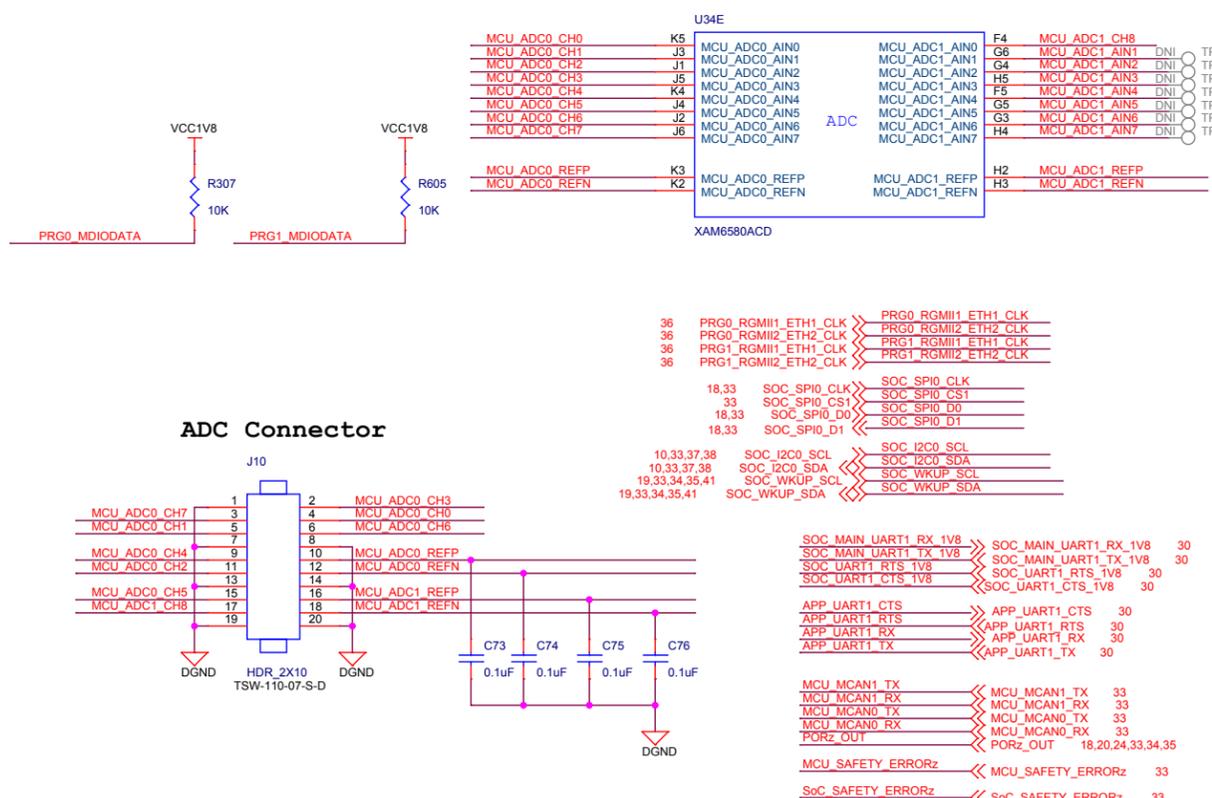
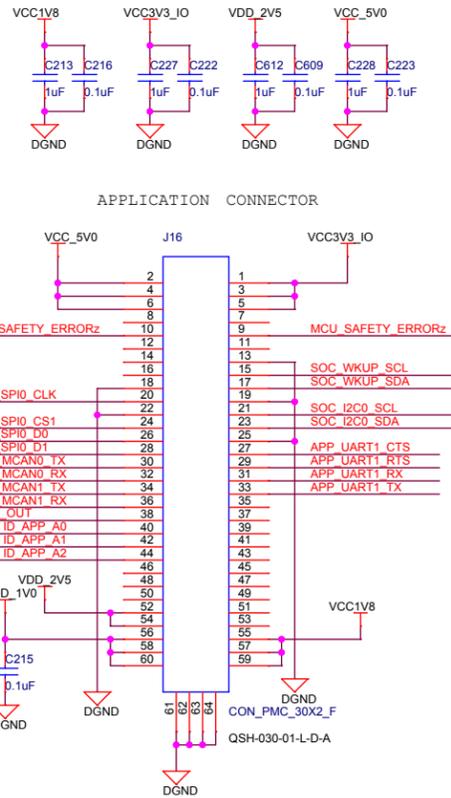
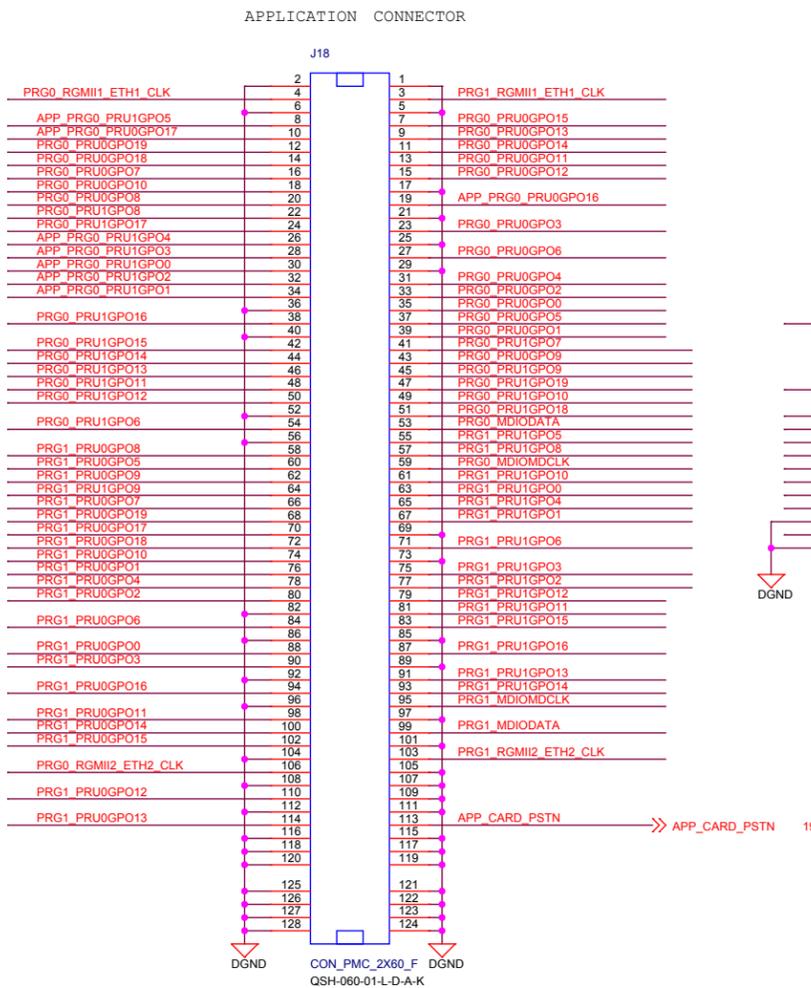
Title		FT4232 LEVEL TRANSLATOR
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E4
Date:	Wednesday, August 28, 2019	Sheet 30 of 44

APPLICATION BOARD INTERFACE



0- Ohm Res MUX between APPLICATION Board connector and HDMI / GPMC Daughter card.
 -For APPLICATION Board connector R570, R589, R576, R580, R578, R574, R572 & R587 Should be installed and R569, R590, R575, R579, R577, R573, R571 & R588 Should be DNI'd.
 -For HDMI / GPMC Daughter card R569, R590, R575, R579, R577, R573, R571 & R588 Should be installed and R570, R589, R576, R580, R578, R574, R572 & R587 should be DNI'd.

APPLICATION BOARD CONNECTORS

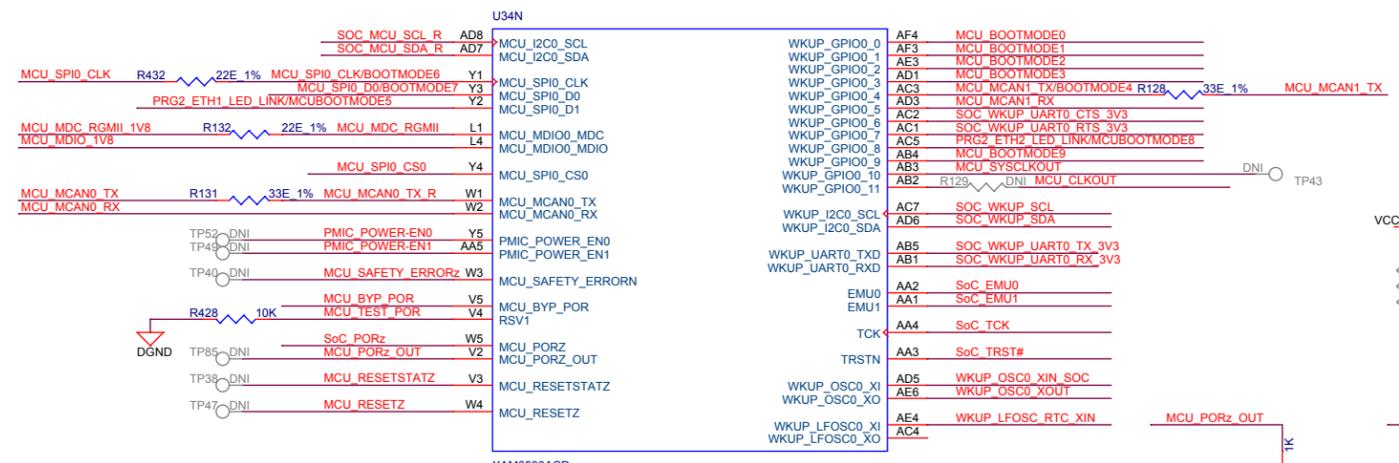
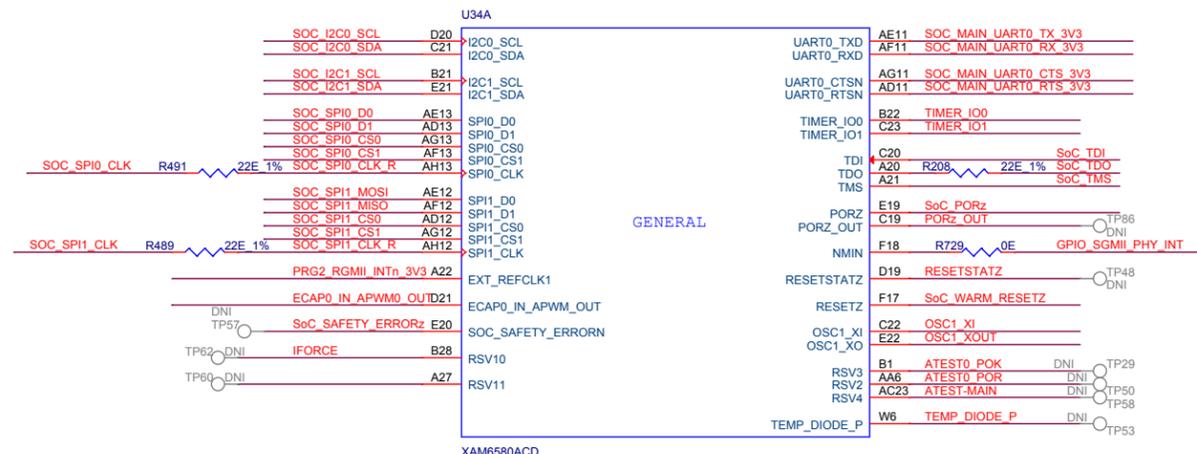


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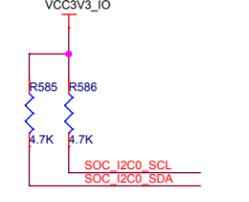
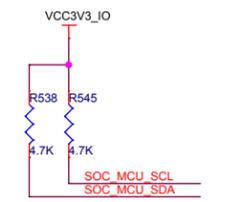
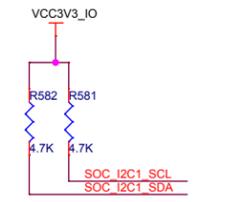


Title		APPLICATION BOARD CONNECTOR
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E4
Date:	Wednesday, August 28, 2019	Sheet 32 of 44

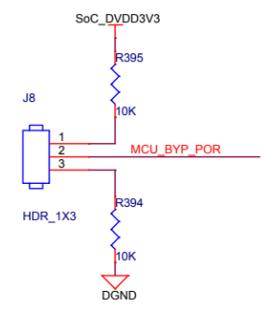
GENERAL & MCU_GENERAL



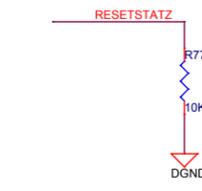
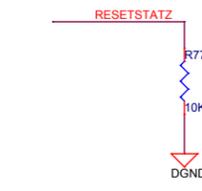
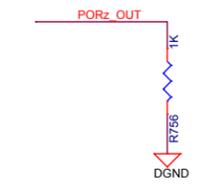
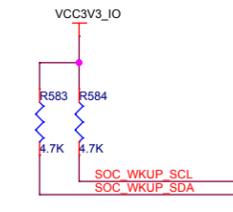
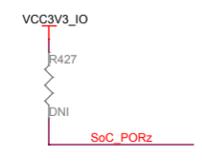
SOC_I2C1_SCL	DNI	TP67
SOC_I2C1_SDA	DNI	TP68
SOC_MCU_SCL	DNI	TP69
SOC_MCU_SDA	DNI	TP70
SOC_WKUP_SCL	DNI	TP71
SOC_WKUP_SDA	DNI	TP72



Jumper to select Internal PORz & External PORz



To Disable the Internal PORz ,
Connect the Jumper between Pin no 1 & 2 of J8.
To Enable the Internal PORz,
Connect the Jumper between Pin no 2 & 3 of J8

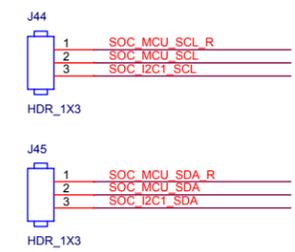


MCU_MDC_RGMII_1V8	MCU_MDC_RGMII_1V8	22
MCU_MDI0_1V8	MCU_MDI0_1V8	22
OSC1_XI	OSC1_XI	10
OSC1_XOUT	OSC1_XOUT	10
SoC_PORz	SoC_PORz	34,39
SoC_WARM_RESETZ	SoC_WARM_RESETZ	10
SOC_I2C1_SCL	SOC_I2C1_SCL	34
SOC_I2C1_SDA	SOC_I2C1_SDA	34
SOC_MCU_SCL	SOC_MCU_SCL	19,34,35
SOC_MCU_SDA	SOC_MCU_SDA	19,34,35
MCU_MCAN1_TX	MCU_MCAN1_TX	32
MCU_MCAN1_RX	MCU_MCAN1_RX	32
MCU_MCAN0_TX	MCU_MCAN0_TX	32
MCU_MCAN0_RX	MCU_MCAN0_RX	32
SoC_TDI	SoC_TDI	27
SoC_TDO	SoC_TDO	27
SoC_TMS	SoC_TMS	27
SoC_TCK	SoC_TCK	27
SoC_TRST#	SoC_TRST#	27
SoC_EMU1	SoC_EMU1	27
SoC_EMU0	SoC_EMU0	27
GPIO_MCU_RGMII_RSTN	GPIO_MCU_RGMII_RSTN	22,37
SOC_I2C0_SCL	SOC_I2C0_SCL	10,32,37,38
SOC_I2C0_SDA	SOC_I2C0_SDA	10,32,37,38
RESETSTATZ	RESETSTATZ	17

PRG2_RGMII_INTn_3V3	PRG2_RGMII_INTn_3V3	38
TIMER_I00	TIMER_I00	38
TIMER_I01	TIMER_I01	38
MCU_SPIO_CS0	MCU_SPIO_CS0	35
SOC_WKUP_UART0_TX_3V3	MCU_SPIO_CS0	35
SOC_WKUP_UART0_RX_3V3	SOC_WKUP_UART0_TX_3V3	30,38
SOC_WKUP_UART0_CTS_3V3	SOC_WKUP_UART0_CTS_3V3	30
SOC_WKUP_UART0_RTS_3V3	SOC_WKUP_UART0_RTS_3V3	30,38
SOC_WKUP_SCL	SOC_WKUP_SCL	19,32,34,35,41
SOC_WKUP_SDA	SOC_WKUP_SDA	19,32,34,35,41
PORz_OUT	PORz_OUT	18,20,24,32,34,35
MCU_PORz_OUT	MCU_PORz_OUT	22
GPIO_SGMII_PHY_INT	GPIO_SGMII_PHY_INT	34
ECAP0_IN_APWM0_OUT	ECAP0_IN_APWM0_OUT	34
SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	30
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	30
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	30
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	30
SOC_SPI1_CLK	SOC_SPI1_CLK	34,35,38
SOC_SPI1_MOSI	SOC_SPI1_MOSI	34,35,38
SOC_SPI1_MISO	SOC_SPI1_MISO	34,35,38
SOC_SPI1_CS0	SOC_SPI1_CS0	34,38
SOC_SPI1_CS1	SOC_SPI1_CS1	35,38
MCU_SAFETY_ERRORz	MCU_SAFETY_ERRORz	32
SoC_SAFETY_ERRORz	SoC_SAFETY_ERRORz	32

MCU_BOOTMODE0	MCU_BOOTMODE0	24,37
MCU_BOOTMODE1	MCU_BOOTMODE1	24,37
MCU_BOOTMODE2	MCU_BOOTMODE2	24
MCU_BOOTMODE3	MCU_BOOTMODE3	24
MCU_MCAN1_TX/BOOTMODE4	MCU_MCAN1_TX/BOOTMODE4	24
MCU_SPIO_CLK/BOOTMODE6	MCU_SPIO_CLK/BOOTMODE6	24
MCU_SPIO_D0/BOOTMODE7	MCU_SPIO_D0/BOOTMODE7	24,35
MCU_BOOTMODE9	MCU_BOOTMODE9	24
MCU_CLKOUT	MCU_CLKOUT	36
WKUP_OSC0_XIN_SOC	WKUP_OSC0_XIN_SOC	10
WKUP_OSC0_XOUT	WKUP_OSC0_XOUT	10
WKUP_LFOSC_RTC_XIN	WKUP_LFOSC_RTC_XIN	10
MCU_SPIO_CLK	MCU_SPIO_CLK	35
SOC_SPIO_CS1	SOC_SPIO_CS1	32
SOC_SPIO_CLK	SOC_SPIO_CLK	18,32,33
SOC_SPIO_CS0	SOC_SPIO_CS0	18
SOC_SPIO_D0	SOC_SPIO_D0	18,32
SOC_SPIO_D1	SOC_SPIO_D1	18,32
PRG2_ETH2_LED_LINK/MCUBOOTMODE8	PRG2_ETH2_LED_LINK/MCUBOOTMODE8	21,24
PRG2_ETH1_LED_LINK/MCUBOOTMODE5	PRG2_ETH1_LED_LINK/MCUBOOTMODE5	20,24

Jumper option to connect the peripherals connected on MCU_I2C to SoC I2C1

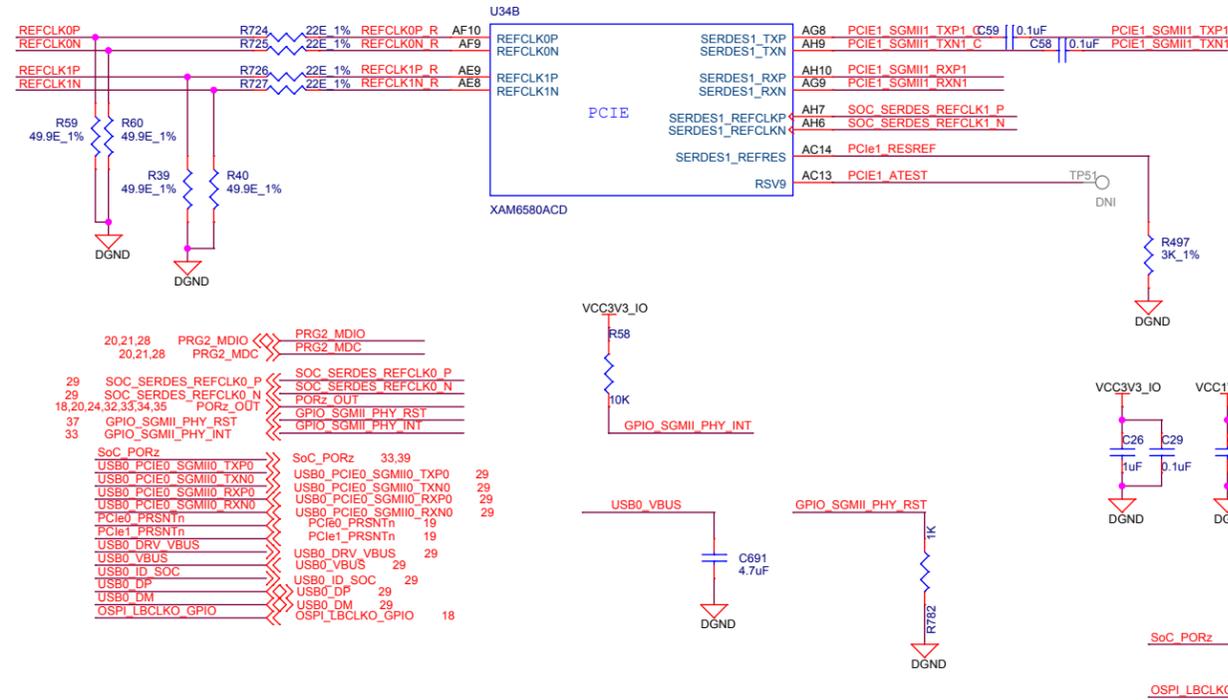


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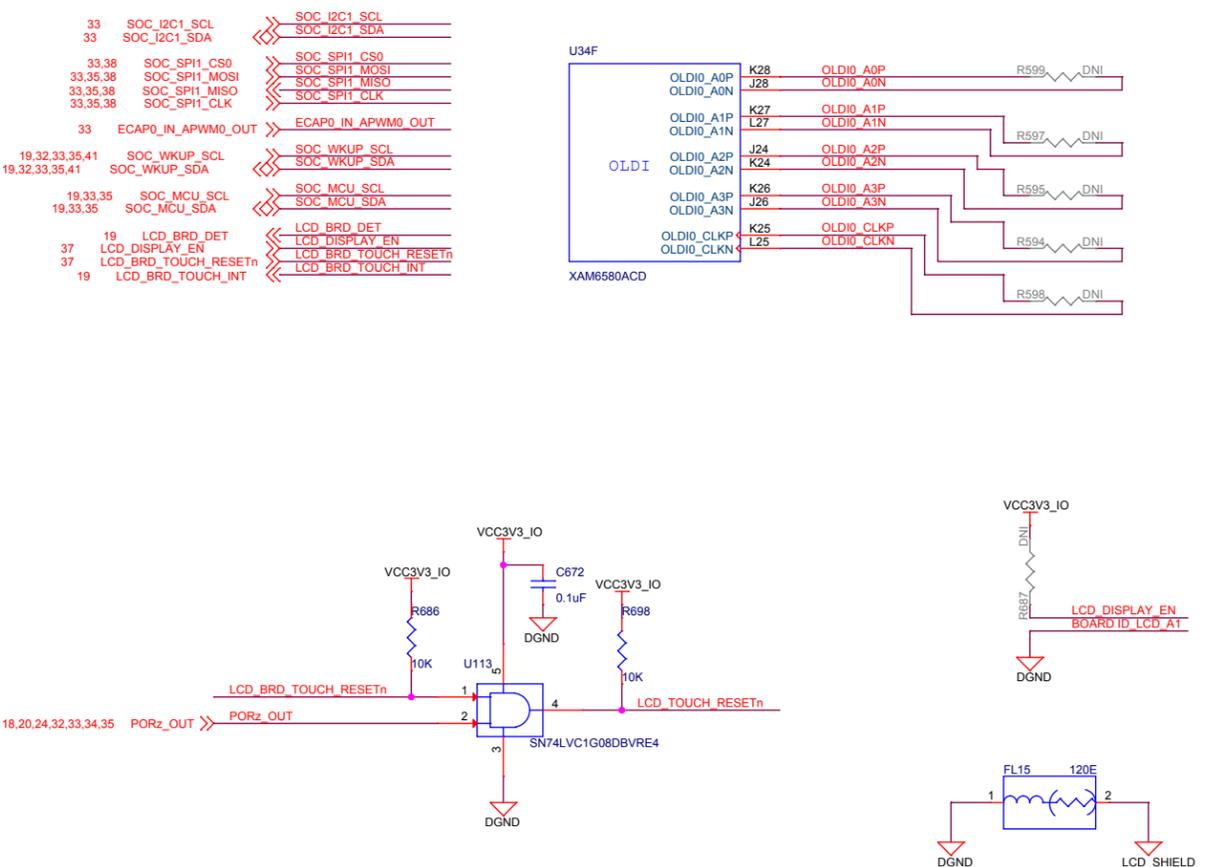


Title		SOC_GENERAL & MCU GENERAL	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E4
Date:	Thursday, August 29, 2019	Sheet	33 of 44

SERDES INTERFACE



OLDI INTERFACE

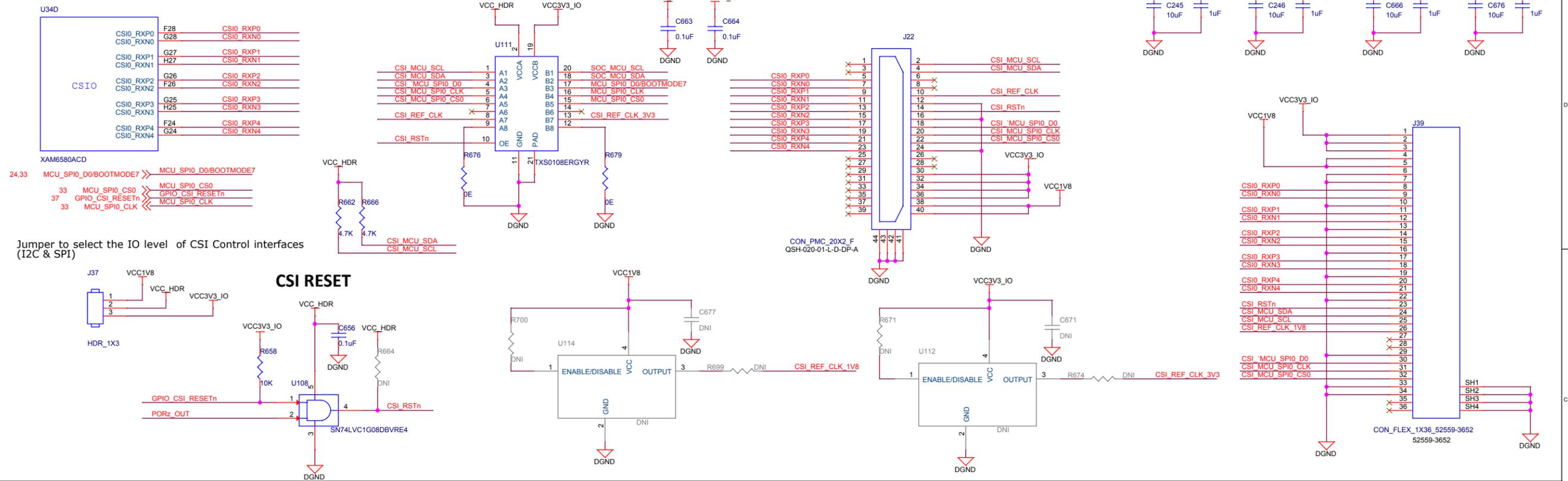


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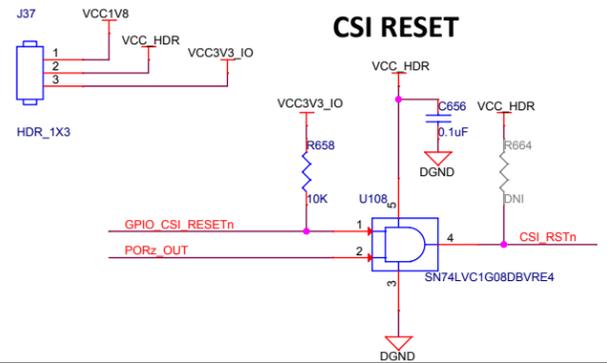


Title		SERDES & DISPLAY INTERFACE	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E4
Date:	Wednesday, August 28, 2019	Sheet	34 of 44

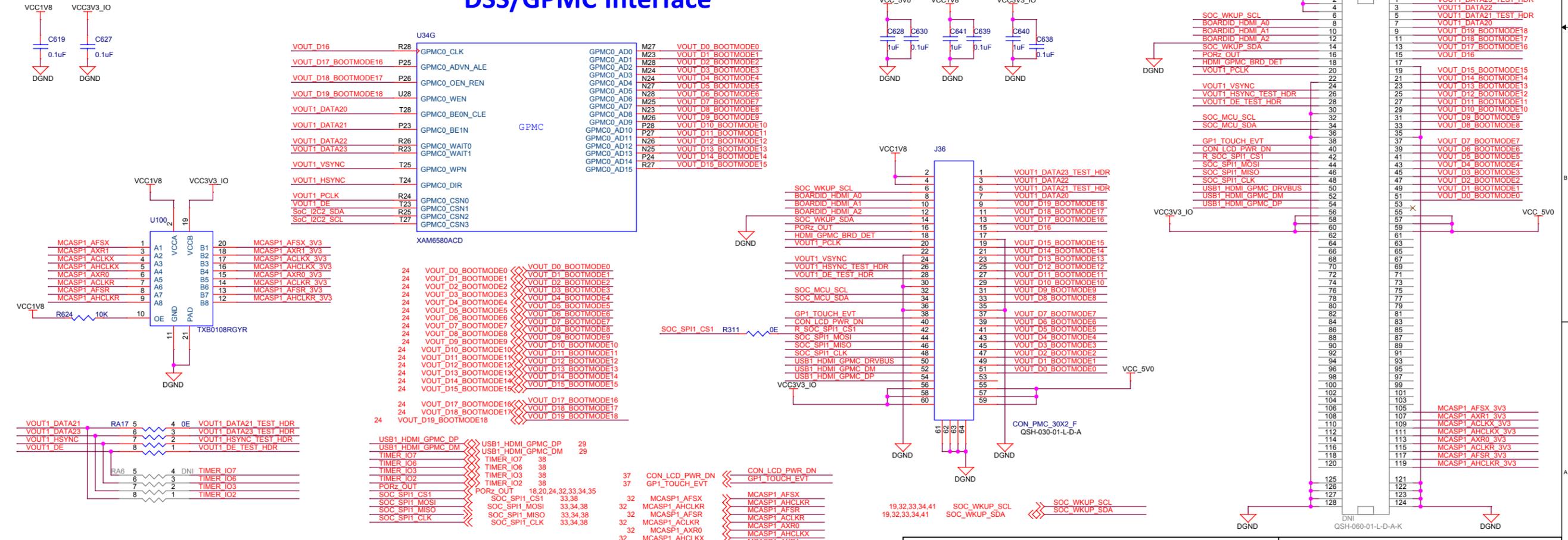
CSI INTERFACE



CSI RESET

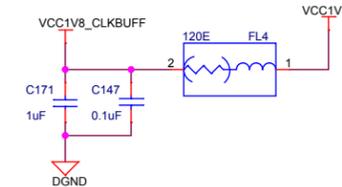
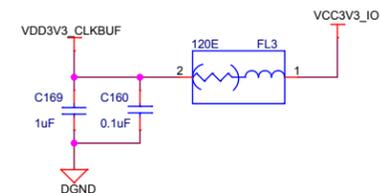
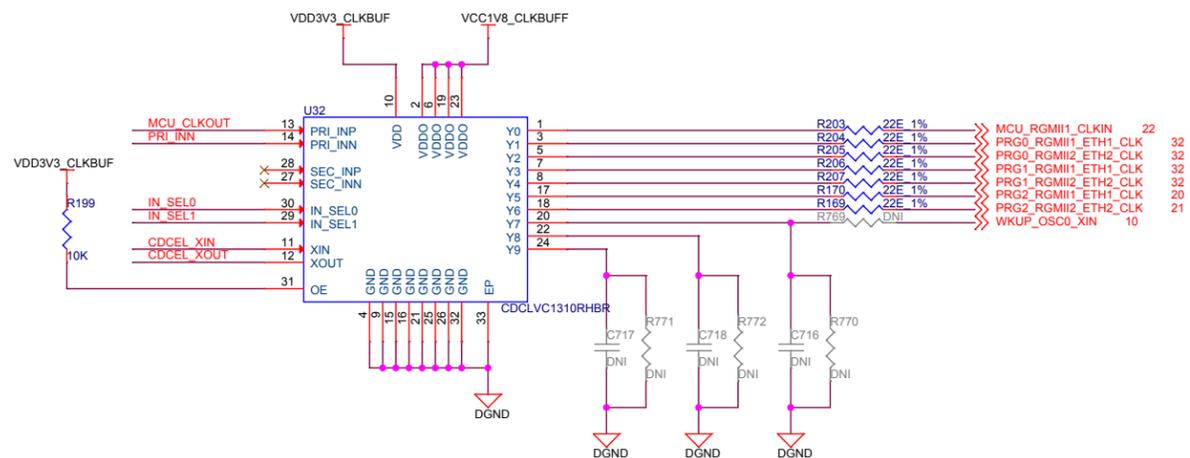
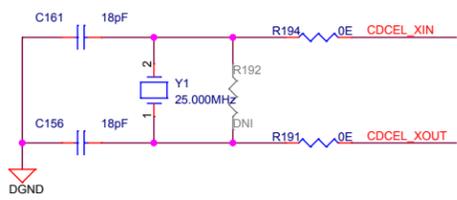
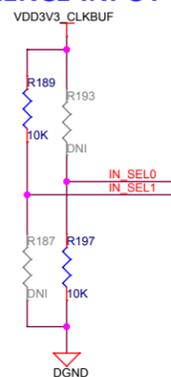


DSS/GPMC Interface

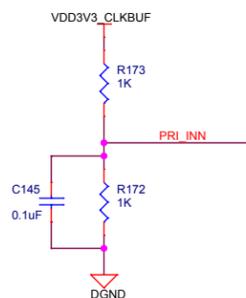
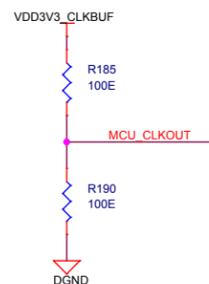


ETHERNET PHY CLOCK BUFFER

REFERENCE INPUT SELECTION



MCU_CLKOUT → MCU_CLKOUT 33



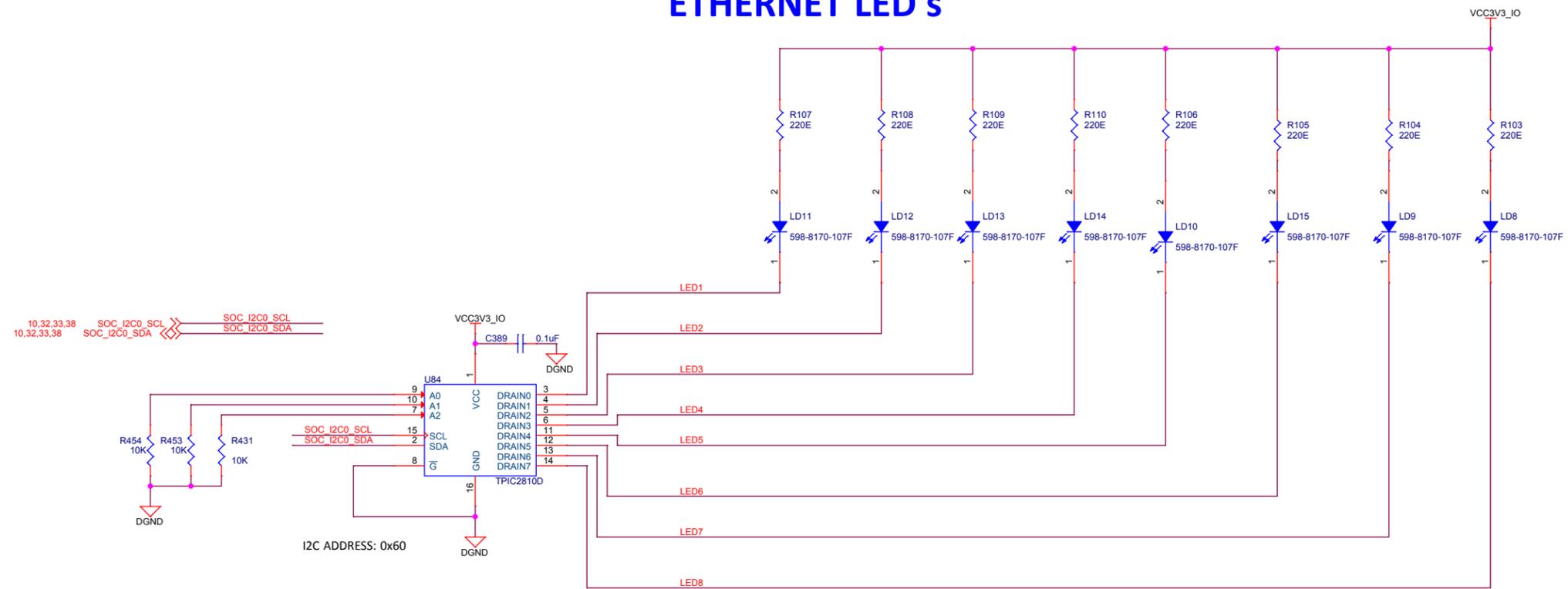
Designed for TI by Mistral Solutions Pvt Ltd



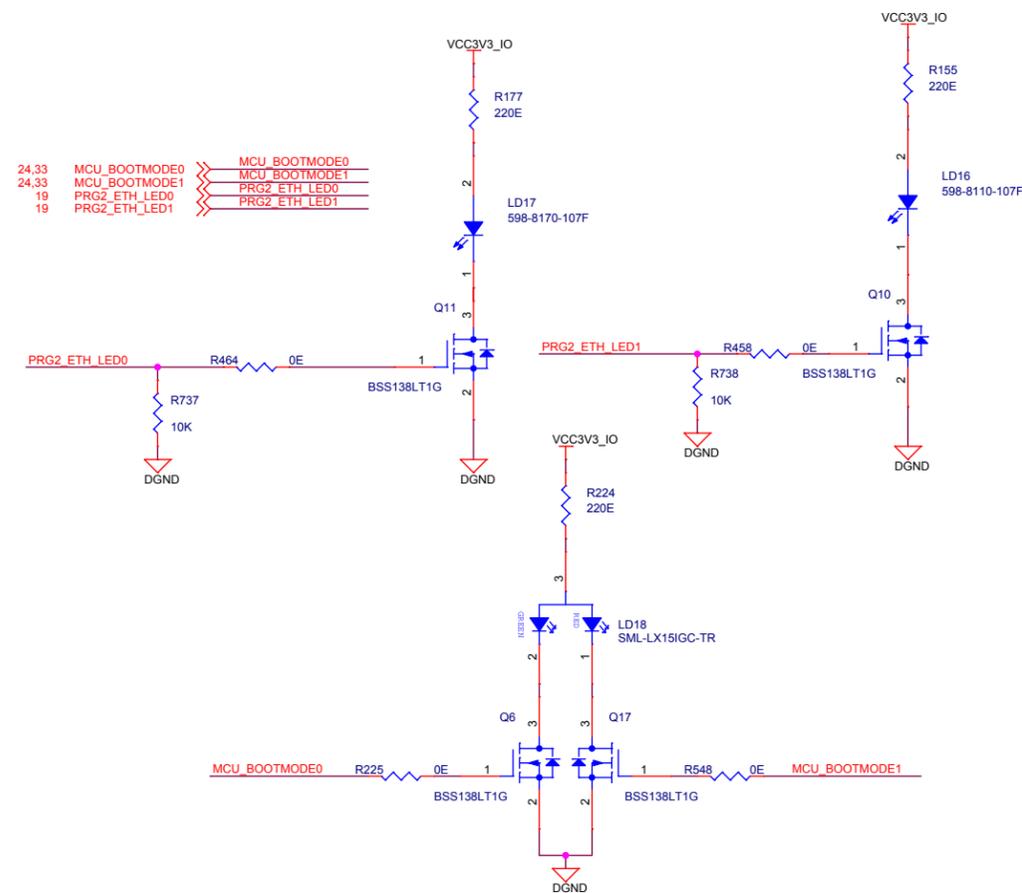
Title: ETHERNET PHY CLOCK GENERATOR

Size		Rev
C	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	E4
Date:	Wednesday, August 28, 2019	Sheet 36 of 44

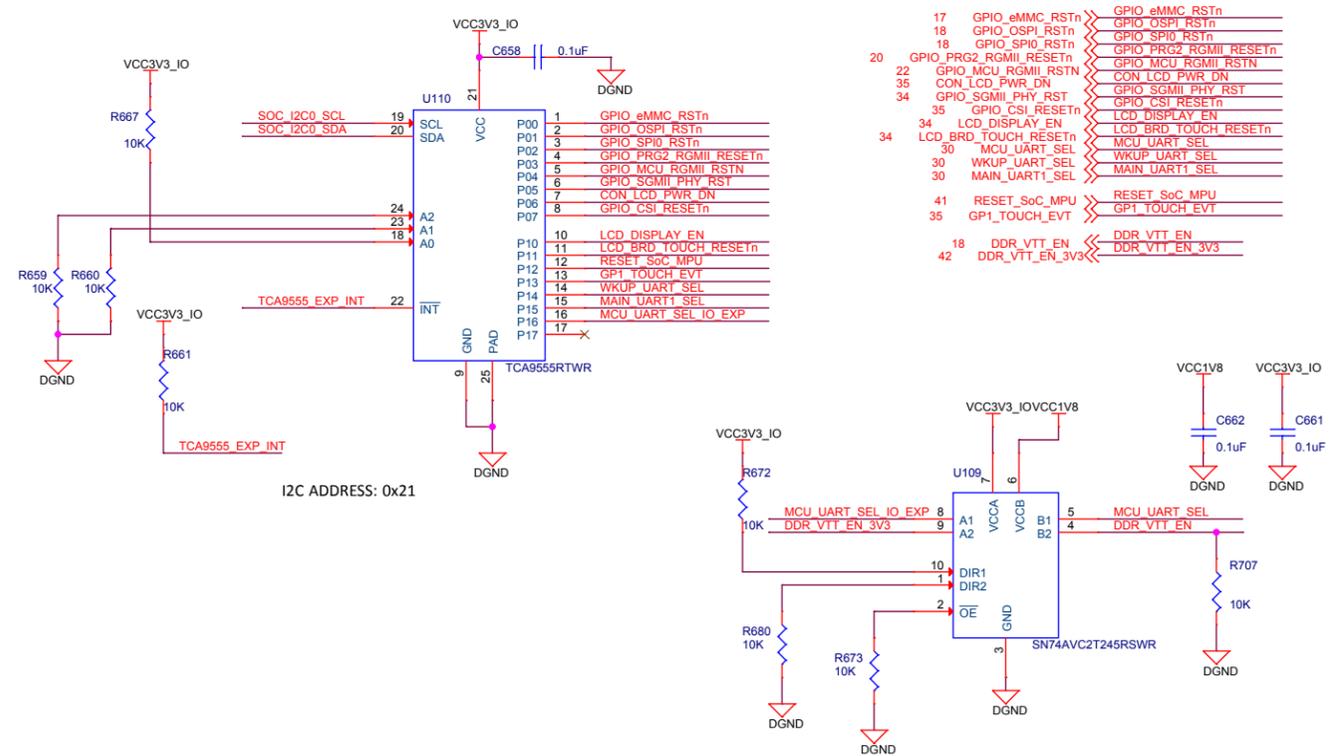
ETHERNET LED'S



PRG2 ETHERNET LED'S



I2C IO Expander

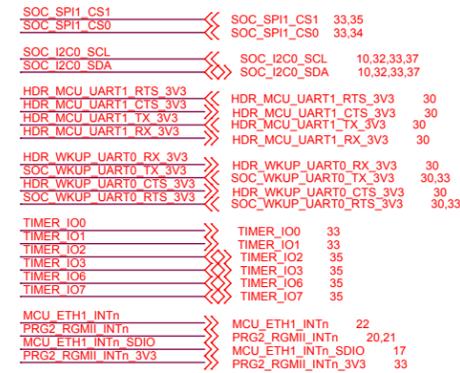
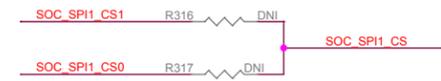


Designed for TI by Mistral Solutions Pvt Ltd

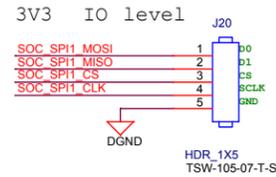


Title		ETHERNET LED'S	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	
C		E4	
Date:	Wednesday, August 28, 2019	Sheet	37 of 44

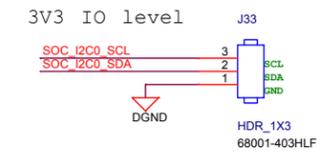
TEST HEADER



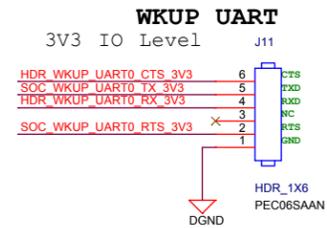
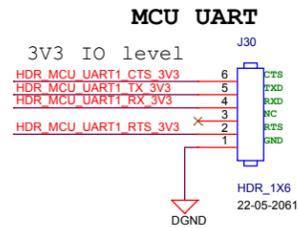
SPI TEST HEADER



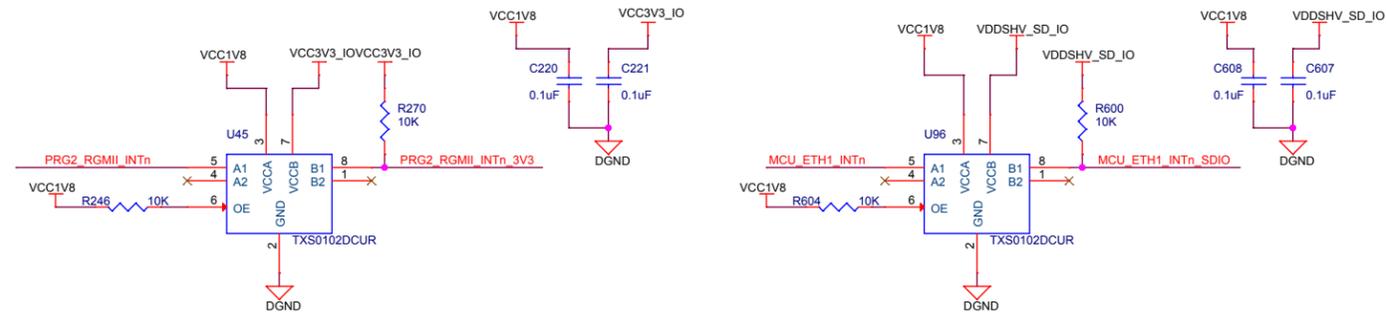
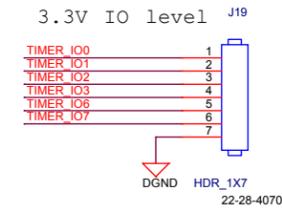
I2C TEST HEADER



UART TEST HEADER



TIMER SIGNALS TEST HEADER



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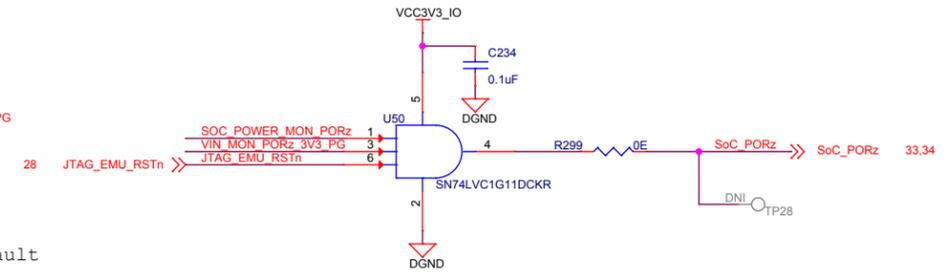
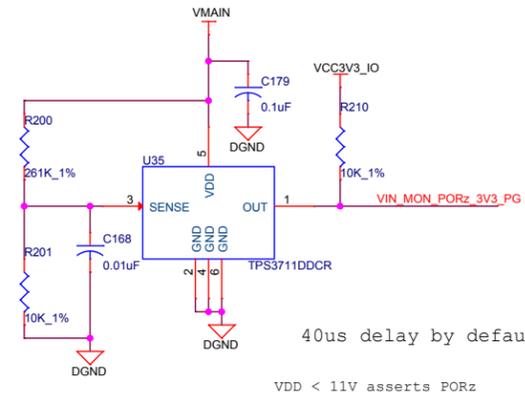
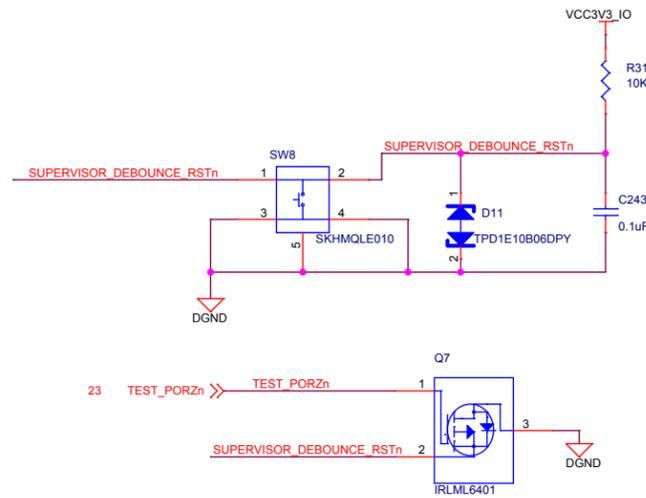


Title TEST HEADER

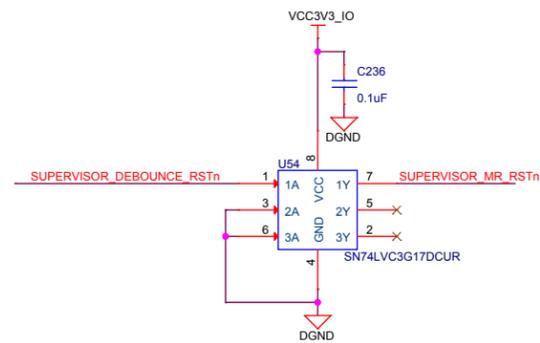
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 38 of 44

VOLTAGE SUPERVISOR

Under Voltage Monitor (VMAIN)

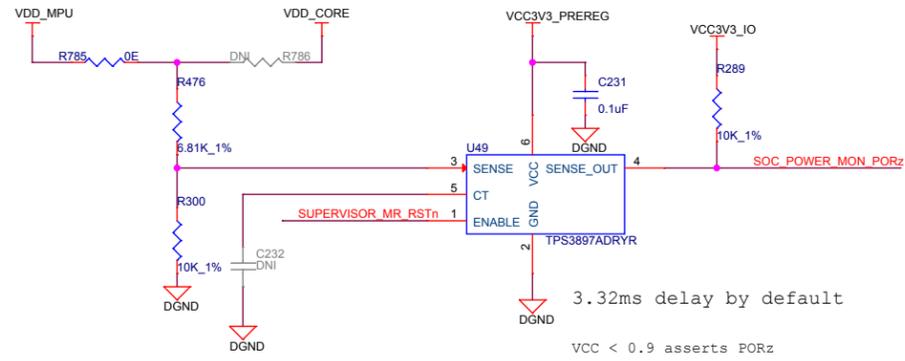


DEBOUNCE CIRCUIT



41.42 VIN_MON_PORz_3V3_PG << VIN_MON_PORz_3V3_PG

Under Voltage Monitor (VDD_MPU / VDD_CORE)



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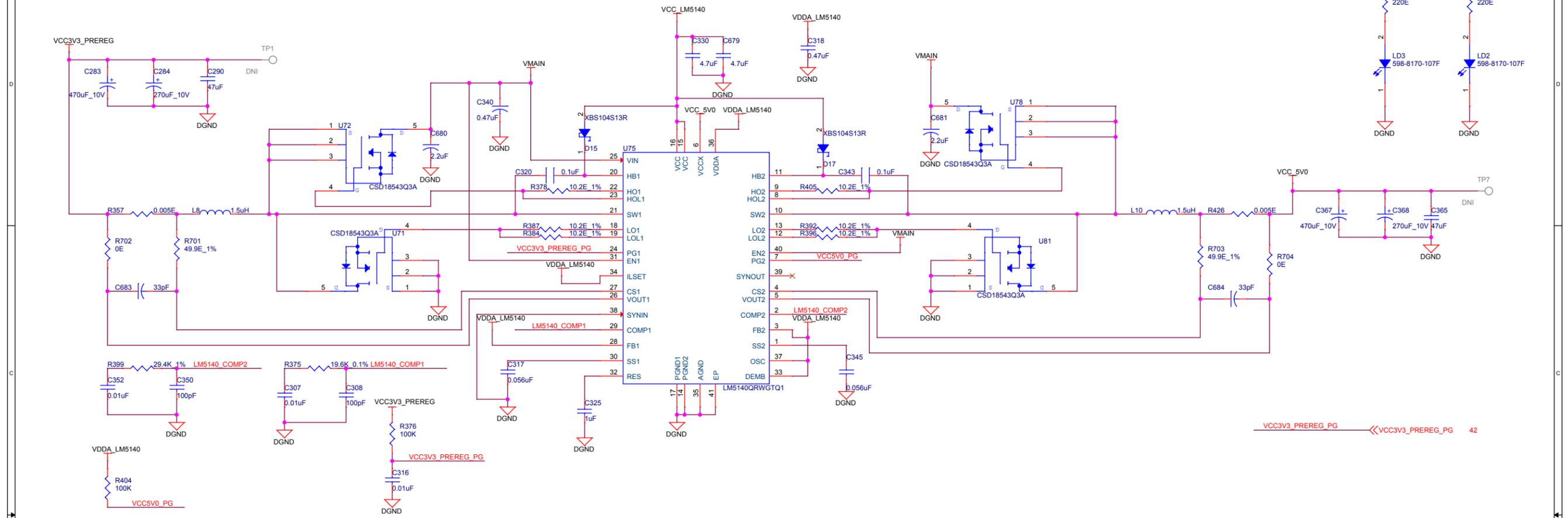
Title VOLTAGE SUPERVISOR & WKUP LEDs

Size Variant Name = PROC082 001 OPN#TMDX654IDKEVM Rev E4

Date: Wednesday, August 28, 2019 Sheet 39 of 44

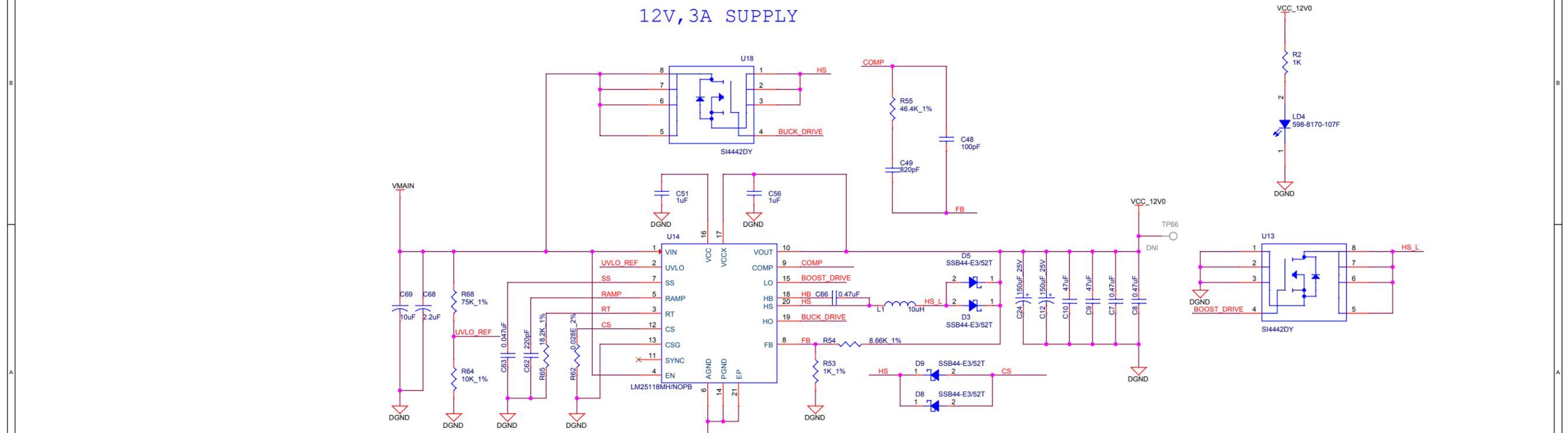
PRE_REG POWER SUPPLY

5V, 10A and 3.3V, 10A Dual SUPPLY



SERDES POWER SUPPLY

12V, 3A SUPPLY



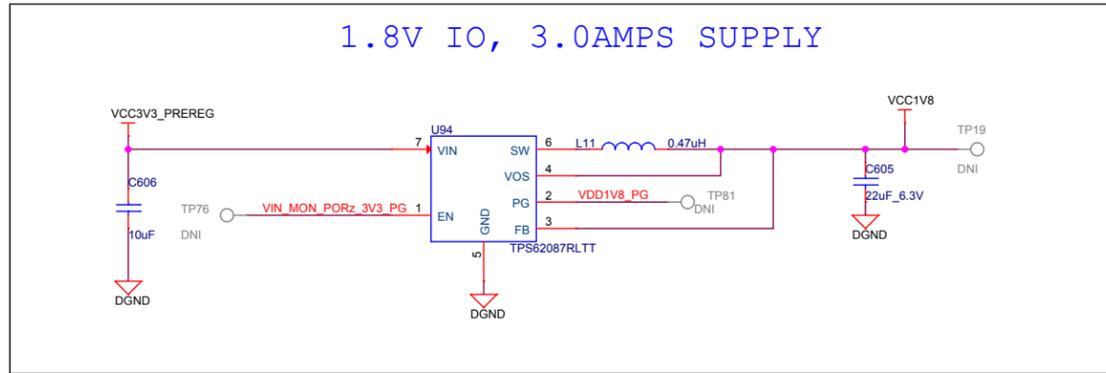
Designed for TI by Mistral Solutions Pvt Ltd



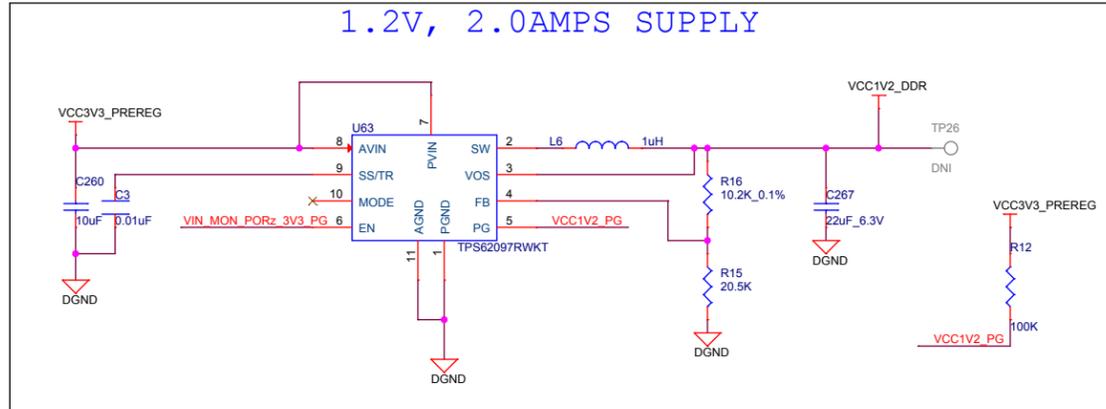
Title		PRE_REG and SERDES POWER SUPPLY	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E4
Date:	Wednesday, August 28, 2019	Sheet	40 of 44

SoC POWER SUPPLY

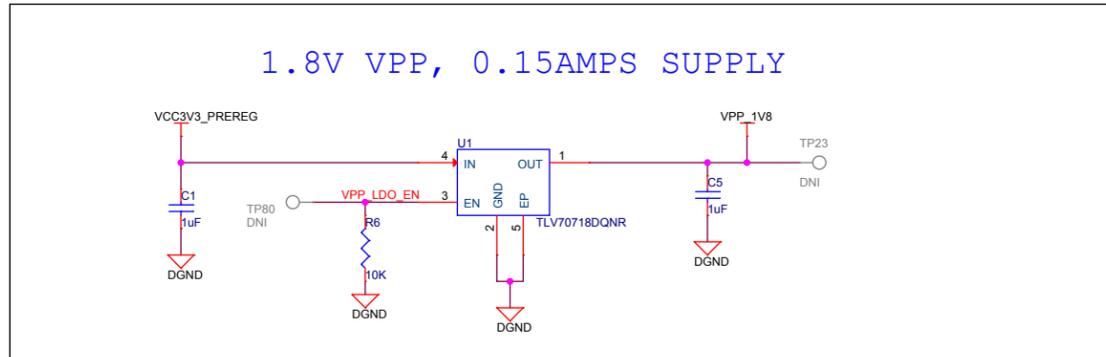
1.8V IO, 3.0AMPS SUPPLY



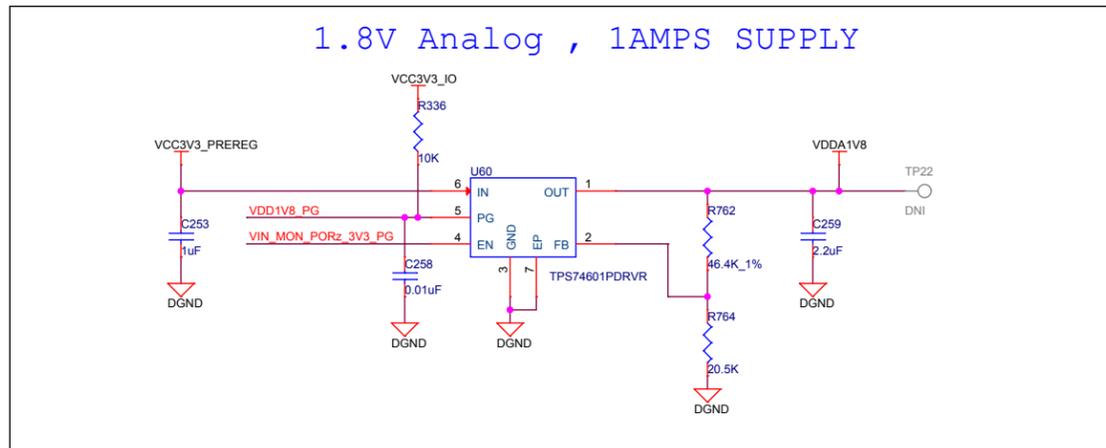
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY

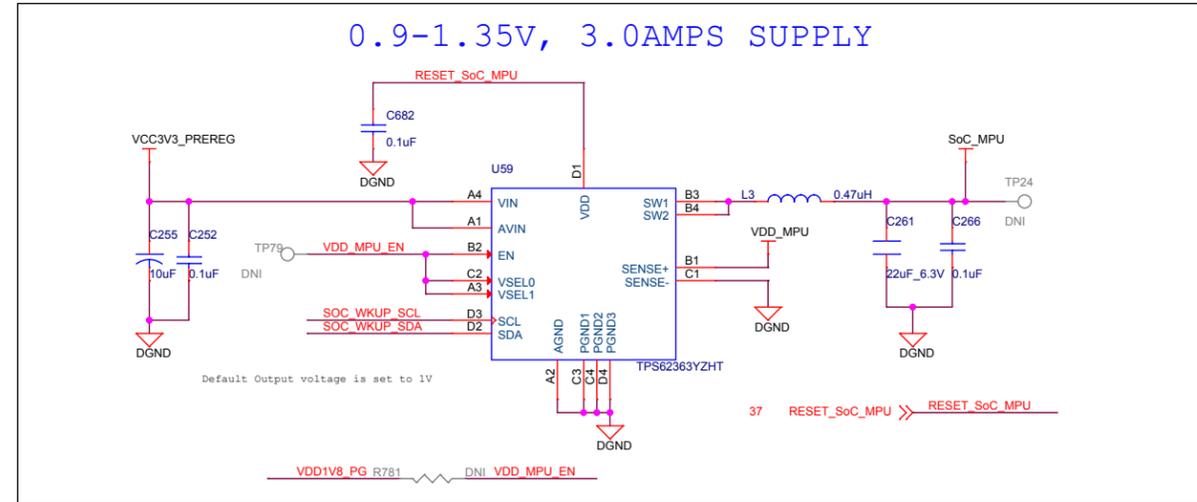


1.8V Analog , 1AMPS SUPPLY

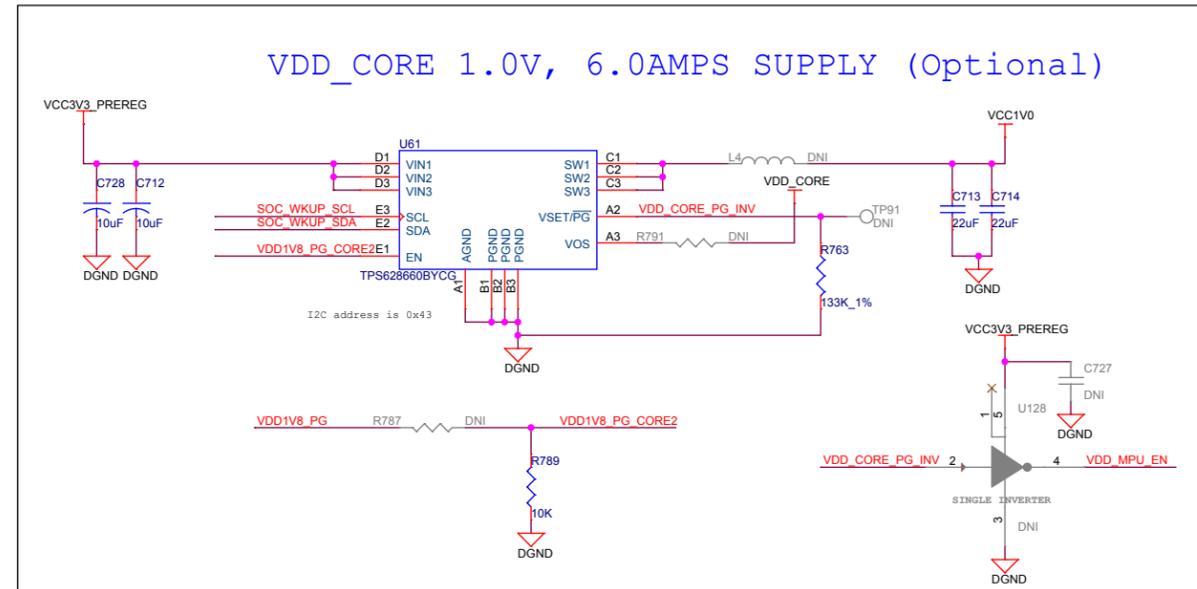


- 19,32,33,34,35 SOC_WKUP_SCL >> SOC_WKUP_SCL
- 19,32,33,34,35 SOC_WKUP_SDA <<> SOC_WKUP_SDA
- 18 VPP_LDO_EN <<< VPP_LDO_EN
- 39,42 VIN_MON_PORz_3V3_PG <<< VIN_MON_PORz_3V3_PG
- 39,42 VDD1V8_PG <<< VDD1V8_PG

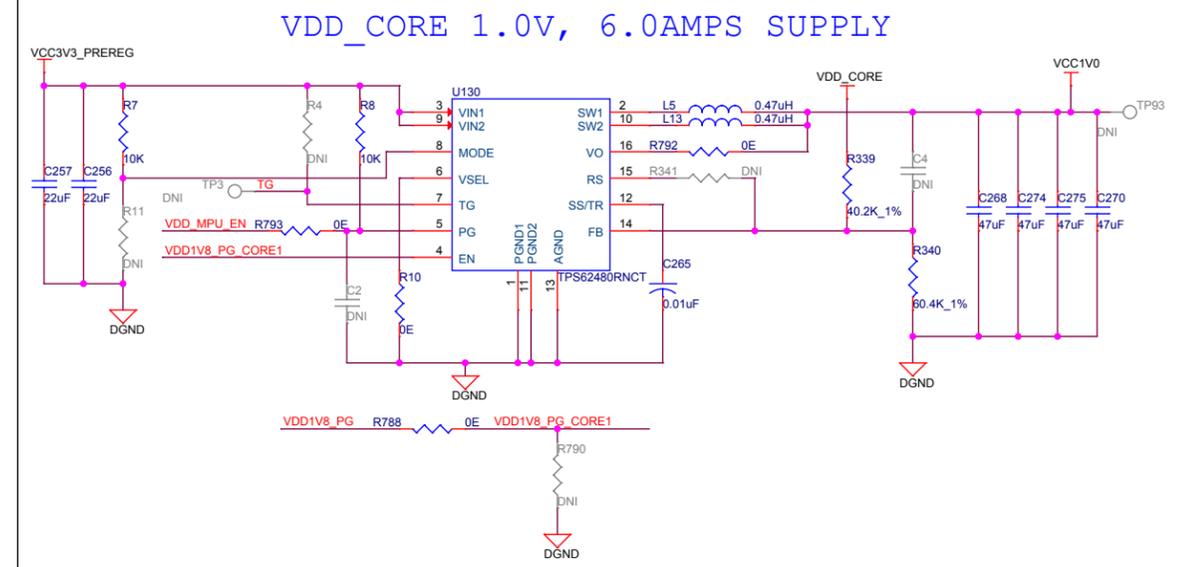
0.9-1.35V, 3.0AMPS SUPPLY



VDD_CORE 1.0V, 6.0AMPS SUPPLY (Optional)



VDD_CORE 1.0V, 6.0AMPS SUPPLY



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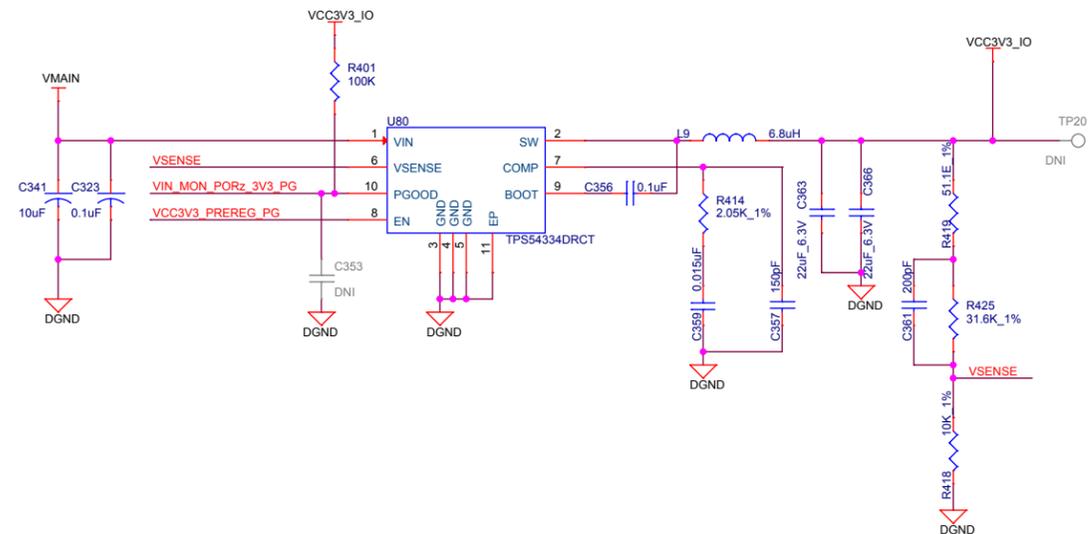


Title SoC POWER SUPPLY

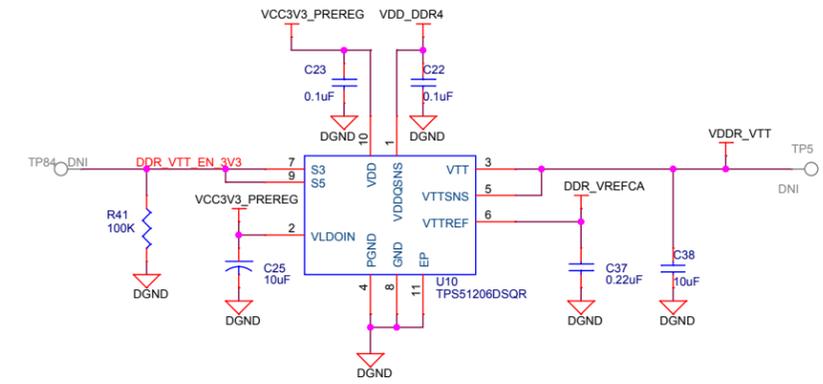
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Wednesday, August 28, 2019	Sheet 41 of 44

PERIPHERAL POWER SUPPLY

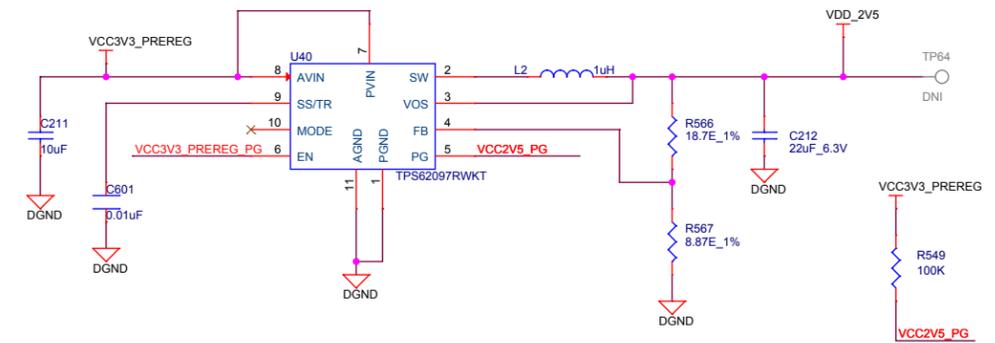
3.3V, 3.0AMPS SUPPLY



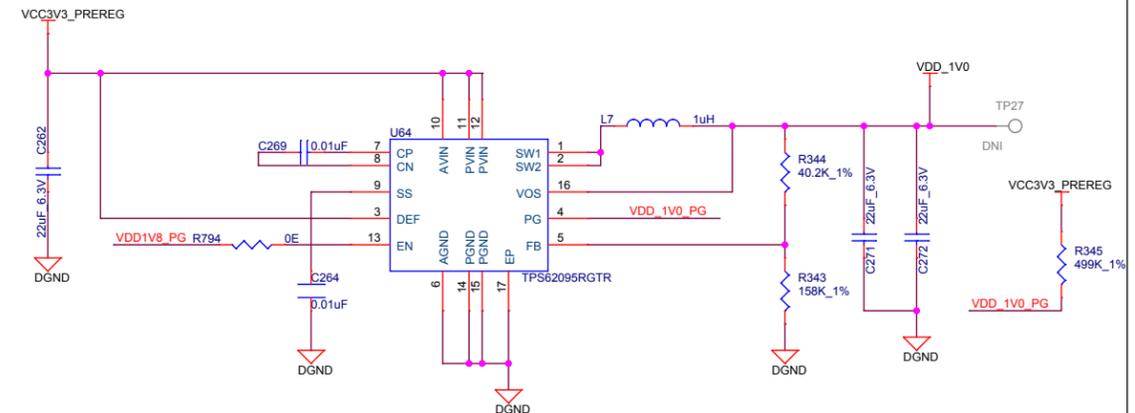
VTT SUPPLY FOR DDR4



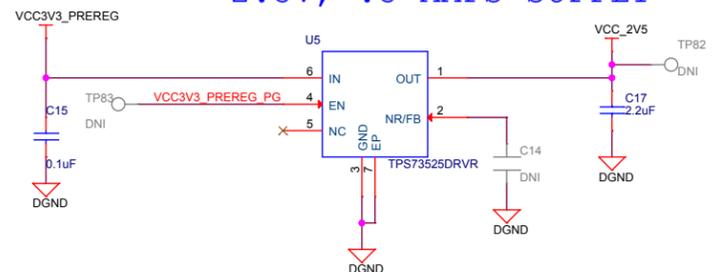
2.5V, 2.0AMPS SUPPLY



1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



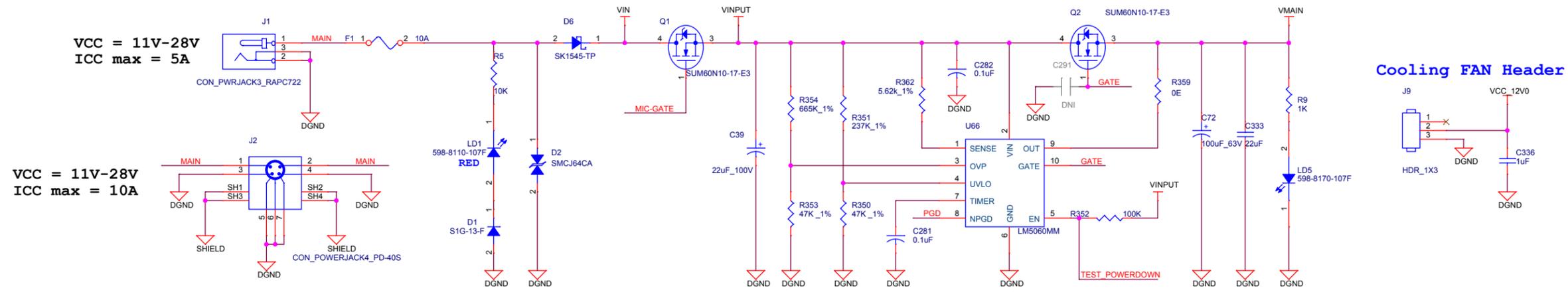
- 40 VDD1V8_PG >> VDD1V8_PG
- 40 VCC3V3_PREREG_PG >> VCC3V3_PREREG_PG
- 39,41 VIN_MON_PORz_3V3_PG << VIN_MON_PORz_3V3_PG
- 37 DDR_VTT_EN_3V3 << DDR_VTT_EN_3V3

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Title PERIPHERAL POWER SUPPLY		
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date: Wednesday, August 28, 2019	Sheet 42 of 44	

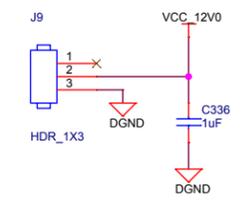
OVER VOLTAGE PROTECTION CIRCUIT



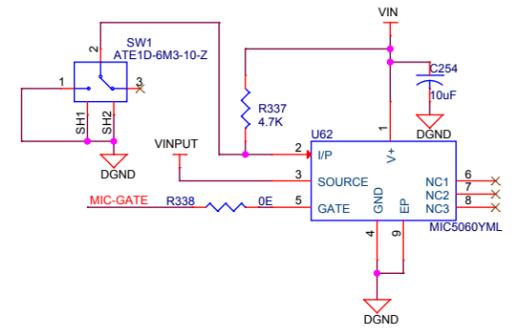
VCC = 11V-28V
ICC max = 5A

VCC = 11V-28V
ICC max = 10A

Cooling FAN Header



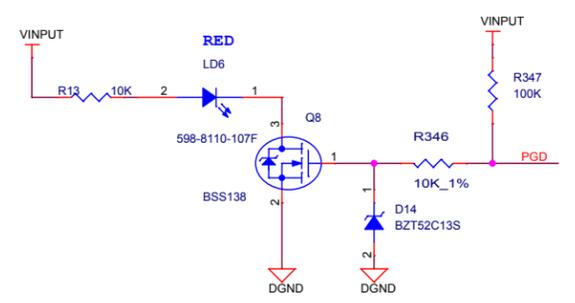
ON/ OFF Control SWITCH



Condition	LED Status (LD1)
Reverse Voltage	ON

Note:-
UVLO set for 11V
OVP set for 28V

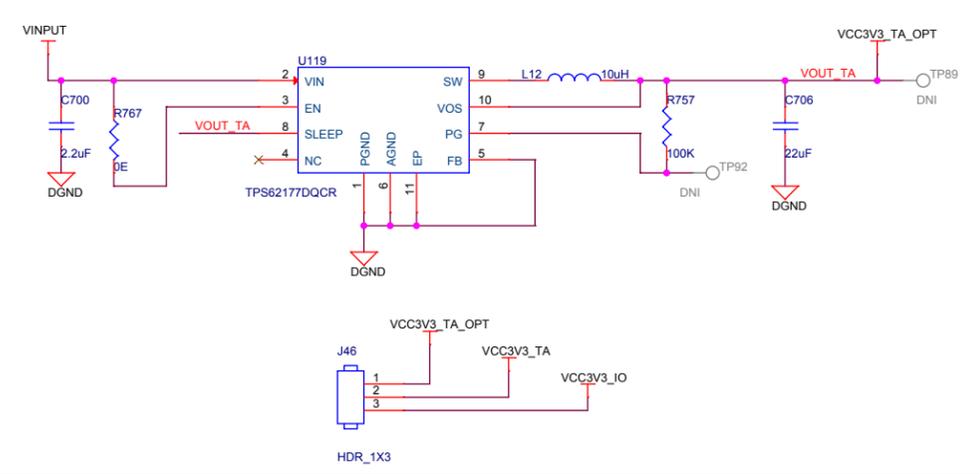
Fault Indication



Condition	LED Status (LD6)
VINPUT between 11 to 28V	OFF
VINPUT above 28V or below 11V	ON

Note:-
When fault is indicated, set to proper voltage and power cycle the board.

TEST AUTOMATION BOARD POWER



Ground test points



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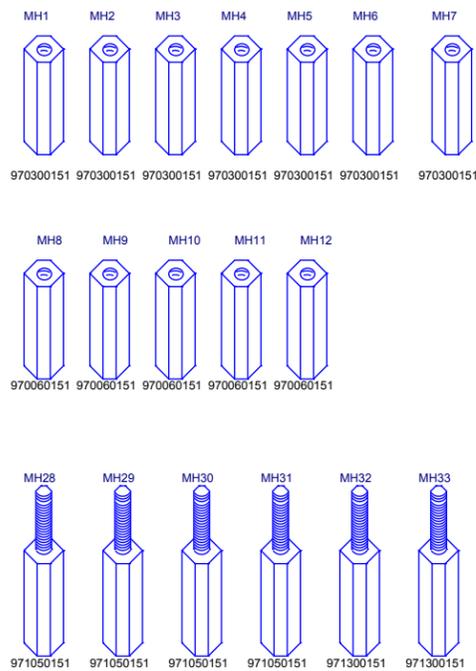
Title OVER VOLTAGE PROTECTION CKT AND TEST AUTOMATION POWER		
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date: Wednesday, August 28, 2019	Sheet 43 of 44	

HARDWARE SCHEMATICS

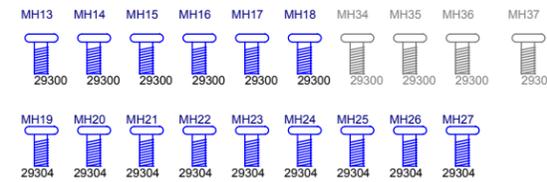
ASSEMBLY NOTES

- All MSL components should be baked as per JEDEC standard.
- PCB should be baked at 120 degree for 8 hours.
- Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- These assemblies are ESD sensitive, ESD precautions shall be observed.
- These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Provide serial numbers to the assembled boards for identification.
- The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

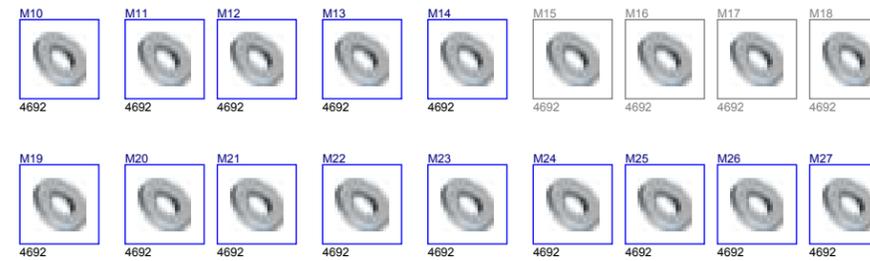
STANDOFFS



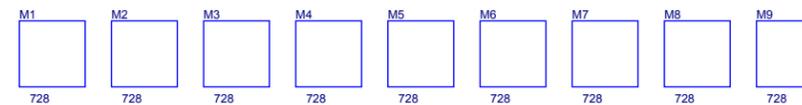
SCREWS



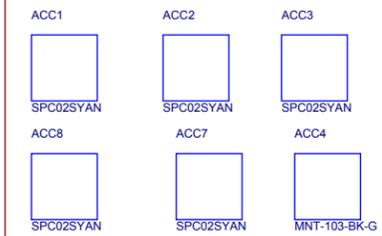
WASHER'S



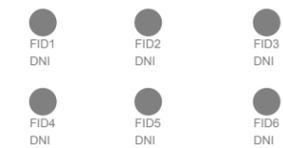
RUBBER FEET



JUMPERS



FIDUCIALS



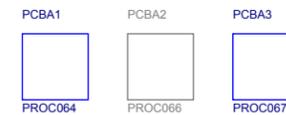
Socket & Processor as Accessories



BARE PCB



Assembled PCB's



Board Serial No.



LABELS

ORDERABLE PART NO



Orderable part number	
Variant	Label Text
001	TMDX654IDKEVM
002	TMDX654HSEVM
003	TMDX654GPEVM
004	TMDX654IDKEVM-S
005	TMDX654GPEVM-S

LOGOs



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E4
Date:	Thursday, August 22, 2019	Sheet 44 of 44