

# MAXWELL CUSTOMER PROCESSOR BOARD

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<b>REV</b>	E3
<b>VER</b>	1.0

## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	29th MAY 2018	Drafted from "PROC062_REV E2_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	13th JUN 2018	Updated REV E3 schematic as per change list document.	Mistral Design Team	AJIT MB	AJIT MB
1.0	04th SEP 2018	Baselined	Mistral Design Team	AJIT MB	AJIT MB

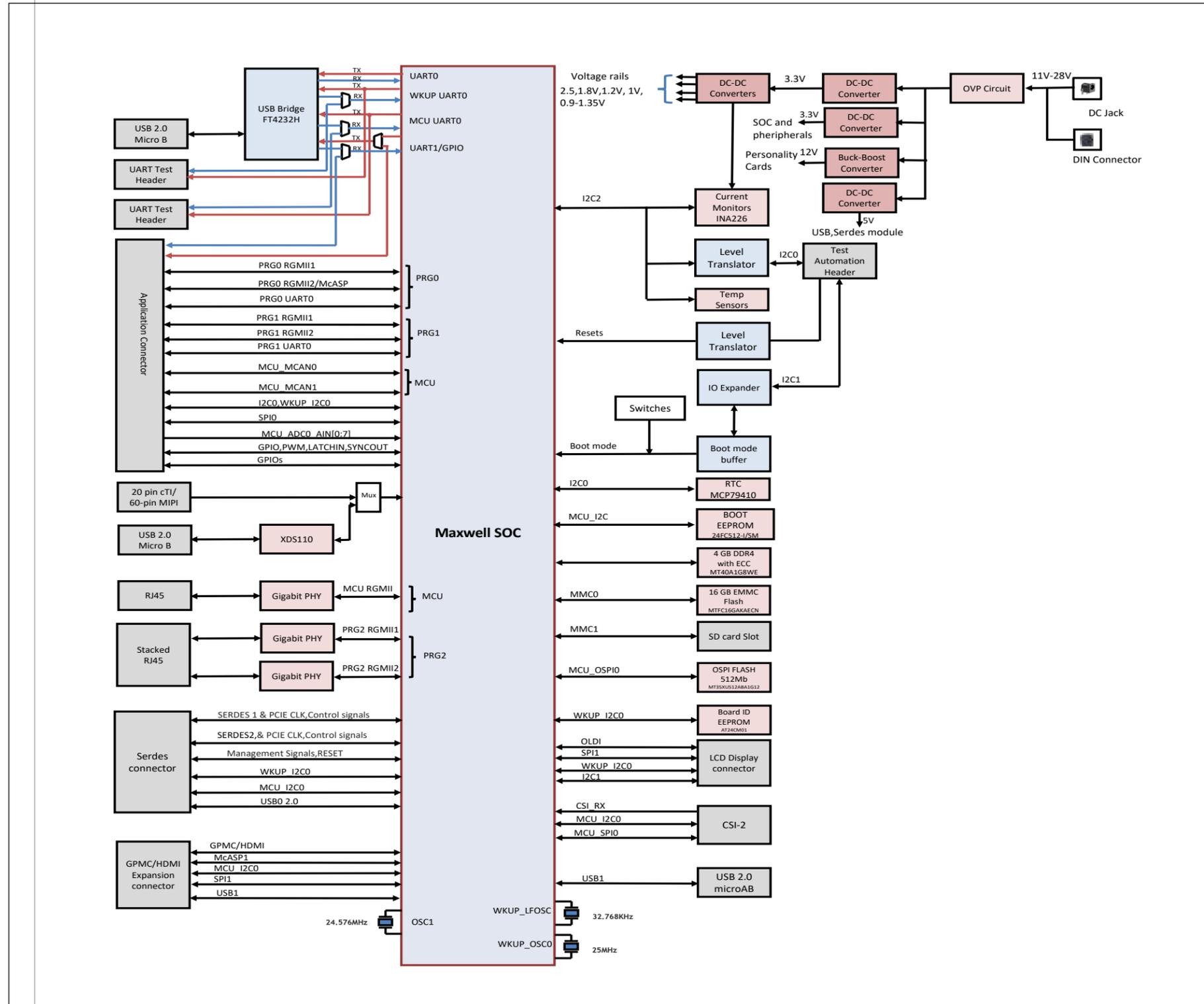
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Title REVISION HISTORY

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, September 04, 2018	Sheet 2 of 44

# BLOCK DIAGRAM\_CP BOARD



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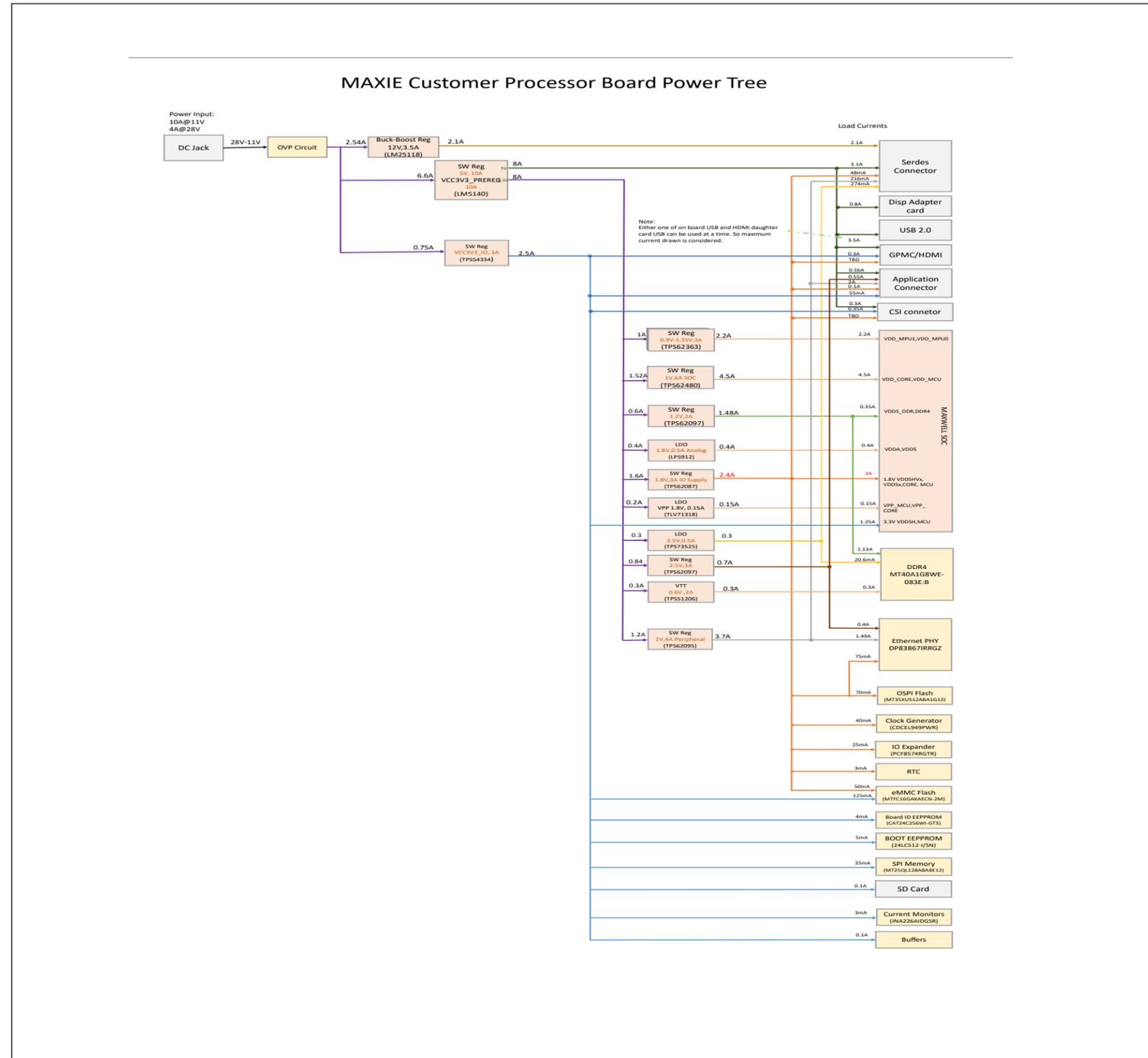


Title BLOCK DIAGRAM\_CP BOARD

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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# POWER FLOW DIAGRAM



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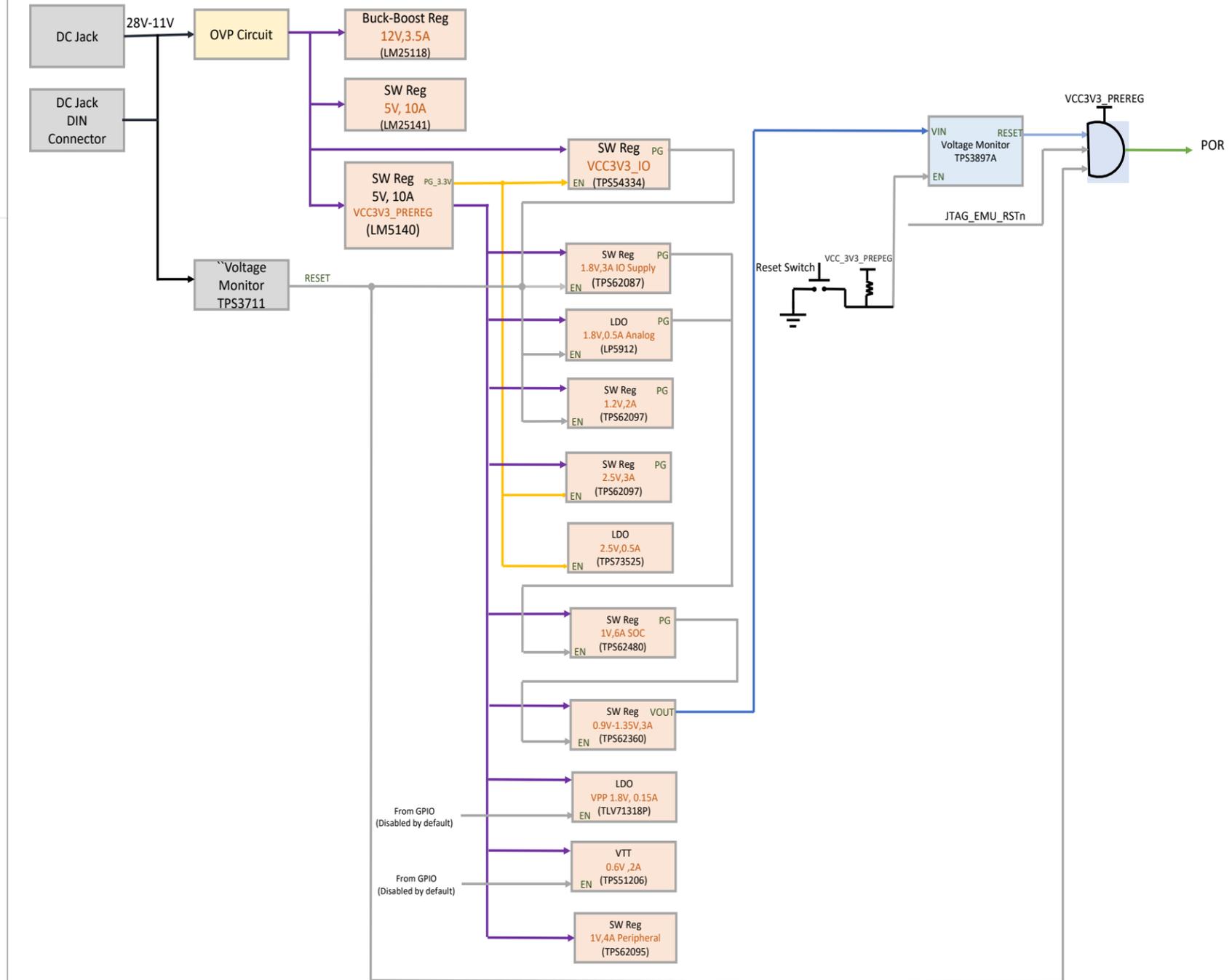


Title POWER FLOW DIAGRAM

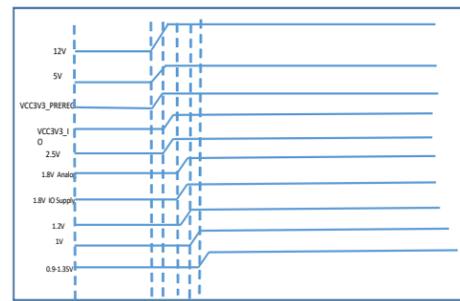
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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# POWER SEQUENCE

## MAXIE Customer Processor Board Power Sequencing



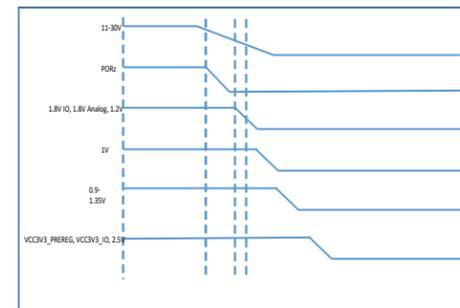
Power up Sequence



Power up Sequence:  
12V, 5V, VCC3V3\_IO, 2.5V → 1.8V Analog, 1.8V IO Supply → 1V SOC → 0.9-1.35V

There is no sequencing for 1V Peripheral supply

Power Down Sequence



Power down Sequence:  
1.2V, 1.8V Analog, 1.8V IO Supply, 1V SOC, 0.9V-1.35V → VCC3V3\_PREREG, VCC3V3\_IO, 2.5V

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Title POWER SEQUENCE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
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## GPIO MAPPING TABLE

Total No of GPIOs Required from Maxwell SoC								
SI No	GPIO Description	Required on	FUNCTIONALITY	GPIO Number	SoC Muxed Signal name	Direction WRT CTRL	Default state	Active state
1	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_24	MCU_OSPI0_CSN1	Input	High	Low
2	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_27	MCU_OSPI1_DQS	Input	High	Low
3	eMMC Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
4	OSPI flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
5	SPI NOR flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
6	ICSSG_PRG2_Ethernet PHY Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
7	ICSSG_PRG2_Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_87	EXT_REFCLK1	Input/Output	High	Low
8	ICSSG_Ethernet PHY_1 Link Detection GPIO	Customer Processor Board	Link Detection ( GPIO Input)	GPIO1_13	MMC0_SDCD	Input	Low	High
9	ICSSG_Ethernet PHY_2 Link Detection GPIO	Customer Processor Board	Link Detection ( GPIO Input)	GPIO1_14	MMC0_SDWP	Input	Low	High
10	MCU domain Ethernet PHY Reset Control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
11	MCU domain Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_80	MMC1_SDWP	Input/Output	High	Low
12	Three GPIO's are required to control the Mux select between UART test header RX , Application board & FT4232_UART_RX	Customer Processor Board	Mux Selection	I2C GPIO Expander		Output	High	Low
13				I2C GPIO Expander		Output	High	Low
14				I2C GPIO Expander		Output	High	Low
15	VPP LDO enable	Customer Processor Board	VPP_EN	WKUP_GPIO0_26	MCU_OSPI1_LBCLKO	Output	Low	High
16	One WKUP_GPIO for VTT Regulator Enable	Customer Processor Board	VTT_EN	WKUP_GPIO0_28	MCU_OSPI1_D0	Output	Low	High
17	GPIO0 to drive PRG2 LED0	Customer Processor Board	LEDs	WKUP_GPIO0_8	WKUP_GPIO0_8	Output	Low	High
18	GPIO1 to drive PRG2 LED1	Customer Processor Board	LEDs	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	Low	High
19	GPIO2 to drive PRG2 LED2	Customer Processor Board	LEDs	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	Low	High
20	GPIO3 to drive PRG2 LED3	Customer Processor Board	LEDs	WKUP_GPIO0_50	MCU_SPI0_D1	Output	Low	High
21	IDK_ICSSG_PRG0_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO1_34	PRG0_PRU0GPO5	Output	High	Low
22	IDK_ICSSG_PRG0_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO1_37	PRG0_PRU0GPO8	Input/Output	High	Low
23	IDK_ICSSG_PRG1_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO0_61	PRG1_PRU0GPO5	Output	High	Low
24	IDK_ICSSG_PRG1_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO0_81	PRG1_PRU1GPO5	Output	High	Low
25	IDK_ICSSG_Ethernet PHY_1 Link Detection GPIO	IDK /GP Application board	Link Detection ( GPIO Input)	GPIO0_84	PRG1_PRU1GPO8	Input	Low	High
26	IDK_ICSSG_Ethernet PHY_2 Link Detection GPIO	IDK /GP Application board	Link Detection ( GPIO Input)	GPIO0_64	PRG1_PRU0GPO8	Input	Low	High
27	IDK_ICSSG_Ethernet PHY_3 Link Detection GPIO	IDK /GP Application board	Link Detection ( GPIO Input)	GPIO1_39	PRG0_PRU0GPO10	Input	Low	High
28	IDK_ICSSG_Ethernet PHY_4 Link Detection GPIO	IDK /GP Application board	Link Detection ( GPIO Input)	GPIO1_57	PRG0_PRU1GPO8	Input	Low	High
29	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO0_83	PRG1_PRU1GPO7	Output	Low	High
30	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO0_93	PRG1_PRU1GPO17	Output	Low	High
31	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO0_95	PRG1_PRU1GPO19	Output	Low	High
32	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO0_94	PRG1_PRU1GPO18	Output	Low	High
33	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_58	PRG0_PRU1GPO9	Output	Low	High
34	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_54	PRG0_PRU1GPO5	Output	Low	High
35	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_38	PRG0_PRU0GPO9	Output	Low	High
36	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_59	PRG0_PRU1GPO10	Output	Low	High
37	Touch Reset Control GPIO	LCD Adapter Board	Reset	I2C GPIO Expander		Output	High	Low
38	Touch Interrupt GPIO	LCD Adapter Board	Interrupt	I2C GPIO Expander		Input	Low	High
39	LCD Display Enable GPIO	LCD Adapter Board	LCD_EN	I2C GPIO Expander		Output	High	Low
40	CSI Camera Module Reset Control GPIO	CSI Connector	Reset	I2C GPIO Expander		Output	High	Low
41	Display_Power_Down GPIO	HDMI / GPMC Daughter Card	Display_PowerDown	I2C GPIO Expander		Output	High	Low
42	Touch Event GPIO	HDMI / GPMC Daughter Card	Interrupt	I2C GPIO Expander		Input	High	Low
43	SGMII PHY reset control	Serdes Modules	Reset	I2C GPIO Expander		Output	High	Low
44	SGMII PHY Interrupt	Serdes Modules	Interrupt	GPIO1_81	NMIN	Input/Output	High	Low

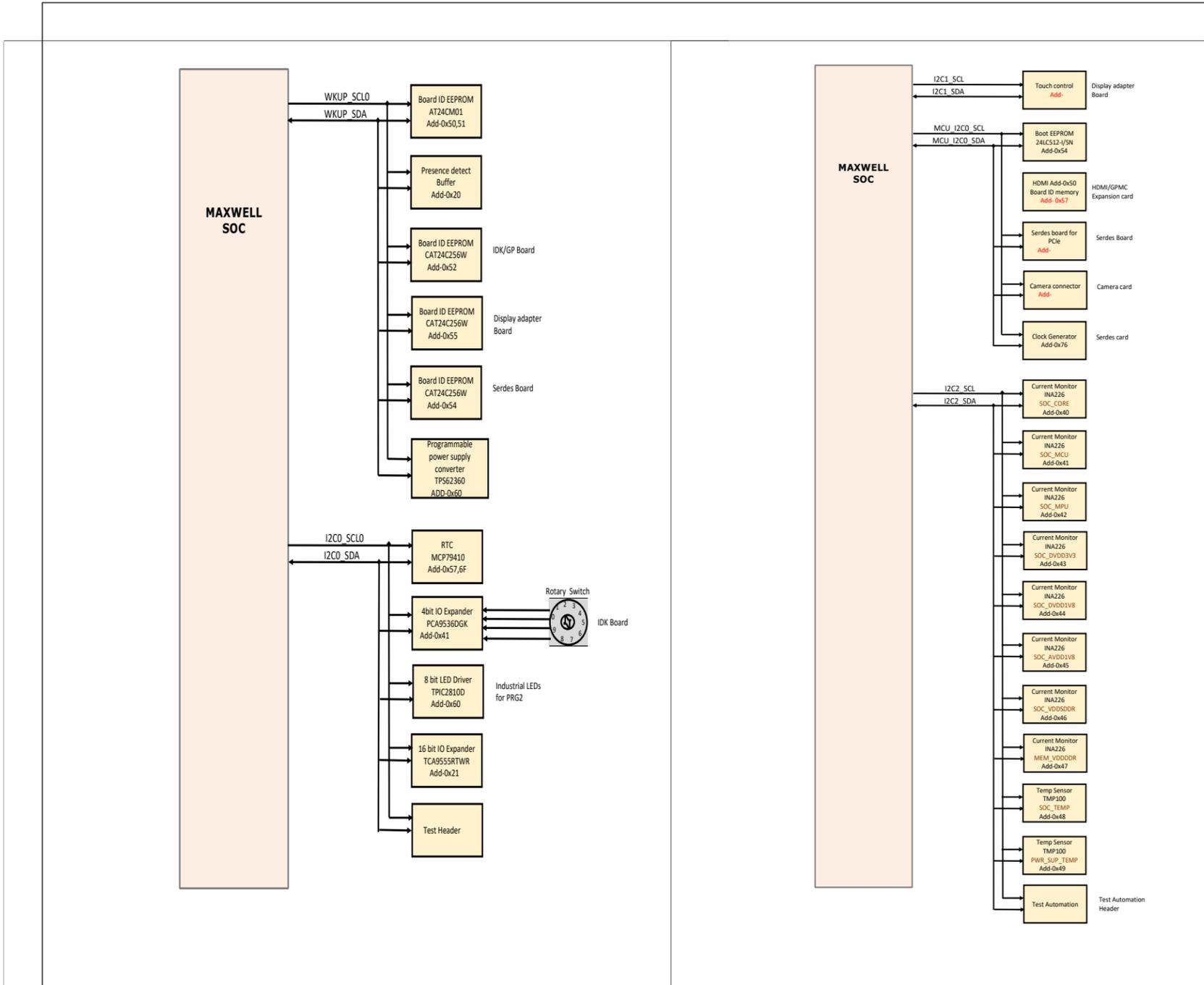
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Title GPIO MAPPING TABLE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 7 of 44

# I2C TREE



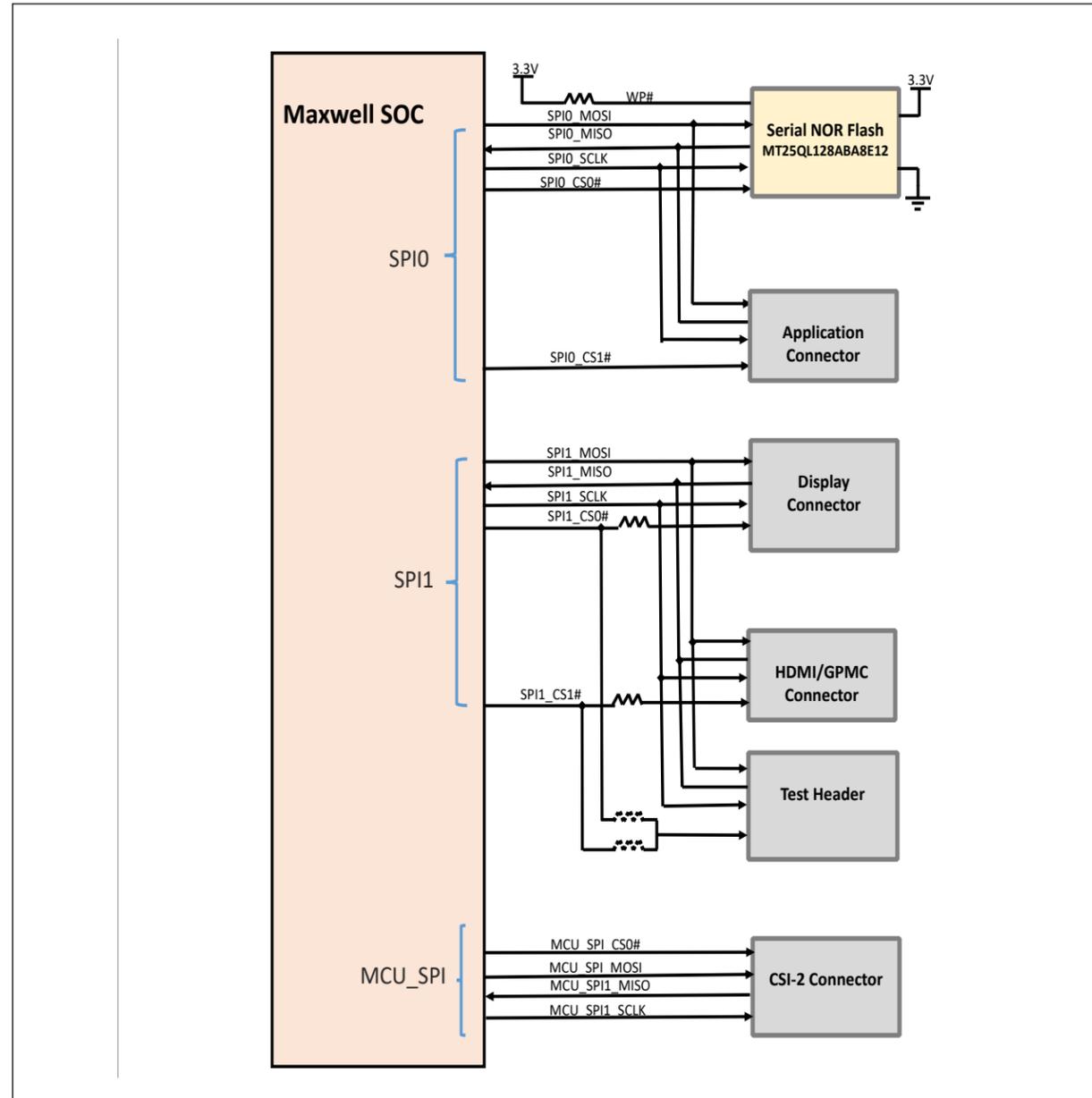
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Title I2C TREE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 8 of 44

# SPI TREE



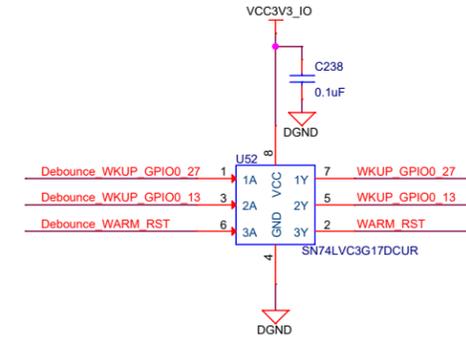
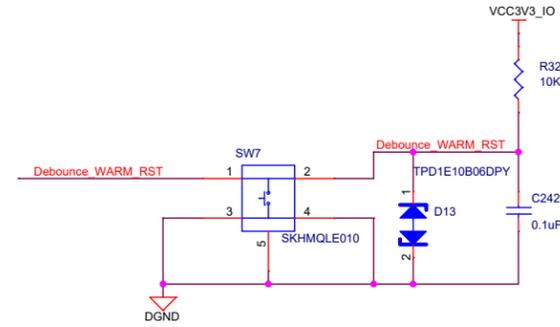
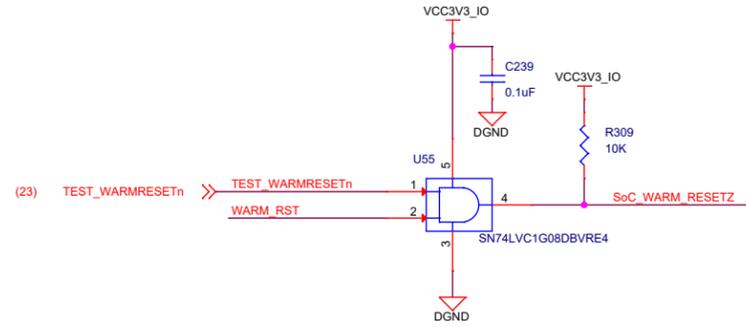
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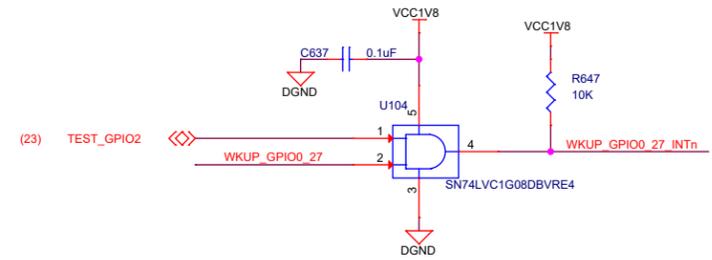
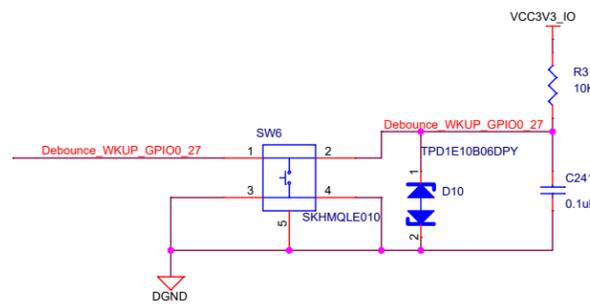
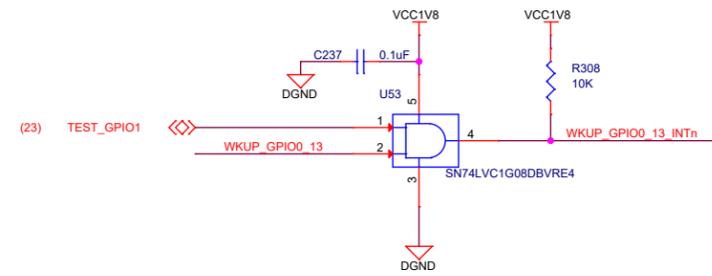
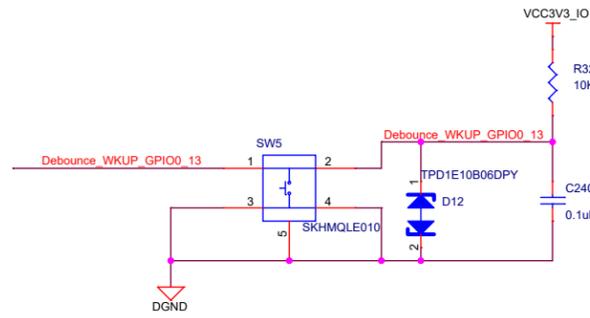
Title SPI TREE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 9 of 44

## SoC WARM\_RST

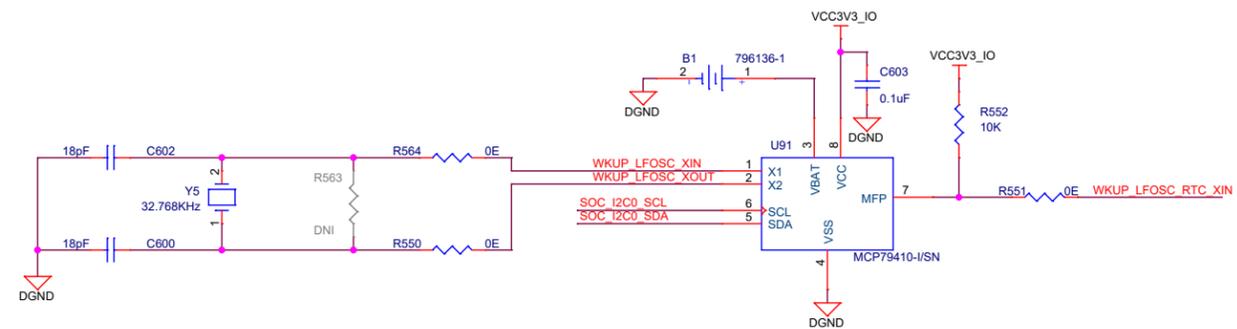
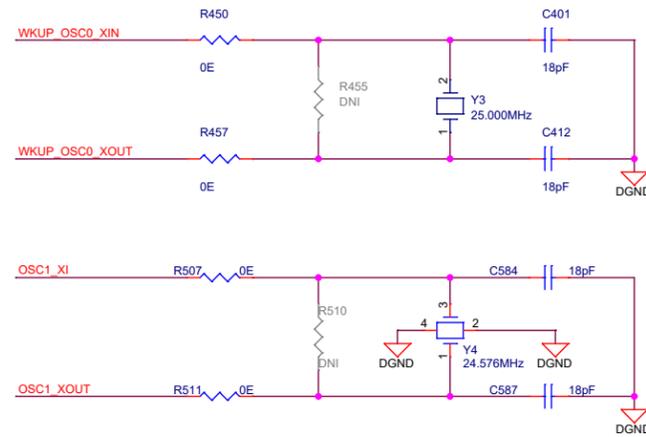


## MCU\_PUSH BUTTONS



SoC_WARM_RESETZ	>>	SoC_WARM_RESETZ	(33)
(18) WKUP_GPIO0_13_INTn	>>	WKUP_GPIO0_13_INTn	
(18) WKUP_GPIO0_27_INTn	>>	WKUP_GPIO0_27_INTn	
(33,36) WKUP_OSC0_XIN	>>	WKUP_OSC0_XIN	
(33) WKUP_OSC0_XOUT	>>	WKUP_OSC0_XOUT	
(33) OSC1_XI	>>	OSC1_XI	
(33) OSC1_XOUT	>>	OSC1_XOUT	
(33) WKUP_LFOSC_RTC_XIN	>>	WKUP_LFOSC_RTC_XIN	
(32,33,37,38) SOC_I2C0_SCL	>>	SOC_I2C0_SCL	
(32,33,37,38) SOC_I2C0_SDA	>>	SOC_I2C0_SDA	

## SoC CLOCK



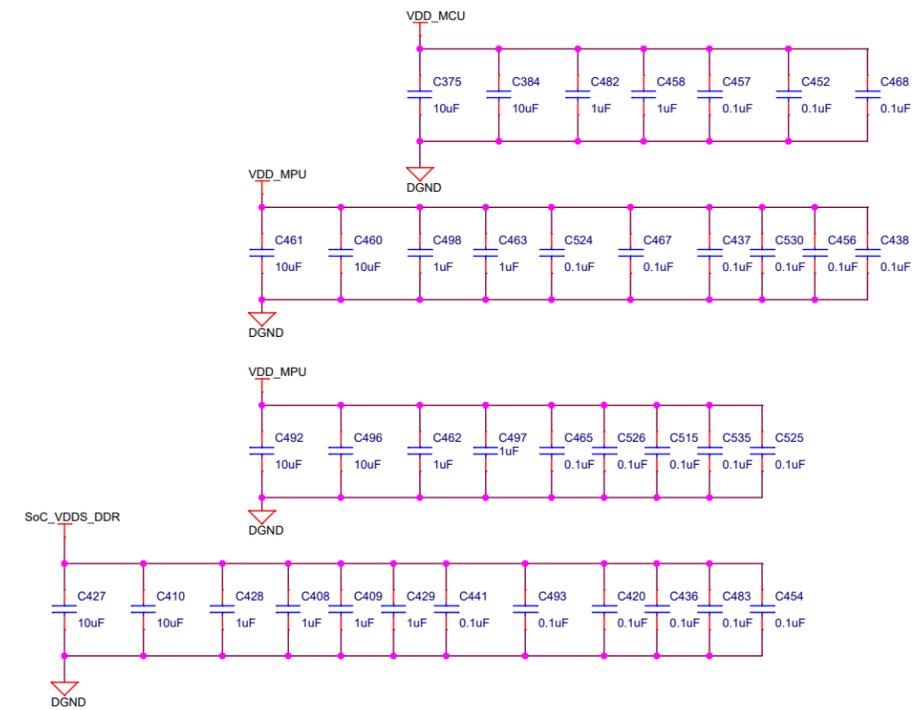
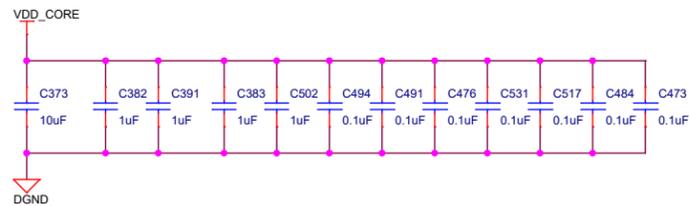
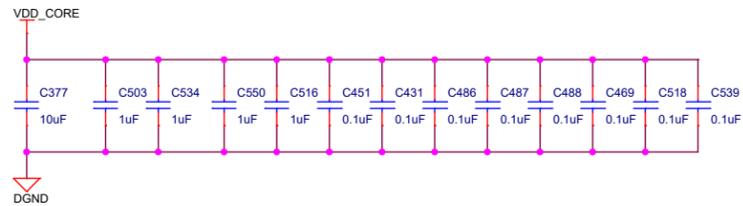
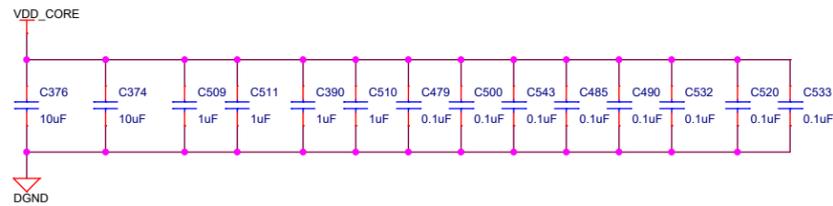
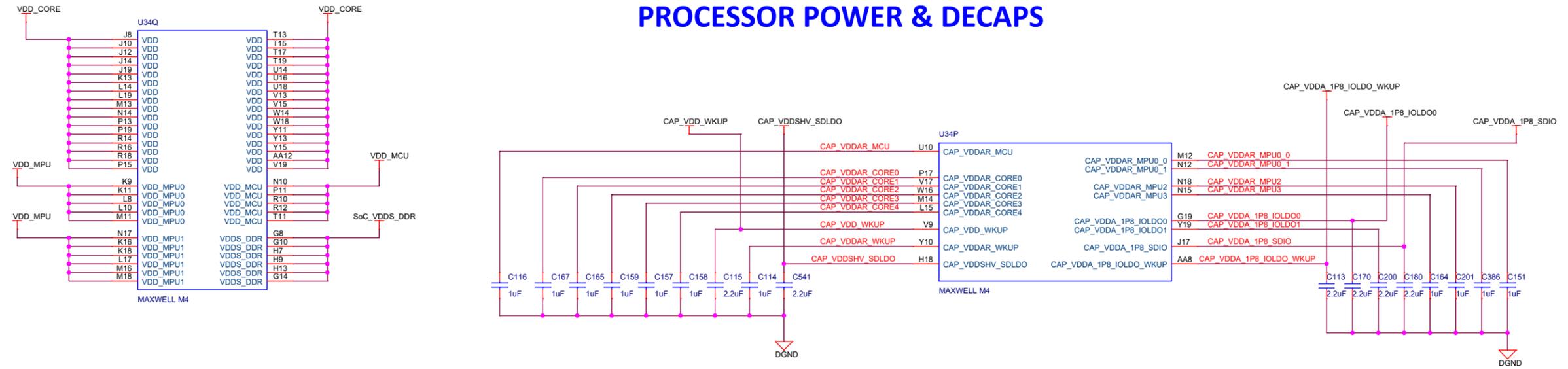
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Title SoC CLOCK & RESET

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
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# PROCESSOR POWER & DECAPS



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Title SoC POWER1

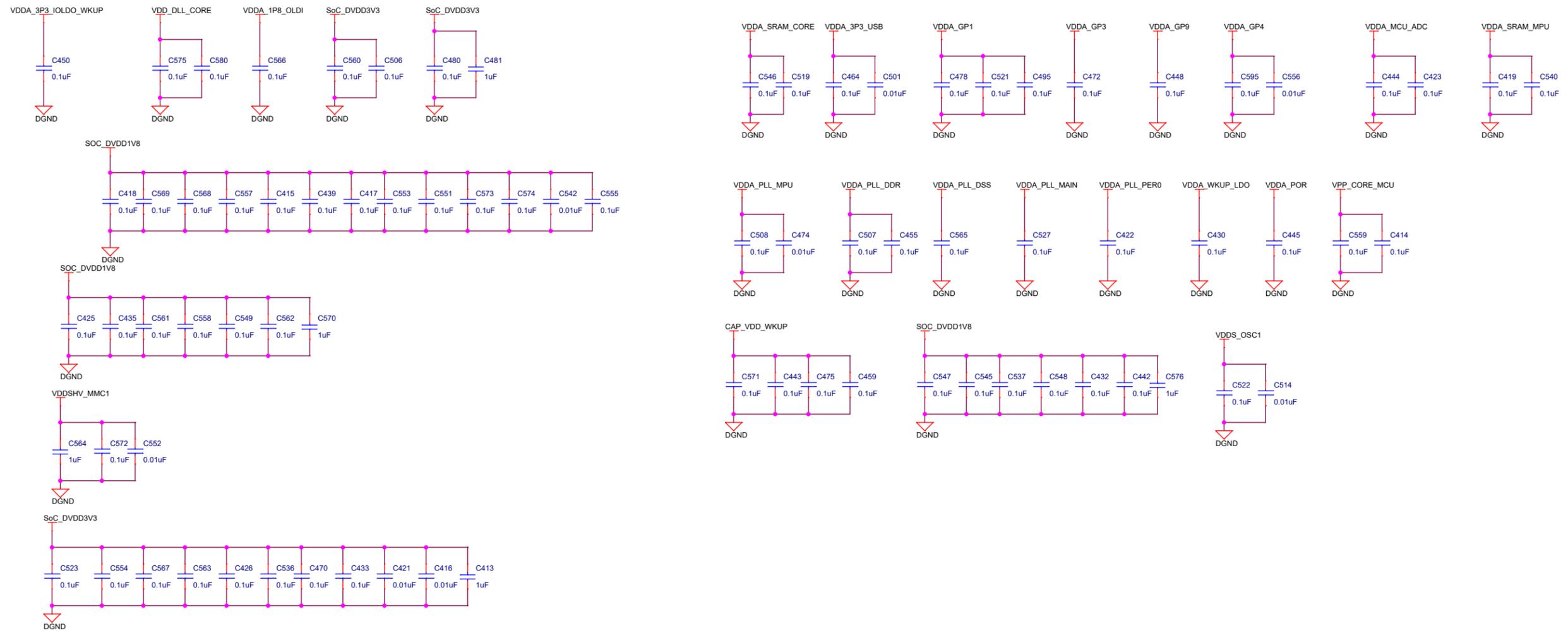
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Date: Friday, August 31, 2018

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# PROCESSOR DECAPS



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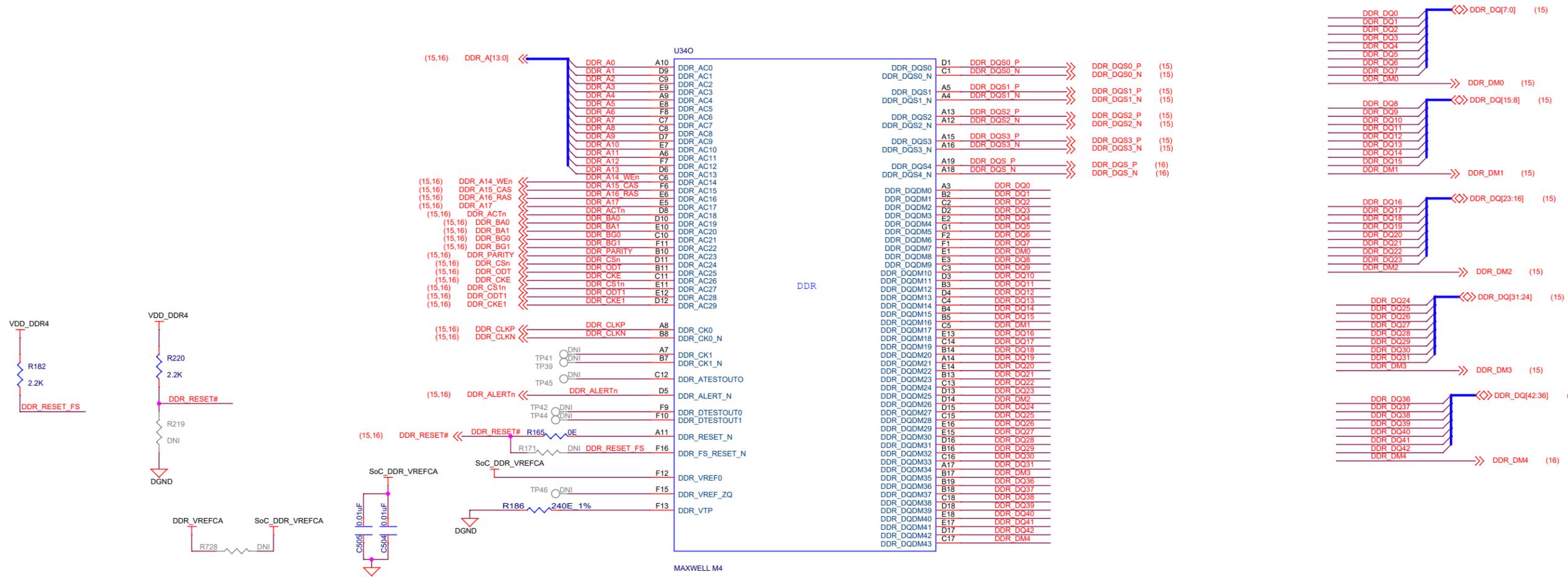
Title SoC POWER3

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
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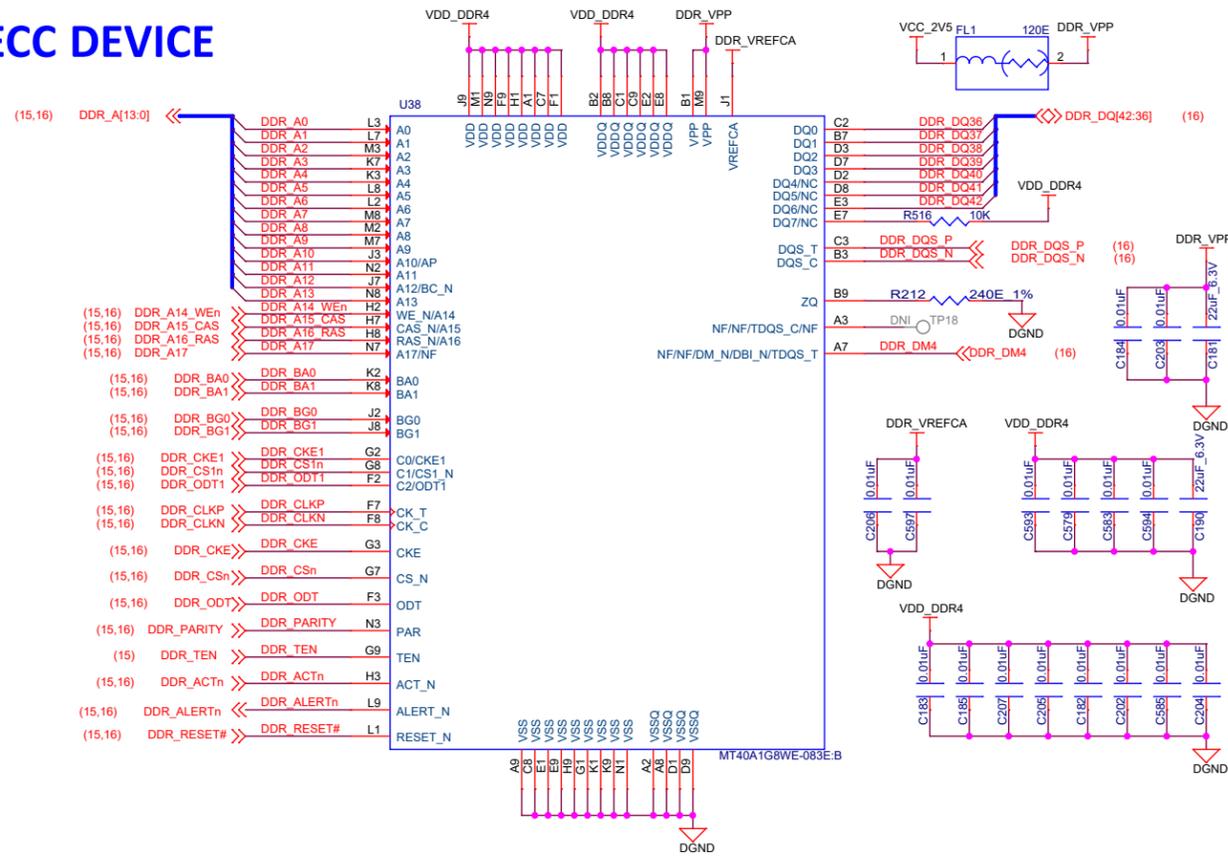




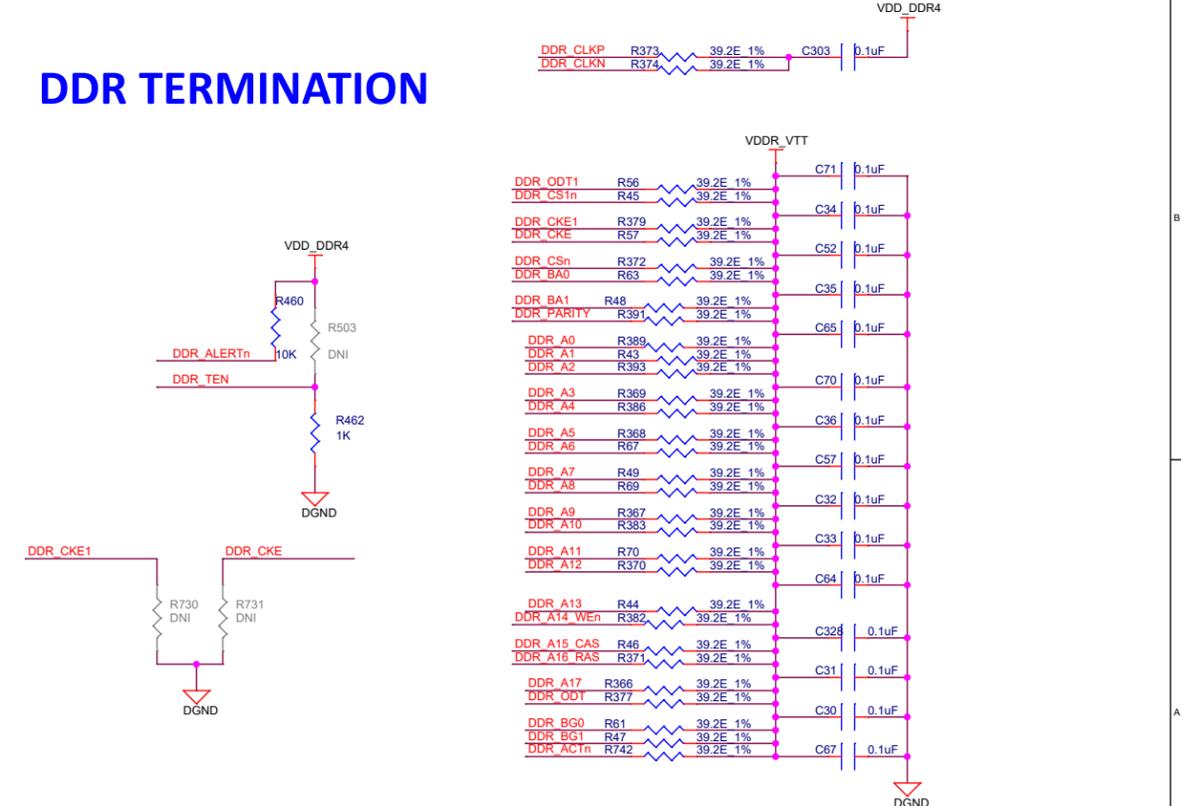
# SoC DDR INTERFACE



# ECC DEVICE



# DDR TERMINATION

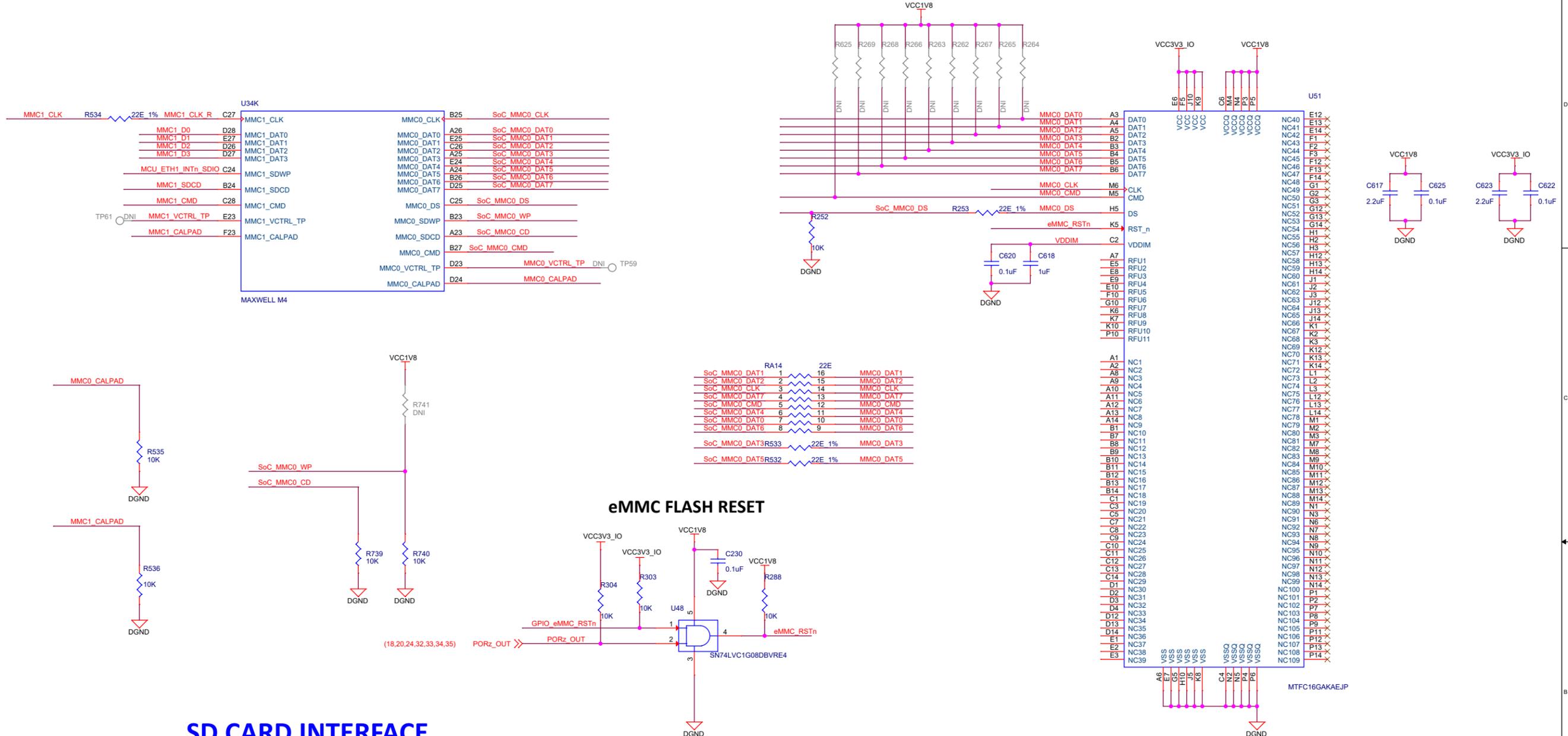


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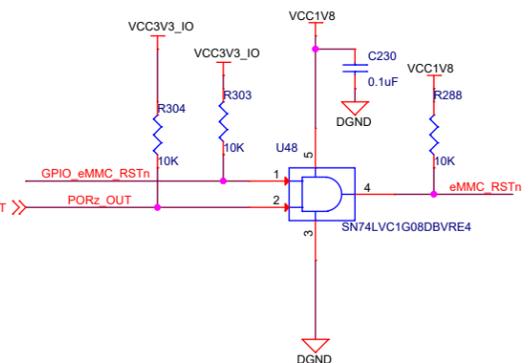


Title: DDR4 ECC & TERMINATIONS		
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E3
Date: Friday, August 31, 2018	Sheet 16 of 44	

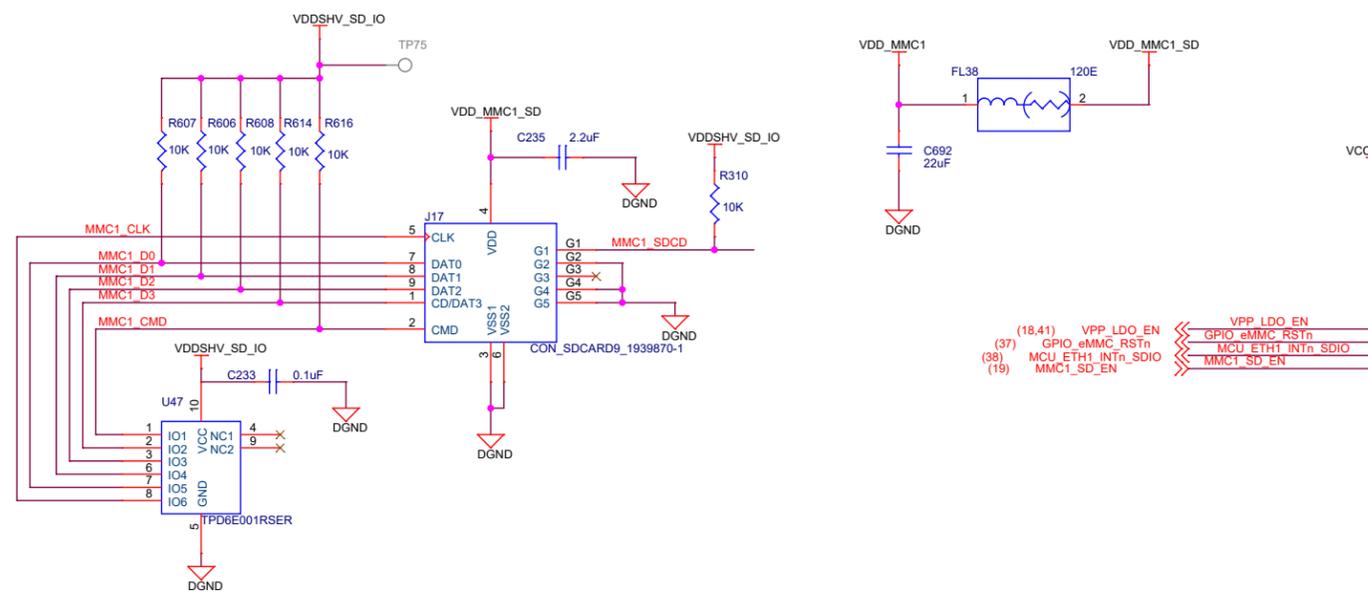
# eMMC FLASH



## eMMC FLASH RESET



## SD CARD INTERFACE

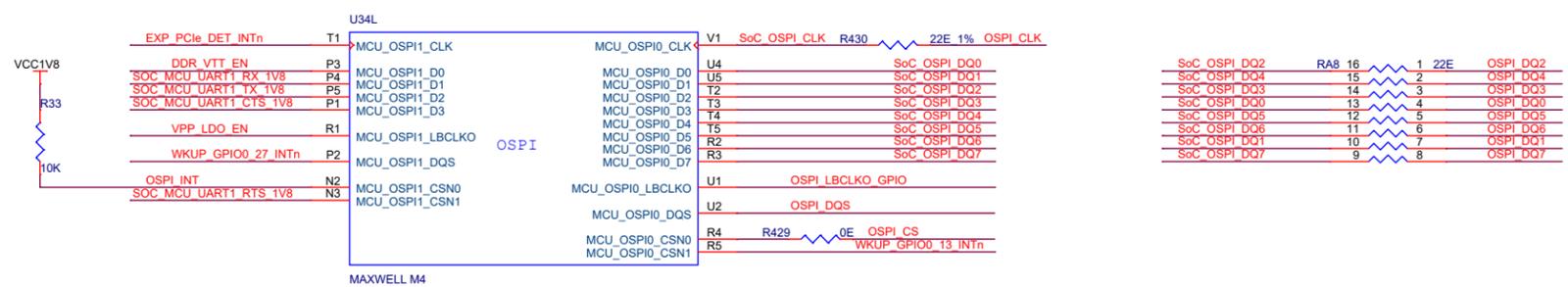
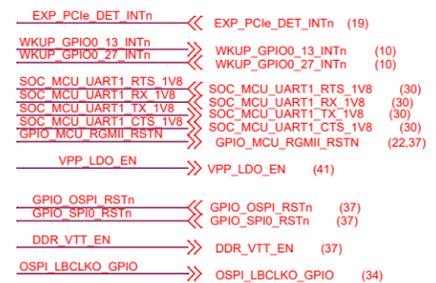


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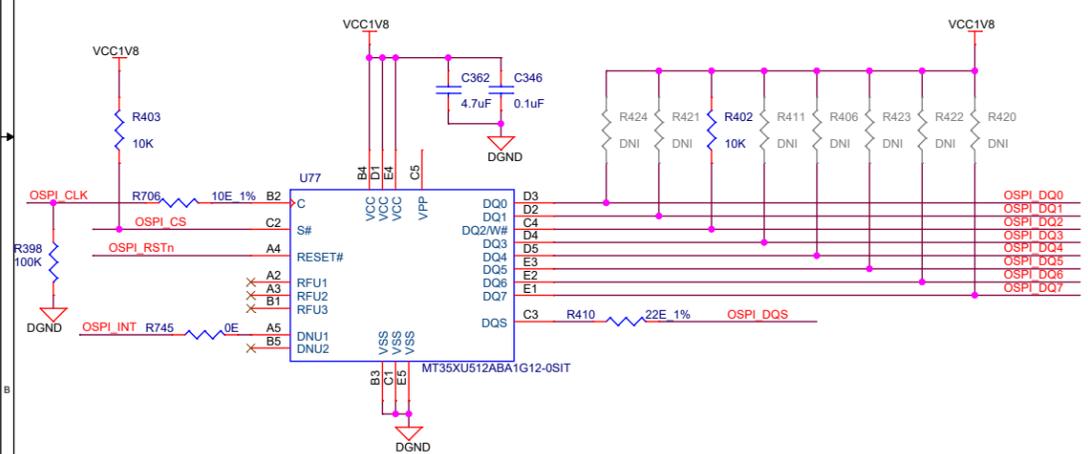


Title		
eMMC_FLASH_SD_CARD_INTERFACE		
Size	Rev	
C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	E3
Date:	Friday, August 31, 2018	Sheet 17 of 44

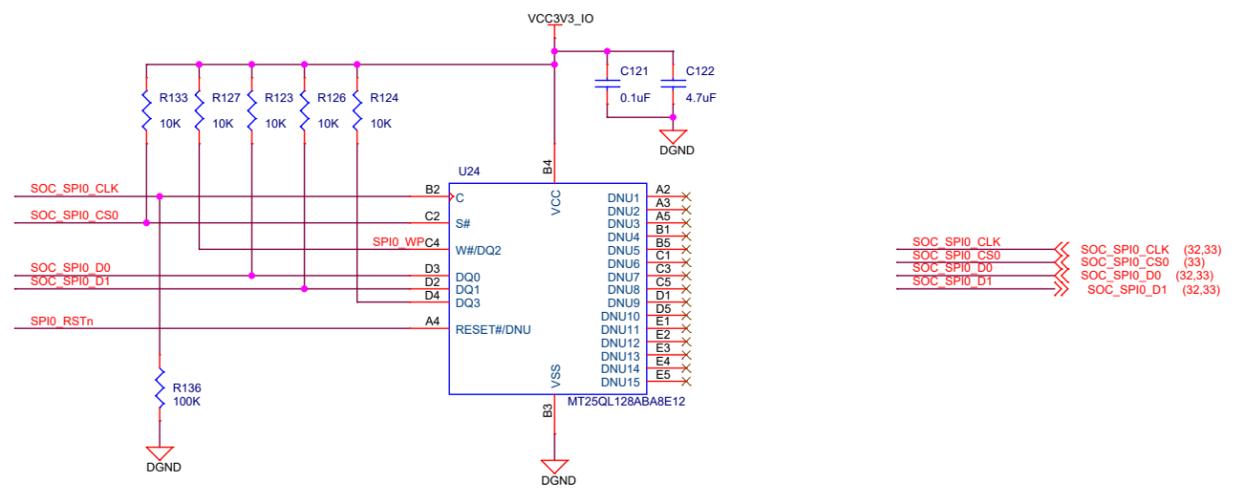
# SOC OSPI INTERFACE



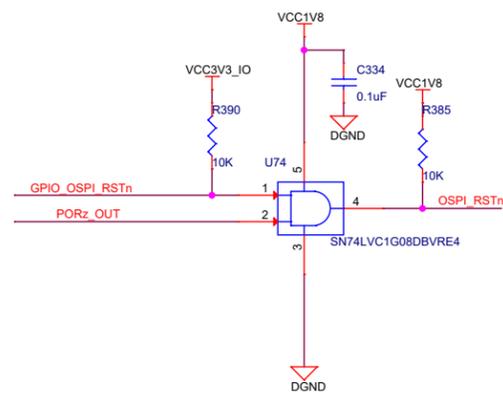
## OSPI FLASH



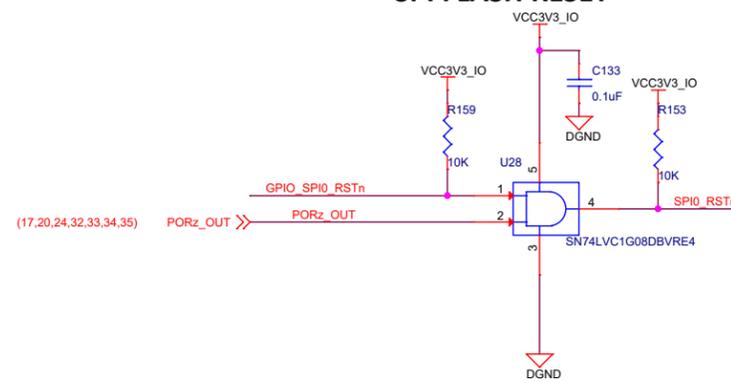
## SPI NOR Flash



## OSPI FLASH RESET



## SPI FLASH RESET



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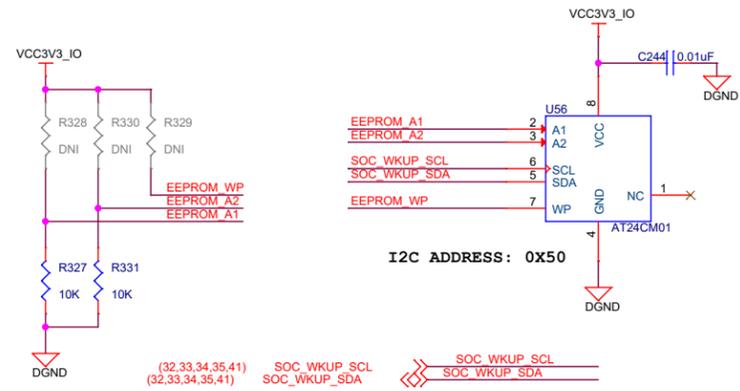
Title OSPI FLASH & SPI NOR FLASH

Size Variant Name = PROC082 001 OPN#TMDX654IDKEVM Rev E3

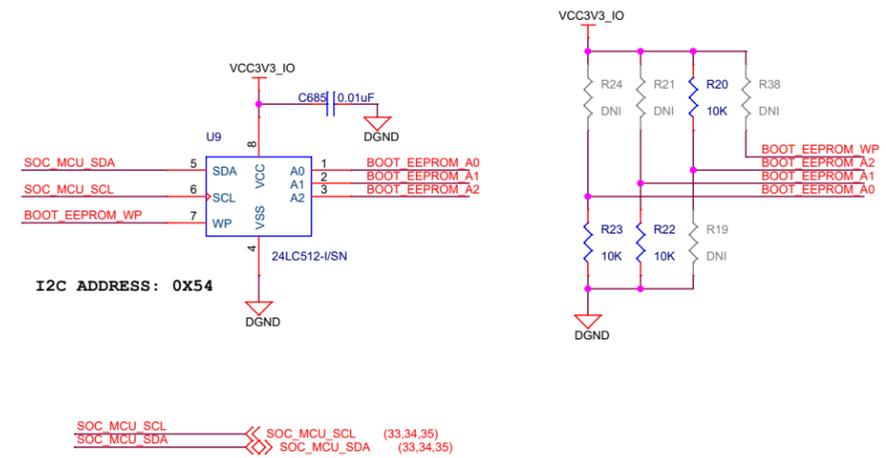
Date: Friday, August 31, 2018

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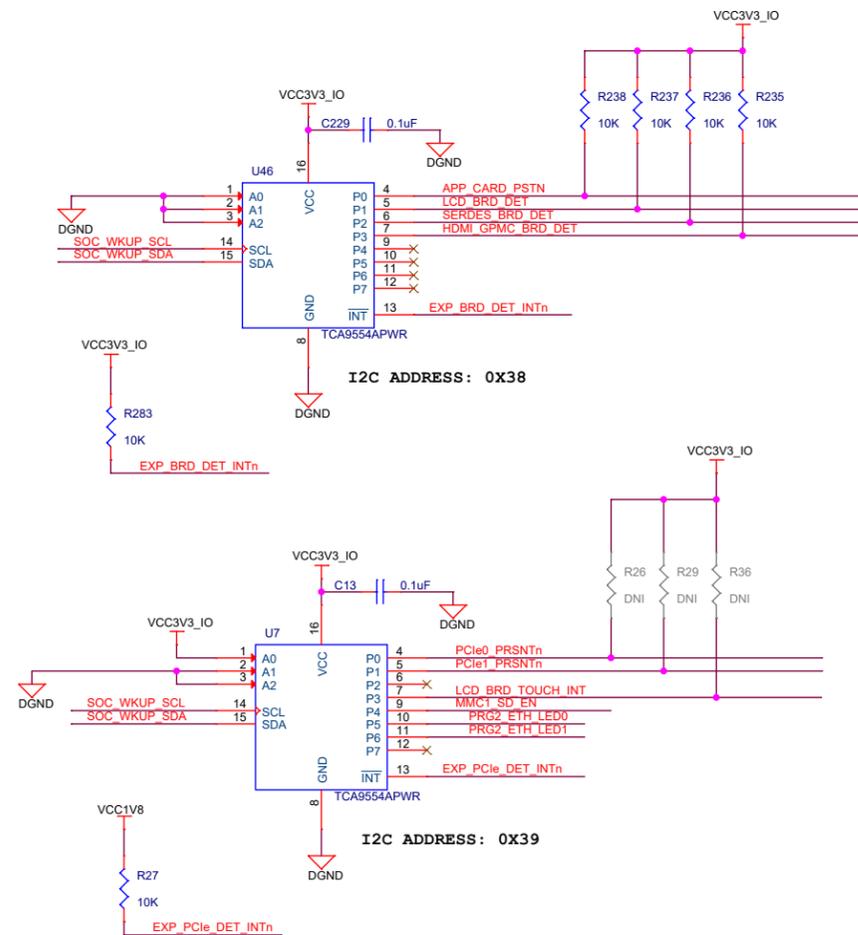
## BOARD ID EEPROM



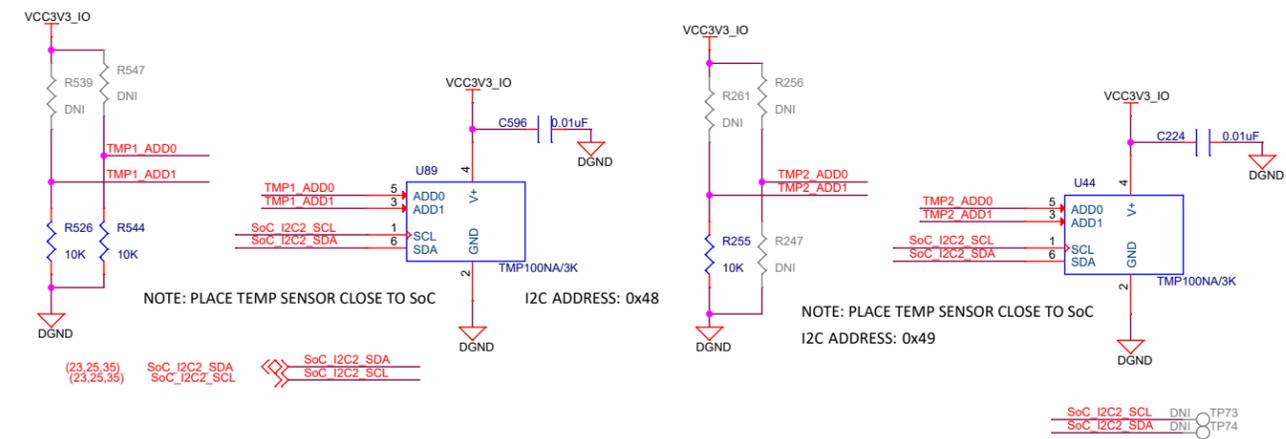
## BOOT EEPROM



## BOARD PRESENCE DETECT CIRCUIT



## TEMPERATURE SENSOR

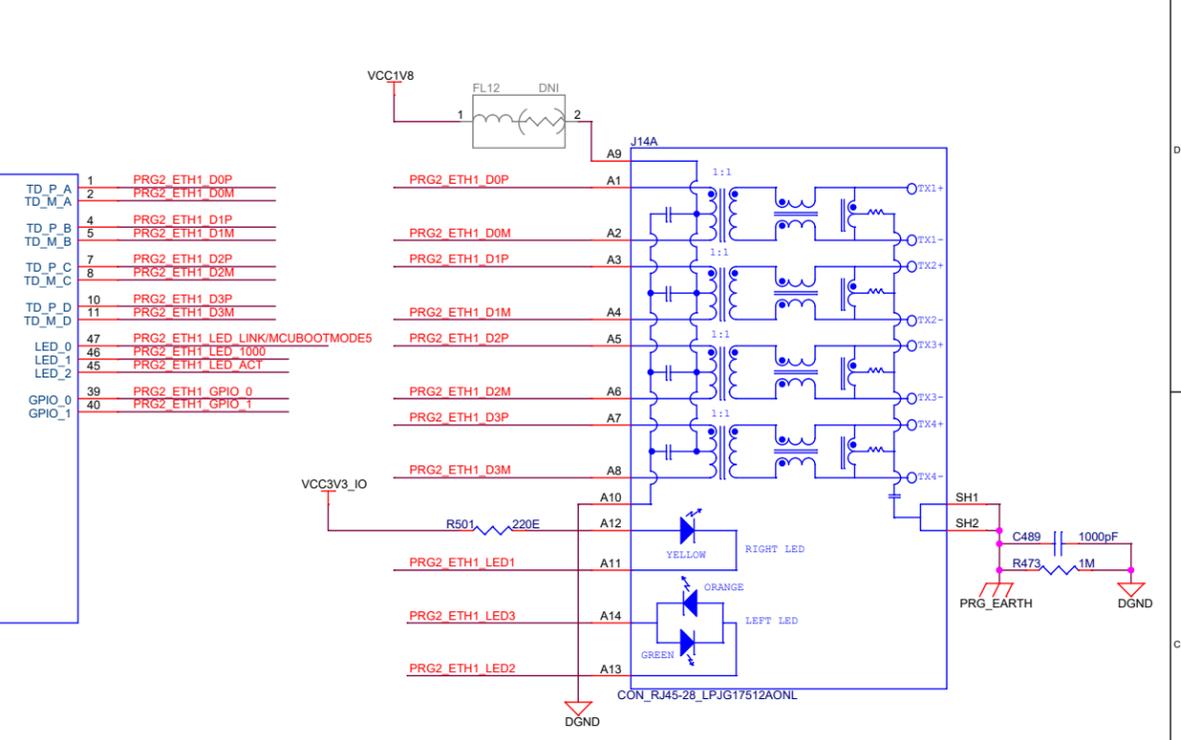
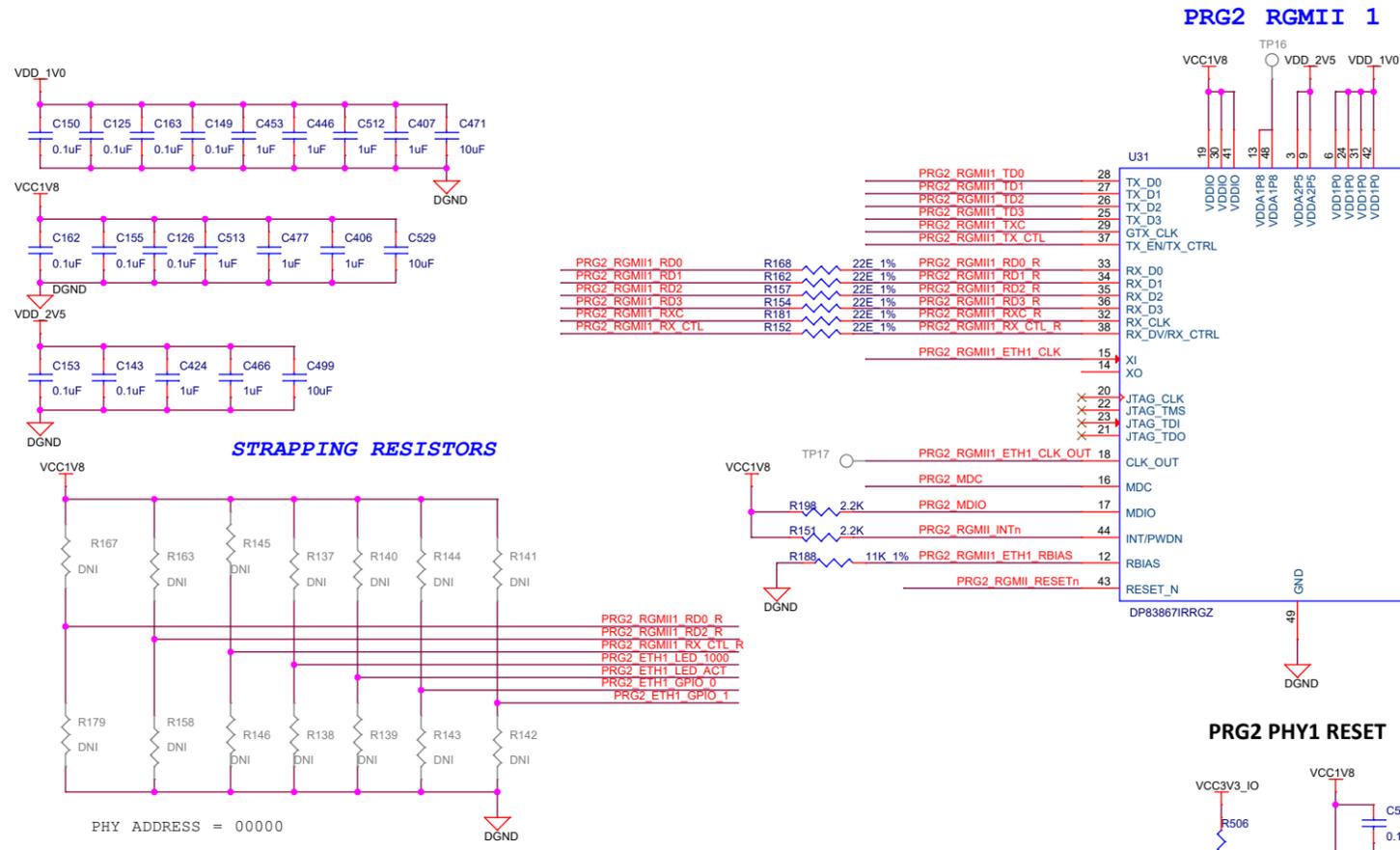


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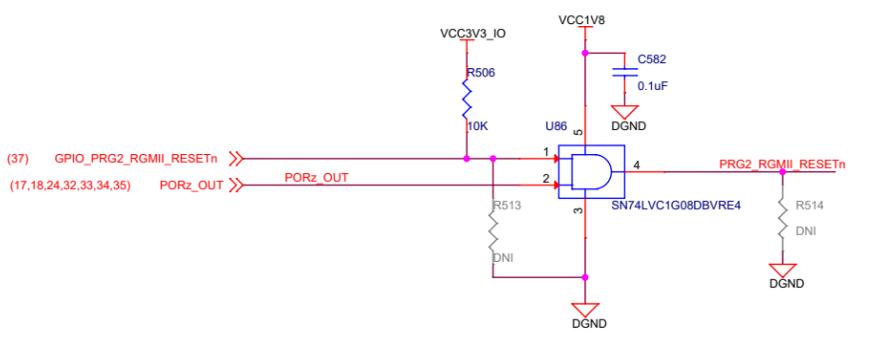


Title EEPROM, PRESENCE DETECTION & TEMP SENSOR

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
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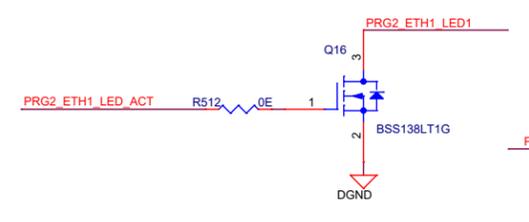
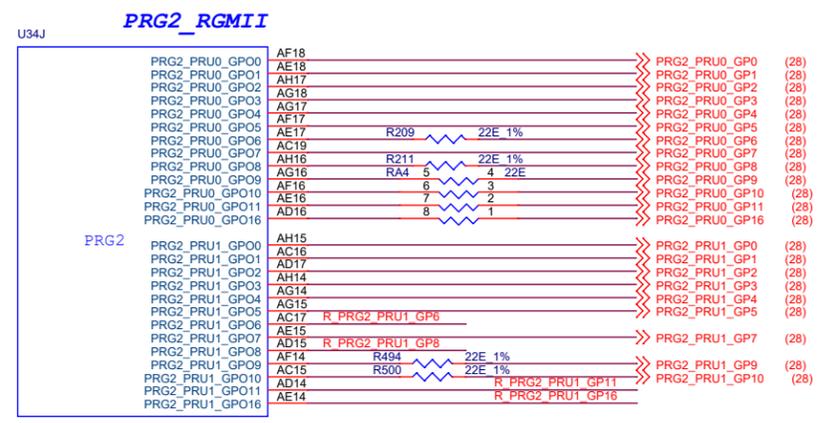


### PRG2 PHY1 RESET

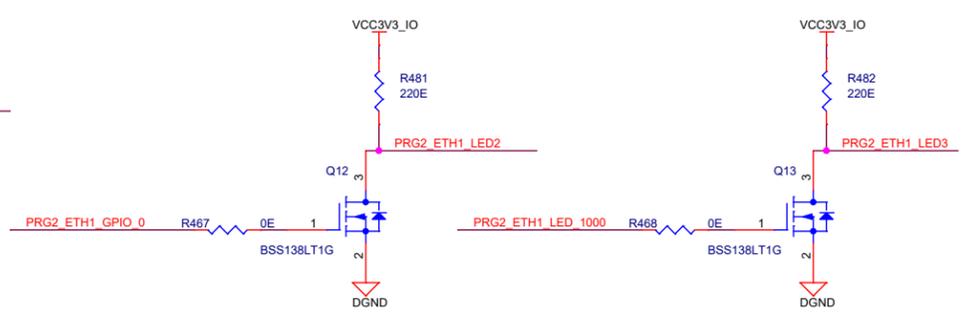


(21,38) PRG2_RGMII1_INTn	<<>	PRG2_RGMII1_INTn
(36) PRG2_RGMII1_ETH1_CLK	<<>	PRG2_RGMII1_ETH1_CLK
(28) PRG2_RGMII1_TD0	<<>	PRG2_RGMII1_TD0
(28) PRG2_RGMII1_TD1	<<>	PRG2_RGMII1_TD1
(28) PRG2_RGMII1_TD2	<<>	PRG2_RGMII1_TD2
(28) PRG2_RGMII1_TD3	<<>	PRG2_RGMII1_TD3
(28) PRG2_RGMII1_TXC	<<>	PRG2_RGMII1_TXC
(28) PRG2_RGMII1_TX_CTL	<<>	PRG2_RGMII1_TX_CTL
(28) PRG2_RGMII1_RD0	<<>	PRG2_RGMII1_RD0
(28) PRG2_RGMII1_RD1	<<>	PRG2_RGMII1_RD1
(28) PRG2_RGMII1_RD2	<<>	PRG2_RGMII1_RD2
(28) PRG2_RGMII1_RD3	<<>	PRG2_RGMII1_RD3
(28) PRG2_RGMII1_RXC	<<>	PRG2_RGMII1_RXC
(28) PRG2_RGMII1_RX_CTL	<<>	PRG2_RGMII1_RX_CTL
(21,28,34) PRG2_MDC	<<>	PRG2_MDC
(21,28,34) PRG2_MDIO	<<>	PRG2_MDIO
(21) PRG2_RGMII1_RESETn	<<>	PRG2_RGMII1_RESETn
(24,33) PRG2_ETH1_LED_LINK/MCUBOOTMODE5	<<>	PRG2_ETH1_LED_LINK/MCUBOOTMODE5

## RGMII ETHERNET PHY - ICSSG



## PRG2\_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS

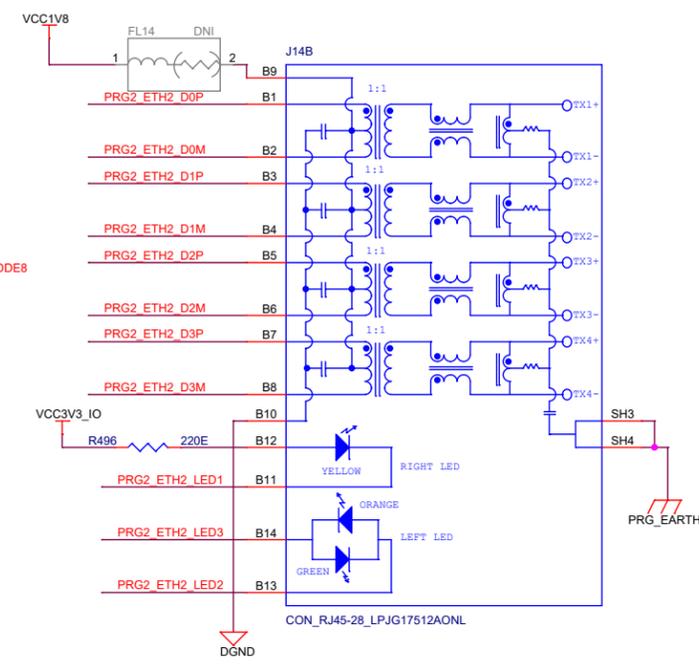
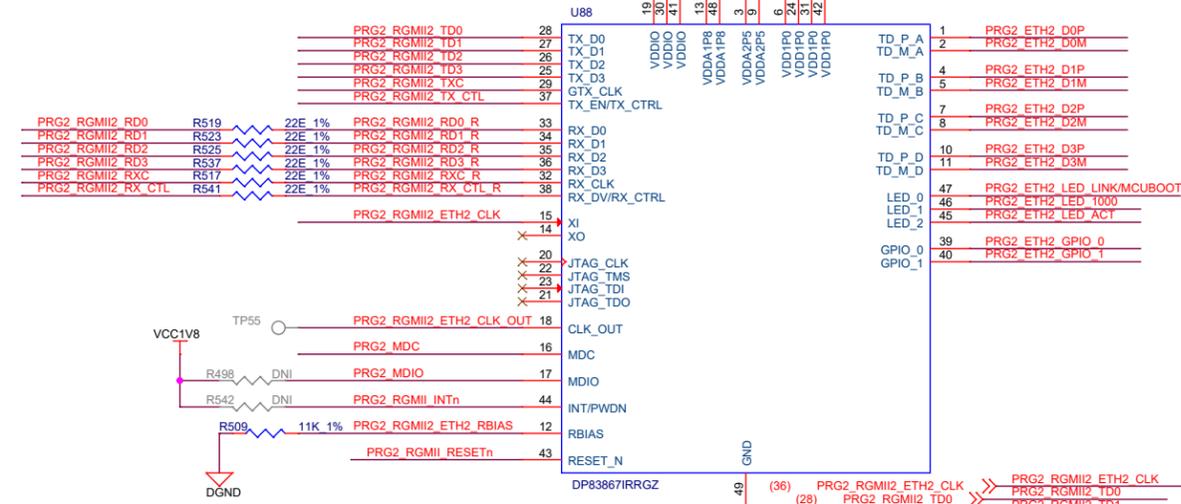
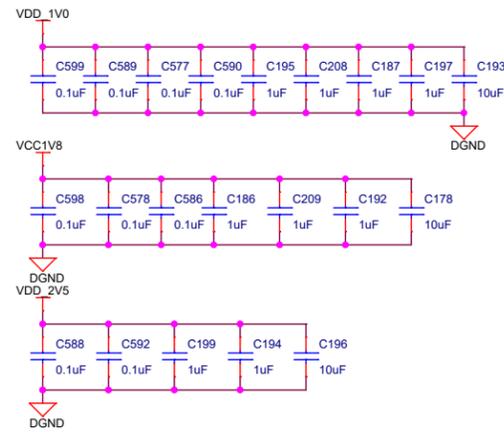


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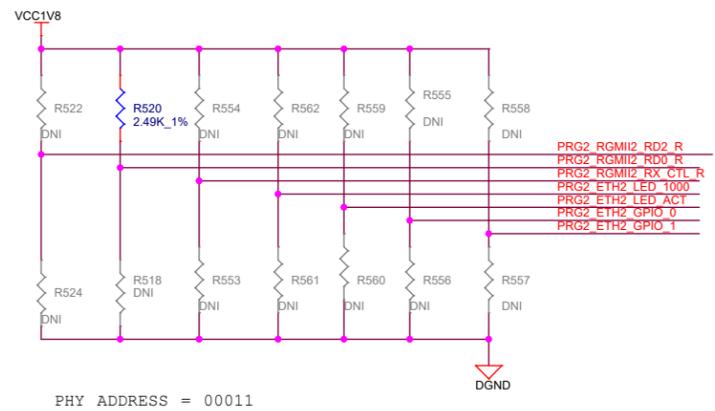
**TEXAS INSTRUMENTS** **MISTRAL**

Title		RGMII ETHERNET PHY - ICSSG PRG2_PRU0	
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev	
C		E3	
Date:	Tuesday, September 04, 2018	Sheet	20 of 44

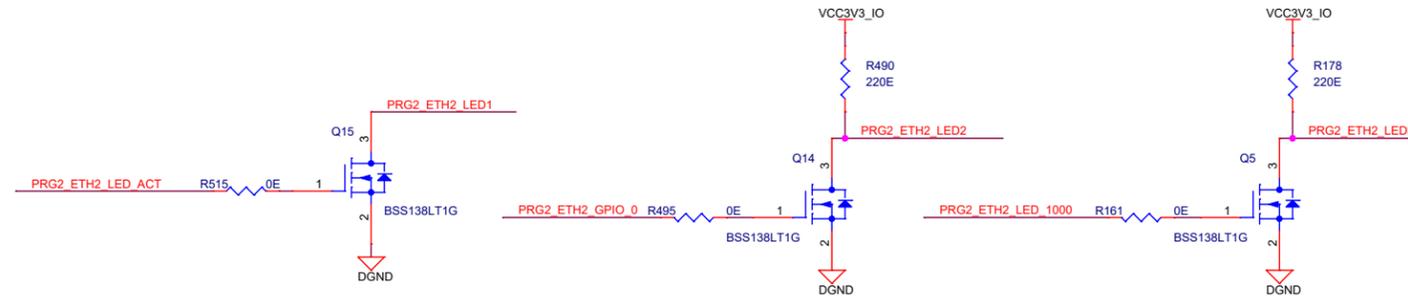
PRG2 RGMII 2



STRAPPING RESISTORS



PRG2\_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



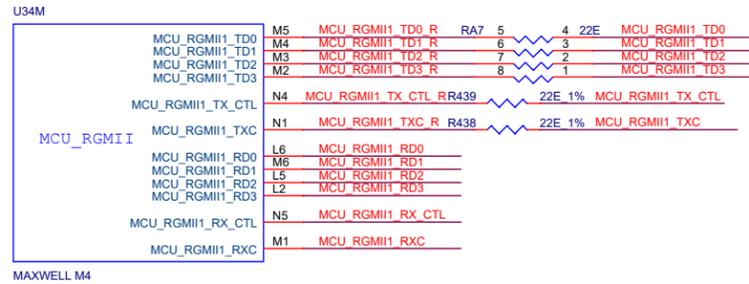
Designed for TI by Mistral Solutions Pvt Ltd



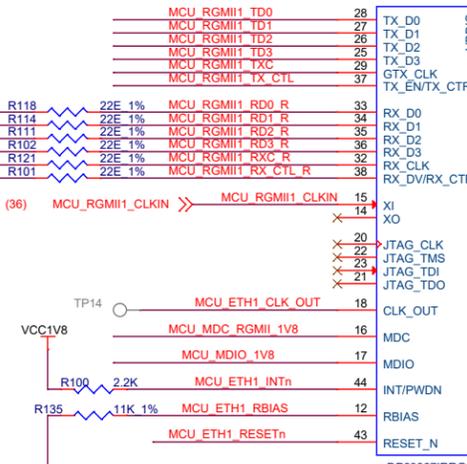
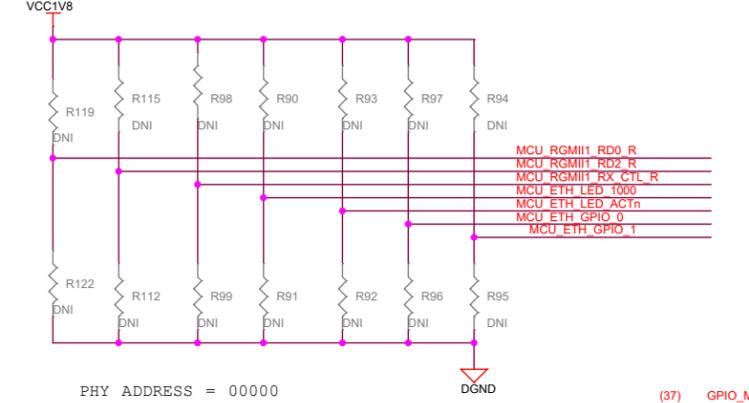
Title		RGMII ETHERNET PHY - ICSSG PRG2_PRU1	
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev	
C		E3	
Date:	Tuesday, September 04, 2018	Sheet	21 of 44

# RGMII ETHERNET PHY - MCU

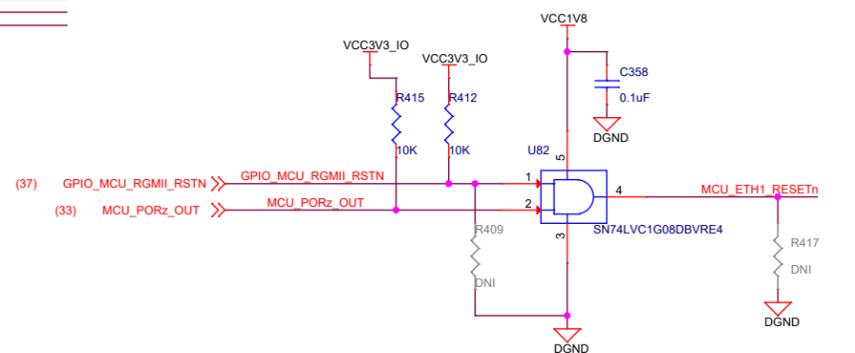
## MCU\_RGMII



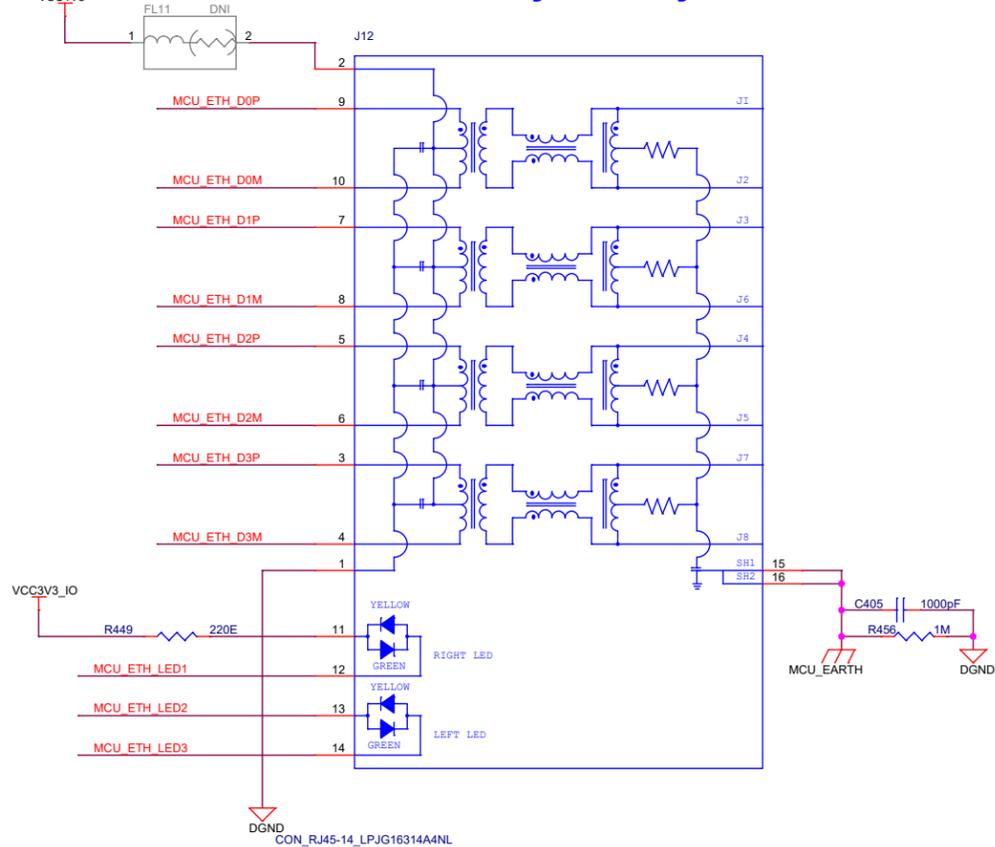
## STRAPPING



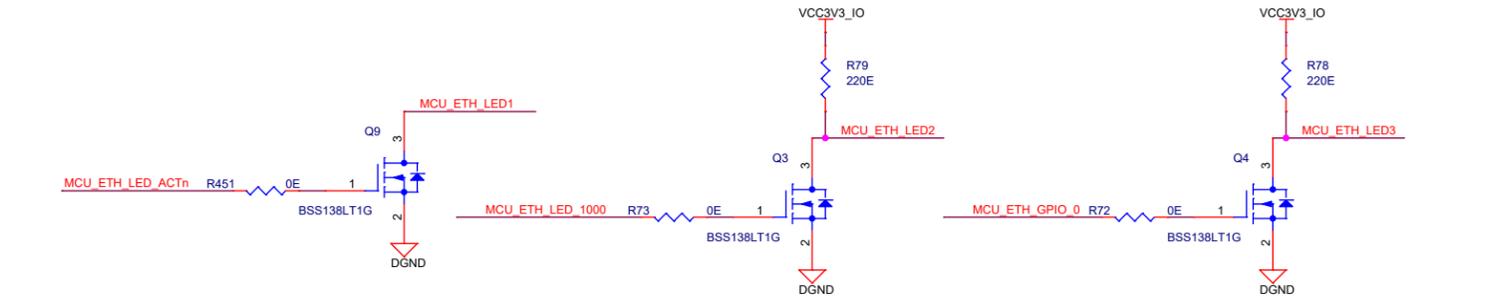
## PHY\_RESET



## RJ45 with Integrated Magnetics



## MCU SPEED & ACTIVITY LED DRIVERS



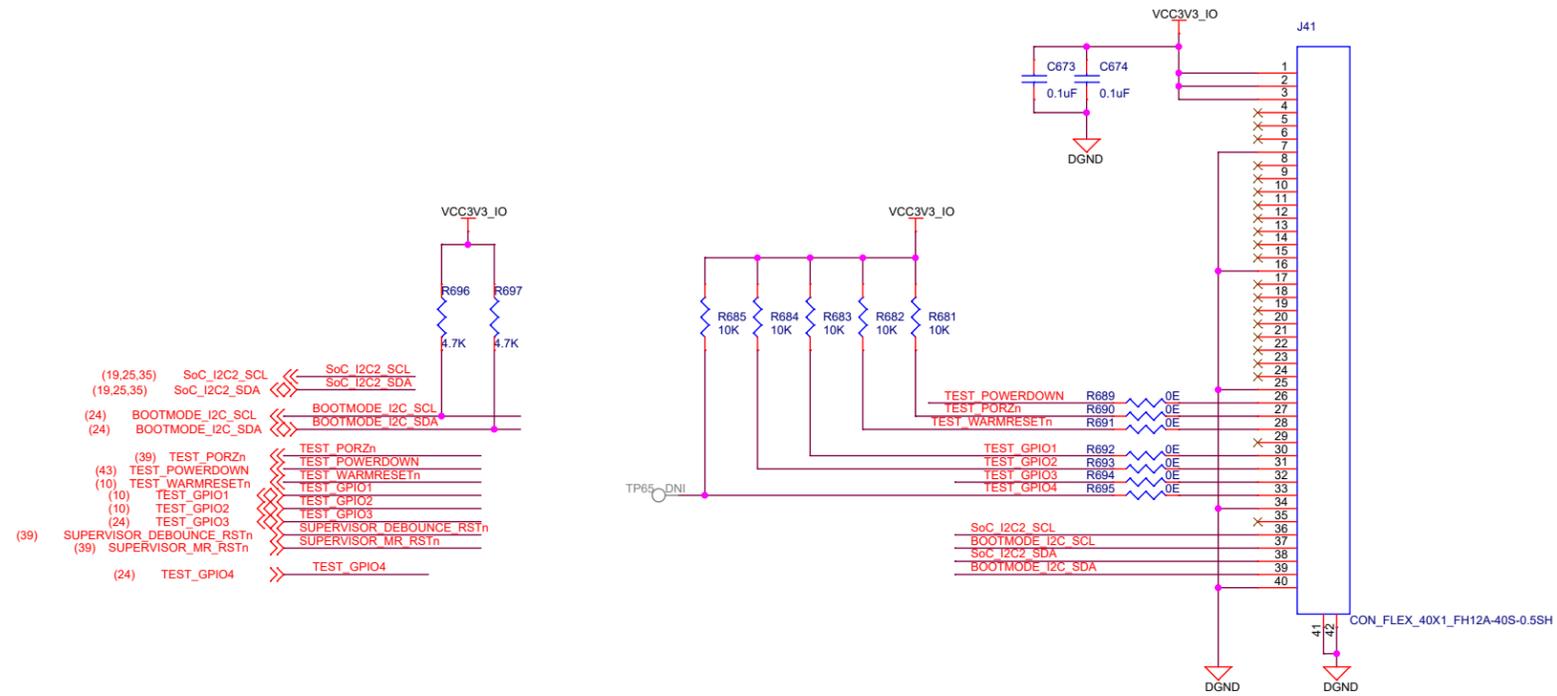
Designed for TI by Mistral Solutions Pvt Ltd

**TEXAS INSTRUMENTS** **MISTRAL**

Title: RGMII ETHERNET PHY - MCU		Rev: E3
Size: C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev: E3
Date: Tuesday, September 04, 2018	Sheet: 22 of 44	

# TEST AUTOMATION

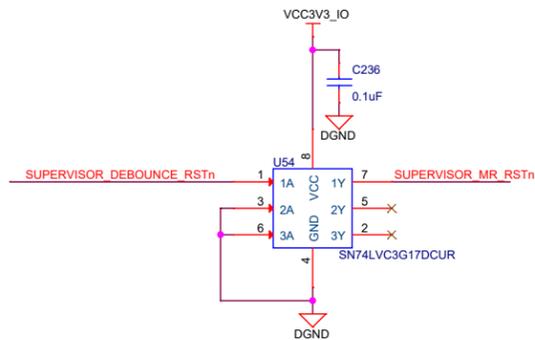
## 40-PIN AUTOMATION HEADER



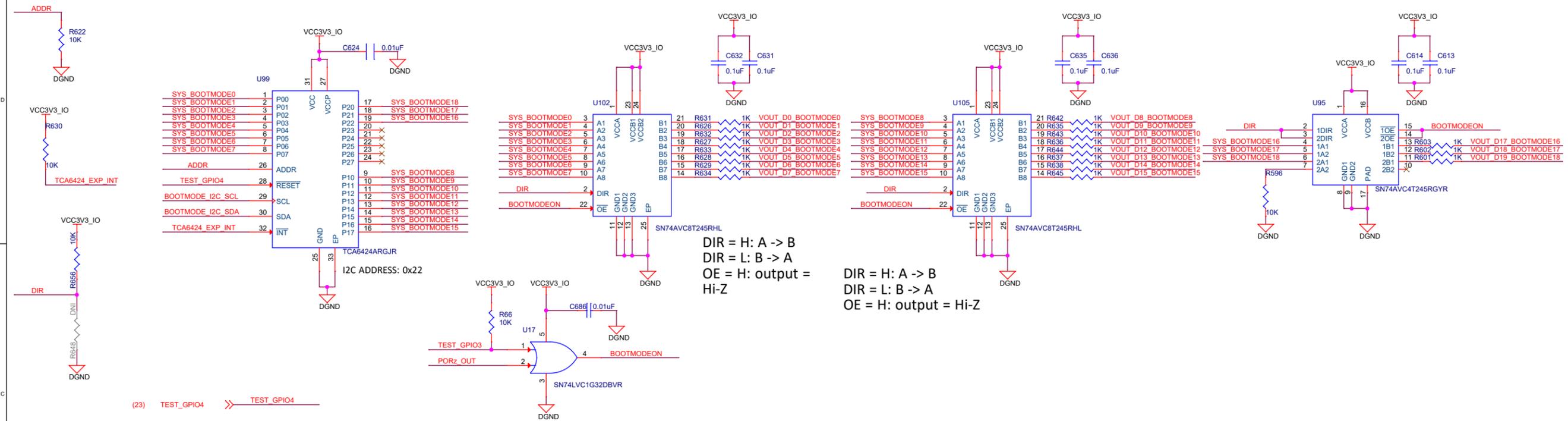
## TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on WKUP_GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Used to Generate the interrupt on WKUP_GPIO0_27_INTn	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

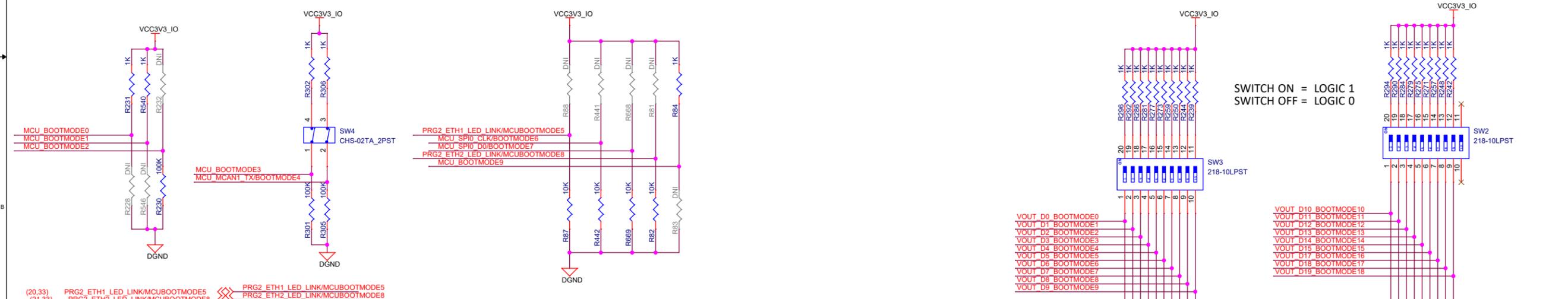
## DEBOUCE CIRCUIT



# BOOT MODE BUFFER & SWITCHES



# BOOT CONFIGURATION SETTINGS



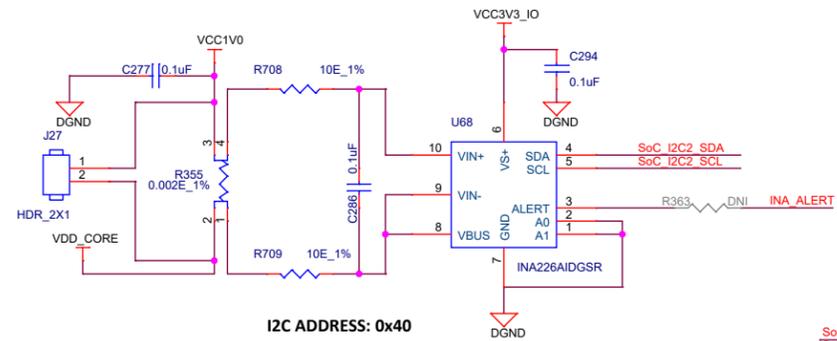
## BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. PCIE (endpoint)
5. CPSW Ethernet Slave
6. USB Host
7. USB Device

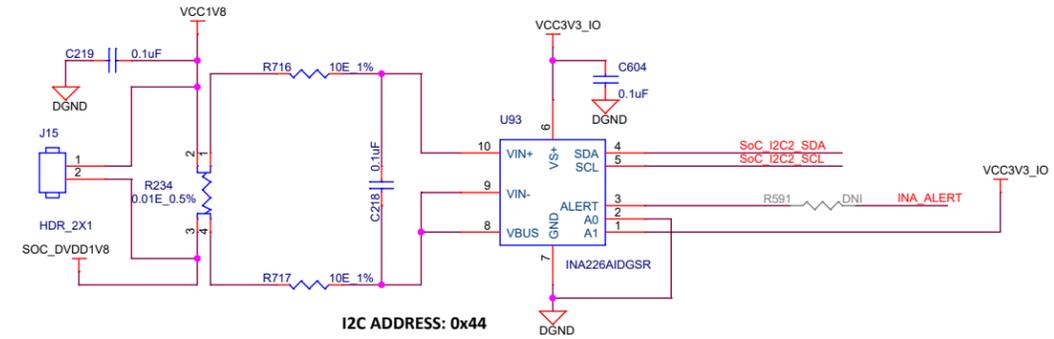
(20,33)	PRG2_ETH1_LED_LINK/MCUBOOTMODE5	PRG2_ETH1_LED_LINK/MCUBOOTMODE5
(21,33)	PRG2_ETH2_LED_LINK/MCUBOOTMODE8	PRG2_ETH2_LED_LINK/MCUBOOTMODE8
(35)	VOUT_D0_BOOTMODE0	VOUT_D0_BOOTMODE0
(35)	VOUT_D1_BOOTMODE1	VOUT_D1_BOOTMODE1
(35)	VOUT_D2_BOOTMODE2	VOUT_D2_BOOTMODE2
(35)	VOUT_D3_BOOTMODE3	VOUT_D3_BOOTMODE3
(35)	VOUT_D4_BOOTMODE4	VOUT_D4_BOOTMODE4
(35)	VOUT_D5_BOOTMODE5	VOUT_D5_BOOTMODE5
(35)	VOUT_D6_BOOTMODE6	VOUT_D6_BOOTMODE6
(35)	VOUT_D7_BOOTMODE7	VOUT_D7_BOOTMODE7
(35)	VOUT_D8_BOOTMODE8	VOUT_D8_BOOTMODE8
(35)	VOUT_D9_BOOTMODE9	VOUT_D9_BOOTMODE9
(35)	VOUT_D10_BOOTMODE10	VOUT_D10_BOOTMODE10
(35)	VOUT_D11_BOOTMODE11	VOUT_D11_BOOTMODE11
(35)	VOUT_D12_BOOTMODE12	VOUT_D12_BOOTMODE12
(35)	VOUT_D13_BOOTMODE13	VOUT_D13_BOOTMODE13
(35)	VOUT_D14_BOOTMODE14	VOUT_D14_BOOTMODE14
(35)	VOUT_D15_BOOTMODE15	VOUT_D15_BOOTMODE15
(35)	VOUT_D16_BOOTMODE16	VOUT_D16_BOOTMODE16
(35)	VOUT_D17_BOOTMODE17	VOUT_D17_BOOTMODE17
(35)	VOUT_D18_BOOTMODE18	VOUT_D18_BOOTMODE18
(35)	VOUT_D19_BOOTMODE19	VOUT_D19_BOOTMODE19
(33,37)	MCU_BOOTMODE0	MCU_BOOTMODE0
(33,37)	MCU_BOOTMODE1	MCU_BOOTMODE1
(33)	MCU_BOOTMODE2	MCU_BOOTMODE2
(33)	MCU_BOOTMODE3	MCU_BOOTMODE3
(33)	MCU_MCANT1_TX/BOOTMODE4	MCU_MCANT1_TX/BOOTMODE4
(33)	MCU_SPI0_CLK/BOOTMODE6	MCU_SPI0_CLK/BOOTMODE6
(33,35)	MCU_SPI0_D0/BOOTMODE7	MCU_SPI0_D0/BOOTMODE7
(33)	MCU_BOOTMODE9	MCU_BOOTMODE9
(17,18,20,32,33,34,35)	PORz_OUT	PORz_OUT
(23)	TEST_GPIO3	TEST_GPIO3
(33,34,39)	SoC_PORz	SoC_PORz
(23)	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
(23)	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA

# CURRENT MONITORING DEVICES

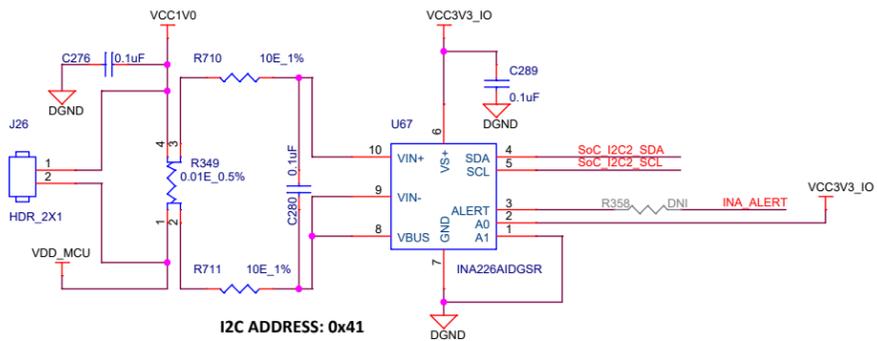
## VDD\_CORE



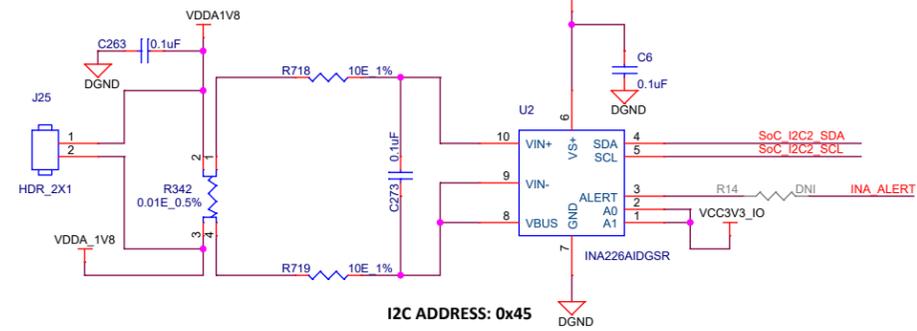
## SoC\_DVDD1V8



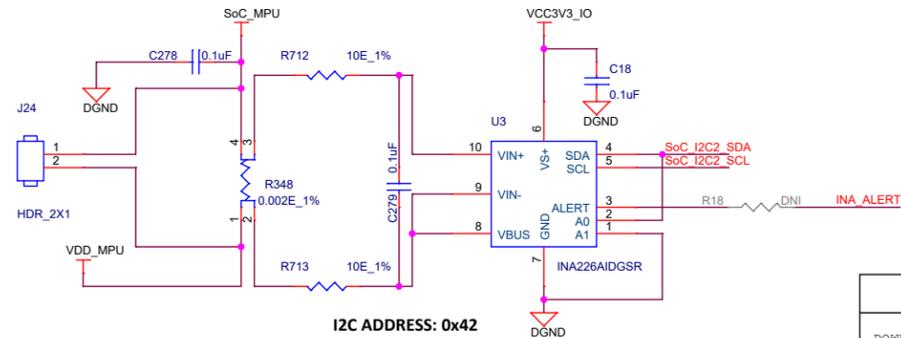
## VDD\_MCU



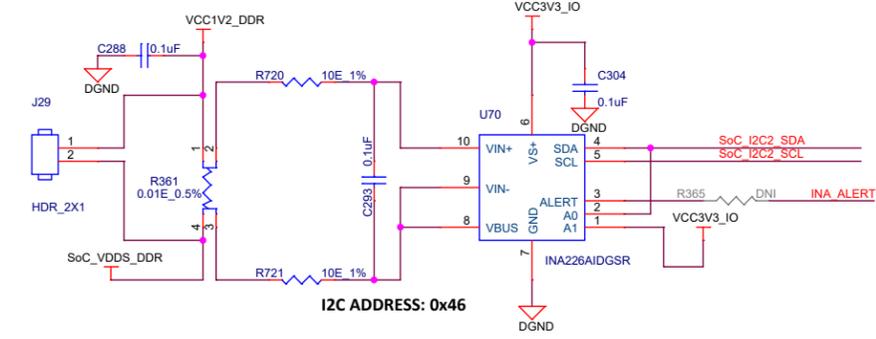
## SoC\_AVDD1V8



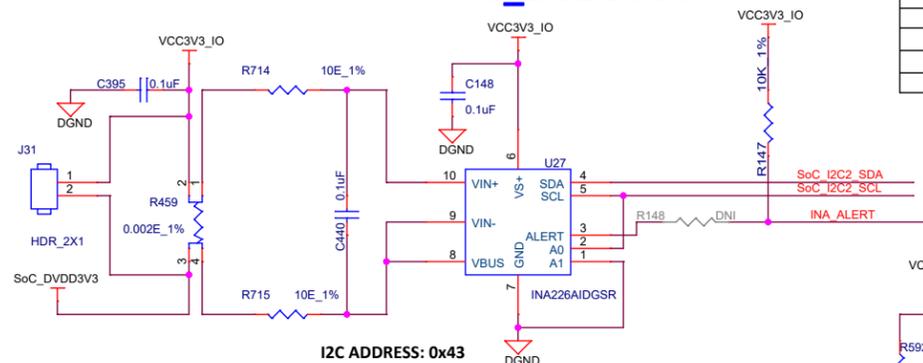
## VDD\_MPU



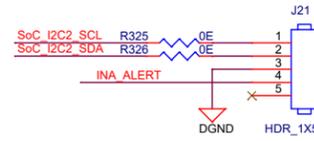
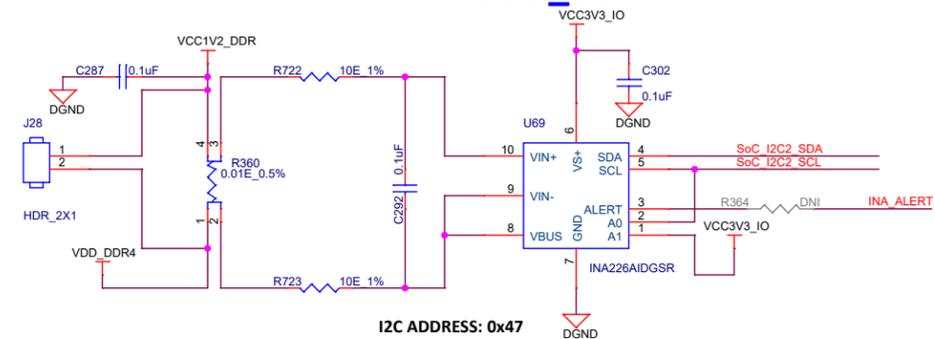
## SoC\_VDDS\_DDR



## SoC\_DVDD3V3



## VDD\_DDR



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC1V0	VDD_CORE	40
VCC1V0	VDD_MCU	41
SoC MPU	VDD_MPU	42
VCC3V3_IO	SoC_DVDD3V3	43
VCC1V8	SoC_DVDD1V8	44
VDDA1V8	SoC_AVDD1V8	45
VCC1V2_DDR	SoC_VDDS_DDR	46
VCC1V2_DDR	VDD_DDR	47



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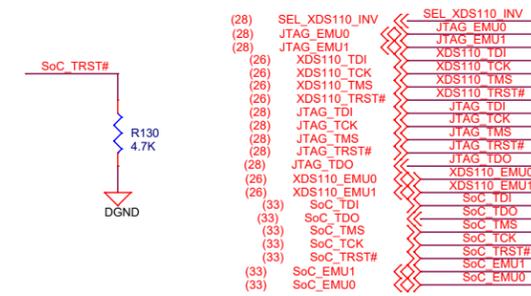
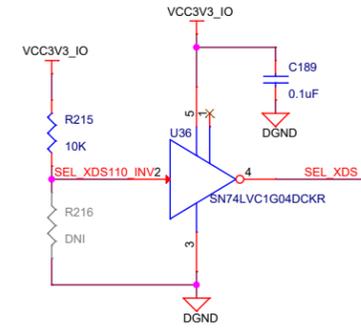


Title CURRENT MONITORING DEVICES

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 25 of 44

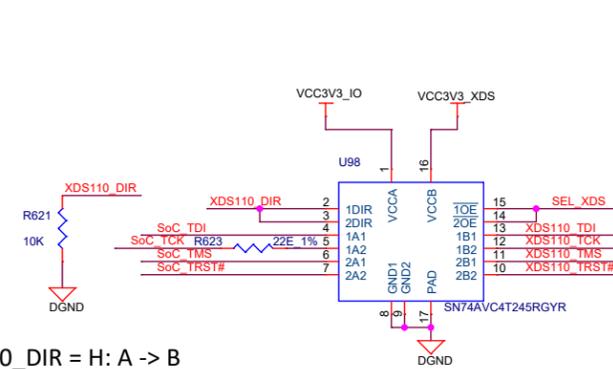


# JTAG BUFFER

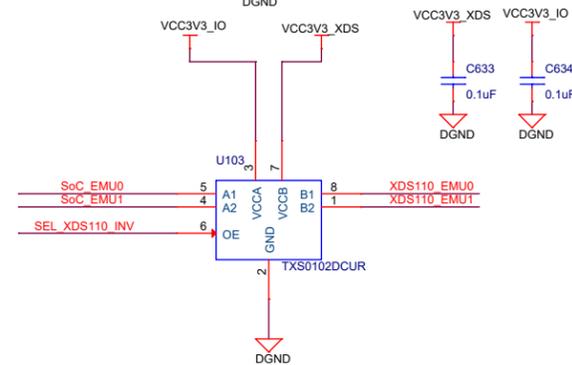
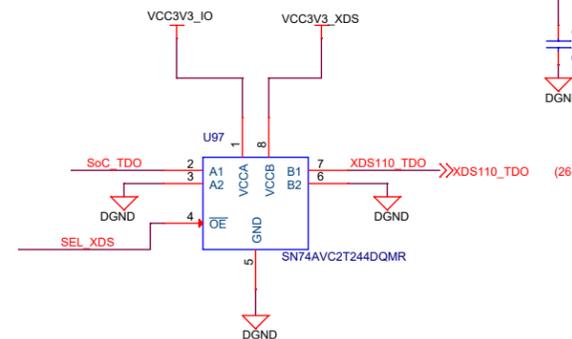


(28)	SEL_XDS110_INV	SEL_XDS110_INV
(28)	JTAG_EMU0	JTAG_EMU0
(28)	JTAG_EMU1	JTAG_EMU1
(26)	XDS110_TDI	XDS110_TDI
(26)	XDS110_TCK	XDS110_TCK
(26)	XDS110_TMS	XDS110_TMS
(26)	XDS110_TRST#	XDS110_TRST#
(28)	JTAG_TDI	JTAG_TDI
(28)	JTAG_TCK	JTAG_TCK
(28)	JTAG_TMS	JTAG_TMS
(28)	JTAG_TRST#	JTAG_TRST#
(28)	JTAG_TDO	JTAG_TDO
(28)	JTAG_TDO	XDS110_EMU0
(26)	XDS110_EMU0	XDS110_EMU1
(26)	XDS110_EMU1	XDS110_EMU1
(33)	SoC_TDI	SoC_TDI
(33)	SoC_TDO	SoC_TDO
(33)	SoC_TMS	SoC_TMS
(33)	SoC_TCK	SoC_TCK
(33)	SoC_TRST#	SoC_TRST#
(33)	SoC_EMU1	SoC_EMU1
(33)	SoC_EMU0	SoC_EMU0

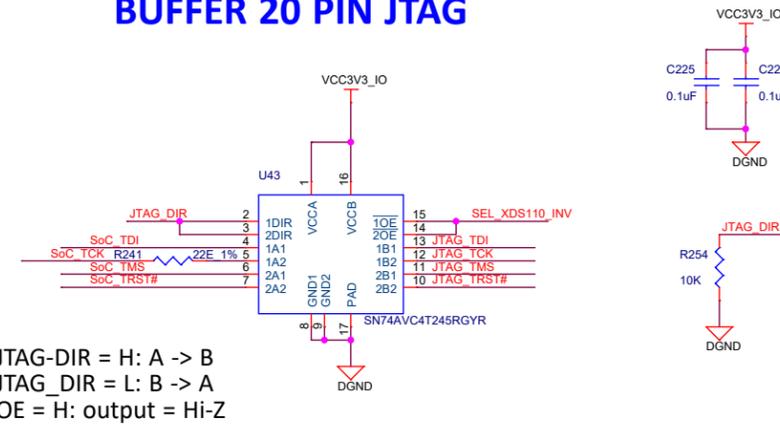
## BUFFER XDS110



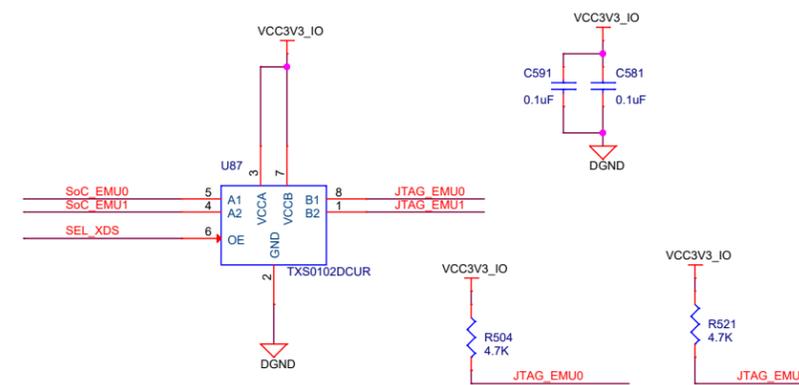
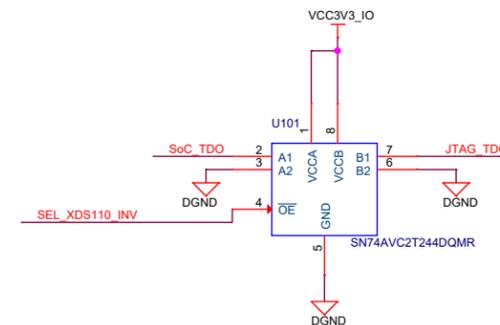
XDS110\_DIR = H: A -> B  
 XDS110\_DIR = L: B -> A  
 OE = H: output = Hi-Z



## BUFFER 20 PIN JTAG



JTAG\_DIR = H: A -> B  
 JTAG\_DIR = L: B -> A  
 OE = H: output = Hi-Z



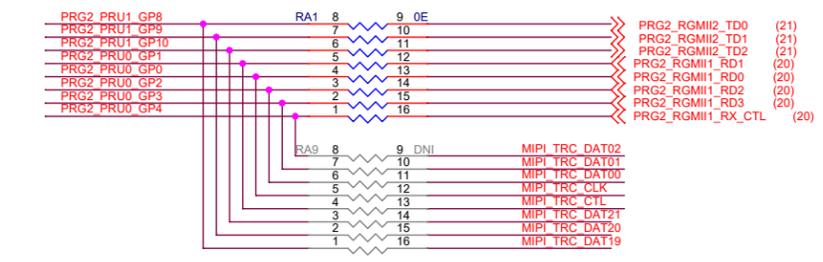
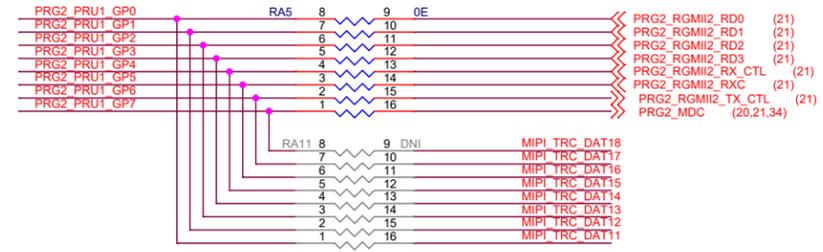
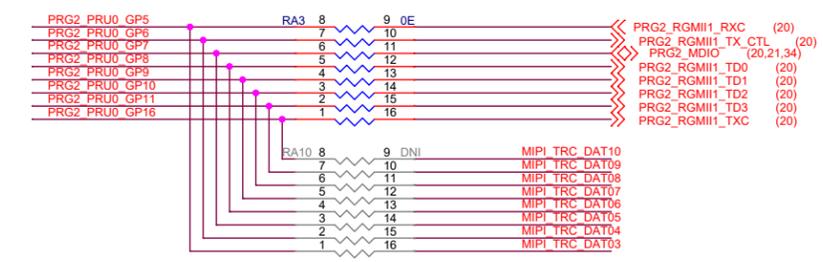
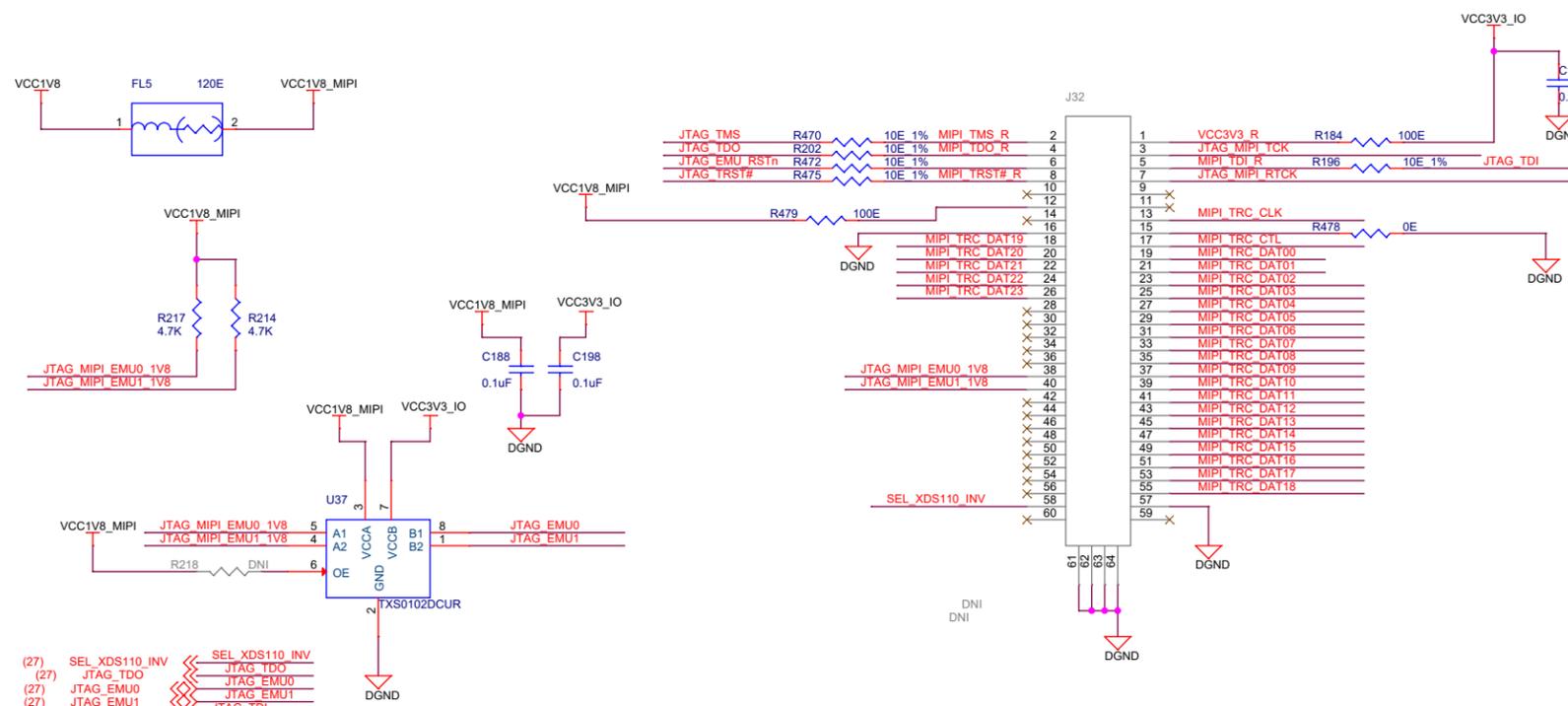
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Title		JTAG BUFFER
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Friday, August 31, 2018	Sheet 27 of 44

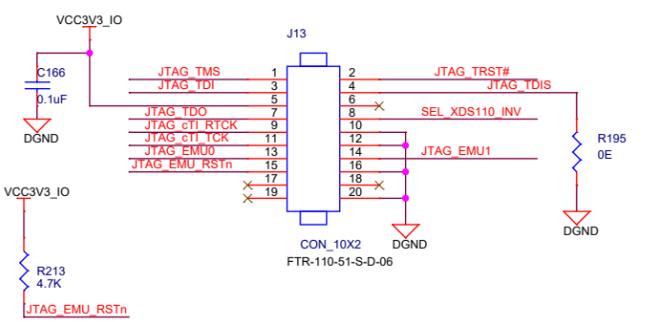
# MIPI 60 PIN CONNECTOR

0- Ohm Res MUX between PRG2\_Ethernet PHY (CP Board PHY) and JTAG TRACE Functionality  
 -For PRG2\_Ethernet PHY RA3, RA5, RA1, R180 & R183 Should be installed and RA10, RA11, RA9, R466 & R463 Should be DNI'd.  
 -For TRACE RA10, RA11, RA9, R466 & R463 Should be Installed and RA3, RA5, RA1, R180 & R183 Should be DNI'd.

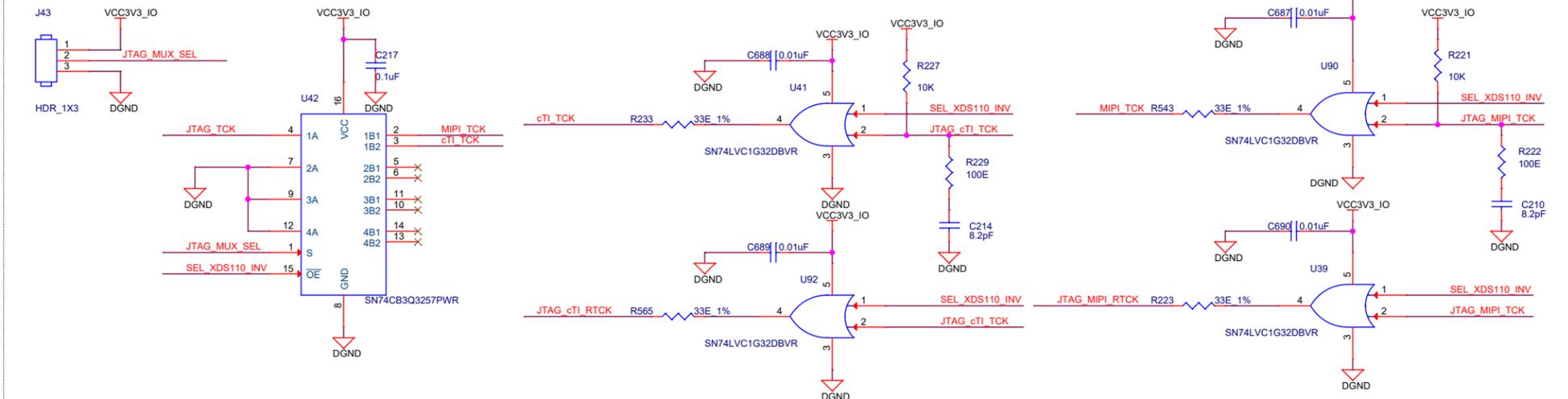


- (27) SEL\_XDS110\_INV
- (27) JTAG\_TDO
- (27) JTAG\_EMU0
- (27) JTAG\_EMU1
- (27) JTAG\_TDI
- (27) JTAG\_TCK
- (27) JTAG\_TMS
- (27) JTAG\_TRST#
- (20) PRG2\_PRU0\_GP0
- (20) PRG2\_PRU0\_GP1
- (20) PRG2\_PRU0\_GP2
- (20) PRG2\_PRU0\_GP3
- (20) PRG2\_PRU0\_GP4
- (20) PRG2\_PRU0\_GP5
- (20) PRG2\_PRU0\_GP6
- (20) PRG2\_PRU0\_GP7
- (20) PRG2\_PRU0\_GP8
- (20) PRG2\_PRU0\_GP9
- (20) PRG2\_PRU0\_GP10
- (20) PRG2\_PRU0\_GP11
- (20) PRG2\_PRU0\_GP16
- (20) PRG2\_PRU1\_GP0
- (20) PRG2\_PRU1\_GP1
- (20) PRG2\_PRU1\_GP2
- (20) PRG2\_PRU1\_GP3
- (20) PRG2\_PRU1\_GP4
- (20) PRG2\_PRU1\_GP5
- (20) PRG2\_PRU1\_GP6
- (20) PRG2\_PRU1\_GP7
- (20) PRG2\_PRU1\_GP8
- (20) PRG2\_PRU1\_GP9
- (20) PRG2\_PRU1\_GP10
- (20) PRG2\_PRU1\_GP11
- (20) PRG2\_PRU1\_GP16
- (39) JTAG\_EMU0\_RSTn

# JTAG 20 PIN cTI CONNECTOR



# JTAG CLOCK BUFFER

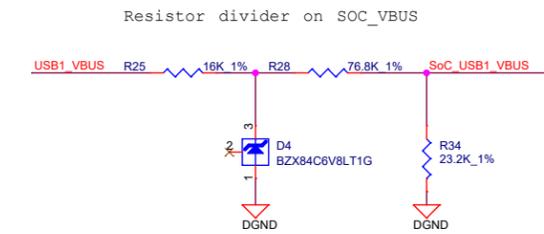
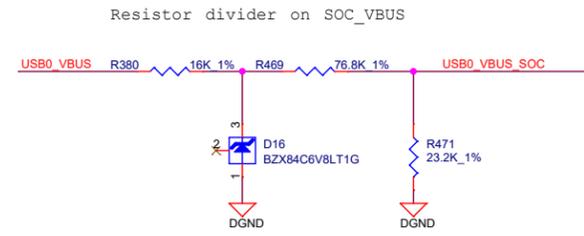
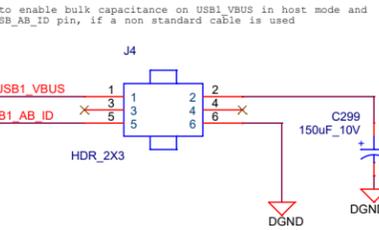
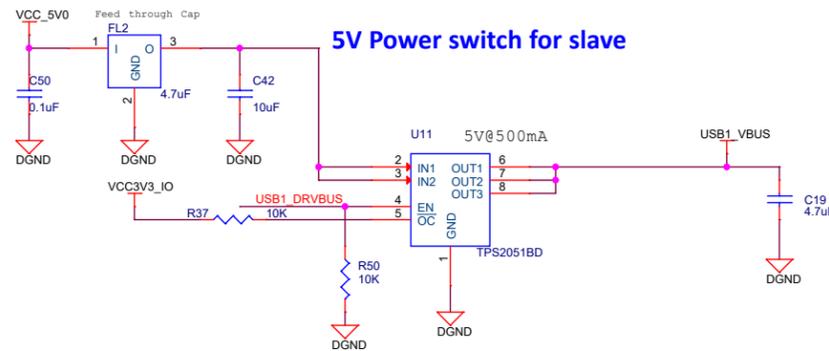
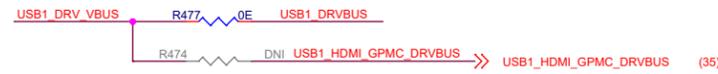
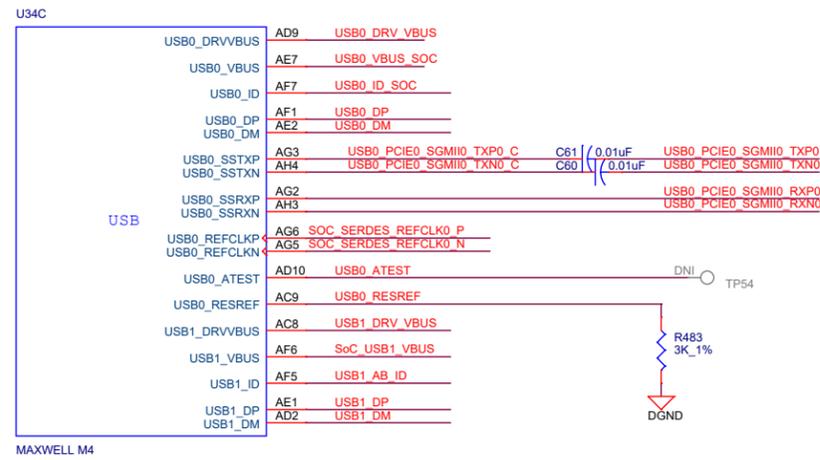


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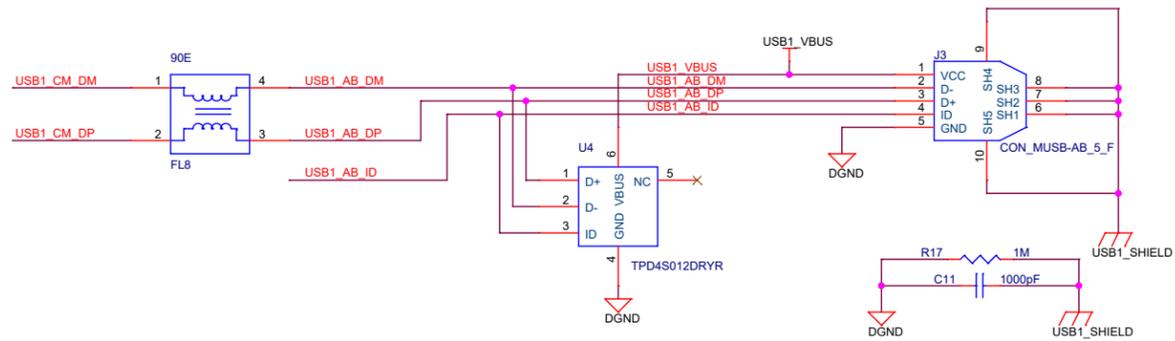


Title: MIPI 60 PIN CONNECTOR		
Size: C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev: E3
Date: Friday, August 31, 2018	Sheet: 28 of 44	

# USB 2.0 INTERFACE



## Micro USB 2.0 AB Connector



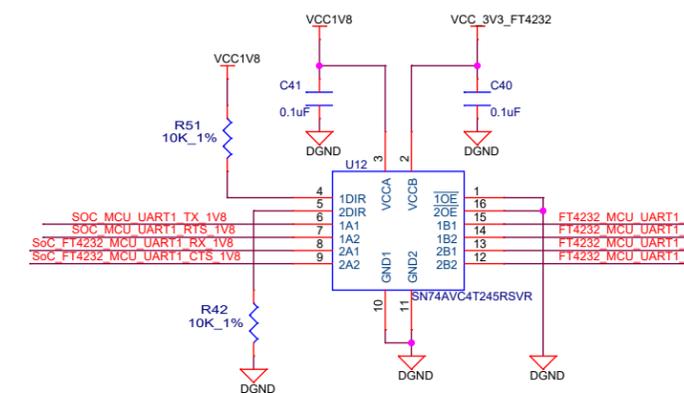
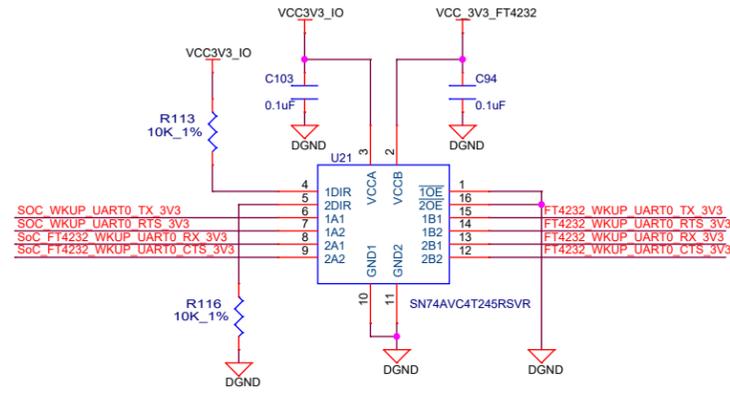
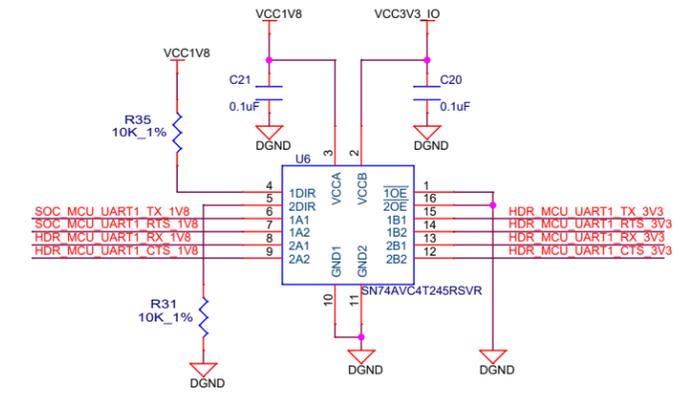
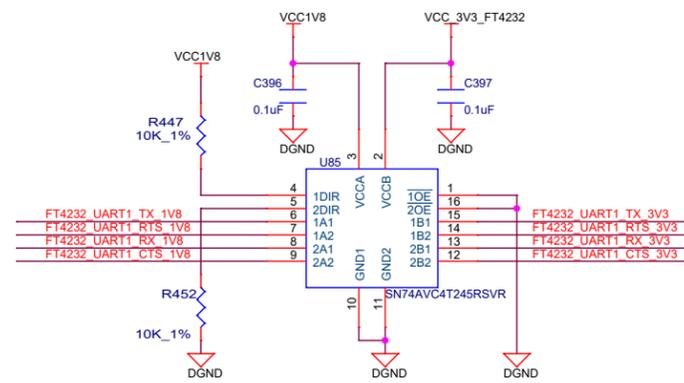
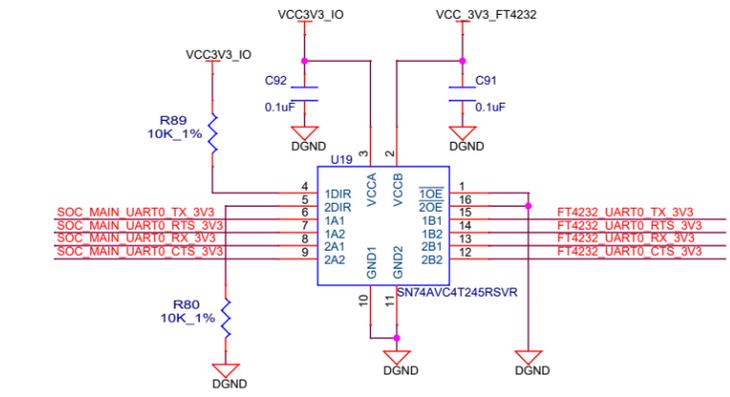
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Title: USB 2.0 INTERFACE

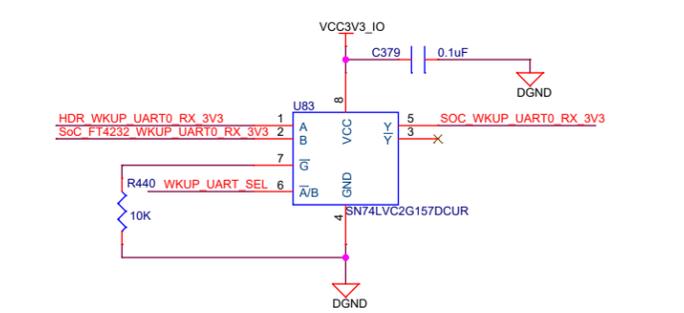
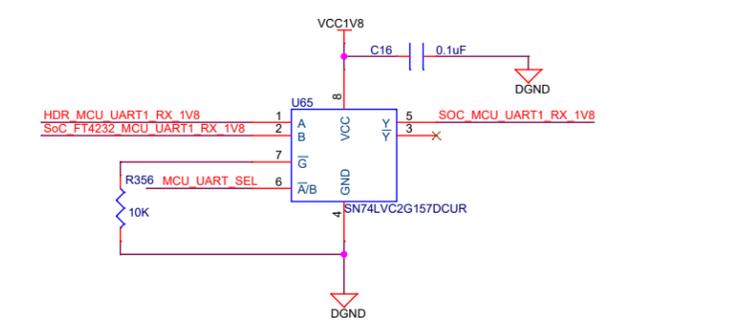
Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 29 of 44

## FT4232 LEVEL TRANSLATOR

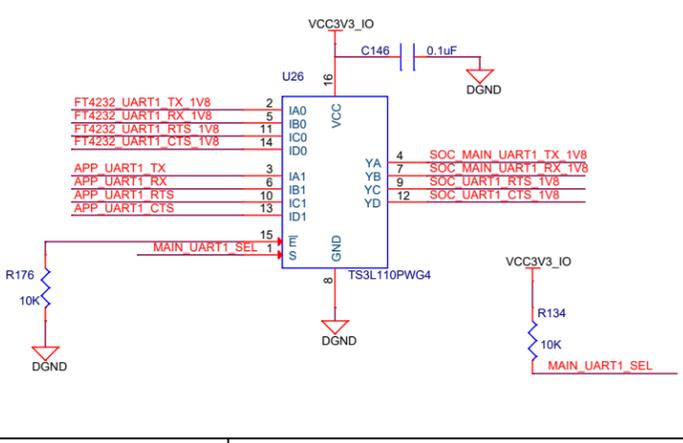
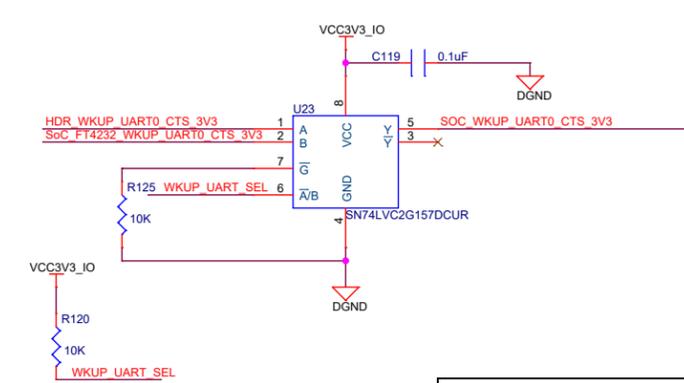
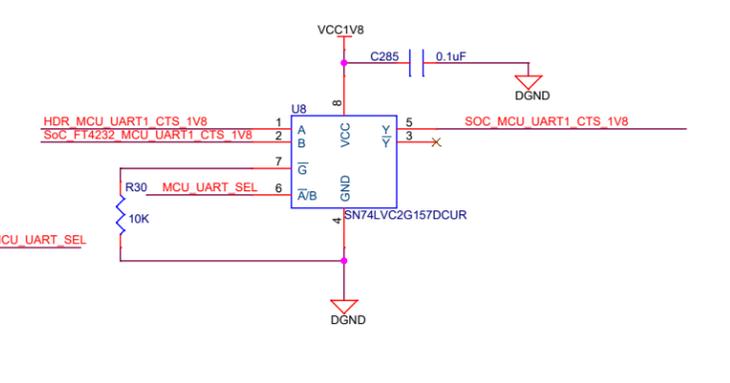


MCU_UART_SEL	<<	MCU_UART_SEL	(37)
WKUP_UART_SEL	<<	WKUP_UART_SEL	(37)
MAIN_UART1_SEL	<<	MAIN_UART1_SEL	(37)
SOC_MAIN_UART0_RX_3V3	<<	SOC_MAIN_UART0_RX_3V3	(33)
SOC_MAIN_UART0_TX_3V3	<<	SOC_MAIN_UART0_TX_3V3	(33)
SOC_MAIN_UART0_RTS_3V3	<<	SOC_MAIN_UART0_RTS_3V3	(33)
SOC_MAIN_UART0_CTS_3V3	<<	SOC_MAIN_UART0_CTS_3V3	(33)
SOC_WKUP_UART0_RX_3V3	<<	SOC_WKUP_UART0_RX_3V3	(33)
SOC_WKUP_UART0_TX_3V3	<<	SOC_WKUP_UART0_TX_3V3	(33,38)
SOC_WKUP_UART0_RTS_3V3	<<	SOC_WKUP_UART0_RTS_3V3	(33,38)
SOC_WKUP_UART0_CTS_3V3	<<	SOC_WKUP_UART0_CTS_3V3	(33)
SOC_MCU_UART1_RX_1V8	<<	SOC_MCU_UART1_RX_1V8	(18)
SOC_MCU_UART1_TX_1V8	<<	SOC_MCU_UART1_TX_1V8	(18)
SOC_MCU_UART1_RTS_1V8	<<	SOC_MCU_UART1_RTS_1V8	(18)
SOC_MCU_UART1_CTS_1V8	<<	SOC_MCU_UART1_CTS_1V8	(18)
SOC_MAIN_UART1_RX_1V8	<<	SOC_MAIN_UART1_RX_1V8	(32)
SOC_MAIN_UART1_TX_1V8	<<	SOC_MAIN_UART1_TX_1V8	(32)
SOC_UART1_RTS_1V8	<<	SOC_UART1_RTS_1V8	(32)
SOC_UART1_CTS_1V8	<<	SOC_UART1_CTS_1V8	(32)
APP_UART1_CTS	<<	APP_UART1_CTS	(32)
APP_UART1_RTS	<<	APP_UART1_RTS	(32)
APP_UART1_RX	<<	APP_UART1_RX	(32)
APP_UART1_TX	<<	APP_UART1_TX	(32)
HDR_MCU_UART1_RTS_3V3	<<	HDR_MCU_UART1_RTS_3V3	(38)
HDR_MCU_UART1_CTS_3V3	<<	HDR_MCU_UART1_CTS_3V3	(38)
HDR_MCU_UART1_TX_3V3	<<	HDR_MCU_UART1_TX_3V3	(38)
HDR_MCU_UART1_RX_3V3	<<	HDR_MCU_UART1_RX_3V3	(38)
HDR_WKUP_UART0_RX_3V3	<<	HDR_WKUP_UART0_RX_3V3	(38)
HDR_WKUP_UART0_CTS_3V3	<<	HDR_WKUP_UART0_CTS_3V3	(38)

## 2:1 MUX



FT4232_UART0_TX_3V3	<<	FT4232_UART0_TX_3V3	(31)
FT4232_UART0_RTS_3V3	<<	FT4232_UART0_RTS_3V3	(31)
FT4232_UART0_RX_3V3	<<	FT4232_UART0_RX_3V3	(31)
FT4232_UART0_CTS_3V3	<<	FT4232_UART0_CTS_3V3	(31)
FT4232_UART1_TX_3V3	<<	FT4232_UART1_TX_3V3	(31)
FT4232_UART1_RTS_3V3	<<	FT4232_UART1_RTS_3V3	(31)
FT4232_UART1_RX_3V3	<<	FT4232_UART1_RX_3V3	(31)
FT4232_UART1_CTS_3V3	<<	FT4232_UART1_CTS_3V3	(31)
FT4232_WKUP_UART0_TX_3V3	<<	FT4232_WKUP_UART0_TX_3V3	(31)
FT4232_WKUP_UART0_RTS_3V3	<<	FT4232_WKUP_UART0_RTS_3V3	(31)
FT4232_WKUP_UART0_RX_3V3	<<	FT4232_WKUP_UART0_RX_3V3	(31)
FT4232_WKUP_UART0_CTS_3V3	<<	FT4232_WKUP_UART0_CTS_3V3	(31)
FT4232_MCU_UART1_TX_3V3	<<	FT4232_MCU_UART1_TX_3V3	(31)
FT4232_MCU_UART1_RTS_3V3	<<	FT4232_MCU_UART1_RTS_3V3	(31)
FT4232_MCU_UART1_RX_3V3	<<	FT4232_MCU_UART1_RX_3V3	(31)
FT4232_MCU_UART1_CTS_3V3	<<	FT4232_MCU_UART1_CTS_3V3	(31)



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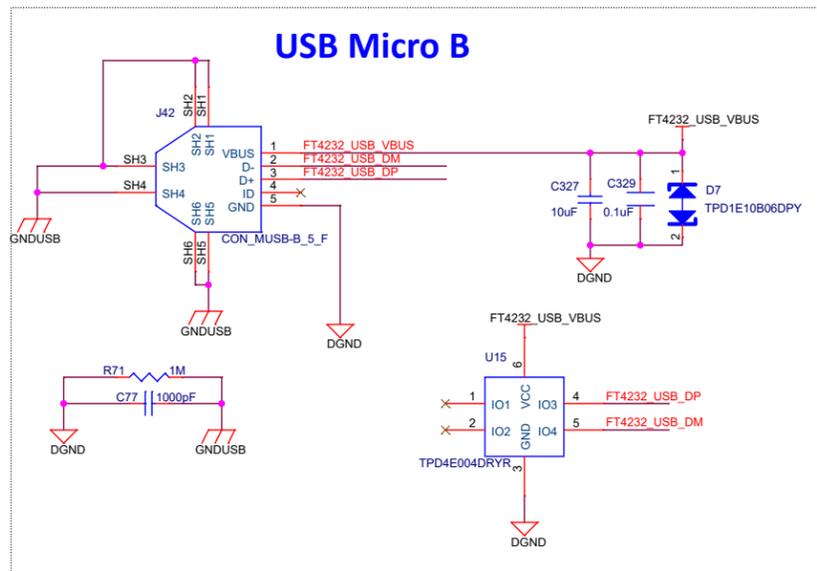


Title FT4232 LEVEL TRANSLATOR

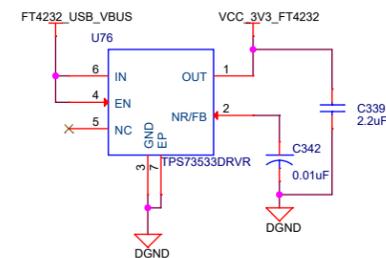
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E3
Date:	Tuesday, September 04, 2018	Sheet	30 of 44

# FT4232 UART

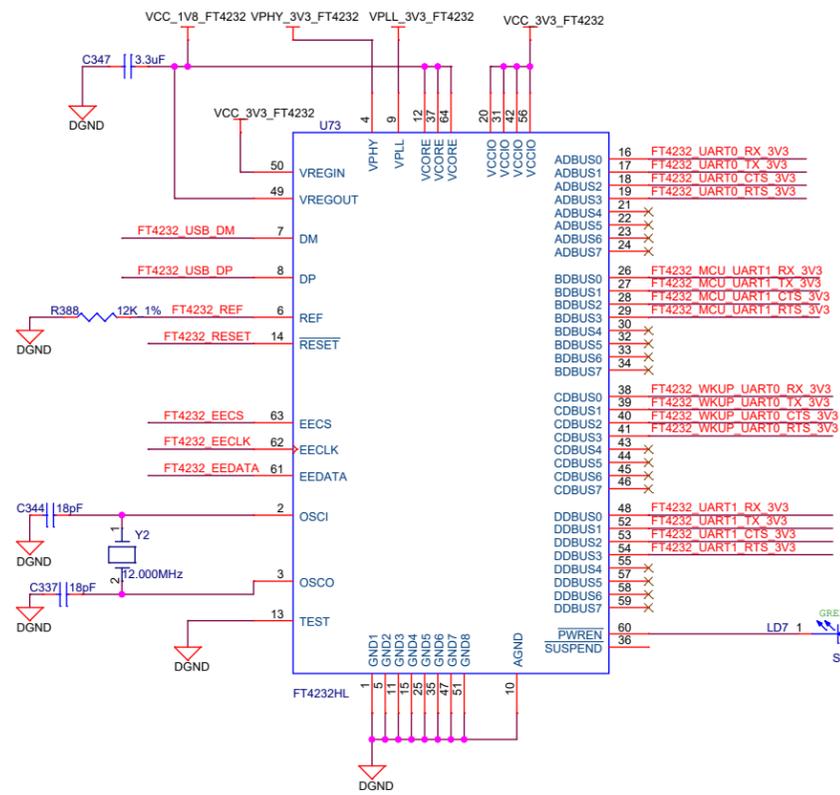
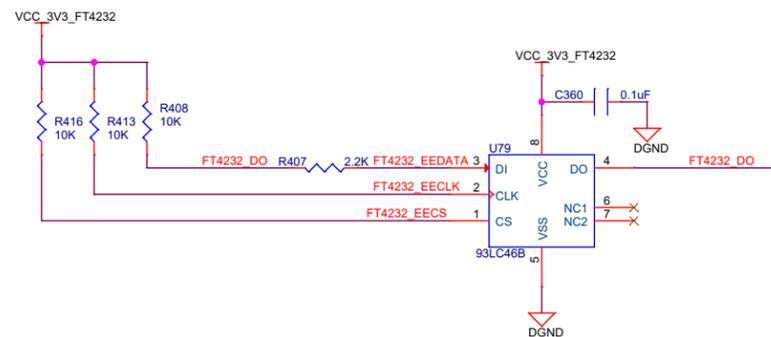
## USB Micro B



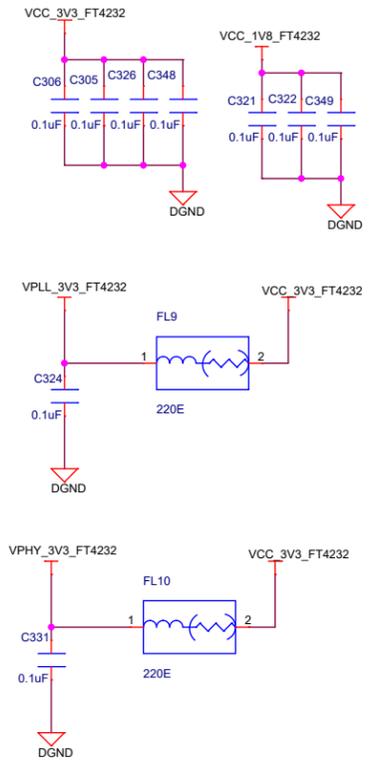
## FT4232: 5V to 3.3V@500mA LDO



## EEPROM



FT4232 UART0 TX_3V3	<<FT4232_UART0_TX_3V3	(30)
FT4232 UART0 RTS_3V3	<<FT4232_UART0_RTS_3V3	(30)
FT4232 UART0 RX_3V3	<<FT4232_UART0_RX_3V3	(30)
FT4232 UART0 CTS_3V3	<<FT4232_UART0_CTS_3V3	(30)
FT4232 UART1 TX_3V3	<<FT4232_UART1_TX_3V3	(30)
FT4232 UART1 RTS_3V3	<<FT4232_UART1_RTS_3V3	(30)
FT4232 UART1 RX_3V3	<<FT4232_UART1_RX_3V3	(30)
FT4232 UART1 CTS_3V3	<<FT4232_UART1_CTS_3V3	(30)
FT4232 WKUP UART0 TX_3V3	<<FT4232_WKUP_UART0_TX_3V3	(30)
FT4232 WKUP UART0 RTS_3V3	<<FT4232_WKUP_UART0_RTS_3V3	(30)
FT4232 WKUP UART0 RX_3V3	<<FT4232_WKUP_UART0_RX_3V3	(30)
FT4232 WKUP UART0 CTS_3V3	<<FT4232_WKUP_UART0_CTS_3V3	(30)
FT4232 MCU UART1 TX_3V3	<<FT4232_MCU_UART1_TX_3V3	(30)
FT4232 MCU UART1 RTS_3V3	<<FT4232_MCU_UART1_RTS_3V3	(30)
FT4232 MCU UART1 RX_3V3	<<FT4232_MCU_UART1_RX_3V3	(30)
FT4232 MCU UART1 CTS_3V3	<<FT4232_MCU_UART1_CTS_3V3	(30)

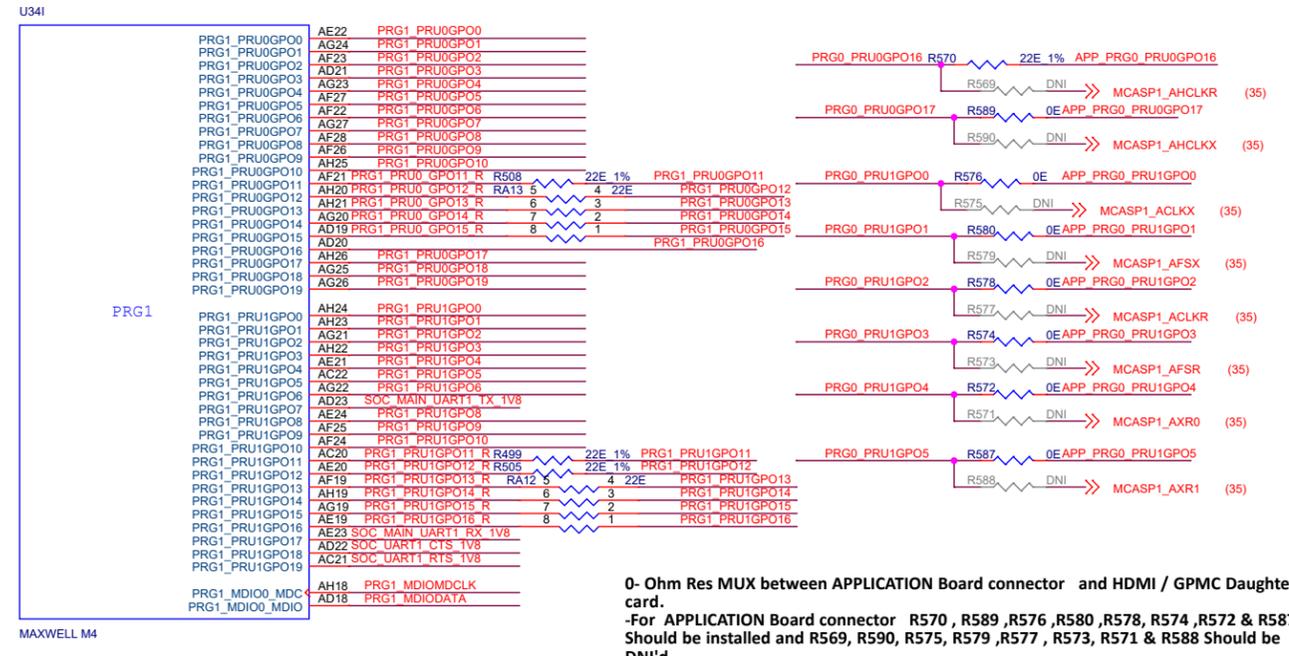
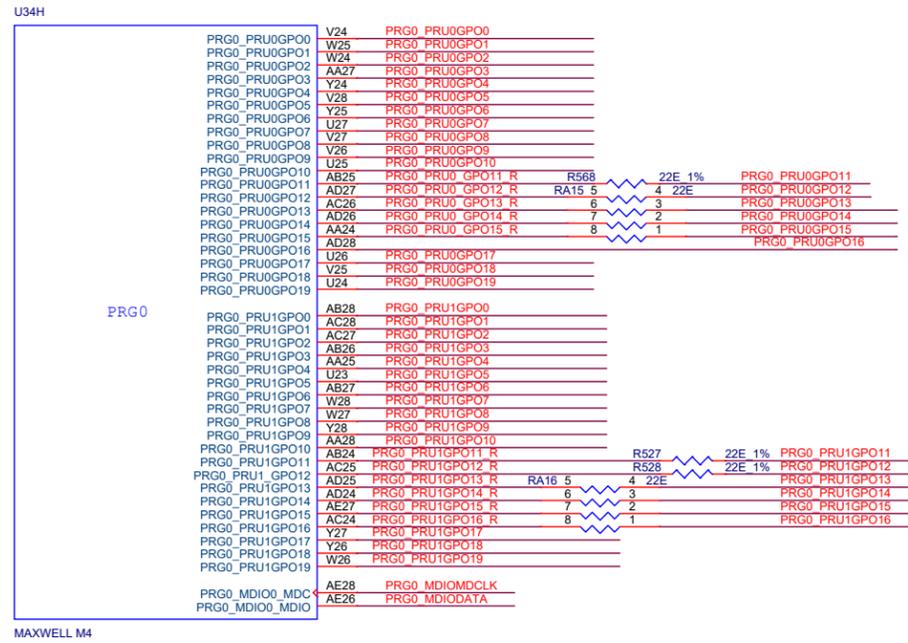


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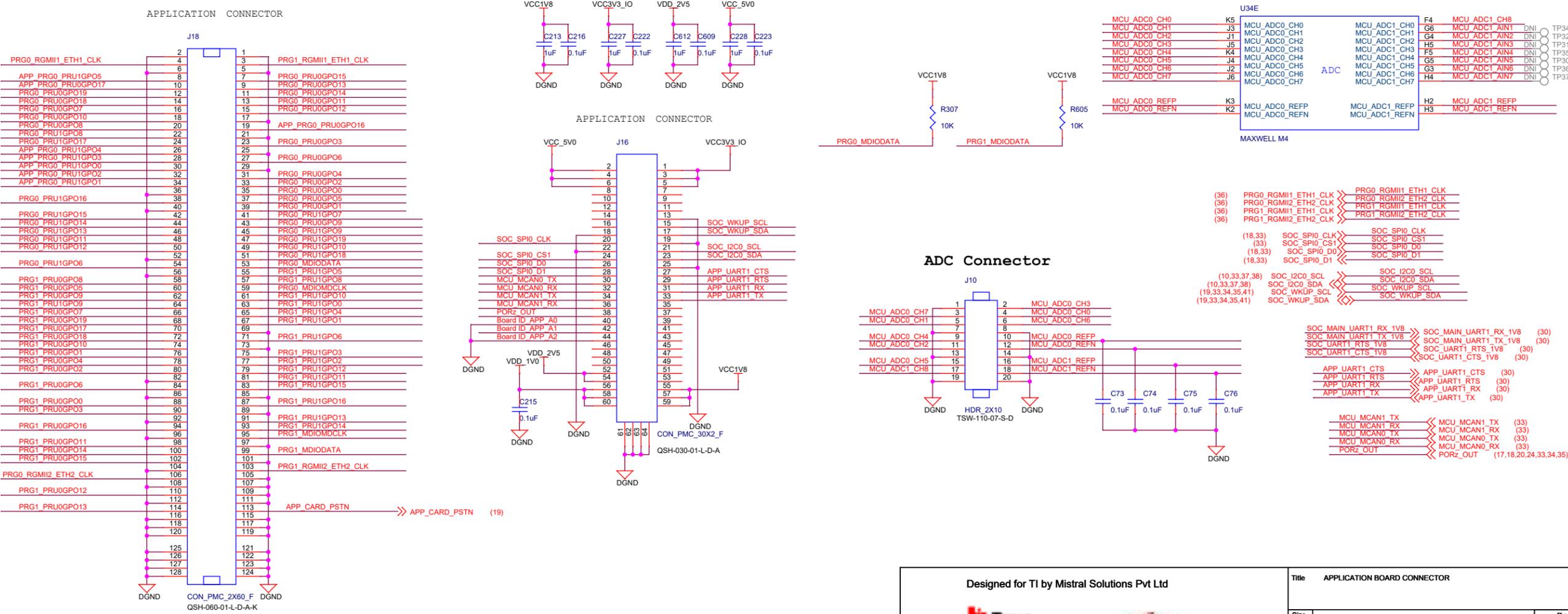
Title		FT4232 UART TO USB BRIDGE	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E3
Date:	Friday, August 31, 2018	Sheet	31 of 44

# APPLICATION BOARD INTERFACE



0- Ohm Res MUX between APPLICATION Board connector and HDMI / GPMC Daughter card.  
 -For APPLICATION Board connector R570, R589, R576, R580, R578, R574, R572 & R587 Should be installed and R569, R590, R575, R579, R577, R573, R571 & R588 Should be DNI'd.  
 -For HDMI / GPMC Daughter card R569, R590, R575, R579, R577, R573, R571 & R588 Should be installed and R570, R589, R576, R580, R578, R574, R572 & R587 Should be DNI'd.

## APPLICATION BOARD CONNECTORS

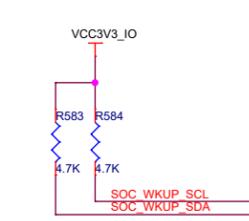
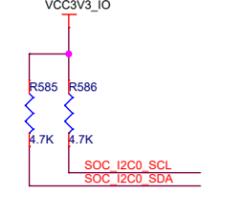
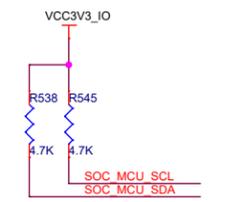
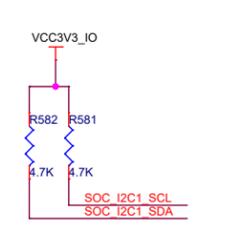
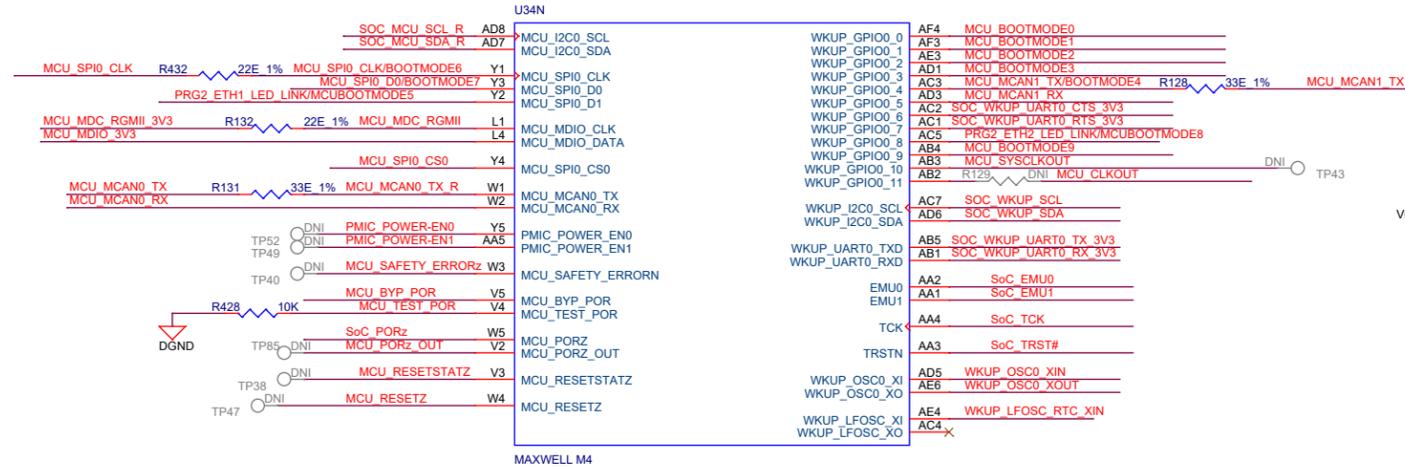
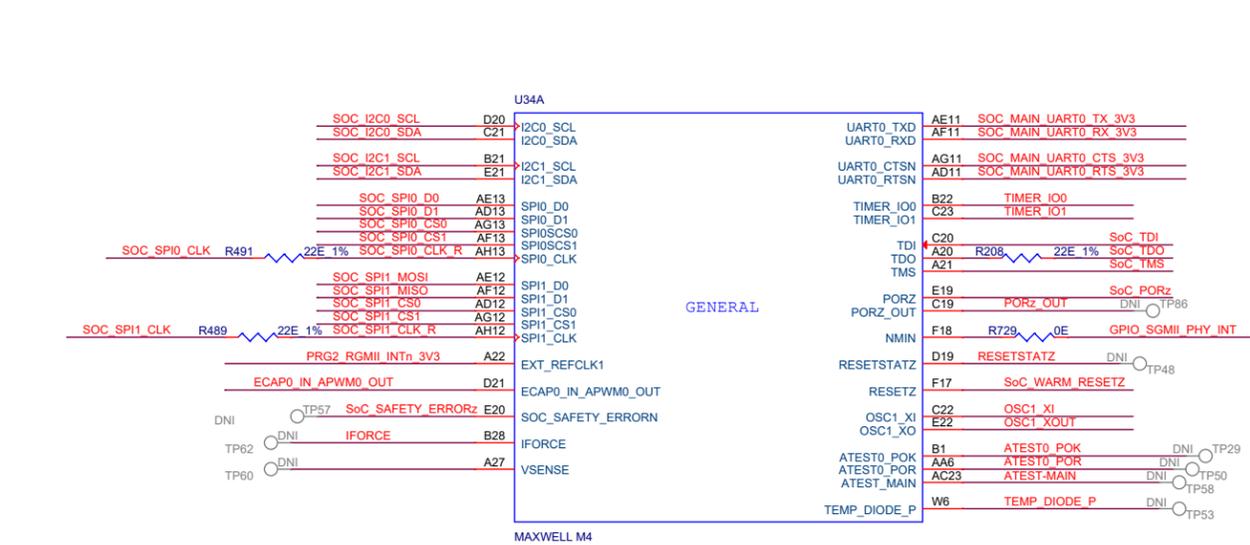


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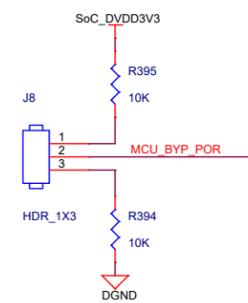
**TEXAS INSTRUMENTS** **MISTRAL**

Title: APPLICATION BOARD CONNECTOR		Rev: E3
Size: C	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev: E3
Date: Tuesday, September 04, 2018	Sheet: 32 of 44	

# GENERAL & MCU\_GENERAL

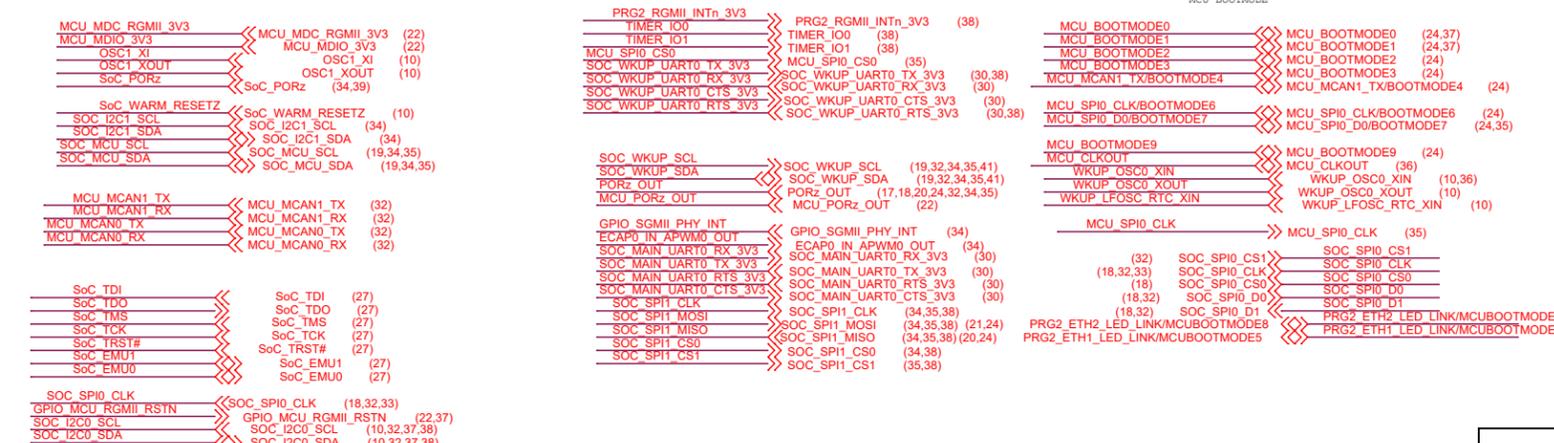
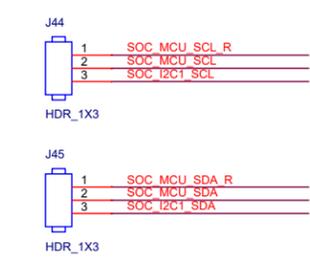


## Jumper to select Internal PORz & External PORz

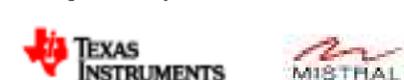


To Disable the Internal PORz, Connect the Jumper between Pin no 1 & 2 of J8.  
To Enable the Internal PORz, Connect the Jumper between Pin no 2 & 3 of J8

## Jumper option to connect the peripherals connected on MCU\_I2C to SoC I2C1

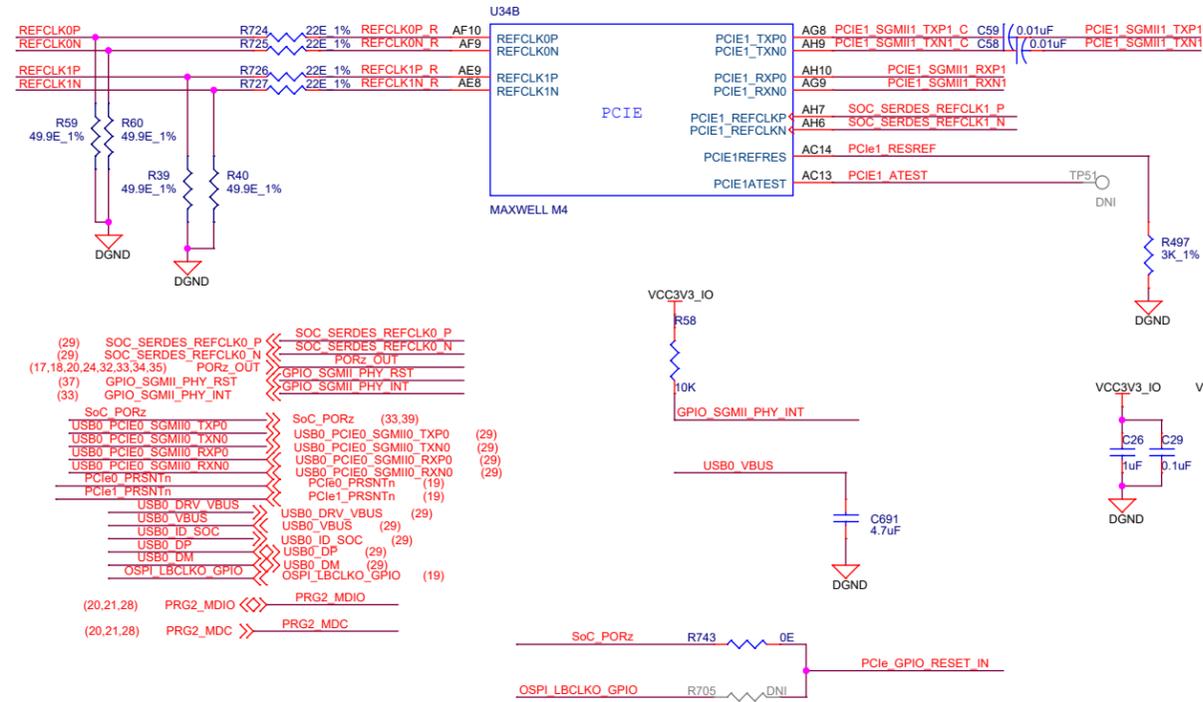


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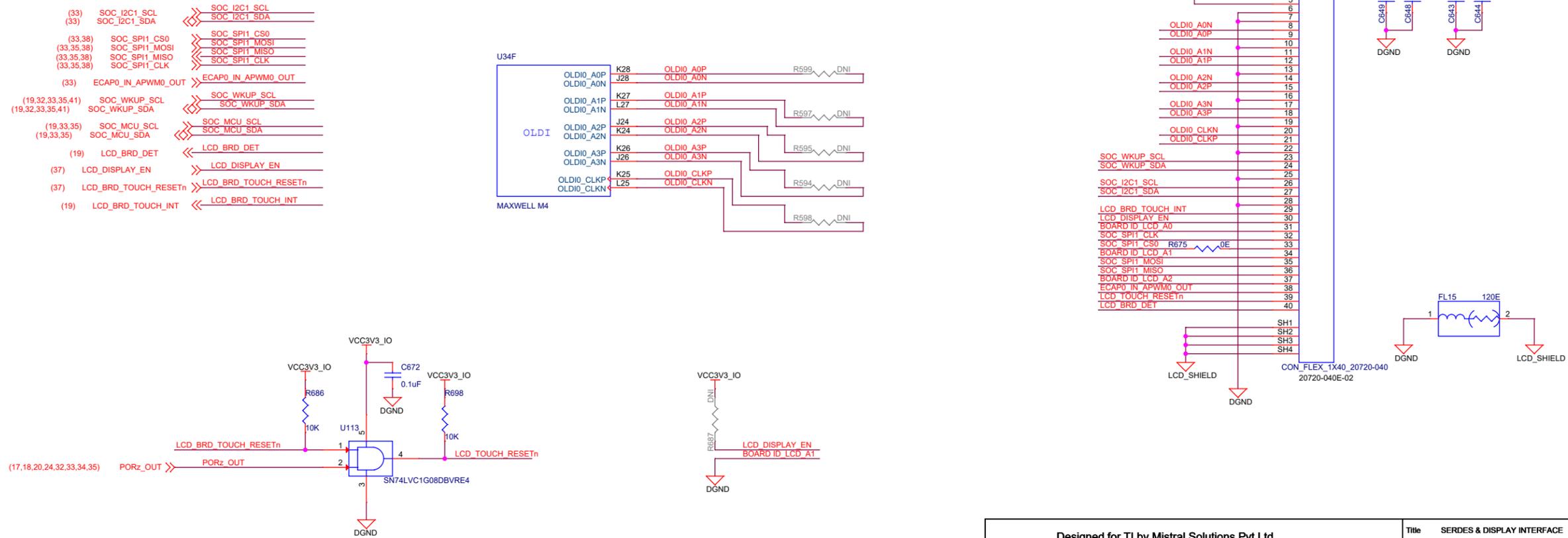


Title		SOC_GENERAL & MCU GENERAL	
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev	E3
Date:	Tuesday, September 04, 2018	Sheet	33 of 44

# SERDES INTERFACE



# OLDI INTERFACE



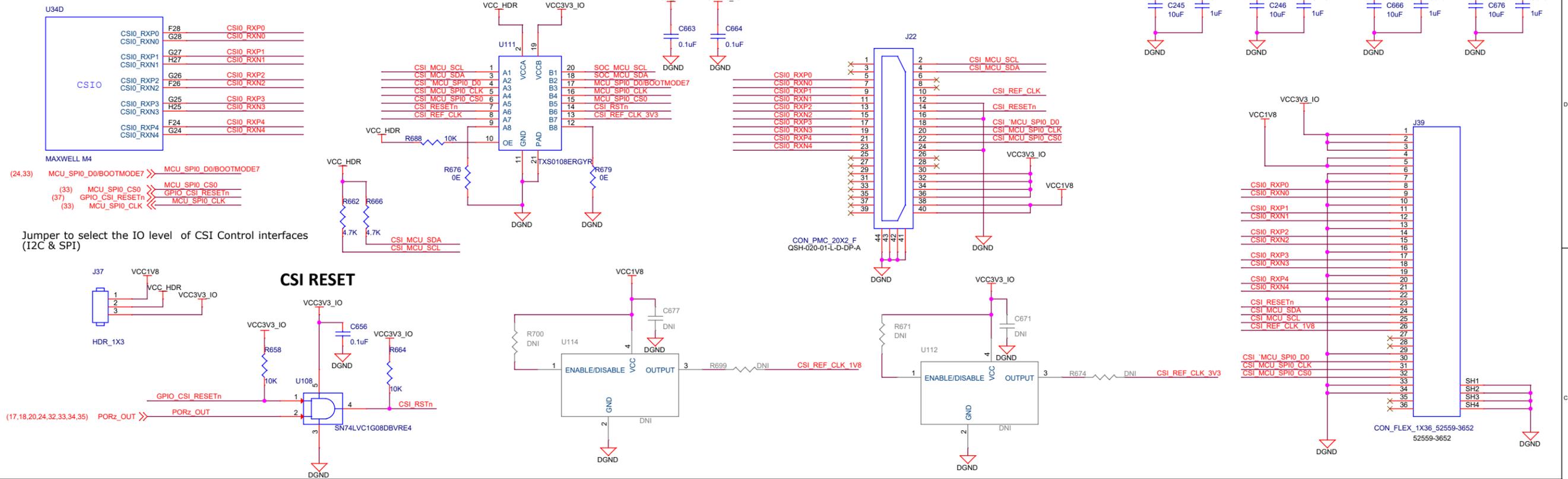
Designed for TI by Mistral Solutions Pvt Ltd



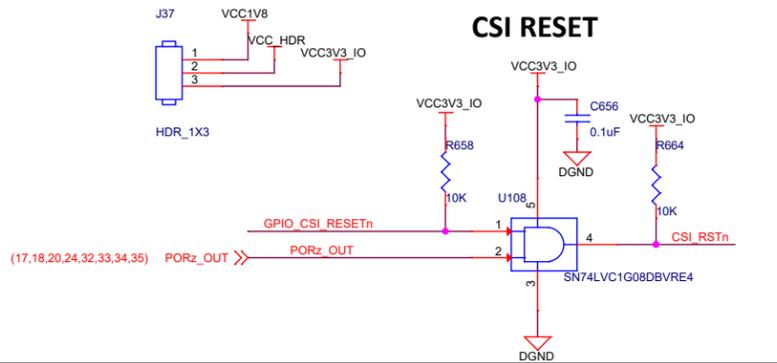
Title SERDES & DISPLAY INTERFACE

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, September 04, 2018	Sheet 34 of 44

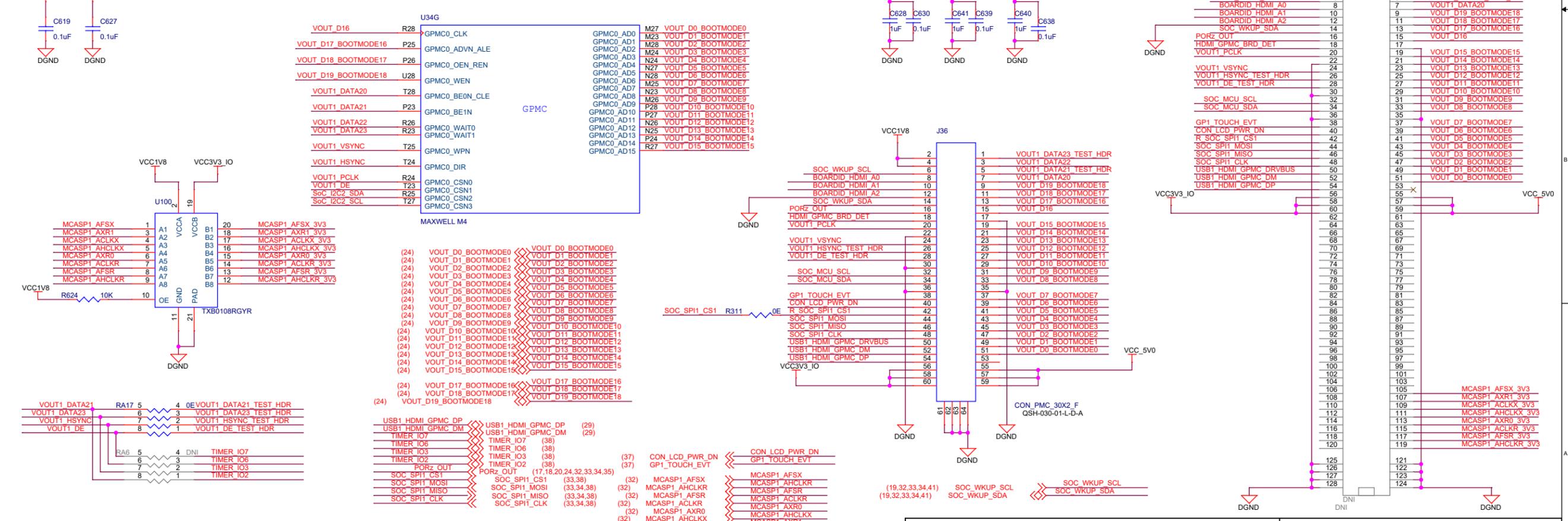
# CSI INTERFACE



## CSI RESET



# DSS/GPMC Interface



0- Ohm Res MUX between HDMI / GPMC and Test Header Timer signals.  
 -For HDMI / GPMC , RA17 Should be installed and RA6 Should be DNI'd.  
 -For test header Timer signals, RA6 Should be installed and RA17 Should be DNI'd.

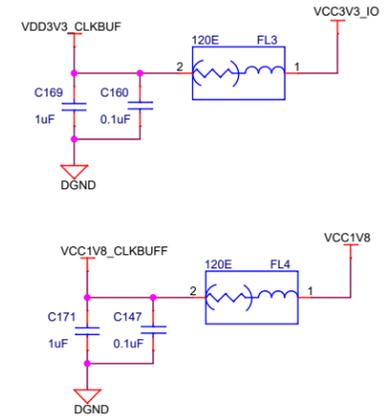
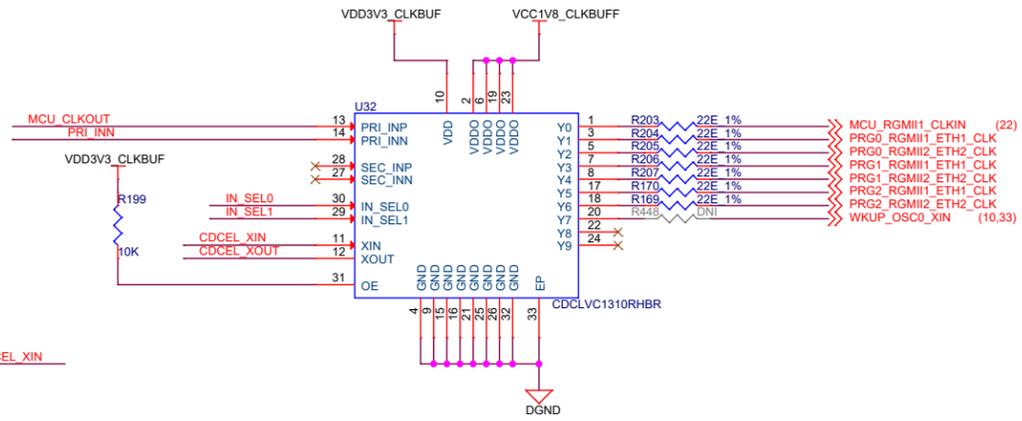
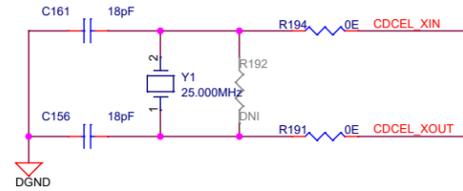
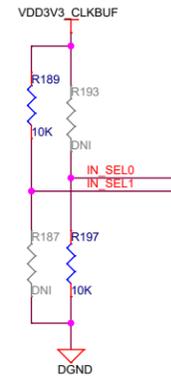
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**TEXAS INSTRUMENTS** **MISTRAL**

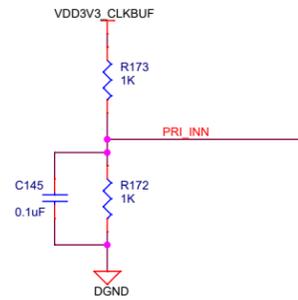
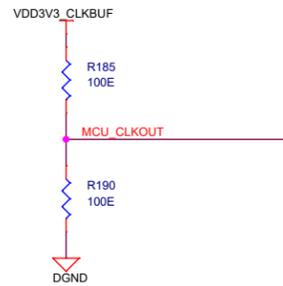
Title		CSI,GPMC/DSS INTERFACE
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E3
Date:	Tuesday, September 04, 2018	Sheet 35 of 44

# ETHERNET PHY CLOCK BUFFER

## REFERENCE INPUT SELECTION



MCU\_CLKOUT → MCU\_CLKOUT (33)

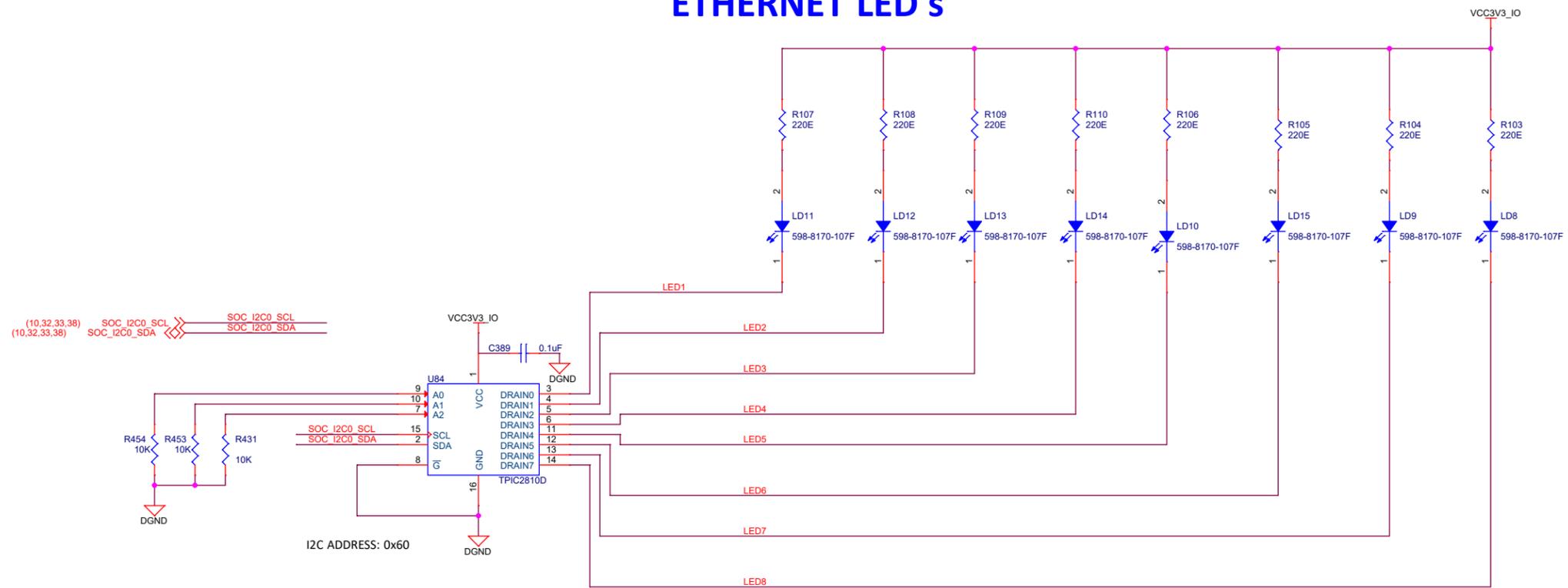


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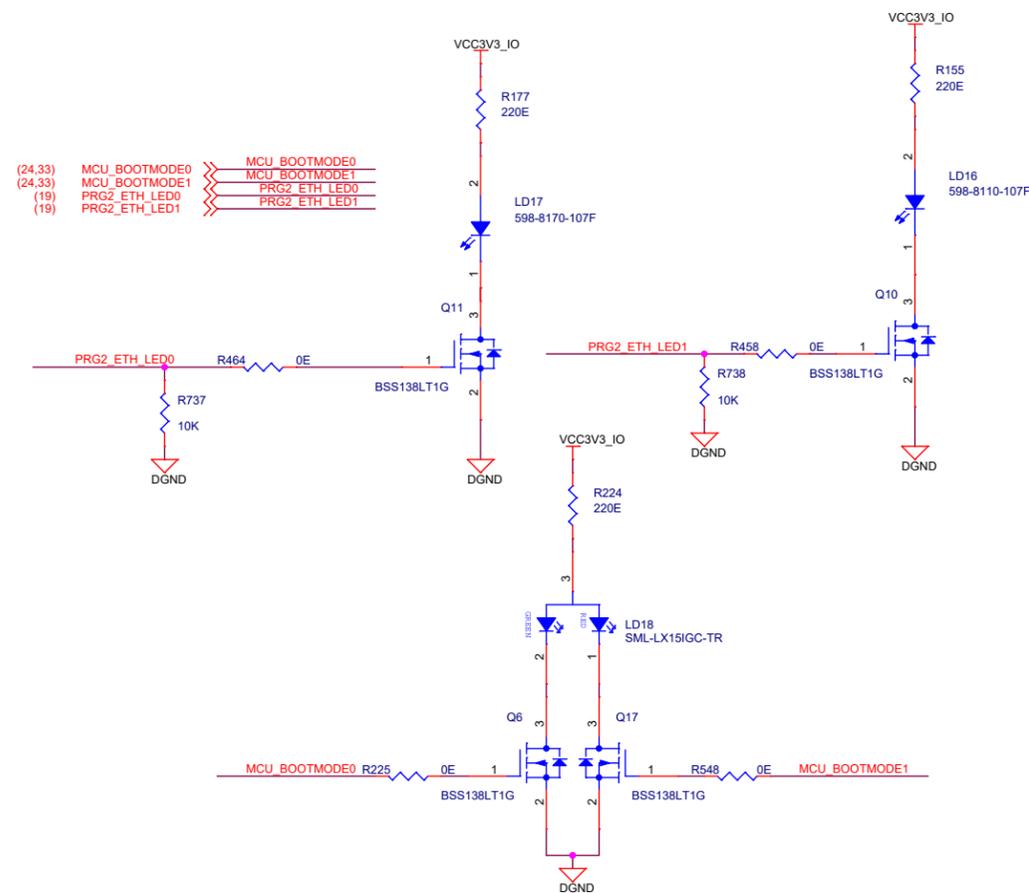


Title		ETHERNET PHY CLOCK GENERATOR	
Size		Rev	
C	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	E3	
Date:	Friday, August 31, 2018	Sheet	36 of 44

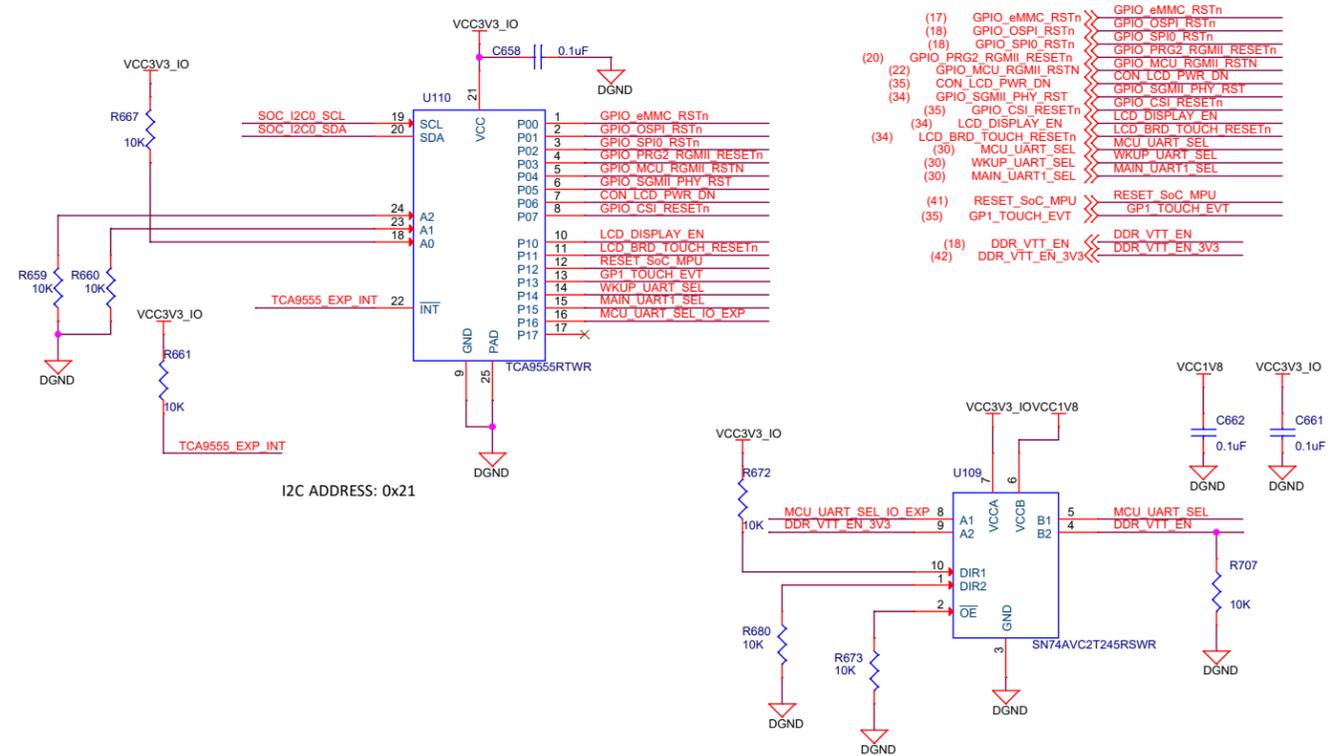
# ETHERNET LED'S



# PRG2 ETHERNET LED'S



# I2C IO Expander

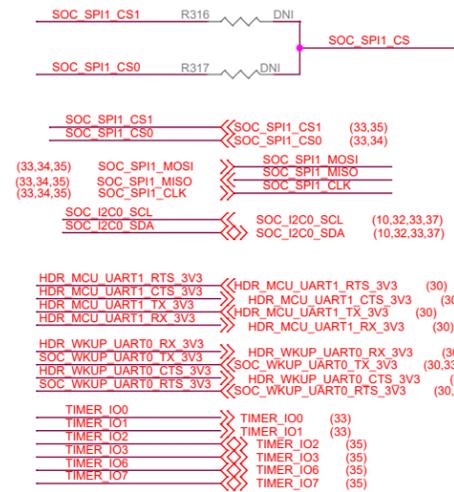


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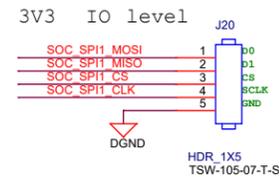


Title		ETHERNET LED'S
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev E3
Date:	Tuesday, July 24, 2018	Sheet 37 of 44

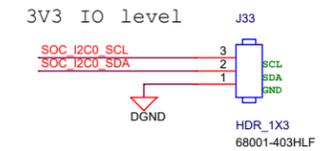
# TEST HEADER



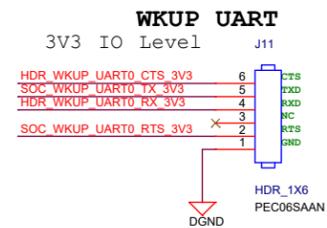
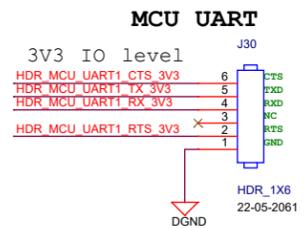
## SPI TEST HEADER



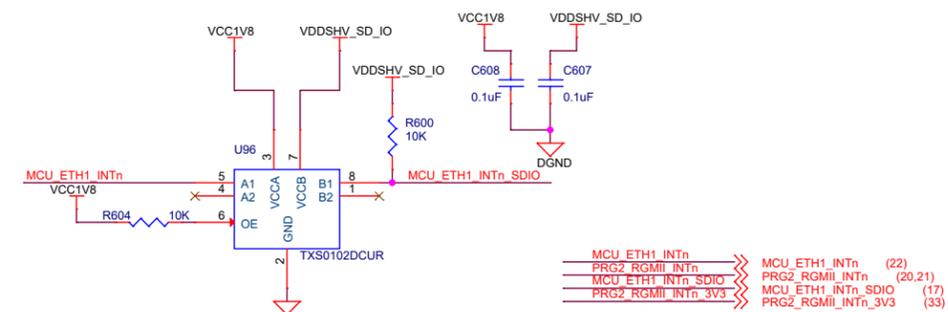
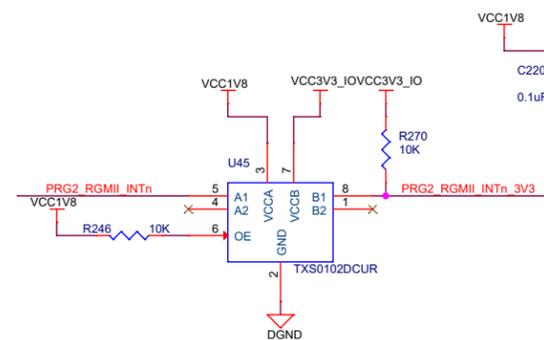
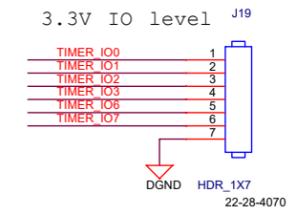
## I2C TEST HEADER



## UART TEST HEADER



## TIMER SIGNALS TEST HEADER



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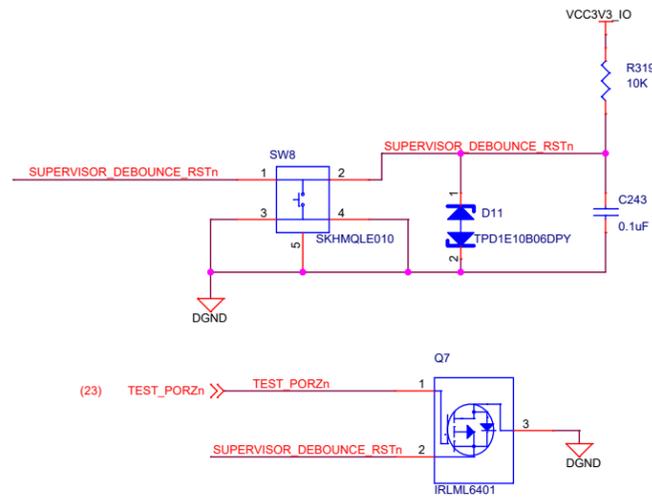


Title TEST HEADER

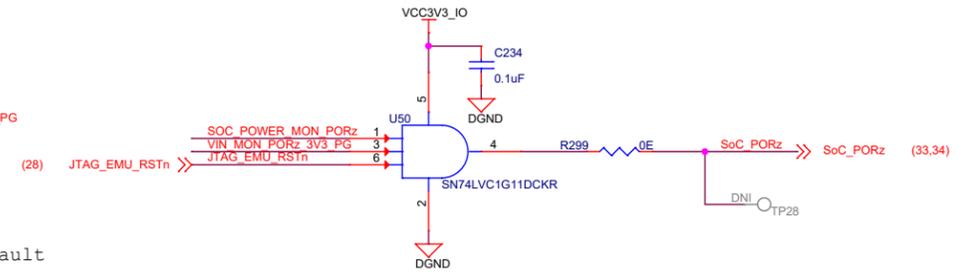
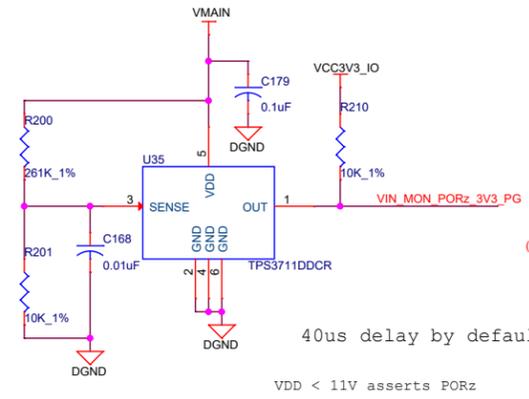
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, July 24, 2018	Sheet 38 of 44

# VOLTAGE SUPERVISOR

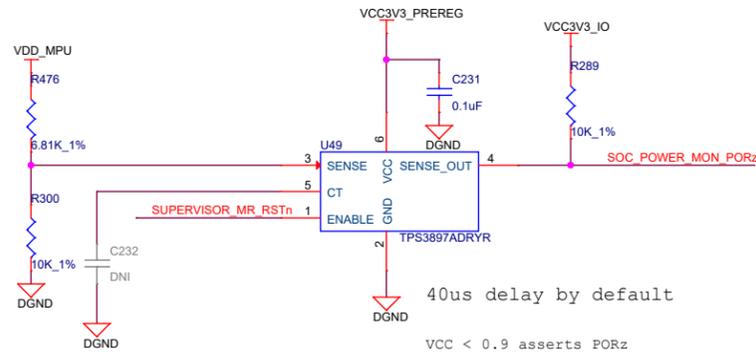
## Under Voltage Monitor (VMAIN)



(23) SUPERVISOR\_DEBOUNCE\_RSTn >> SUPERVISOR\_DEBOUNCE\_RSTn  
 (23) SUPERVISOR\_MR\_RSTn >> SUPERVISOR\_MR\_RSTn  
 (41,42) VIN\_MON\_PORz\_3V3\_PG >> VIN\_MON\_PORz\_3V3\_PG



## Under Voltage Monitor (VDD\_MPU)



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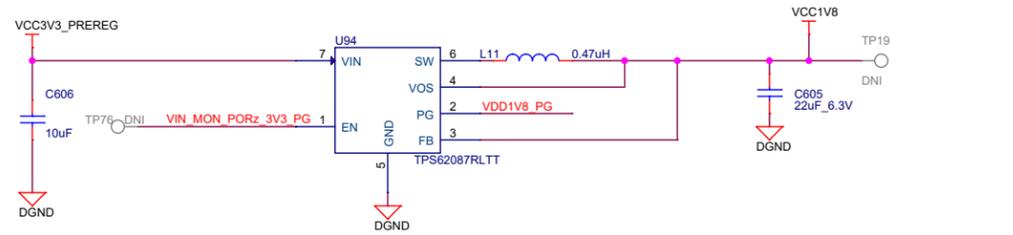
Title VOLTAGE SUPERVISOR & WKUP LEDs

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Friday, August 31, 2018	Sheet 39 of 44

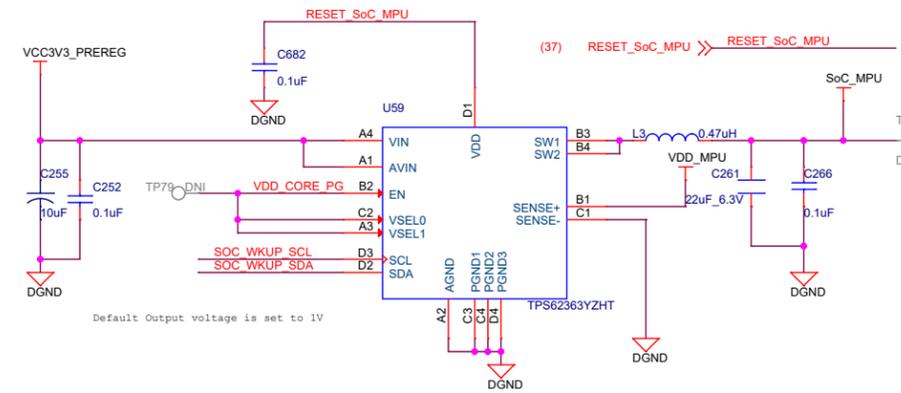


# SoC POWER SUPPLY

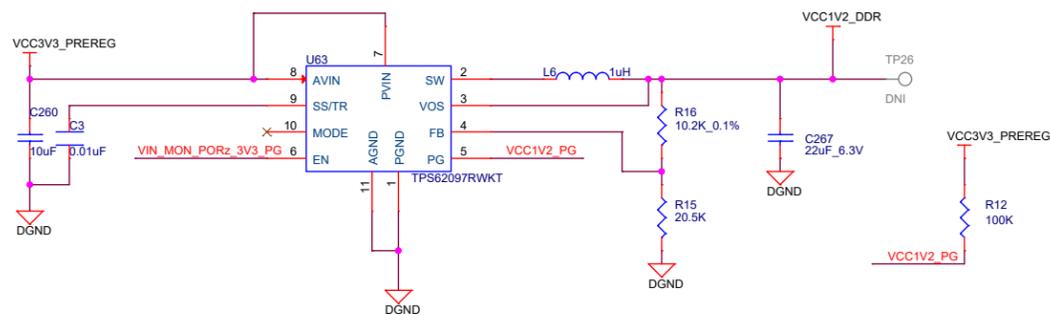
## 1.8V IO, 3.0AMPS SUPPLY



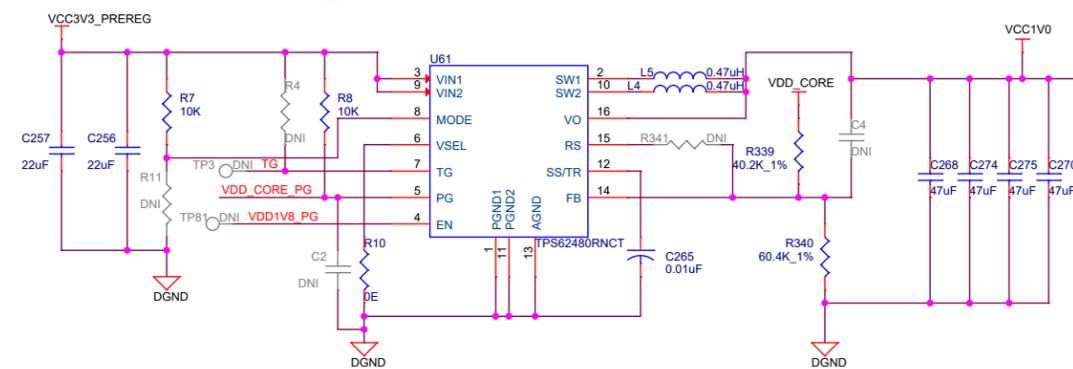
## 0.9-1.35V, 3.0AMPS SUPPLY



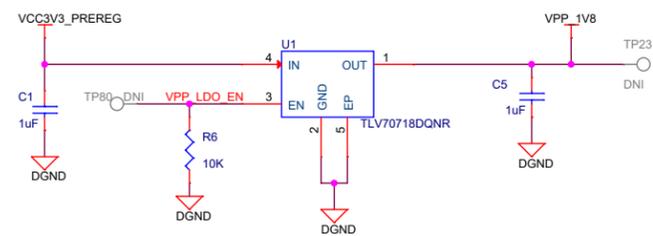
## 1.2V, 2.0AMPS SUPPLY



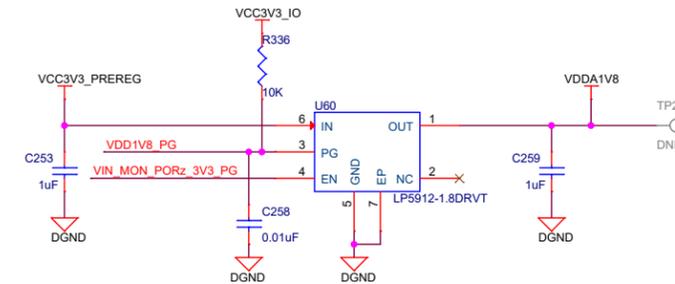
## VDD\_CORE 1.0V, 6.0AMPS SUPPLY



## 1.8V VPP, 0.15AMPS SUPPLY



## 1.8V Analog , 0.4AMPS SUPPLY



(19,32,33,34,35) SOC\_WKUP\_SCL <<> SOC\_WKUP\_SCL  
 (19,32,33,34,35) SOC\_WKUP\_SDA <<> SOC\_WKUP\_SDA  
 (18) VPP\_LDO\_EN <<< VPP\_LDO\_EN  
 (39,42) VIN\_MON\_PORz\_3V3\_PG <<< VIN\_MON\_PORz\_3V3\_PG

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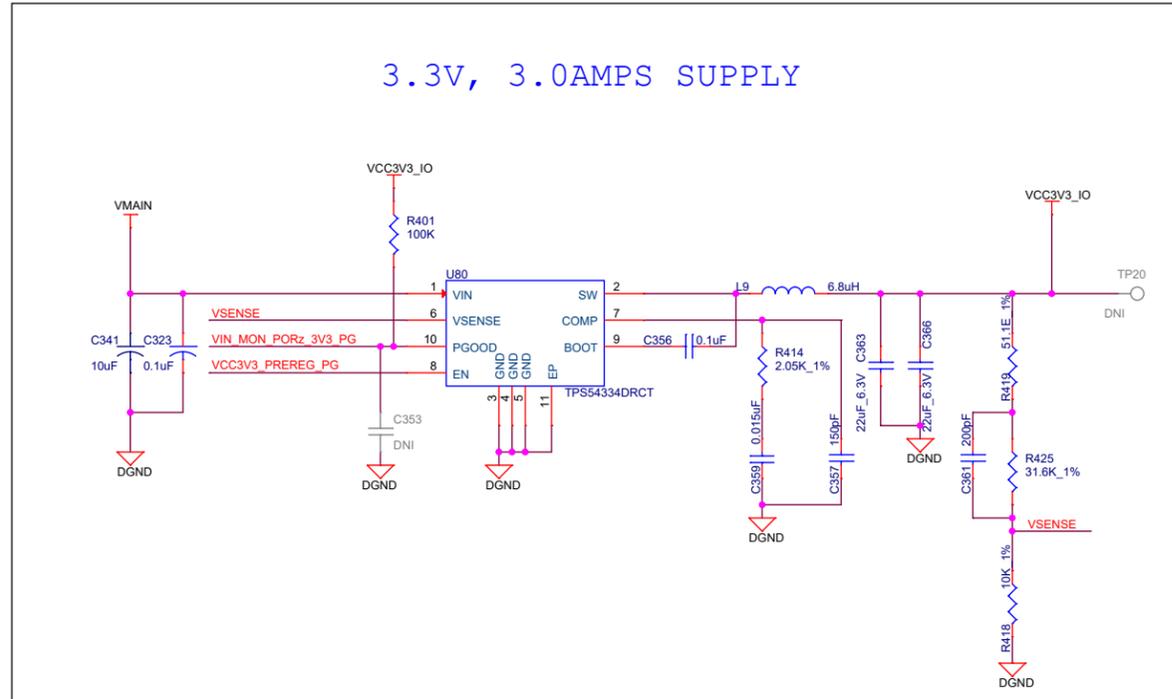


Title SoC POWER SUPPLY

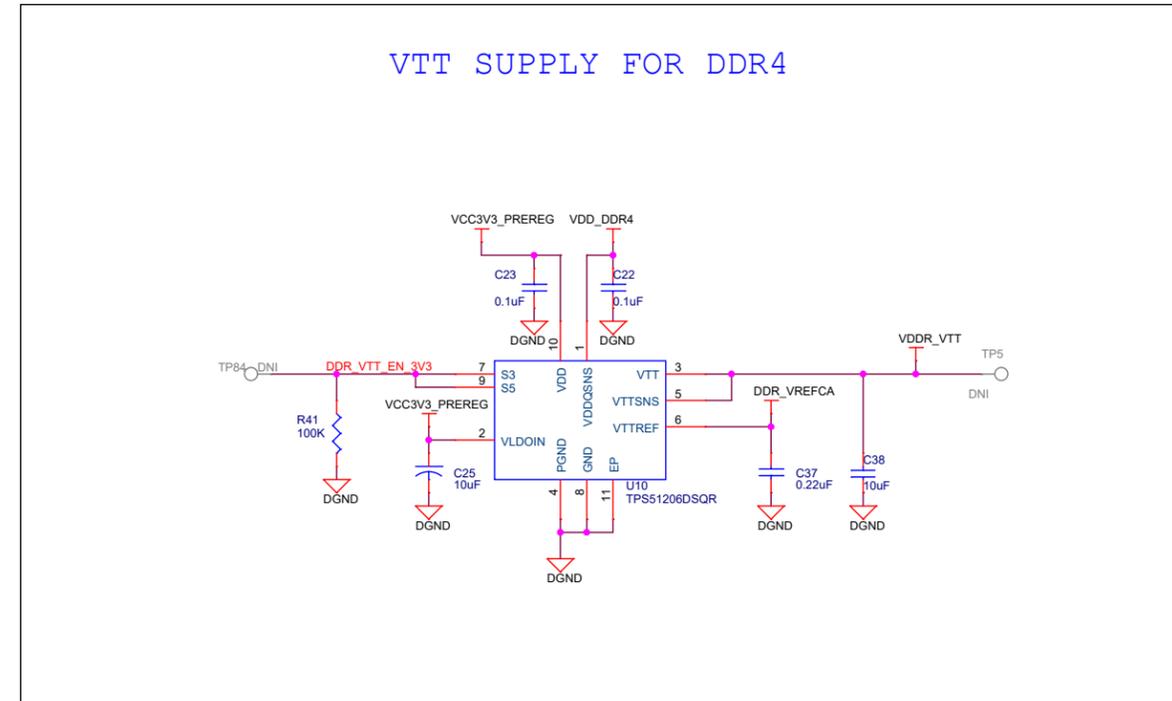
Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, September 04, 2018	Sheet 41 of 44

# PERIPHERAL POWER SUPPLY

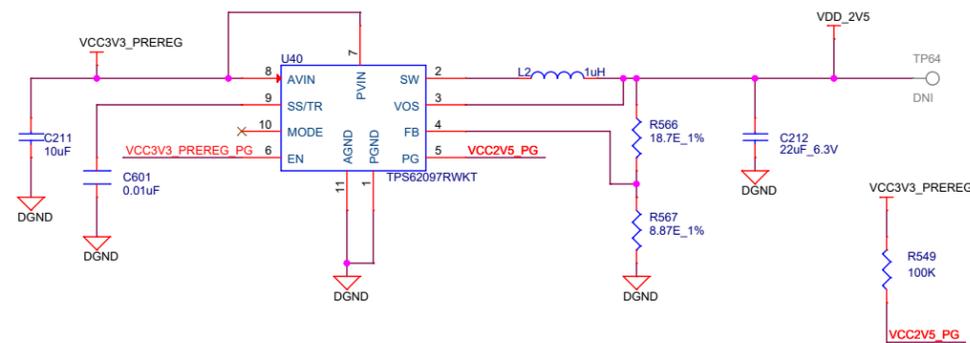
## 3.3V, 3.0AMPS SUPPLY



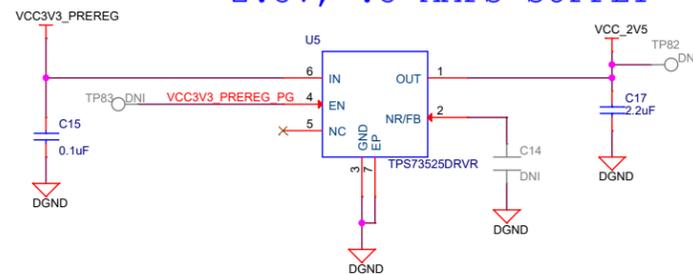
## VTT SUPPLY FOR DDR4



## 2.5V, 2.0AMPS SUPPLY

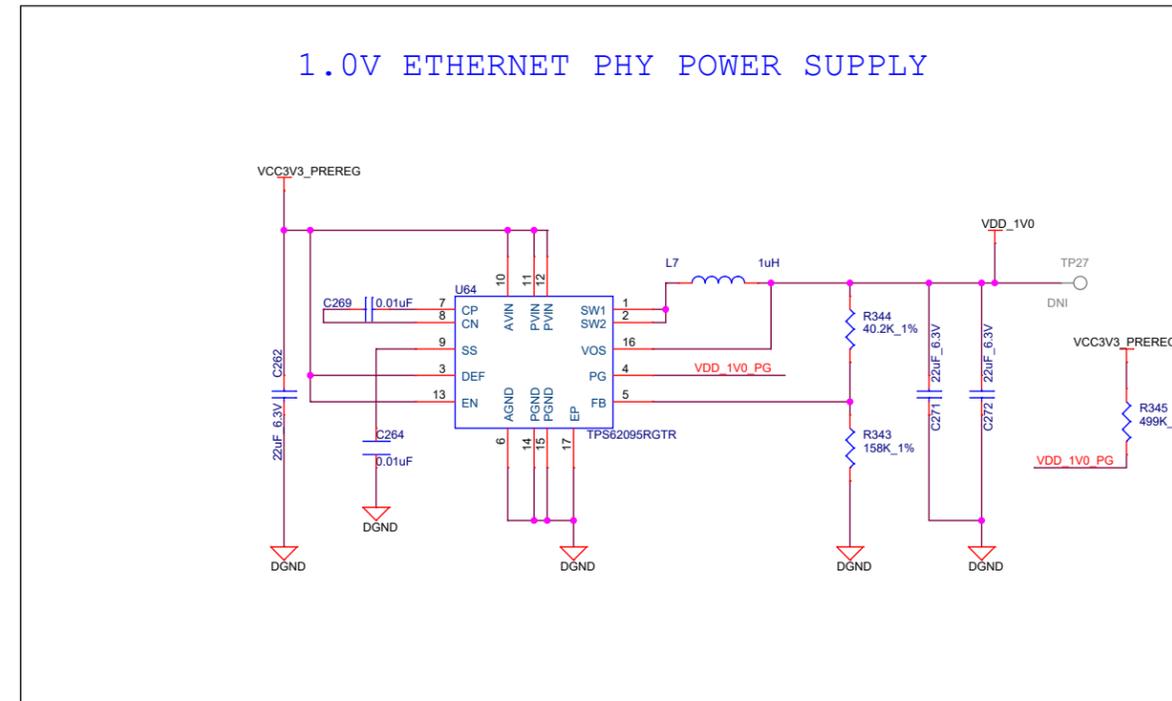


## 2.5V, .5 AMPS SUPPLY



(40) VCC3V3\_PREREG\_PG >> VCC3V3\_PREREG\_PG  
 (39.41) VIN\_MON\_PORz\_3V3\_PG >> VIN\_MON\_PORz\_3V3\_PG  
 (37) DDR\_VTT\_EN\_3V3 >> DDR\_VTT\_EN\_3V3

## 1.0V ETHERNET PHY POWER SUPPLY



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Title PERIPHERAL POWER SUPPLY

Size	Variant Name = PROC082 001 OPN#TMDX654IDKEVM	Rev
C		E3
Date:	Tuesday, September 04, 2018	Sheet 42 of 44

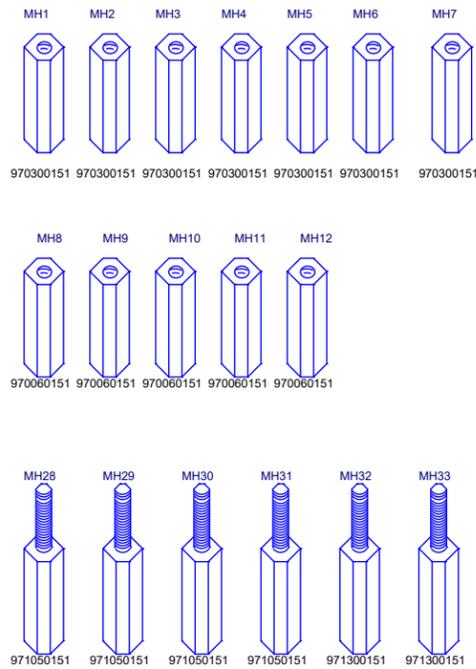


# HARDWARE SCHEMATICS

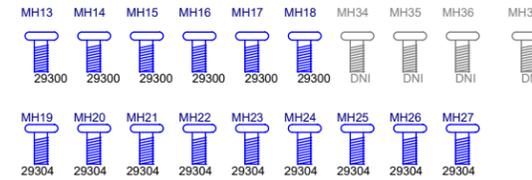
## ASSEMBLY NOTES

- All MSL components should be baked as per JEDEC standard.
- PCB should be baked at 120 degree for 8 hours.
- Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- These assemblies are ESD sensitive, ESD precautions shall be observed.
- These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Provide serial numbers to the assembled boards for identification.
- The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

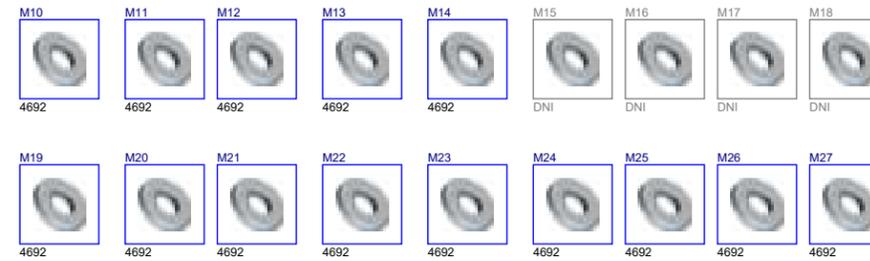
## STANDOFFS



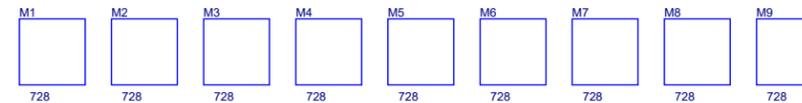
## SCREWS



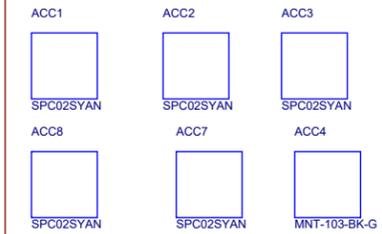
## WASHER'S



## RUBBER FEET



## JUMPERS



## FIDUCIALS



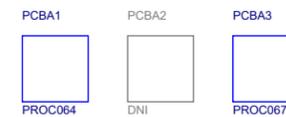
## Socket & Processor as Accessories



## BARE PCB



## Assembled PCB's



## Board Serial No.



## LABELS

## ORDERABLE PART NO



### Orderable part number

Variant	Label Text
001	TMDX654IDKEVM
002	TMDX654HSEVM
003	TMDX654GPEVM
004	TMDX654IDKEVM-S
005	TMDX654GPEVM-S

## LOGOs



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Title: HARDWARE SCHEMATICS

Size	Variant Name = PROC062 001 OPN#TMDX654IDKEVM	Rev
C		E3
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