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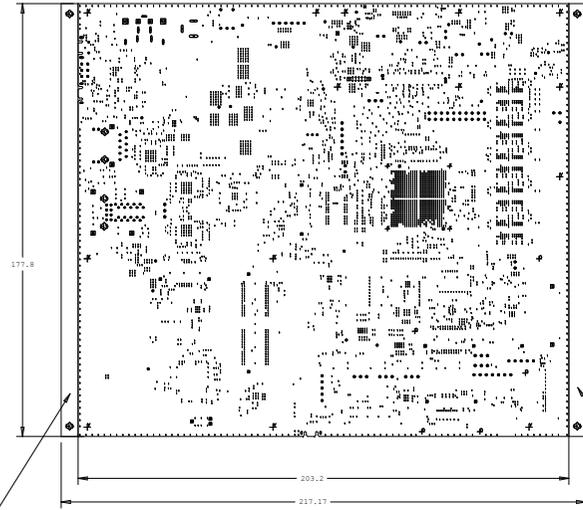
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REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

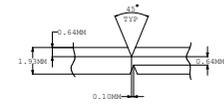
- FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2/ PER IPC-6011. PCB SHALL BE MANUFACTURED USING I-SPEED OR EQUIVALENT.
- MATERIALS:
 - LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/125. (MIN.TG 170)
 - COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150, UNLESS OTHERWISE SPECIFIED. ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35UM (1 OZ.). FOR OUTER LAYERS 46UM (1.3 OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
- ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
- BOM AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTHS.
- CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:
 - ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04+0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
 - APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE EPOXY MATERIAL AND CAP PLATED. ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN. THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED.
 - SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREA.
 - SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.00079"), INCREASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM (0.00047") AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM (0.0006").
- ALL HOLES SURROUNDED BY LAND $0.010''$ SHALL BE COMPLIANT TO IPC6012, CLASS 2.
- MARKING:
 - BOARD SHALL MEET THE REQUIREMENTS OF UL-796 WITH FLAMMABILITY RATING OF MINIMUM 94V-1. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- TEST REQUIREMENTS:
 - 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
- THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
- TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
- FINISHED PCB THICKNESS SHALL BE 0.0759" +/-10%.
- MIN TRACE WIDTH/SPACING ON BOARD IS 0.0037/0.0047".
- ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
- DA WITH 40UM DRILL HAS A DUPLICATE HOLE AT ONE OF THE LOCATION, THIS SHALL BE IGNORED DURING FABRICATION. AND QUANTITY CAN BE CONSIDERED AS 11 HOLES.
- REMOVE ALL NON FUNCTIONAL VIA PAD ONLY ON ALL INTERNAL LAYERS.

DRILL CHART: TOP TO BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+3.0/-4.0	PLATED	4867
•	24.0	+3.0/-3.0	PLATED	10
•	32.0	+2.0/-2.0	PLATED	2
•	32.0	+3.0/-3.0	PLATED	5
•	36.0	+2.0/-3.0	PLATED	38
•	40.0	+2.0/-2.0	PLATED	38
•	40.0	+3.0/-3.0	PLATED	63
•	44.0	+2.0/-2.0	PLATED	21
•	46.0	+3.0/-3.0	PLATED	6
•	46.0	+3.0/-3.0	PLATED	8
•	46.0	+3.0/-3.0	PLATED	8
•	46.0	+3.0/-3.0	PLATED	2
•	46.0	+3.0/-3.0	NON-PLATED	2
•	46.0	+3.0/-3.0	NON-PLATED	12
•	46.0	+3.0/-3.0	NON-PLATED	3
•	46.0	+3.0/-3.0	NON-PLATED	4
•	46.0	+3.0/-3.0	NON-PLATED	4
•	46.0	+3.0/-3.0	NON-PLATED	5
•	46.0	+3.0/-3.0	NON-PLATED	14
•	46.0	+3.0/-3.0	NON-PLATED	8
•	52.0x24.0	+3.0/-3.0	PLATED	2
•	52.0x24.0	+3.0/-3.0	PLATED	2
•	64.0x32.0	+3.0/-3.0	PLATED	2
•	66.0x24.0	+3.0/-3.0	PLATED	1
•	66.0x24.0	+3.0/-3.0	PLATED	2
•	66.0x24.0	+3.0/-3.0	PLATED	4
•	120.0x30.0	+3.0/-3.0	PLATED	1
•	120.0x30.0	+3.0/-3.0	PLATED	1
•	140.0x40.0	+3.0/-3.0	PLATED	1



DETAIL-A

DETAIL-A



DETAIL-A (V-GROOVE DETAILS) SCALE: NTS

IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH (Mils)	SPACING (Mils)	IMPEDANCE (Ohms)	REF LAYER
01	EDGE COUPLED STRIPLINE	L12	3.0	7.9	100	L11/L13
02	EDGE COUPLED STRIPLINE	L5	3.5	5.0	90	L4/L6
03	EDGE COUPLED STRIPLINE	L10, L12	4.3	4.4	80	L9/L11, L11/L13
04	STRIPLINE	L3	3.3	NA	50	L2/L4, L4/L6
05	STRIPLINE	L3, L5, L10, L12	5.0	NA	40	L2/L4, L4/L6, L9/L11, L11/L13
06	EDGE COUPLED MICROSTRIP	L1, L14	4.2	7.4	100	L2, L13
07	EDGE COUPLED MICROSTRIP	L1, L14	4.1	4.4	90	L2, L13
08	EDGE COUPLED MICROSTRIP	L1, L14	6.2	5.3	80	L2, L13
10	EDGE COUPLED MICROSTRIP	L1	10.5	5.0	85	L4
11	MICROSTRIP	L1, L14	5.2	NA	50	L2, L13
12	MICROSTRIP	L1, L14	8.2	NA	40	L2, L13

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS (INCHES)
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01 PRIMARY SIDE	-0.5oz+PLATING		0.00320
L02 GROUND-PLANE-1	1oz.		0.00400
L03 INNER-SIGNAL-1	1oz.		0.00350
L04 GROUND-PLANE-2	1oz.		0.00400
L05 INNER-SIGNAL-2	1oz.		0.00350
L06 POWER-PLANE-1	1oz.		0.00350
L07 POWER-PLANE-2	1oz.		0.00350
L08 POWER-PLANE-3	1oz.		0.00950
L09 GROUND-PLANE-3	1oz.		0.00500
L10 INNER-SIGNAL-3	1oz.		0.00350
L11 GROUND-PLANE-4	1oz.		0.00400
L12 INNER-SIGNAL-4	1oz.		0.00350
L13 GROUND-PLANE-5	1oz.		0.00400
L14 SECONDARY SIDE	-0.5oz+PLATING		0.00320
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

SIGNATURES	DATE	TEXAS INSTRUMENTS	PROC062
LAYOUT BY JA	280819		
REVIEWED BY UAK	280819		
APPROVED BY AMB	280819		
AM654x EVM PROCESSOR BOARD			
	SIZE D		Rev 24
	SCALE: NONE		SHEET 1 OF 21

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