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REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

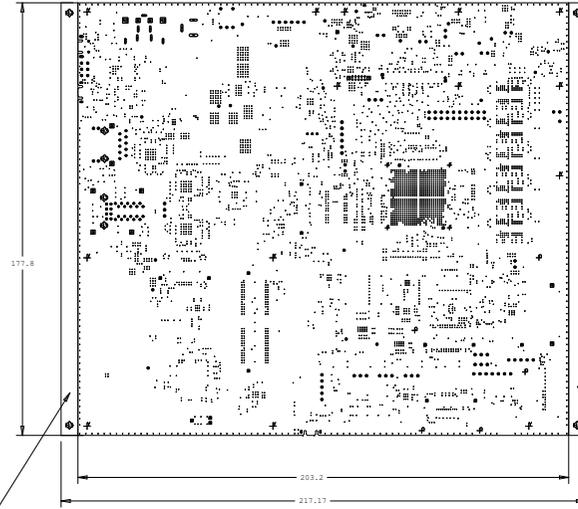
FABRICATION NOTES:

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING 1-SPEED OR EQUIVALENT.
- MATERIALS:
  - LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/124. (MIN.TG 170)
  - COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150, UNLESS OTHERWISE SPECIFIED. ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PREAM LAYERS TO BE 15UM (1 OZ.). FOR OUTER LAYERS 46UM (1.3 OZ.). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
- ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
- BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
- CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:
  - ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.145/0.04 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
  - APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-BM-840, CLASS B, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDERMASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN. VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE EPOXY MATERIAL AND CAP PLATED.
  - SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
  - SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.00079"), INCREASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM (0.00047") AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM (0.0006").
  - ALL HOLES SURROUNDED BY LAND <=0.10" SHALL BE COMPLIANT TO IPC6012, CLASS 2.
- MARKING:
  - BOARD SHALL MEET THE REQUIREMENTS OF UL-796 WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- TEST REQUIREMENTS:
  - 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
- THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
- TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
- FINISHED PCB THICKNESS SHALL BE 0.075" +/-10%.
- MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.004".
- ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
- DA WITH 40UM DRILL HAS A DUPLICATED HOLE AT ONE OF THE LOCATION, THIS SHALL BE IGNORED DURING FABRICATION. AND QUANTITY CAN BE CONSIDERED AS 11 HOLES.
- REMOVE ALL NON FUNCTIONAL VIA PAD ONLY ON ALL INTERNAL LAYERS.
- FOR STACKUP DETAILS PROC62 STACKUP.pdf SHALL BE REFERRED.
- ENSURE THAT UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON PCB SILKSCREEN

DRILL CHART: TOP TO BOTTOM

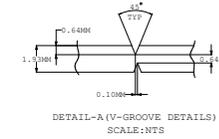
ALL UNITS ARE IN MILS

FIGURE	SIZE	IMPEDANCE	PLATED	QTY
1	24.0	+3.0/-3.0	PLATED	10
2	32.0	+2.0/-2.0	PLATED	2
3	32.0	+3.0/-3.0	PLATED	8
4	36.0	+3.0/-3.0	PLATED	38
5	40.0	+2.0/-2.0	PLATED	36
6	40.0	+3.0/-3.0	PLATED	63
7	44.0	+2.0/-2.0	PLATED	23
8	46.0	+3.0/-3.0	PLATED	4
9	66.0	+3.0/-3.0	PLATED	2
10	86.0	+3.0/-3.0	PLATED	2
11	34.0	+2.0/-2.0	NON-PLATED	2
12	40.0	+3.0/-3.0	NON-PLATED	12
13	42.0	+3.0/-3.0	NON-PLATED	3
14	36.0	+3.0/-3.0	NON-PLATED	4
15	68.0	+3.0/-3.0	NON-PLATED	4
16	88.0	+3.0/-3.0	NON-PLATED	5
17	138.0	+3.0/-3.0	NON-PLATED	14
18	126.0	+3.0/-3.0	NON-PLATED	8
19	52.0x24.0	+3.0/-3.0	PLATED	2
20	52.0x24.0	+3.0/-3.0	PLATED	2
21	54.0x24.0	+3.0/-3.0	PLATED	2
22	86.0x24.0	+3.0/-3.0	PLATED	1
23	86.0x24.0	+3.0/-3.0	PLATED	2
24	98.0x24.0	+3.0/-3.0	PLATED	4
25	120.0x30.0	+3.0/-3.0	PLATED	1
26	120.0x30.0	+3.0/-3.0	PLATED	1
27	140.0x40.0	+3.0/-3.0	PLATED	1



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(OHMS)	REF LAYER
01	EDGE COUPLED STRIPLINE	L12	3.0	7.9	100	L11/L13
02	EDGE COUPLED STRIPLINE	L5	3.5	5.0	90	L4/L6
03	EDGE COUPLED STRIPLINE	L3, L12	4.3	4.4	80	L2/L4
04	STRIPLINE	L10, L12	3.3	NA	50	L9/L11, L14/L16
05	STRIPLINE	L3, L5	5.0	NA	40	L2/L4, L4/L6
06	EDGE COUPLED MICROSTRIP	L1, L14	4.2	7.4	100	L2, L13
07	EDGE COUPLED MICROSTRIP	L1, L14	4.1	4.4	90	L2, L13
08	EDGE COUPLED MICROSTRIP	L1, L14	6.2	5.3	80	L2, L13
10	EDGE COUPLED MICROSTRIP	L1	10.5	5.0	85	L4
11	MICROSTRIP	L1, L14	5.2	NA	50	L2, L13
12	MICROSTRIP	L1, L14	8.2	NA	40	L2, L13



LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS (INCHES)
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01 PRIMARY SIDE	-0.5oz*PLATING		0.00320
L02 GROUND-PLANE-1	1oz.		0.00400
L03 INNER-SIGNAL-1	1oz.		0.00350
L04 GROUND-PLANE-2	1oz.		0.00400
L05 INNER-SIGNAL-2	1oz.		0.00350
L06 POWER-PLANE-1	1oz.		0.00350
L07 POWER-PLANE-2	1oz.		0.00950
L08 POWER-PLANE-3	1oz.		0.00500
L09 GROUND-PLANE-3	1oz.		0.00500
L10 INNER-SIGNAL-3	1oz.		0.00400
L11 GROUND-PLANE-4	1oz.		0.00350
L12 INNER-SIGNAL-4	1oz.		0.00350
L13 GROUND-PLANE-5	1oz.		0.00400
L14 SECONDARY SIDE	-0.5oz*PLATING		0.00320
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

SIGNATURES	DATE	TEXAS INSTRUMENTS AM654x EVM PROCESSOR BOARD	PROC62
LAYOUT BY VU/UD	280421		
REVIEWED BY ZA	280421		
APPROVED BY AMB	280421		
SCALE: NONE		SIZE D	Rev B
		SHEET 1 OF 21	

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