MAXWELL CUSTOMER PROCESSOR BOARD

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REV	B
VER	1.0

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Texas Instruments

MISTRAL

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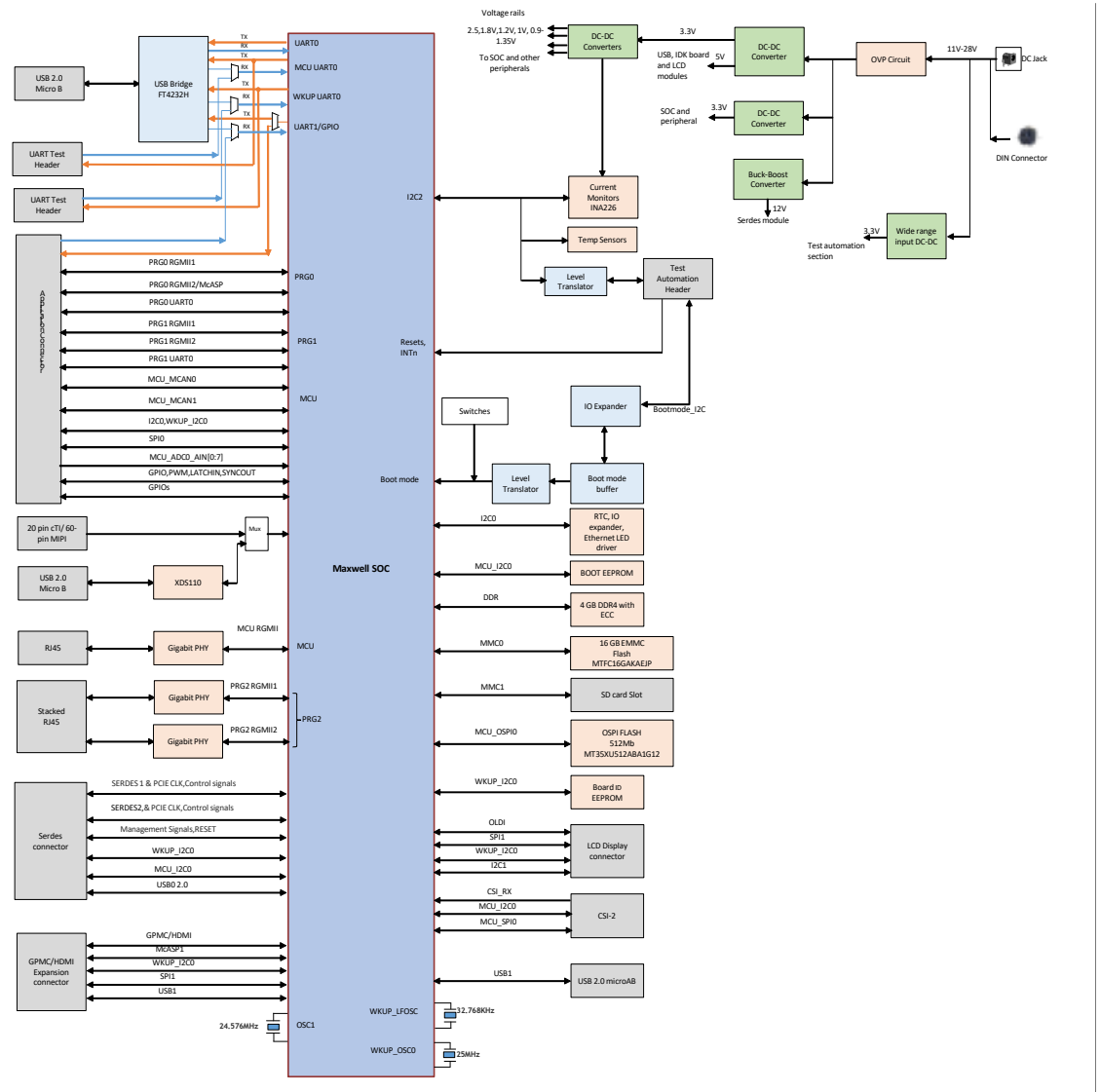
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	7th APR 2021	Drafted from "PROC062A_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	7th APR 2021	Changed SD card Load Switch to TPS22918DBVR	Mistral Design Team	AJIT MB	AJIT MB
1.0	12th APR 2021	Baselined	Mistral Design Team	AJIT MB	AJIT MB

BLOCK DIAGRAM_CP BOARD



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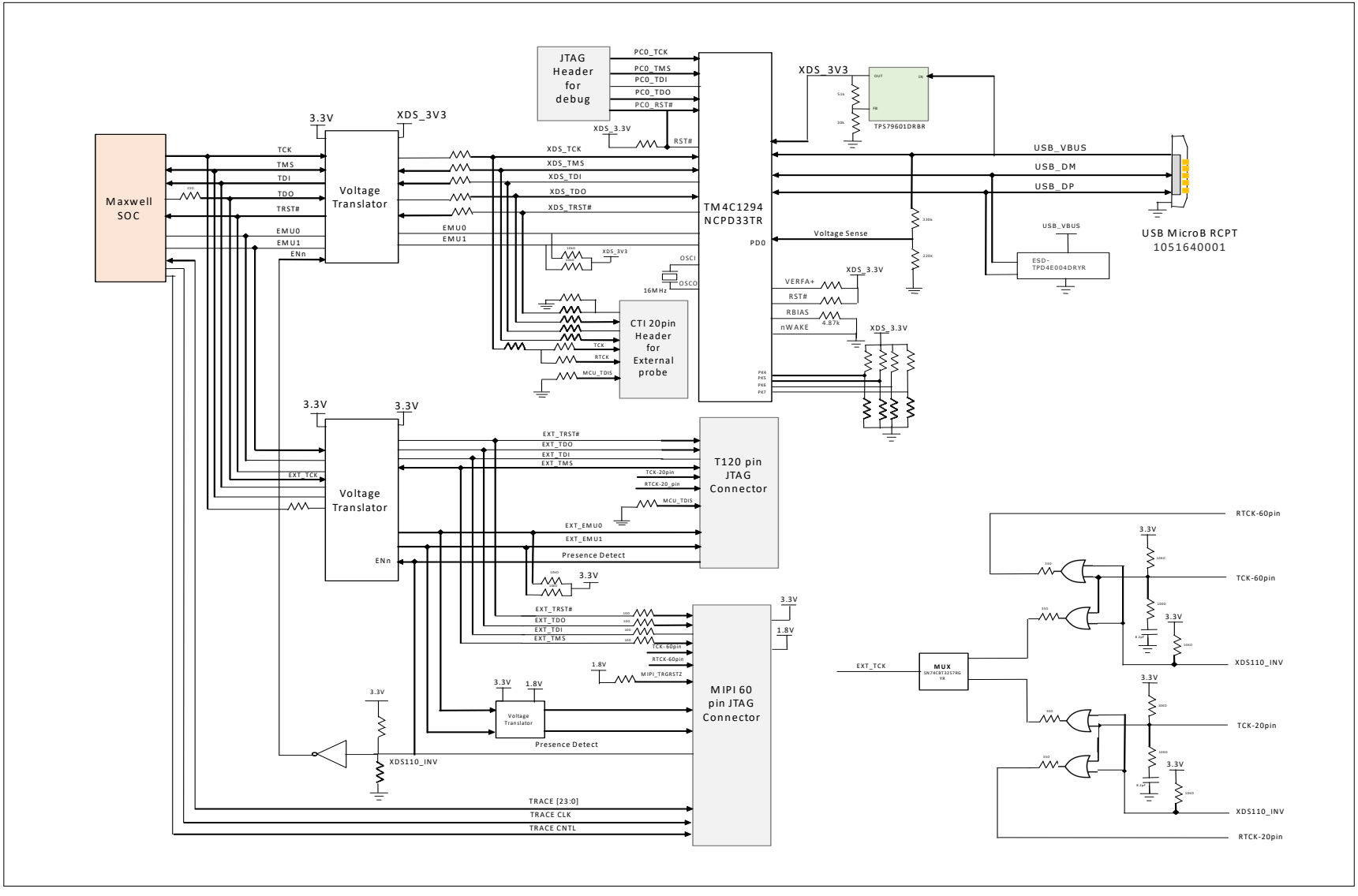
BLOCK DIAGRAM_XDS110



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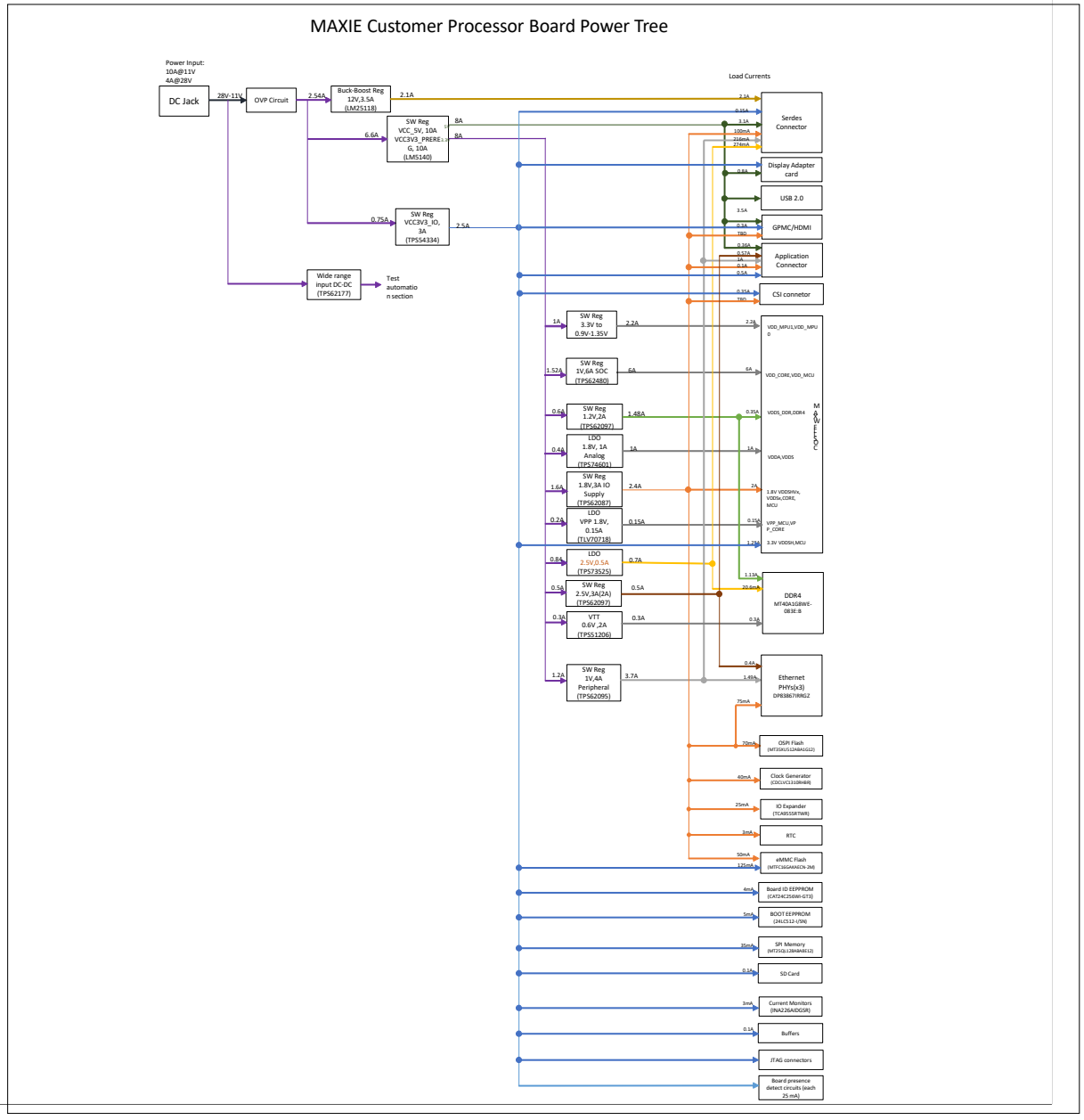
POWER FLOW DIAGRAM



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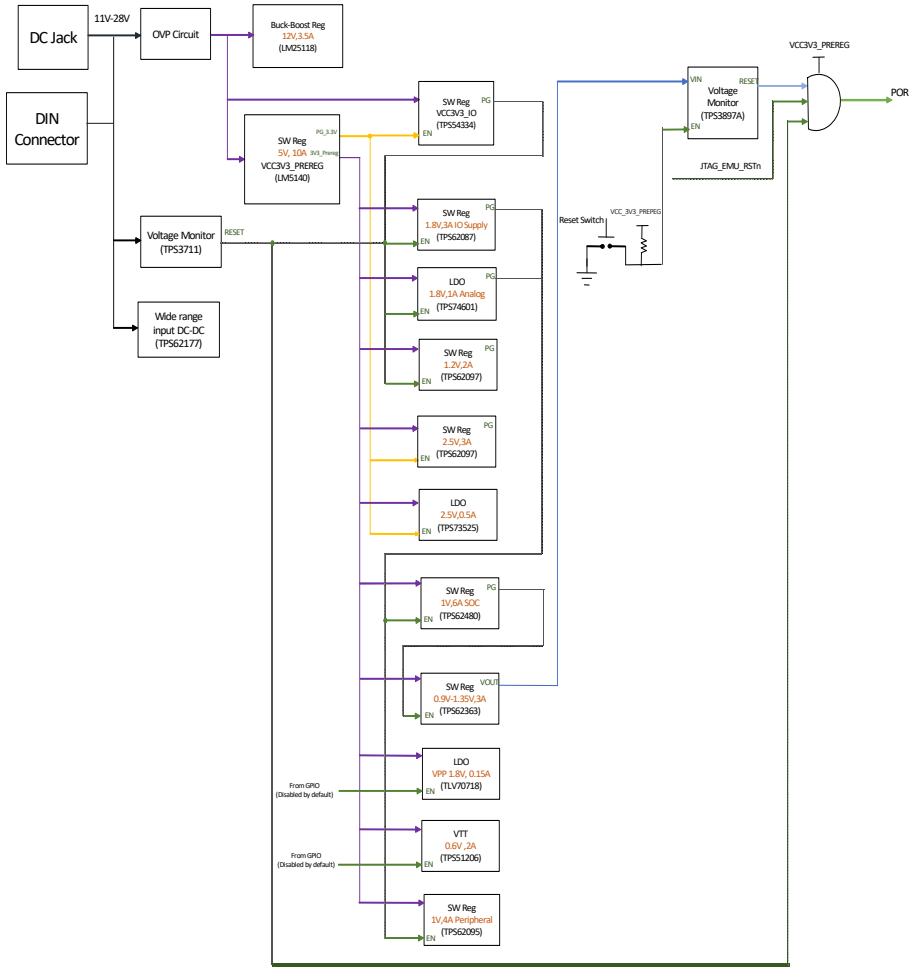
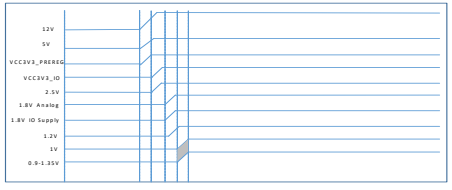
POWER SEQUENCE



Power up Sequence

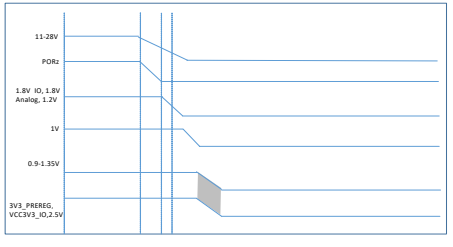


Power up Sequence:
12V, 5V,3V3_PREREG --->VCC3V3_IO, 2.5V --->1.8V Analog, 1.8V IO Supply ---> 1V SOC ,0.9-1.35V

There is no sequencing for 1V Peripheral supply

Note: Grey shaded areas are windows where it is valid to ramp the voltage rail.

Power down Sequence



Power down Sequence:
1.2V, 1.8V Analog, 1.8V IO Supply ---> 1V SOC ---> 0.9-1.35V --->3V3_PREREG, VCC3V3_IO, 2.5V

Note: Grey shaded areas are windows where it is valid to ramp down the voltage rail.

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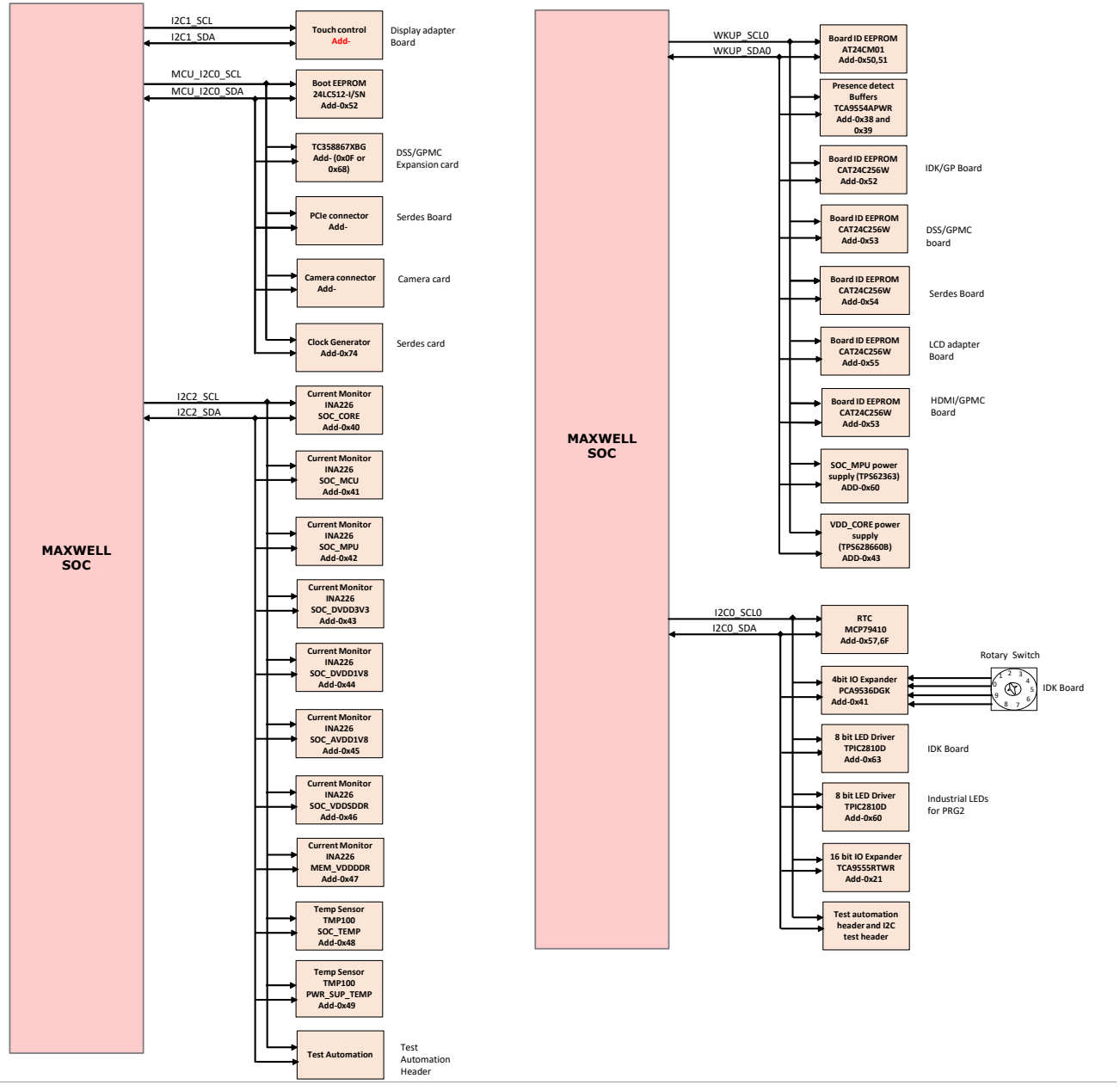
GPIO MAPPING TABLE

Total No of GPIOs Required from Maxwell SoC								
Sl No	**GPIO Description**	**Required on**	**FUNCTIONALITY**	**GPIO Number**	**SoC Muxed Signal name**	**Direction WRT CTRL**	**Default state**	**Active state**
1	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_24	MCU_OSPI0_CSN1	Input	High	Low
2	Two MCU Domain GPIO for CP board push button1	Customer Processor Board	Push button	WKUP_GPIO0_27	MCU_OSPI1_DQS	Input	High	Low
3	eMMC Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
4	OSPI flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
5	SPI NOR flash Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
6	ICSSG_PRG2_Ethernet PHY Reset control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
7	ICSSG_PRG2_Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_87	EXT_REFCLK1	Input/Output	High	Low
8	ICSSG_Ethernet PHY_1 Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	WKUP_GPIO0_50	MCU_SPI0_D1	Input	Low	High
9	ICSSG_Ethernet PHY_2 Link Detection GPIO	Customer Processor Board	Link Detection (GPIO Input)	WKUP_GPIO0_8	WKUP_GPIO0_8	Input	Low	High
10	MCU domain Ethernet PHY Reset Control GPIO	Customer Processor Board	Reset	I2C GPIO Expander		Output	High	Low
11	MCU domain Ethernet PHY Interrupt GPIO	Customer Processor Board	Interrupt	GPIO1_80	MMC1_SDWP	Input/Output	High	Low
12	Three GPIO's are required to control the Mux select between UART test header RX , Application board & FT4232_ UART _RX	Customer Processor Board	Mux Selection	I2C GPIO Expander		Output	High	Low
13				I2C GPIO Expander		Output	High	Low
14				I2C GPIO Expander		Output	High	Low
15	VPP LDO enable	Customer Processor Board	VPP_EN	WKUP_GPIO0_26	MCU_OSPI1_LBCLKO	Output	Low	High
16	One WKUP_GPIO for VTT Regulator Enable	Customer Processor Board	VTT_EN	WKUP_GPIO0_28	MCU_OSPI1_D0	Output	Low	High
17	GPIO0 to drive PRG2 LED0	Customer Processor Board	LEDs	I2C GPIO Expander		Output	Low	High
18	GPIO1 to drive PRG2 LED1	Customer Processor Board	LEDs	I2C GPIO Expander		Output	Low	High
19	GPIO2 to drive PRG2 LED2	Customer Processor Board	LEDs	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	Low	High
20	GPIO3 to drive PRG2 LED3	Customer Processor Board	LEDs	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	Low	High
21	SOC MPU regulator reset control	Customer Processor Board	RESET_SoC_MPU	I2C GPIO Expander		Output	High	Low
22	SD card load switch enable control	Customer Processor Board	MMC1_SD_EN	I2C GPIO Expander		Output	High	Low
23	IDK_ICSSG_PRG0_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO1_58	PRG0_PRU1_GPO9	Output	High	Low
24	IDK_ICSSG_PRG0_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO1_39	PRG0_PRU0_GPO10	Input/Output	High	Low
25	IDK_ICSSG_PRG1_Ethernet PHY Reset Control GPIO	IDK /GP Application board	Reset	GPIO1_38	PRG0_PRU0_GPO9	Output	High	Low
26	IDK_ICSSG_PRG1_Ethernet PHY Interrupt GPIO	IDK /GP Application board	Interrupt	GPIO1_59	PRG0_PRU1_GPO10	Output	High	Low
27	IDK_ICSSG_Ethernet PHY_1 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO1_36/GPIO1_37	PRG0_PRU0_GPO7/PRG0_PRU0_GPO8	Input	Low	High
28	IDK_ICSSG_Ethernet PHY_2 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO1_56/GPIO1_57	PRG0_PRU1_GPO7/PRG0_PRU1_GPO8	Input	Low	High
29	IDK_ICSSG_Ethernet PHY_3 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO0_63/GPIO0_64	PRG1_PRU0_GPO7/PRG1_PRU0_GPO8	Input	Low	High
30	IDK_ICSSG_Ethernet PHY_4 Link Detection GPIO	IDK /GP Application board	Link Detection (GPIO Input)	GPIO0_83/GPIO0_84	PRG1_PRU1_GPO7/PRG1_PRU1_GPO8	Input	Low	High
31	IDK_ICSSG0_Ethernet LED0	IDK /GP Application board	LEDs	GPIO1_46	PRG0_PRU0_GPO17	Output	Low	High
32	IDK_ICSSG0_Ethernet LED1	IDK /GP Application board	LEDs	GPIO1_66	PRG0_PRU1_GPO17	Output	Low	High
33	IDK_ICSSG0_Ethernet LED2	IDK /GP Application board	LEDs	GPIO1_48	PRG0_PRU0_GPO19	Output	Low	High
34	IDK_ICSSG0_Ethernet LED3	IDK /GP Application board	LEDs	GPIO1_68	PRG0_PRU1_GPO19	Output	Low	High
35	IDK_ICSSG0_Ethernet LED4	IDK /GP Application board	LEDs	GPIO0_73	PRG1_PRU0_GPO17	Output	Low	High
36	IDK_ICSSG0_Ethernet LED5	IDK /GP Application board	LEDs	GPIO0_93	PRG1_PRU1_GPO17	Output	Low	High
37	IDK_ICSSG0_Ethernet LED6	IDK /GP Application board	LEDs	GPIO0_75	PRG1_PRU0_GPO19	Output	Low	High
38	IDK_ICSSG0_Ethernet LED7	IDK /GP Application board	LEDs	GPIO0_95	PRG1_PRU1_GPO19	Output	Low	High
39	Touch Reset Control GPIO	LCD Adapter Board	Reset	I2C GPIO Expander		Output	High	Low
40	Touch Interrupt GPIO	LCD Adapter Board	Interrupt	I2C GPIO Expander		Input	Low	High
41	LCD Display Enable GPIO	LCD Adapter Board	LCD_EN	I2C GPIO Expander		Output	High	Low
42	CSI Camera Module Reset Control GPIO	CSI Connector	Reset	I2C GPIO Expander		Output	High	Low
43	Display_ Power_Down GPIO	HDMI / GPMC Daughter Card	Display_PowerDown	I2C GPIO Expander		Output	High	Low
44	Touch Event GPIO	HDMI / GPMC Daughter Card	Interrupt	I2C GPIO Expander		Input	High	Low
45	SGMII PHY reset control	Serdes Modules	Reset	I2C GPIO Expander		Output	High	Low
46	SGMII PHY Interrupt	Serdes Modules	Interrupt	GPIO1_81	NMIN	Input/Output	High	Low

I2C TREE



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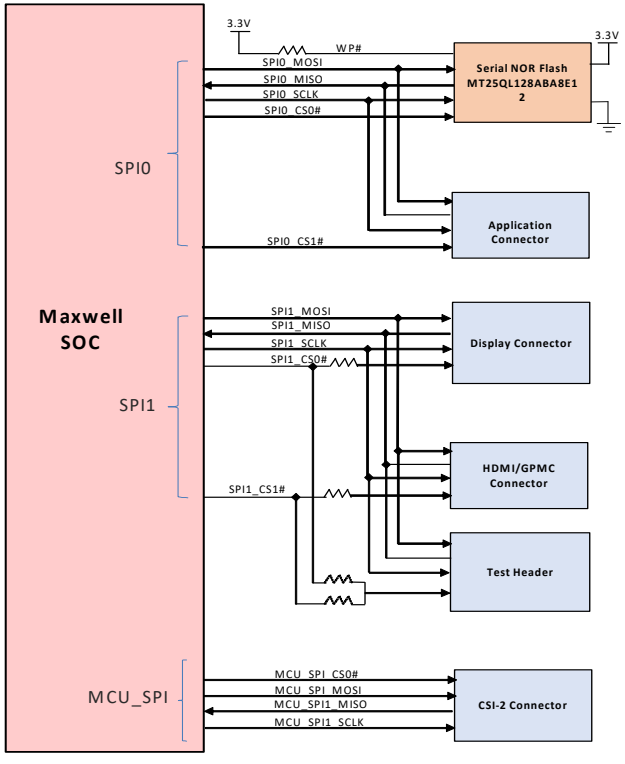
SPI TREE



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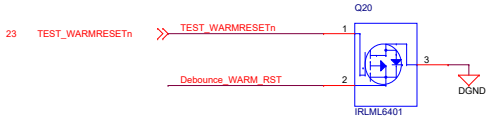
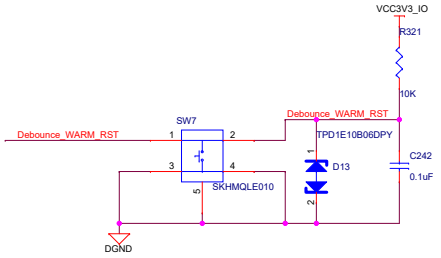
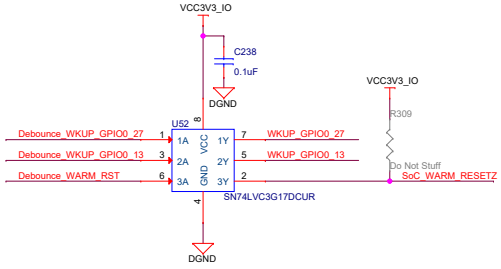
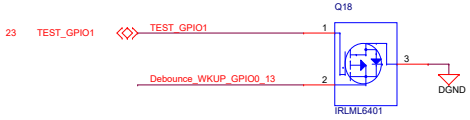
SoC WARM_RST

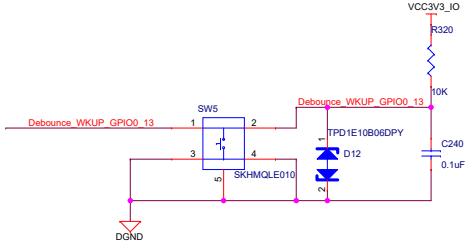


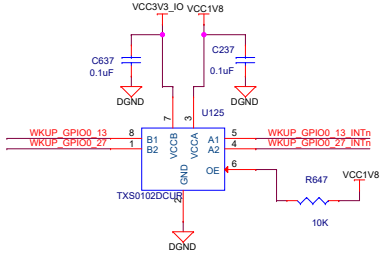


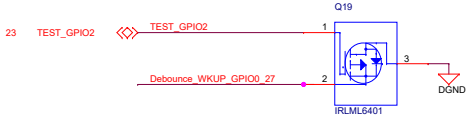


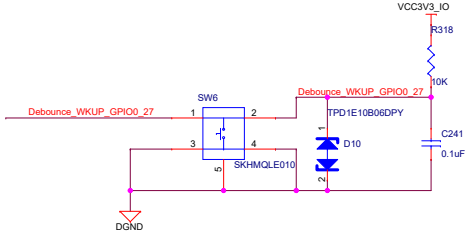
MCU_PUSH BUTTONS

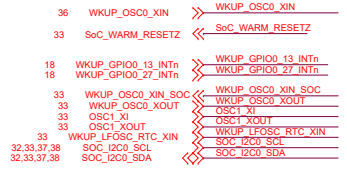




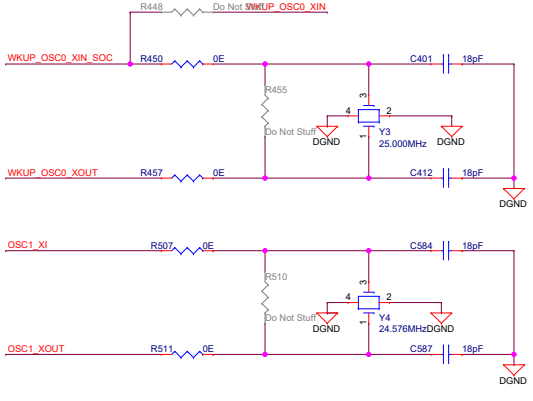


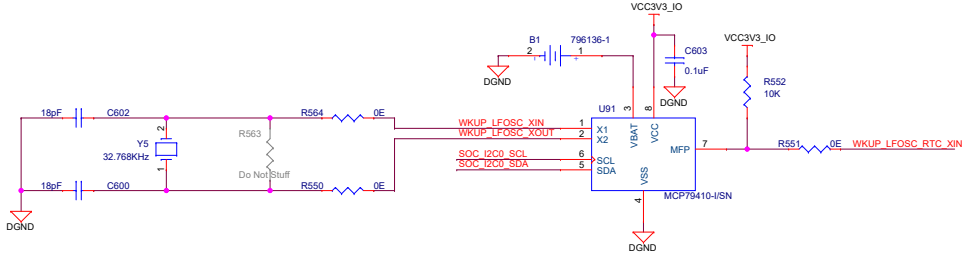






SoC CLOCK





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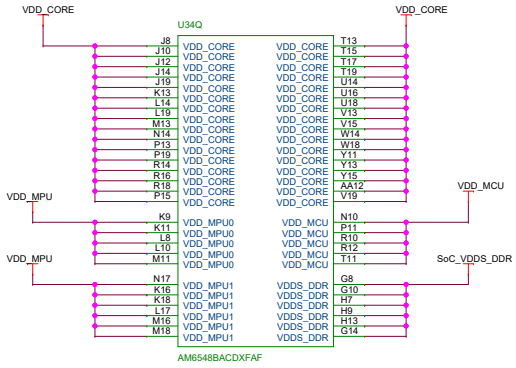
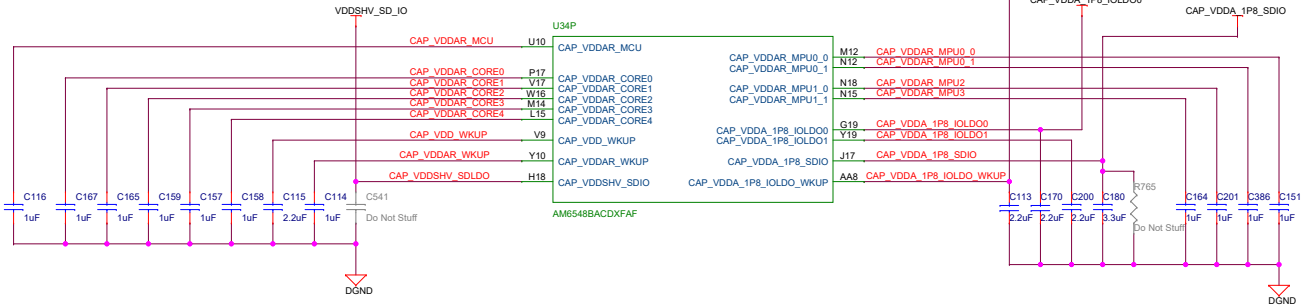
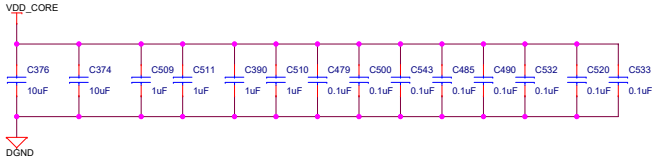
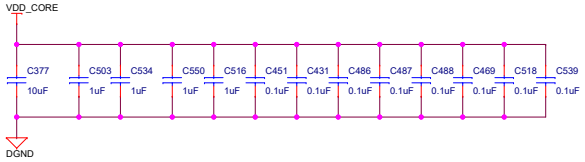
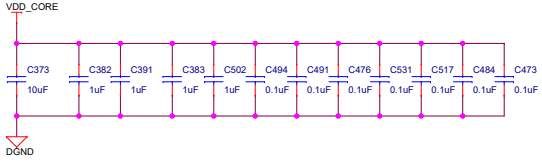
PROCESSOR POWER & DECAPS

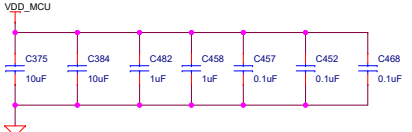


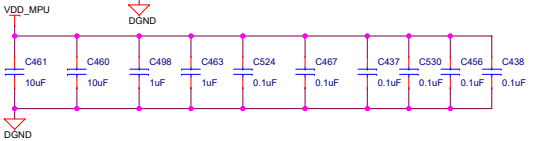


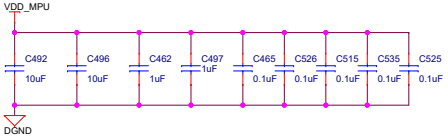


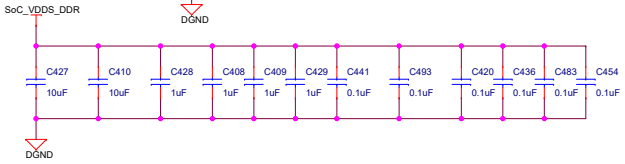












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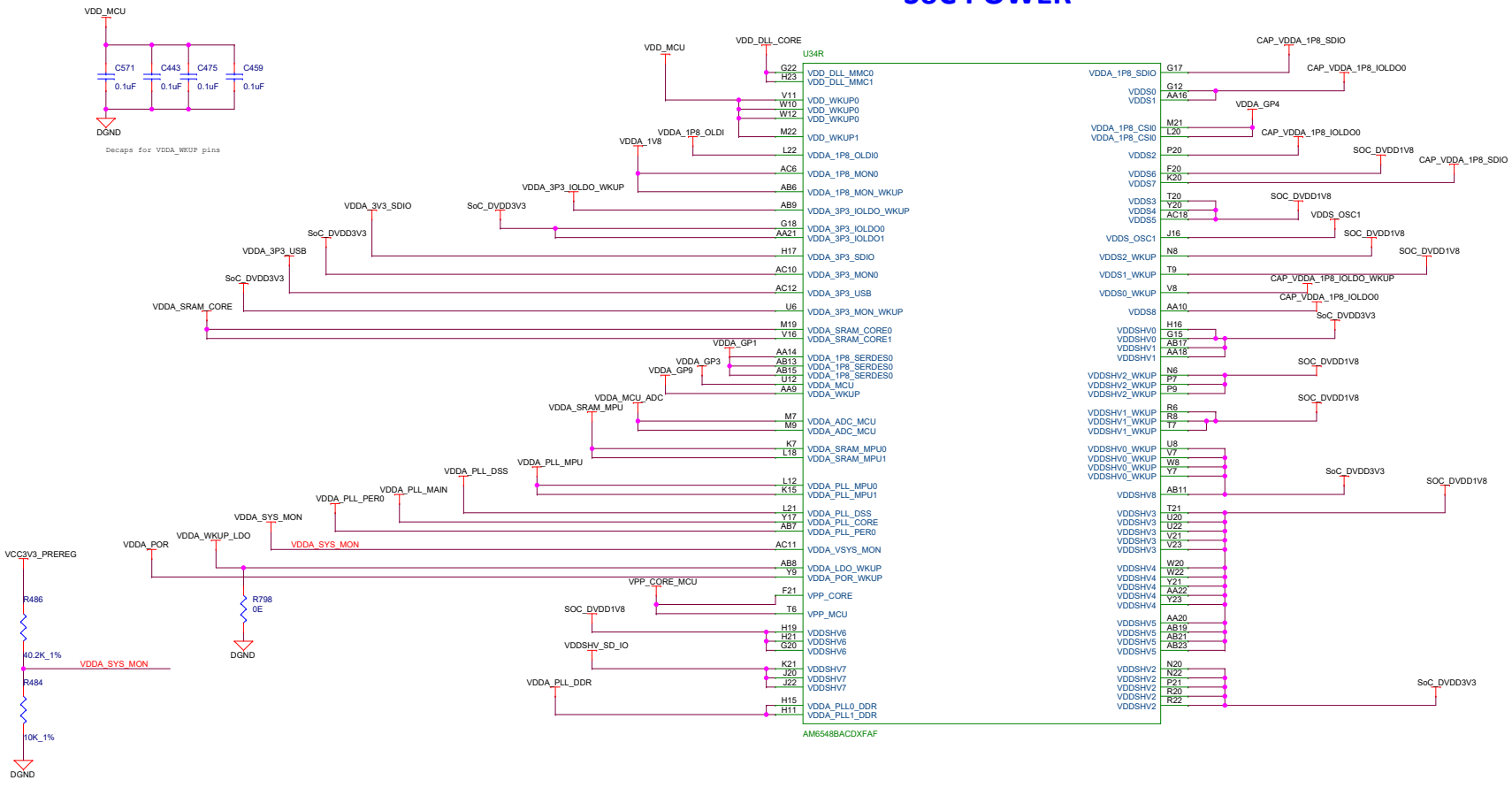
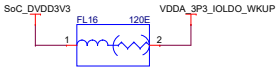
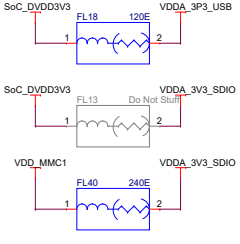
SoC POWER



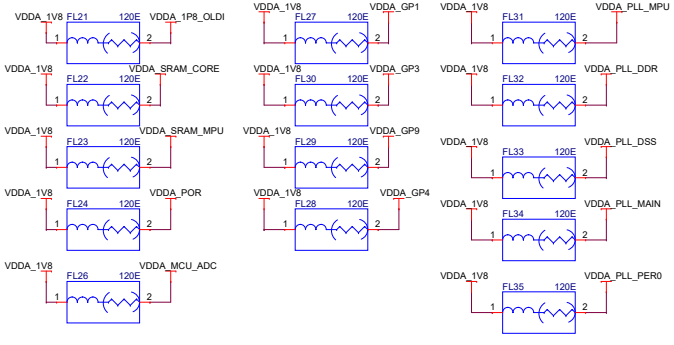
3.3V IO SUPPLY



3.3V ANALOG SUPPLY

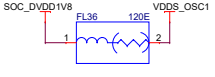


1.8V Analog SUPPLY

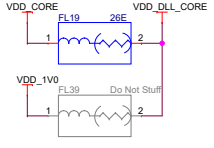


VPP SUPPLY

OSCILLATOR SUPPLY



CORE SUPPLY



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Title	SoC POWER2		
Size	Variant Name = PROC062B001		Rev
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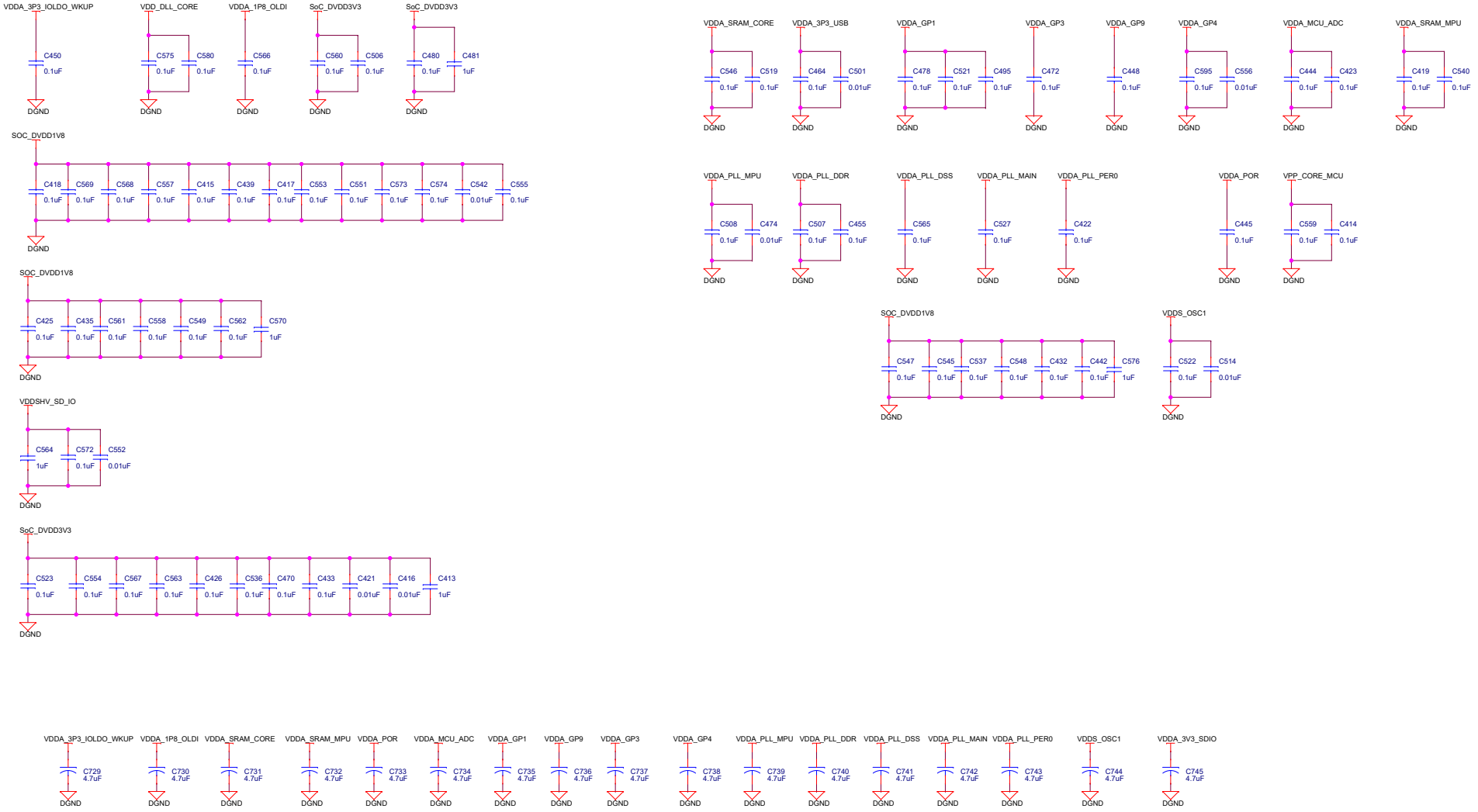
PROCESSOR DECAPS



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Title	SoC POWER3	
Size: C	Variant Name = PROC062B001	Rev: A
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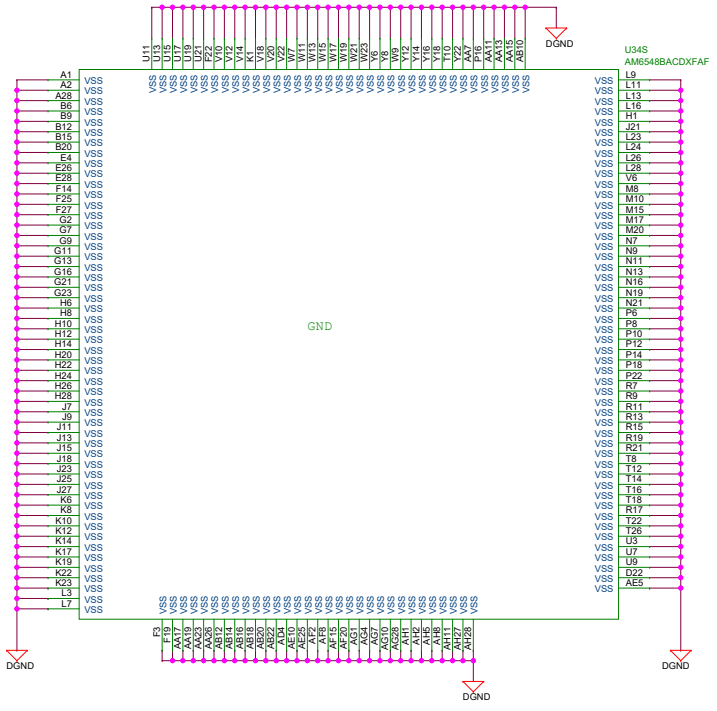
SoC POWER - VSS



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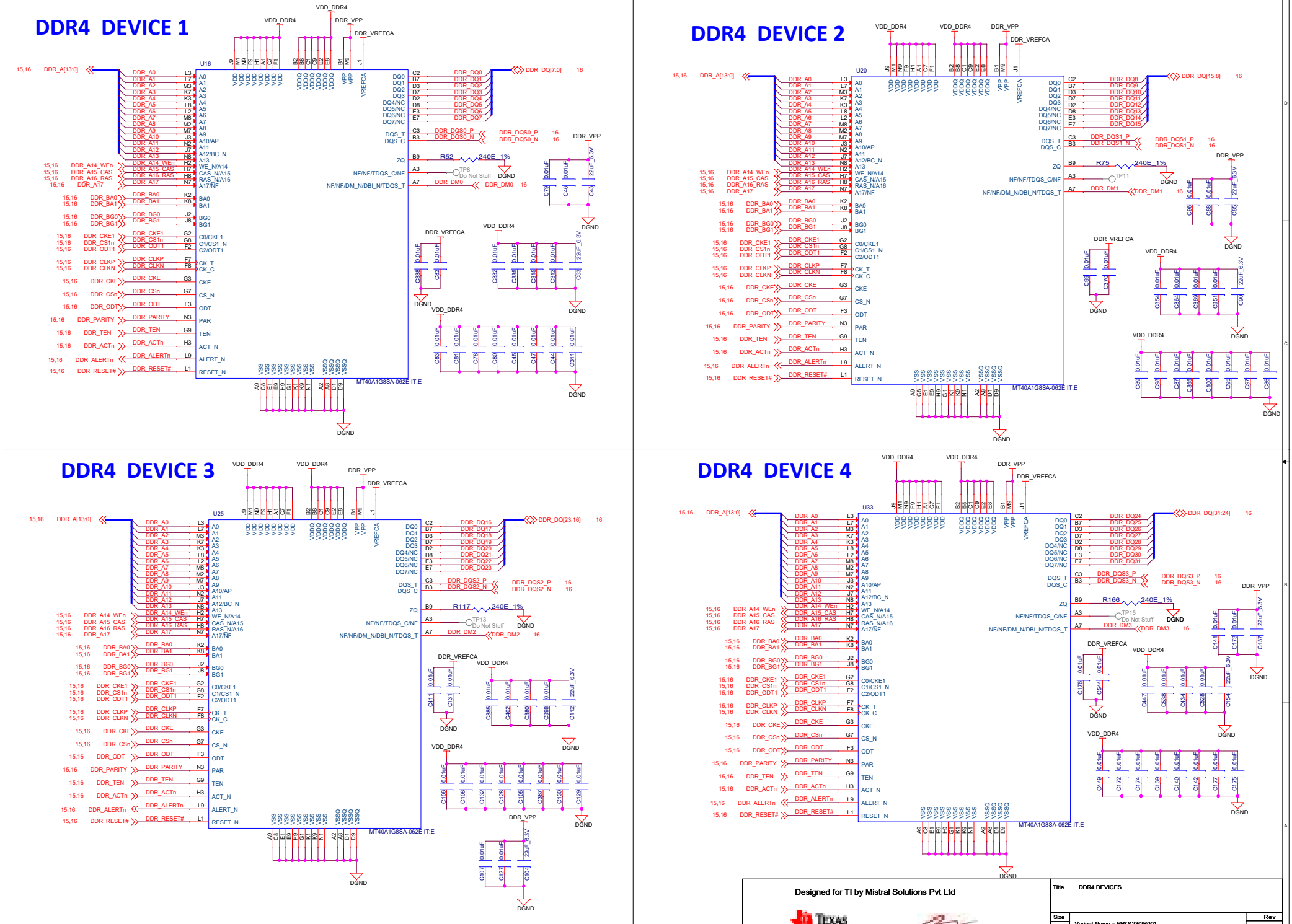
Title	SoC POWER4	
Size	Variant Name = PROC062B001	Rev
C		A
Date: Thursday, July 01, 2021	Sheet 14 of 44	


DDR4 DEVICE 1
DDR4 DEVICE 2
DDR4 DEVICE 3
DDR4 DEVICE 4
VDD_DDR4
DDR_VPP
DDR_VREFCA
DDR_A[13:0]
DDR_DQ[7:0]
DDR_DQ[15:8]
DDR_DQ[23:16]
DDR_DQ[31:24]
MT40A1G8SA-062E IT:E
DGND
Designed for TI by Mistral Solutions Pvt Ltd
Title DDR4 DEVICES
Size C
Variant Name = PROC062B001
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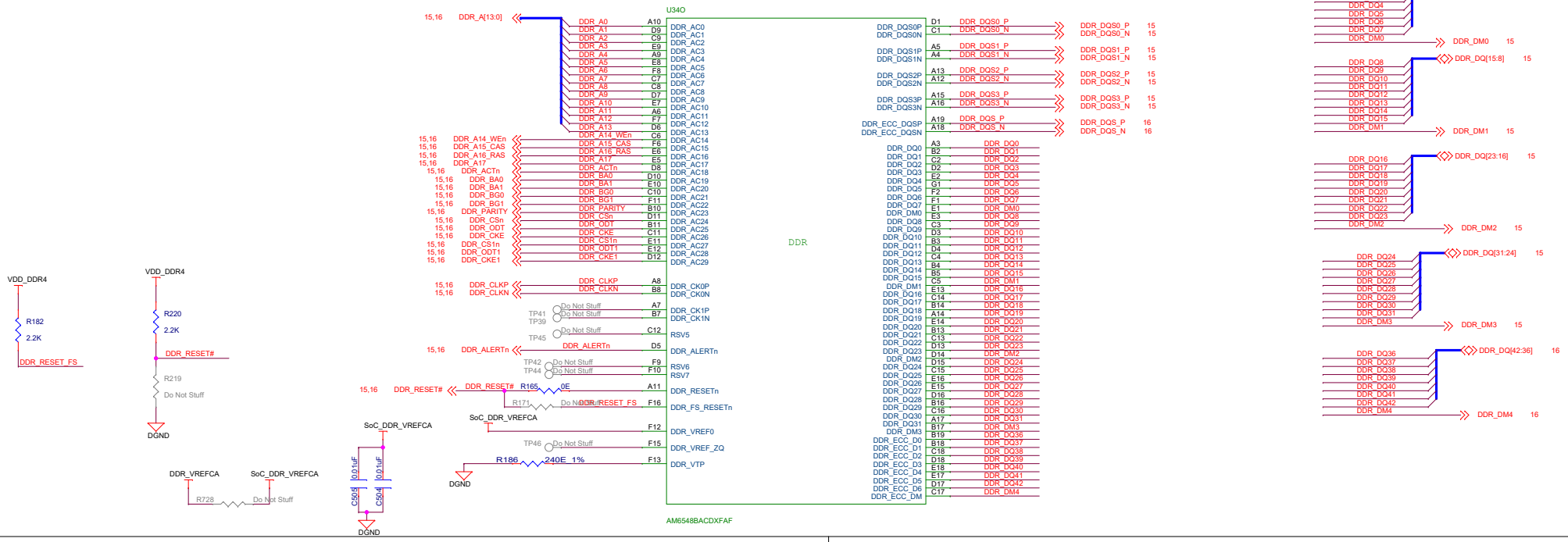
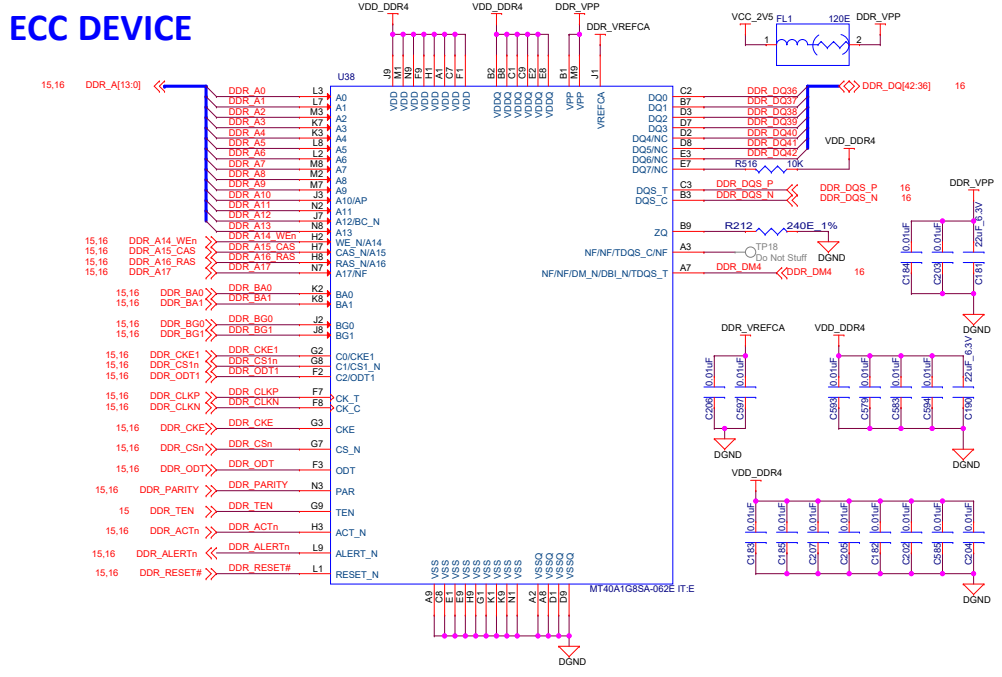
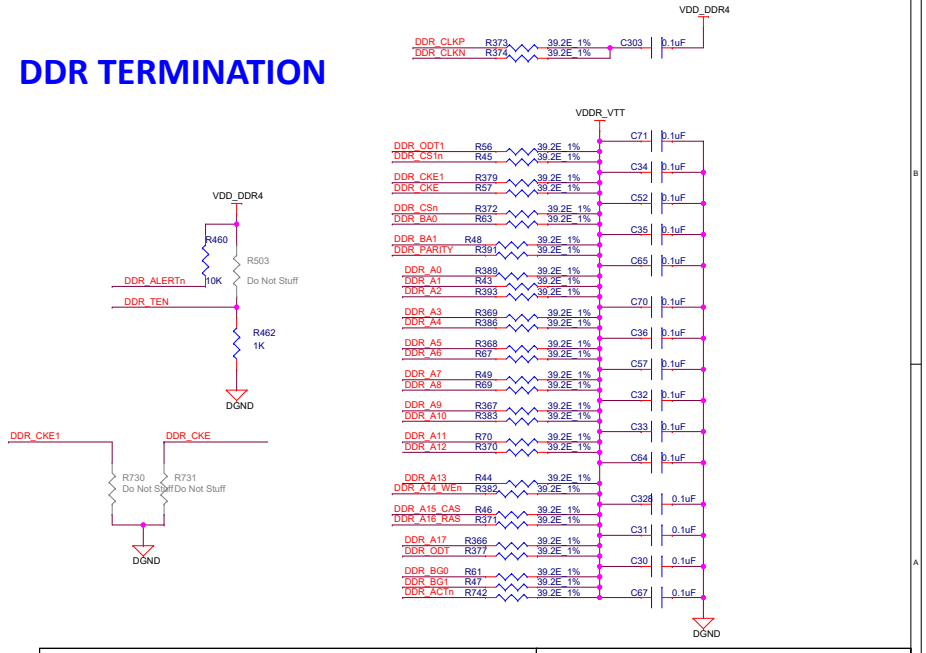
SoC DDR INTERFACE



ECC DEVICE



DDR TERMINATION



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Title	DDR4 ECC & TERMINATIONS	
Size	Variant Name = PROC062B001	Rev
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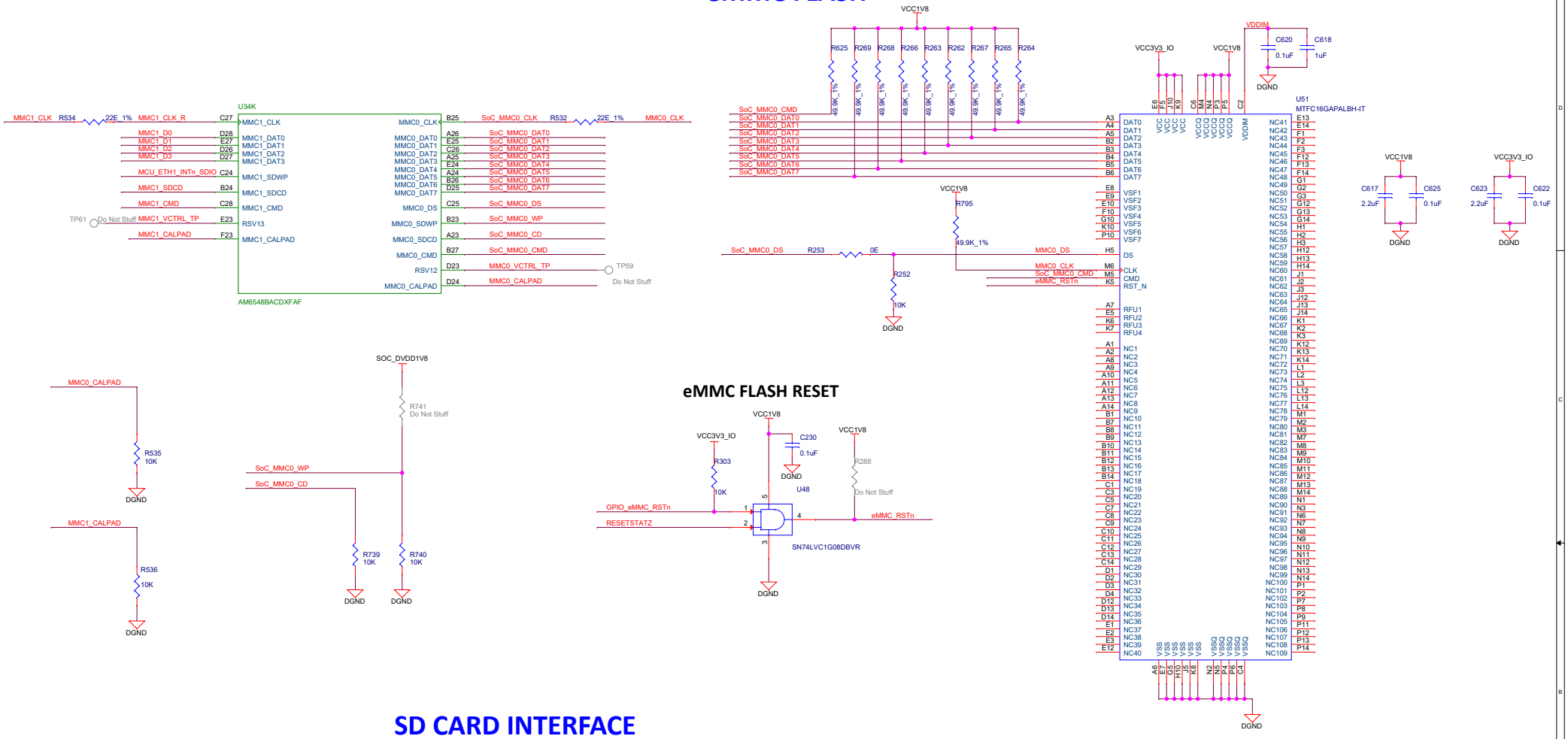
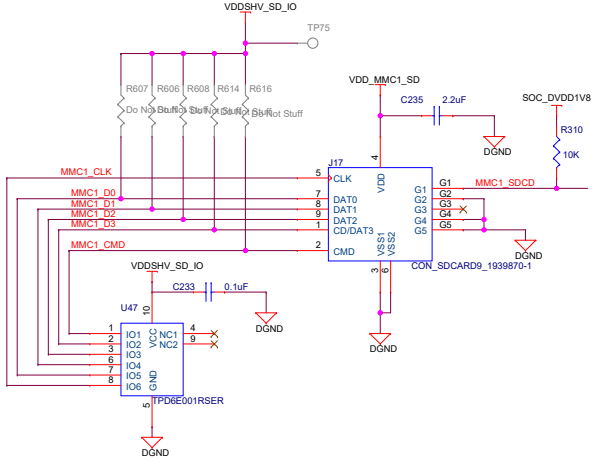
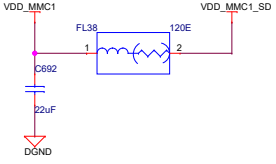
eMMC FLASH

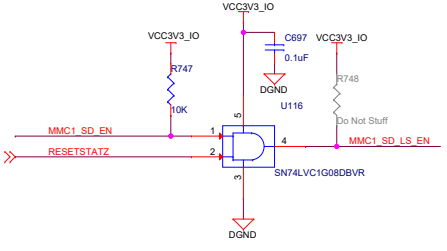


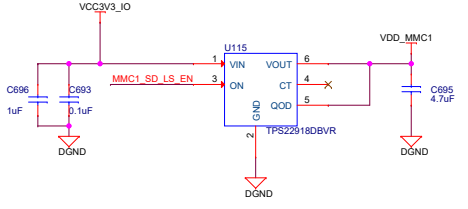
eMMC FLASH RESET

SD CARD INTERFACE









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Title	eMMC FLASH_SDCARD INTERFACE	
Size	Variant Name = PROC062B001	Rev
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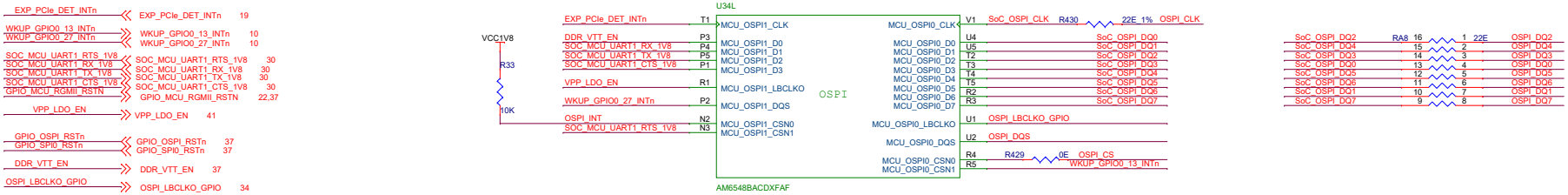
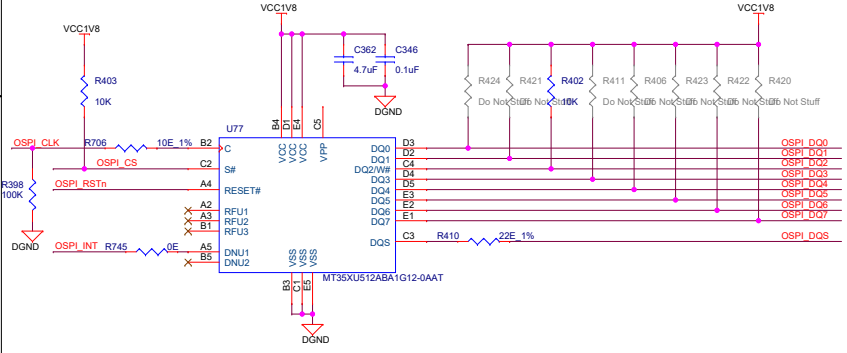
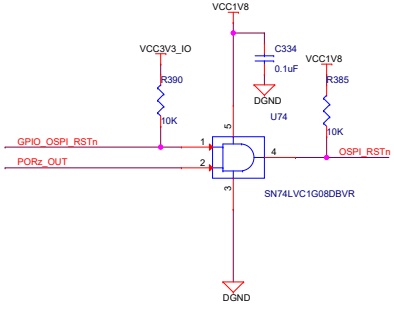
SOC OSPI INTERFACE

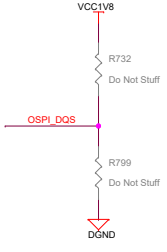


OSPI FLASH

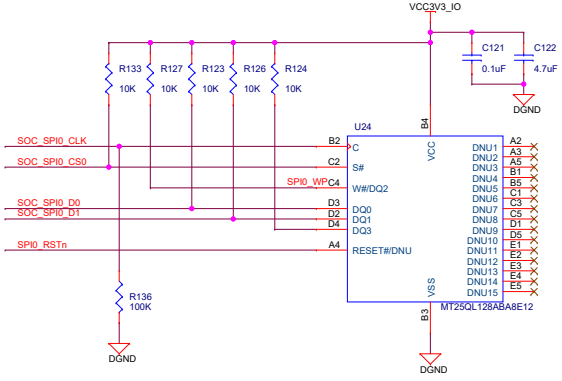


OSPI FLASH RESET

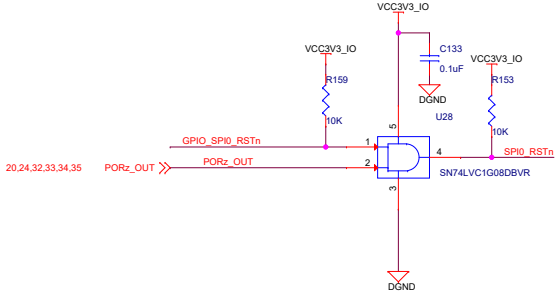




SPI NOR Flash



SPI FLASH RESET



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Title	OSPI FLASH & SPI NOR FLASH	
Size C	Variant Name = PROC062B001	Rev A
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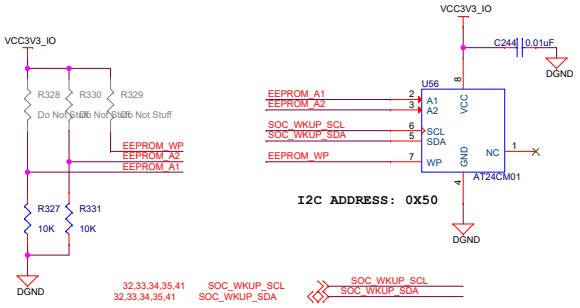
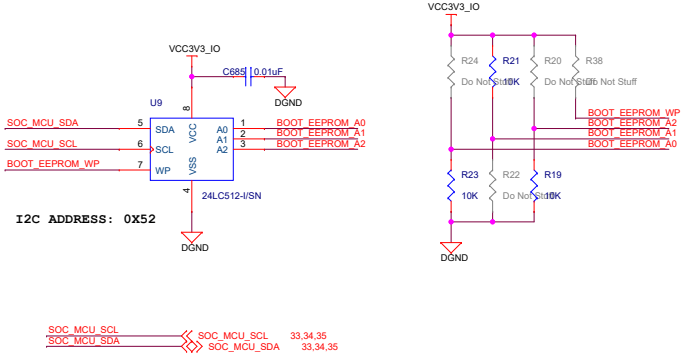
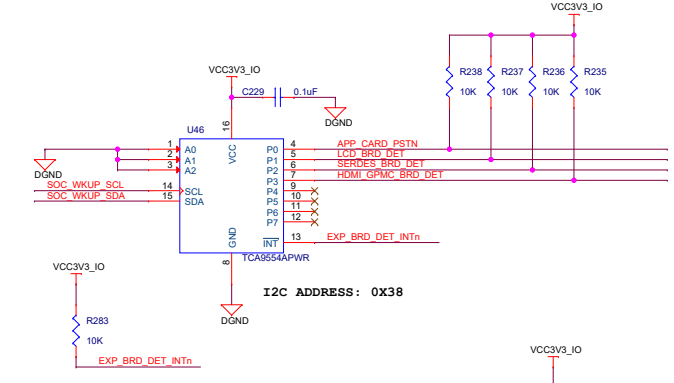
BOARD ID EEPROM



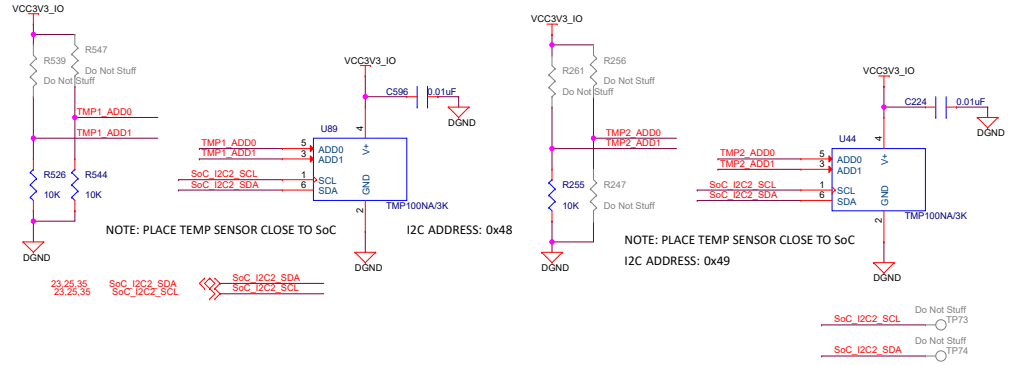
BOOT EEPROM



BOARD PRESENCE DETECT CIRCUIT



TEMPERATURE SENSOR



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Title	EEPROM,PRESENCE DETECTION & TEMP SENSOR	
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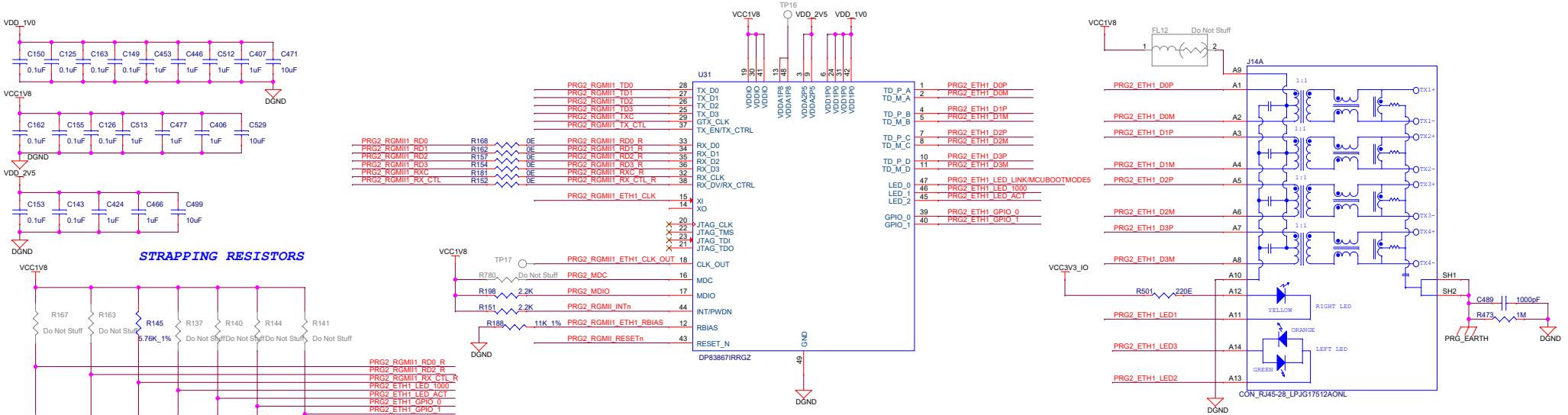
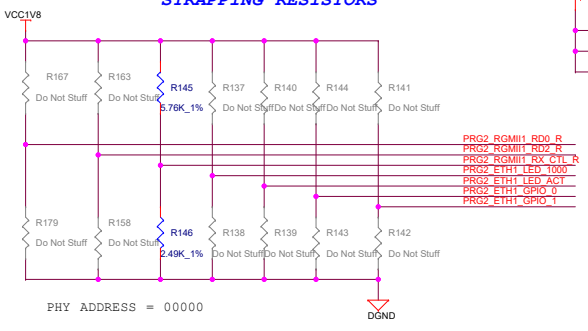
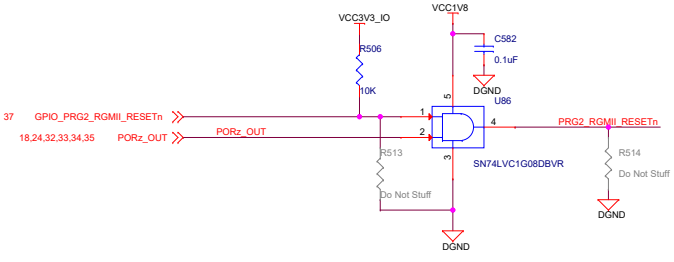
PRG2 RGMII 1

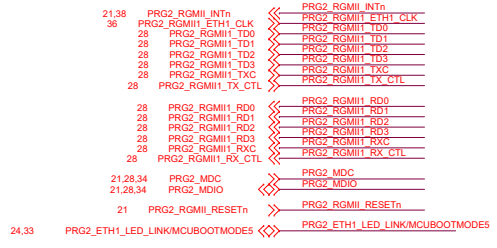


STRAPPING RESISTORS



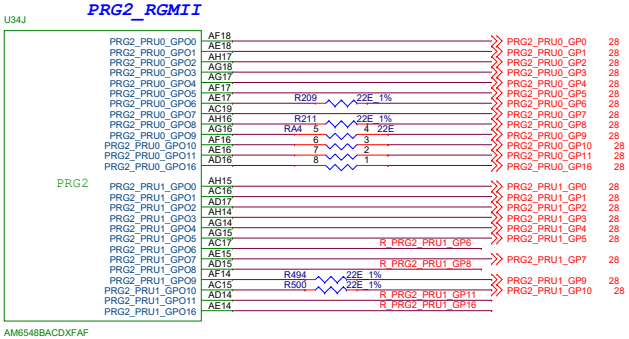
PRG2 PHY1 RESET

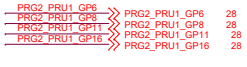




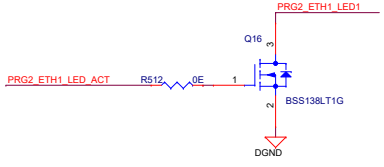
RGMII ETHERNET PHY - ICSSG

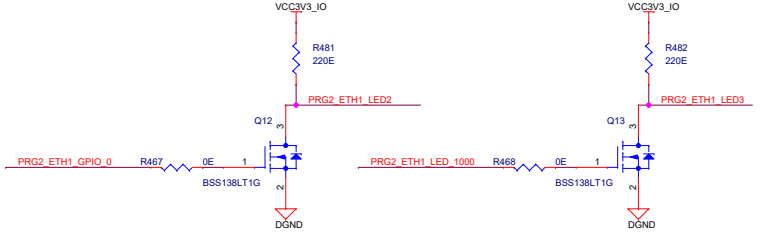
PRG2_RGMII





PRG2_ETHERNET PHY- 1 SPEED & ACTIVITY LED 's DRIVERS





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Title	RGMII ETHERNET PHY - ICSSG PRG2_PRU0		
Size			Rev
C	Variant Name = PROC062B001		A
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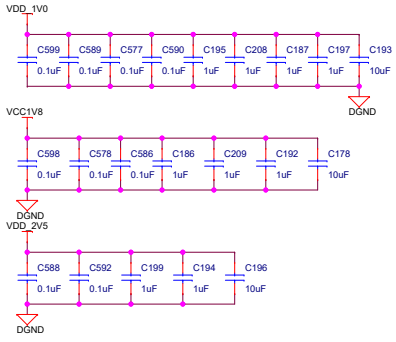
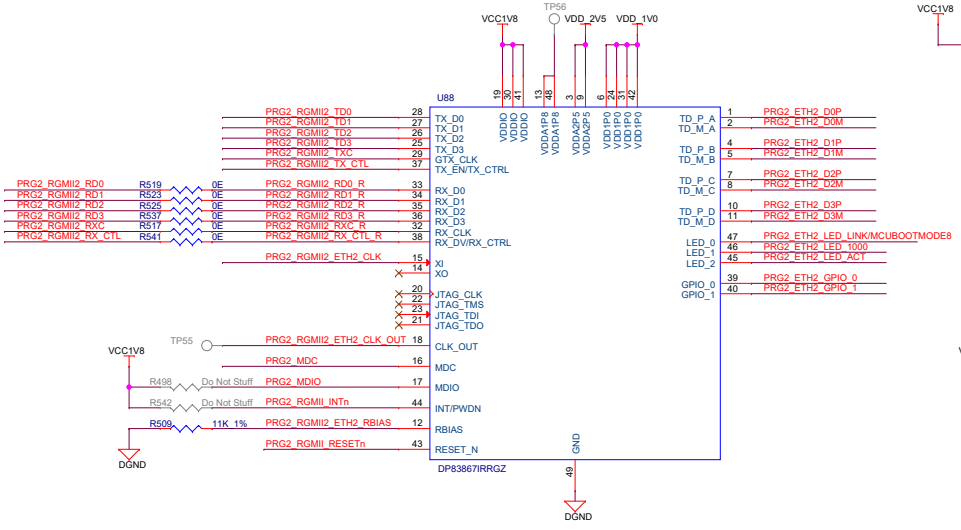
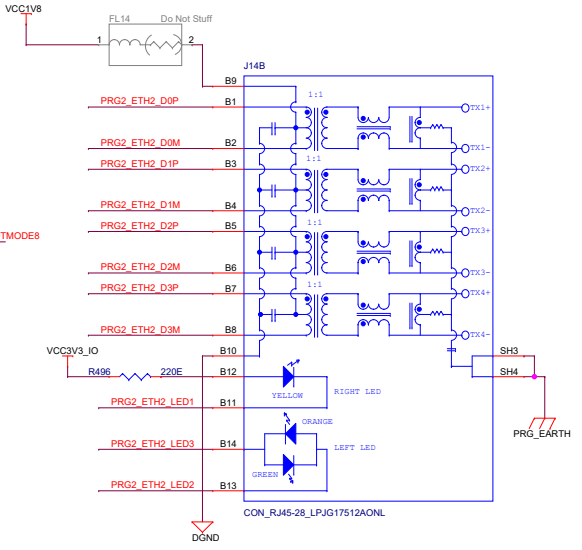
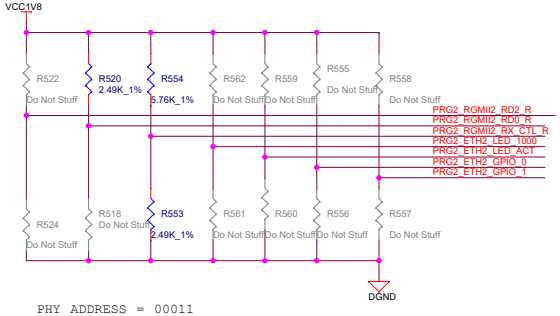
PRG2 RGMII 2



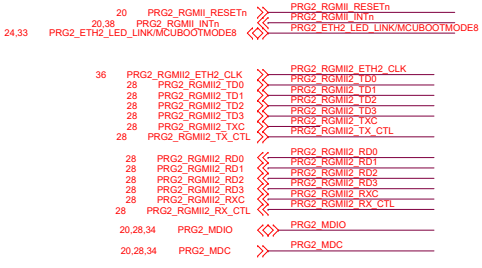




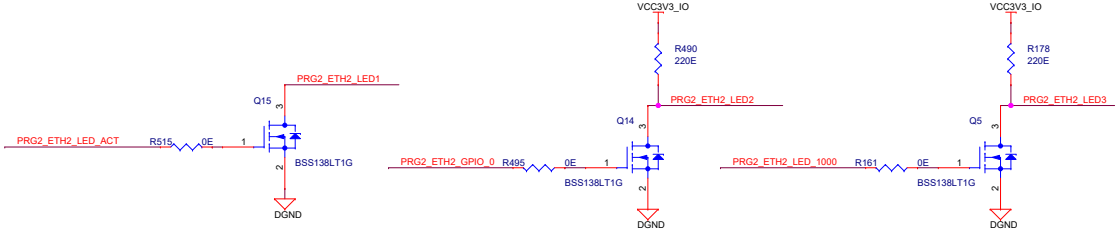
STRAPPING RESISTORS



PHY ADDRESS = 00011



PRG2_ETHERNET - 2 SPEED & ACTIVITY LED 's DRIVERS



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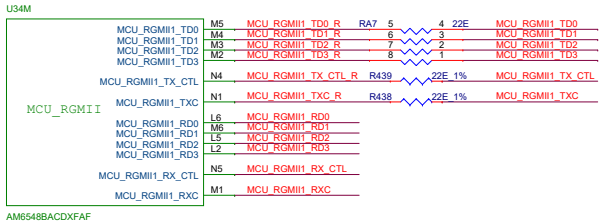
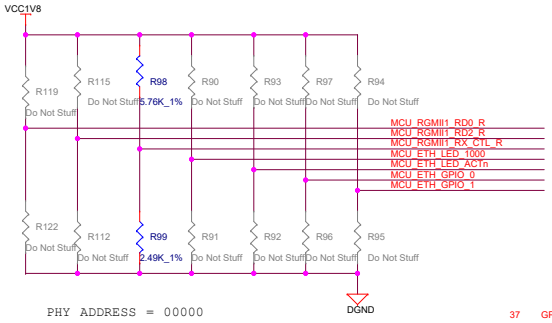
RGMII ETHERNET PHY - MCU

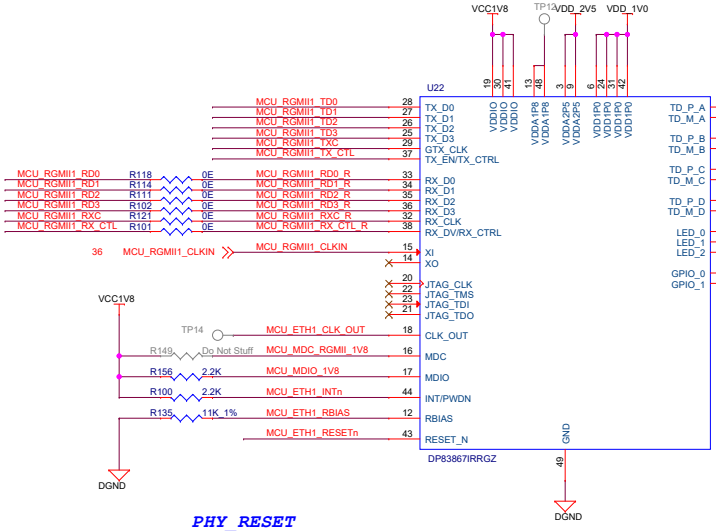
MCU_RGMII

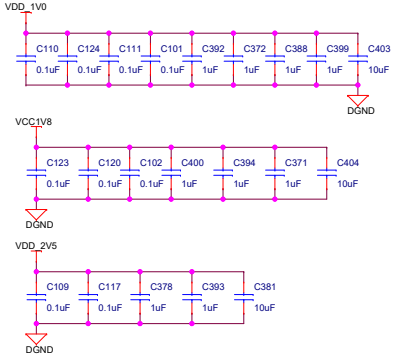


STRAPPING

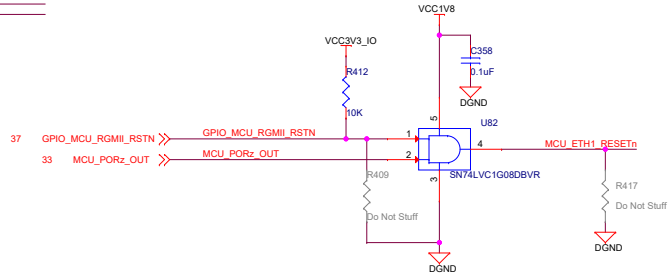


PHY ADDRESS = 00000

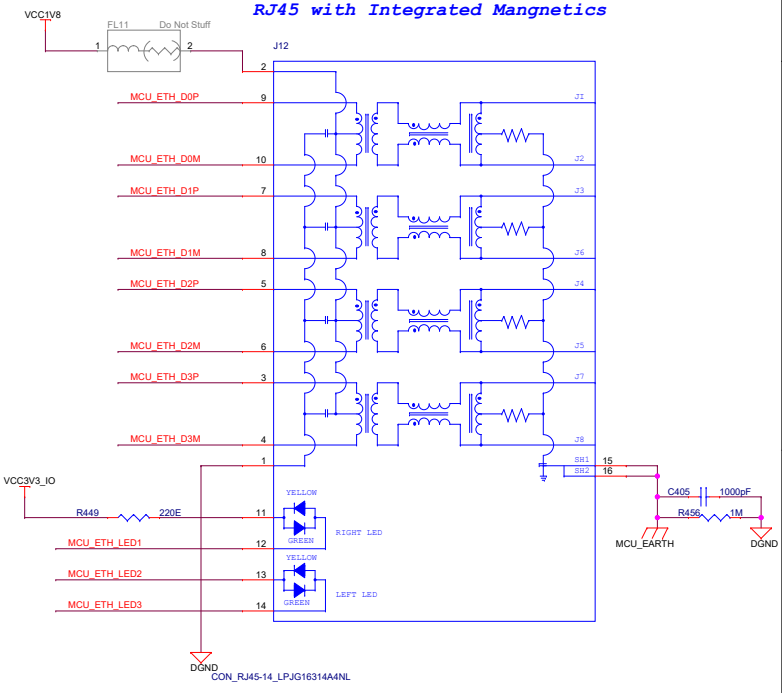




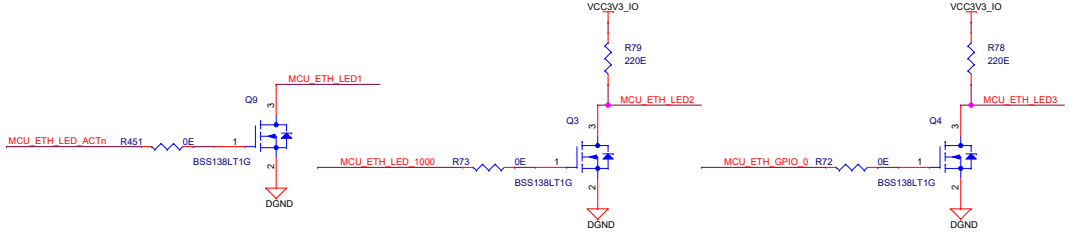
PHY_RESET



RJ45 with Integrated Mangnetics



MCU SPEED & ACTIVITY LED DRIVERS



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Title	RGMII ETHERNET PHY - MCU	
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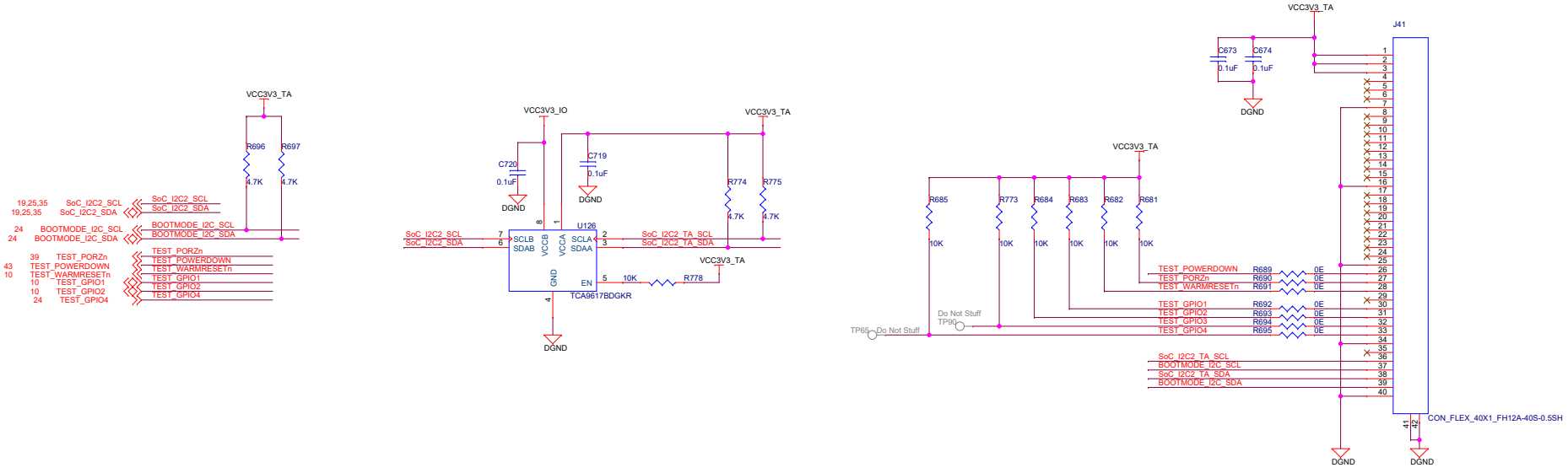
TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on WKUP_GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Used to Generate the interrupt on WKUP_GPIO0_27_INTn	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

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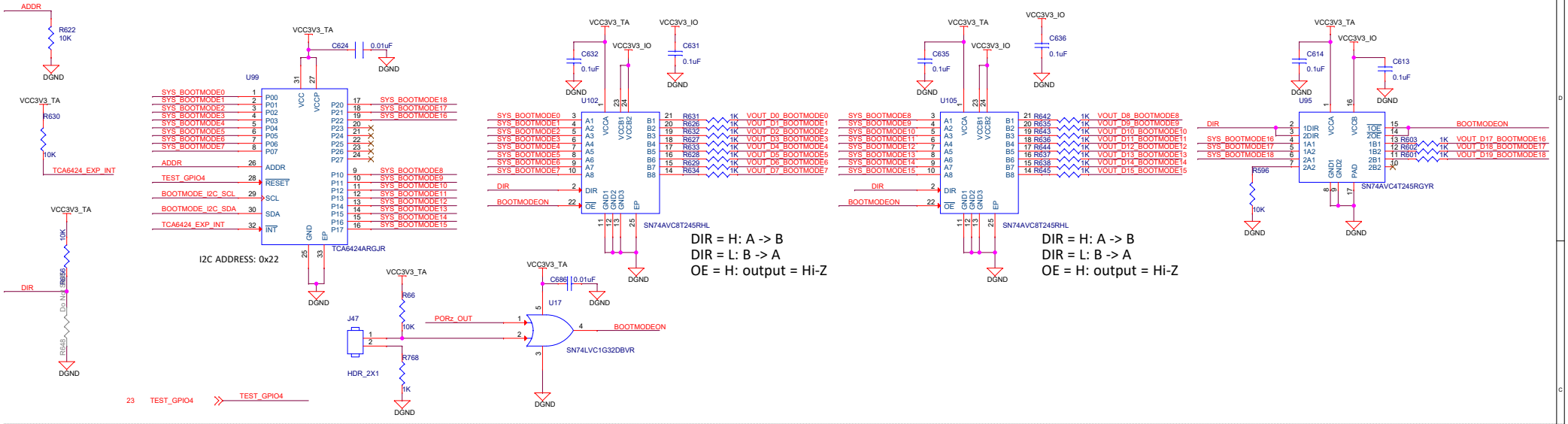
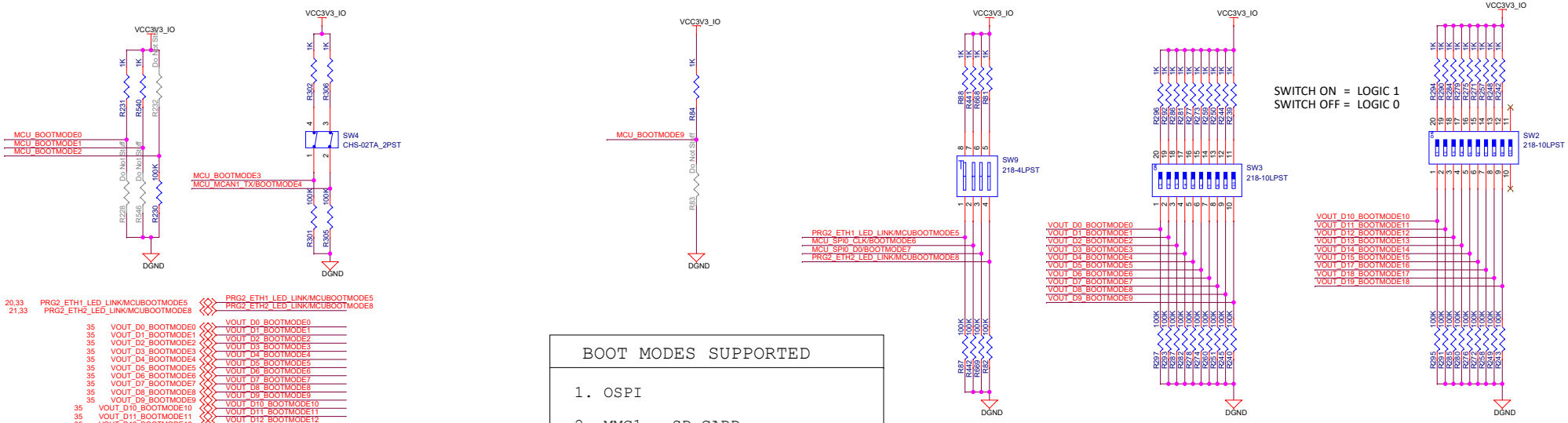
BOOT MODE BUFFER & SWITCHES





BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. PCIE (endpoint)
5. CPSW Ethernet Slave
6. USB Host
7. USB Device

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOOT MODE BUFFER & SWITCHES	
Size: C	Variant Name = PROC062B001	Rev: A
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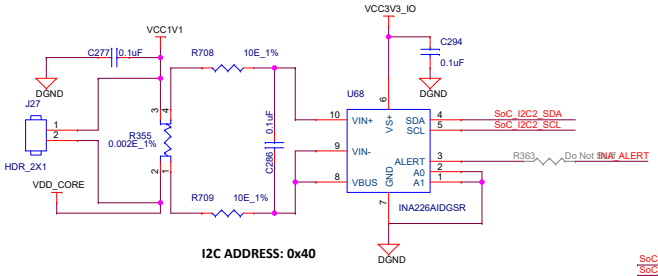
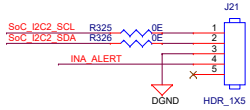
CURRENT MONITORING DEVICES

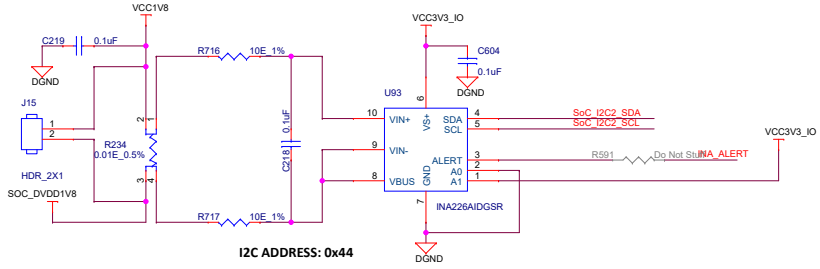
VDD_CORE



I2C ADDRESS: 0x40

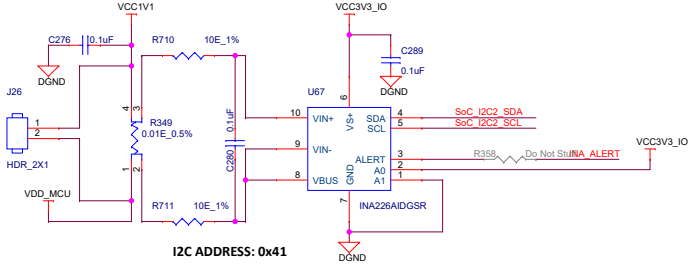


SoC_DVDD1V8



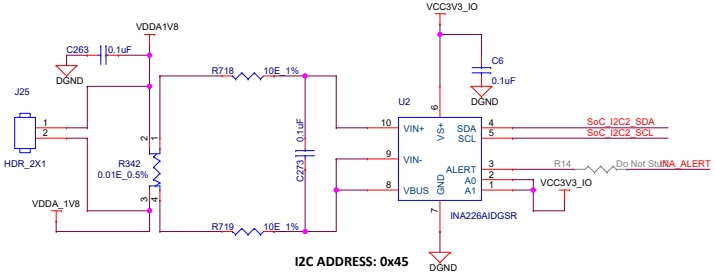
I2C ADDRESS: 0x44

VDD_MCU



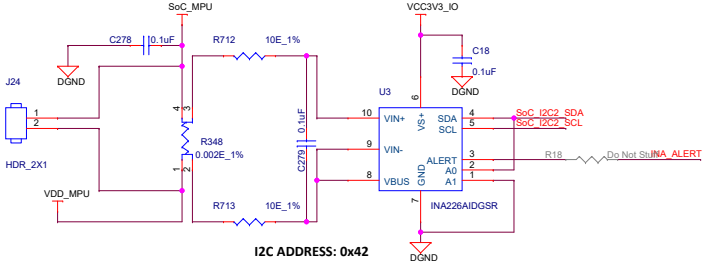
I2C ADDRESS: 0x41

SoC_AVDD1V8



I2C ADDRESS: 0x45

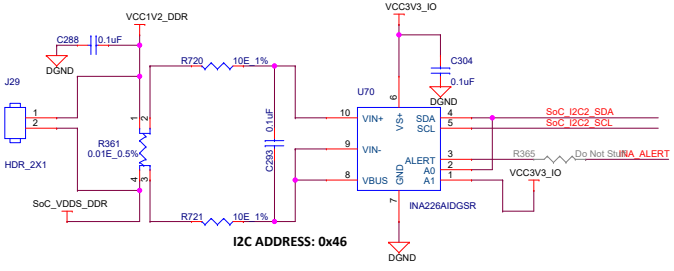
VDD_MPU



I2C ADDRESS: 0x42

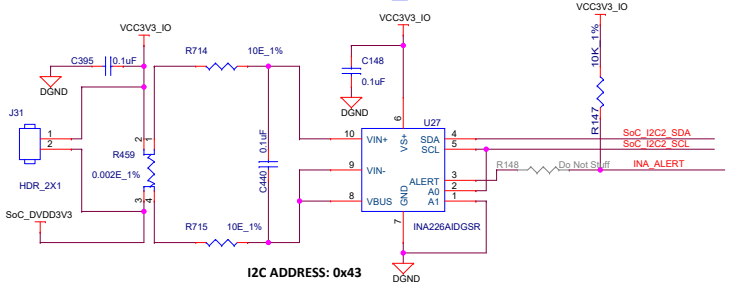
INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC1V0	VDD_CORE	40
VCC1V0	VDD_MCU	41
SoC_MPU	VDD_MPU	42
VCC3V3_IO	SoC_DVDD3V3	43
VCC1V8	SoC_DVDD1V8	44
VDDA1V8	SoC_AVDD1V8	45
VCC1V2_DDR	SoC_VDDS_DDR	46
VCC1V2_DDR	VDD_DDR	47

SoC_VDDS_DDR



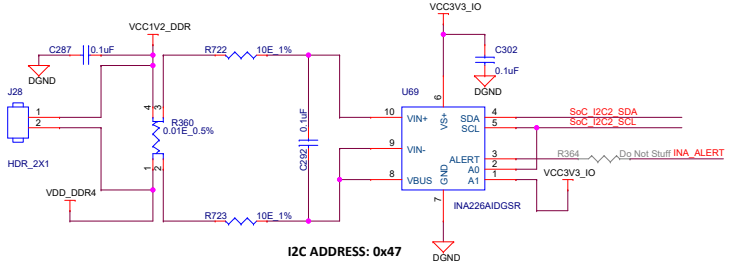
I2C ADDRESS: 0x46

SoC_DVDD3V3



I2C ADDRESS: 0x43

VDD_DDR



I2C ADDRESS: 0x47

Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES	
Size C	Variant Name = PROC062B001	Rev A
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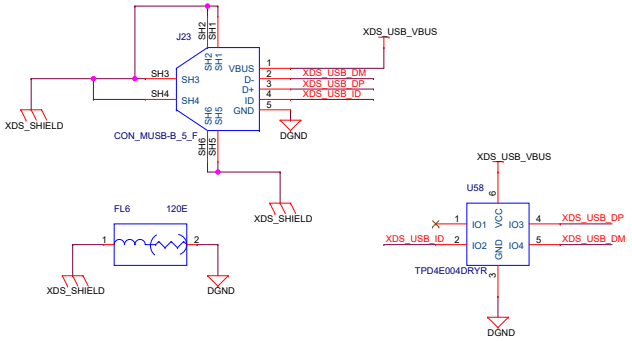
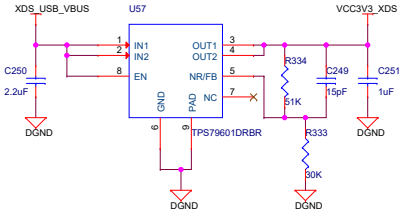
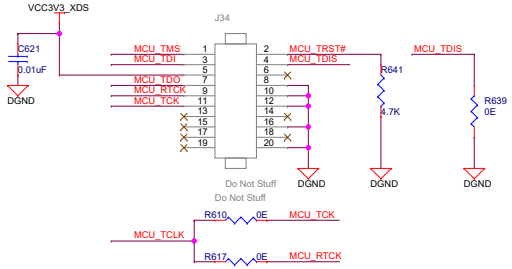
XDS110 POWER

USB Connector

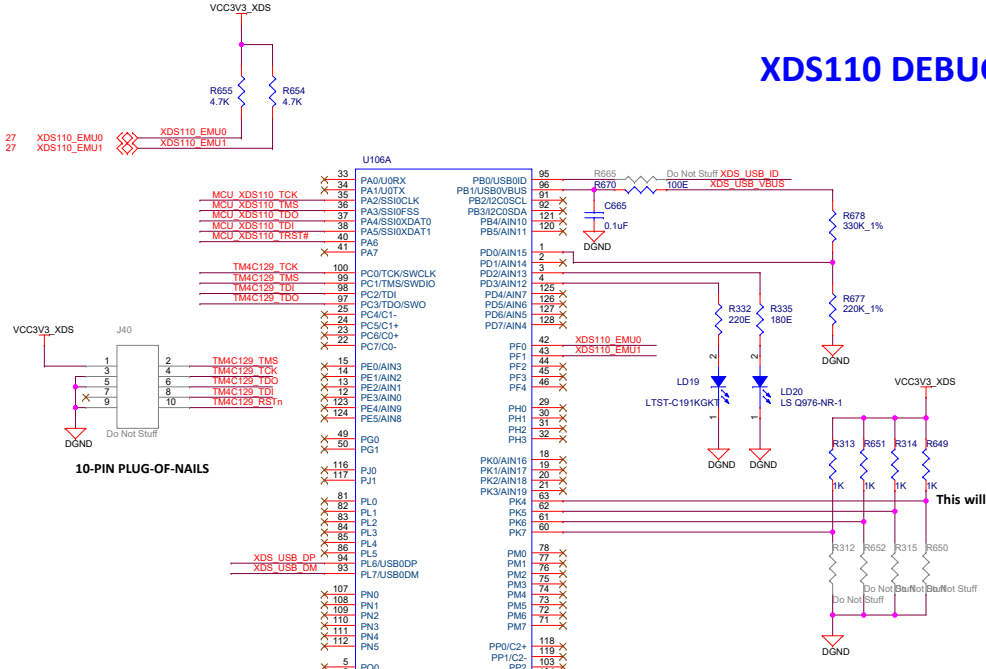


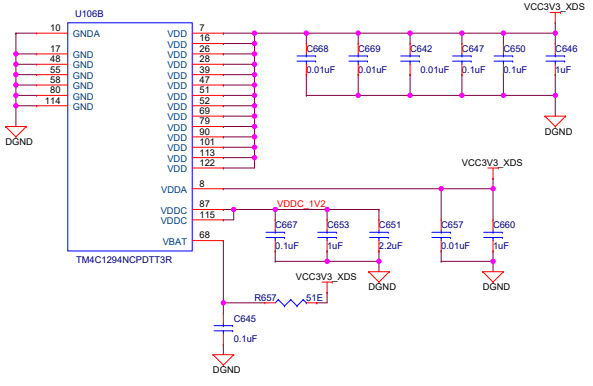


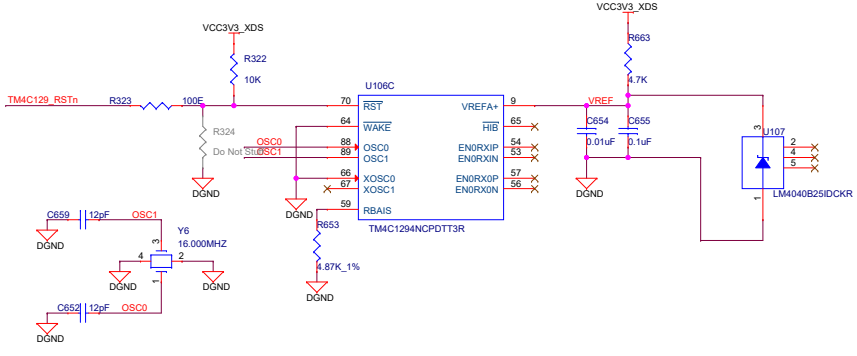
CTI 20 Pin Header external probe

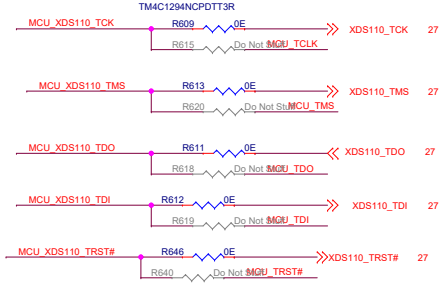


XDS110 DEBUGGER









0- Ohm Res MUX between XDS110 JTAG and MCU cTI 20 pin connector.
-For XDS110 JTAG R609,R613,R611,R612 and R646 Should be installed and R615,R620,R618,R619 and R640 Should be DNI'd.
-For MCU cTI 20 pin , R615,R620,R618,R619 and R640 Should be Installed and R609,R613,R611,R612 and R646 Should be DNI'd.

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Title	XDS110 DEBUGGER	
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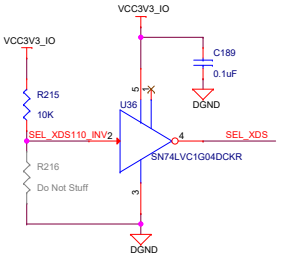
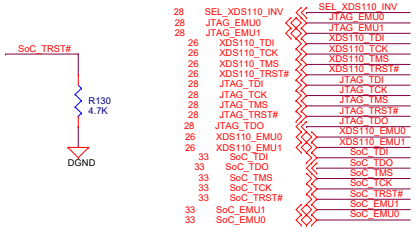
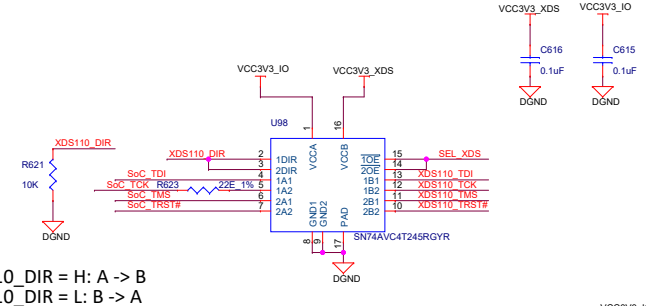
JTAG BUFFER

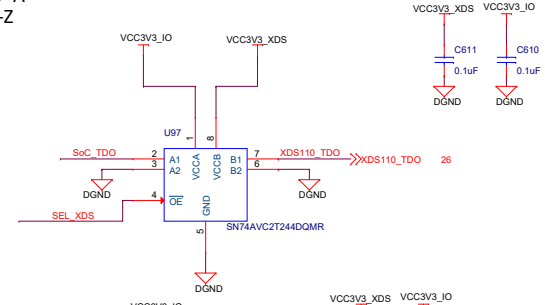


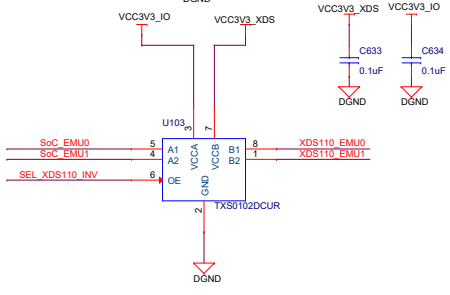


BUFFER XDS110

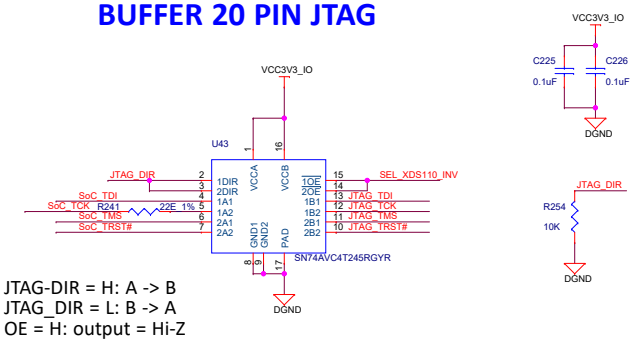


XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

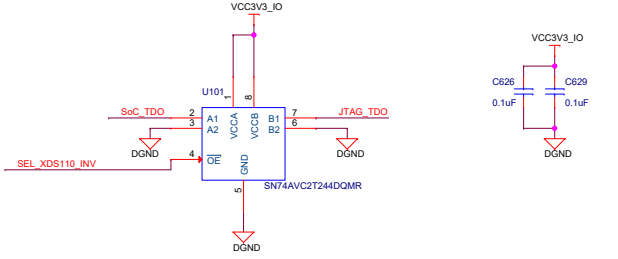


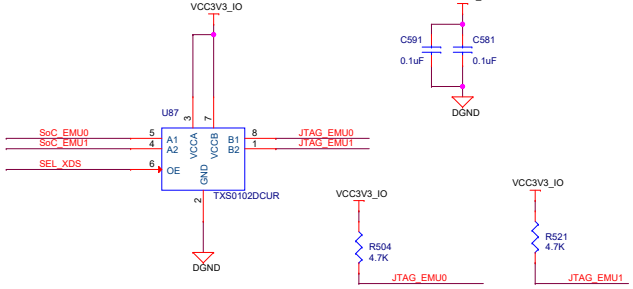


BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B
JTAG_DIR = L: B -> A
OE = H: output = Hi-Z





Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size	Variant Name = PROC062B001	Rev
C		A
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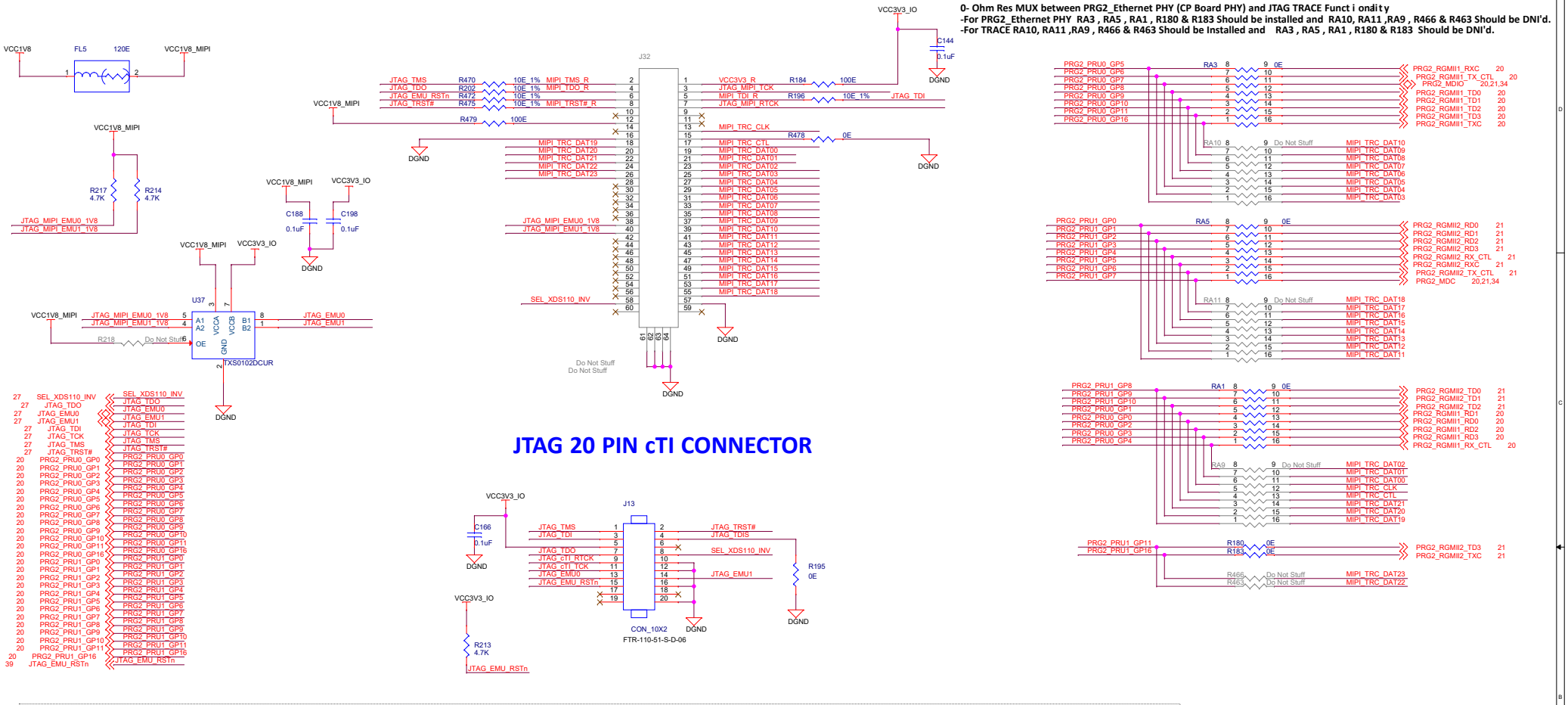
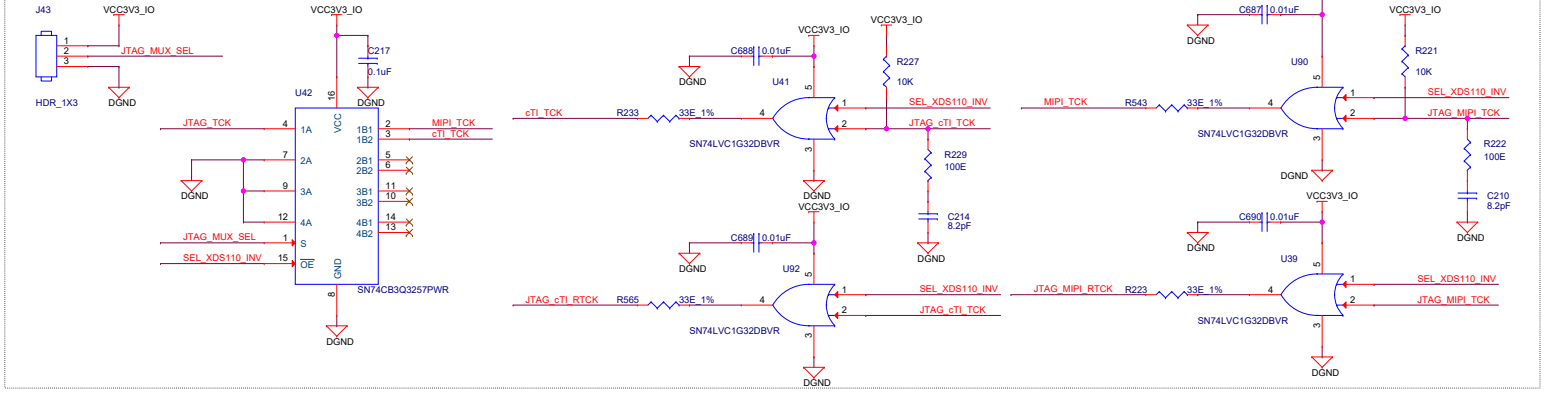
MIPI 60 PIN CONNECTOR

0- Ohm Res MUX between PRG2_Ethernet PHY (CP Board PHY) and JTAG TRACE Funct i onal ity
-For PRG2_Ethernet PHY RA3 , RA5 , RA1 , R180 & R183 Should be installed and RA10, RA11 ,RA9 , R466 & R463 Should be DNI'd.
-For TRACE RA10, RA11 ,RA9 , R466 & R463 Should be Installed and RA3 , RA5 , RA1 , R180 & R183 Should be DNI'd.



JTAG 20 PIN cTI CONNECTOR

JTAG CLOCK BUFFER



Designed for TI by Mistral Solutions Pvt Ltd

Title	MIPI 60 PIN CONNECTOR	
Size C	Variant Name = PROC062B001	Rev A
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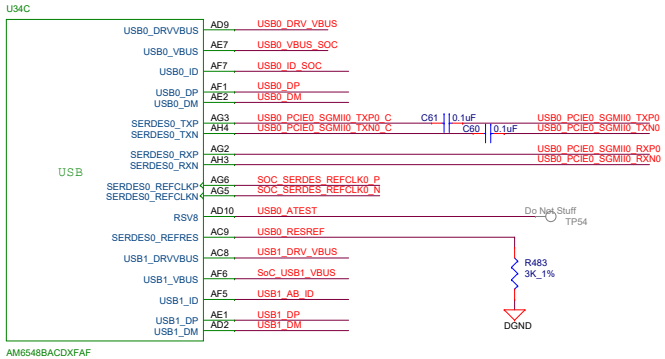
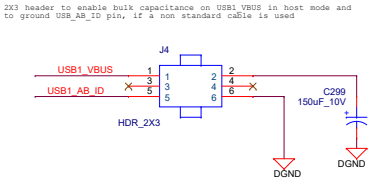
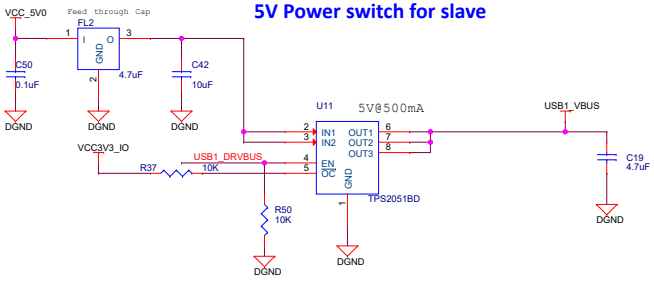
USB 2.0 INTERFACE

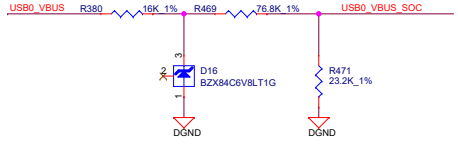




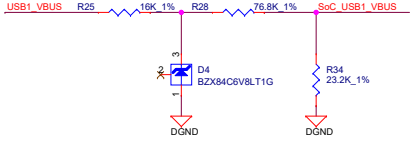
5V Power switch for slave

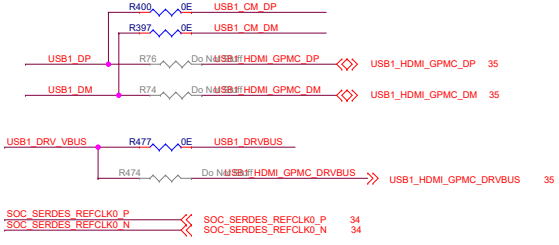


Resistor divider on SOC_VBUS

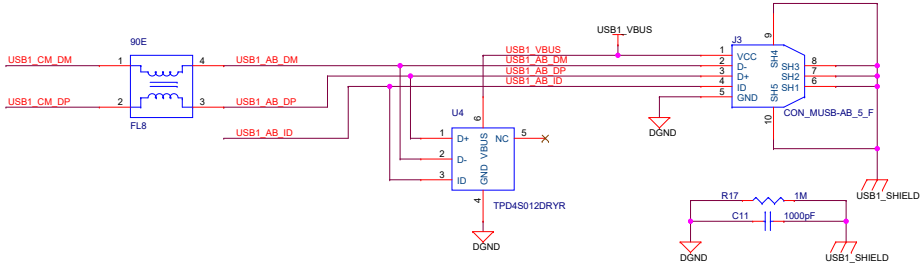


Resistor divider on SOC_VBUS





Micro USB 2.0 AB Connector



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Title	USB 2.0 INTERFACE	
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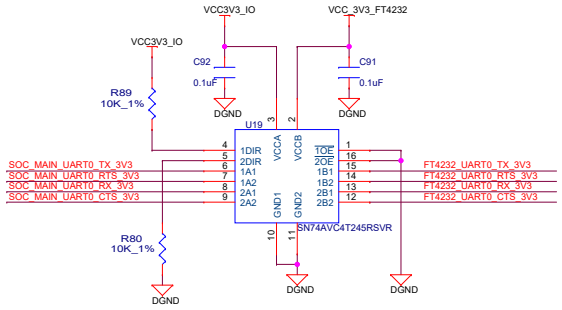
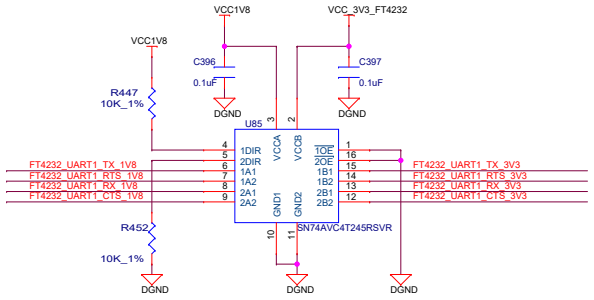
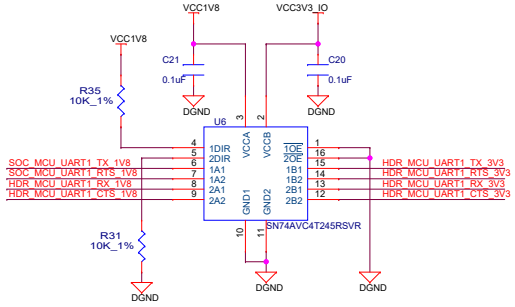
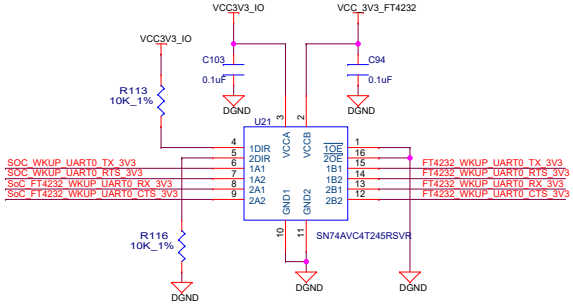
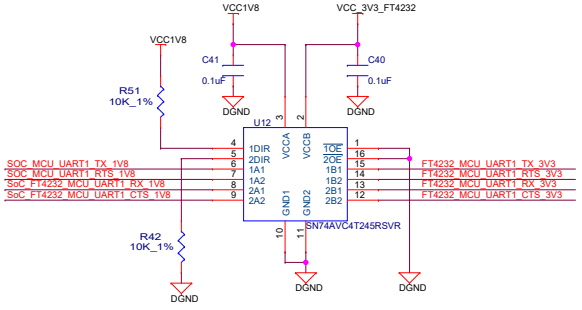
FT4232 LEVEL TRANSLATOR

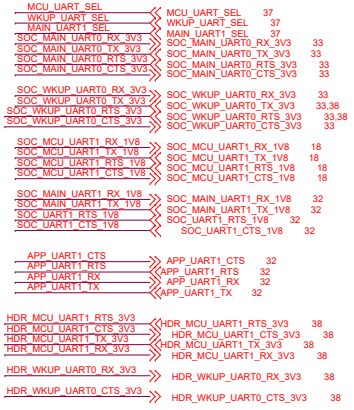




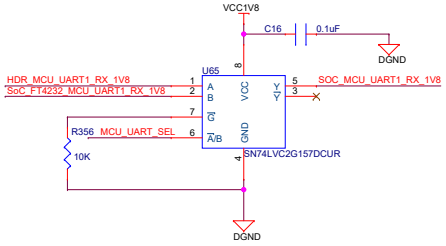


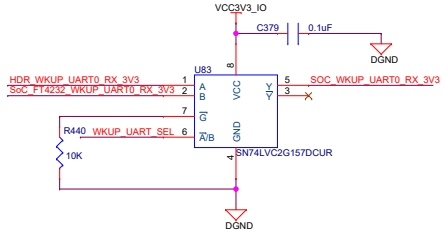


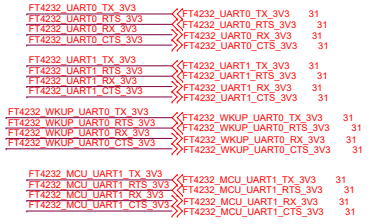


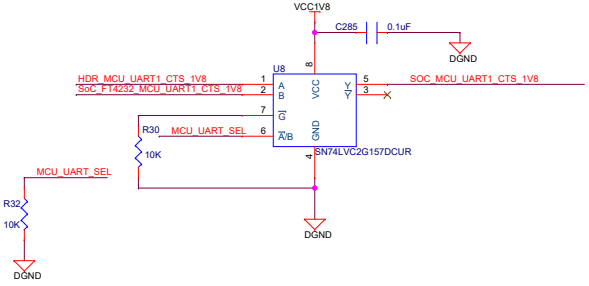


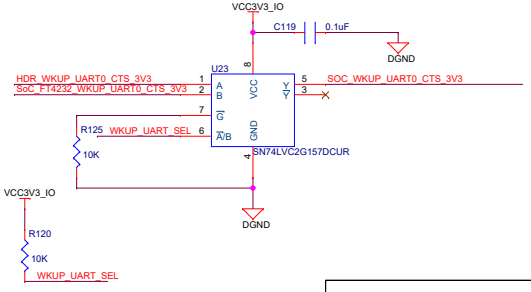
2:1 MUX

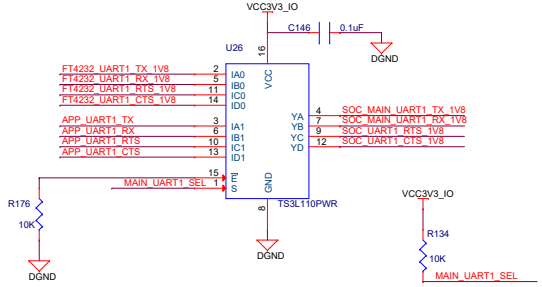












Designed for TI by Mistral Solutions Pvt Ltd

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Size	Variant Name = PROC062B001	Rev
C		A
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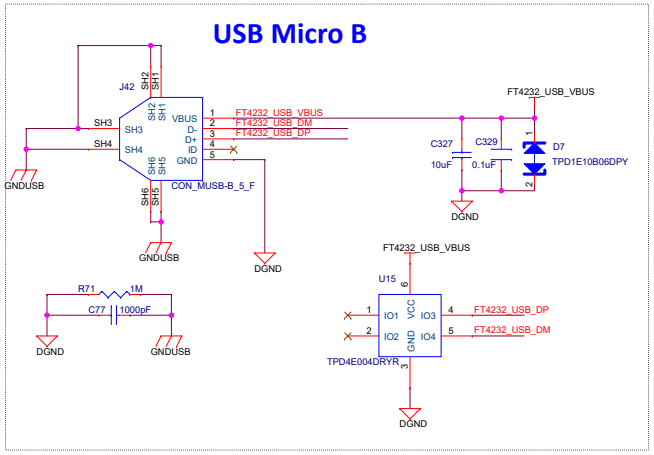
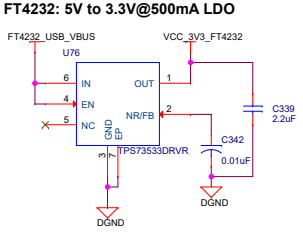
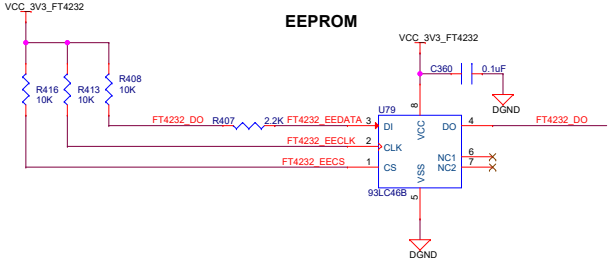
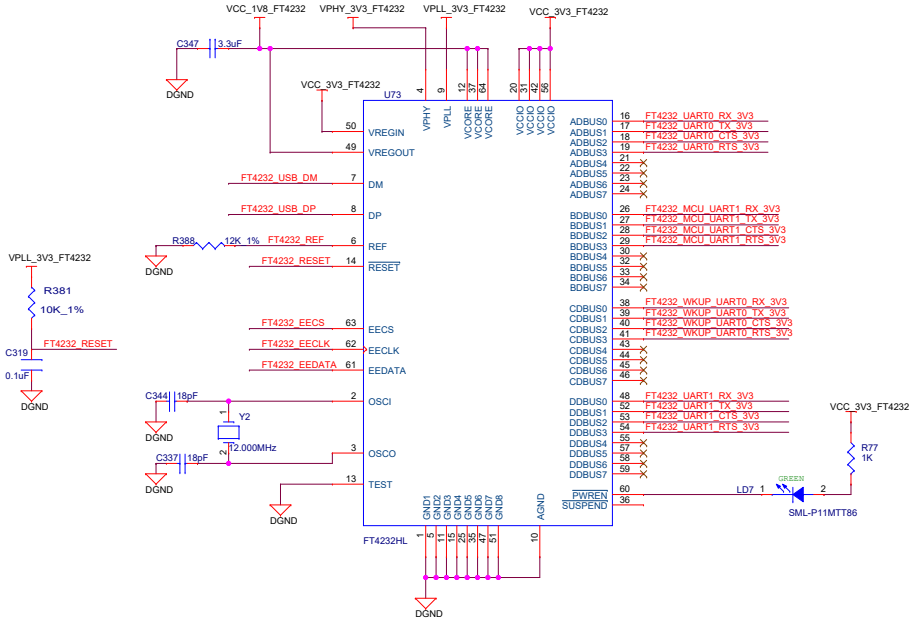
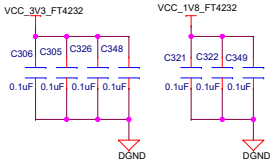
FT4232 UART

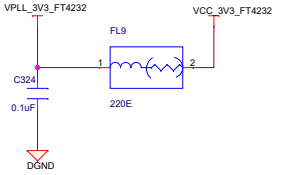


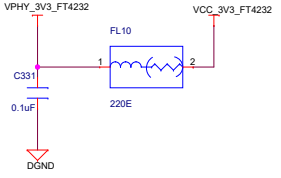


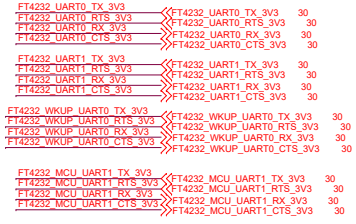












Designed for TI by Mistral Solutions Pvt Ltd

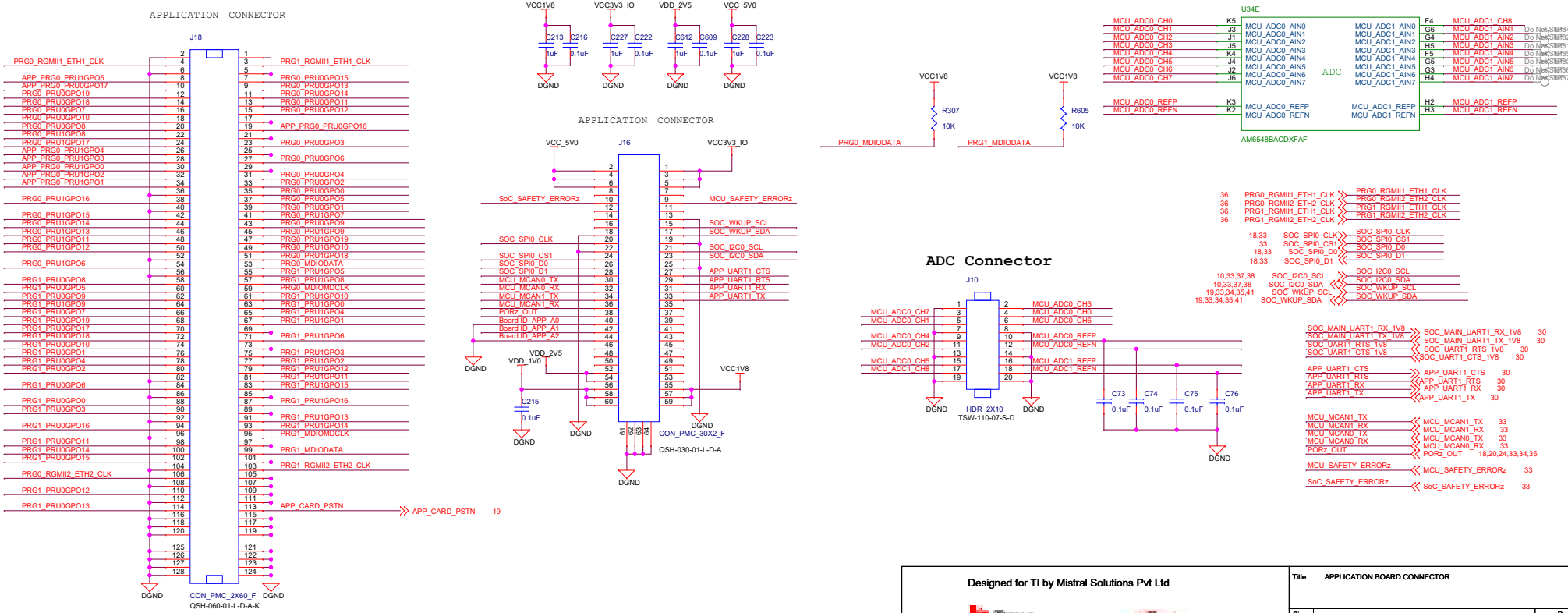
Title	FT4232 UART TO USB BRIDGE	
Size: C	Variant Name = PROC062B001	Rev: A
Date: Thursday, July 01, 2021	Sheet 31 of 44	

APPLICATION BOARD INTERFACE

0- Ohm Res MUX between APPLICATION Board connector and HDMI / GPMC Daughter card.
-For APPLICATION Board connector R570 , R589 ,R576 ,R580 ,R578, R574 ,R572 & R587 Should be installed and R569, R590, R575, R579 ,R577 , R573, R571 & R588 Should be DNI'd.
-For HDMI / GPMC Daughter card R569, R590, R575, R579 ,R577 , R573, R571 & R588 Should be Installed and R570 , R589 ,R576 ,R580 ,R578, R574 ,R572 & R587 Should be DNI'd.

Customer Note – See Users Guide for more information on DNI resistor alternatives

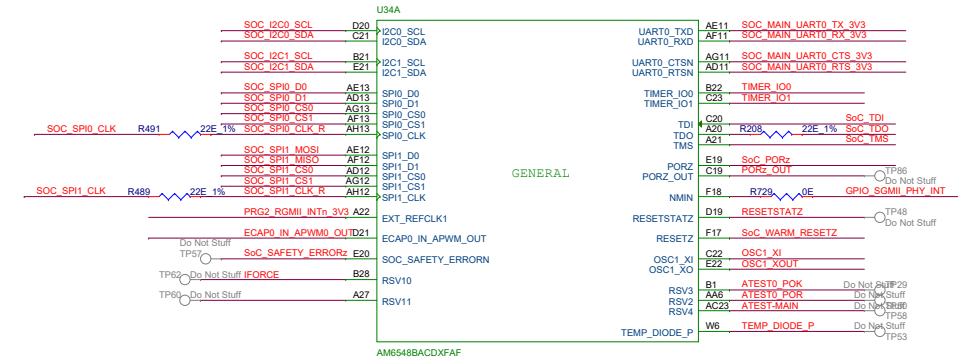
APPLICATION BOARD CONNECTORS

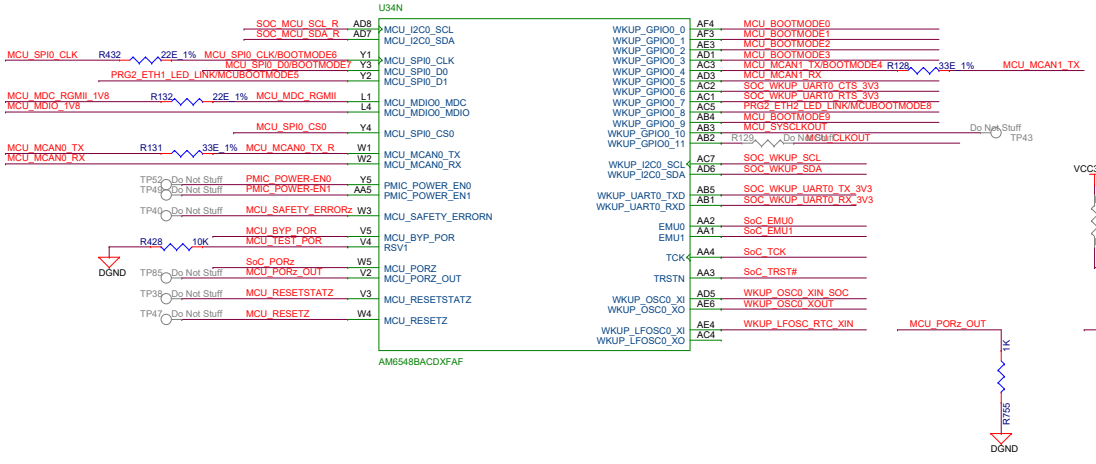


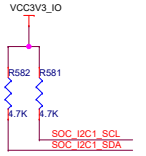
Designed for TI by Mistral Solutions Pvt Ltd

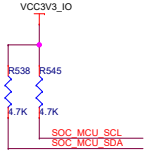
Title	APPLICATION BOARD CONNECTOR	
Size	Variant Name = PROC062B001	Rev
C		A
Date: Thursday, July 01, 2021	Sheet 32 of 44	

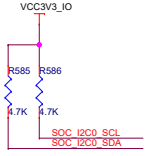
GENERAL & MCU_GENERAL

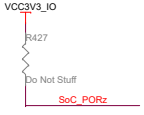


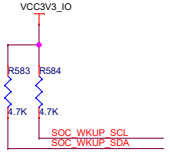


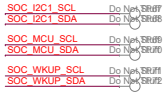




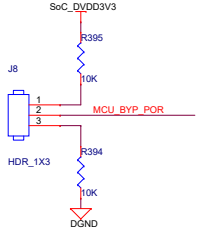




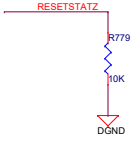


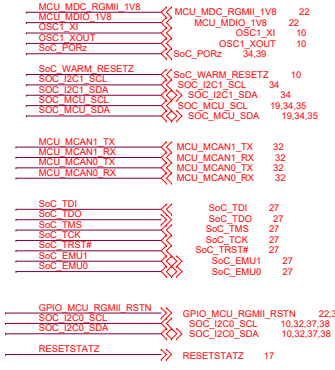


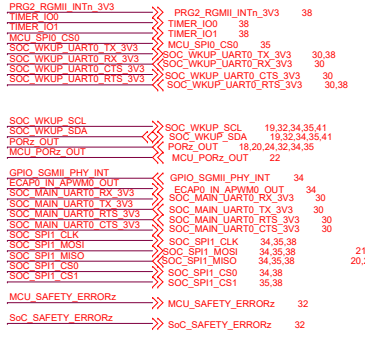
Jumper to select Internal PORz & External PORz

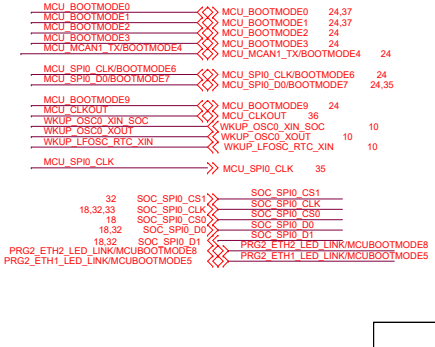


To Disable the Internal PORz ,
Connect the Jumper beween Pin no 1 & 2 of J8.
To Enable the Internal PORz,
Connect the Jumper between Pin no 2 & 3 of J8

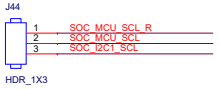


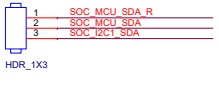






Jumper option to connect the peripherals connected on MCU_I2C to SoC I2C1

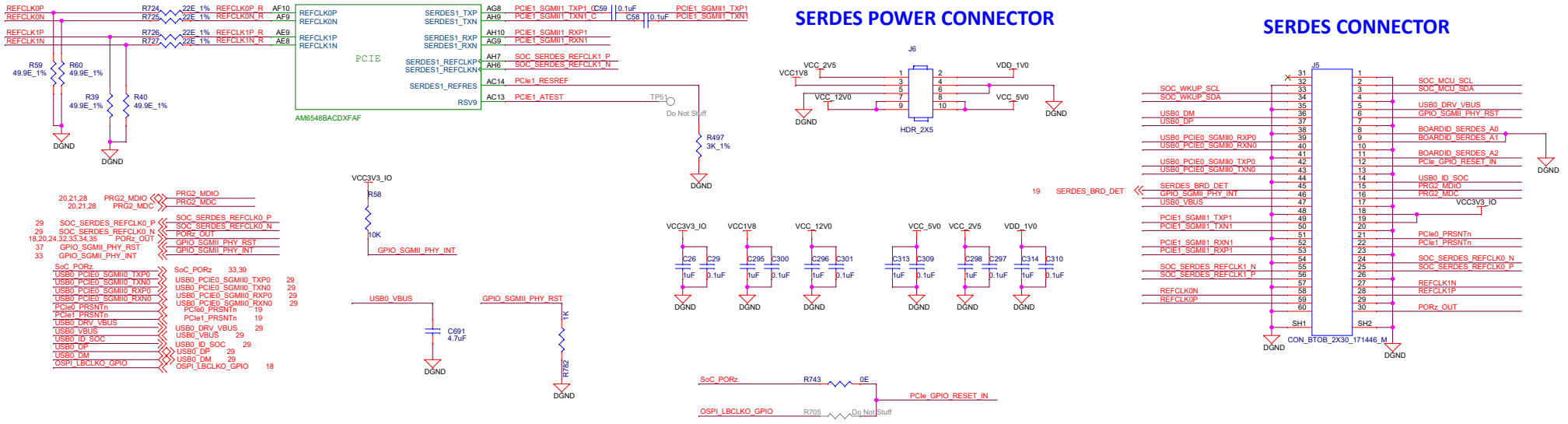




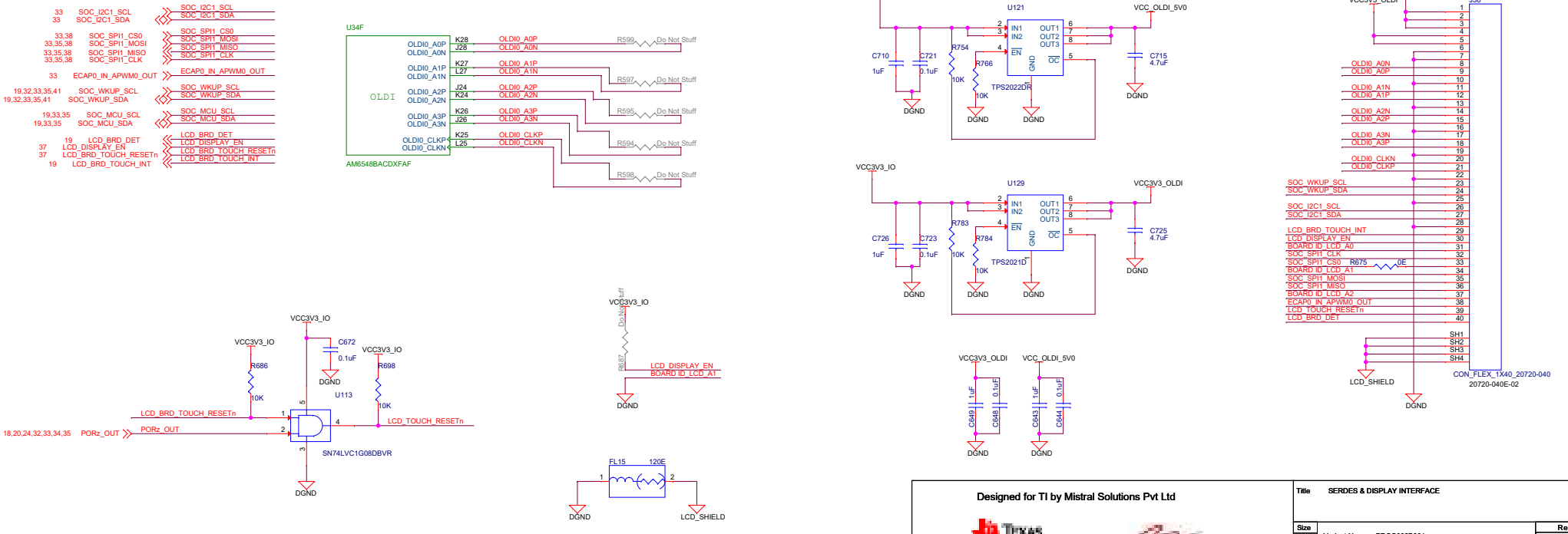
Designed for TI by Mistral Solutions Pvt Ltd

Title	SOC_GENERAL & MCU GENERAL		
Size			Rev
C	Variant Name = PROC062B001		A
Date:	Thursday, July 01, 2021	Sheet	33 of 44

SERDES INTERFACE



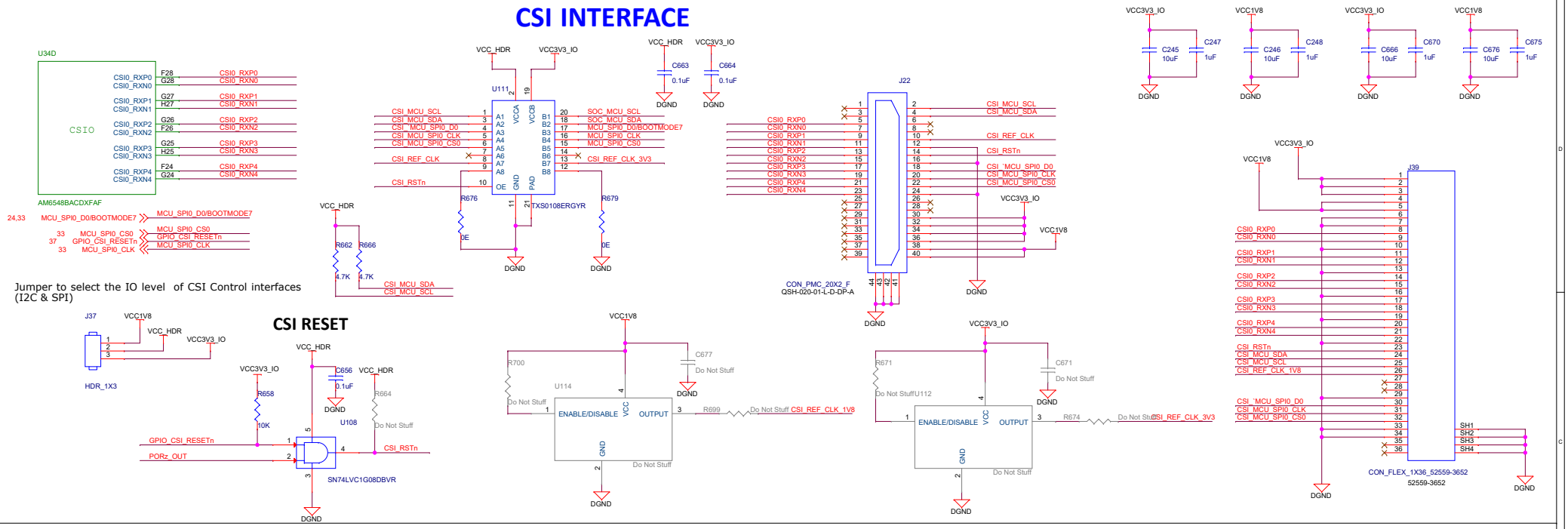
OLDI INTERFACE



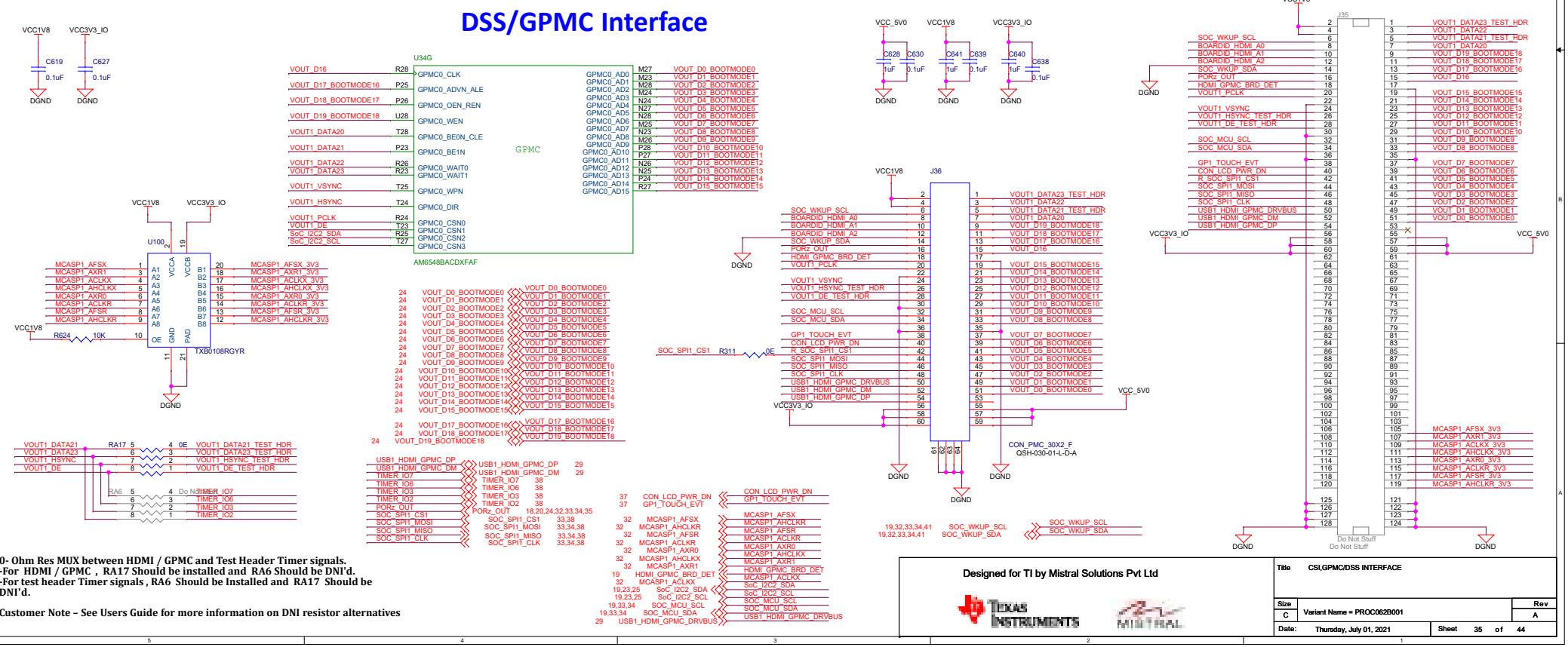
Designed for TI by Mistral Solutions Pvt Ltd

Title	SERDES & DISPLAY INTERFACE		
Size	Variant Name = PROC062B001		Rev
C			A
Date:	Thursday, July 01, 2021	Sheet	34 of 44

CSI INTERFACE



DSS/GPMC Interface



0- Ohm Res MUX between HDMI / GPMC and Test Header Timer signals.
-For HDMI / GPMC , RA17 Should be installed and RA6 Should be DNI'd.
-For test header Timer signals , RA6 Should be Installed and RA17 Should be DNI'd.

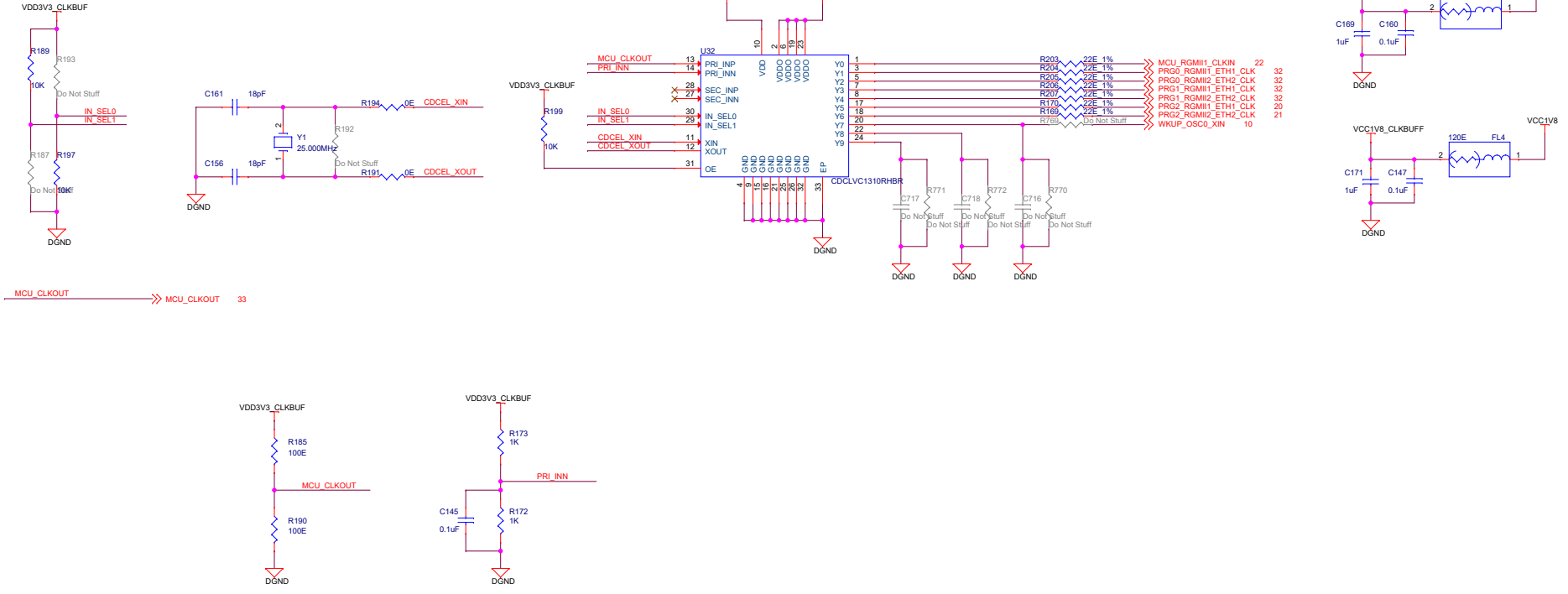
Customer Note – See Users Guide for more information on DNI resistor alternatives

Designed for TI by Mistral Solutions Pvt Ltd

Title	CSI,GPMC/DSS INTERFACE	
Size C	Variant Name = PROC062B001	Rev A
Date: Thursday, July 01, 2021	Sheet 35 of 44	

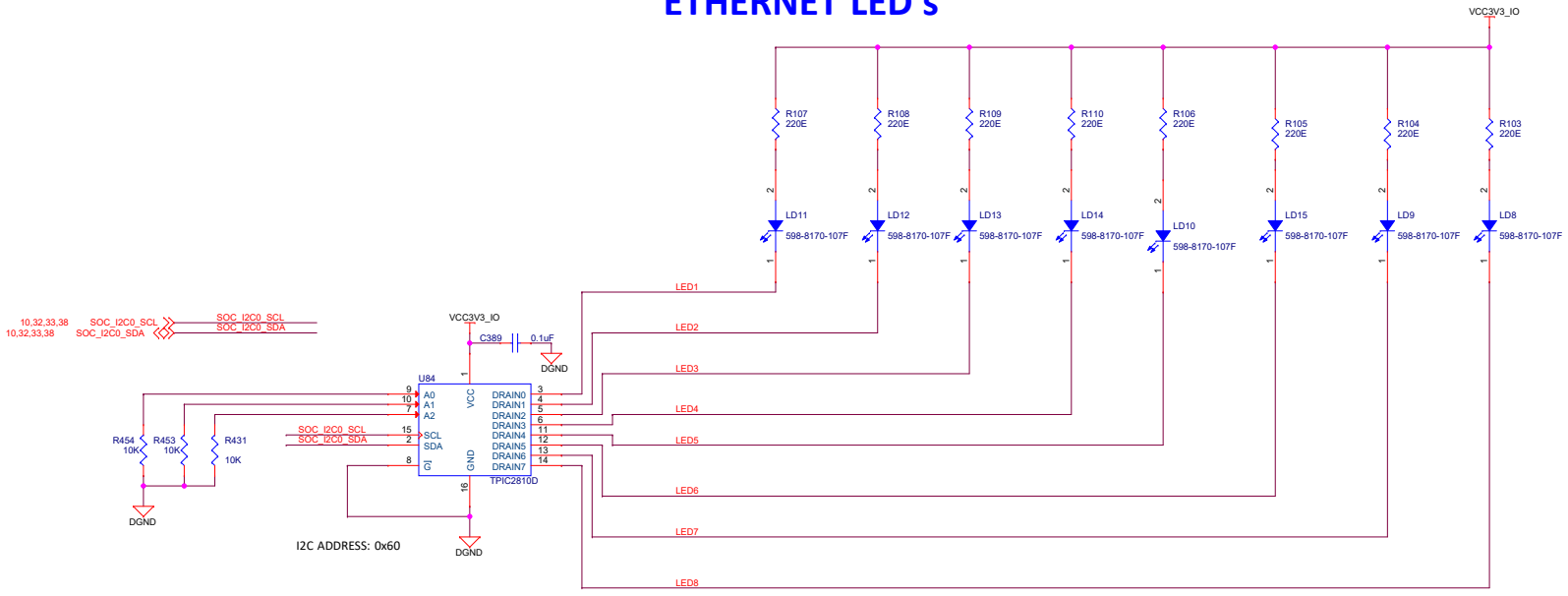
ETHERNET PHY CLOCK BUFFER

REFERENCE INPUT SELECTION

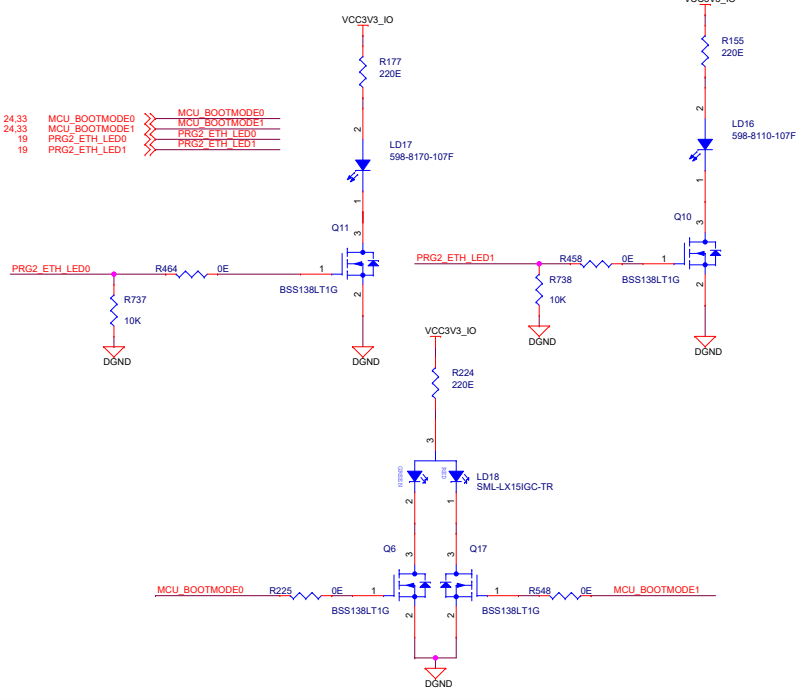


Designed for TI by Mistral Solutions Pvt Ltd	Title: ETHERNET PHY CLOCK GENERATOR	
	Size: C — Variant Name = PROC062B001	Rev: A
	Date: Thursday, July 01, 2021	Sheet 36 of 44

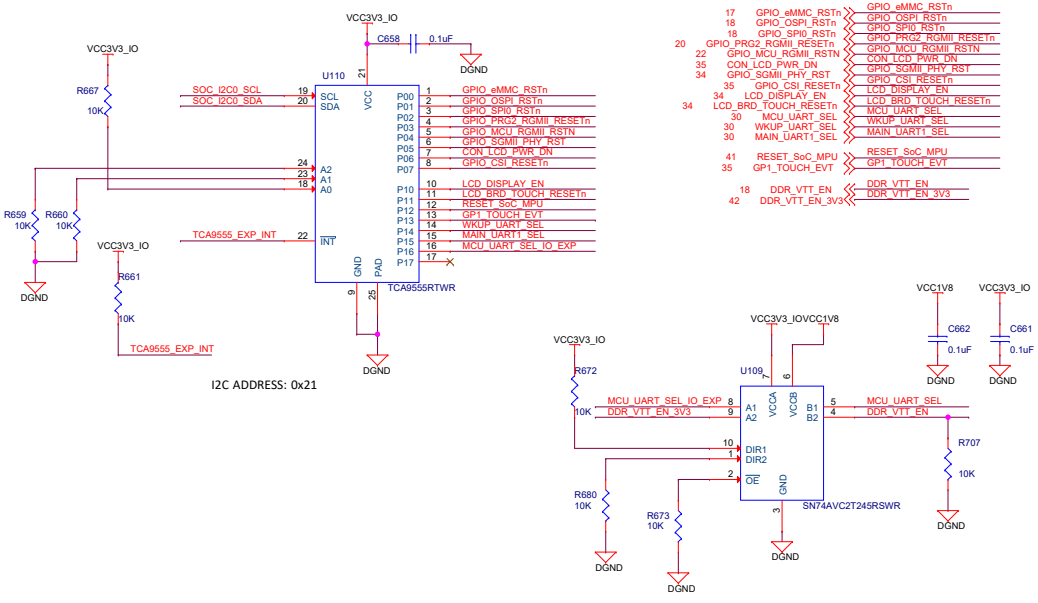
ETHERNET LED's



PRG2 ETHERNET LED's



I2C IO Expander

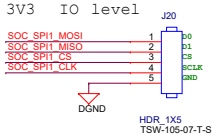


Designed for TI by Mistral Solutions Pvt Ltd

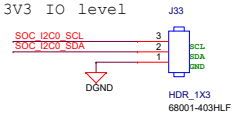
Title	ETHERNET LEDs		
Size			Rev
C	Variant Name = PROC062B001		A
Date:	Thursday, July 01, 2021	Sheet 37 of 44	

TEST HEADER

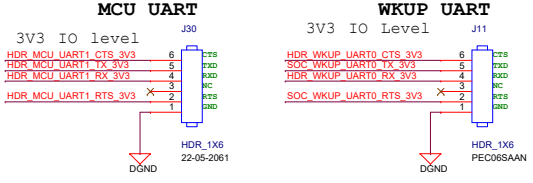
SPI TEST HEADER



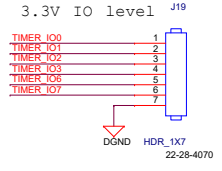
I2C TEST HEADER

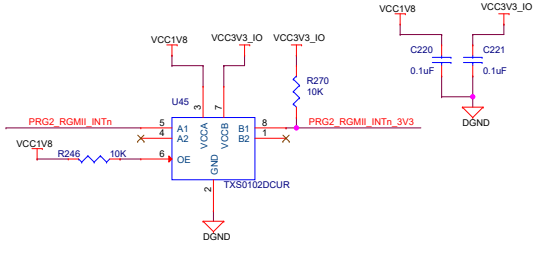


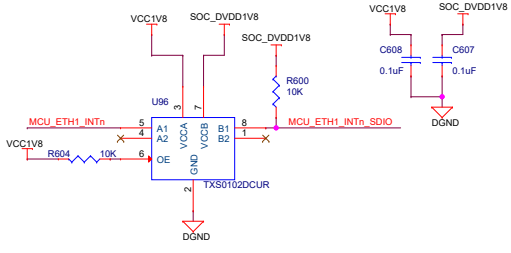
UART TEST HEADER



TIMER SIGNALS TEST HEADER







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Title	TEST HEADER	
Size C	Variant Name = PROC062B001	Rev A
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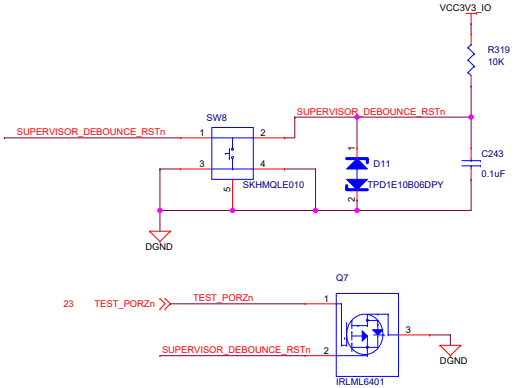
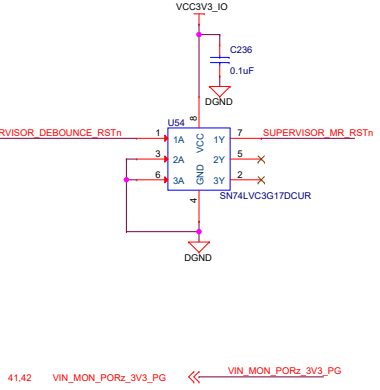
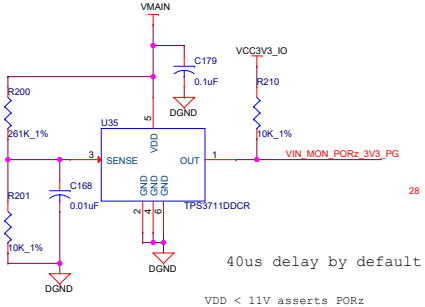
VOLTAGE SUPERVISOR

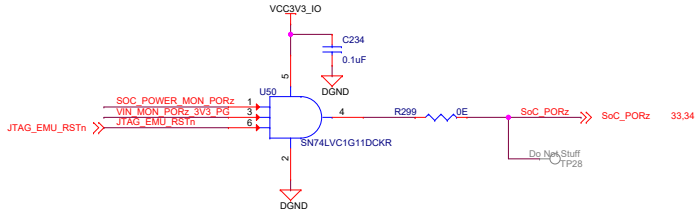
DEBOUNCE CIRCUIT



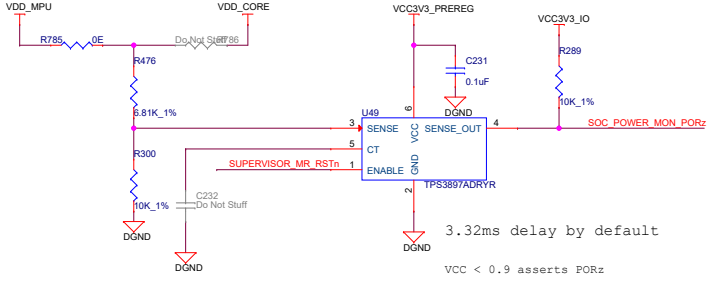


Under Voltage Monitor (VMAIN)





Under Voltage Monitor (VDD_MPU / VDD_CORE)

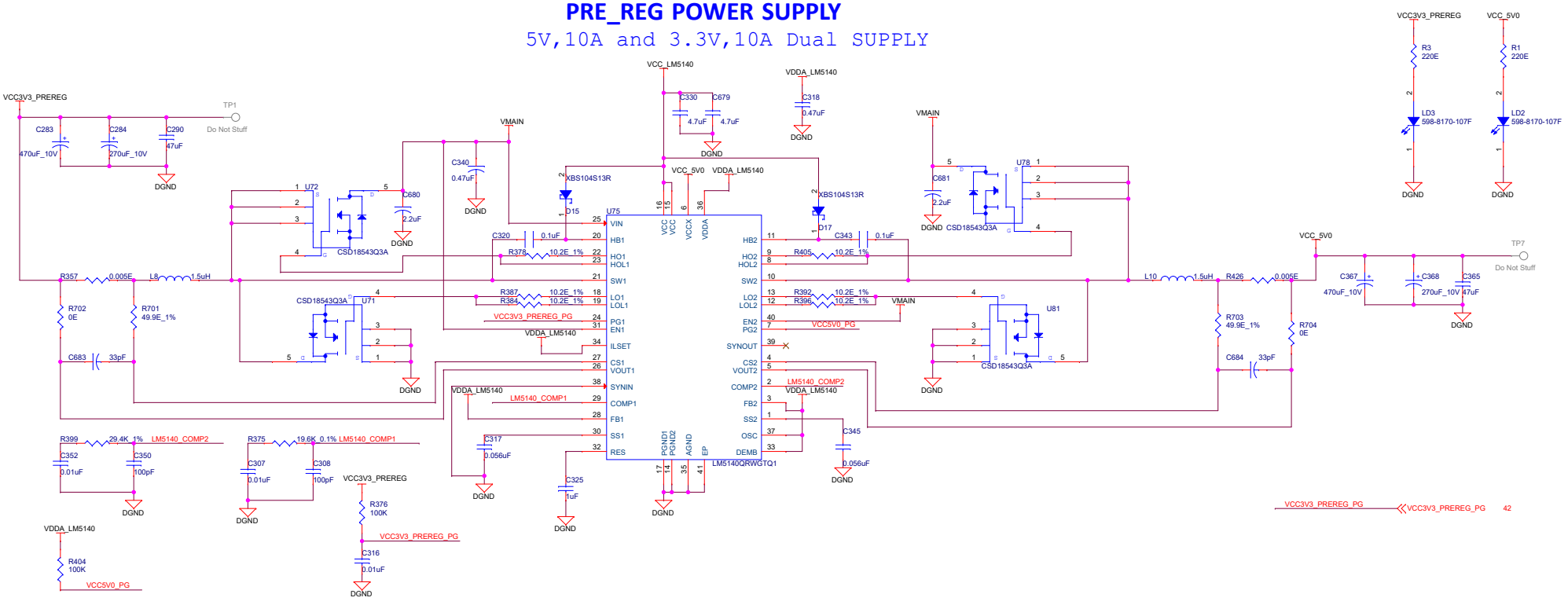


Designed for TI by Mistral Solutions Pvt Ltd

Title	VOLTAGE SUPERVISOR & WKUP LEDs	
Size	Variant Name = PROC062B001	Rev
C		A
Date: Thursday, July 01, 2021	Sheet 39 of 44	

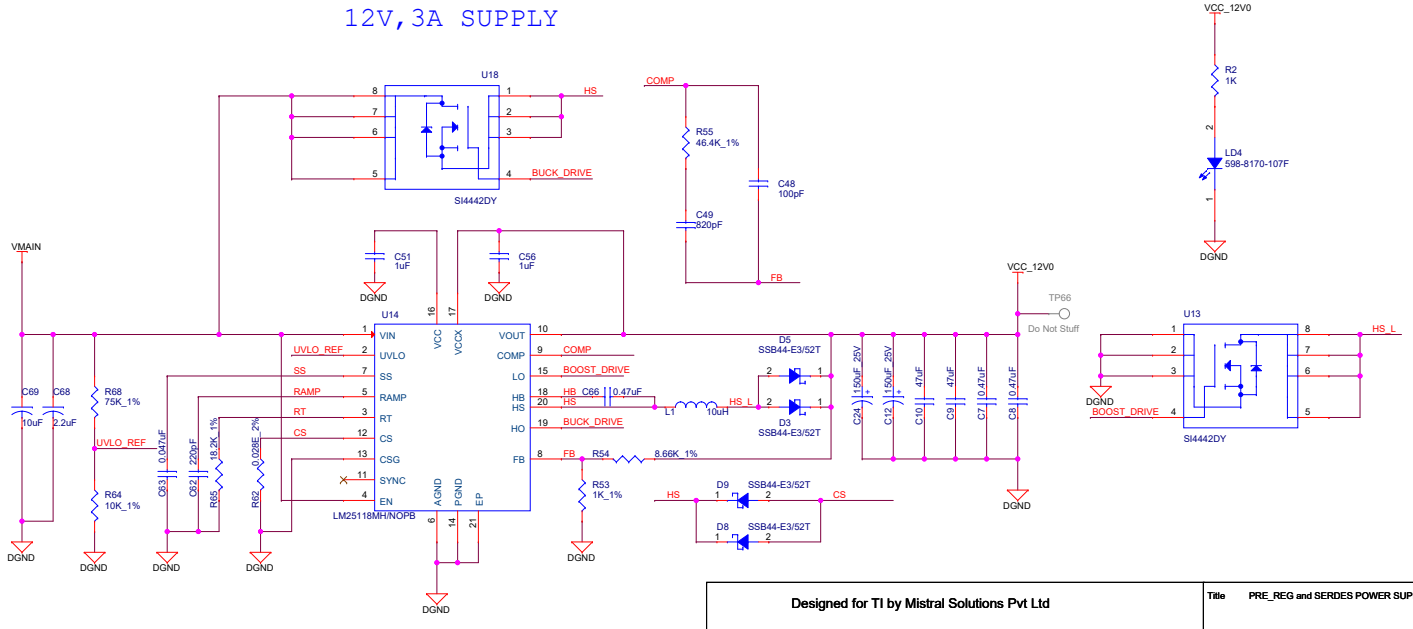
PRE_REG POWER SUPPLY

5V,10A and 3.3V,10A Dual SUPPLY



SERDES POWER SUPPLY

12V,3A SUPPLY



Designed for TI by Mistral Solutions Pvt Ltd

Title	PRE_REG and SERDES POWER SUPPLY		
Size	Variant Name = PROC062B001		Rev
C			A
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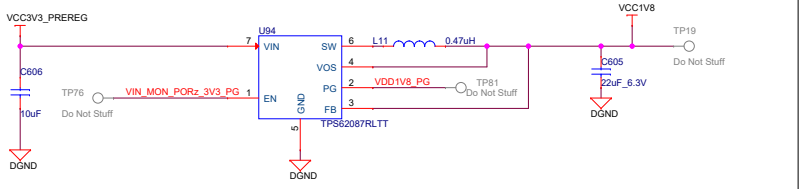
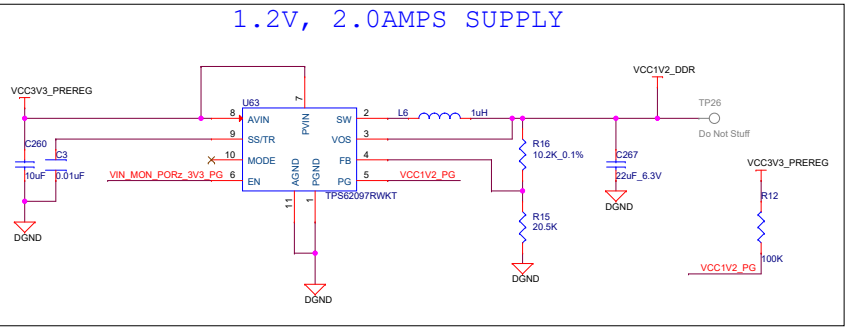
SoC POWER SUPPLY

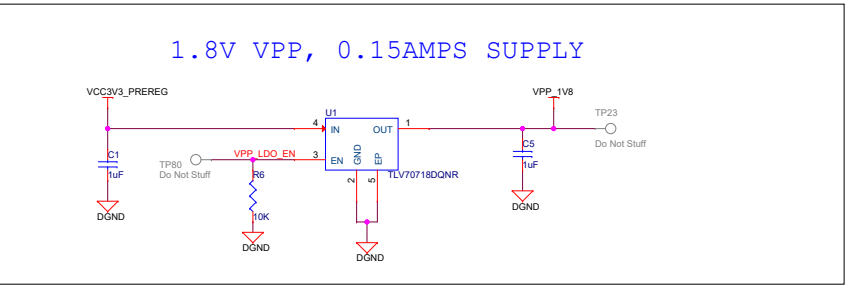
1.8V IO, 3.0AMPS SUPPLY



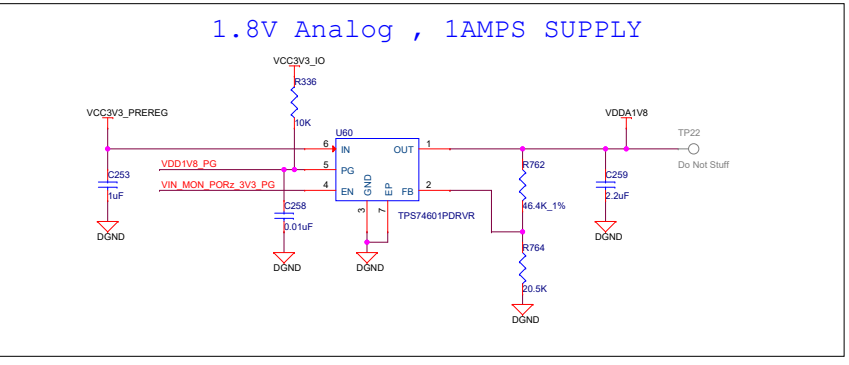
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY

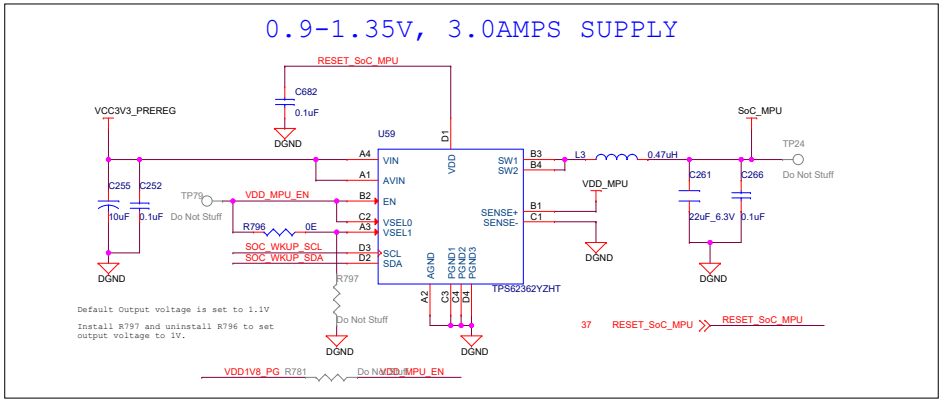


1.8V Analog , 1AMPS SUPPLY

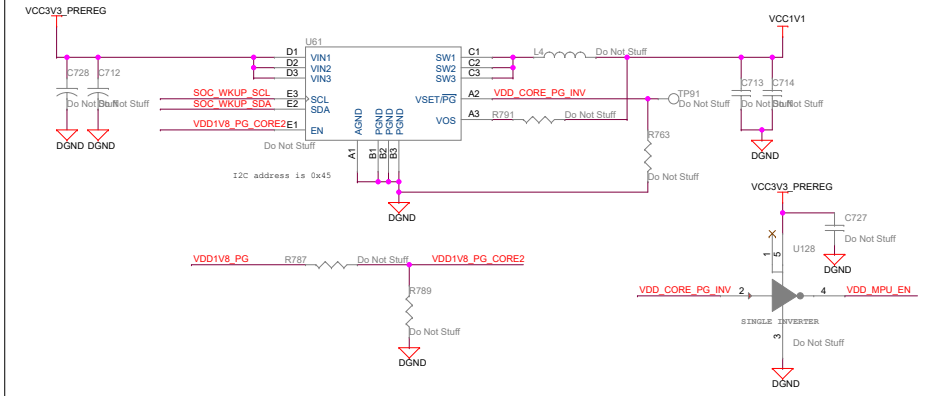


19,32,33,34,35 SOC_WKUP_SCL >> SOC_WKUP_SCL
19,32,33,34,35 SOC_WKUP_SDA <> SOC_WKUP_SDA
18 VPP_LDO_EN << VPP_LDO_EN
39,42 VIN_MON_PORz_3V3_PG << VIN_MON_PORz_3V3_PG
39,42 VDD1V8_PG << VDD1V8_PG

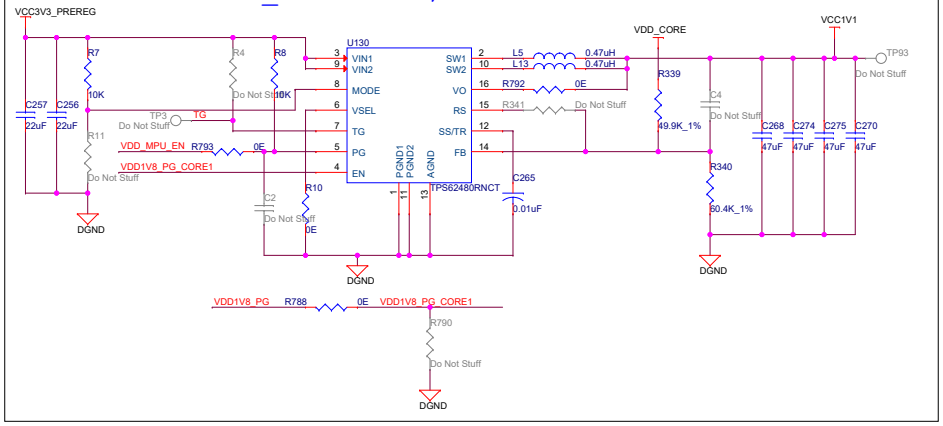
0.9-1.35V, 3.0AMPS SUPPLY



VDD_CORE 1.1V, 6.0AMPS SUPPLY (Optional)



VDD_CORE 1.1V, 6.0AMPS SUPPLY

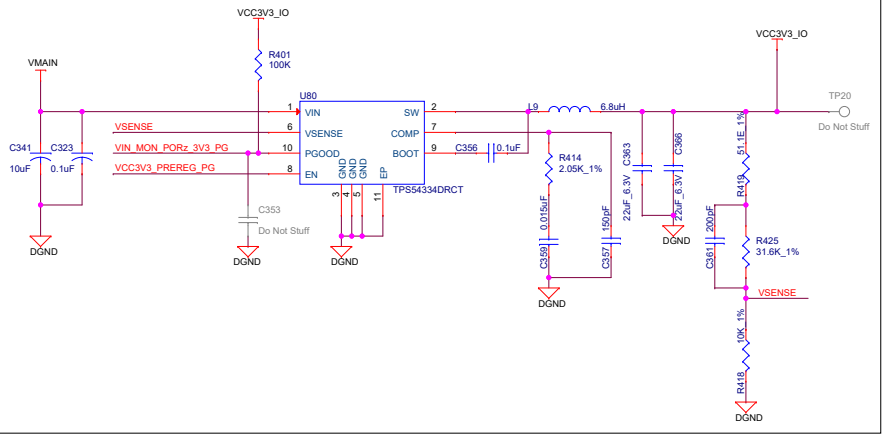


Designed for TI by Mistral Solutions Pvt Ltd

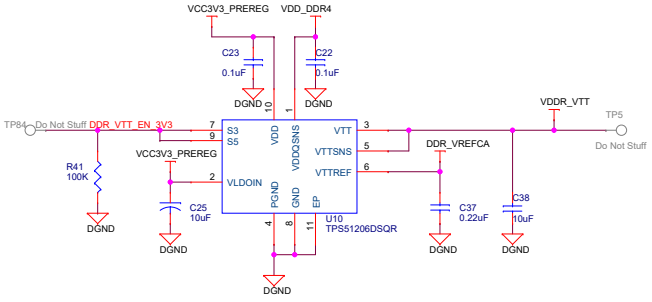
Title	SoC POWER SUPPLY		
Size	Variant Name = PROC062B001		Rev
C			A
Date:	Thursday, July 01, 2021	Sheet 41 of 44	

PERIPHERAL POWER SUPPLY

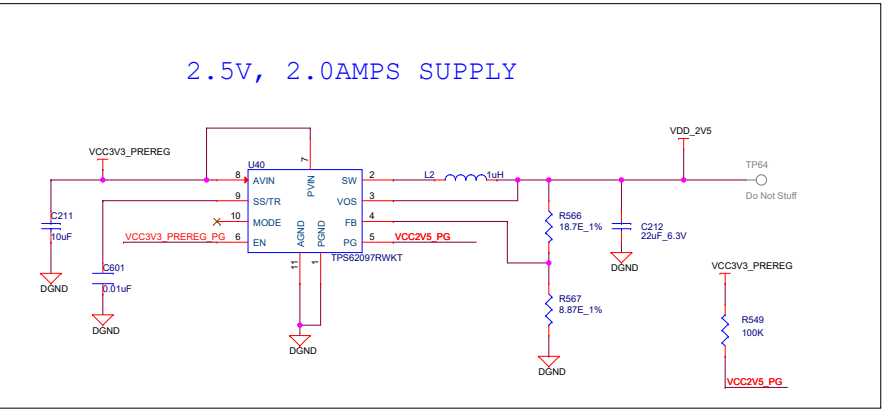
3.3V, 3.0AMPS SUPPLY



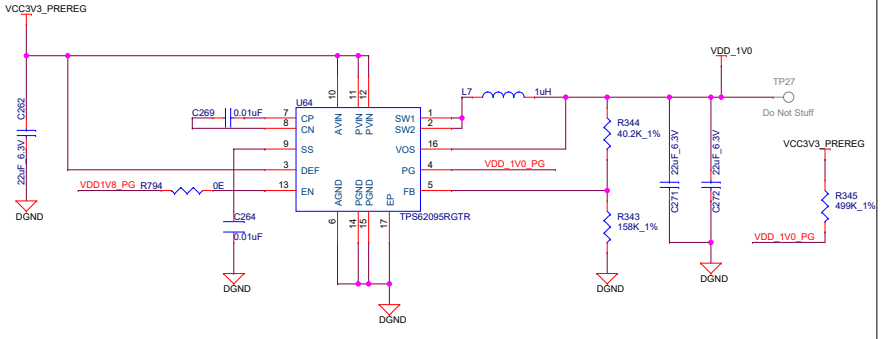
VTT SUPPLY FOR DDR4



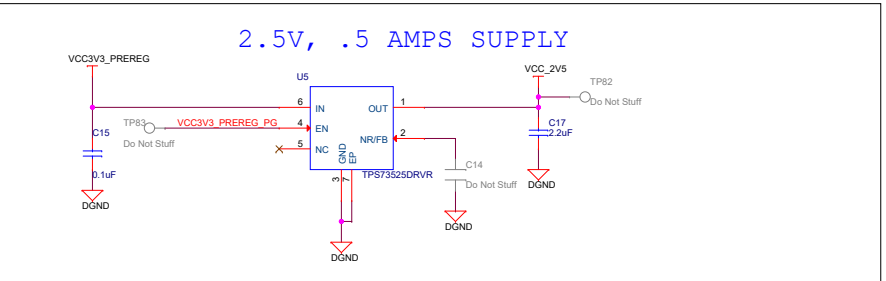
2.5V, 2.0AMPS SUPPLY



1.0V ETHERNET PHY POWER SUPPLY



2.5V, .5 AMPS SUPPLY



40	VDD1V8_PG	VDD1V8_PG
40	VCC3V3_PREREG_PG	VCC3V3_PREREG_PG
39,41	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG
37	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3

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Title	PERIPHERAL POWER SUPPLY	
Size: C	Variant Name = PROC062B001	Rev: A
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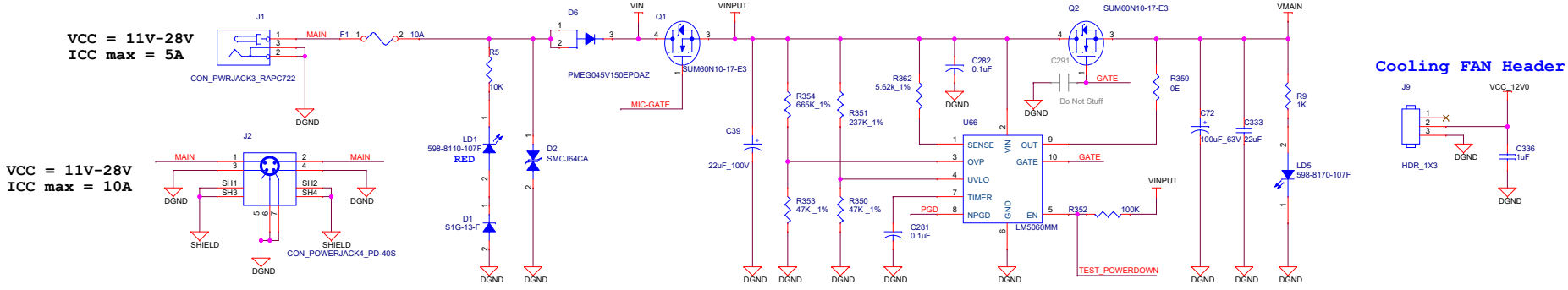
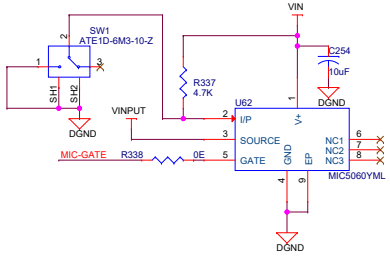
OVER VOLTAGE PROTECTION CIRCUIT



Cooling FAN Header

ON/ OFF Control SWITCH



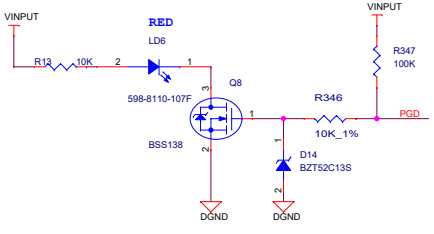
Condition	LED Status(LD1)
Reverse Voltage	ON

23 TEST_POWERDOWN TEST_POWERDOWN

Note:-

UVLO set for 11V
OVP set for 28V

Fault Indication

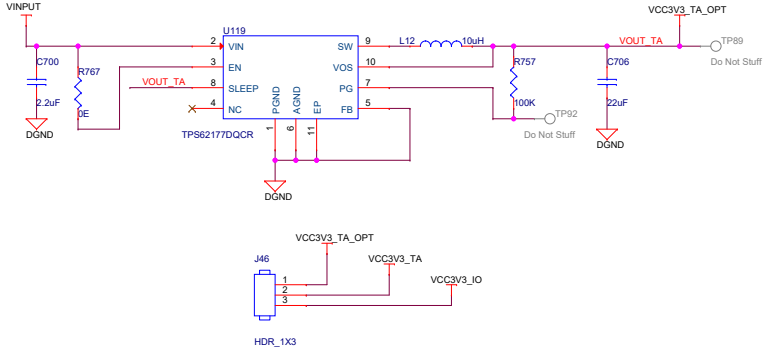


Condition	LED Status(LD6)
VINPUT between 11 to 28V	OFF
VINPUT above 28V or below 11V	ON

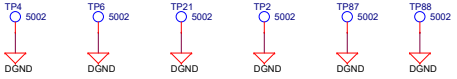
Note:-

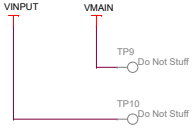
When fault is indicated, set to proper voltage and power cycle the board.

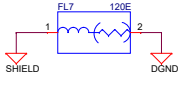
TEST AUTOMATION BOARD POWER



Ground test points







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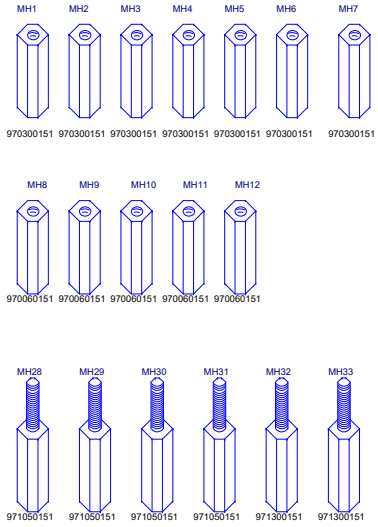
Title	OVER VOLTAGE PROTECTION CKT AND TEST AUTOMATION POWER	
Size C	Variant Name = PROC062B001	Rev A
Date: Thursday, July 01, 2021	Sheet 43 of 44	

HARDWARE SCHEMATICS

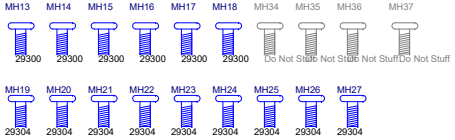
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

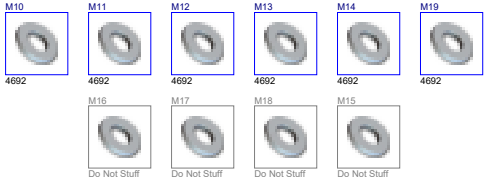
STANDOFFs



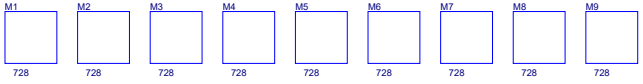
SCREWS



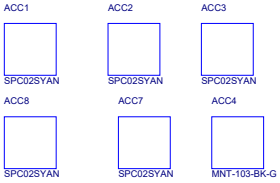
WASHER's



RUBBER FEET



JUMPERs



FIDUCIALS

SOCKET, PROCESSOR & HEATSINK AS ACCESSORIES

BARE PCB

ASSEMBLED PCB'S

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision

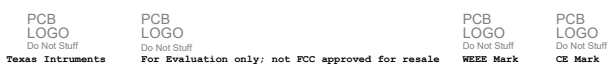
LBL3
PCB LABEL
THT-103-423-10

ORDERABLE PART NO

LBL2
PCB LABEL
THT-103-423-10

Orderable part number	
Variant	**Label Text**
001	TMDX654IDKEVM
002	TMDX654HSEVM
003	TMDX654GPEVM
004	TMDX654IDKEVM-S
005	TMDX654GPEVM-S

LOGOs



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Title	HARDWARE SCHEMATICS	
Size: C	Variant Name = PROC062B001	Rev: A
Date: Thursday, July 01, 2021	Sheet 44 of 44	