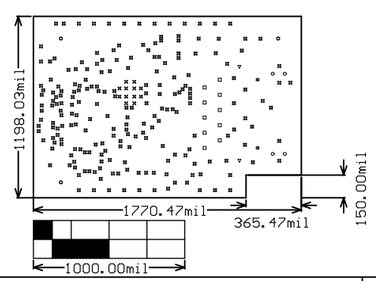
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	Iteq IT180A Prepreg	3.51mil	4.13	
2	Layer 2 - GND	CF-004	1.38mil		
	Dielectric 2	Iteq IT180A 4 mil core	4.00mil	4.1	
3	Layer 3 - Signal/Power	CF-004	1.38mil		
	Dielectric1	FR-4 High Tg	36.80mil	4.2	
4	Layer 4 - VDDIO	CF-004	1.38mil		
	Dielectric 3	Iteq IT180A 4 mil core	4.00mil	4.1	
5	Layer 5 - GND	CF-004	1.38mil		
	Dielectric 4	Iteq IT180A Prepreg	3.51mil	4.13	
6	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Top and Bottom Layers contain 100ohm +/-10% differential pairs for Ethernet using 5mil traces with 8mil spacking

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
	12	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
	212	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	
	10	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer	
	4	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
	2	66.93mil (1.700mm)	PTH	Round	Top Layer - Bottom Layer	
	3	104.33mil (2.650mm)	NPTH	Round	Top Layer - Bottom Layer	
	2	127.95mil (3.250mm)	NPTH	Round	Top Layer - Bottom Layer	
	245 Total					



Minimum allowed radius for interior corner is 31mils

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 4.7 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-4 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER Red
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☐ REQUIRED ☒ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: DP83867-EVM-AM
DESIGNED FOR: Public Release
FILE NAME: DP83867-EVM-AM2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE | BOARD #: PROC188 | REV: A | SVN REV: ab3fb1f6524b28b1277c5acb9e45c1f39536b1d14
LAYER NAME = [illegible]ions | TID #: N/A
PLOT NAME = Fabrication Drawing | GENERATED : 1/23/2025 5:54:57 PM | TEXAS INSTRUMENTS

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ENGINEER: Darius Williams
LAYOUT BY: a0272566
SCALE: 1.00
ALTIUM DESIGNER VERSION: 23.4.1.23