PCI Express M.2 Specification

Revision 5.0, Version 1.0

April 29, 2023

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Revision History

Rev	Version	History	Date
1.0		**Initial Release**	November 1, 2013
1.1		**Incorporated the following ECNs:** • Transition of NFC Signals from 3.3 V to 1.8 V ECN • M.2 COEX Signal Definition – UART ECN • M.2 2242 WWAN Module ECN • M.2 Signal Definition – Audio and ANTCTL Functions ECN • Tx Blanking and SYSCLK on Socket 1 Related Pinouts ECN • Power-up Requirements for PCIe Side Bands (PERST#, etc.) ECN • Power-up Requirements for PCIe Side Bands in a V_{BAT} Powered System ECN • MiniEx_M2_ECN_SMBus_for_SSD_Socket2_Socket3 - 1112_14 • WWAN_Key_C_Definition_ECN_WW12.3 • SMBus ECN, Clarification • BGA-SSD ECN • M.2 SSIC Eye Limits Definitions **Other changes:** • Incorporated all changes from *M2_10 Errata Table and Backup of M 2 0 Errata Table 04292015-6.8.* • Added section 6.8, *High Speed Differential P Rev1 air AC Coupling Capacitor Values and Capacitor Location Examples* • Changed all Mid-Line and Mid-plane to Mid-mount per WG decision • Clarified the terms Module, Add-in Card, Adapter • Capitalized Platform • Removed all + signs from voltages • Updated per *PCI SIG Style Guide* • Updated specification to USB3.1 Gen1 • Added *MIPI Alliance Specification for RF Front-End Control Interface (RFFE[SM]),* Version 2.0, September 25, 2014 to section 1.3	December 15, 2016
3.0	1.2	**Incorporated the following ECNs:** • PCIe BGA SSD 11.5x13 ECN • Add a second PCIe lane to Type 1216 SDIO Based LGA Module ECN • Additional voltage value for PWR_1 rail V0.3 ECN • Enable PCIe and USB 3.1 Gen1 on M.2 Card Key B ECN • Corrected Table 3-15 **Replaced the following Figures:** • Figure 2-8. M.2 Type 3042-S3 Mechanical Outline Drawing (Key B example shown) • Figure 3-9. Type 2226 SDIO Based Module-side Pinout • Figure 3-10. Type 1216 SDIO Based Module-side Pinout • Figure 3-11. Type 3026 DisplayPort Pinouts Extension Over an SDIO Based Module-side Pinout • Figure 3-18. Type 1620 BGA Module-side Ballmap (Top View) • Figure 3-19. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View) • Figure 3-20. Type 1113 BGA Module-side Ballmap (Top View) • Figure 5-1. Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform • Figure 5-2. Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform • Figure 5-3. Type 3026 LGA Pinout Using SDIO Based Socket 1 and DisplayPort Based Socket 1 Pinout on Platform • Figure 5-4. Type 1620 BGA Pinout on Platform (Top View) • Figure 5-6. Type 1113 BGA Socket Map on Platform (Top View)	July 11, 2019

Rev	Version	History	Date

4.0	1.0	**Incorporated the following ECNs:**
		• BGA SSD Voltage ID ECR 2018-10-31a
		• M.2_8G_Compliance_ECN
		• NCTF Ground Ball Definition for PCIe BGA SSD 11.5x13 ECN
		• PLI_1.8V_USB_Higher Power ECN
		• Added 16 G Updates
		• Incorporated clarification and editorial changes based on errata M2_40_errata_table_06_03_2020.docIncorporated *Cin Maximum Increase* ECN. (see Table 4-1 and Table 4-2).
		• Incorporated *Add core voltage 0.8 V in PWR_3 for BGA SSD* ECN (see Table 3-31, Table 3-32, Table 3-33, and Table 4-5)
		• Incorporated M.2 Socket-1 Enhancements ECN
		  - Added Section 3.1.15, Optional Signals
		  - Added Table 3-11
		  - Updated Table 2-9, Table 3-1, Table 3-12, Table 3-13, Table 3-14, Table 5-3, and Table 5-4
		• Incorporated High-Power M.2 Heat Spreader ECN
			November 5, 2020

4.0	1.1	**Incorporated the following ECNs:** • Voltage Indication for PCIe BGA 1113 SSD and 1.0 V PWR3 support. • M.2 3052 3060 WWAN Module • M2PWRDIS asserted hold time reduction **Other changes** • Incorporated Errata dated August 17, 2022	April 14, 2022
5.0	1.0	**Incorporated the following ECNs/Errata:** • Incorporated ECN: Add core voltage 0.75 V in PWR_3 rail for BGA SSD • 1.8V IO for LGAs • M.2_5.0_Ver0.7_errata_table_Nov30_2022 • Incorporated ECN M.2-1A Add-in Card and Connector Amperage Improvement	April 29, 2023

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1. Introduction to M.2 Specification

The M.2 form factor is intended for Mobile Adapters. The M.2 is a natural transition from the Mini Card and Half-Mini Card (refer to the *PCI Express Mini CEM Specification*) to a smaller form factor in both size and volume. The M.2 is a family of form factors that enables expansion, contraction, and higher integration of functions onto a single form factor module solution.

One of the goals for M.2 is to be significantly smaller in the XYZ and overall volume than the Half-Mini Card for the very thin computing Platforms (e.g., Notebook, Tablet/Slate Platforms) that require a much smaller solution.

The M.2 comes in two main formats:

❑ Connectorized
❑ Soldered-down

Figure 1-1 shows the concept board Add-in Card and Module.
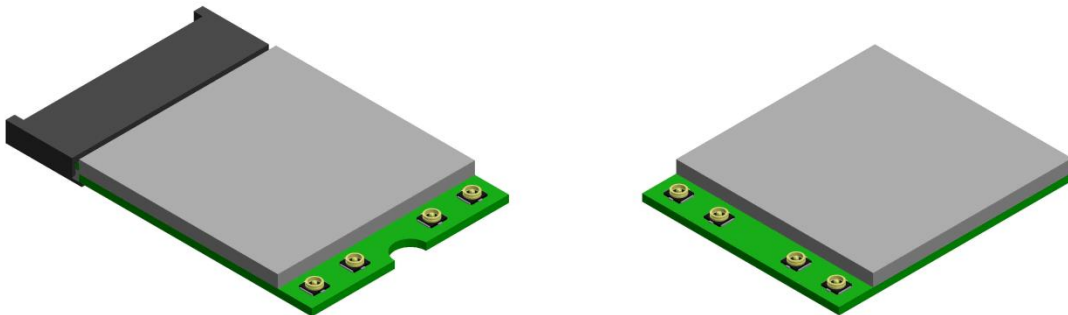
Figure 1-1. M.2 Concept Add-in Card and Module

In general, M.2 supports addressing system manufacturers' needs for build-to-order (BTO) and configure-to-order (CTO). It is expected that system manufacturers that build to and order modules to this specification are responsible for indicating to their module suppliers which optional features are required to support their specific system.

1.1.   Terms and Definitions

A	Amperage or Amp
Adapter	Used generically to refer to an Add-in Card or Module.
Add-in Card	A card that is plugged into a connector and mounted in a chassis socket.
BGA	Ball Grid Array
BIOS	Basic Input Output System
BT	Bluetooth
BTO	Build-to-Order
CEM	Card Electromechanical
CTO	Configure To Order
DC	Direct Current
DNU	Do Not Use
DPR	Dynamic Power Reduction
GND	Ground
GNSS	Global Navigation Satellite System (GPS+GLONASS)
HDR	Hybrid Digital Radio
Host	Typically referring to the electrical interface source/root complex
HSB	Host-specific Balls
HSIC	High Speed Inter-Chip
I/F	Interface
I/O (O/I)	Input/Output (Output/Input)
IR	Current x Resistance = Voltage
I^{2}C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
LED	Light Emitting Diode
LGA	Land Grid Array
M.2	Formerly called Next Generation Form Factor (NGFF)
mA	milliamp
mm	millimeter
mΩ	milliohm
Module	Device that is soldered down to the Platform motherboard.
M-PCIe	PCIe over MIPI Alliance M-PHY

mV	millivolt
N/A	Not Applicable
NB	Notebook
NC	Not Connected
NCTF	Non-Critical To Function
NFC	Near Field Communications
NIC	Network Interface Card
OD	Open Drain
OEM	Original Equipment Manufacturer
OS	Operating System
PCIe	PCI Express®
Platform	Typically referring to the system within which a Main Board or Mother Board (MB) is located, to which the Module or Add-in Card are mounted.
SATA	Serial Advanced Technology Attachment or Serial ATA
PCM	Pulse Code Modulation
RF	Radio Frequency
RFU	Reserved for Future Use
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances Directive
RSS	Root Sum Square
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface Pins
SSD	Sold-State Drive
SSIC	Super Speed USB Inter-Chip
RF	Radio Frequency
USB	Universal Serial Bus
UART	Universal Asynchronous Receive Transmit
V	Voltage
W	Wattage or Watts

WiGig	60 GHz multi-gigabit speed wireless communication
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network
x1, x2, x4	x1 refers to one Lane of basic bandwidth. x2 refers to a collection of two Lanes. x4 refers to a collection of four Lanes. This is applicable to PCIe, DisplayPort and other host interfaces that are permitted to use multi-Lane.

1.2.　　Targeted Application

This M.2 family of form factors is intended to support multiple function Adapter that include the following:

❑ Wi-Fi

❑ Bluetooth (BT)

❑ Global Navigation Satellite Systems (GNSS)

❑ Near Field Communication (NFC)

❑ WiGig

❑ WWAN (2G, 3G, and 4G)

❑ Solid-State Storage Devices (SSD)

❑ Other and Future Solutions (e.g., Hybrid Digital Radio (HDR))

❑ Hardware Accelerator

This specification covers multiple Host Interface solutions including:

❑ PCIe

❑ SPI

❑ HSIC

❑ SSIC

❑ M-PCIe

❑ USB

❑ SDIO

❑ UART

❑ PCM/I2S

❑ I^2C

❑ SMBus

❑ SATA

❑ DisplayPort

❑ All future variants of the interfaces in this list

In light of the fact that the number of host interfaces has dramatically increased and in order to support the multitude of Comms and other solutions typically integrated into Notebook (NB)-based and very thin-based Platforms, there is a need to clearly define several distinct sockets:

❑ Connectivity Socket (typically Wi-Fi, BT, NFC or WiGig) designated as Socket 1

❑ WWAN/SSD/Other Socket that will support various WWAN+GNSS solutions, various SSD and SSD Cache configurations and potentially other yet undefined solutions designated as Socket 2

❑ SSD Drive Socket with SATA or up to 4 lanes of PCIe designated as Socket 3

Each of the three sockets is unique and incorporates a different collection of host interfaces to support the specific functionality of the Add-in Card. The Add-in Cards are typically not interchangeable between sockets. Therefore, each Socket will have a unique mechanical key. However, there are cases where a dual mechanical key scheme will enable dual socket support. Details of the sockets will be described in the following sections of this document.

> **!** **CAUTION: M.2 Add-in Cards are not designed or intended to support Hot-Swap or Hot-Plug connections. Performing Hot-Swap or Hot-Plug may pose danger to the M.2 Add-in Card, to the system Platform, and to the person performing this act**.

For the sake of coverage, the M.2 Add-in Card will be defined as both single-sided for low profile solutions and double-sided to enable more content to be integrated in the Platform. Several target Z-heights will be outlined as part of the specification. Actual configuration implementation will be determined between customer and vendor. A naming convention will enable an exact definition of all key parameters.

1.3. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

❑ *PCI Express Mini Card Electromechanical (Mini CEM) Specification*, Revision 2.1

❑ *PCI Express Card Electromechanical (CEM) Specification*, Revision 5.0, Version 1.0

❑ *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 6.1

❑ *PCI Express Base Specification*, Revision 5.0, Version 1.0

❑ *SDIO 3.0 Specification*

❑ *SSIC – SuperSpeed USB Inter-Chip Supplement to the USB 3.0 Specification,* Revision 1.02, May 19, 2014

❑ *HSIC – High-Speed Inter-Chip USB Electrical Specification*, Version 1.0 (September 23, 2007), plus *HSIC ECN Disconnect Supplement to High Speed Inter Chip Specification*, Revision 0.94 (Sep 20, 2012)

❑ USB2.0 – *Universal Serial Bus Specification*, Revision 2.0, plus ECN and Errata, July 14, 2011, available from http://www.usb.org

❑ *USB3.2 – Universal Serial Bus USB3.2 Specification*, Revision 1.0

❑ *DisplayPort Standard Specifications*, version 1.4

❑ *ISO/IEC 7816-2 Specification*

- *ISO/IEC 7816-3 Specification*
- *Serial ATA Specification*, available from www.sata-io.org
- *I²C BUS Specifications*, Version 2.1, January 2000
- *EIA-364 Electrical Connector/Socket Test Procedures* including Environmental Classifications
- EIA-364-1000.01: *Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- M-PHY – *MIPI Alliance Specification for M-PHY*, Version 3.0
- *MIPI Alliance Specification for RF Front-End Control Interface (RFFE*[SM]*)*, Version 2.0, September 25, 2014
- *JTAG (IEEE 1149.1) Specification*, available from https://www.ieee.org
- *System Management Bus (SMBus) Specification*, Version 3.1, March 19, 2018, available from http://smbus.org/
- *BT-SIG – Bluetooth Core Specification*, v5.3, July 13, 2021
- *PCI Express Architecture, PHY Test Specification*, Revision 5.0

2

2. Mechanical Specification

2.1.   Overview

This specification defines a family of M.2 Adapters and the corresponding system interconnects based on a 75-position edge card connection scheme or a derivation of the card edge and a soldered-down scheme for system interfaces.

The M.2 family comprised of several Adapter sizes and designated by the following names (see Figure 2-1):

- ❑ Type 1113
- ❑ Type 1216
- ❑ Type 1620
- ❑ Type 1630
- ❑ Type 2024
- ❑ Type 2226
- ❑ Type 2228
- ❑ Type 2230
- ❑ Type 2242
- ❑ Type 2260
- ❑ Type 2280
- ❑ Type 2828
- ❑ Type 3026
- ❑ Type 3030
- ❑ Type 3042
- ❑ Type 3052
- ❑ Type 3060
- ❑ Type 22110
- ❑ Type 25110

NOTE: KEY OPTION IS A REPRESENTATION ONLY
AND DOES NOT PROHIBIT ADDITIONAL OPTIONS

GENERAL TOLERANCE IS ±0.15 mm
ALL DIMENSIONS IN mm

GENERAL TOLERANCE IS ± 0.15 mm
ALL DIMENSIONS IN mm

M.2-0101
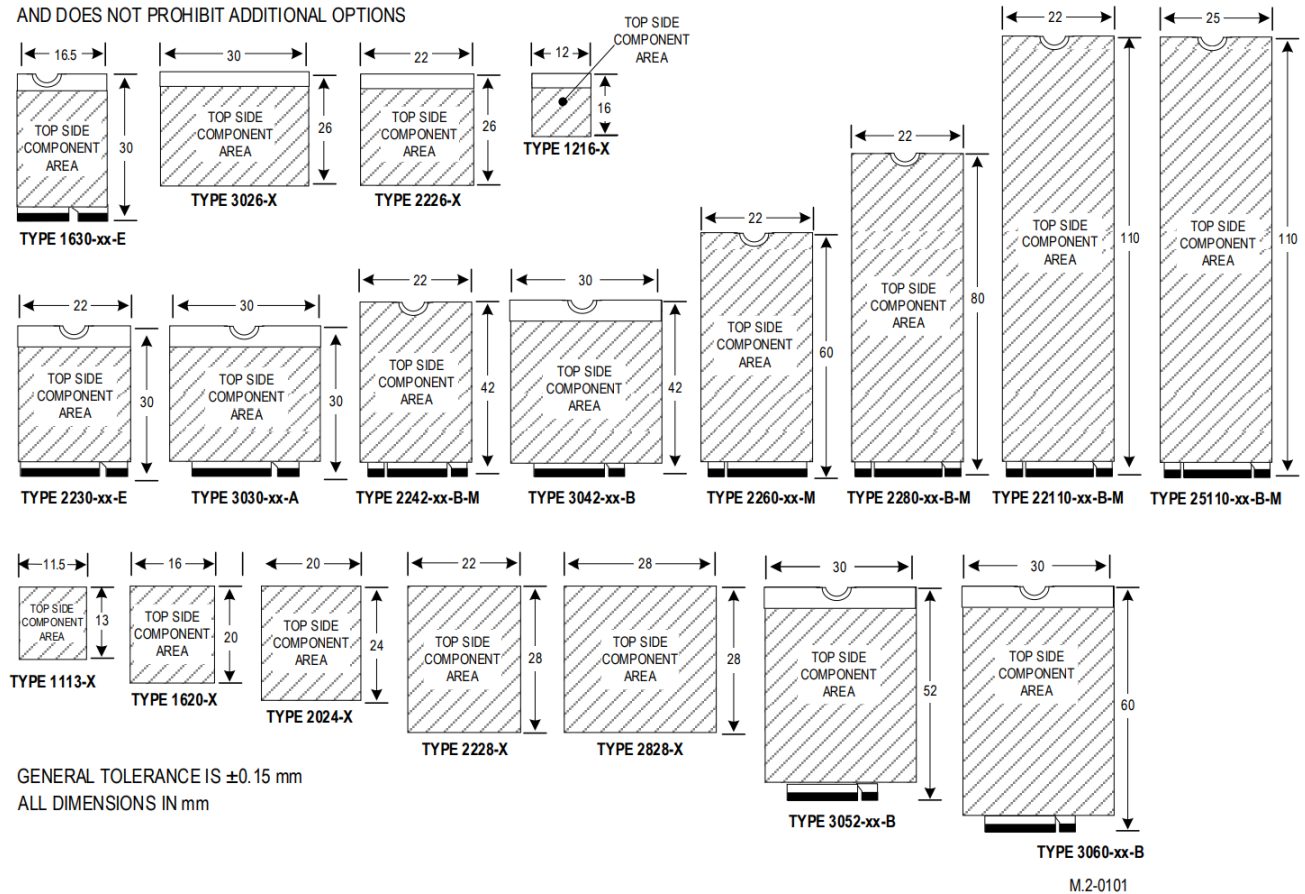
Figure 2-1.   M.2 Family of Form Factors

The majority of M.2 types are connectorized using an edge connection scheme that is either single-sided or double-sided assembly. There will be several component Z-height options defined in this specification. The type of edge connector will cater to different Platform Z-height requirements. In all cases, the board thickness is 0.8 mm ±10%. The Type 1216, Type 2226, and Type 3026 are soldered down solutions that have a Land Grid Array (LGA) pattern on the back. Therefore, they are single-side and the board thickness does not need to adhere to the 0.8 mm ±10% requirement. The Type 1113, Type 1620, Type 2024, Type 2228, and Type 2828 are soldered-down solutions that have Ball Grid Array (BGA) pattern on the back and are defined for BGA SSDs. These BGA solutions are placed directly on host Platforms as standalone BGA SSDs (see Section 3.4 for the interface specification). Some BGA types are mounted on SSD Socket 2 or SSD Socket 3 Add-in Cards (see Sections 3.2 and 3.3 for interface specification). When a BGA SSD is mounted on SSD Socket 2 or SSD Socket 3 Add-in Cards, the Add-in Card is responsible for implementing the voltage conversion circuitry to provide the voltages required.

The connectorized types include a mechanical key for accurate alignment. The location of the mechanical key along the Gold Finger contacts will make each key unique per a given socket connector. This prevents wrongful insertion of an incompatible board which prevents a safety hazard.

The board type, the type of assembly, the component Z-heights on top and bottom, and the mechanical key will make up the M.2 board naming convention detailed in the next section.

2.2.   Card Type Naming Convention

Since there are various types of M.2 solutions and configurations, a standard naming convention will be employed to define the main features of a specific solution.

The naming convention will identify the following:

❑   The Adapter size (width and length).

❑   The component assembly maximum Z-height for the top and bottom sides of the Adapter.

❑   The Mechanical Connector Key/Add-in Card key location/assignment or multiple locations/assignments

These naming conventions will clearly define the Adapter functionality, what connector it coincides with, and what Z-heights are met. Figure 2-2 diagrams the naming convention.

The Adapter width options are 11.5 mm, 12 mm, 16 mm, 16.5 mm, 20 mm, 22 mm, 28 mm, and 30 mm.

The Adapter length scales to various lengths to support the content and expand as the content increases. The lengths supported are 13 mm, 16 mm, 20 mm, 24 mm, 26 mm, 28 mm, 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

Together these two dimensions make up the first part of the Adapter type definition portion of the Adapter name.

The next part of the name describes whether the Adapter is single-sided or double-sided and contains a secondary definition of what are the maximum Z-heights of the components on the top and bottom side of the Adapter. Z-height limits are 2.0 mm, 1.75 mm, 1.5 mm, 1.35 mm, or 1.2 mm on the top-side and 1.5 mm, 1.35 mm, 0.7 mm, or 0 mm on the bottom side. The letter S will designate Single-sided and the letter D will designate Double-sided. This will be complimented with a number that designates the specific Z-height combination option.

The last section of the name will designate the mechanical connector key/Add-in Card key name and the coinciding pin location. These will be designated by a letter from A to M. In cases where the Add-in Card will have a dual key scheme to enable insertion of the Add-in Card into two different keyed sockets, a second letter will be added to designate the second mechanical connector key/Add-in Card key.

Key ID assignments must be approved by the PCI-SIG. Unauthorized Key IDs render the Add-in Card incompatible with this specification.

Figure 2-3 shows an example of Add-in Card Type 2242 – D2 – B – M.

Module Nomenclature
Sample Type 2242-D2-B-M

Type XX XX – XX – X – X$^{(1)}$ – P$^{(7)}$– 1A(X)$^{(8)}$

Used only when Add-in-Card uses M.2-1A Card Outline.
A: M.2-1A Type A Card Outline
B: M.2-1A Type B Card Outline
C: M.2-1A Type C Card Outline
D: M.2-1A Type D Card Outline

Used only when specifying the top surface as planar with dimensional tolerances of +0 / -0.5 mm
and flatness of 0.3 mm; see Figures 2-15, 2-16 and 2-17 for details.

Label$^{(2)}$	Component Max Ht (mm)	
	Top Max	Bottom Max
S1	1.2$^{(4)}$	0$^{(5)}$
S2	1.35$^{(4)}$	0$^{(5)}$
S3	1.5$^{(4)}$	0$^{(6)}$
S4	1.75$^{(4)}$	0$^{(5)}$
S5	2.0$^{(4)}$	0$^{(5)}$
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5
D6	3.2	1.5
D7	3.2	2.0
D8	6.5	1.5

Length (mm)
16
20
24
26
28
30
42
60
80
110

Width (mm)
12
16
20
22$^{(9)}$
25
28
30$^{(9)}$

Key ID	Pin	Interface
A	8-15	2x PCIe x1/USB 2.0/I2C/DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C/SMBus
C	16-23	PCIe/M-PCIe/USB 2.0/USB 3.0/SSIC/I2C-SlimBus/UIM/ANTCTL
D	20-27	Reserved for Future Use
E	24-31	2x PCIe x1/USB 2.0/I2C/SDIO/UART/PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)$^{(6)}$
H	43-50	Reserved for Future Use
J	47-54	Reserved for Future Use
K	51-58	Reserved for Future Use
L	55-62	Reserved for Future Use
M	59-66	PCIe x4/SATA/SMBus

(1)   Use ONLY when a double slot is being specified.
(2)   Label included in height dimension.
(3)   This dimension is 11.5mm but is written as 11 in Type name (I.e. BGA Type 1113)
(4)   For BGA SSD, Max Height is measured with solder balls collapsed and is valid whether BGA
       is located directly on a platform or mounted on a module board
(5)   Insulating label allowed on connector-based designed
(6)   Key G is intended for customer use. Devices with this key will not be M.2 compliant. Use at your own risk.
(7)   Use only when specifying the top surface as planar, see Figures 2-15, 2-16, and 2-17 for details.
(8)   Use only when Add-in-Card current consumption requirements exceed 0.5 A per pin (normal Power Rating) and/or card outline is changed to an M.2-1A type.
(9)   M.2-1A only supports widths of 22 mm and 30 mm.

Figure 2-2.   M.2 Naming Nomenclature
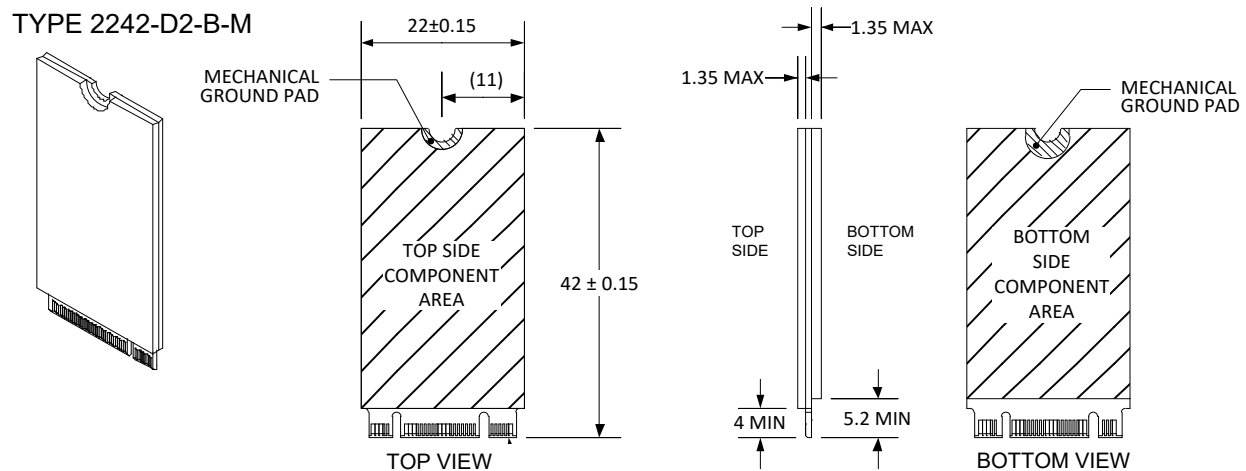
TYPE 2242-D2-B-M

Note: For card-edge details, see Section 2.3.4.

Figure 2-3.   Example of Type 2242-D2-B-M Nomenclature

The board is 22 mm x 42 mm, Double-sided with a maximum Z-height of 1.35 mm on both the Top and Bottom, and it has two mechanical connector keys/ Add-in Card keys at locations B and M which will enable it to plug into two types of connectors (Key B or Key M).

See Table 2-1 for various board configuration options as a function of the Socket, Adapter Function, and Adapter size.

Type 1113, Type 1216, Type 1620, Type 2024, Type 2226, Type 2228, Type 2828, and Type 3026 are Soldered-Down solutions while all the others are connectorized with a PCB Gold Finger layout that coincides with an Edge Card connector. The Soldered-Down solutions do not have mechanical keys and their pinout configuration needs to be specifically called out.

Table 2-1.   Optional Adapter Configurations

		Soldered-down Module Height Options	Pinout Key	Connector Key		Connectorized Add-in Card Height Options	Module Key
	Type				Type		
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230		A, E, A+E
	3026	S1, S3	A+E	A, E	3030		A, E, A+E
Socket 2 WWAN/Other	N/A	N/A	N/A	B, C	3042	S1, D1, S3, D3, D4	B, C
	N/A	N/A	N/A	B, C	2242		B, C
	N/A	N/A	N/A	B, C	3052		B, C
	N/A	N/A	N/A	B, C	3060		B, C
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2242		B+M
	N/A	N/A	N/A	B	2260		B+M
	N/A	N/A	N/A	B	2280		B+M
	N/A	N/A	N/A	B	22110		B+M
	1113	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
Socket 3 SSD Drive	N/A	N/A	N/A	M	2230	S2, D2, S3, D3, D5, D6, D7, D8, S4, S5	M, B+M
	N/A	N/A	N/A	M	2242		M, B+M
	N/A	N/A	N/A	M	2260		M, B+M
	N/A	N/A	N/A	M	2280		M, B+M
	N/A	N/A	N/A	M	22110		M, B+M
	N/A	N/A	N/A	M	25110		M, B+M
	1113	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A

2.3.   Card Specifications

There are multiple defined card outlines. Card thickness is fixed at 0.8 mm ±10% with optional increased/decreased XY dimensions so as to incorporate more or less functionality on the board.

For purposes of the drawings in this specification, the following notes apply:

- ❑ All dimensions are in millimeters (mm), unless otherwise specified.
- ❑ All dimension tolerances are ± 0.15 mm, unless otherwise specified.
- ❑ Insulating material must not interfere with or obstruct mounting holes or grounding pads.
- ❑ The Add-in Card has a 4 mm tall strip at the lower end of the board intended to support the Gold Finger pads used in conjunction with an Edge Card connector. The Gold Fingers appear on both top and bottom side of the Add-in Card PCB.
- ❑ In some configuration, the Adapter has a 3.8 mm strip intended to support Radio Frequency (RF) connectors.
- ❑ All connectorized versions have a mounting/retention screw (half-moon cutout) at the upper end of the Add-in Card used to hold down the Add-in Card onto the motherboard or chassis.
- ❑ The remainder of the board area available is intended for Active Components but not limited to this. Encroachment into this area is permitted if extra area is needed for additional RF antenna connectors.
- ❑ The diagrams showing mechanical connector key/Add-in Card key locations in this document are for example only. Actual Key location/definition is part of the actual Adapter name per the naming convention.
- ❑ Summary of the general tolerance is given in Table 2-2.
- ❑ The component areas defined in this section are the maximum volume available for component placement.

Table 2-2.   General Tolerance

	+ Plus	– Minus
PCB Size Tolerance	0.15 mm	0.15 mm
PCB Thickness	0.08 mm	0.08 mm
Bevel Capabilities	0.25 mm	0.25 mm
Drill Capabilities for Add-in Card key	0.05 mm	0.05 mm

2.3.1.   Card Form Factors Intended for Connectivity Socket 1

2.3.1.1.   Type 2230 Specification

The Generic Adapter size used for the majority of the Connectivity solutions such as Wi-Fi+BT type solutions is Type 2230. This board size also is permitted to accommodate other multi-Comm and Combo solutions.

The Type 2230 Add-in Card is intended to support the multiple Wi-Fi configurations such as 1x1, 2x2, and 3x3. An example of the Type 2230 Add-in Card mechanical outline drawing is shown in Figure 2-4 and Figure 2-5.

The Type 2230 Add-in Card uses a 75-position host interface connector and has room to support up to four RF connectors in the upper section. The recommended location and assignment of the four RF connectors is described in Section 2.3.7. RF connectors are permitted to be placed in other locations on the Type 2230 Add-in Card. In cases where additional RF connectors are needed, they are permitted to be added in the active component area and should maintain a minimal distance of 4.5 mm center-to-center to enable manufacturing test interface of the RF connection.
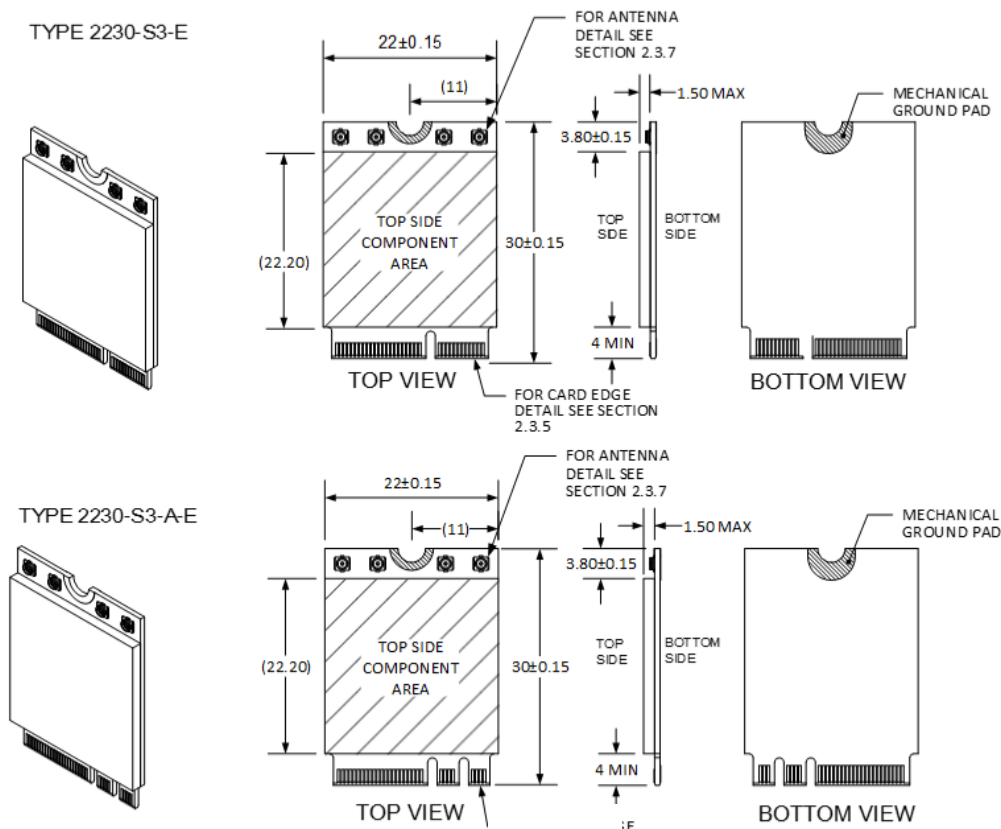
Note: For card-edge details, see Section 2.3.4.

Figure 2-4.   M.2 Type 2230-S3 Mechanical Outline Drawing (Key E and Key A-E examples shown)

TYPE 2230-D3-E
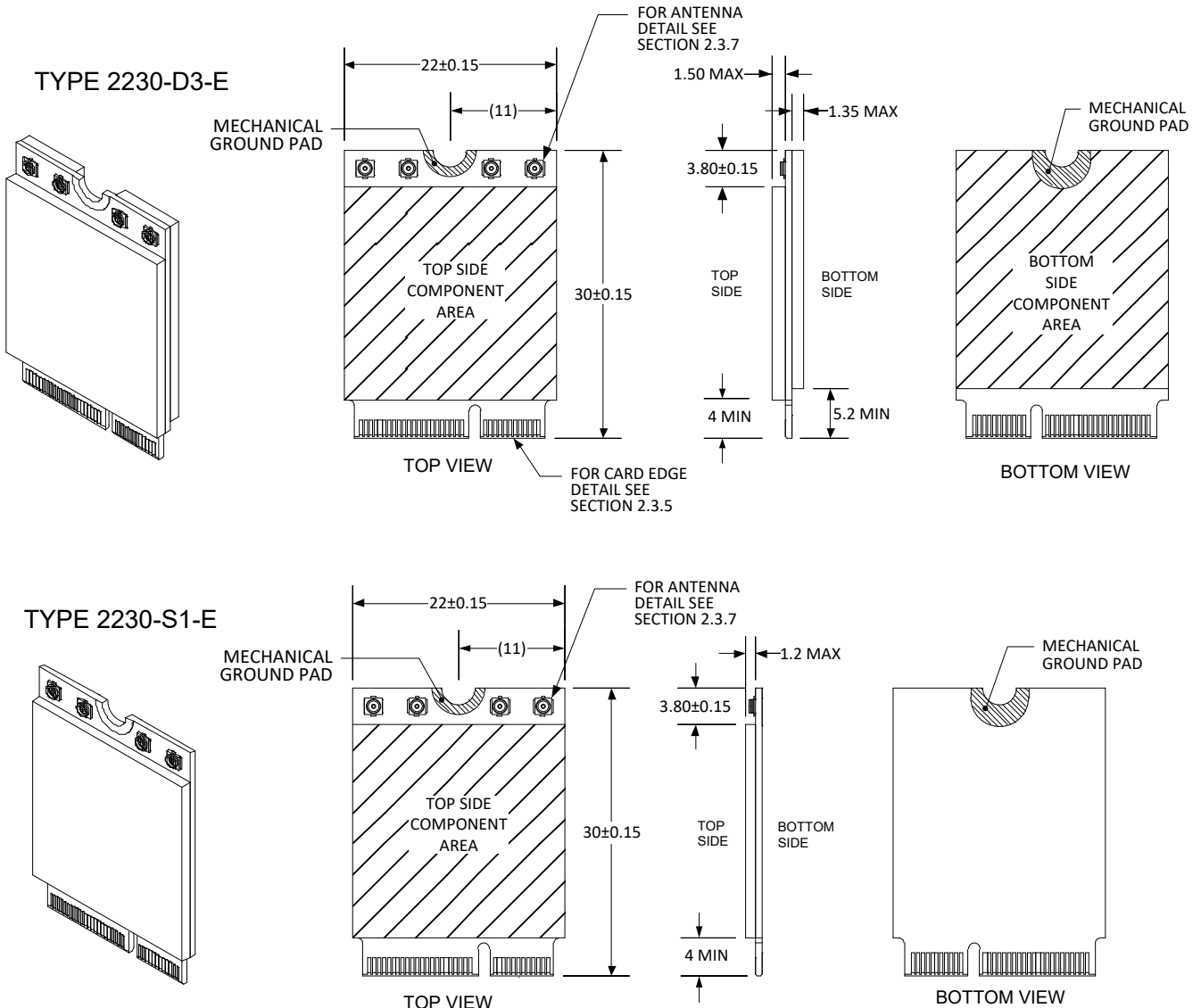
TYPE 2230-S1-E

Note: For card-edge details, see Section 2.3.4.

Figure 2-5.   M.2 Type 2230-D3/S1 Mechanical Outline Drawing
(Key E examples shown)

2.3.1.2.   **Type 1630 Specification**

Type 1630 is a smaller M.2 Add-in Card size used for single Comm or more simplistic Comm combo solutions such as Wi-Fi 1x1 or 2x2 + BT only or future multi-Comm solutions that fits in a smaller footprint.

The Type 1630 is a subset of the Type 2230 board with 5.5 mm sliced off along the entire length of the board.

Therefore, it is inherently limited in the number of RF connections and has a reduced number of pins used in the Host Interface connector. Since the Type 1630 Add-in Card utilizes only the first 57 pin locations (a mechanical key uses eight pins and the connector uses 49 pins for the host interface), it is limited in its connection capability. Therefore, it is limited in the number of Comms that are simultaneously supported on an Add-in Card.

The mounting hole and the mechanical key are the same as those in the Type 2230 so that the motherboard Socket is capable of supporting both Type 2230 and Type 1630.

> **Note:** Add-in Card Type 1630 is limited to Key ID A through H only.

An example of the Type 1630 Add-in Card mechanical outline drawing is shown in Figure 2-6.
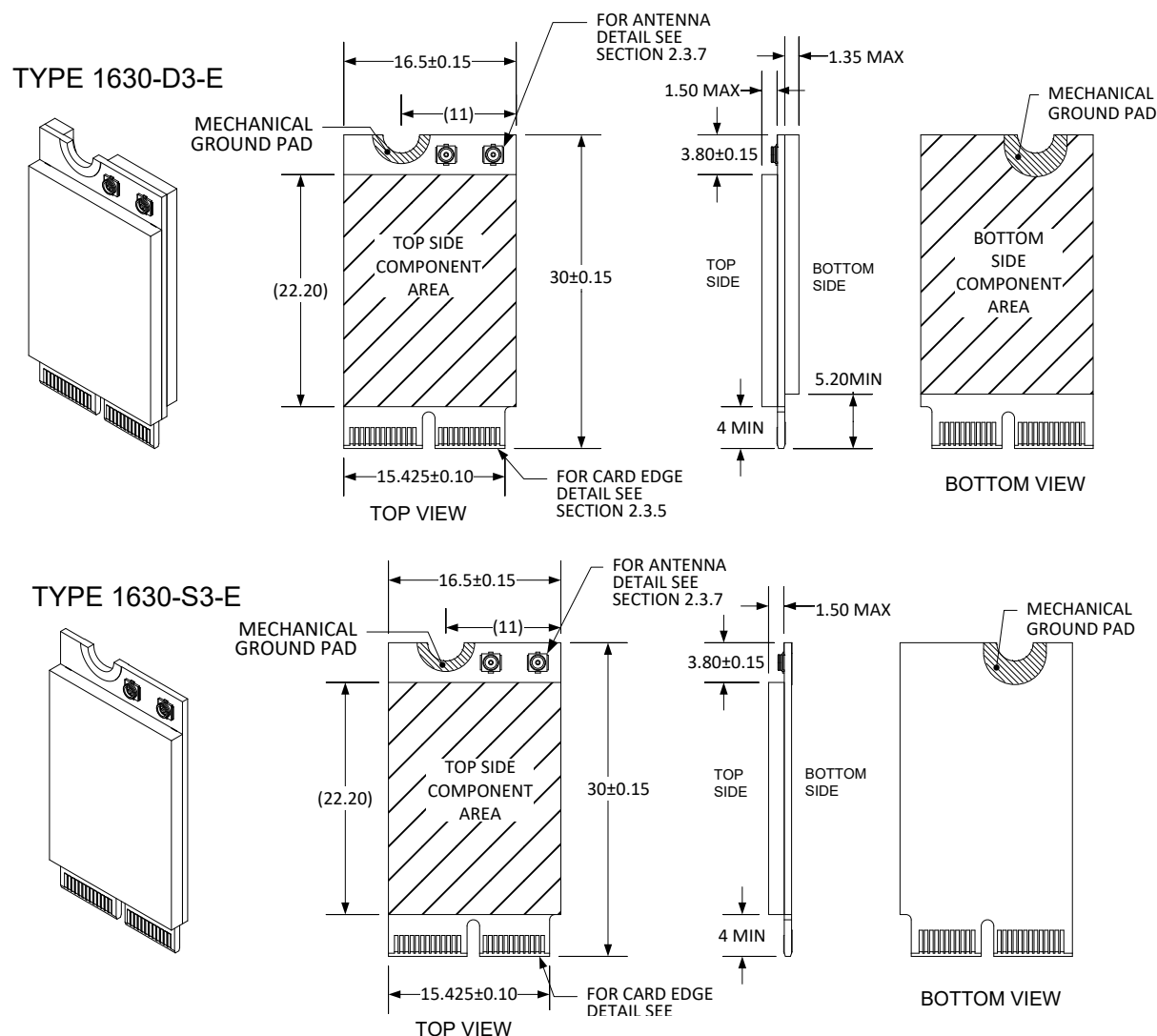
Note: For card-edge details, see Section 2.3.4.

Figure 2-6.   M.2 Type 1630-D3/S3 Mechanical Outline Drawing (Key E examples shown)

2.3.1.3.   Type 3030 Specification

Type 3030 is an extended width M.2 Add-in Card size used for more complex Comm combo solutions.

In principle the board is still comprised of three sections:

❑   Host interface section

❑   RF connector and mounting hole section

❑   Active Component section

The active component section is 8 mm wider making an overall width of 30 mm (instead of the generic 22 mm width). The length remains the same at 30 mm so that it coincides with the other Type xx30 Add-in Cards.

An example of the Type 3030 Add-in Card mechanical outline drawing is shown in Figure 2-7. The wider board size supports a greater number of RF connectors. Up to six (6) RF connectors are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See Section 2.3.7 in this document for recommended locations and assignments.
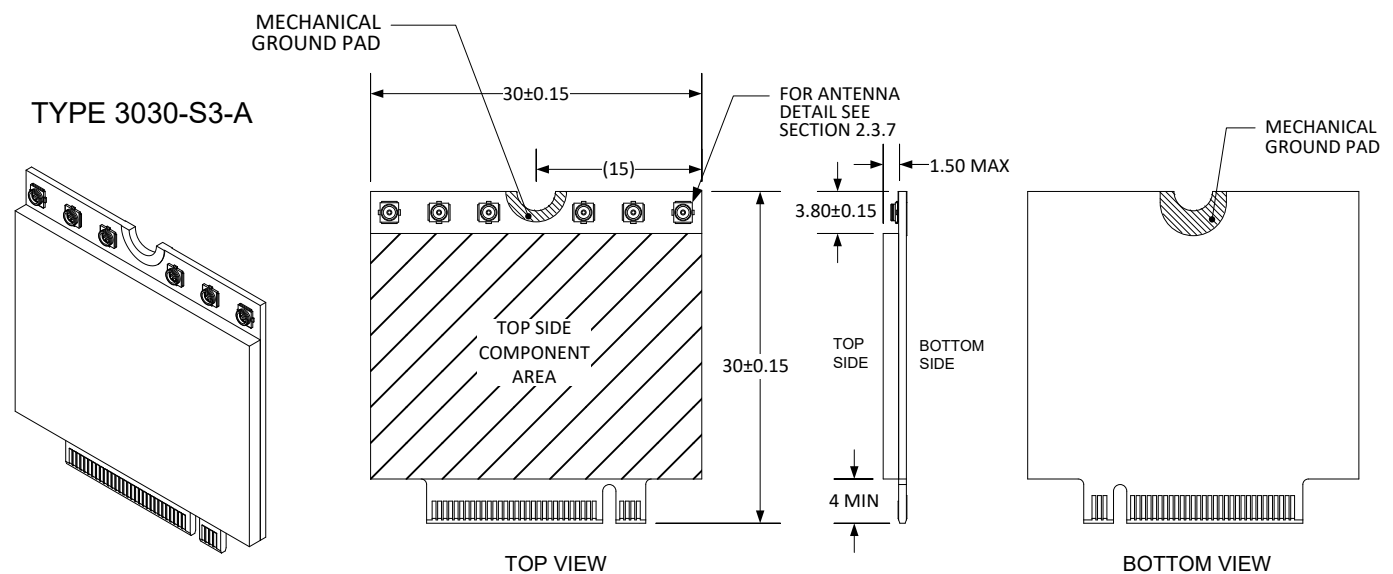
Note: For card-edge details, see Section 2.3.4.

Figure 2-7.   M.2 Type 3030-S3 Mechanical Outline Drawing
(Key A example shown)

2.3.2. Card Form Factors Intended for WWAN Socket 2

2.3.2.1. Type 3042 Specification

Type 3042 is an extended-width M.2 Add-in Card size used for WWAN solutions.

In principle the board is still comprised of three sections:

❑ Host interface section

❑ RF connector and mounting hole section

❑ Active Component section

The active component section is 8 mm wider making it wider than other Add-in Card alternatives intended for Socket 2 with the same overall length of 42 mm.

An example of the Type 3042 Add-in Card mechanical outline drawing is shown in Figure 2-8.

The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See Section 2.3.7 in this document for recommended locations and assignments.
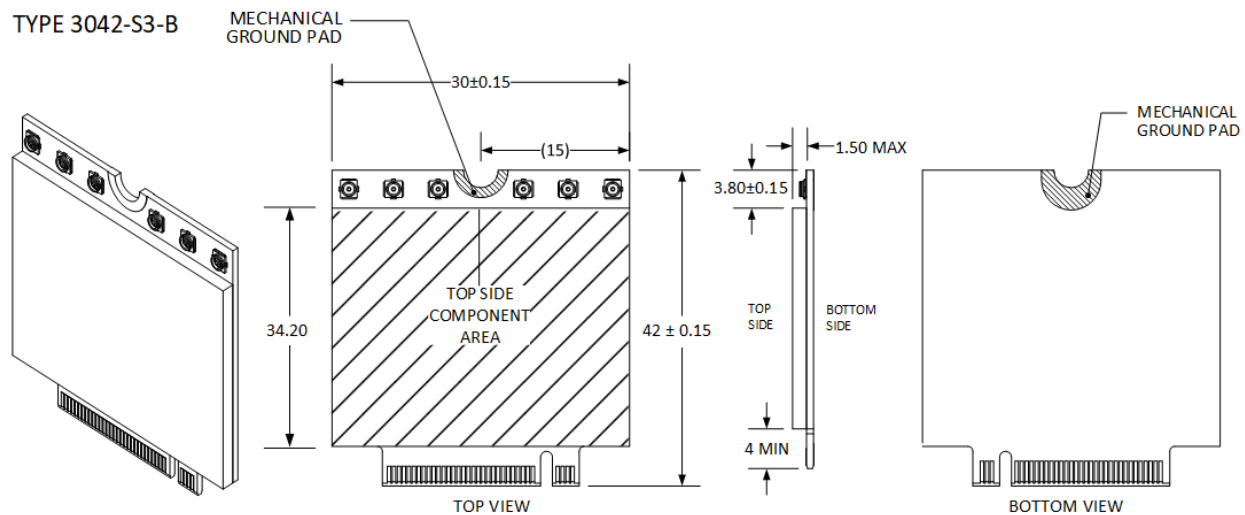
Note: For card-edge details, see Section 2.3.4.

Figure 2-8.   M.2 Type 3042-S3 Mechanical Outline Drawing (Key B example shown)

2.3.2.2. Type 3052 Specification

Type 3052 is an extended-width-length M.2 Add-in Card size used for WWAN solutions.

In principle the board is still comprised of three sections:

❑ Host interface section

❑ RF connector and mounting hole section

❑ Active Component section

The active component section is 8 mm wider making it wider than other Add-in Card alternatives intended for Socket 2. The overall length is extended to 52 mm. An example of the Type 3052 Add-in Card mechanical outline drawing is shown in Figure 2-9.

The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See Section 2.3.7 in this document for recommended locations and assignments.
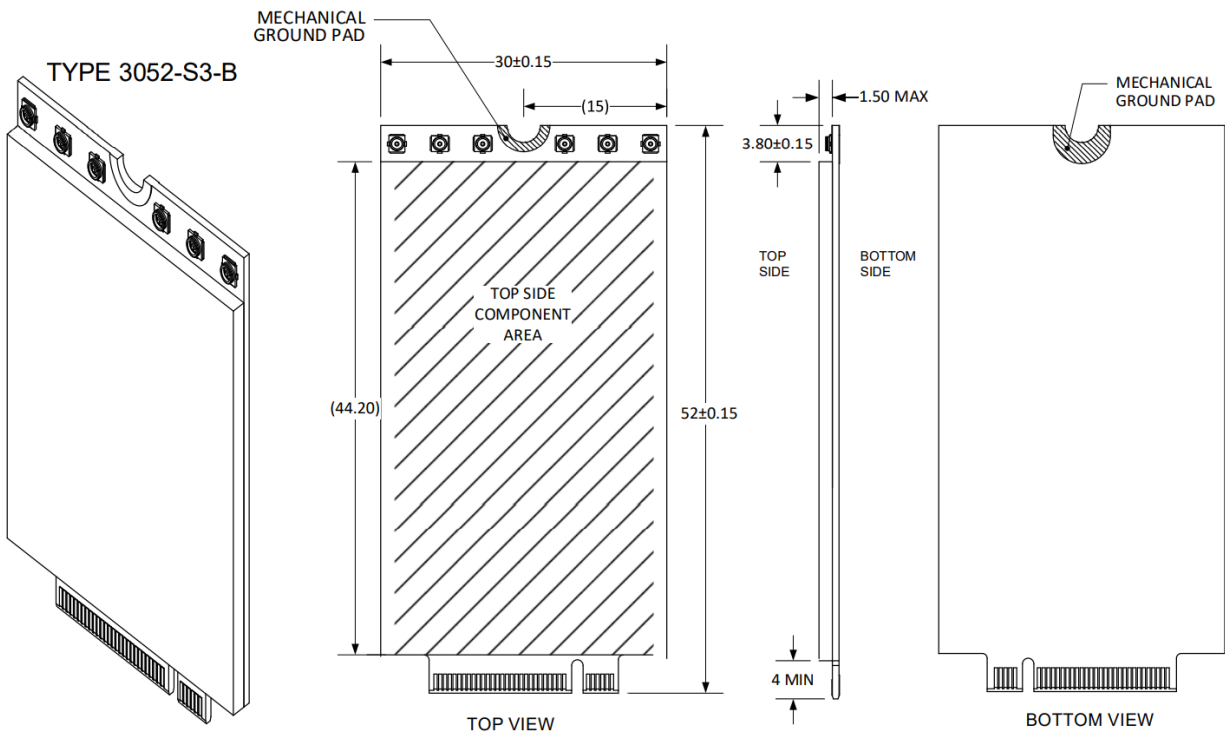
Note: For card-edge details, see Section 2.3.4.

Figure 2-9. M.2 Type 3052-S3 Mechanical Outline Drawing (Key B example shown)

2.3.2.3. Type 3060 Specification

Type 3060 is an extended-width-length M.2 Add-in Card size used for WWAN solutions.

In principle the board is still comprised of three sections:

❑ Host interface section

❑ RF connector and mounting hole section

❑ Active Component section

The active component section is 8 mm wider making it wider than other Add-in Card alternatives intended for Socket 2. The overall length is extended to 60 mm. An example of the Type 3060 Add-in Card mechanical outline drawing is shown in Figure 2-10.

The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See Section 2.3.7 in this document for recommended locations and assignments.
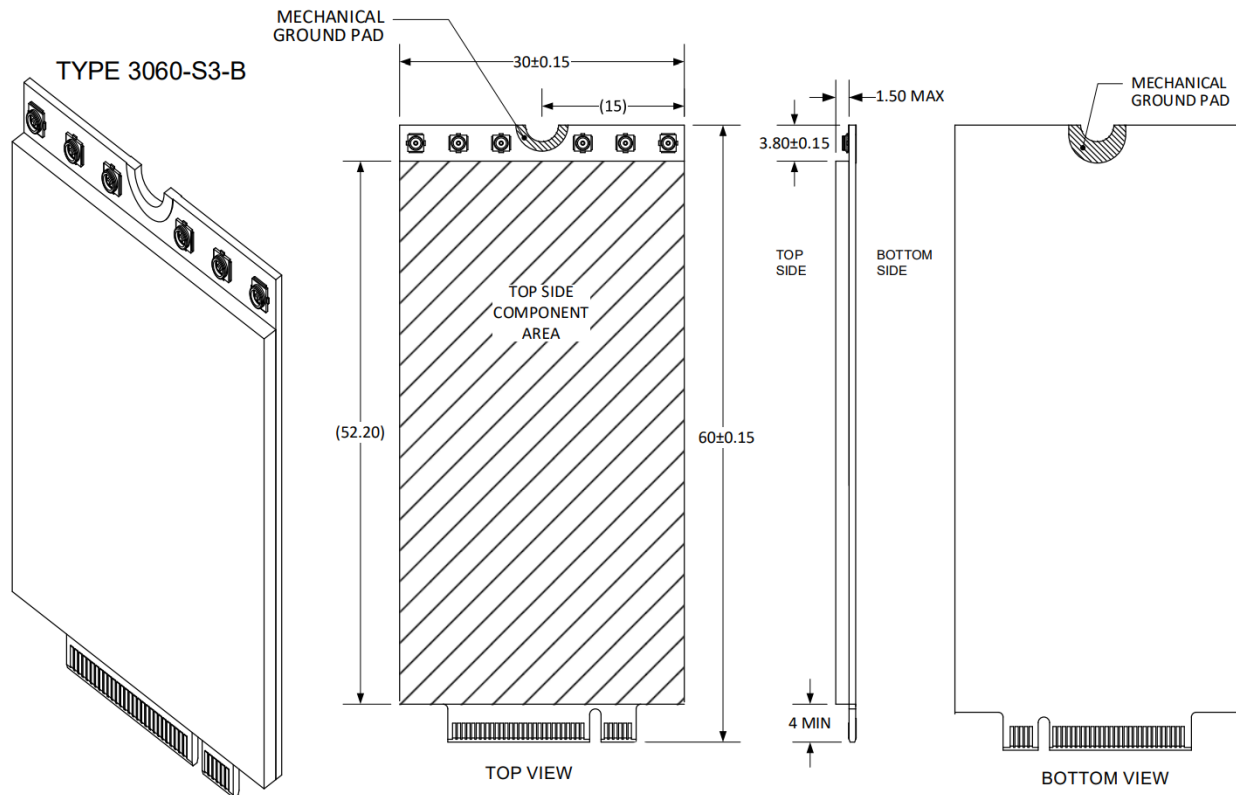
Note: For card-edge details, see Section 2.3.4.

Figure 2-10. M.2 Type 3052-S3 Mechanical Outline Drawing (Key B example shown)

2.3.2.4. **Type 2242 Specification**

Type 2242 is an M.2 Add-in Card size used on Socket 2 and intended to support WWAN solutions. In principle the board is comprised of three sections:

❑ Host interface section

❑ RF connector and mounting hole section

❑ Active Component section

The active component section is 22 mm wide with the same overall length of 42 mm like the other Add-in Card intended for Socket 2.

An example of the Type 2242 Add-in Card mechanical outline drawing is shown in Figure 2-11.

The board size supports up to four (4) RF connectors that are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See Section 2.3.7 in this document for recommended locations and assignments.
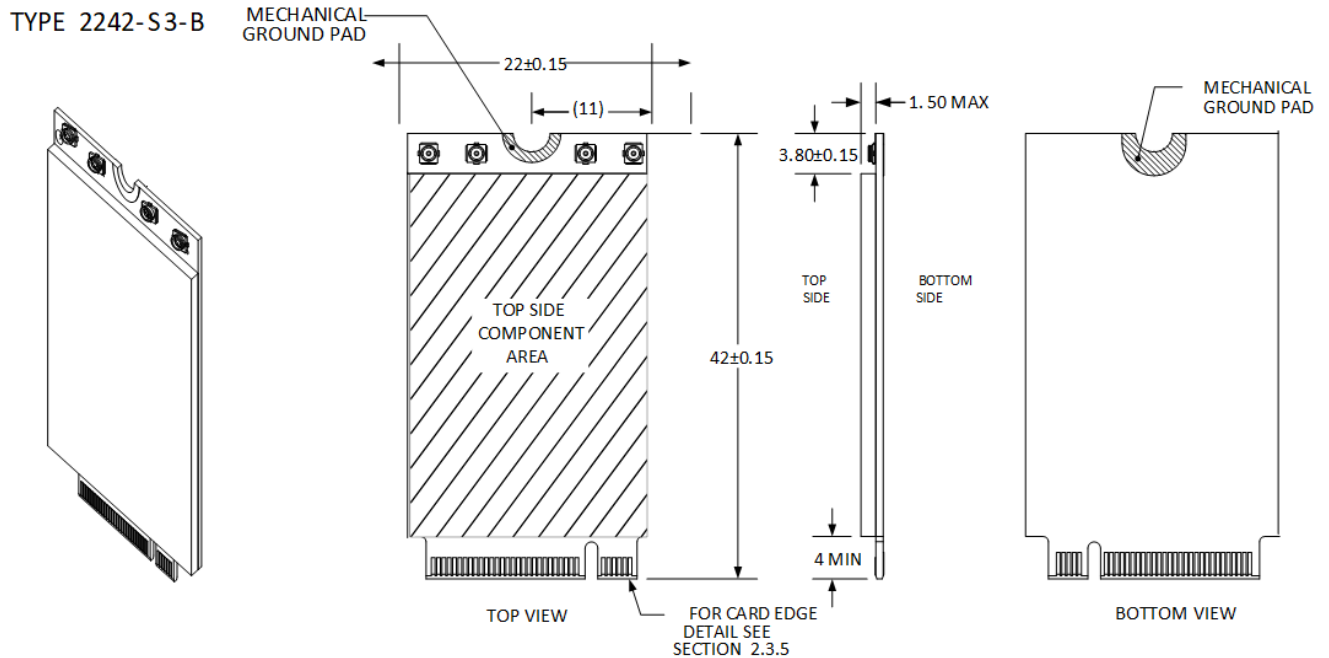
Note: For card-edge details, see Section 2.3.4.

Figure 2-11. M.2 Type 2242-S3 Mechanical Outline Drawing
            (Key B example shown)

2.3.3.   Card Form Factor for SSD Socket 2 and 3

2.3.3.1.   Type 2230 Specification

Type 2230 is an M.2 Add-in Card size used on Socket 2 and Socket 3. It is intended to support SSD solutions and possibly other PCI Express®-based solutions. The board is comprised of two sections:

❑   Host interface section

❑   Active Component section

The active component section including the mounting-hole area has an overall length of 26 mm top-side and 24.8 mm bottom-side when applicable. Figure 2-12 shows Type 2230 Add-in Card mechanical outline drawing.

TYPE 2230-S2-B
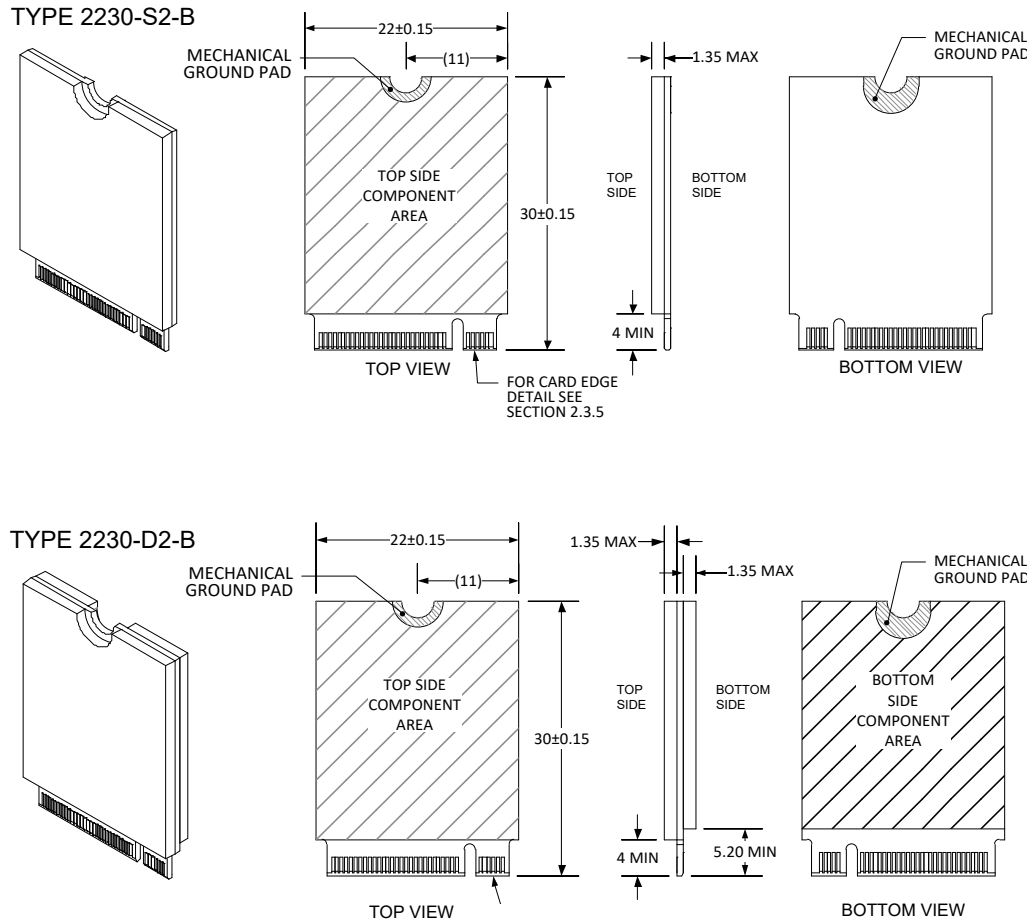
TYPE 2230-D2-B

Note: For card-edge details, see Section 2.3.4.

Figure 2-12. M.2 Type 2230-S2/D2 Mechanical Outline Drawing (Key B example shown)

2.3.3.2. **Type 2242 Specification**

Type 2242 is an M.2 Add-in Card size used on Socket 2 and intended to support SSD solutions and possibly other PCI Express based solutions. In principle, the board is still comprised of two sections:

❑ Host interface section

❑ Active Component section

The active component section including the mounting hole area has an overall length of 38 mm top-side and 36.8 mm bottom side when applicable. Figure 2-13 shows Type 2242 Add-in Card mechanical outline drawing. The SSD Add-in Card takes advantage of the Dual Add-in Card key scheme to enable this Add-in Card to plug into two different SSD-capable Sockets (e.g., Socket 2 and Socket 3).

TYPE 2242-D2-B
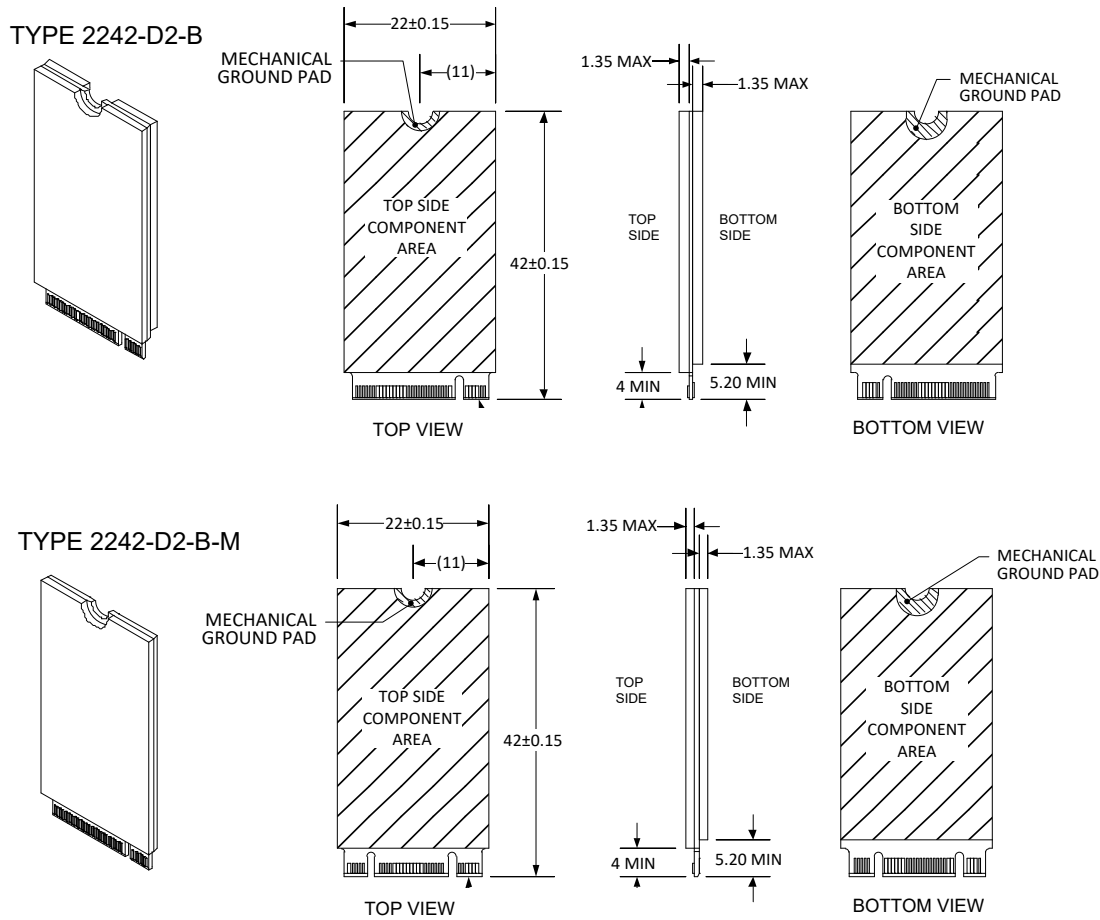
TYPE 2242-D2-B-M

Note: For card-edge details, see Section 2.3.4.

Figure 2-13.   M.2 Type 2242-D2 Mechanical Outline Drawing (Key B and Key B-M examples shown)

2.3.3.3.   **Type 2260 Specification**

Type 2260 Add-in Card is primarily intended to support high-capacity SSD solutions. Figure 2-14 shows an example of Type 2260.

TYPE 2260-D2-M

22±0.15

MECHANICAL
GROUND PAD

(11)

1.35 MAX

1.35 MAX

MECHANICAL
GROUND PAD

TOP
SIDE

BOTTOM
SIDE

TOP SIDE
COMPONENT
AREA

60±0.15

BOTTOM
SIDE
COMPONENT
AREA

4 MIN

5.20 MIN

TOP VIEW

BOTTOM VIEW
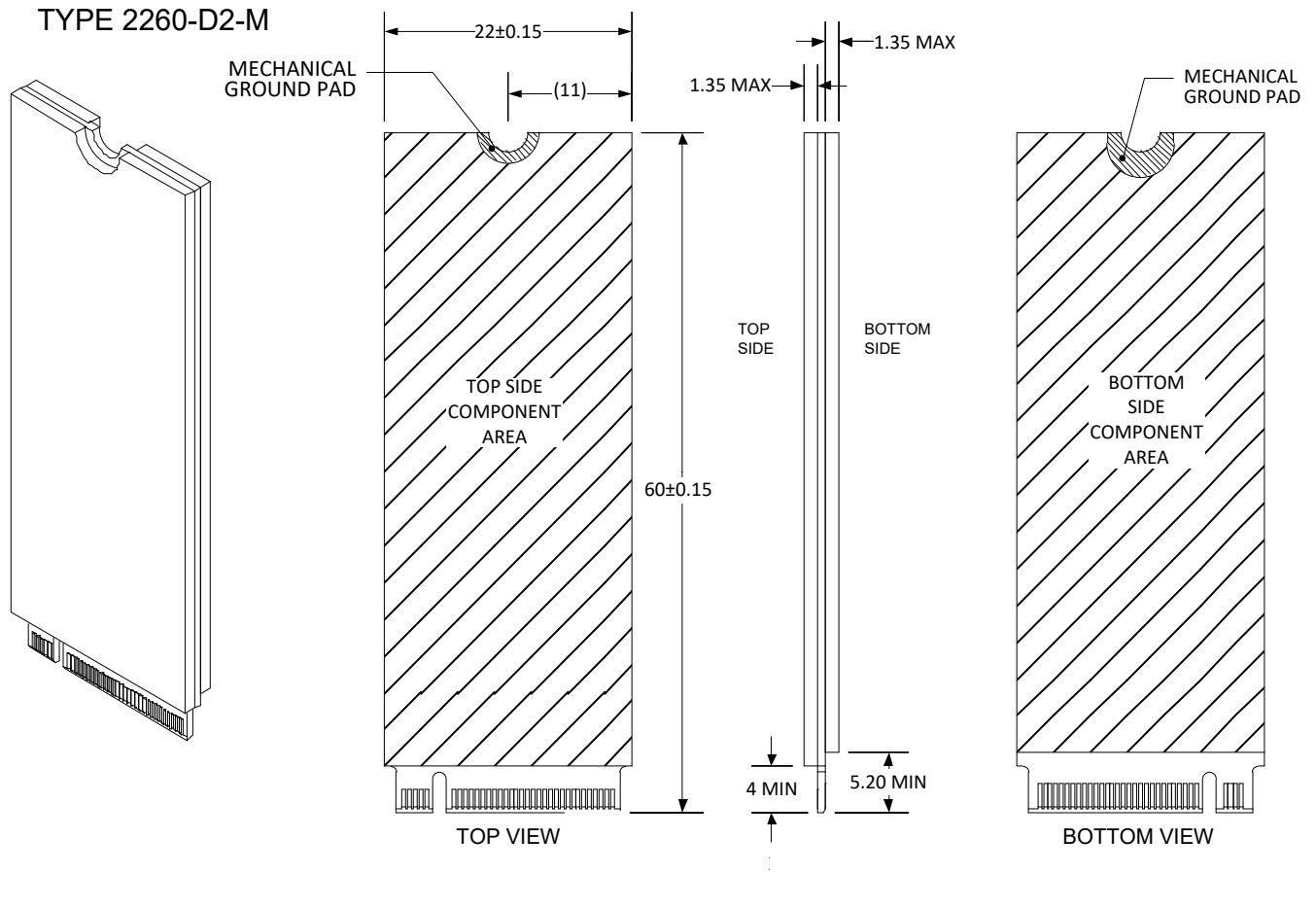
Note: For card-edge details, see Section 2.3.4.

Figure 2-14. M.2 Type 2260-D2 Mechanical Outline Drawing (Key M example shown)

2.3.3.4. **Type 2280 Specification**

Type 2280 Add-in Card type is primarily intended to support high-capacity SSD solutions. Figure 2-15 shows an example of Type 2280.
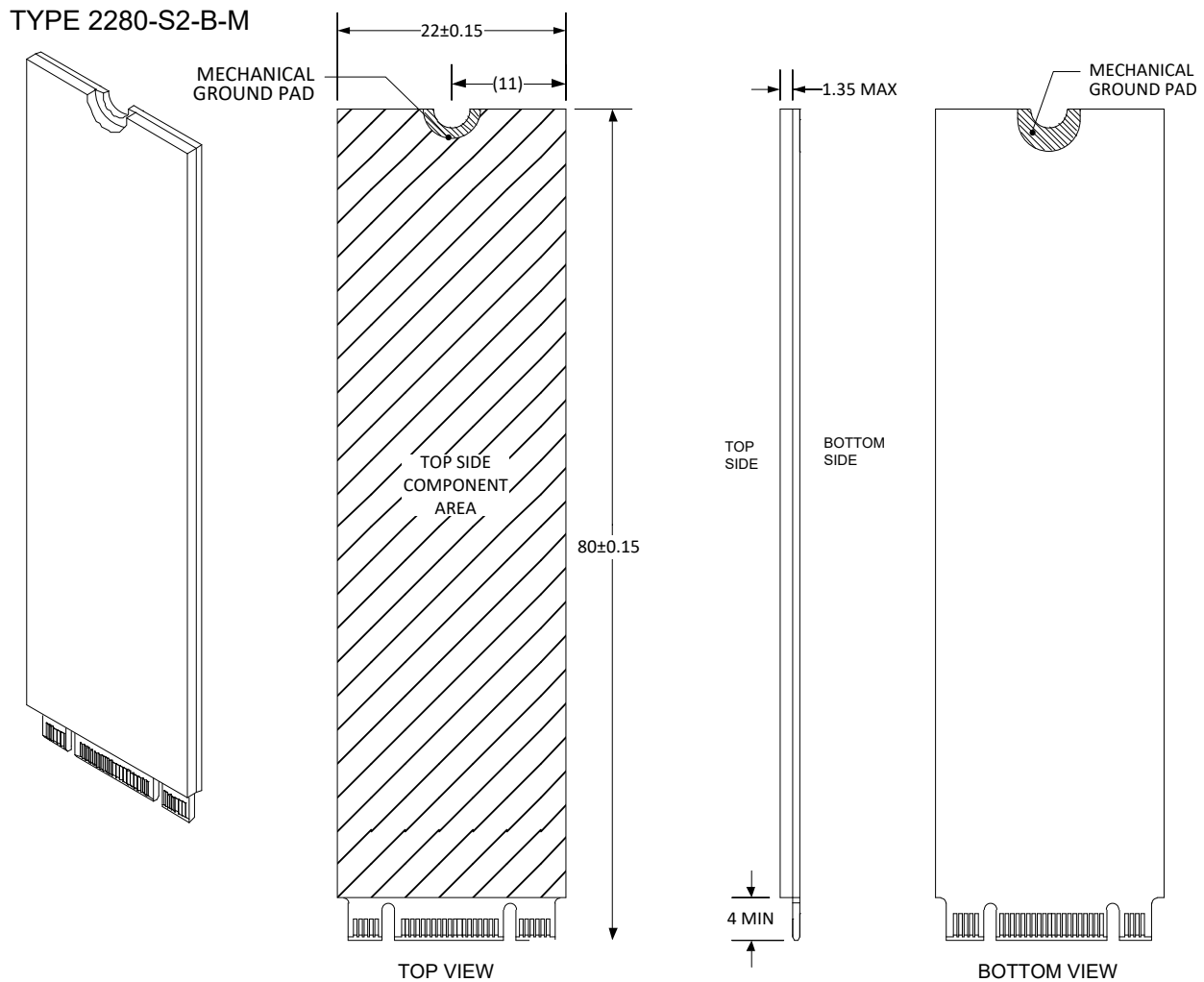
TYPE 2280-S2-B-M

Note: For card-edge details, see Section 2.3.4.

Figure 2-15. M.2 Type 2280-S2 Mechanical Outline Drawing (Key B-M example shown)

2.3.3.5. **Type 22110 Specification**

The Type 22110 Add-in Card type is primarily intended to support high-capacity SSD solutions. Figure 2-16 shows an example of Type 22110.
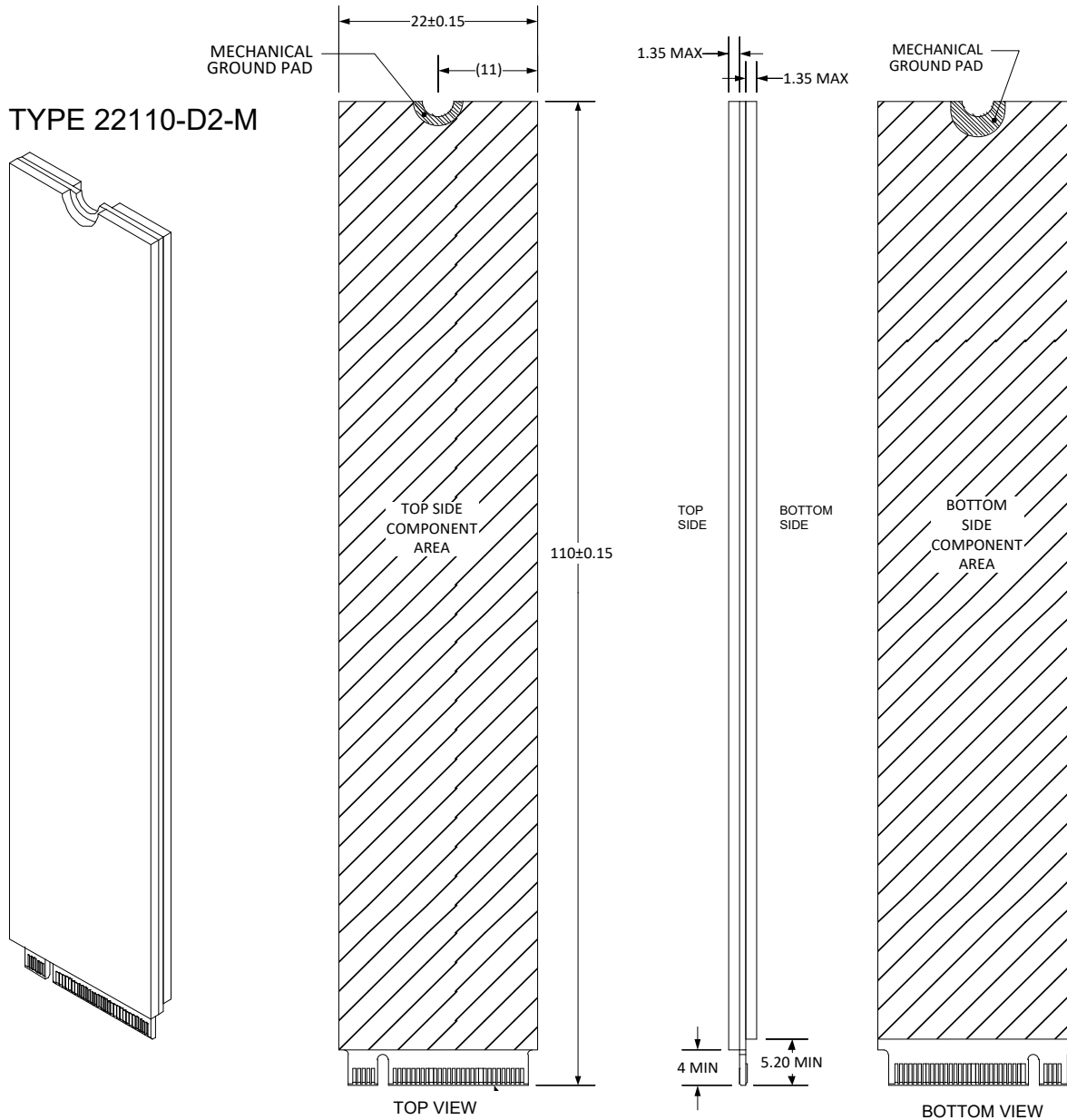
Note: For card-edge details, see Section 2.3.4.

Figure 2-16. M.2 Type 22110-D2 Mechanical Outline Drawing (Key M example shown)

This Add-in Card type is primarily intended to support high-power SSD solutions.

Figure 2-17, Figure 2-18, and Figure 2-19 show examples of Type 22110-D6-M-P. The topside planar surface is intended to maintain a uniform surface with the potential to mount a heat sink. The planar surface can be constructed as a heat spreader. When constructing a heat spreader, a single continuous surface is not required for the heat spreader; this allows thermal decoupling between heat-generating devices. To allow for a variety of heat spreader attachment options, the presence of mounting holes, inserts, or standoffs is permitted. However, any discontinuity in the heat spreader surface should be minimized to ensure thermal performance. GND is the only signal allowed electrical conductivity to the heat spreader, and all other signals must be electrically isolated. The attachment method is outside the scope of this document.
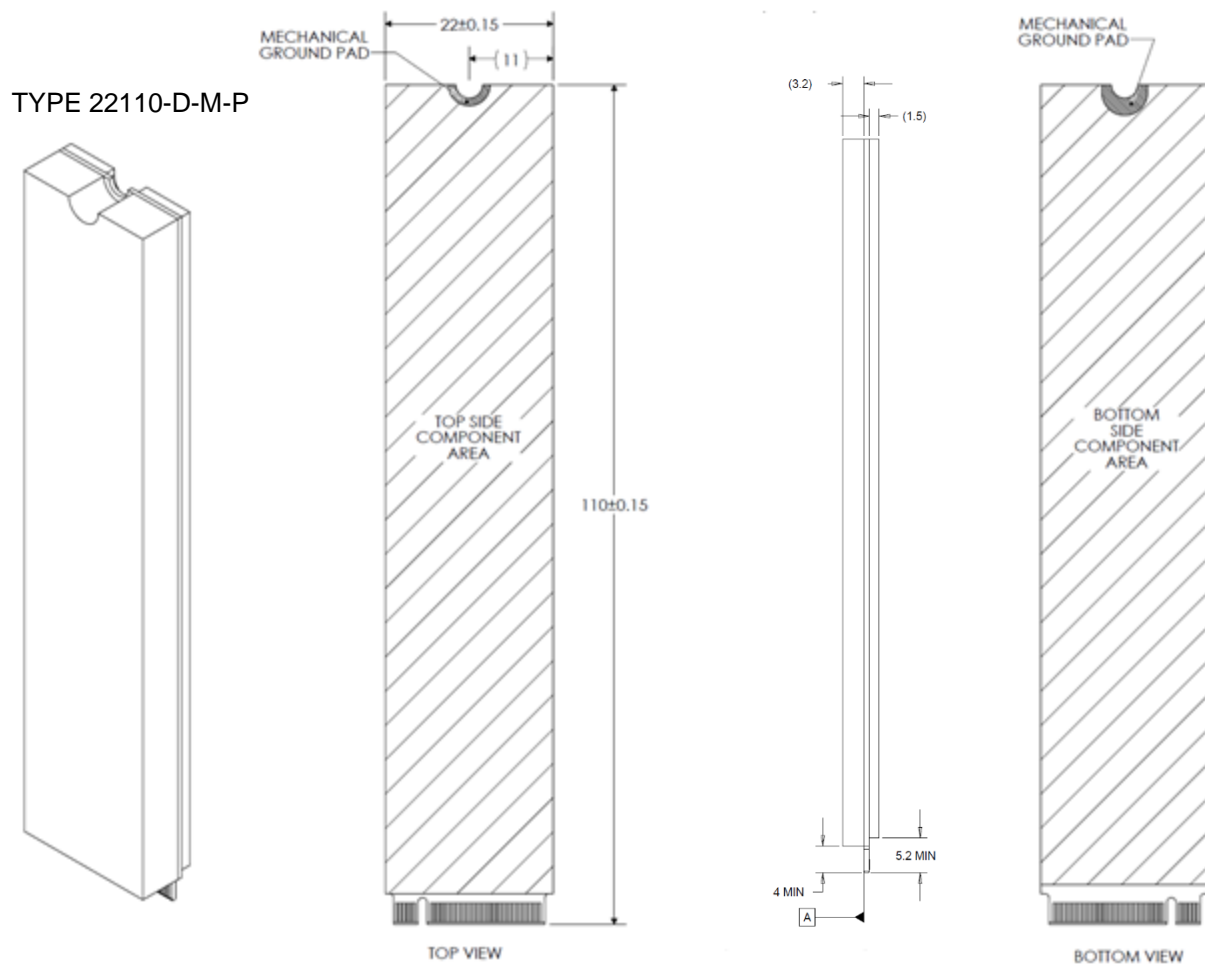
Figure 2-17. Type 22110-D6-M-P Mechanical Outline Drawing
(Key M example shown)
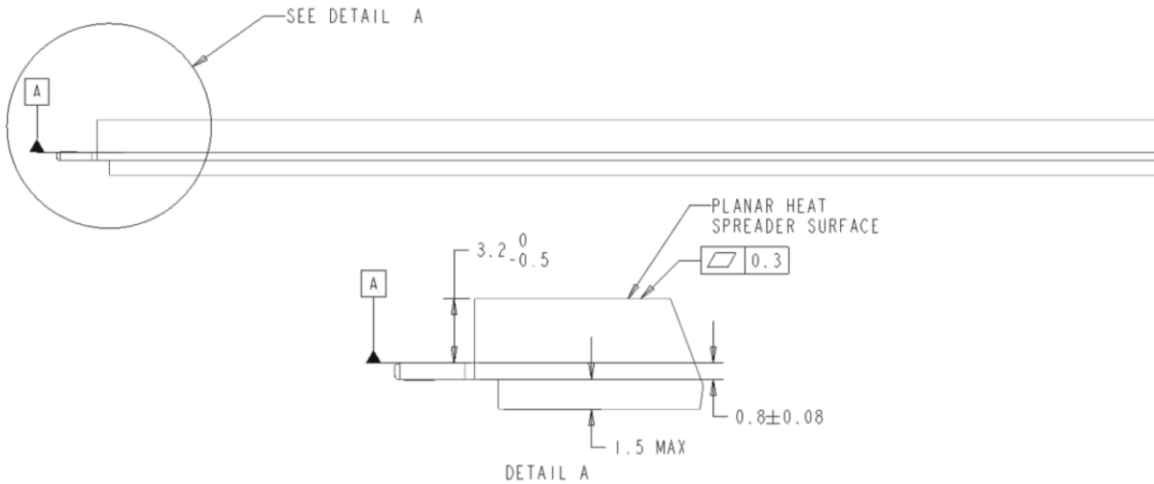
Figure 2-18. Type 22110-D6-M-P Mechanical Card Edge Detail
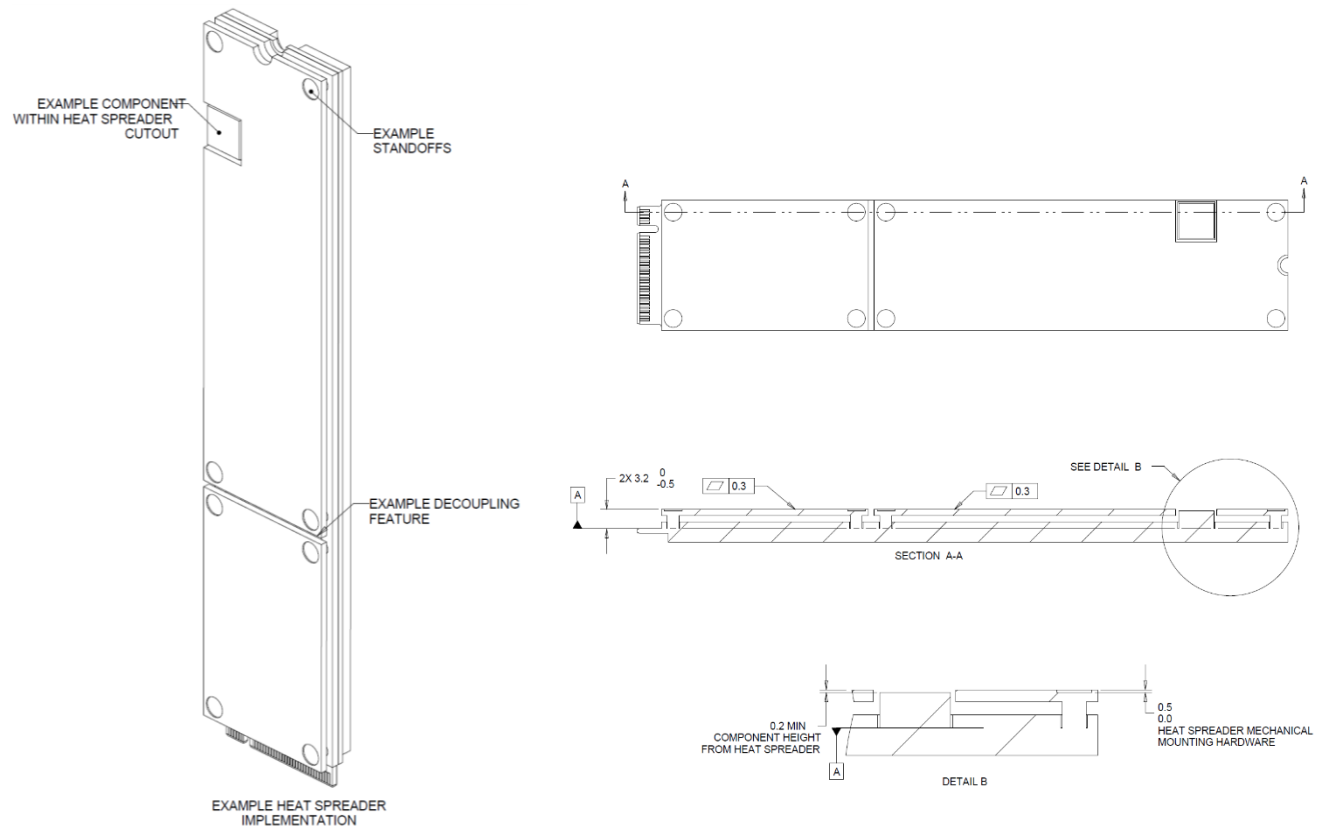
Note: GND is the only signal allowed electrical conductivity to the heat spreader. All other signals shall be electrically isolated.

Figure 2-19. Type 22110-D6-M-P Mechanical Outline Drawing
(Key M example shown)

2.3.3.6.   Type 25110 Specification

This Add-in Card type is primarily intended to support high-power SSD solutions using an optional heatsink. Figure 2-20 shows an example of a Type 25110-D8-M. The top surface is not required to be planar to allow for fin structures.
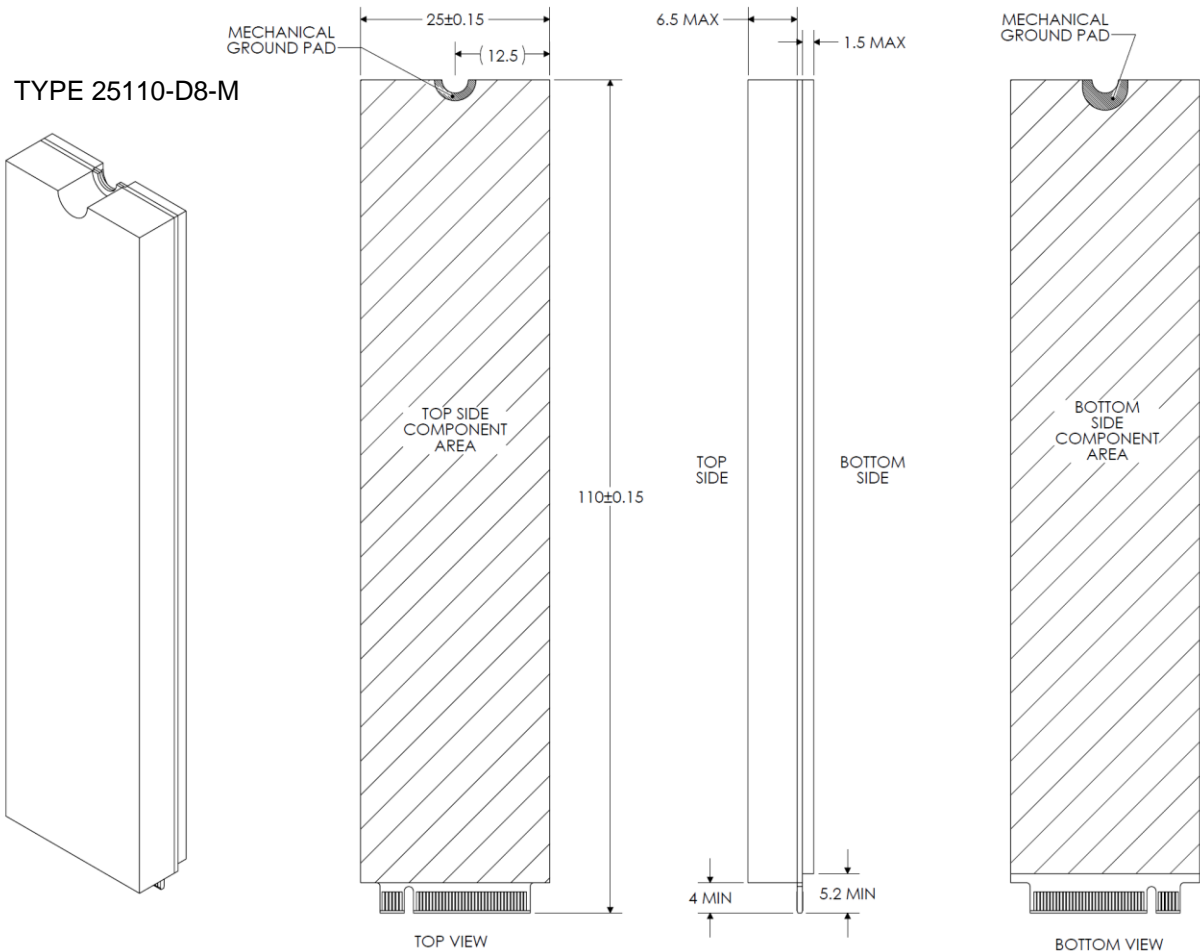
Figure 2-20. Type 25110-D8-M Mechanical Outline Drawing
(Key M example shown)

2.3.4.   Card PCB Details

2.3.4.1.   Mechanical Outline of Card-Edge

Figure 2-21 through Figure 2-35 show typical card-edge mechanical outlines.
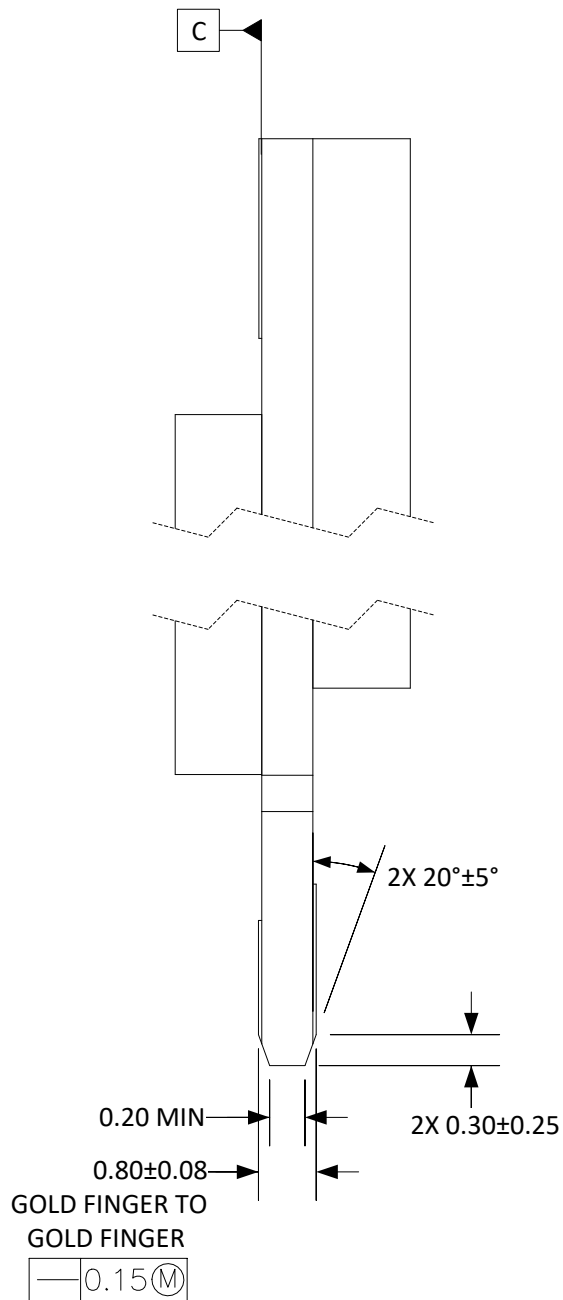
Figure 2-21. Card Edge Bevel
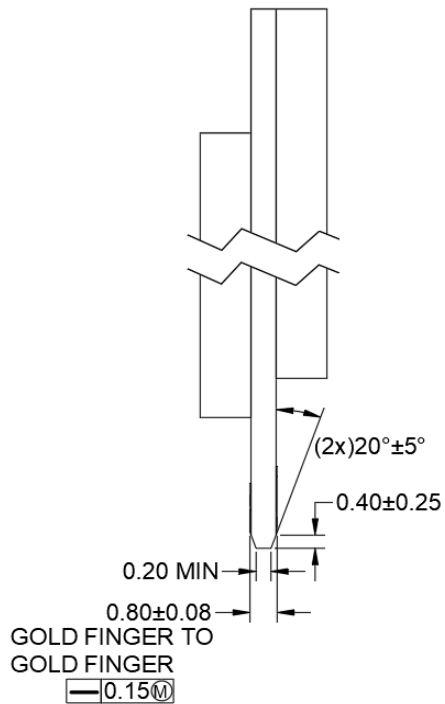
Figure 2-22. M.2-1A(A, B, C, D) Card Edge Bevel
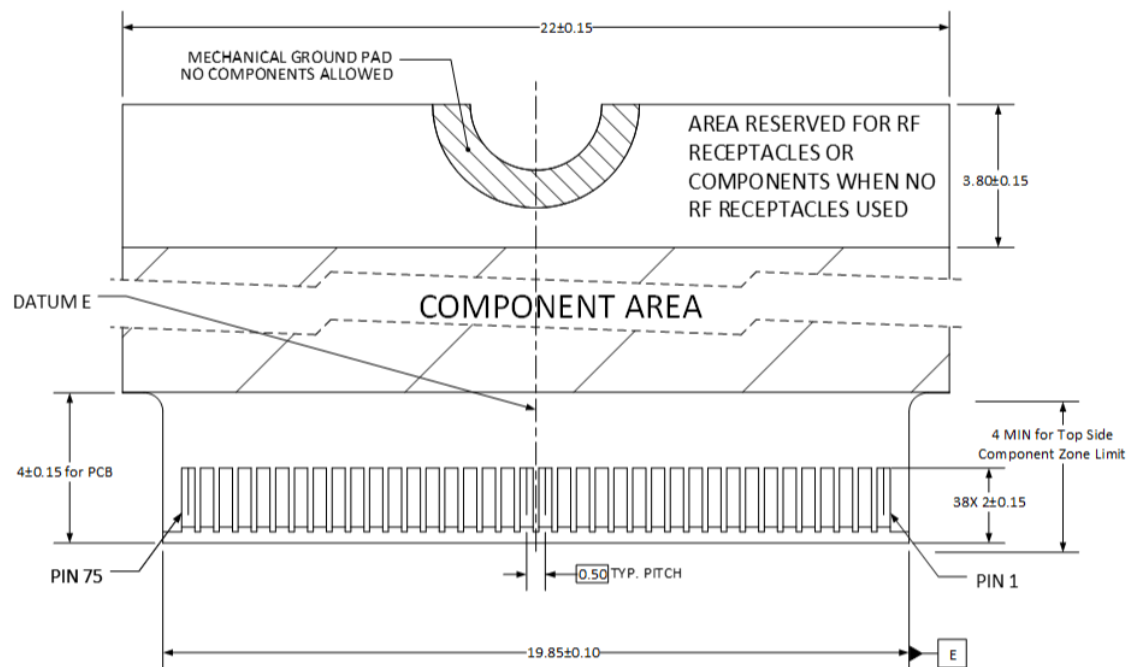
Figure 2-23. Card Edge Outline Topside
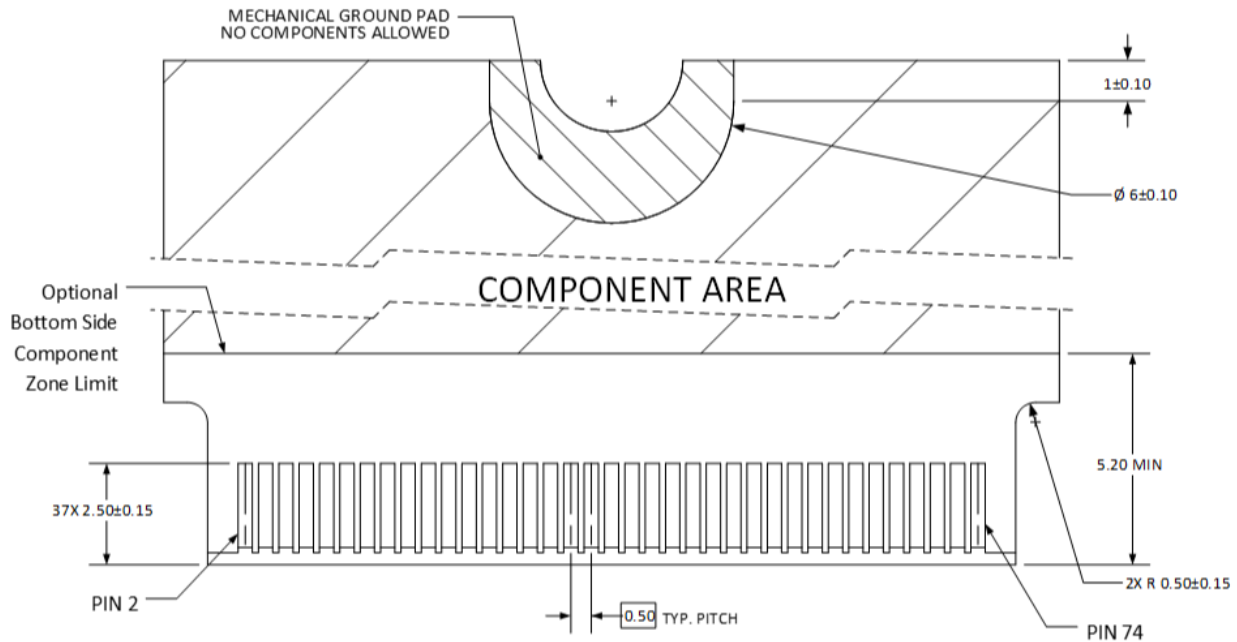
Figure 2-24. Card Edge Outline Bottom-side
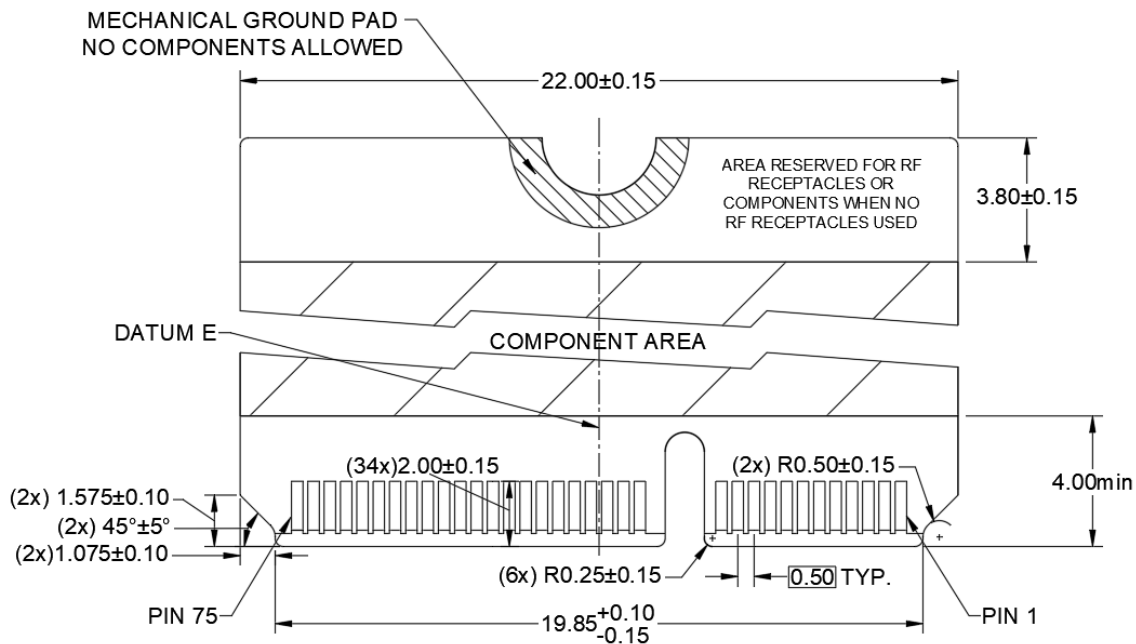
Figure 2-25. M.2 22XXX-XX-X-1A(A) Card Edge Outline Top-side
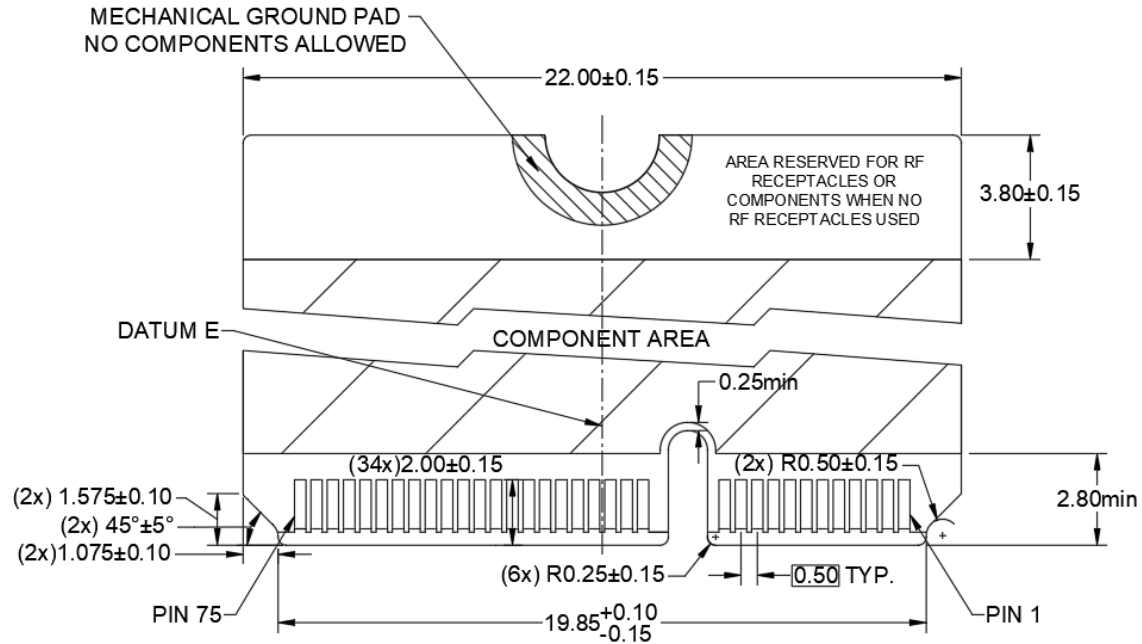
Figure 2-26. M.2 22XXX-XX-X-1A(B) Card Edge Outline Top-side
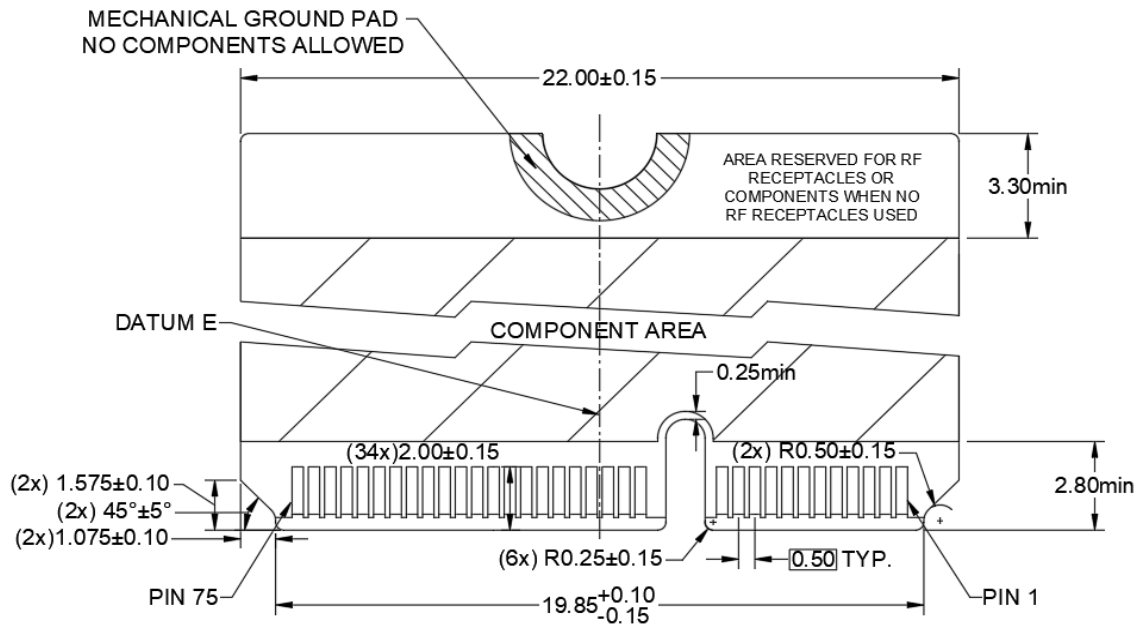
Figure 2-27. M.2 22XXX-XX-X-1A(C) Card Edge Outline Top-side
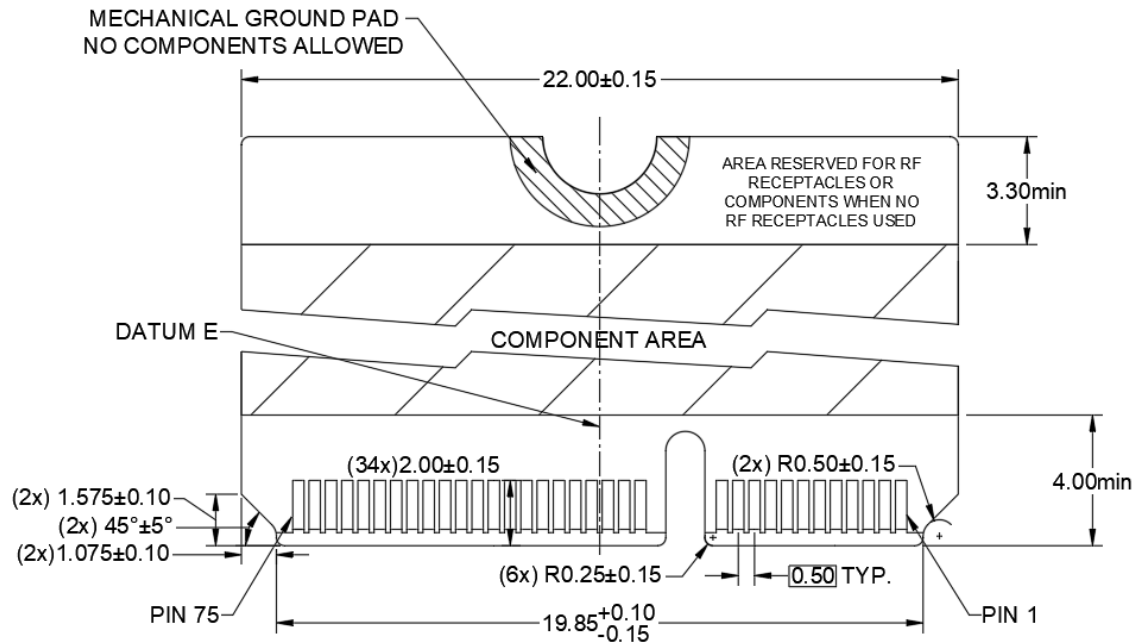
Figure 2-28. M.2 22XXX-XX-X-1A(D) Card Edge Outline Topside
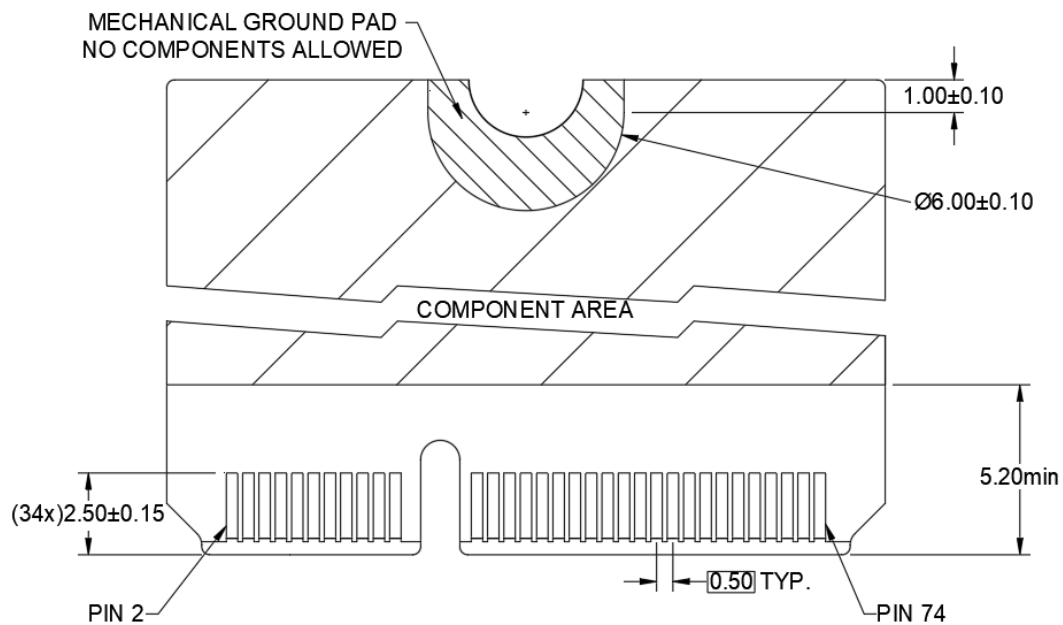
Figure 2-29. M.2 22XXX-XX-X-1A(A, B, C, D) Card Edge Outline Bottom-side
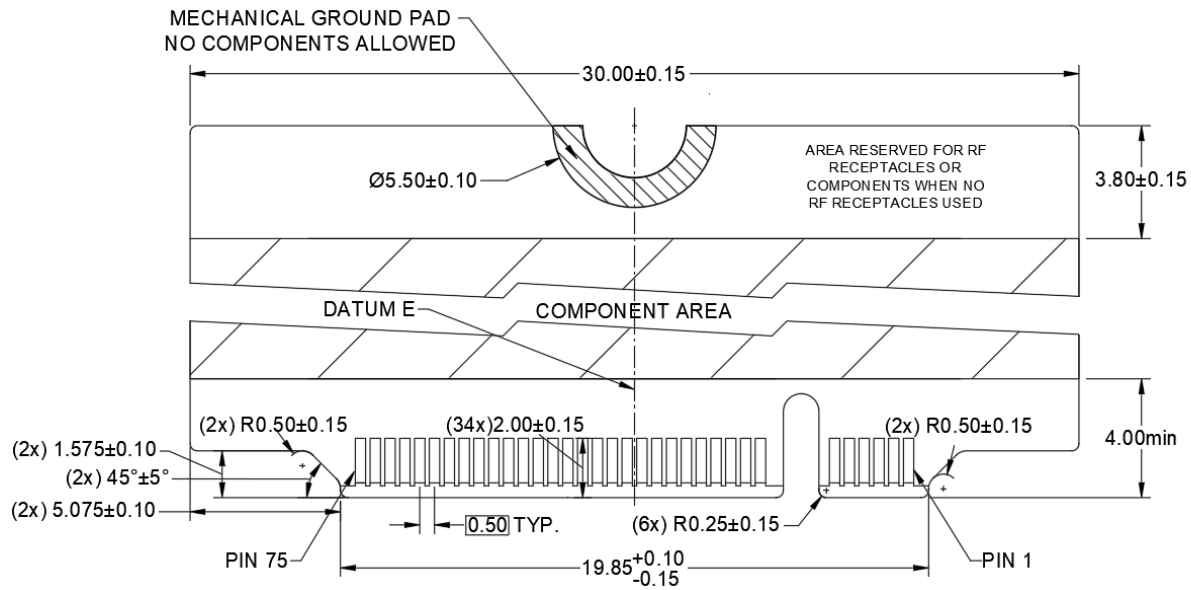
Figure 2-30. M.2 30XXX-XX-X-1A(A) Card Edge Outline Topside
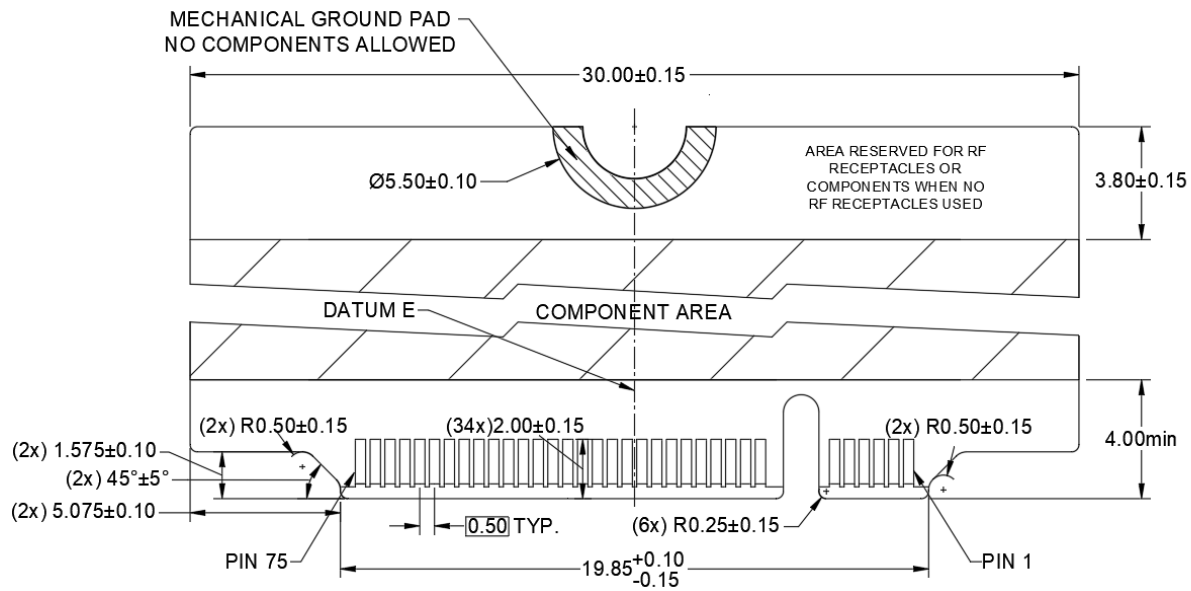
Figure 2-31. M.2 30XXX-XX-X-1A(B) Card Edge Outline Topside
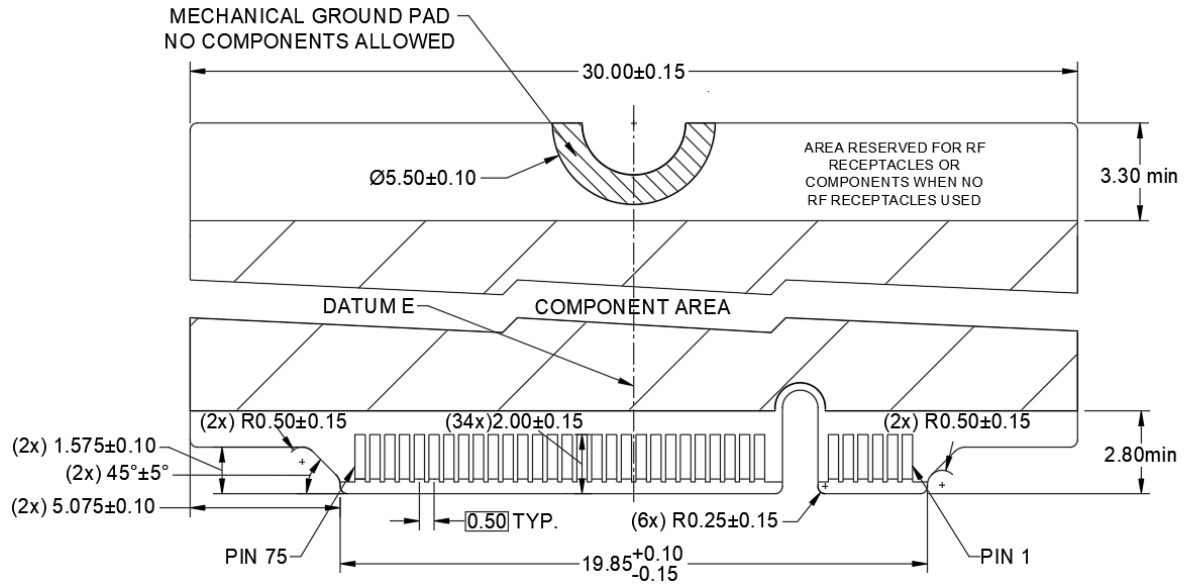
Figure 2-32. M.2 30XXX-XX-X-1A(C) Card Edge Outline Topside
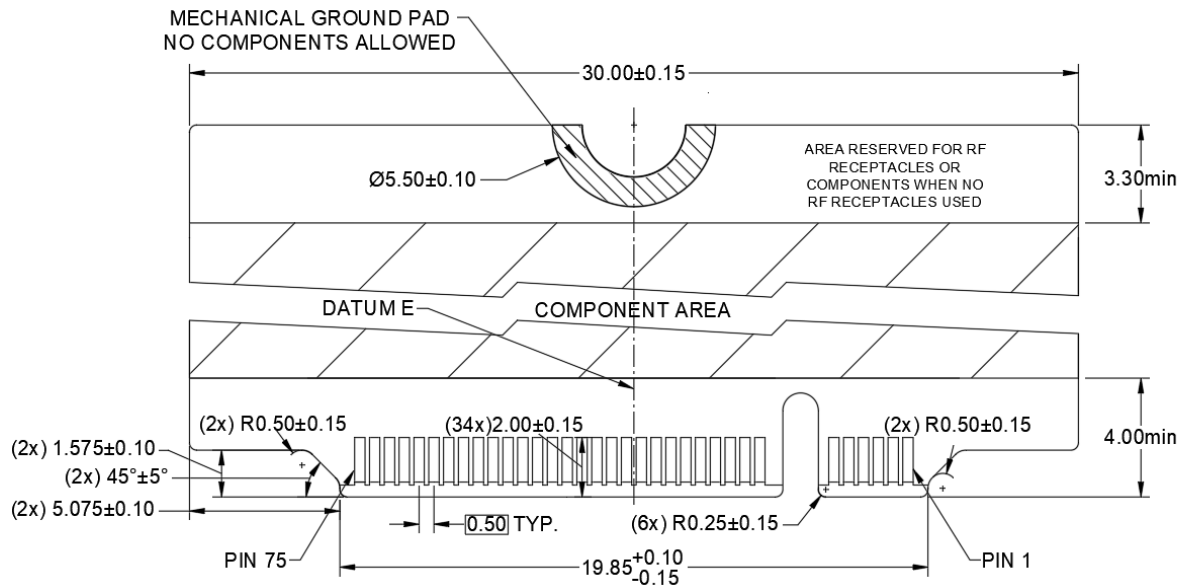
Figure 2-33. M.2 30XXX-XX-X-1A(D) Card Edge Outline Topside
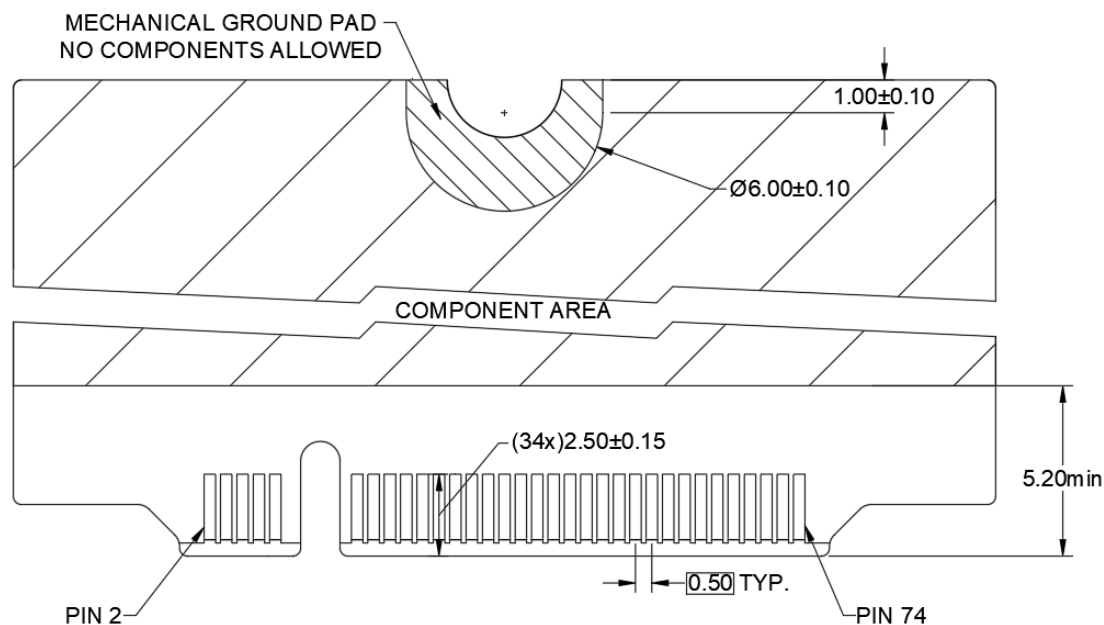
Figure 2-34. M.2-30XXX-XX-X-1A(A, B, C, D) Card Edge Outline
Bottom-side
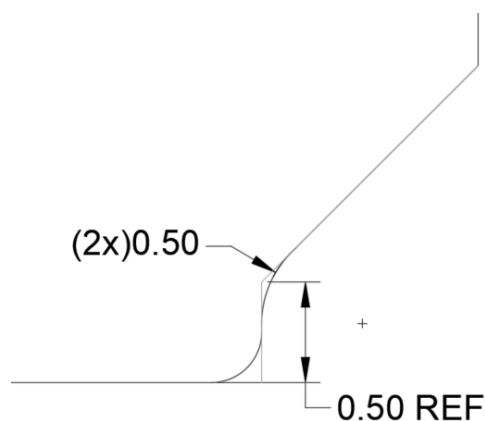
Figure 2-35. M.2-1A(A, B, C, D) Card Edge Outline Side Chamfer

2.3.4.2.   **Add-in Card Keying**

> **Note:** Key G is shown for reference only. This Key is allocated for custom use at one's own risk. It is not used for M.2 spec compliant devices.

Keying is required to provide configurability as well as preventing incompatible Add-in Card insertion. See the following figures and tables for dimensional values.

❑ Table 2-3.   Key Location/Pin Block Dimensions for Keys A to F
❑ Table 2-4.   Key Location/Pin Block Dimensions for Keys G to M
❑ Figure 2-36.   Key Detail for Keys A to F
❑ Figure 2-37.   Key Detail for Keys G to M
❑ Figure 2-38.   Dual Key A-E Example
❑ Figure 2-39.   Dual Key B-M Example

The key locations and pin block dimensions for Keys A to F are listed in Table 2-3. Table 2-4 lists Keys G to M. The key designation identifier should be marked with either Silk Screen, reverse copper etching, or solder mask removal on the Top-side of the Add-in Card to the right of the Add-in Card key, as shown in Figure 2-36 and Figure 2-37. The letter size should be at least 1 mm tall.

Table 2-3.   Key Location/Pin Block Dimensions for Keys A to F

Dimension	Key ID					
	A	B	C	D	E	F
Q	6.625	5.625	4.625	3.625	2.625	1.625
R	1.50	2.50	3.50	4.50	5.50	6.50
S	14.50	13.50	12.50	11.50	10.50	9.50
T	1.00	2.00	3.00	4.00	5.00	6.00
U	14.50	13.50	12.50	11.50	10.50	9.50

Table 2-4.   Key Location/Pin Block Dimensions for Keys G to M

Dimension	Key ID					
	G	H	J	K	L	M
V	1.125	2.125	3.125	4.125	5.125	6.125
W	9.00	10.00	11.00	12.00	13.00	14.00
X	7.00	6.00	5.00	4.00	3.00	2.00
Y	9.00	10.00	11.00	12.00	13.00	14.00
Z	6.50	5.50	4.50	3.50	2.50	1.50

Two Key designation identifiers should be marked when the Add-in Card employs a dual Add-in Card key scheme as shown in Figure 2-37 and Figure 2-38 respectively.
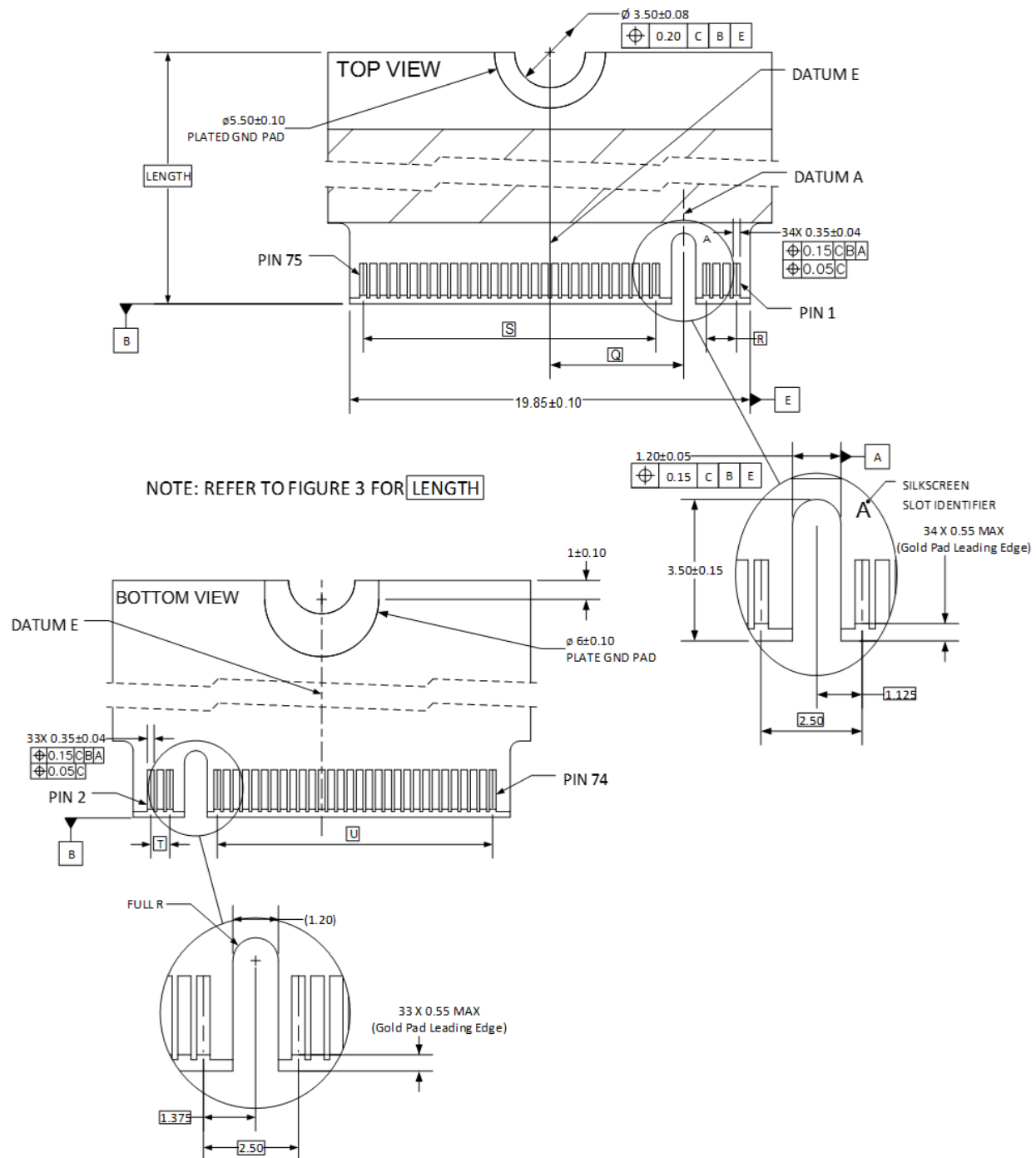
Note: See Figure 2-2 for LENGTH

Figure 2-36. Key Detail for Keys A to F
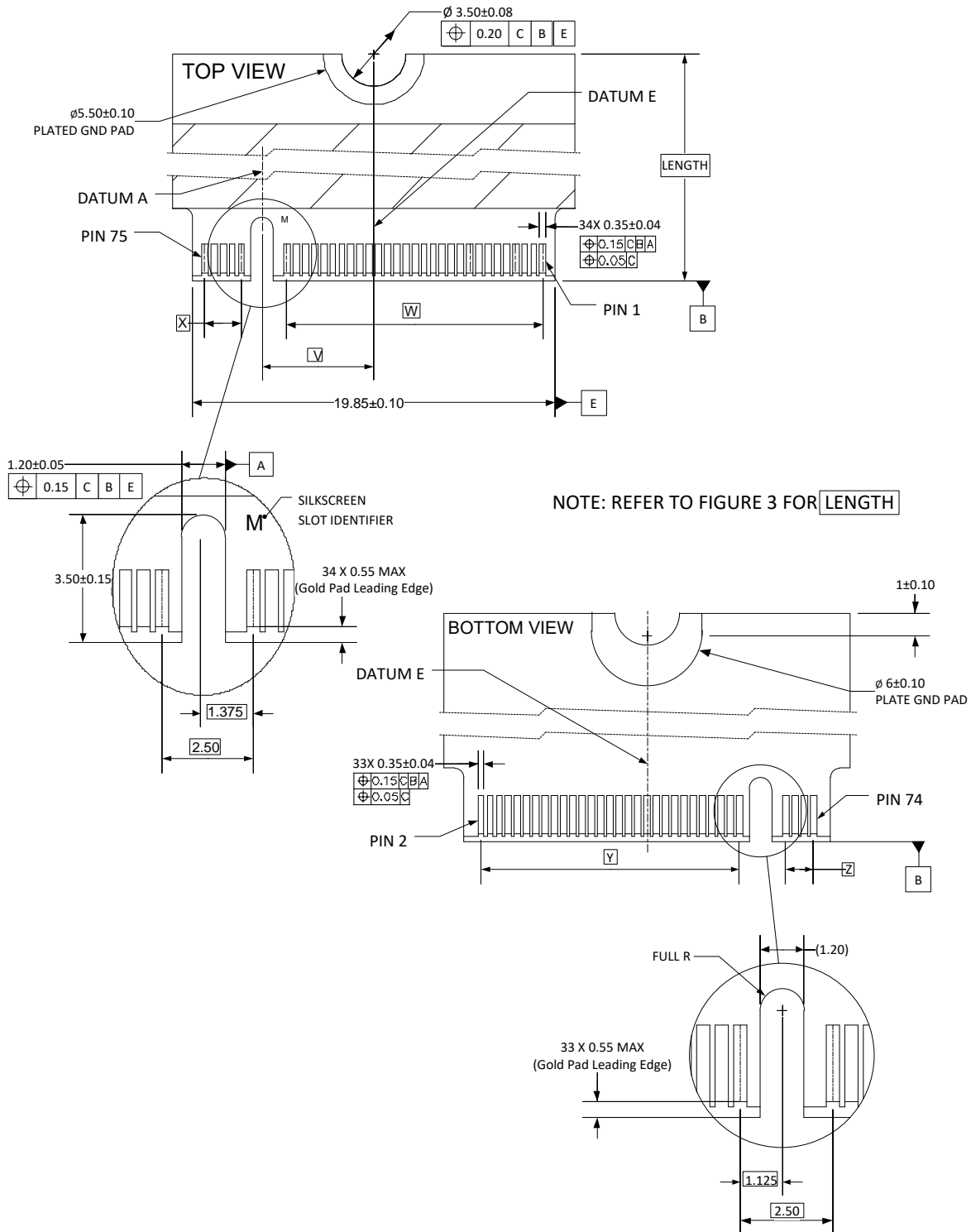
Note: See Figure 2-2 for LENGTH

Figure 2-37. Key Detail for Keys G to M
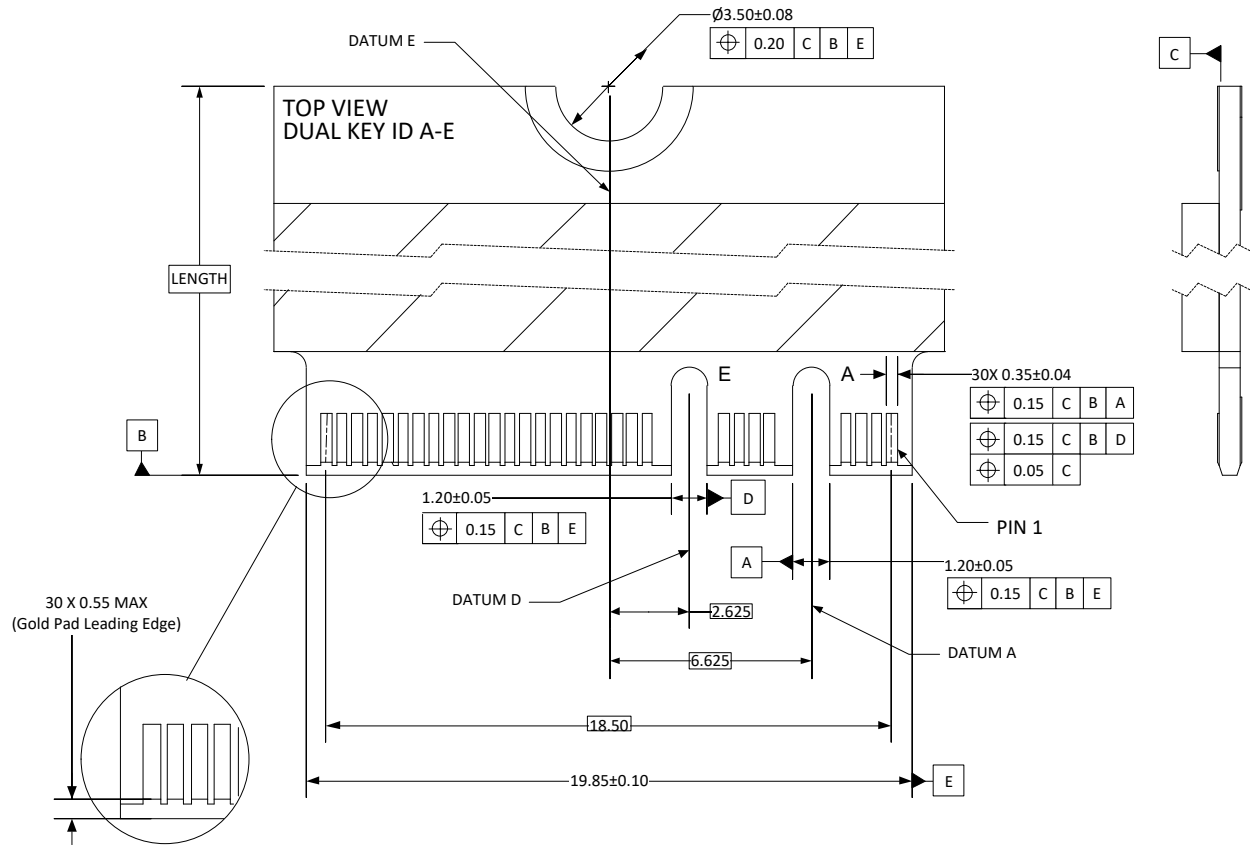
Note: See Figure 2-2 for LENGTH

Figure 2-38. Dual Key A-E Example
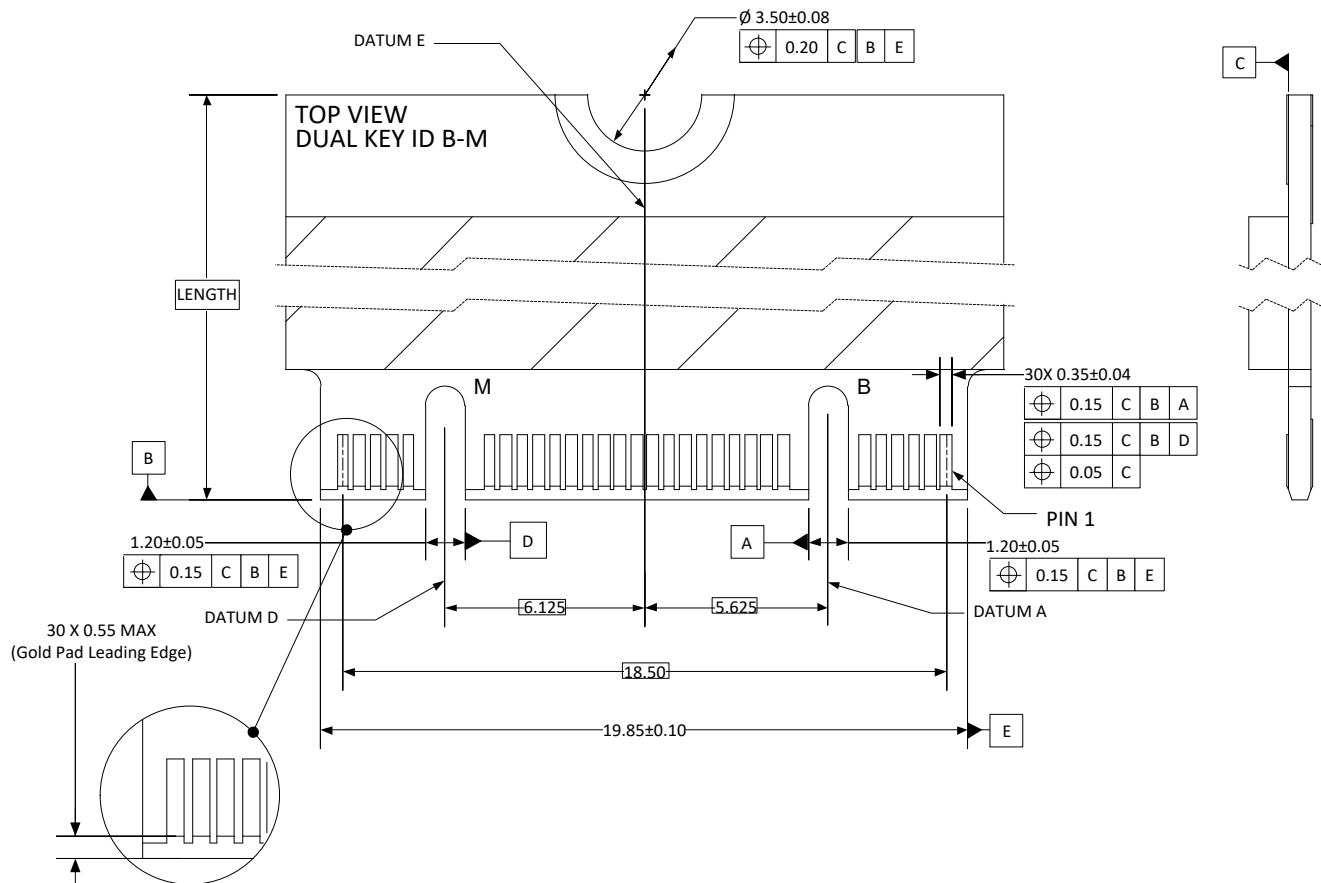
Note: See Figure 2-2 for LENGTH

Figure 2-39. Dual Key B-M Example

2.3.5.   Soldered-down Form Factors

2.3.5.1.   Type 2226 Specification

Type 2226 Module is a soldered-down, single-sided version of Type 2230 Add-in Card. It is therefore assuming the same board technology and silicon package technology. It has an LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. As a result of this, Type 2226 is 4 mm shorter.

To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (e.g., outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 2-40 shows the mechanical outline drawing for Module Type 2226. The recommended land pattern is given in Figure 2-41.

Figure 2-40. M.2 Type 2226-S3 Mechanical Outline Drawing Example
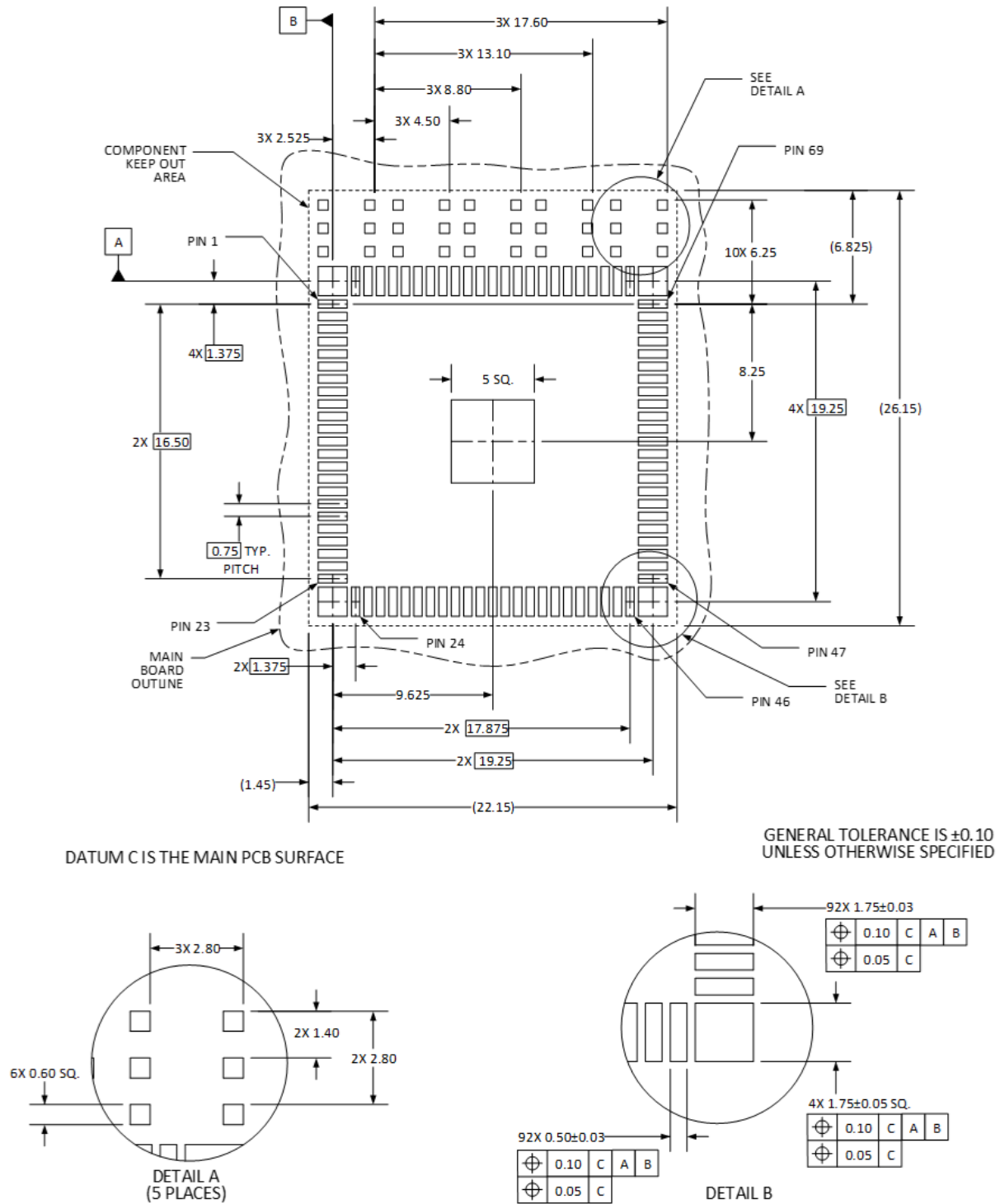
Figure 2-41. Recommended Land Pattern for Module Type 2226

2.3.5.2.　Type 1216 Specification

This Module type is another single-sided soldered-down solution based on a higher density interconnect technology and a smaller silicon package technology. It has an LGA land pattern on the backside and therefore the size is smaller.

To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (e.g., outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 2-42 shows the mechanical outline drawing for Module Type 1216. The recommended land pattern is given in Figure 2-43.
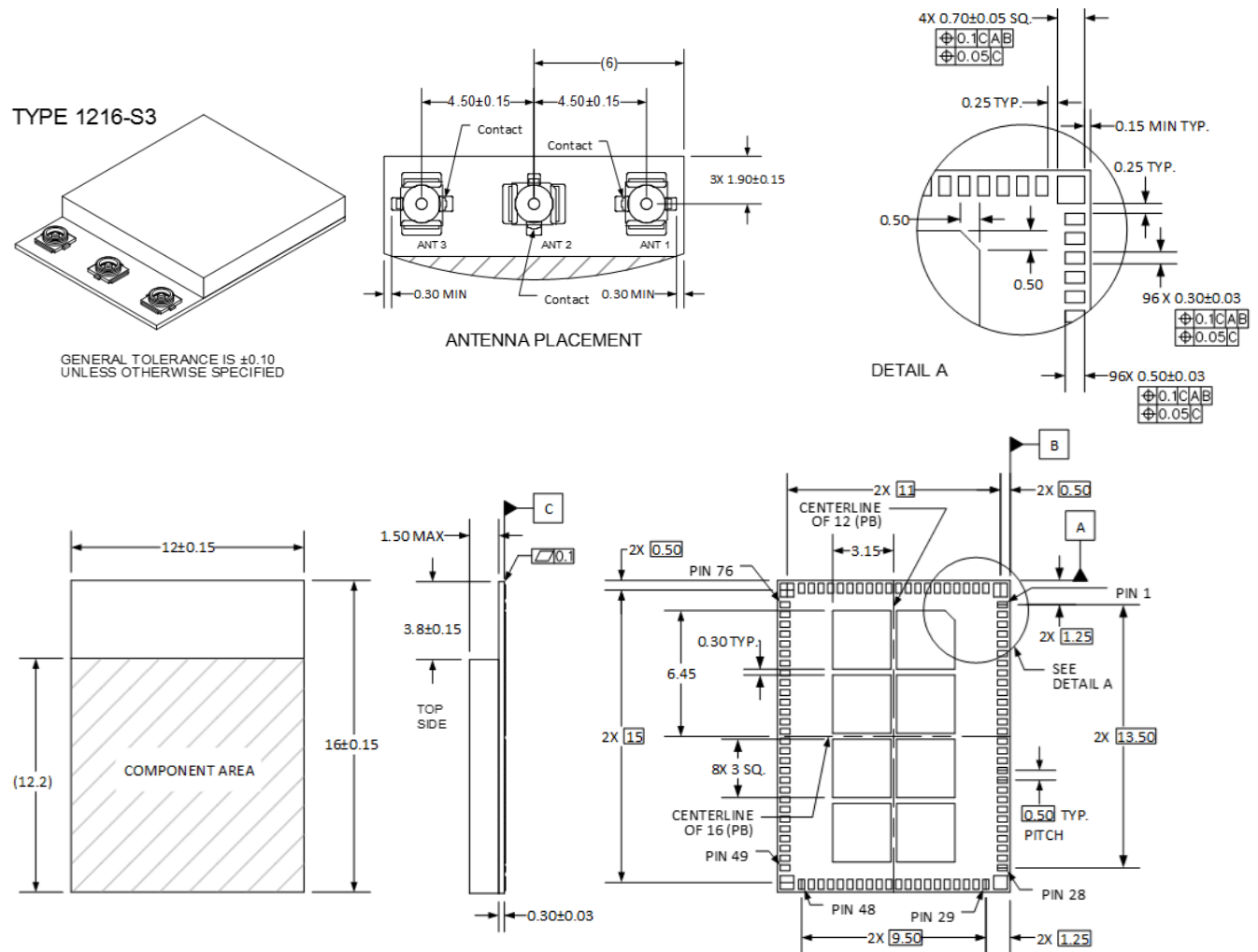
Figure 2-42.　M.2 Type 1216-S3 Mechanical Outline Drawing Example
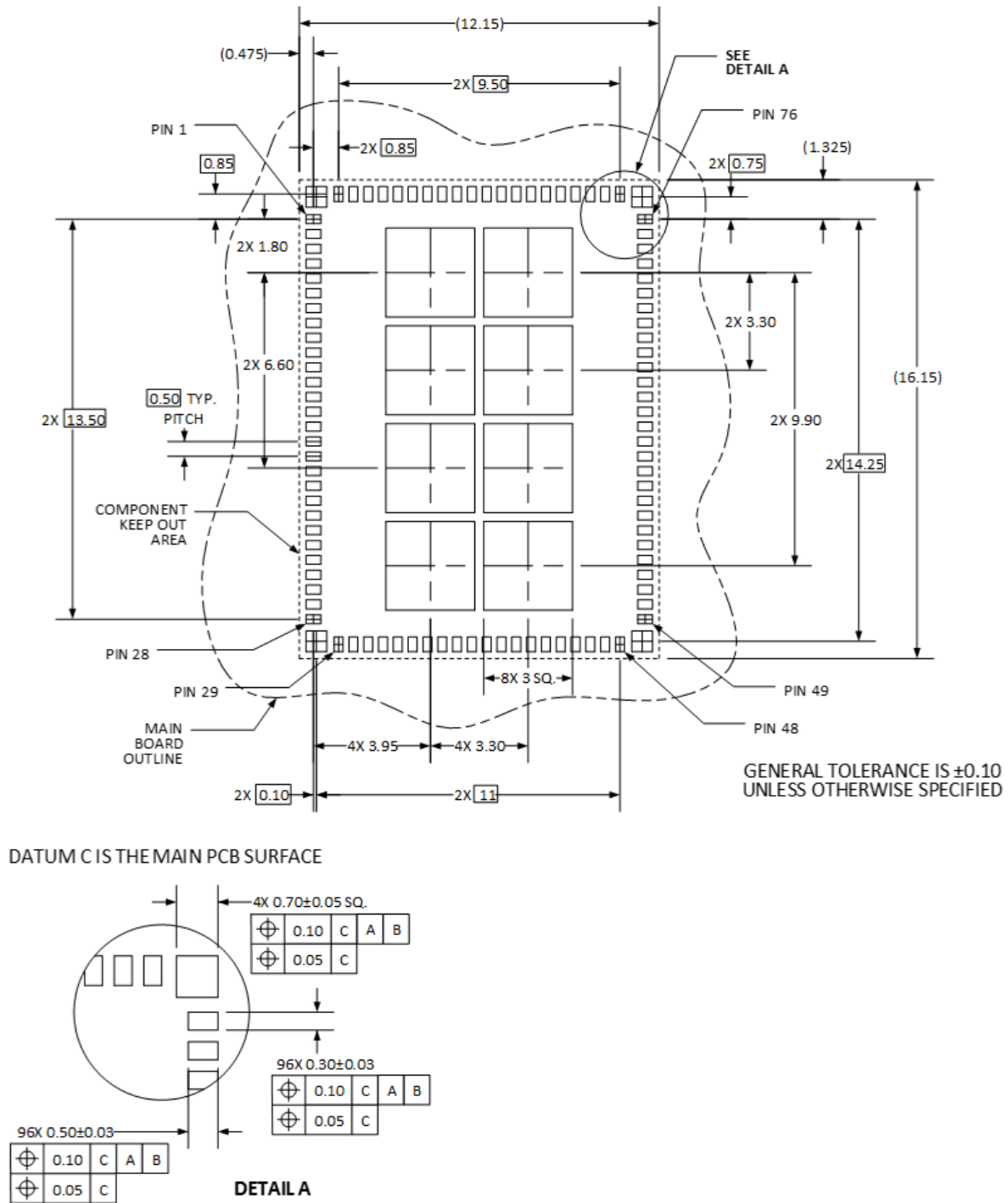
Figure 2-43. Recommended Land Pattern for Module Type 1216

2.3.5.3. Type 3026 Specification

This Module type is a single-sided soldered-down version of the Type 3030 Add-in Card and assumes the same board and silicon package technology. It has a unique LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. This LGA pattern accommodates a Type 2226 Module as a drop-in replacement located at the center with two sets of LGA pads along the sides that cover the entire 3026 Module size. Like the Type 2226 Module, the Module size is also 4 mm shorter than the Add-in Card version.

To help prevent the Module from warping, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (e.g., outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 2-44 shows the mechanical outline drawing for Module Type 3026. See Figure 2-45 for more detailed information. The recommended land pattern is given in Figure 2-46.
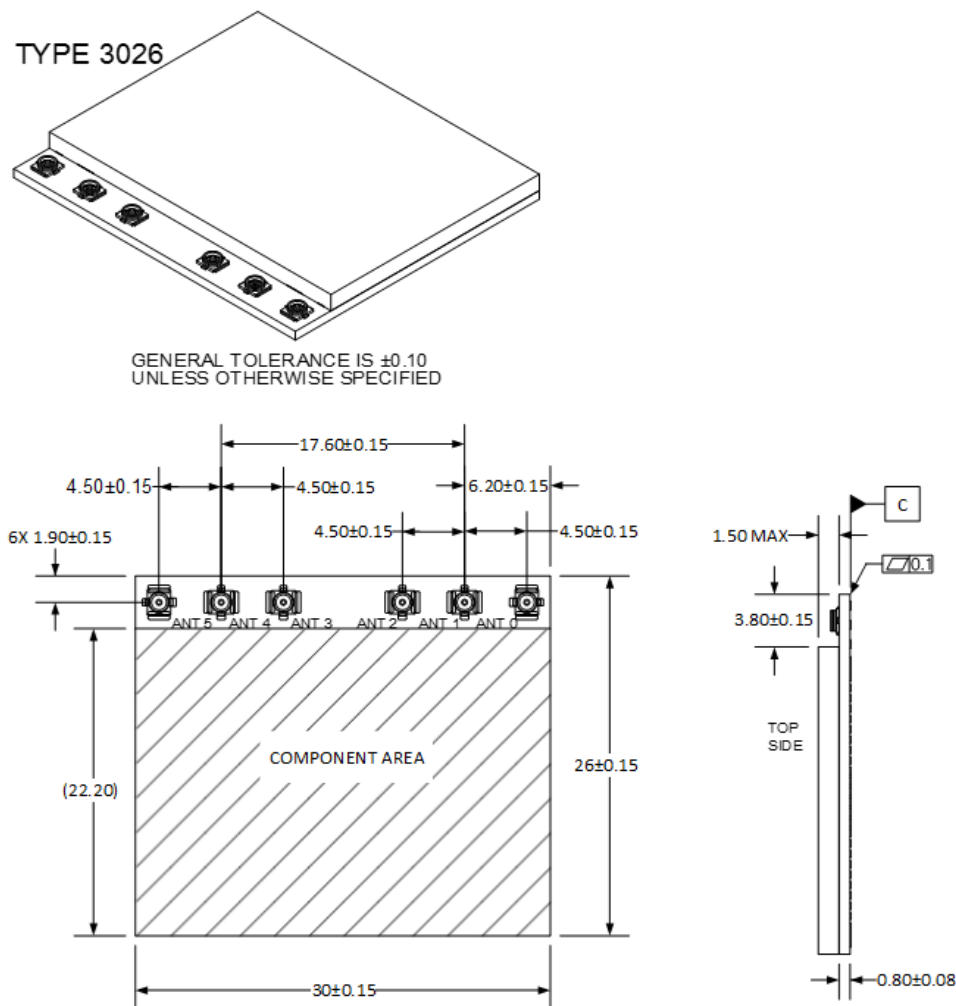
Figure 2-44. M.2 Type 3026-S3 Mechanical Outline Drawing Example
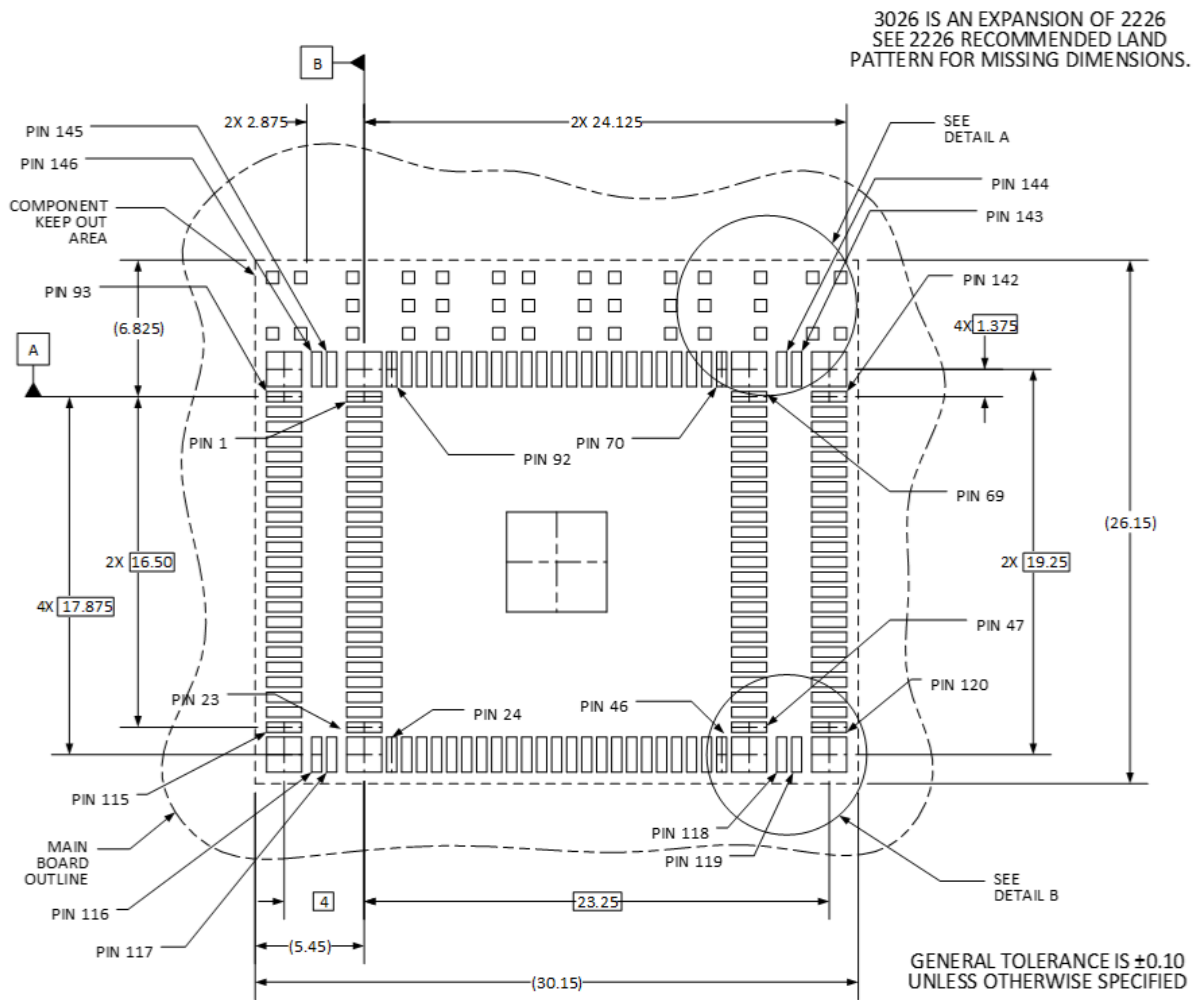
Figure 2-45. M.2 Type 3026-S3 Mechanical Outline Drawing Details Example
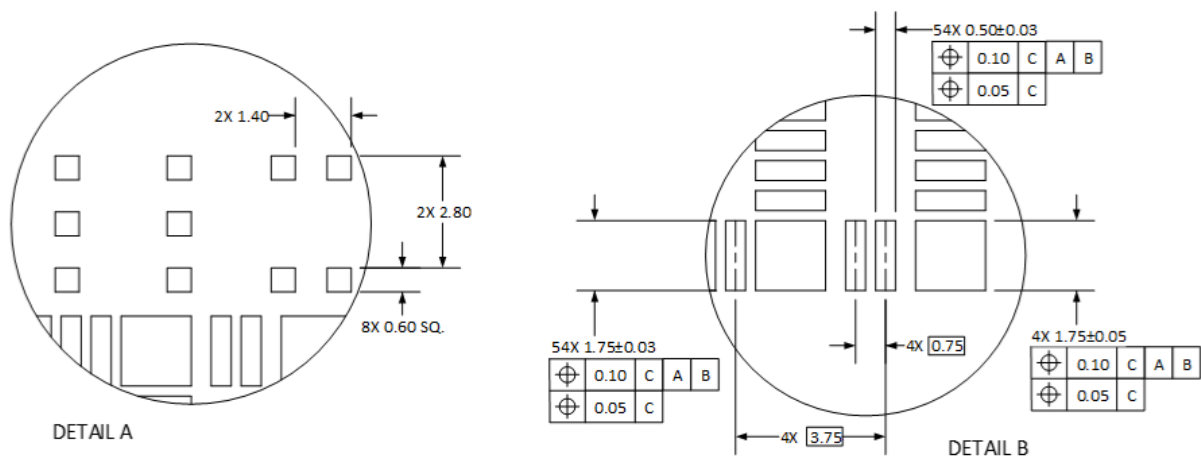
Figure 2-46. Recommended Land Pattern for Module Type 3026

2.3.6. Soldered-Down Form Factors for BGA SSDs

Following different sizes are defined for the soldered-down BGA SSDs:

- ❑ Type 1113
- ❑ Type 1620
- ❑ Type 2024
- ❑ Type 2228
- ❑ Type 2828

All these types are soldered-down and single-sided. They have a BGA land pattern on the backside.

To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (e.g., outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

The target differential impedance of the PCIe and SATA signals on the package is 85 Ω. Differential coupling from other signals must be reduced to ensure signal integrity of the differential pair.

2.3.6.1. Type 1113 Specification

The BGA package size of 11.5 mm x 13 mm contains the ball map for Type 1113.

Figure 2-47 shows the mechanical outline drawing for BGA Type 1113 and Figure 2-48 shows a recommended land pattern for the Type 1113 package. The dimensions shown in Figure 2-48 are nominal.
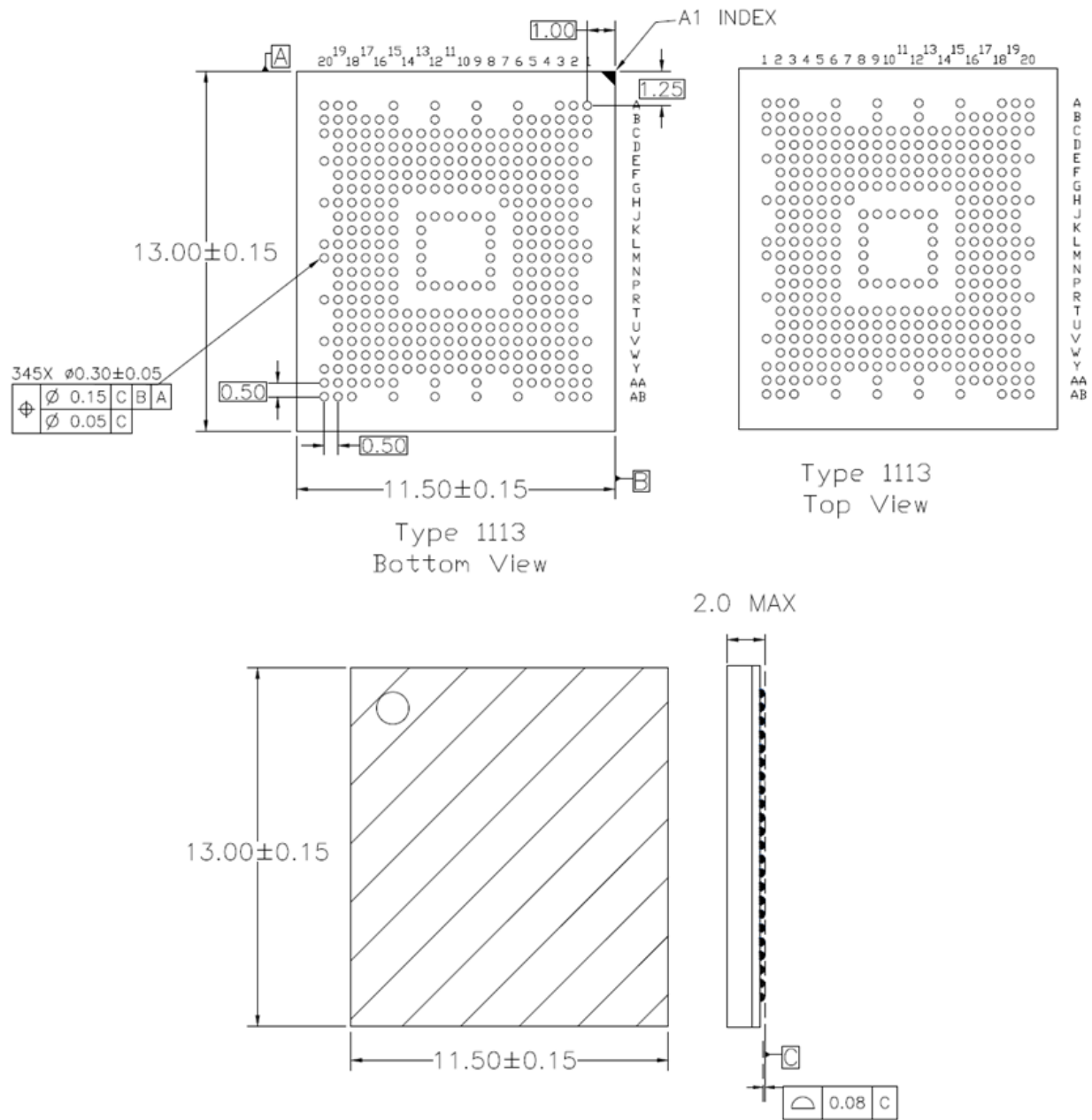
Figure 2-47. M.2 Type 1113-S5 Mechanical Outline Drawing Example

BALL A1

345X ⌀0.30

11.50

13.00

1.25

0.50

0.50

1.00
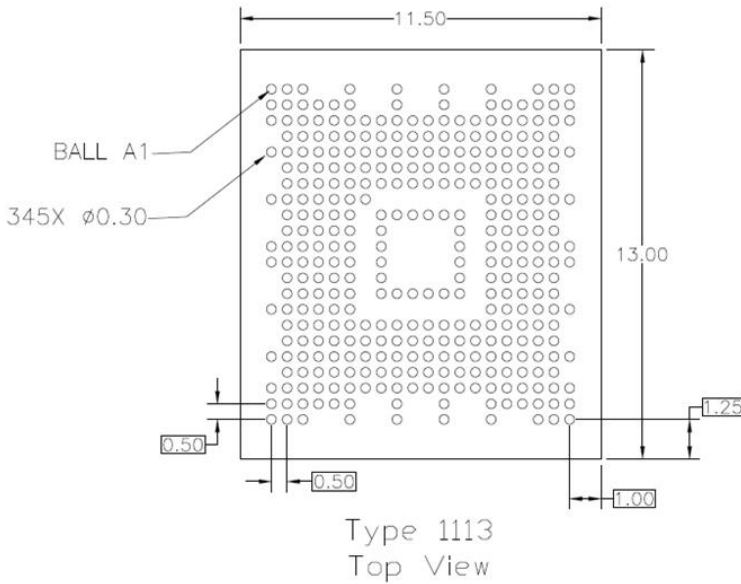
Type 1113
Top View

Figure 2-48. Recommended Land Pattern for M.2 Type 1113 BGA (Top View)

2.3.6.2.   Type 1620 Specification

BGA package sizes of 2024, 2228, and 2828 contain the common core ball map of Type 1620. The larger packages of Type 2024, Type 2228, and Type 2828 have retention balls in addition to the core Type 1620 ball map.

Figure 2-49 shows the mechanical outline drawing for BGA Type 1620 and Figure 2-50 shows a recommended land pattern for Type 1620 package. The dimensions shown in Figure 2-50 are nominal.
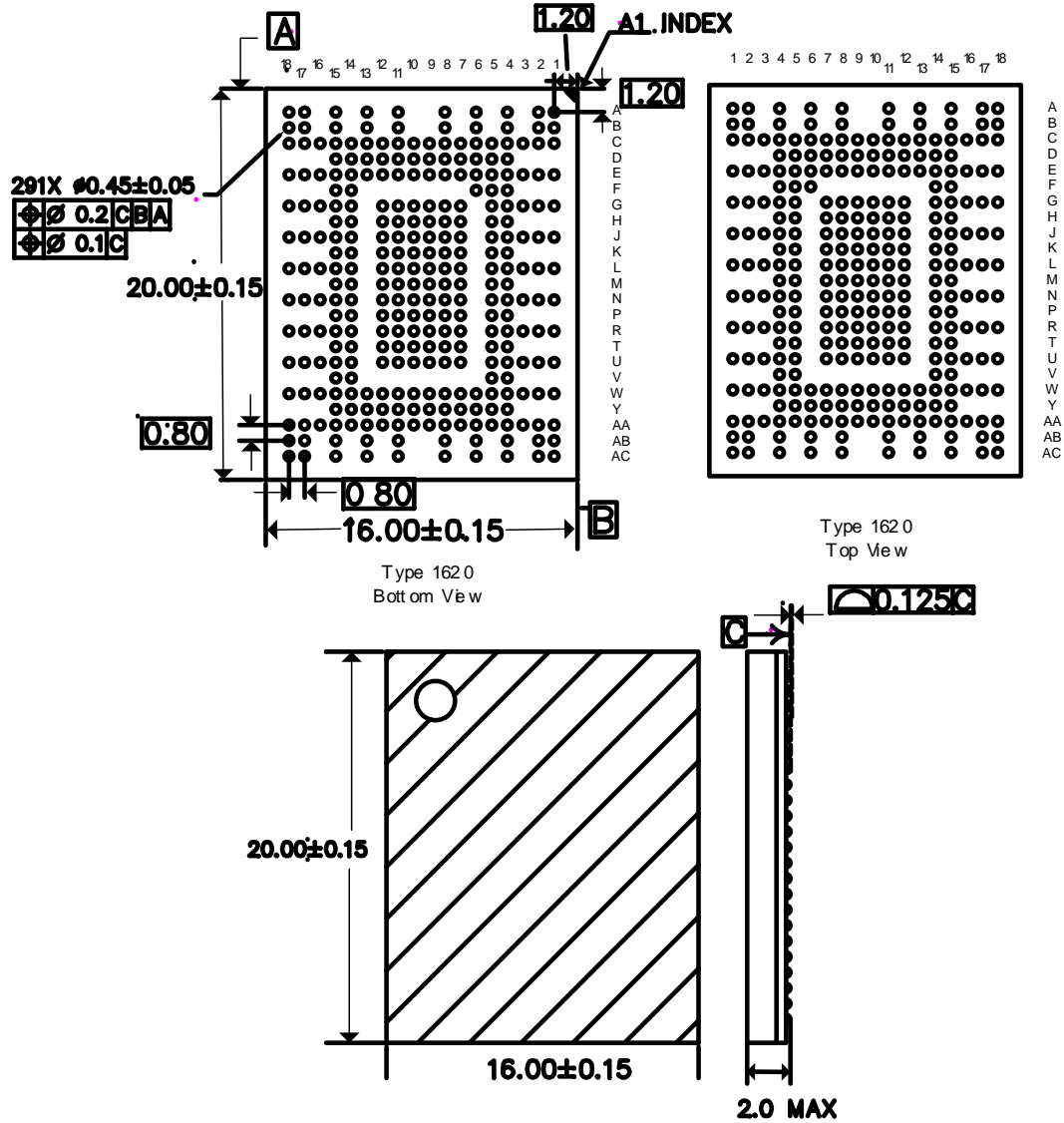
Figure 2-49. M.2 Type 1620-S5 Mechanical Outline Drawing Example
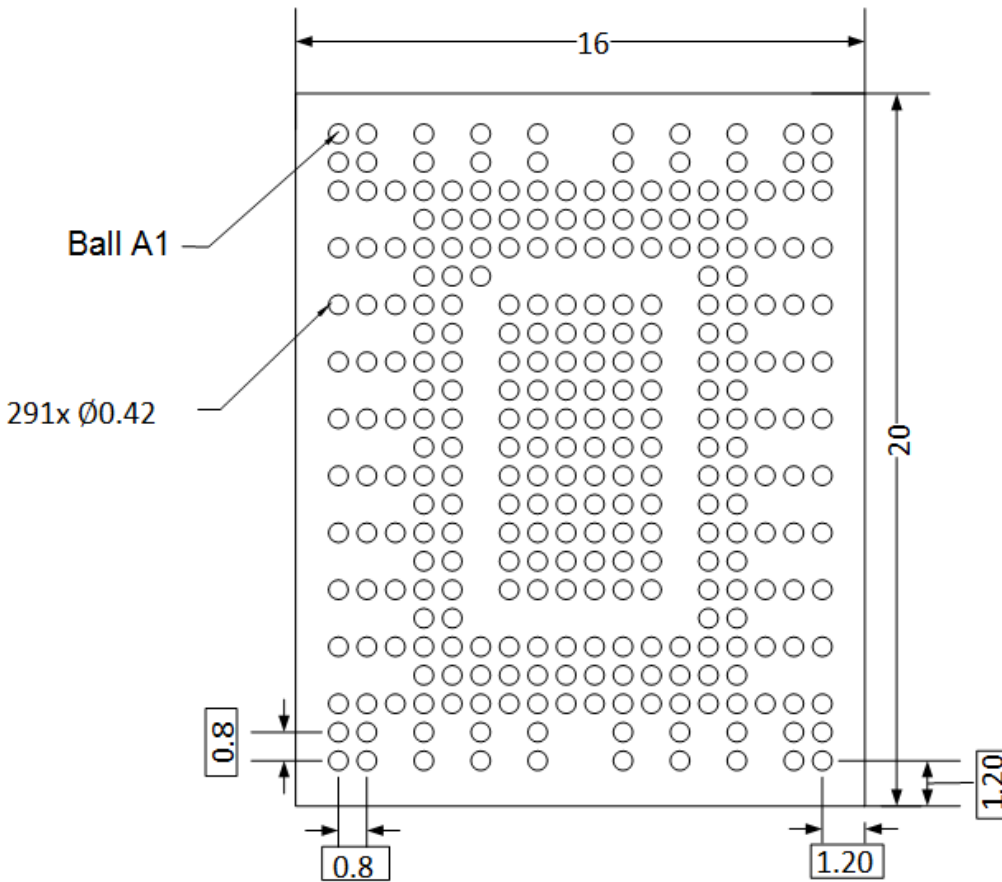
Figure 2-50. Recommended Land Pattern for M.2 Type 1620 BGA (Top View)

2.3.6.3.   Type 2024 Specification

Figure 2-51 shows an example of the M.2 Type 2024-S5 mechanical outline drawing and Figure 2-52 shows a recommended land pattern for the Type 2024 package (dimensions shown in this figure are nominal).
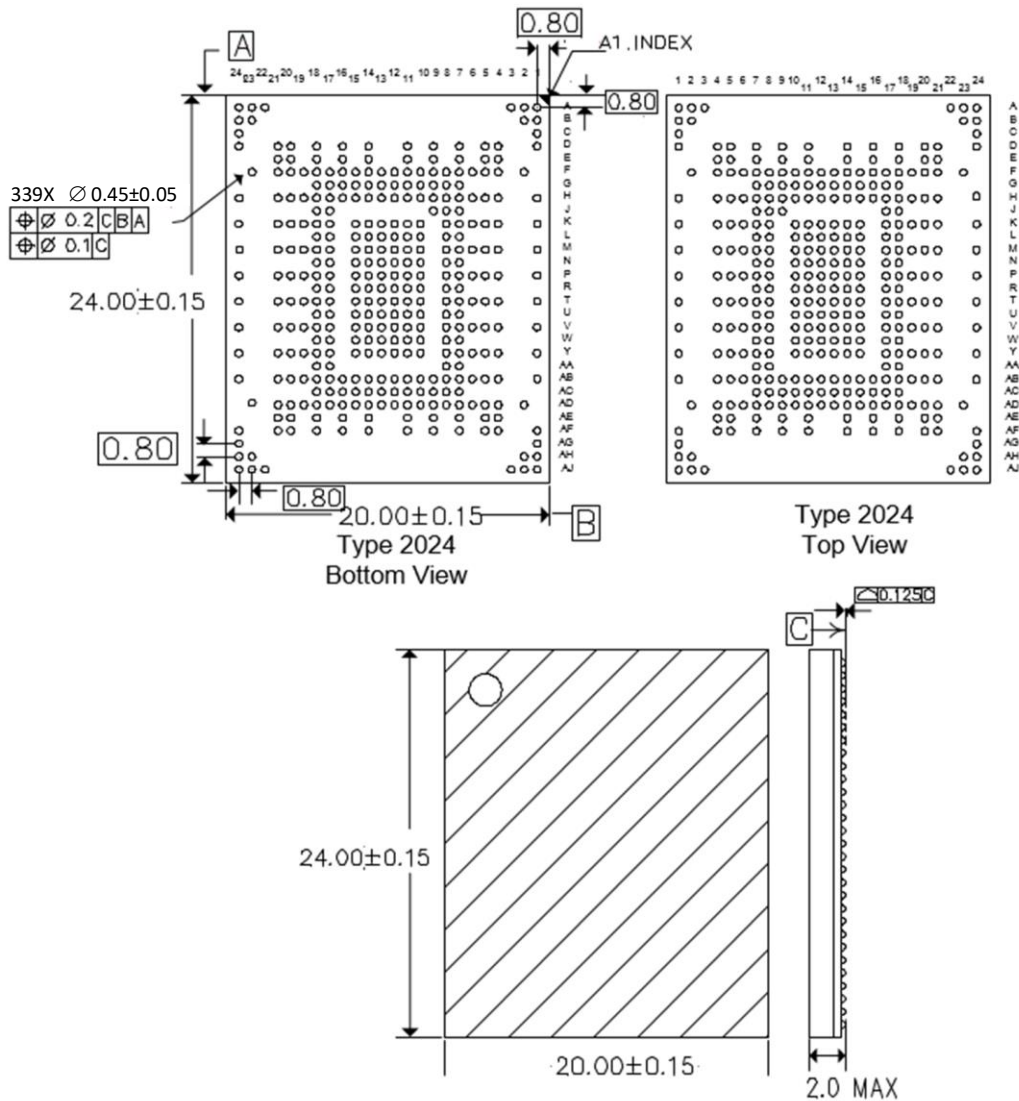
Figure 2-51. M.2 Type 2024-S5 Mechanical Outline Drawing Example
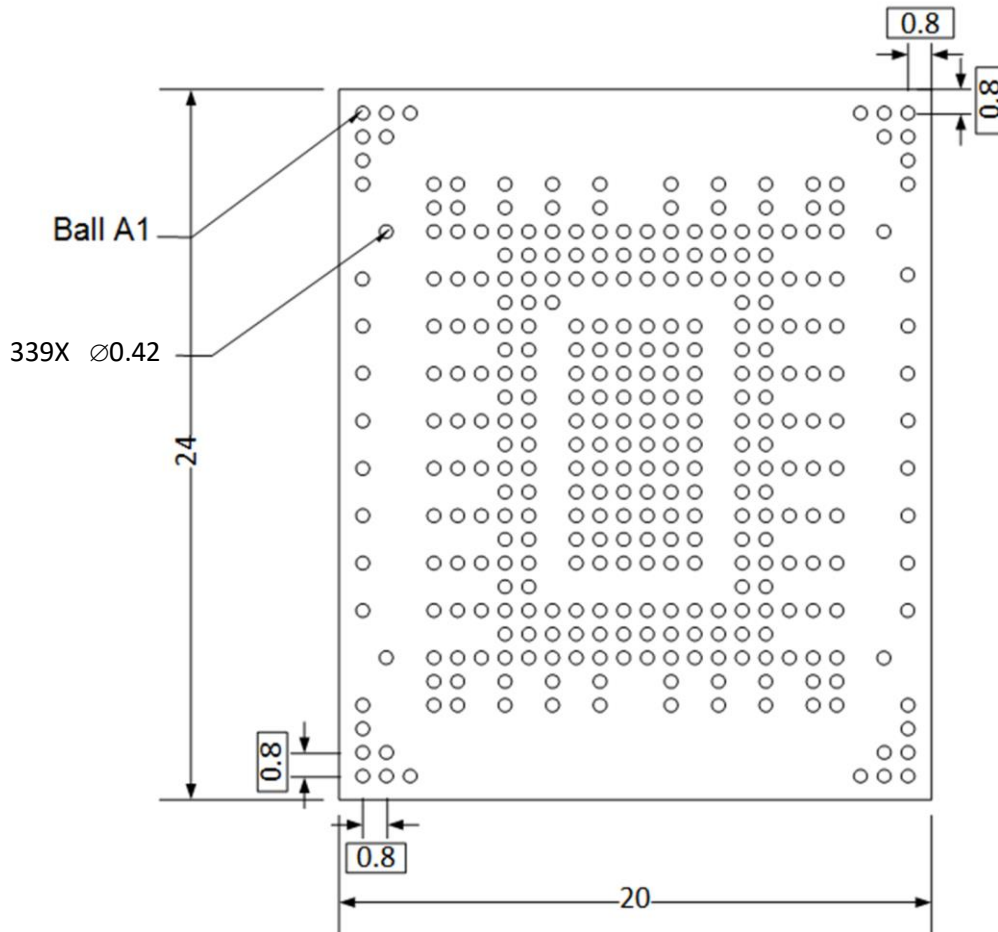
Figure 2-52. Recommended Land Pattern for M.2 Type 2024 BGA
(Top View)

2.3.6.4. Type 2228 Specification

Figure 2-53 shows an example of the M.2 Type 2228-S5 mechanical outline drawing and Figure 2-54 shows the recommended land pattern for Type 2228 package (dimensions shown in this figure are nominal).
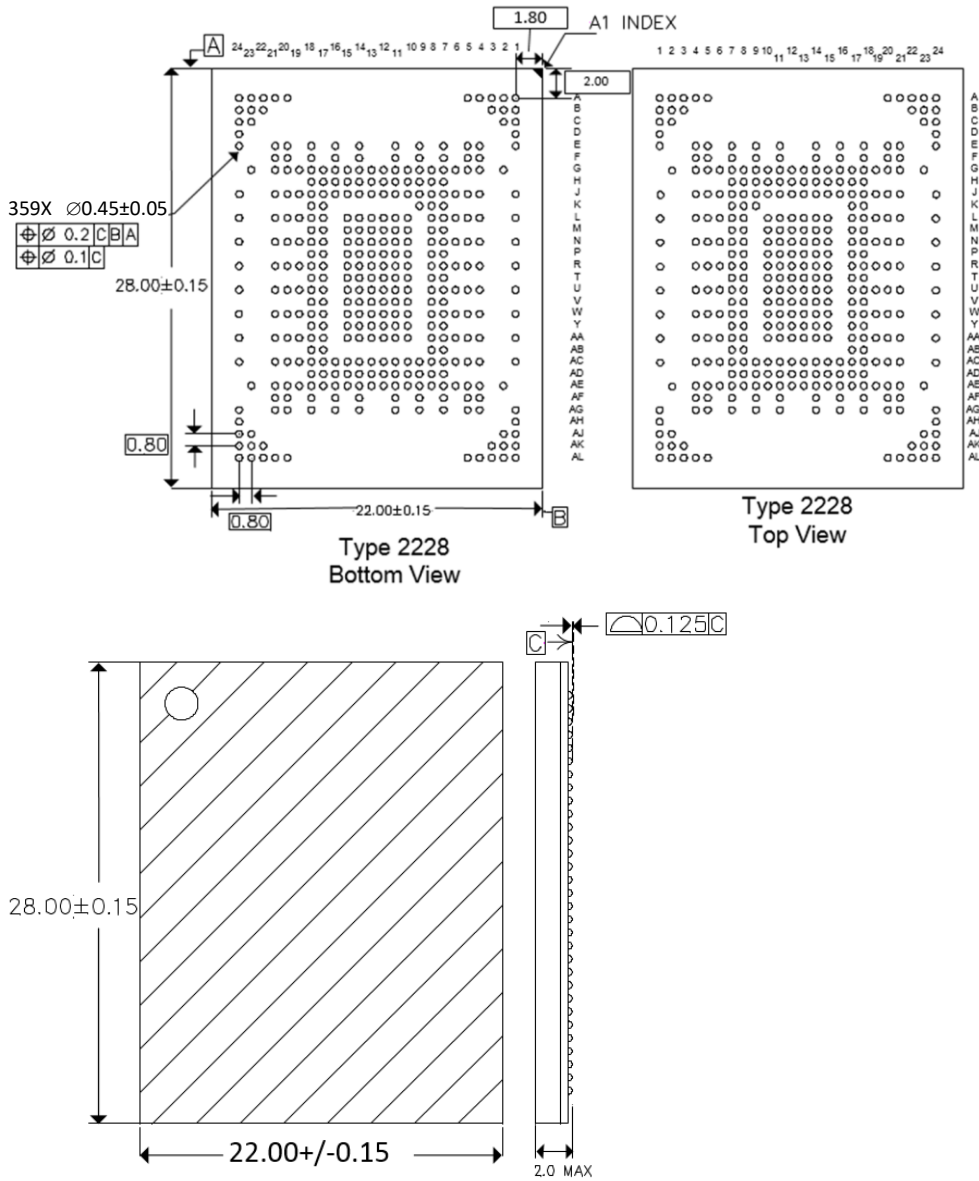
Figure 2-53. M.2 Type 2228-S5 Mechanical Outline Drawing Example
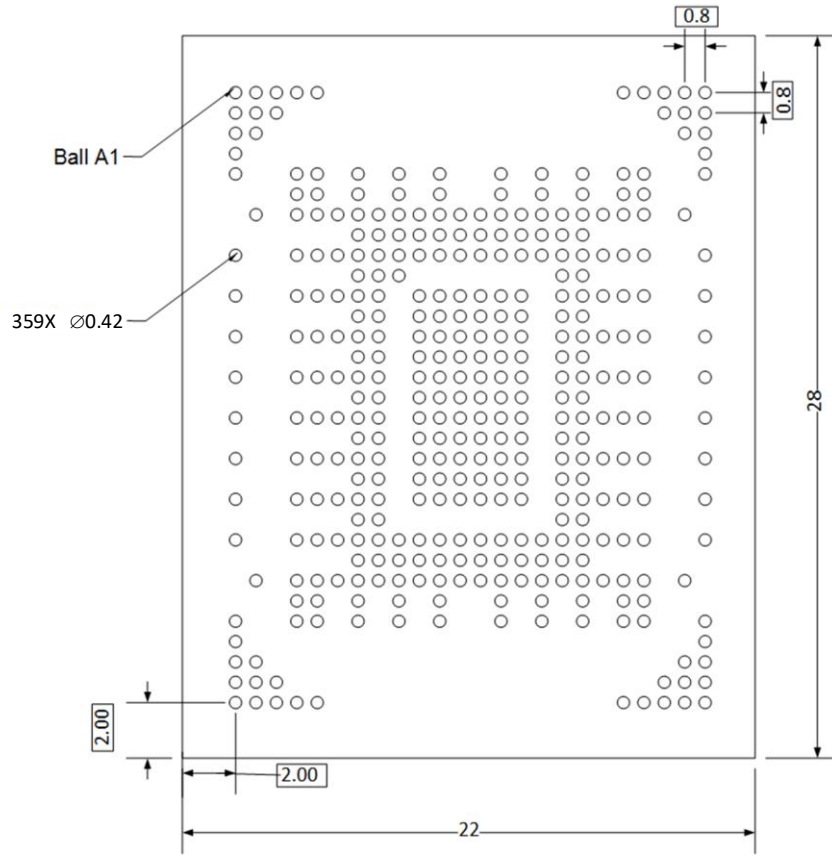
Figure 2-54. Recommended Land Pattern for M.2 Type 2228 BGA (Top View)

2.3.6.5. Type 2828 Specification

Figure 2-55 shows an example of the M.2 Type 2828-S5 mechanical outline drawing and Figure 2-56 shows the recommended land pattern for Type 2828 package (dimensions shown in this figure are nominal).
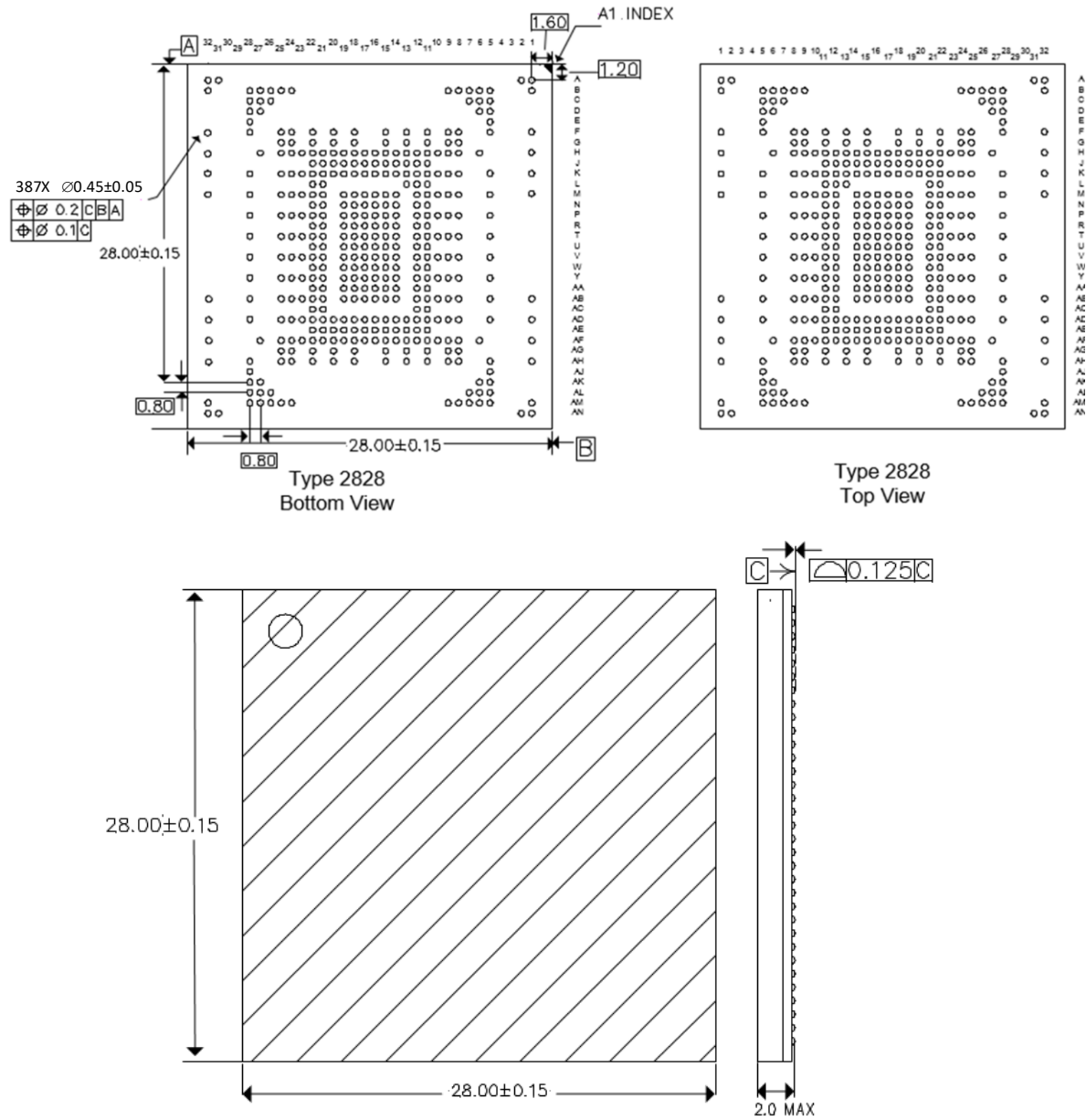
Figure 2-55. M.2 Type 2828-S5 Mechanical Outline Drawing Example
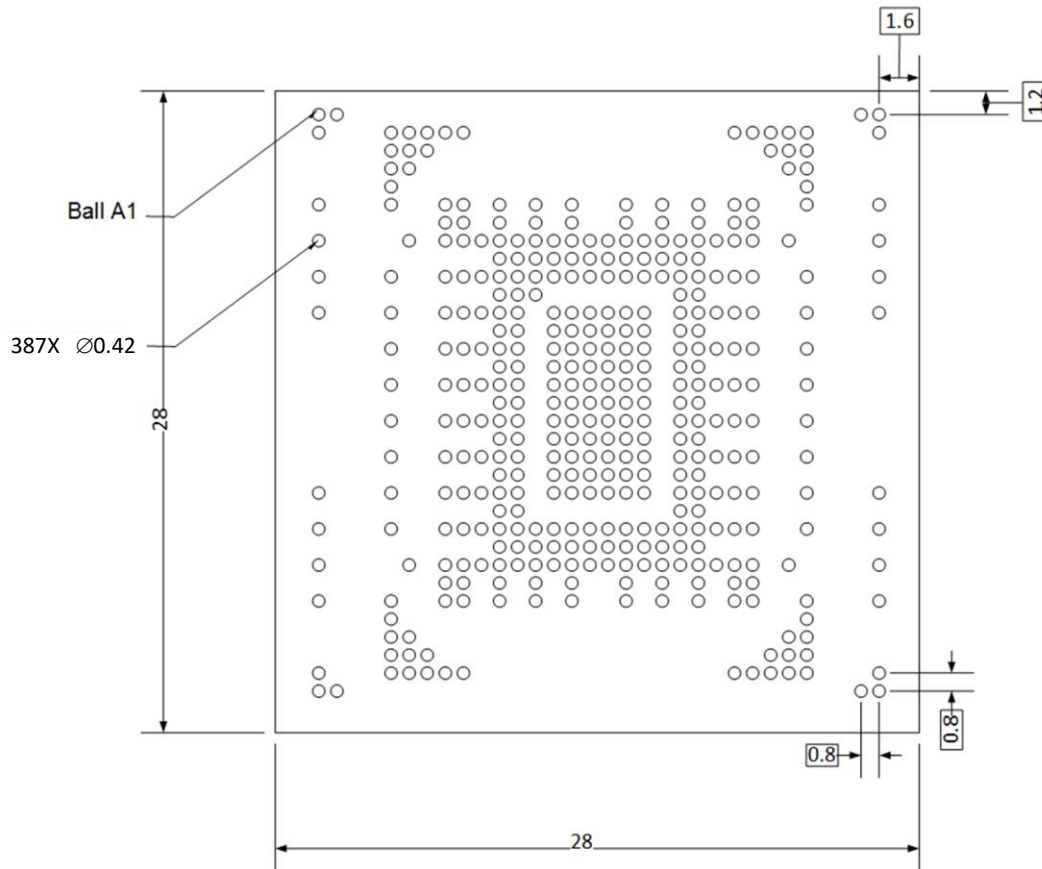
Figure 2-56. Recommended Land Pattern for M.2 Type 2828 BGA
(Top View)

2.3.7. RF Connectors

The top end of the wireless Adapter board area is the preferred location for the RF connectors. However, other areas are used in cases that this area is not enough at the expense of the component area (see Figure 2-57).

The standard 2x2 mm size RF receptacle connectors (see Figure 2-58) to be used in conjunction with the M.2 Adapters will accept two types of mating plugs that will meet a maximum Z-height of 1.45 mm (see Figure 2-59) utilizing a Ø 1.13 mm (Diameter (Ø) = 1.13 mm) coax cable or a maximum Z-height of 1.2 mm using a Ø 0.81 mm coax cable (see Figure 2-60). Figure 2-61 shows the antenna connector designation scheme.
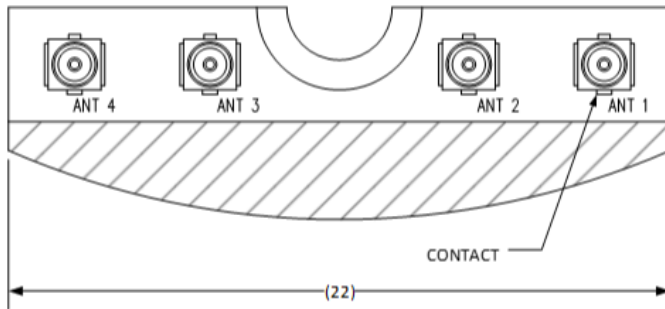
Figure 2-57. Board Type 2230 Antenna Connector Designation Scheme
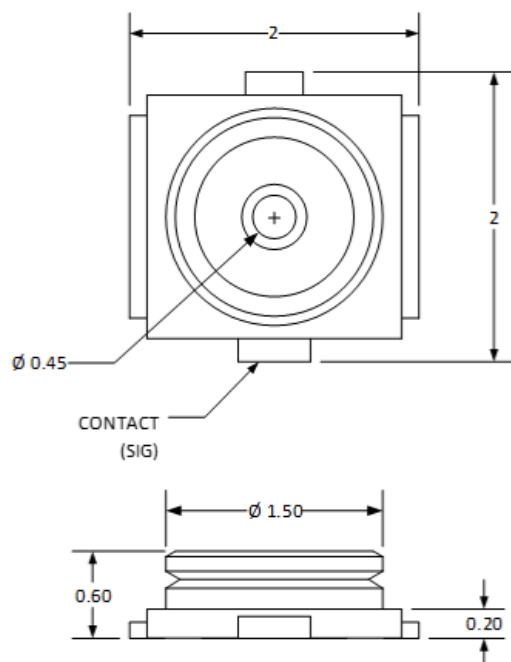
Figure 2-58. Generic 2x2 mm RF Receptacle Connector Diagram
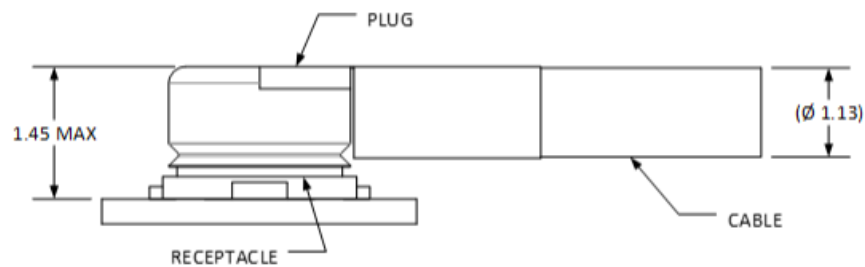
Figure 2-59. Mated Plug for Ø 1.13 mm Coax Cable
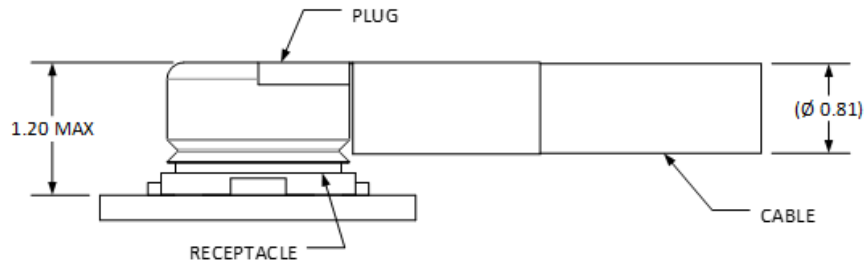
Figure 2-60. Mated Plug for Ø 0.81 mm Coax Cable
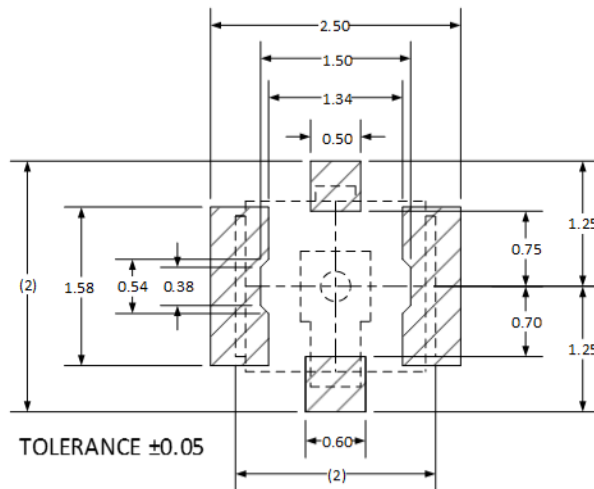
Figure 2-61. Antenna Connector PCB Recommended Land Pattern

Note: An optional Non-Plated Through Hole is permitted at the center of the land pattern for improved performance, enforcement of a trace Keep Out Zone and/or mechanical alignment. See example in Figure 2-45.

The minimum requirements for the RF Connector are listed in Table 5 to Table 8.

- Table 2-5.   RF Connector Physical Characteristics
- Table 2-6.   RF Connector Mechanical Requirements
- Table 2-7.   RF Connector Electrical Requirements
- Table 2-8.   RF Connector Environmental Requirements

Table 2-5.   RF Connector Physical Characteristics

Characteristic	Description
Receptacle Physical Outline	2 mm x 2 mm x 0.60 mm
Receptacle OD	1.5 mm
Housing Material	High Temperature Plastic
Flammability	UL 94-V0
Contact Material	Copper Alloy/Gold Plating
Ground Contact Material	Copper Alloy/Gold Plating

Table 2-6.   RF Connector Mechanical Requirements

Description	Standard Requirement	Improved Requirement
Mating force	30 N Maximum	
Un-mating force	5 N Initial, 3 N Minimum after 30 cycles, 20 N Maximum	
Cable Retention at 0 Degree Pull (Parallel to PCB)	5 N Minimum	20 N Minimum (Ø 1.13 mm wire) 10 N Minimum (Ø 0.81 mm wire)
Cable Retention at 30 Degree Pull (PCB to Cable Angle)	Not Recommended	10 N Minimum
Durability (# of mating cycles)	30 cycles (Contact Resistance = 20 mΩ)	
Receptacle Shearing Strength	20 N Minimum	
Vibration	No momentary disconnections of 1 µs Minimum	

Table 2-7.   RF Connector Electrical Requirements

Description	Requirements	Notes
Voltage Rating	60 V AC	
Current Rating	1.0 A Maximum	
Impedance	50 Ω	
Receptacle VSWR- 100 MHz ≤ f < 3 GHz	1.3 Maximum	1
Receptacle VSWR- 3 GHz ≤ f < 6 GHz	1.45 Maximum	1
Optional Enhanced Frequency Receptacle VSWR- 3 GHz ≤ f < 12 GHz	2.0 Maximum	1, 2
Contact Resistance	Inner: 20 mΩ Maximum	
	Outer: 20 mΩ Maximum	
	Initial: 20 mΩ Maximum	
Dielectric Withstanding Voltage	200 V AC for one minute	
Insulation Resistance	500 mΩ for one minute at 100 V DC	

Note: 1. The VSWR of the receptacle is measured differently than the VSWR of the mating plug (see Section 6.4).
   2. The optional Enhanced frequency performance to 12 GHz to be provided upon specific request.

Table 2-8.   RF Connector Environmental Requirements

Description	Requirement
Operating Temperature Range	-40 ˚C to +85 ˚C
Humidity	90%
Soldering Heat Resistance	Lead Free Reflow up to 260 ˚C peak for 10 s
RoHS Compliant/Halogen Free	Must be compliant

2.3.7.1. Socket 1 and 2 RF Connector Pinout

The RF Connector area will allow two (2), three (3), four (4), or six (6) RF connectors to be placed as a function of the board Type:

- ❑ Type 22xx supports up to four RF Connectors
- ❑ Type 1630 supports up to two RF Connectors
- ❑ Type 30xx supports up to six RF Connectors
- ❑ Type 1216 supports up to three RF Connectors

To remain consistent with the host interface pin order, the RF connectors are labeled ANT0, ANT1, ANT2, ANT3, ANT4, and ANT5 from right to left. The recommended antenna function allocation is given in Table 2-9.

Table 2-9. Recommended Antenna Function Allocation Table

#	Function	Location/FF Type	Keys	ANT5	ANT4	ANT3	ANT2	ANT1	ANT0
1	WIFI and BT	Socket 1/ 1630	A, E, A-E	N/A	N/A	N/A	WIFI1	WIFI2+BT	N/A
2	WIFI and BT and/or Other Comms	Socket 1 /2230, 3026, 3030, 2226	A, E, A-E	N/A	Other Comm (when applicable)	WIFI3 (when applicable)	WIFI1	WIFI2+BT	N/A
3	WIFI and/or BT	Socket 1 / 2230, 3026, 3030, 2226	A, E, A-E	N/A	WIFI3+ BT4	WIFI2+ BT3	WIFI1+BT2	BT1	N/A
4	WWAN and/or GNSS	Socket 2/ 2242, 3042, 3052, 3060	B	N/A	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	N/A
5	WWAN and/or GNSS	Socket 2/ 2242, 3042, 3052, 3060	C	VENDOR DEFINED	WWAN Main	VENDOR DEFINED	GNSS (when applicable)	WWAN AUX+GNSS (when shared)	VENDOR DEFINED
6	Any	Solder Down/1216	N/A	N/A	N/A	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	N/A

Notes:
- Actual RF connector functions to be defined by vendor↔customer if not using the recommended allocations in this table.
- ANT0 and ANT5 are an expansion of the basic four antenna connections (ANT1-ANT4) when the board is 30 mm wide.
- A "+" in the ANTx columns indicates Shared Antenna of the listed Comms when applicable.
- "Wi-Fi1" = WIFI antenna 1; "WIFI2" = WIFI antenna 2; "WIFI3" = WIFI antenna 3; "BT1" = BT antenna 1; "BT2" = BT antenna 2; "BT3" = BT antenna 3; "BT4" = BT antenna 4.

> **IMPLEMENTATION NOTE: Antenna Function Allocations**
>
> Platform OEMs may support Adapters from multiple Adapter vendors where each Adapter vendor implements different antenna function allocations. For example, Adapter vendor A may support Row 2 in Table 2-9, while Adapter vendor B may support Row 3. Care must be taken by the Platform OEM to make sure the antenna cables are sufficiently long to accommodate different antenna function locations; that unused antenna cables do not cause interference and the assembly process accommodates different antenna function allocations between Adapters.

The recommended Wi-Fi antenna port assignment implies that the main Wi-Fi antenna port (e.g., Wi-Fi 1x1) would use ANT2 and listed as Wi-Fi1. When Wi-Fi expands to a 2x2 configuration, it should share the antenna port with the BT using ANT1. This is listed as Wi-Fi2+BT. In extended Wi-Fi 3x3 solutions, the third antenna port used is ANT3 and this is listed as Wi-Fi3. Other Comms should use ANT4 when more complex wireless Combo solutions are implemented.

For Socket 1, Figure 2-62 shows Type 2230/2226 and Figure 2-63 shows Type 3030/3026 RF connector assignment recommendations.

GENERAL TOLERANCE IS ±0.15

Antenna	Interface
1	Wi-Fi/Bluetooth
2	Wi-Fi Main
3	Wi-Fi Aux 1
4	Other Wireless
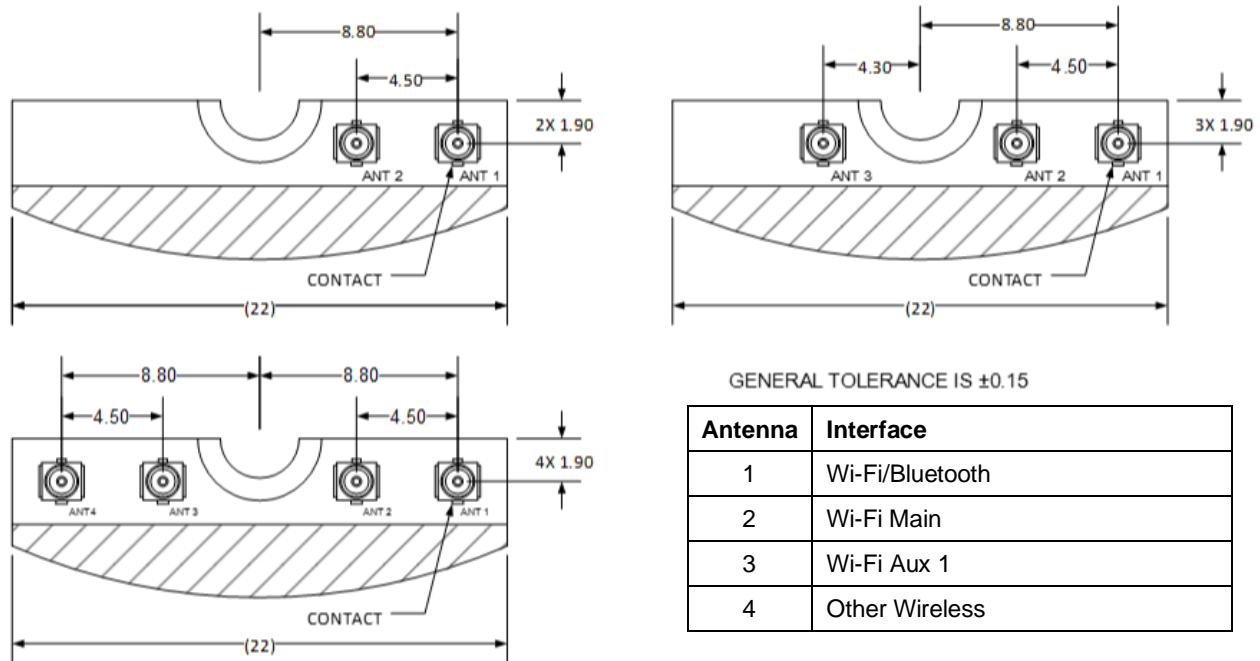
Figure 2-62. Socket 1 Type 2230/2226 RF Connector Assignment Recommendation

Antenna	Interface
0	N/A
1	Wi-Fi/Bluetooth
2	Wi-Fi Main
3	Wi-Fi Aux 1
4	Other Wireless
5	N/A
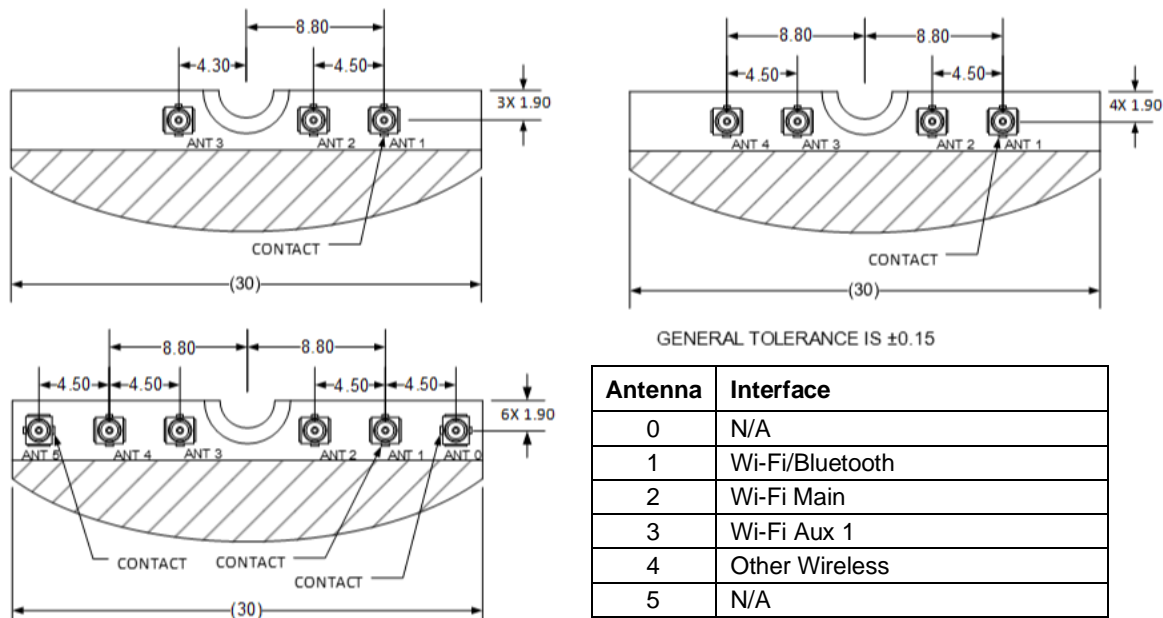
Figure 2-63. Socket 1 Type 3030/3026 RF Connector Assignment Recommendation

Socket 2 Key B Type 2242, Type 3042, Type 3052, and Type 3060 RF connector assignment recommendations are vendor specific. The Socket 2 Key C Type 2242, Type 3042, Type 3052, and Type 3060 RF connector assignment recommendations are listed in Table 2-9 and are seen in Figure 2-64.

Antenna	Key B	Key C
0	Vendor Specific	Vendor Specific
1	Vendor Specific	WWAN Aux
2	Vendor Specific	GNSS
3	Vendor Specific	Vendor Specific
4	Vendor Specific	WWAN Main
5	Vendor Specific	Vendor Specific
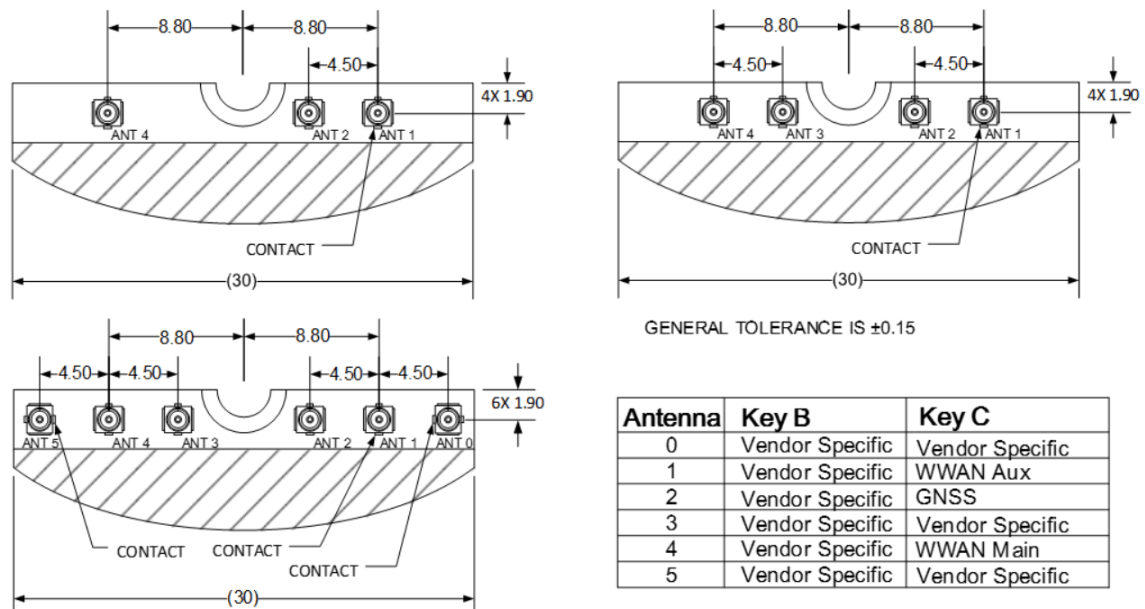
Note: Top 2 drawings in this Figure are also applicable to Type 2242.

Figure 2-64. Socket 2 Type 2242/3042/3052/3060 RF Connector Assignment Recommendation

2.4.   System Connector Specifications

The card interconnect is based on a 75 position Edge Card connector. The 75-position connector is intended to be keyed to distinguish between families of host interfaces and the various Sockets used in NB/very thin Platforms and Tablet Platforms. This specification document makes provision for the following three Socket families:

❑ Connectivity Socket 1

❑ WWAN/SSD/Other Socket 2

❑ SSD Drive Socket 3

To accommodate various product Z-height limitations, there will be generic types of Edge Connectors in multiple height variants designated below:

❑ M1.8 – Mid-mount (1.80 mm Max height (Ht.)) – For very low-profile Platforms

❑ H2.3 – Top-side – Single-sided (2.25 mm Max Ht.) Connector

❑ H2.5 – Top-side – Single-sided (2.45 mm Max Ht.) Connector

❑ H2.8 – Top-side – Double-sided (2.75 mm Max Ht.) Connector

❑ H3.2 – Top-side – Double-sided (3.20 mm Max Ht.) Connector

❑ H4.2 – Top-side – Double-sided (4.20 mm Max Ht.) Connector

This list of connector options is not exclusive; other connector designs are allowed per market needs. However, they must meet normative mechanical mating interface and connector SI requirements contained within this document.

Table 2-10 lists the Adapter heights supported by the different connector types.

Table 2-10.   Connector/Adapter Height Supported Matrix

	Description	S1	S2	S3	S4	S5	D1	D2	D3	D4	D5	D6	D7	D8
		Component Height Descriptors												
M1.8	Mid-mount Connector	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
							(see Note)							
H2.3	Single-sided (2.25 Max Ht.) Connector	✓	✓	✓	✓	✓								
H2.5	Single-sided (2.45 Max Ht.) Connector	✓	✓	✓	✓	✓								
H2.8	Double-sided (2.75 Max Ht.) Connector	✓	✓	✓	✓	✓				✓				
H3.2	Double-sided (3.2 Max Ht.) Connector	✓	✓	✓	✓	✓	✓	✓	✓	✓				
H4.2	Double-sided (4.2 Max Ht.) Connector	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: System clearance will have to be evaluated.

The Hx naming convention along with the mechanical Key letter enables easy recognition of the required connector through simple nomenclature; as shown in the following example:

M.2 Connector H2.3-E-Opt1

❑ **H2.3** designates the connector height; in this case the height supports a Single-sided solution (2.25 mm Max Ht.).

❑ **E** designates Key E.

❑ **Opt1** designates the durability level, the minimum number of insertion/extraction cycles, in this case a minimum of 25 (see the Durability line item in Table 2-12).

This Hx descriptor also aligns with the coinciding Standoff descriptor described in the Section 2.5.

2.4.1. Connector Pin Count

The connector has 75 positions. However, eight positions are used for each connector key, so the pin count is 67 pins.

2.4.2. Contact Pitch

The contact pitch is 0.5 mm. The connector will have two rows of pins, top and bottom. The bottom row is staggered by 0.25 mm from the top row.

2.4.3. System Connector Parametric Specifications

Table 2-11, Table 2-12, and Table 2-13 specify the requirements for physical, environmental, and electrical performance for the M.2 connector.

Table 2-11.   Connector Physical Requirements

Description	Requirement
Connector Housing	UL rated 94-V-0 Must be compatible with lead-free soldering process
Contact: Receptacle	Copper alloy with Gold Plating sufficient to meet all mechanical and environmental requirements
Contact Finish: Receptacle	Must be compatible with lead-free soldering process

Table 2-12.   Connector Environmental Requirements

Test Conditions	Specification
Durability	EIA-364-9: • Option 1 – 25 cycles minimum • Option 2 – 60 cycles minimum M.2 Connectors must meet at least 25 cycles. Upon completion of cycles the sample must meet all visual and electrical performance requirements.
Insertion Force	Insertion Force-25 N (2.55 KgF, 1 Newton = 1 Kg. m/s^2) maximum EIA-364-13, Method A
Shock	• 250 G (Notebook) and 285 G (Tablet) • At 2 ms half sine • On all six (6) axis
Vibration	EIA-364-1000 Test group 3, EIA-364-28
Operating Temperature	-40 °C to 80 °C
Environmental Test Methodology	EIA-364-1000 Test Group 1, 2, 3, and 4
Useful Field Life	Three years

Table 2-13.   Connector Electrical Requirements

Description		Requirement
Low Level Contact Resistance		EIA-364-23 • 55 mΩ maximum (initial) per contact • 20 mΩ maximum change allowed
Insulation Resistance		EIA-364-21 • >5 x 108 Ω @ 500 V DC
Dielectric Withstanding Voltage		EIA-364-20 • >300 V AC (RMS) @ Sea Level
Current Rating	M.2	• 0.5 A/Power Contact (continuous), 1.0 A/Power contact (less than 100 μs duration) • The temperature rise above ambient must not exceed 30 °C. • The ambient condition is still air at 25 °C. • EIA-364-70 Method 2
	M2-1A	• 1.0 A/Power Contact (continuous). 1.2 A/Power Contact (less than 100 μs duration). • The temperature rise above ambient must not exceed 30°C. • The ambient condition is still air at 25°C. • EIA-364-70 Method 2
Voltage Rating		50 V AC per Contact

2.4.4.   Additional Environmental Requirements

The connector must meet RoHS (no exceptions) and Low Halogen compliance.

2.4.5.   Card Insertion

❑   Angled insertion is allowable and preferred; intent is to minimize the insertion/extraction force. The minimum of angle of insertion is 5° (see Figure 2-65)

❑   Minimum two-step insertion is desirable; intent is to minimize the insertion/extraction force.
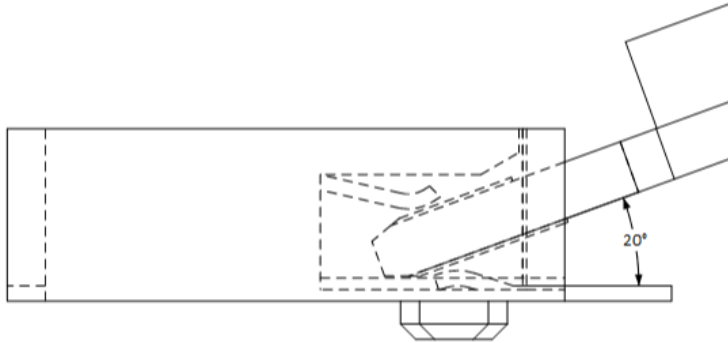
Figure 2-65.   Angle of Insertion

2.4.6.   Point of Contact Guideline

The signal integrity and mechanical requirements yield a starting point for the point of contact to Add-in Card Gold Finger relationship. The range for the upper point of contact measured from the seating plane should be between 0.8 mm to 1.3 mm and the range for the lower point of contact should be between 0.9 mm to 2.2 mm. (see Figure 2-66).

The actual mechanical relationship between connector and Add-in Card within a system is controlled by the Platform implementer. Therefore, Platform implementers should pay attention to all elements of positioning connector and Add-in Card to assure a proper mated condition.

> **Note:** The angle of insertion is a key consideration for determining the point of contact; see Figure 2-66. Objective is to minimize insertion/removal forces while meeting signal integrity requirements.

UPPER POINT OF

Upper Point of Contact

Lower Point of Contact
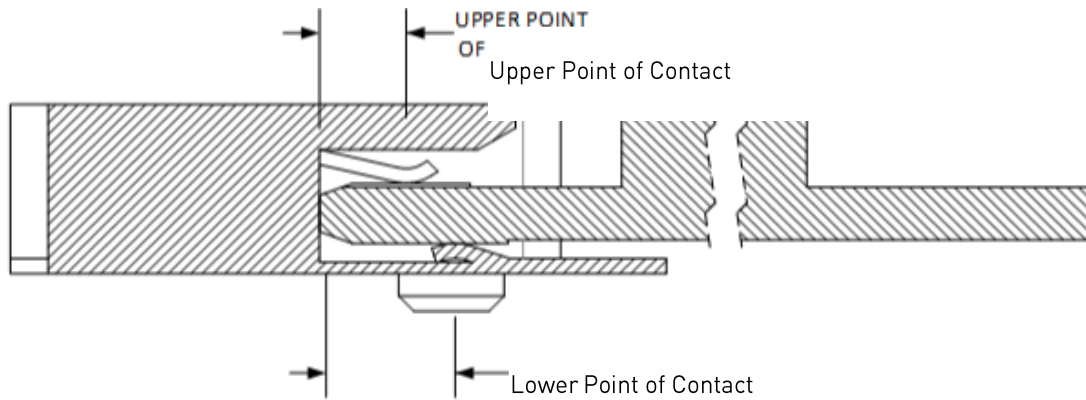
Note: Connector design and contact shape ar~~~~~~~~~~~~~~~~~~~~~~~intent beyond the dimensioned contact point.

Figure 2-66. Point of Contact

2.4.7.   Top-side Connection

2.4.7.1.   Top-side Connector Physical Dimensions

The top-side scheme has two connectors that share a common footprint but have a different stack-up requirement (see Section 2.4.7.3 for more detail).

❑   Length—22 mm maximum including land pattern

❑   Width—9.1 mm maximum including land pattern

Figure 2-67 through Figure 2-73show s the connector dimensions.
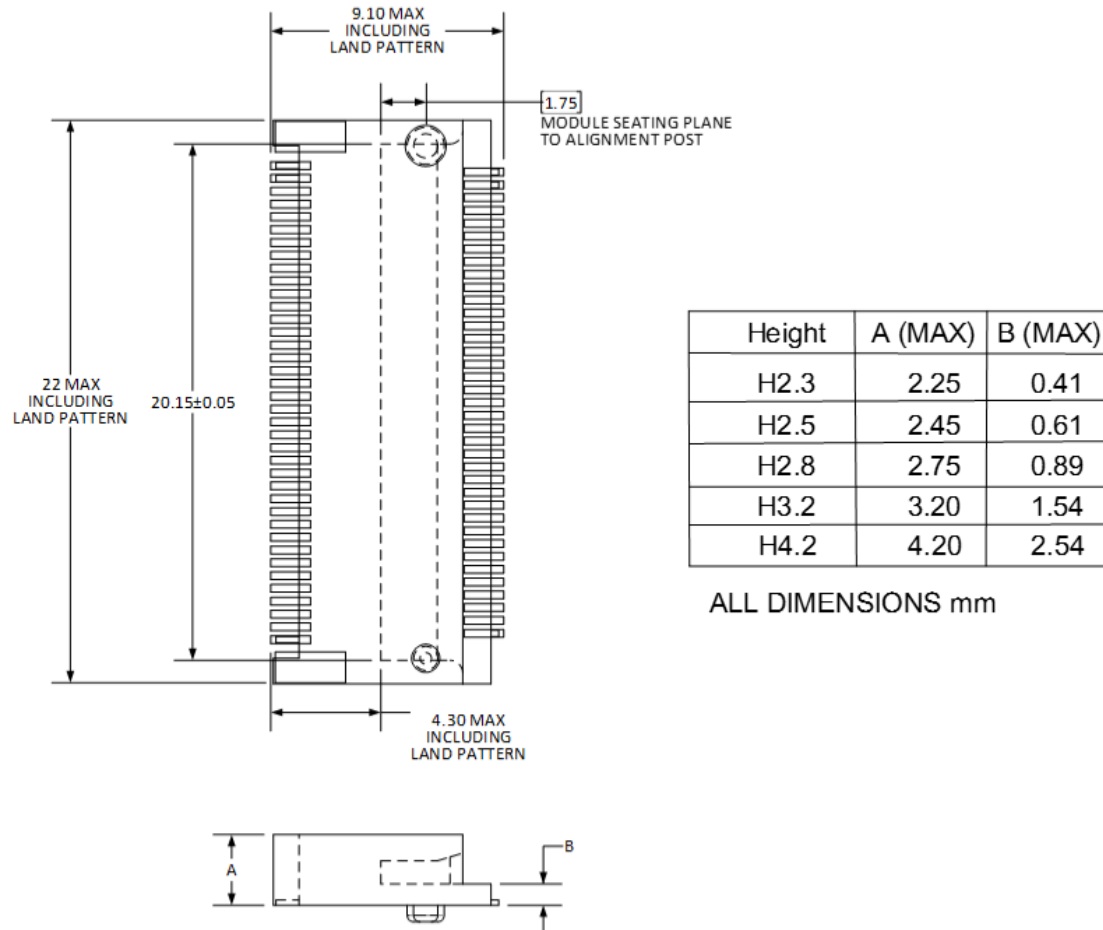
Figure 2-67. Top-side Connector Dimensions

Height	A (MAX)	B (MAX)
H2.3	2.25	0.41
H2.5	2.45	0.61
H2.8	2.75	0.89
H3.2	3.20	1.54
H4.2	4.20	2.54

ALL DIMENSIONS mm
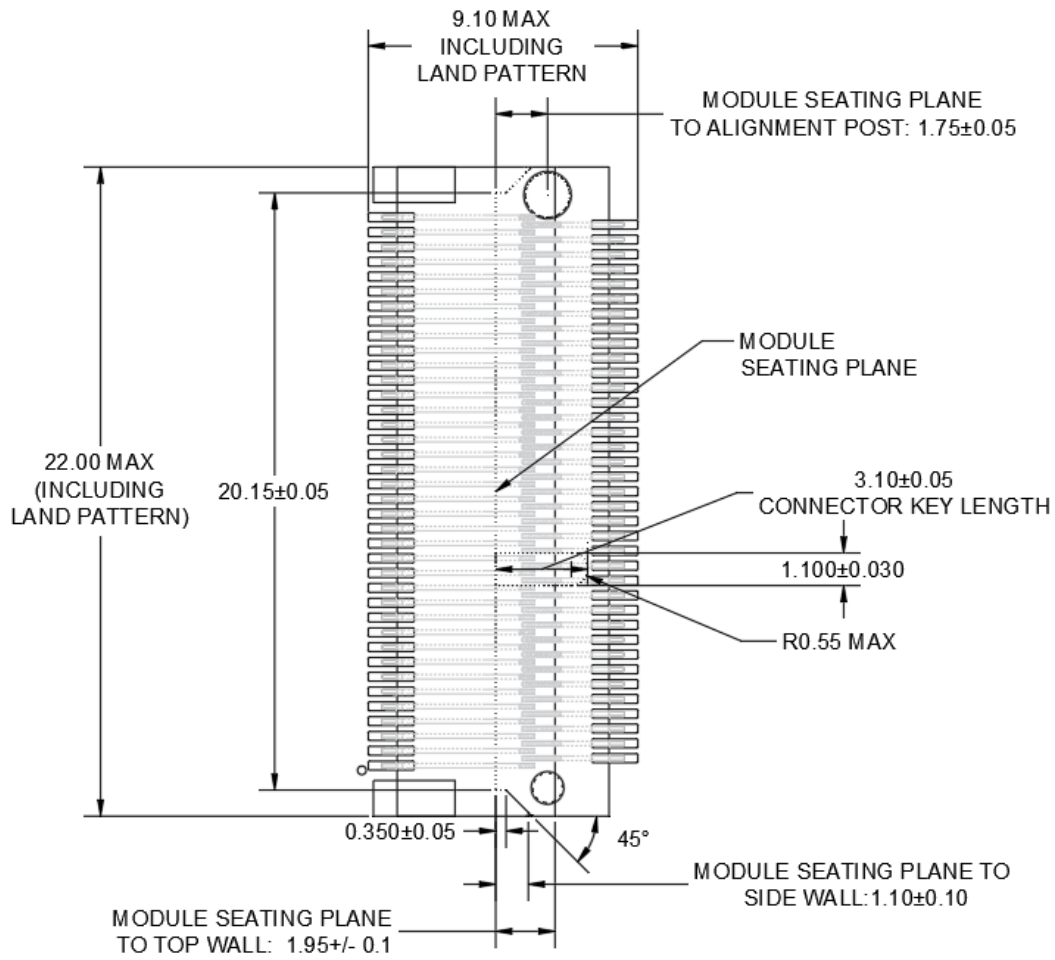
Figure 2-68. M.2-1A Top-side Connector Dimensions
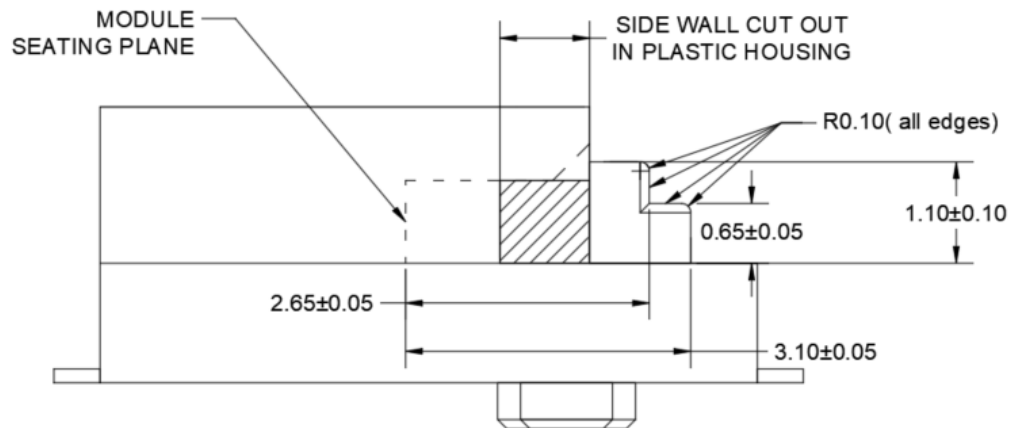
Figure 2-69. M.2-1A Connector Dimensions, Side View
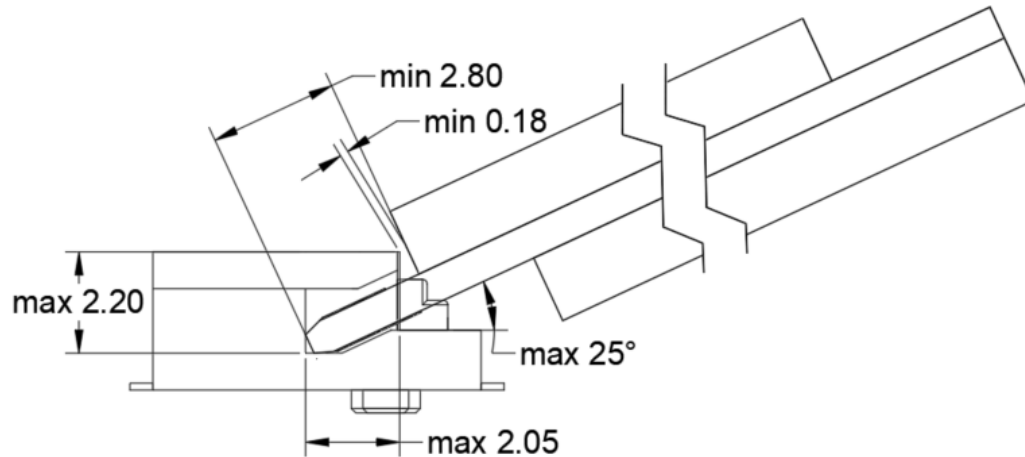
Figure 2-70. M.2-1A(B, C) Connector Angled Insertion Requirement

2.4.7.2.   Top-side Connection Total System Length

The maximum total solution is constrained to the Add-in Card length plus the following increases:

❑   The additional increase in length is 7.05 mm maximum for top-side connector to the Add-in
Card length (see Figure 2-71).
  ● The retention screw adds 2.75 mm maximum.
  ● The maximum extension, including land pattern beyond the Add-in Card leading edge is 4.3 mm.
❑   Add-in Card lengths are 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

4.30   ADD-IN CARD LENGTH   2.75
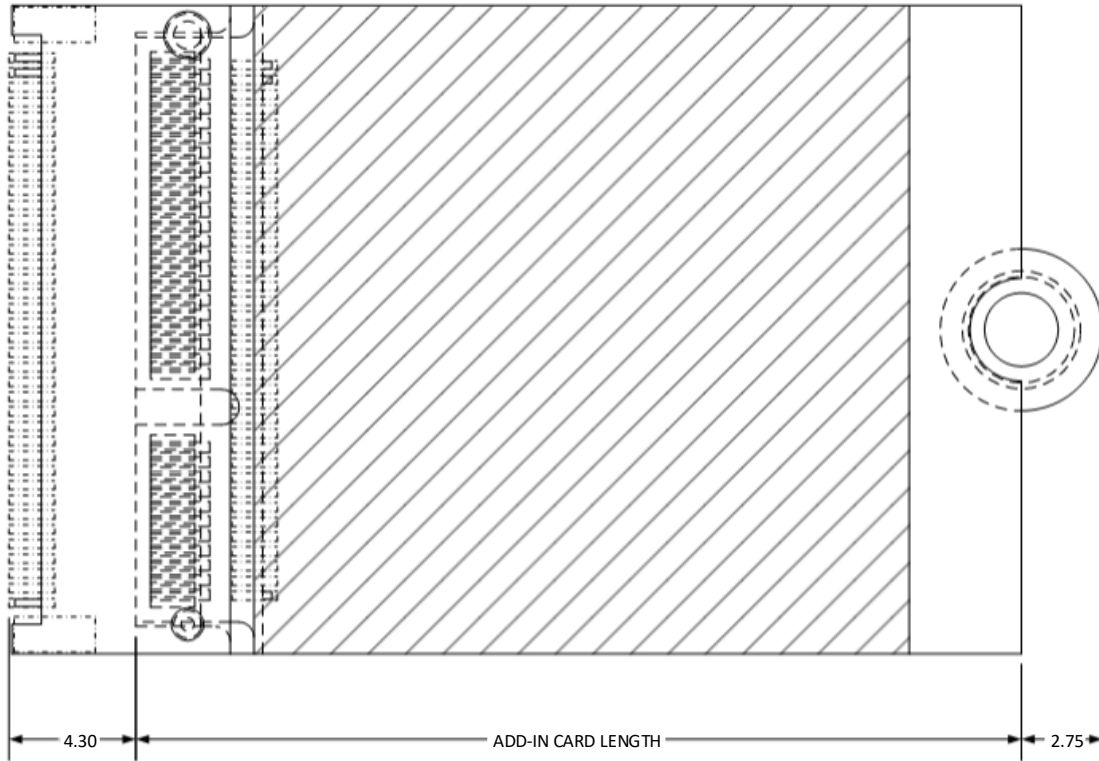
Note: The retention screw and stand-off are required for mechanical hold down and potential thermal path (see Section 2.5).

Figure 2-71. Top Mounting System Length

2.4.7.3.   Top-side Connection Stack-up

2.4.7.3.1.   Single-sided Add-in Card (Using H2.3 Connector)

Total solution above the main board (MB) varies based on the maximum component height on the Add-in Card. Figure 2-72, Figure 2-73, Figure 2-74, Figure 2-75, and Figure 2-76 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, 1.5 mm, 1.75 mm, and 2.00 mm. The maximum Root Sum Square (RSS) given is calculated from the top of the main board to the top of the Add-in Card.
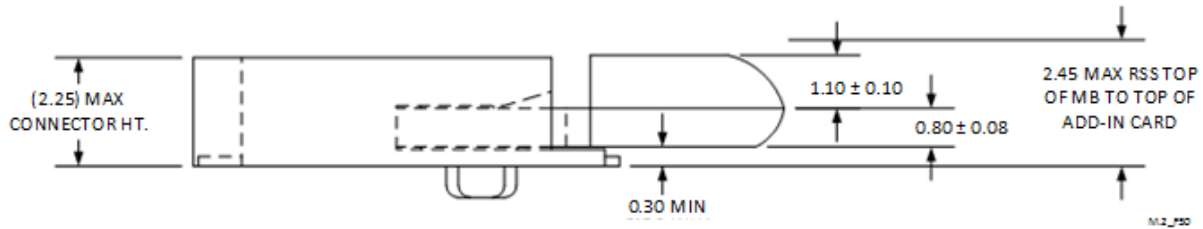
Figure 2-72. H2.3-S1 – Stack-up Top Mount Single-sided Add-in Card for 1.2 Maximum Component Height
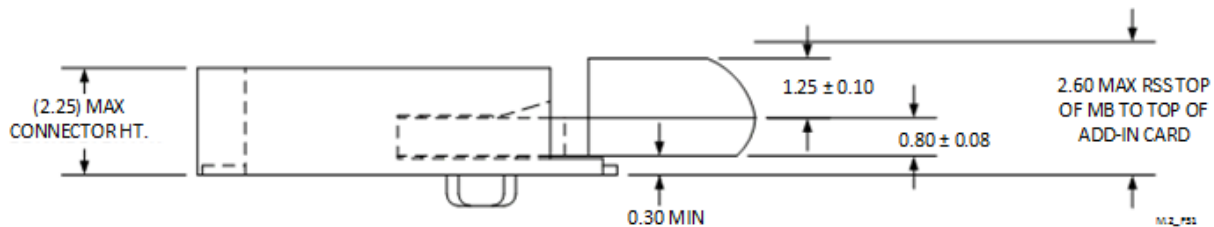
Figure 2-73. H2.3-S2 – Stack-up Top Mount Single-sided Add-in Card for 1.35 Maximum Component Height
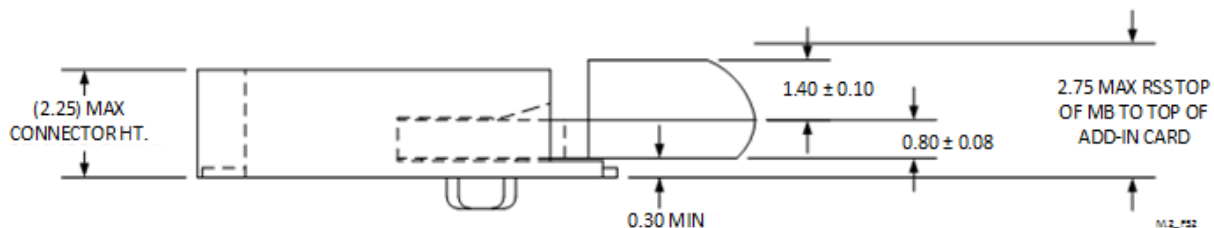
Figure 2-74. H2.3-S3 – Stack-up Top Mount Single-sided Add-in Card for 1.50 Maximum Component Height
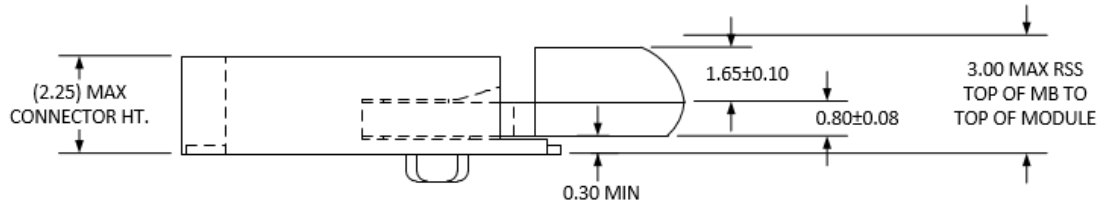
Figure 2-75. H2.3-S4- Stack-up Top Mount Single-sided Add-in Card for 1.75 Maximum Top-side Component Height and with Higher Clearance above Motherboard
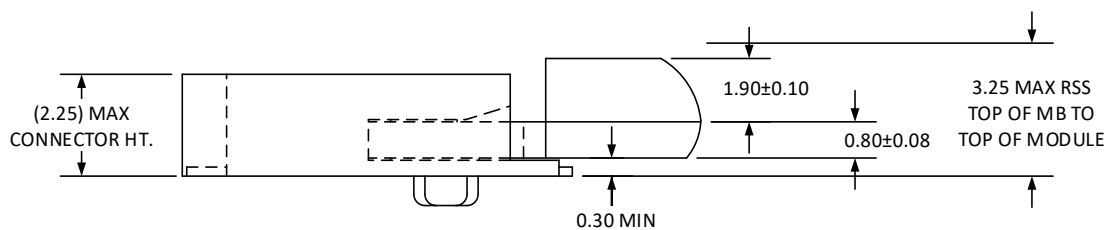
Figure 2-76. H2.3-S5- Stack-up Top Mount Single-sided Add-in Card for 2.00 Maximum Top-side Component Height and with Higher Clearance above Motherboard

2.4.7.3.2. Single-sided Add-in Card (Using H2.5 Connector)

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 2-77, Figure 2-78, Figure 2-79, Figure 2-80, and Figure 2-81 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, 1.5 mm, 1.75 mm, and 2.00 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card.
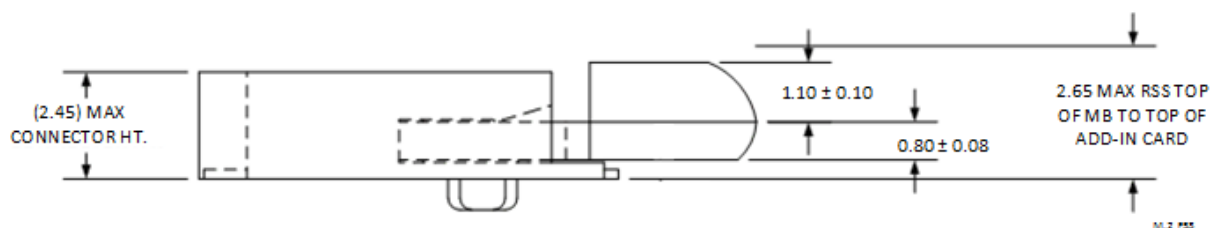
Figure 2-77. H2.5-S1 – Stack-up Top Mount Single-sided Add-in Card for 1.20 Maximum Top-side Component Height and with Higher Clearance above Motherboard
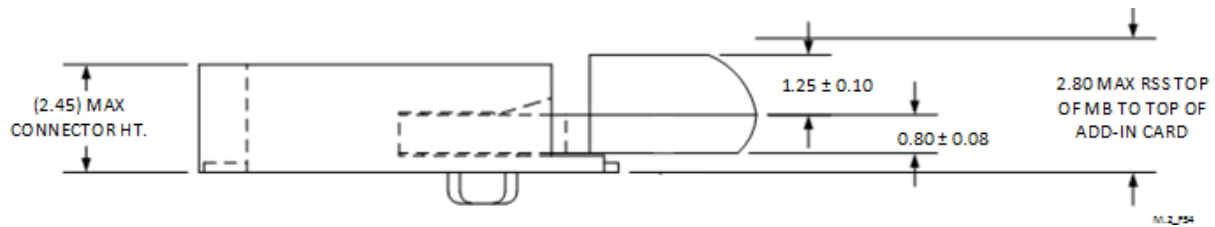
Figure 2-78. H2.5-S2 – Stack-up Top Mount Single-sided Add-in Card for 1.35 Maximum Top-side Component Height and with Higher Clearance above Motherboard
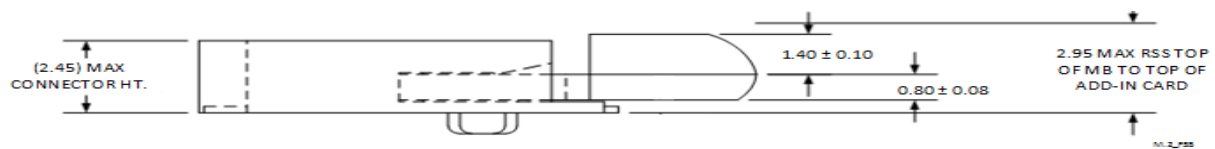
Figure 2-79. H2.5-S3 – Stack-up Top Mount Single-sided Add-in Card for 1.5 Maximum Top-side Component Height and with Higher Clearance above Motherboard
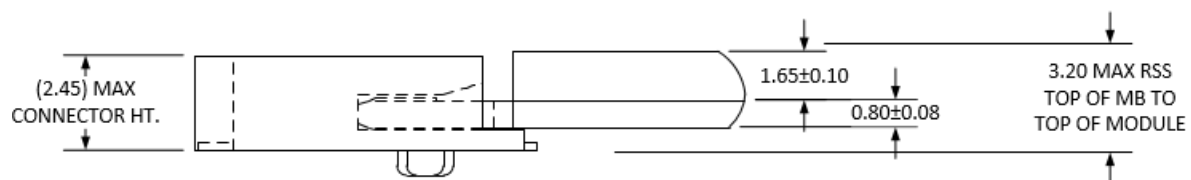
Figure 2-80. H2.5-S4- Stack-up Top Mount Single-sided Add-in Card for 1.75 Maximum Top-side Component Height and with Higher Clearance above Motherboard
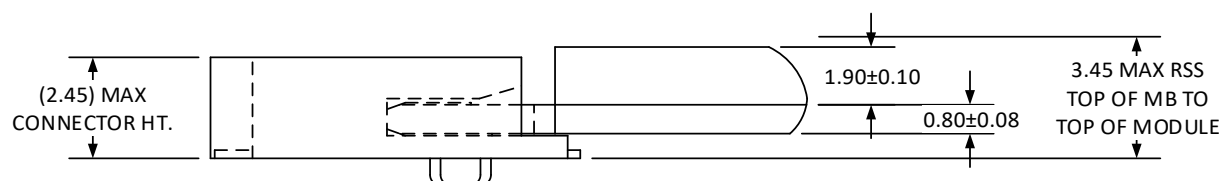
Figure 2-81. H2.5-S5- Stack-up Top Mount Single-sided Add-in Card for 2.00 Maximum Top-side Component Height and with Higher Clearance above Motherboard

2.4.7.3.3. Double-sided Add-in Card (Using H2.8, H3.2 and H4.2 Connector)

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 2-82, Figure 2-83, Figure 2-84, Figure 2-85, Figure 2-86, and Figure 2-87 show the profiles based on five top-side maximum component heights; 1.2 mm, 1.35 mm, 1.5 mm, 3.2 mm, and 6.5 mm. The bottom-side components maximum height is 2.0 mm, 1.50 mm, 1.35 mm, or 0.70 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card.
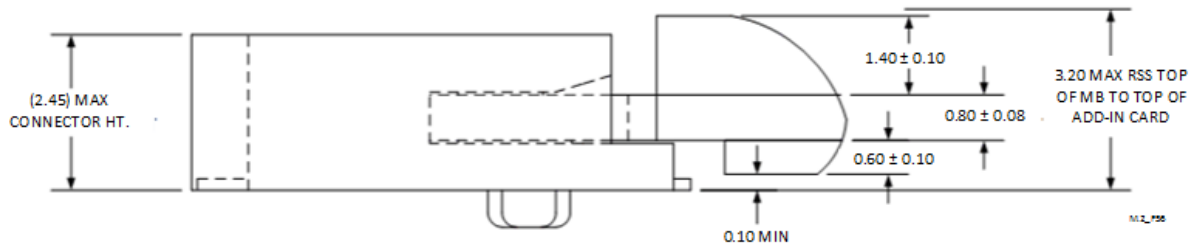
Figure 2-82. H2.8-D4 – Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height with 0.7 Maximum Bottom-side Component Height
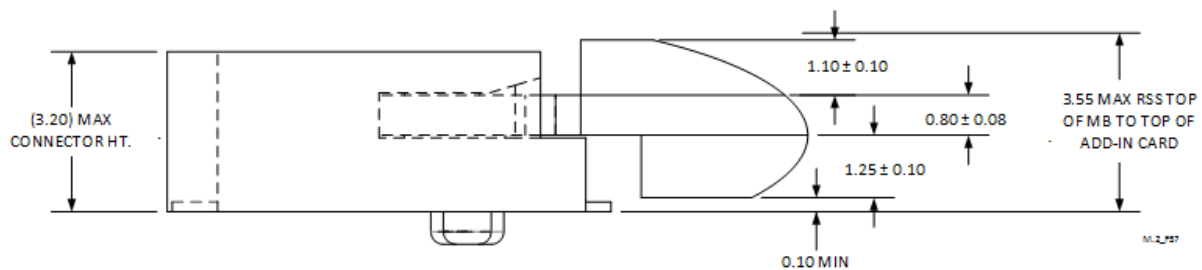
Figure 2-83. H3.2-D1 – Stack-up Top Mount Double-sided Add-in Card for 1.20 Maximum Top-side Component Height
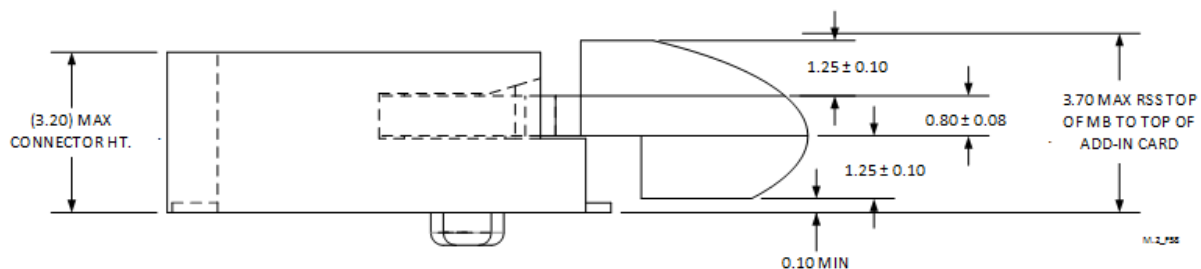
Figure 2-84. H3.2-D2 – Stack-up Top Mount Double-sided Add-in Card for 1.35 Maximum Top-side Component Height
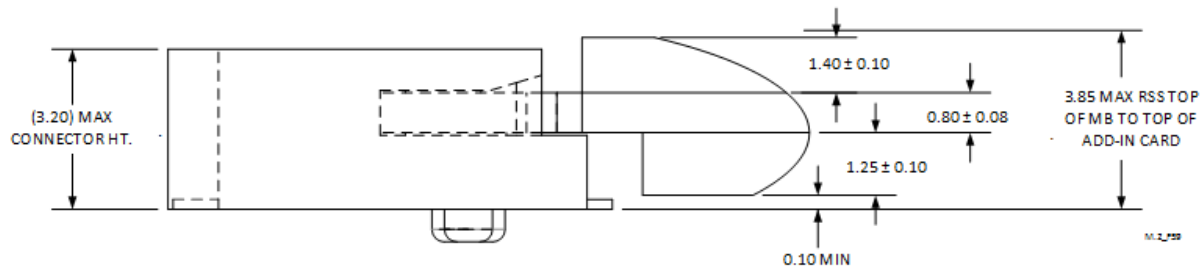
Figure 2-85. H3.2-D3 – Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height
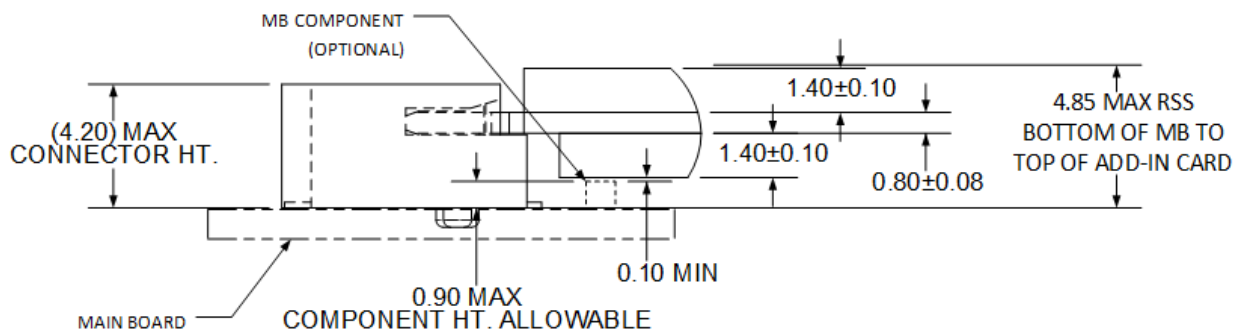
Figure 2-86. H4.2-D5 – Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height with 1.5 Maximum Bottom-side Component Height
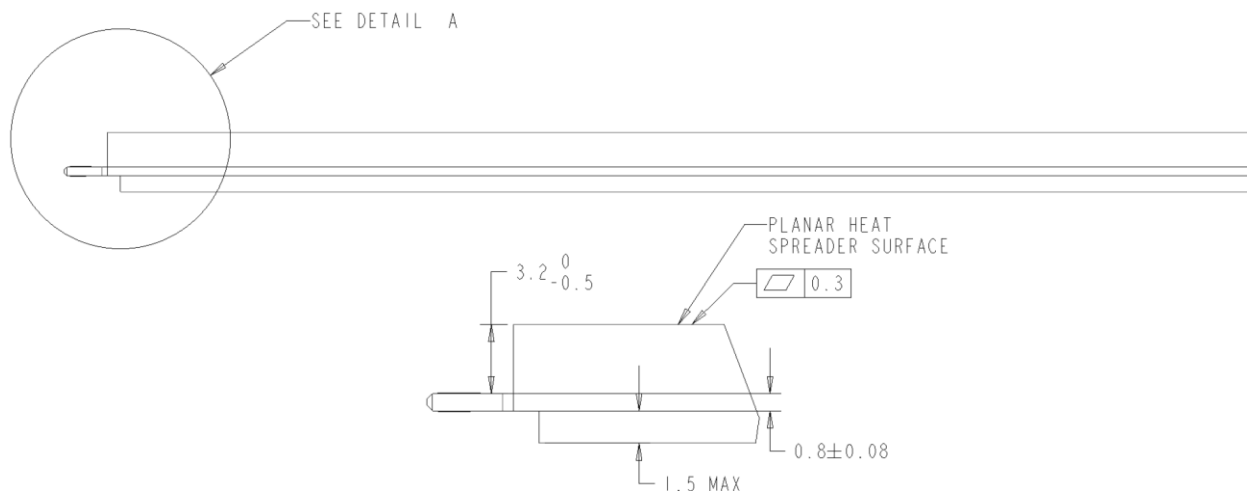
Figure 2-87. H4.2-D8-P Stack-up Top Mount Double-sided Add-in Card for 3.2mm +0 / -0.5 Top-side dimension and 1.5 Maximum Bottom-side Component Height

2.4.7.4. Top-side Connector Layout Pattern

The layout footprint of the Top Mount connector on the Platform side is shown in Figure 2-88. The land pattern includes all 75-pads although only up to 67 pads will be routed out while eight (8) pads will be redundant as they are located where the Mechanical Key is located. Figure 2-88 shows the eight redundant pads of Key B as faded.
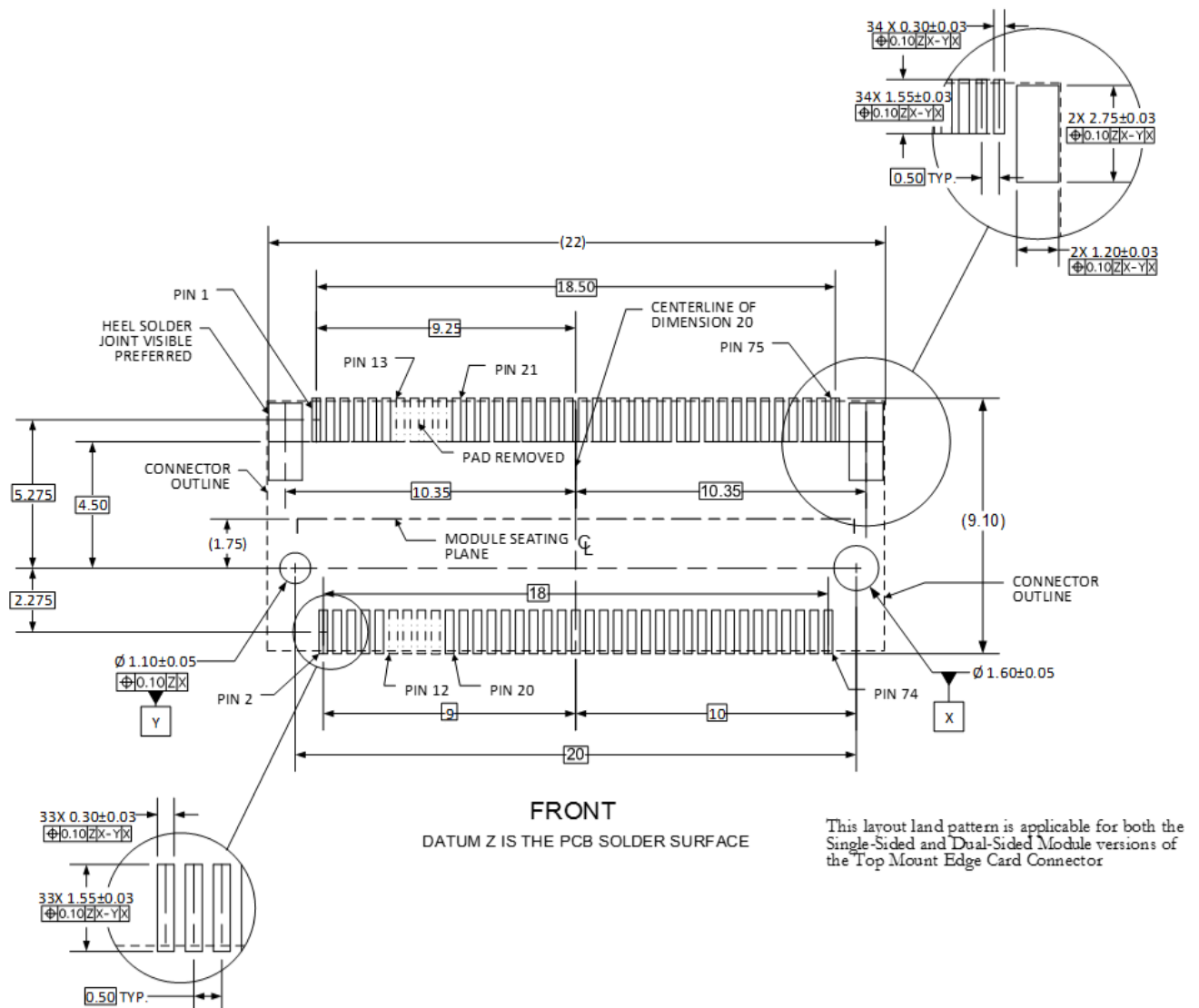
Figure 2-88. Example of Top Mount Motherboard Land Pattern - Key B Shown

2.4.7.5.   **Top-side Connector Insertion Capability**

The M.2-1A top-side connector is capable of having both M.2 Add-in Cards and M.2-1A of the same key ID inserted while the M.2 connector is limited to only accept the M.2 Add-in Card of the same key ID. M.2-1A PCB outline and connector were designed to ensure higher amperage M.2-1A Add-in Cards cannot be inserted into existing M.2 top-side connectors.

Table 2-14.   M.2 and M.2-1A Connector and Card Insertion Capability Matrix

	M.2 Connector	**M.2-1A Connector**
M.2 Add-in Card	Inserts	Inserts
M.2-1A Add-in-Card	Does not insert	Inserts

2.4.8.   **Mid-mount Connection (Using M1.8 Connector)**

2.4.8.1.   **Mid-mount Connector Physical Dimensions**

❑ Length-24 mm maximum including land pattern (see Figure 2-89)

❑ Width-9.5 mm maximum including land pattern
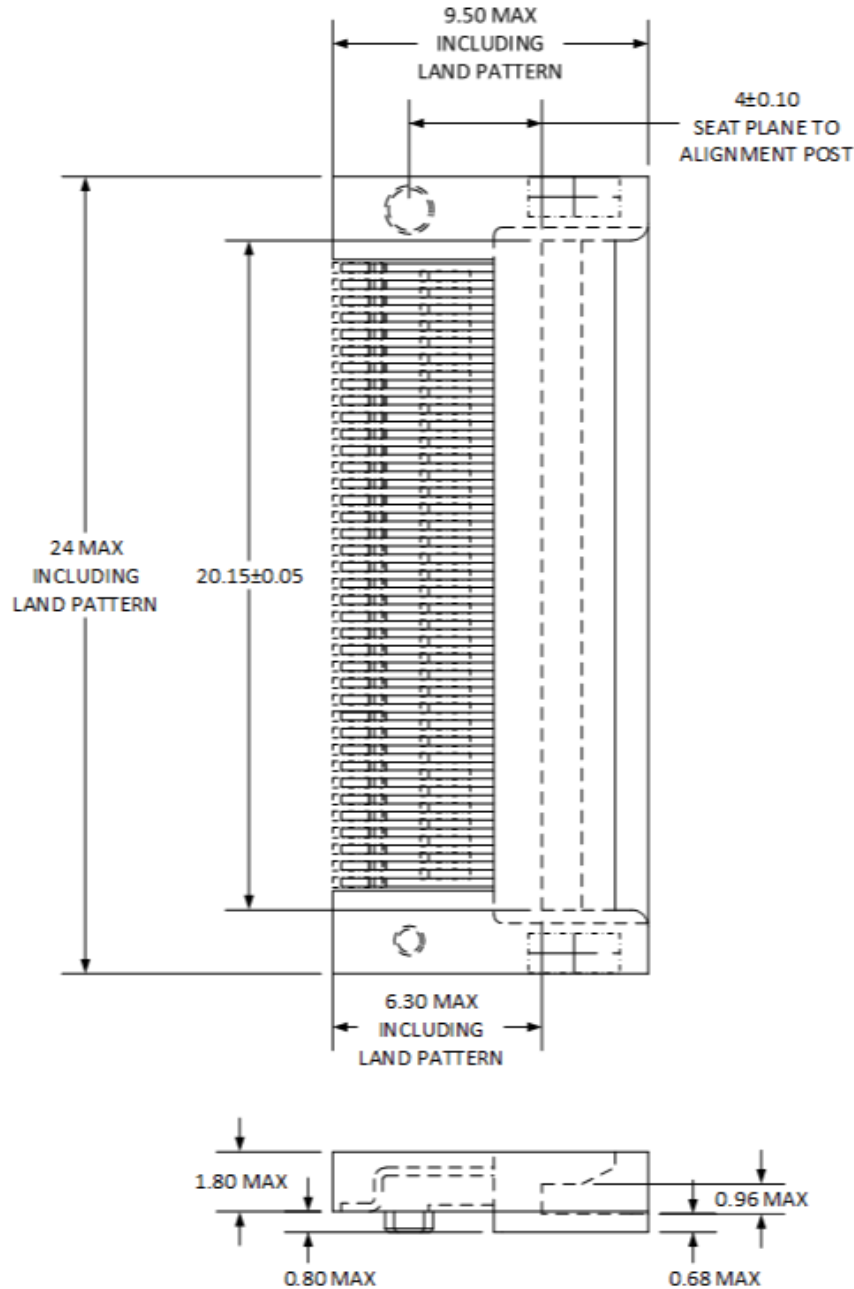
Figure 2-89. Mid-mount (In-line) Connector Dimensions

2.4.8.2. Mid-mount Connection Total System Length

The maximum total solution is constrained to Add-in Card length plus the following increases (see Figure 2-90):

❑ The additional increase in length is 9.05 mm for top-side connector to the Add-in Card length:
- The retention screw adds 2.75 mm maximum.
- The maximum extension, including land pattern beyond the Add-in Card leading edge is 6.3 mm.

❑   Add-in Card lengths are 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.
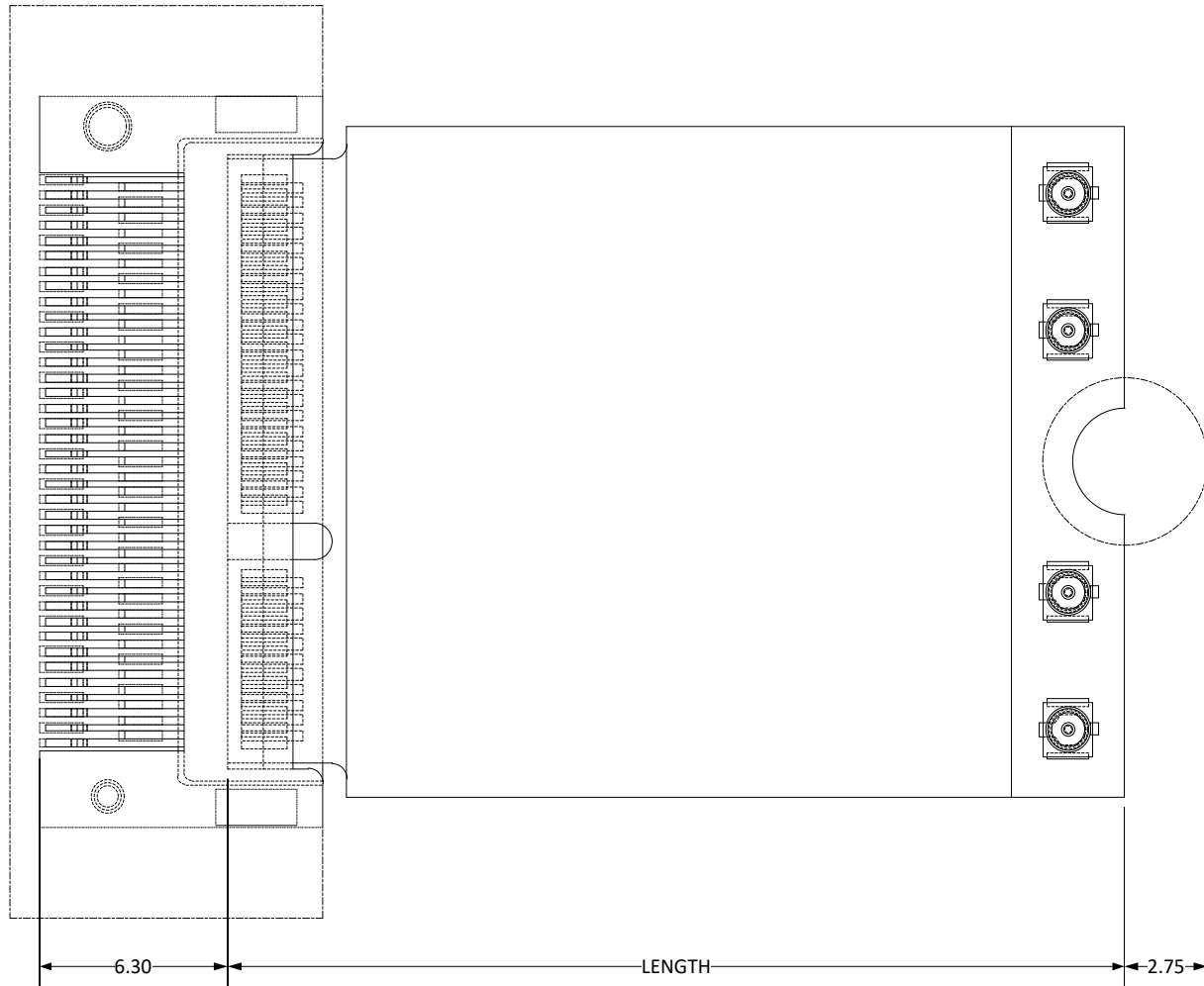
Figure 2-90. Mid-mount (In-line) System Length

2.4.8.3. Mid-mount Connection Stack-up

2.4.8.3.1. Single-sided Add-in Card

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 2-91, Figure 2-92, and Figure 2-93 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The maximum RSS given is measured from the top of the main board to the top of the Add-in Card. Also given is the maximum RSS as calculated from the bottom of the main board to top of the Add-in Card.
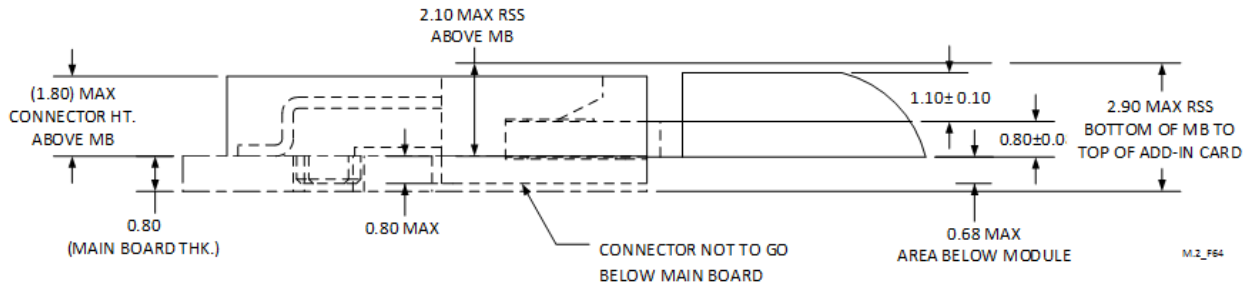
Figure 2-91. Stack-up Mid-mount (In-line) Single-sided (S1) Add-in Card for 1.2 Maximum Component Height
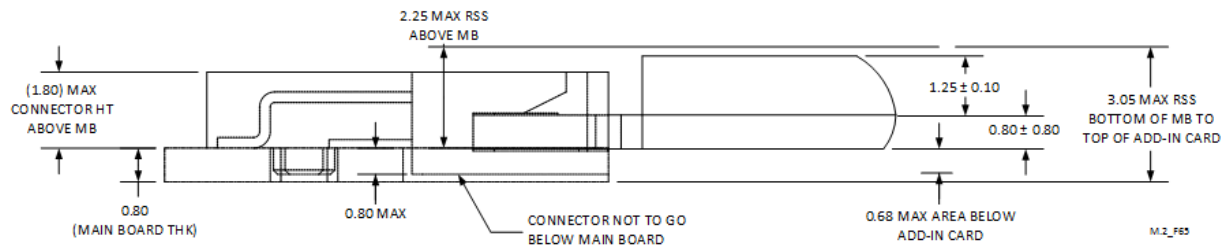
Figure 2-92. Stack-up Mid-mount (In-line) Single-sided (S2) Add-in Card for 1.35 Maximum Component Height
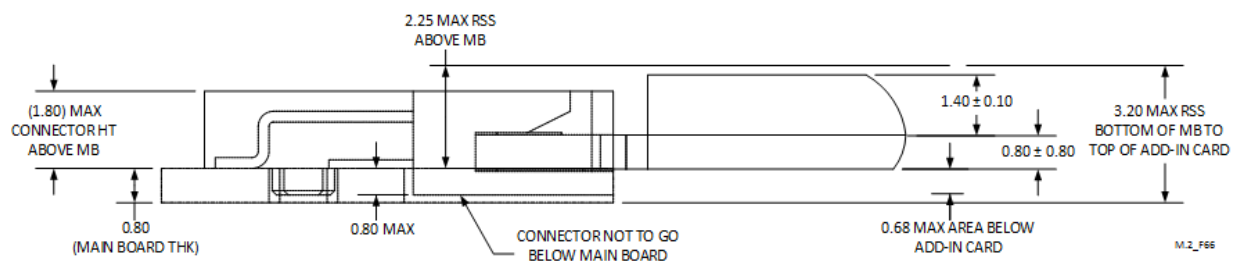
Figure 2-93. Stack-up Mid-mount (In-line) Single-sided (S3) Add-in Card for 1.5 Maximum Component Height

2.4.8.3.2. Double-sided Add-in Card

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 2-94 through Figure 2-98 show the profiles based on three top-side maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The bottom-side components maximum height is 1.5 mm, 1.35 mm, or 0.7 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card.
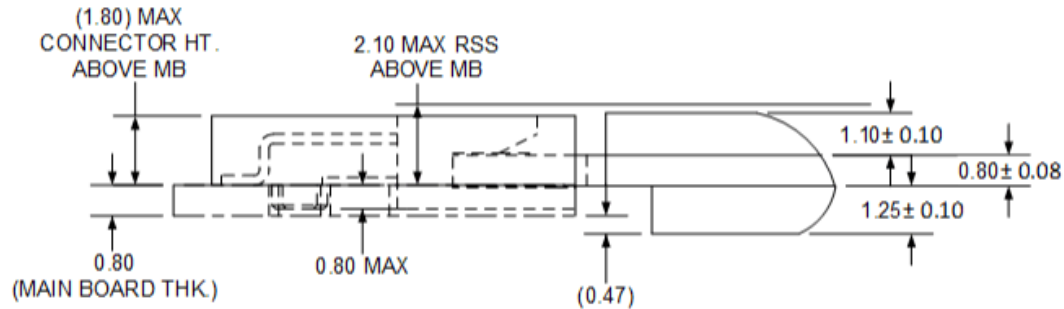
Figure 2-94. Stack-up Mid-mount (In-line) Double-sided (D1) Add-in Card for 1.2 Maximum Top-side Component Height
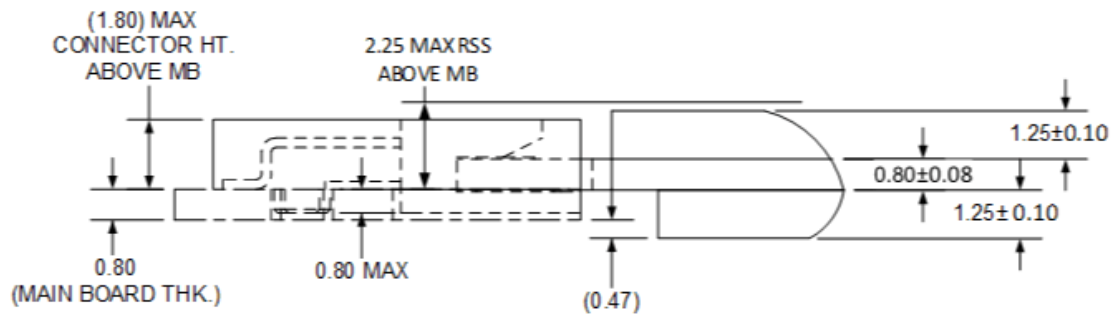
Figure 2-95. Stack-up Mid-mount (In-line) Double-sided (D2) Add-in Card for 1.35 Maximum Top-side Component Height
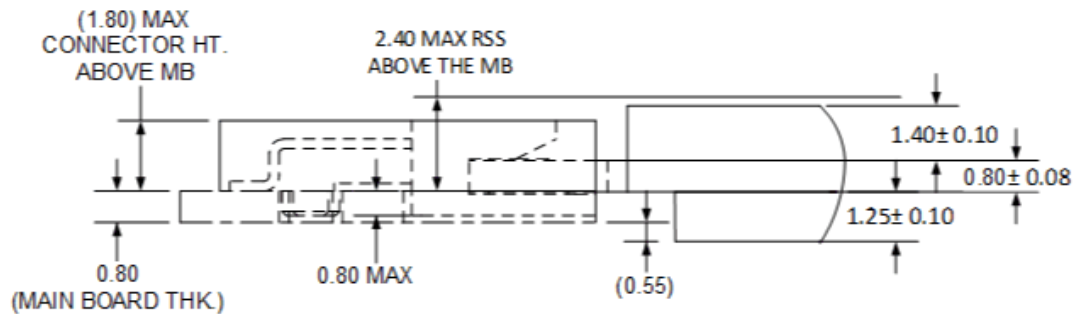
Figure 2-96. Stack-up Mid-mount (In-line) Double-sided (D3) Add-in Card for 1.5 Maximum Top-side Component Height
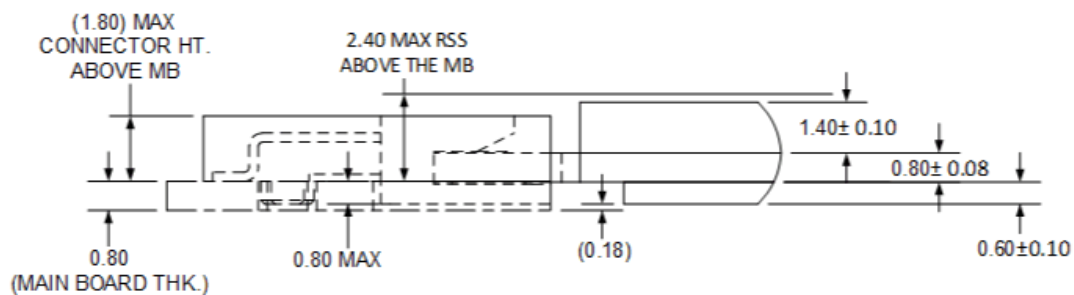
Figure 2-97. Stack-up Mid-mount (In-line) Double-sided (D4) Add-in Card for 1.5 Maximum Top-side Component Height
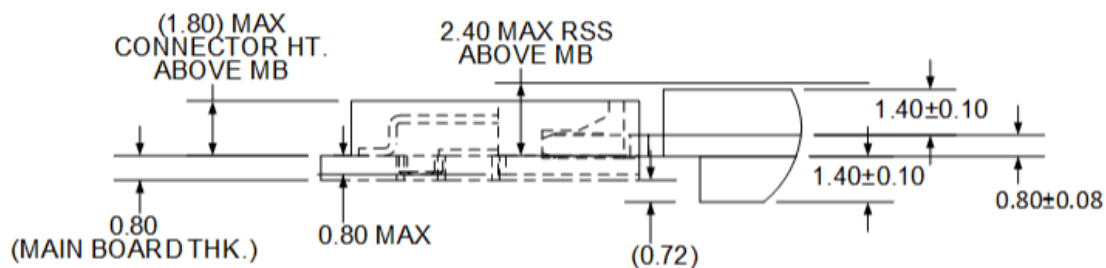
Figure 2-98. Stack-up Mid-mount (In-line) Double-sided (D5) Add-in Card for 1.5 Maximum Top-side and Bottom-side Component Height

2.4.8.4.   Mid-mount Connector Layout Pattern

The layout footprint of the Mid-mount connector on the Platform side is shown in the Figure 2-101. The land pattern includes all 75 pads although only up to 67 pads will be routed out while eight pads

will be redundant as they are located where the Mechanical Key is located. Figure 2-99 shows the eight redundant pads of Key B as faded.
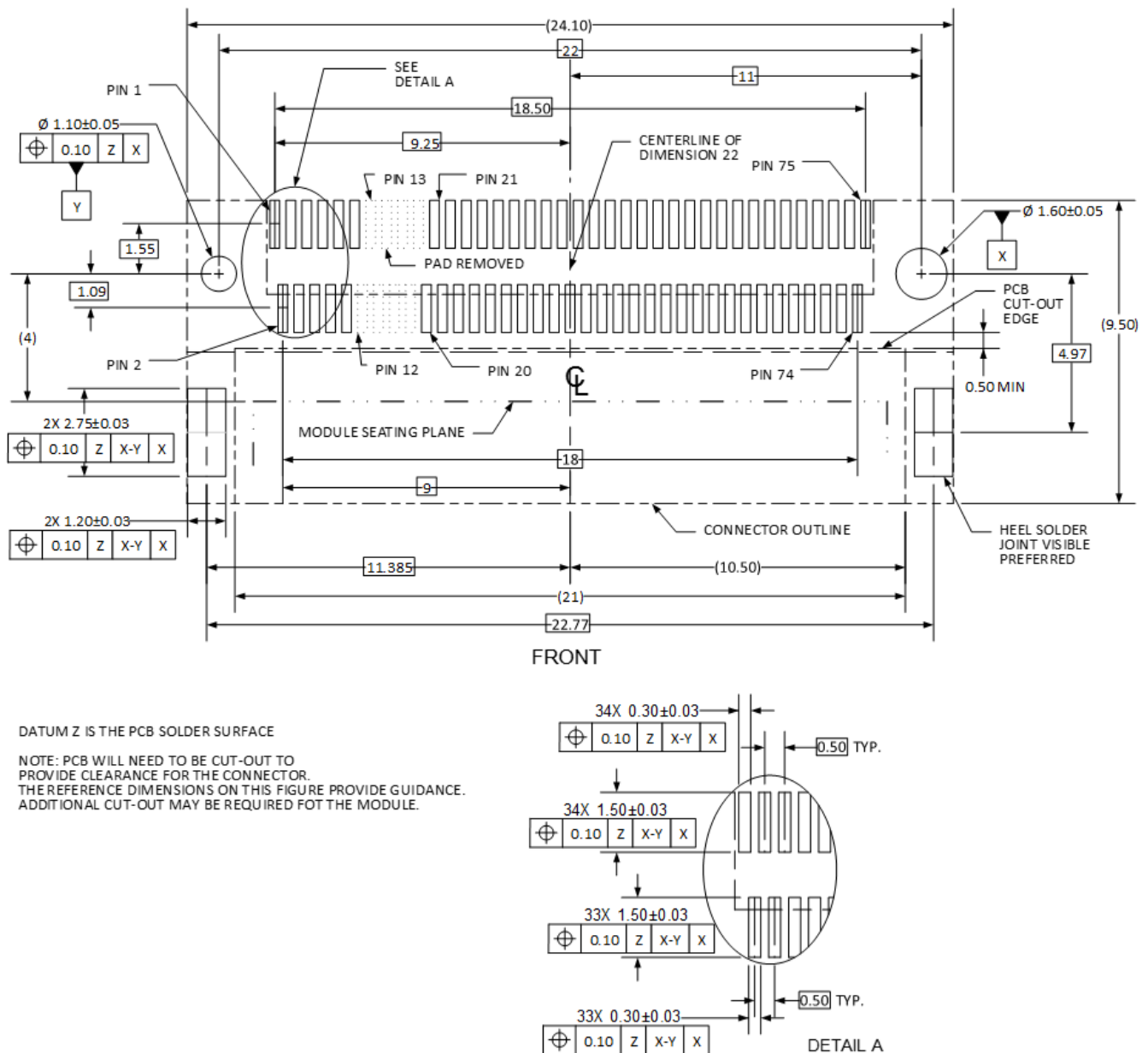
Figure 2-99. Example of Mid-mount Motherboard Land Pattern
Diagram – Key B Shown

2.4.8.5. Mid-mount M.2-1A Connector

The mid-mount connector is out of scope for M.2-1A designs in this specification.

2.4.9.   Connector Key Dimension

The width of the key is shown in Figure 2-100.
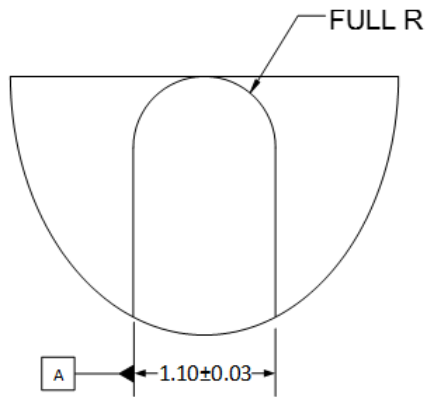
Figure 2-100. Connector Key

2.4.9.1.   Host Connector Keying

The generic 75-position edge card connector on the motherboard side will incorporate a mechanical keying scheme to enable mating with only a matching keyed Add-in Card. The mechanical key uses up eight pin locations (four on the top-side and four on the bottom-side). The generic 75-pin connector is able to accommodate 12 different mechanical Keys that are designated by a *Letter*. Each such Keyed connector has 67 usable pins available but at alternate pin locations within the generic 75 pin locations.

The Mechanical Key mechanism will enable the following:

❑   Each Socket on the motherboard with a different mechanical key location to signify a different pinout and functionality of that socket

❑   To prevent wrongful insertion of an incompatible Add-in Card into a wrong Socket connector on the motherboard, including the potential Add-in Card inversion. This is required for Safety reasons.

❑   Multiple Add-in Card key schemes that will enable insertion into more than one Socket

Mechanical keyed connectors that have their key locations within the first 49 pins (A, B, C, D, E, F, G, and H) also accommodates the smaller 49 pin versions of the M.2 form factors like the Type 1630 Add-in Card.

Figure 2-101 shows the relative location of the Mechanical Keys along the 75-positions. The Green and Blue marked areas are the locations of a reversed board showing that they do not coincide with the upright location of Keys. Assigning Key locations and making sure they are not interchangeable (upright or reversible) results in 12 distinct Keys.
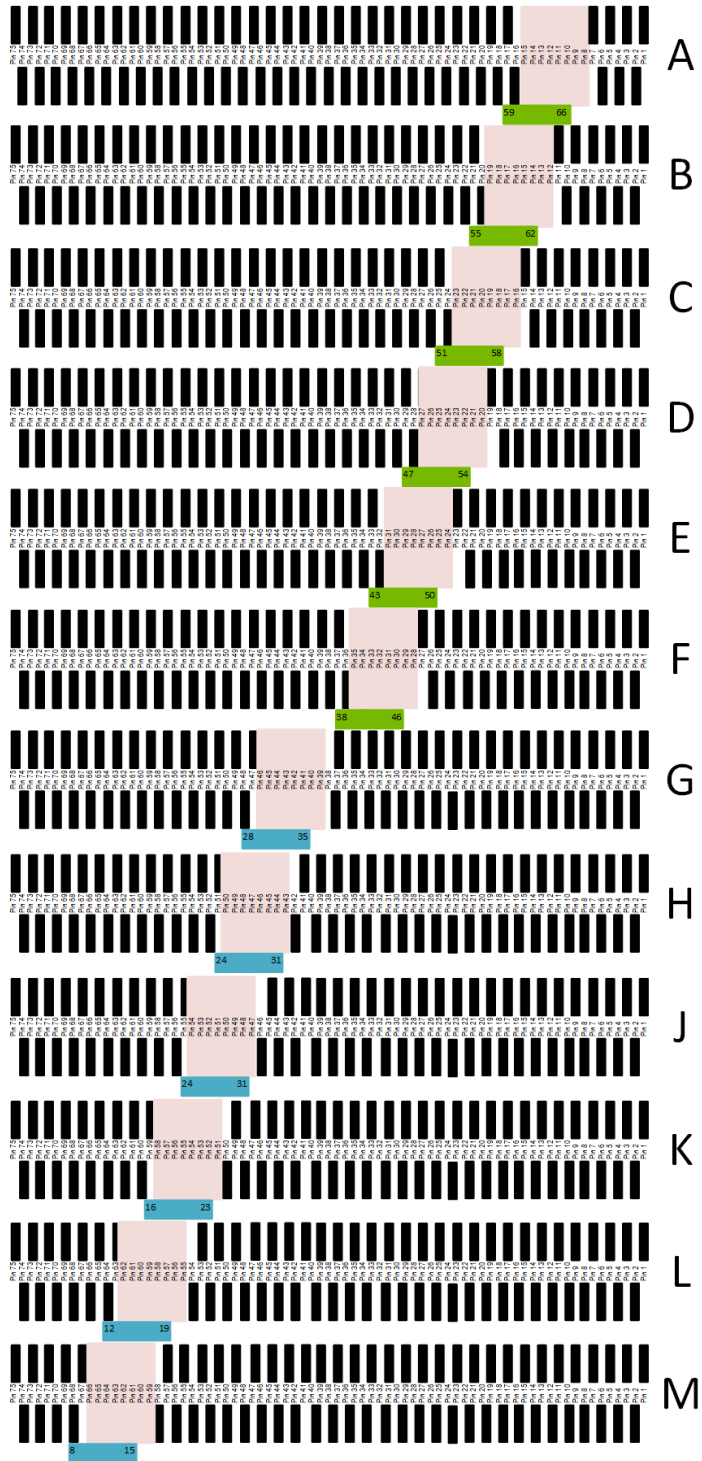
Figure 2-101.M.2 Connector Keying Diagram

This Connector Key/Add-in Card Key system enables some unique solutions in the form of a Dual Add-in Card key scheme. In such cases, an Add-in Card with dual keys would be able to plug into two different Keyed Connectors. However, single key Add-in Card intended for specific connector key would not be interchangeable. An example is shown in Figure 2-102.
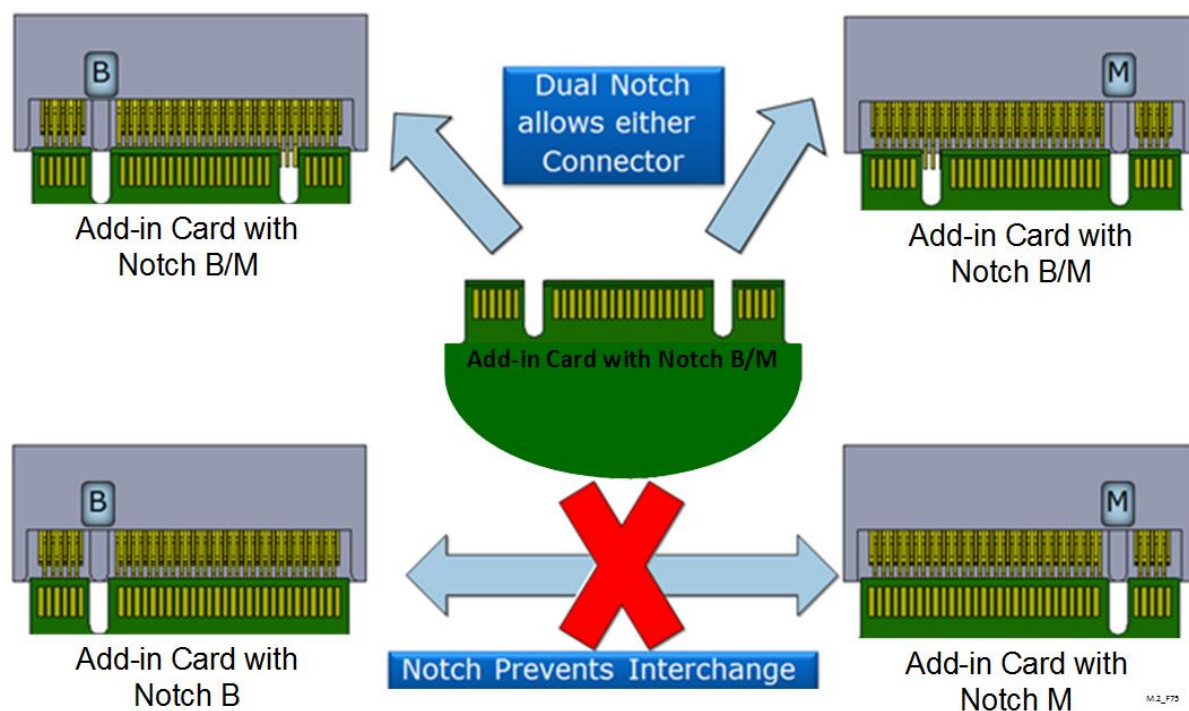
Figure 2-102.Dual Add-in Card Key Scheme Example

Such a scheme enables Add-in Cards to be plugged into two differently keyed connectors. For example, it is possible to plug a SSD Cache Add-in Card that incorporates a dual Add-in Card key to the WWAN/SSD/Other Socket 2 and be plugged into a dedicated SSD Drive Socket 3. More details of such an example are shown in the different Socket pinout section. This scheme is not limited to this example and is implemented in those cases where the pinouts supported are able to support this sort of scheme.

2.5. Module Stand-off

The Add-in Card will need a mechanical retention at the end of the board. The Add-in Card specifies a 5.5 mm diameter Keep-out zone at the end for attaching a screw. This section provides a guideline for using a M2 x 0.4 mm screw with a shoulder stand-off and a M3 x 0.5 mm screw. The guideline for the stand-off on the main board is recommending soldering down and assumed that the top-sided connectors are utilized. Alternatives are acceptable. The system will have to define the stand-off for utilizing the Mid-mount connectors.

2.5.1. Recommended Main Board Hole

The recommended plated-hole sizes for the main board are:

❑ Drill size 4.3 mm

❑ Finish size 4.2 ±0.075 mm

❑ Pad size 6.5 mm

2.5.2. Electrical Ground Path

The Add-in Card Stand-off and mounting screw also serve as part of the Add-in Card Electrical Ground path. The Stand-off must be connected directly to the ground (GND) plane on the Platform. When the Add-in Card is mounted, and the mounting screw is screwed on to hold the Add-in Card in place, this will make the electrical ground connection from the Add-in Card to the Platform ground plane.

2.5.3. Thermal Ground Path

The stand-off must provide a Thermal Ground Path. The design requirements for thermal are a material with a minimum conductivity of 50 watts per meter Kelvin and surface area of 22 mm^2 (see Figure 2-103).

WAFER HEAD STLYE
MAX HEAD THK. 1.20 mm
MAX HEAD DIA. 5.20 mm

LENGTH
TO BE DETERMINED
BY SYSTEM DESIGN
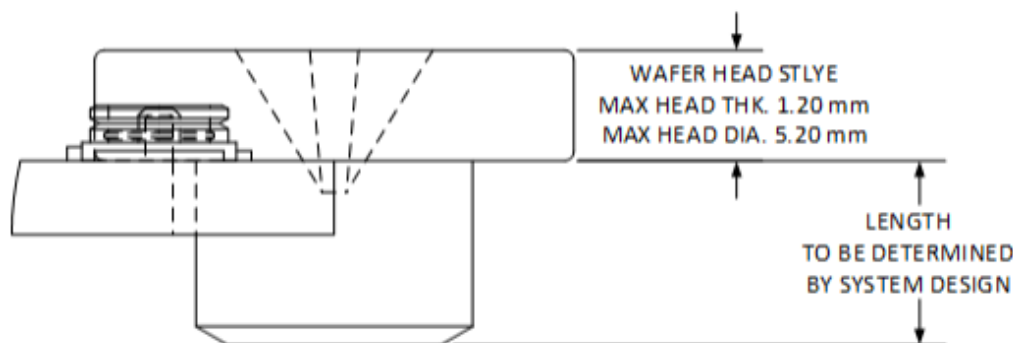
Figure 2-103.Mid-mount Add-in Card Mounting Interface

Top mount connectors will typically be complimented with a top mount stand-off. There are different types of stand-offs to coincide with the different height connectors as shown in the following figures:

❑ Figure 2-104. Single-sided Top Mount Solder-down Stand-off

❑ Figure 2-105. Elevated Single-sided Top Mount Solder Stand-off

❑ Figure 2-106. Low Profile Double-sided Top Mount Solder-down Stand-off

❑ Figure 2-107. Double-sided Top Mount Solder-down Stand-off

❑ Figure 2-108.   Elevated Double-sided Top Mount Solder-down Stand-off
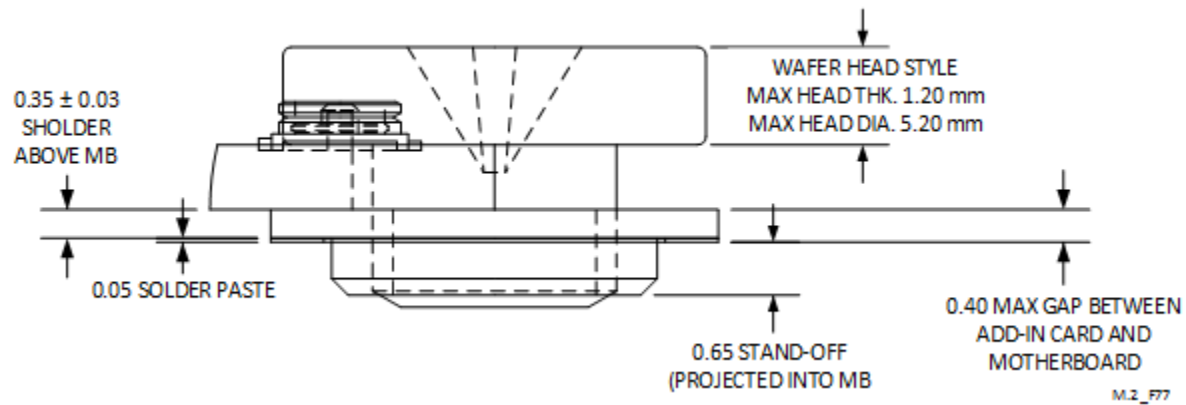
Figure 2-104. Single-sided Top Mount Solder-down Stand-off
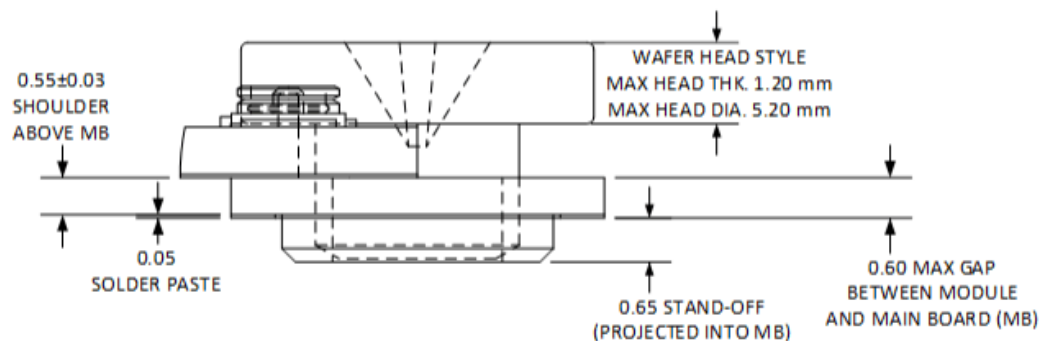
Figure 2-105. Elevated Single-sided Top Mount Solder Stand-off
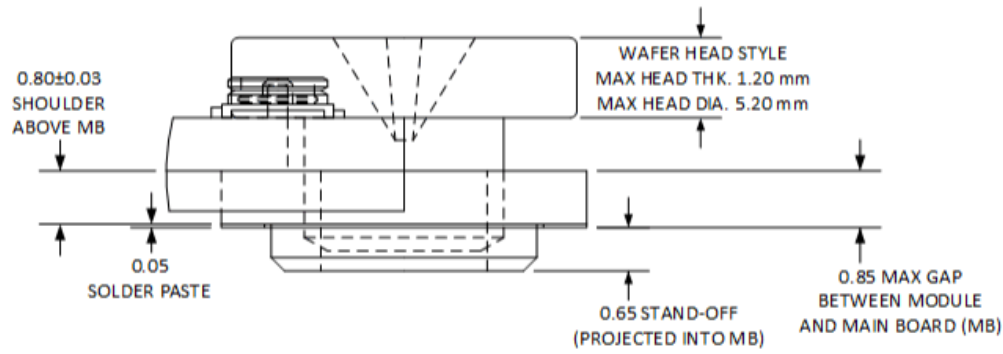
Figure 2-106. Low Profile Double-sided Top Mount Solder-down Stand-off
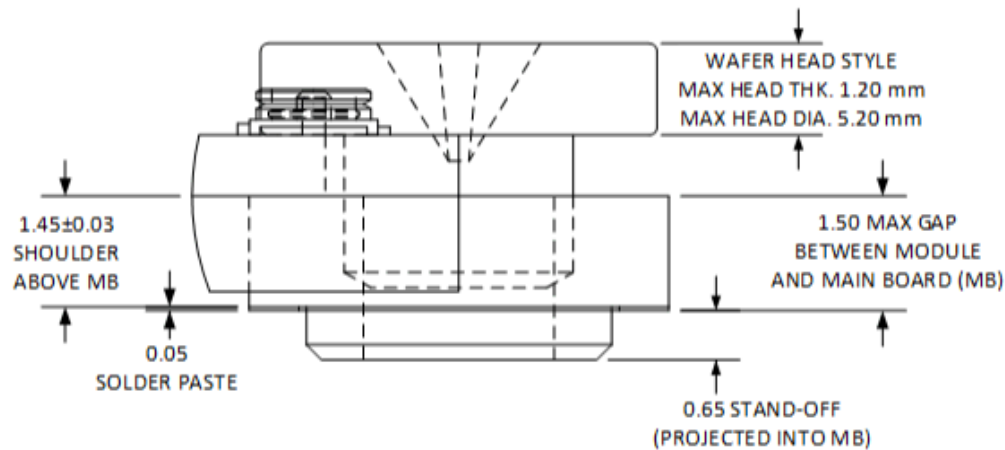
Figure 2-107. Double-sided Top Mount Solder-down Stand-off
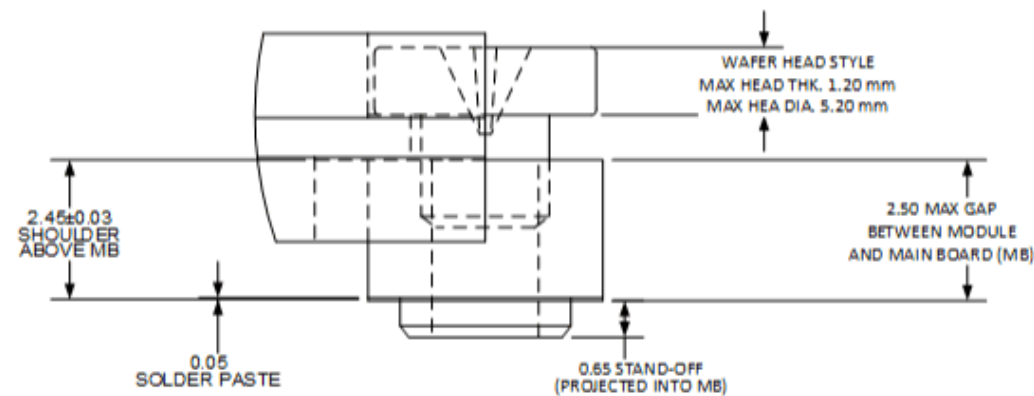
Figure 2-108.   Elevated Double-sided Top Mount Solder-down Stand-off

2.5.4.   Stand-off Guidelines

Figure 2-109 and Figure 2-110 provide a guideline for stand-offs for top-sided connectors.

2.5.4.1.   Stand-off Guidelines Option 1

A flat stand-off is a board-level SMT component (see Figure 2-109) and has an M3 x 0.5 thread. The height of the stand-off is determined by the connector used (see Table 2-15).
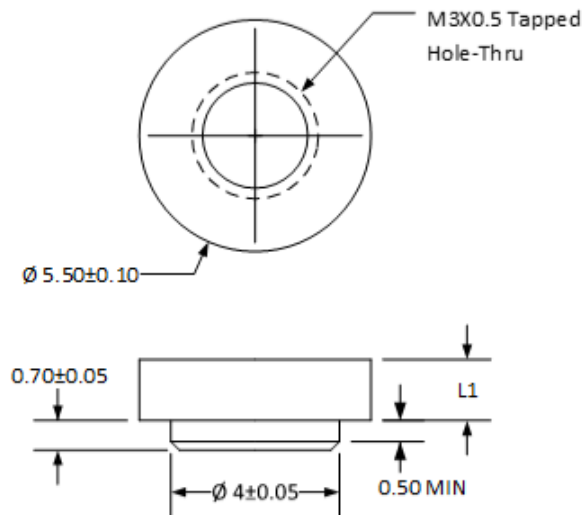
Figure 2-109.   Flat Stand-off

Table 2-15.   Stand-off Height Descriptor Table

Connector Height Descriptor	L1	L2
H2.3	0.35 ± 0.03	
H2.5	0.55 ± 0.03	
H2.8	0.80 ± 0.03	0.80 ± 0.03
H3.2	1.45 ± 0.03	1.45 ± 0.03
H4.2	2.45 ± 0.03	2.45 ± 0.03

Notes:
- Polyimide patch or tape required for vacuum pick-up
- Minimum thermal conductivity of 50 W/(mK) or greater
- Material = Steel
- Finish = Matte tin, 1.2 microns minimum average
- Tape and reel

2.5.4.2. Stand-off Guidelines Option 2

A shoulder stand-off is a board-level SMT component (see Figure 2-110) that has a M2 x 0.4 thread. The height of the stand-off is determined by the connector used (see Table 2-15).

> **Note:** For a single-side connector, the shoulder stand-off is not recommended due to the insertion being nearly horizontal. The shoulder makes insertion/removal of the Add-in Card difficult due to clearing the cut-out.
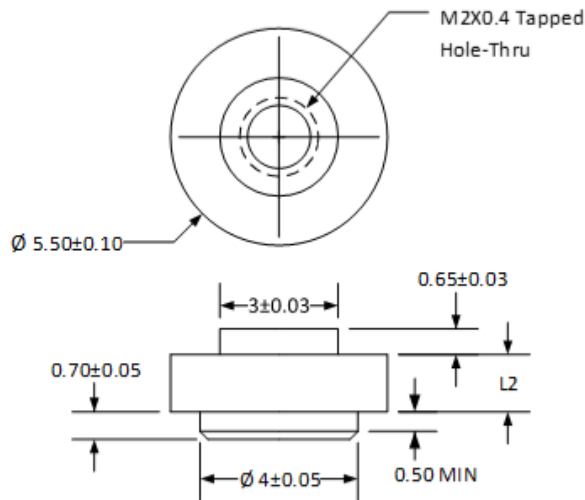
Figure 2-110.Shouldered Stand-off

2.5.5. Screw Selection Guideline

Screw selection consideration should be made according to the usage model. The tolerances of the connector, Add-in Card and stand-off allow for a gap to exist between the seating plane and the contact, see Figure 2-111.
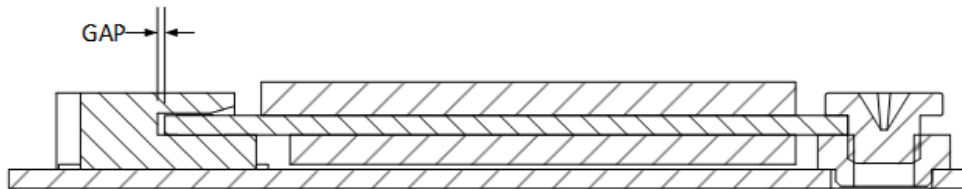
Figure 2-111.Screw Guidelines

2.5.5.1. Option 1, Wafer-head Style M3 Screw

Option 1 provides the guidelines for a wafer-head style M3 screw (see Figure 2-112). In using this screw type, the operator must be made aware that fully seating the Add-in Card is required prior to

securing the screw. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 2-15.
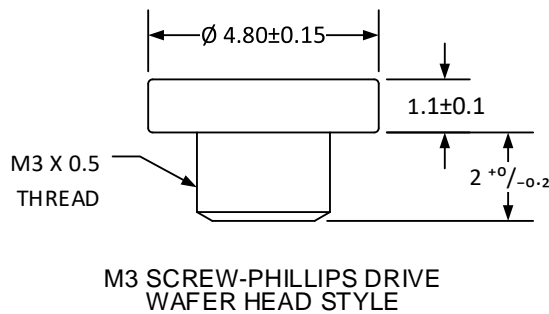
Figure 2-112. Wafer-head Style M3 Screw

2.5.5.2. Option 2, M3 Screw with Tapered Shaft

Option 2 provides the guidelines for a wafer-head style M3 screw (see Figure 2-113) with a tapered shaft. In using this screw type, the taper shaft acts as a mechanical guide to minimize the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 2-15.
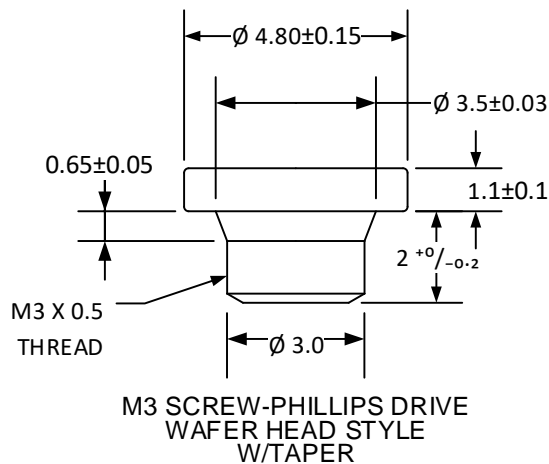
Figure 2-113. M3 Screw with Tapered Shaft

2.5.5.3. Option 3, Wafer-head Style M2 Screw

Option 3 provides the guidelines for a wafer-head style M2 screw (see Figure 2-114). This screw is intended for use only with the shouldered stand-off. It is not recommended to be used alone as the cut-out size provides a strong potential of not seating properly. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 2-15.

Ø 4.8±0.15

1.1±0.1

M2 X 0.4
THREAD

2.5 $^{+0}/_{-0.2}$

M2 SCREW-PHILLIPS DRIVE
WAFER HEAD STYLE
(USED WITH SHOULDER STAND-OFF)
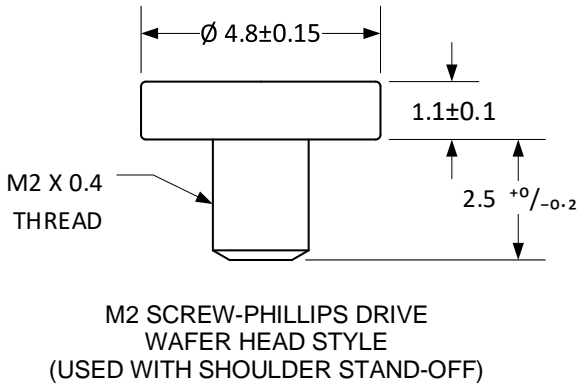
Figure 2-114. Wafer-head Style M2 Screw

2.5.5.4.   Option 4, Flat-head Style M3 Screw

Option 4 provides the guidelines for a flat-head style M3 screw (see Figure 2-115). In using this screw type the taper shaft acts as a mechanical guide to minimize the gap. Caution should be taken not to over torque the screw as it damages the barrel on the plated cut-out. This screw does offer a low-cost standard option providing a mechanism to mechanically control the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 2-15.

Ø 5.45±0.15

1.65±0.1

4 $^{+0}/_{-0.3}$

M3 X 0.5
THREAD

M3 SCREW-PHILLIPS DRIVE
FLAT HEAD STYLE
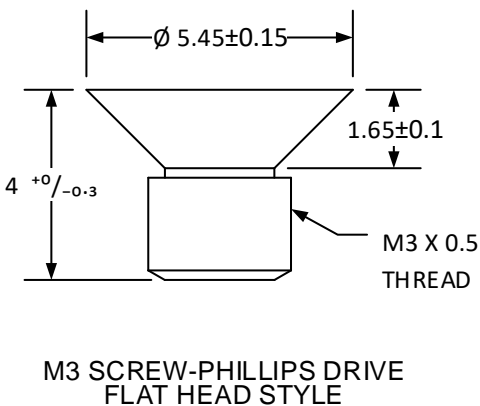
Figure 2-115. Flat-head Style M3 Screw

2.6.   Thermal Guidelines for the M.2

The following thermal guidelines are intended to provide guidance to system designers and Adapter designers using M.2. The thermal dissipation capability of any component or Adapter is a function of the surrounding thermal environment. This guideline gives direction on assessing power dissipation capability for generic Adapters in certain classes of systems when no special thermal enhancement is applied to the Adapter. It also gives the Adapter placement advice, although this advice should be considered informative rather than normative.

No specific maximum dissipation limits are given, as these limits are strongly system, use case, and system skin temperature dependent.

2.6.1. Objective

Establish dissipation response of Adapters, *Thermal Design Power*:

❑ By *generic* system environment (various categories defined, many assumptions)

❑ By card component type (generic packages, power maps defined)

❑ In presence of steady state dissipation in the rest of the system (use cases)

Based on limiting factors:

❑ Skin (exterior surface of casing) or display temperature limits

OR

❑ Die maximum temperature, if this limit is reached first

2.6.2. Introduction to Thermal Management

This section addresses some of the key concepts for Adapter thermal management. Since the connector forms a primary heat path to the main system board, thermal conditions on this board will provide a *background* temperature to an unpowered Adapter. Powering the Adapter increases its temperature as well as that of the surroundings: not only the board on which the connector is mounted but also nearby elements such as system casing, display if present, batteries, and keyboard.

2.6.2.1. Thermal Design Power Definition

The definition of Thermal Design Power (TDP) is worst case average dissipation over a time duration. The time scales for fan systems are in the one-minute range. The time scales for fanless systems are in the three-minute range. Die thermal time constants are on the order of milliseconds, while power transients occur over even shorter time durations. However, since the thermal mass of the surrounding system is significant, the longer response time is of interest.

Note that this longer time scale dissipation is quite different from the maximum power, or even *normal* power drawn by the Adapter, as these tend to occur on a duty cycle with much shorter time scales than the TDP. In addition, any power sent out through an antenna would subtract from the electrical power. The TDP is therefore always less than the maximum electrical power.

2.6.2.2. Skin Temperature Definition

For compact, portable systems, most of all the system's exterior surfaces (*casing* or *skin*) may be touched by the user. There are safety limits that apply to such surfaces, but the user's perception of *hot* is far lower than these safety limits. The perception is highly subjective and a matter of individual preference. Therefore, it is important for the system criteria to include a target temperature for various areas of the outer surface, and the conditions under which these should be met (ambient temperature, system activity, system orientation, area of system, size of hot spot, and so on). Some examples are given in this document, but these are intended only as examples and are not intended

to cover the complete range of all possibilities. Careful consideration of the intended user and environment is imperative.

Note that although the system's exterior housing is often called *skin*, this refers only to the casing material and not to the human skin that may be touching it. In fact, the act of touching the casing changes its temperature. The *perception* of temperature is less a matter of actual temperature than a question of the heat rate into the sensors embedded in human skin. This phenomenon is common in real life (e.g., the perception of *hot* by a young child is very different from the perception by calloused or older hands). The perception aspect of the surface temperature leads to a variety of limit definitions.

2.6.2.3.   Unpowered M.2 Adapter Temperature

The "background" or unpowered Adapter temperature is a function of motherboard *source* power, system environments, and other dissipation distributed around the system. This adiabatic or unpowered temperature is the **starting point for thermal ramp** as Adapter switches from off or idle (~0 W) to powered. Skin temperatures in the vicinity of the Adapter should be below the desired limits when the Adapter is in this state.

Other characteristics of the unpowered Adapter temperature are that it is nearly linear with **System power**; it is *specific to the individual system* (motherboard heat distribution, proximity of Adapters to other heat sources, cooling parameters, etc.); and the Adapter's own dissipation also raises temperatures of neighboring Adapters, motherboard, and system skin. These surrounding temperature increases are also roughly linear with **Adapter power**, and vary with Adapter characteristics (size, heat distribution, heat paths to surroundings) and are also specific to individual system design parameters. Therefore, these characteristics should be quantified for each system design. By extension, the results given in this document are meant to provide only an example of the approach to determining the dissipation response of Adapters.

2.6.2.4.   System Skin Temperature—Fan-based System

In a system that includes a fan, major heat sources are cooled by a thermal solution if needed and a fan. The air flow path is determined by vent placement, fan speed, obstructions, and so on. The cooling strategy should seek to maximize air flow for a given fan speed by reducing the pressure drop though the air path. As a general rule, sources of pressure drop that do not also accomplish a cooling task should be avoided as much as possible.

As skin temperature is a local heat density effect, it is important to flush air through the gap between skin and the Adapter. This will not completely prevent the Adapter heating the skin but does allows more of the Adapter heat to be exhausted from the system without having to pass through the casing. The Adapter dissipation limit depends on air speed, but the air speed depends on the gap size, vent placement, fan speed, and other parameters in the flow path both upstream and downstream.

Another approach to reducing skin temperature over Adapters is to include a long, narrow vent between high heat areas and the Adapter. The vent acts as a thermal break for the Adapter, but it will reduce the area of outer casing available for cooling the high heat components.

In some systems, the fan flow rate is severely restricted by the proximity of the system casing or other elements. The fan's inlet side is obstructed by the resulting narrow gap, and this alters the fan's characteristic curve from published data. Therefore, care should be taken to evaluate the true fan flow rate as installed in the system. In such systems, the low fan flow will exhaust proportionately less heat, leaving the remainder to pass through the casing as for fanless systems, below.

2.6.3.   System Skin Temperature—Fanless System

All heat dissipated inside the system, by any heat source, must pass *through* the casing (which has minimal temperature gradient through the material thickness, even if resin based) and dissipate off the exterior surface to the environment by radiation and natural convection. Thus, the surface temperature is *total system power* and *surface area dependent*. High emissivity of the outer surface in the long-infrared range (e.g., by paint, anodize or resin coating) is helpful for decreasing surface temperature. A metal casing produces more uniform skin temperature than resins but has more restrictive temperature limits. In most cases the heat spreading ability of the metal is beneficial to system cooling despite the lower temperature limits.

2.6.4.   Examples of Dissipation (TDP) Response of Adapters

Examples of dissipation (TDP) response of Adapters in systems are given in Section 6.5. The general trend is that the skin temperature of a system is dominated by the system's use-case and layout—changes in the Adapter TDP locally perturbs the skin temperature. Higher levels of fan ventilation reduce the sensitivity of local skin temperature to Adapter TDP.

3

3. Electrical Specifications

This chapter covers the electrical specifications for the PCI Express M.2 family of Adapters.

> All pinouts tables in this section are written from the Adapter point of view when referencing signal directions.

3.1. Connectivity Socket 1 Adapter Interface Signals

Table 3-1 applies to both Socket 1 SDIO-based and Socket 1 DisplayPort-based pinout versions.

Table 3-1. Socket 1 System Interface Signals and Voltage Table

Signal Group	Signal	I/O	Description	Voltage
Power	3.3 V (4 pins)	I	3.3 V source.	3.3 V
	VIO 1.8 V (1 pin)	I	I/O source (low current)	1.8 V Note 1
	GND		Return current path.	0 V
Wi-Fi-SDIO	SDIO_CLK	I	SDIO 3.0 Clock, 1.8 V for SDR25 and DDR50 mode.	1.8 V
	SDIO_CMD	I/O	SDIO Command Interface, 1.8 V for SDR25 and DDR50 mode.	1.8 V
	SDIO_DATA[0:3]	I/O	Four lines for SDIO data exchange, 1.8 V for SDR25 and DDR50 mode.	1.8 V
	SDIO_WAKE#	O	SDIO sideband Wake. Note: In band SDIO wake is not used for non-active modes. Active Low. Required pull up on the host side (recommended 15 kΩ to 100 kΩ).	1.8 V

Signal Group	Signal	I/O	Description	Voltage
	SDIO_ RESET#	I	SDIO sideband GPIO pin to enable/disable (reset) the Wi-Fi function. Platform firmware is required to assert/de-assert this pin on every boot (warm and cold). The Wi-Fi device uses 0.5 mW to 1 mW in reset. Active Low.	1.8 V
UART Additional parameters may be specified,	UART_RXD	I	UART Receive Data connected to TXD on the Platform.	1.8 V
	UART_TXD	O	UART Transmit Data connected to RXD on the Platform.	1.8 V
	UART_RTS	O	UART Ready to Send connected to CTS on the Platform.	1.8 V
	UART_CTS	I	UART Clear to Send connected to RTS on the Platform.	1.8 V
	UART_WAKE#	O	UART sideband used to Wake up Platform. Open Drain, Active Low. Require pull up on the host side (recommended 15 KΩ to 100 KΩ).	3.3 V
PCM (I2S)	PCM_CLK / I2S_SCK	I/O	PCM Clock/ I2S Continuous Serial Clock (SCK).	1.8 V
	PCM_SYNC / I2S_WS	I/O	PCM synchronous data SYNC/I2S Word Select.	1.8 V
	PCM_IN / I2S_SD_IN	I	PCM synchronous data Input/I2S Serial Data IN.	1.8 V
	PCM_OUT/ I2S_SD_OUT	O	PCM synchronous data Output/I2S Serial Data OUT.	1.8 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Base Specification*.	
	REFCLKp0/ REFCLKn0	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*.	
	PERST0#	I	PCIe Reset is a functional reset to the Adapter as defined by the *PCI Express Base Specification*.	3.3 V 1.8 V Note 2
	CLKREQ0#	I/O	PCIe Clock Request is a reference clock request signal as defined by the *PCI Express Base Specification*. It is also used by L1 PM Substates. Open Drain with pull up on Platform. Active Low.	3.3 V 1.8 V Note 2
	PEWAKE0#	I/O	PCIe WAKE#. Open Drain with pull-up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function-initiated wake event. When the Adapter supports OBFF mechanism, the PEWAKE# signal is used for OBFF signaling.	3.3 V 1.8 V Note 2

Signal Group	Signal	I/O	Description	Voltage
Optional Signals	VIO_CFG	O	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.	0 V/NC
USB	USB_D+, USB_D-	I/O	USB Data ± Differential serial data interface compliant to the *USB 2.0 Specification*.	
I2C	ALERT#	O	IRQ line to host processor. Open Drain with pull up on Platform. Active Low.	1.8 V
	I2C_CLK	I	I2C clock input from host. Open Drain with pull up on Platform.	1 8 V
	I2C_DATA	I/O	I2C data. Open Drain with pull up on Platform.	1.8 V
DisplayPort	DP_HPD	I/O	Hot Plug Detect. Direction is determined by DP_MLDIR.	3.3 V
	DP_MLDIR	I/O	DisplayPort data interface direction.	0 V/ 3.3 V / NC
	DP_AUXp/DP_AUXn	I/O	Auxiliary Channel; Bidirectional half-duplex AUX channel, DisplayPort v1.2, AUX channel 1 Mbit/s. Signal direction dictated by DP_MLDIR.	
	DP_ML0p/DP_ML0n, DP_ML1p/DP_ML1n, DP_ML2p/DP_ML2n, DP_ML3p/DP_ML3n,	I/O	Up to 4 Lane; Effective data rate 1.296 Gb/s, 2.16 Gb/s or 4.32 Gb/s per lane. DisplayPort main link data interface: four unidirectional differential pairs, signal direction dictated by DP_MLDIR.	
Communication-specific Signals	SUSCLK	I	Suspend Clock is a 32.768 kHz clock supply input that is provided by Platform to enable the Adapter to enter reduce power consumption modes. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	3.3 V 1.8 V Note 2
	W_DISABLE1# W_DISABLE2#	I	Active low, debounced signal when applied by the system it will disable radio operation on the Adapter that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the Adapter.	3.3 V 1.8 V Note 2
	LED_1# LED_2#	O	Open drain, active low signal. These signals are used to allow the Adapters to provide status indicators via LED devices that will be provided by the system.	3.3 V

Signal Group	Signal	I/O	Description	Voltage
	COEX_RXD COEX_TXD COEX3	I O I/O	Coexistence between Wi-Fi+BT and WWAN on Socket 2. UART_TXD and UART_RXD signals per BT-SIG coexistence protocol + an undefined signal.	1.8 V
	TX_BLANKING	I	TX_BLANKING GNSS Aiding signal from WWAN (see Section 3.2.12.3.1 for more information).	1.8 V
	SYSCLK	I	SYSCLK GNSS Aiding signal from WWAN (see Section 3.2.12.3.1 for more information).	1.8 V
NFC-UIM Signals	UIM_POWER_SRC/ GPIO_1	I	UICC power out from BB PMU.	Per ISO 7816 Spec
	UIM_POWER_SNK	O	NFC PMU power to the UICC.	
	UIM_SWP	I/O	UICC Secure element.	

Notes:
1. Required for PCIe-based Adapters that support 1.8 V sideband signaling.
2. Must be 3.3 V tolerant for Adapters that support 1.8 V sideband signaling. See Section 3.1. for more details. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters.

3.1.1. Power Sources and Grounds

PCI Express M.2 Socket 1 utilizes a single 3.3 V power sources. The voltage source, 3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving GND pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the GND planes within a card design.

The VIO 1.8 V power source is provided to supply the Adapter I/O buffer circuitry operating at 1.8 V sideband signaling. This power source is required for Adapters that support 1.8 V sideband signaling. Platforms that support 1.8 V sideband signaling must provide this power source. Adapters may provide 1.8 V sideband signaling based on the detection of this power source.

3.1.2. PCI Express Interface

The PCI Express interface supports a x1 (one Lane) or a x2 (two Lanes). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

Socket 1 pinouts has provision for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets serve as the second Lane to the original PCI Express interface, or alternatively, they are complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent Reserved pins to form a complete second PCI Express x1 interface.

IMPLEMENTATION NOTE: Lane Polarity

By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) are connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express M.2 Adapter. Similarly, by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) are connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express M.2 Adapter.

However, the **p** and **n** connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI Express receivers incorporate automatic Lane polarity inversion as part of the Link initialization and training and will correct the polarity independently on each Lane.

Refer to the *PCI Express Base Specification* for more information on Link initialization and training.

IMPLEMENTATION NOTE: Link Power Management

PCI Express M.2 Adapters that implement PCI Express interfaces are required by the *PCI Express Base Specification* to implement Link power management states, including optional support for the L0s and L1 states (in addition to the mandatory L0 and L3 states). For PCI Express M.2 implementations, Active State Power Management for both L0s and L1 states are enabled by default. Refer to the *PCI Express Base Specification* for more information regarding Active State Power Management.

3.1.3.   PCI Express Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture but may be required by specific implementations such as a PCI Express M.2 Device. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the 3.3 V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with 3.3 V. The use of the 3.3 V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Device and system connectors support the auxiliary signals that are described in the following sections.

3.1.3.1.   Reference Clock

The REFCLKp/REFCLKn is the 100 MHz common reference clock that must be used with PCIe. The REFCLKp/REFCLKn signals are used to assist the synchronization of the device's PCI Express interface timing circuits. Availability of the reference clock is gated by the CLKREQ# signal as described in Section 3.1.3.2. When the reference clock is not available, it will be in the *parked* state. A

parked state is when the clock is not being driven by a clock driver and both REFCLKp and REFCLKn are pulled to ground by the GND termination resistors. Refer to the *PCI Express Base Specification* for more details on the functional and tolerance requirements for the reference clock signals. M.2 Adapters and systems must comply to reference clock requirements in the *PCI Express Base Specification* and this specification.

Following clocking architectures will be supported:

❑ Common Reference Clock
❑ Separate Reference Clock with Independent SSC (SRIS)
❑ Separate Reference Clock No SSC (SRNS)

Table 3-2 shows Clocking Architectures supported by M.2 Platforms and Adapters.

Table 3-2.   M.2 Clocking Architecture Requirements

Clocking Architecture	PCIe 1.x, 2.x, 3.x		PCIe 4.0/5.0 Platform	PCIe 4.0/5.0 Adapter	Retimer	Carrier Card Riser
	Adapter	Platform				
Common Clock	Required	Required	Optional (Note 1)	Required	Implementation specific	
SRIS	N/A	N/A	Optional (Note 1)	Optional (Note 2)		
SRNS	N/A	N/A	Required if SRIS supported	Optional (Note 2)		

Notes
1. PCIe 4.0/5.0 Platforms must support one or both of these clocking Architectures.
2. PCIe 4.0/5.0 Adapters are allowed to support any combination of SRIS and SRNS.

The PCIe 4.0/5.0 Adapters are required to support Common Clock as default clocking architecture and are permitted to support SRIS (or SRNS or both). If PCIe 4.0/5.0 Adapters support multiple clocking architectures and the reference clock is not detected by the Adapter upon PERST# de-assertion, then PCIe 4.0/5.0 Adapters may switch into SRIS (or SRNS) mode.

PCIe 4.0/5.0 Platforms are required to support Common Clock architecture or SRIS/SRNS or both (Common Clock and SRIS/SRNS). PCIe 4.0/5.0 Platforms supporting SRIS are required to support SRNS. Refer to the *PCI Express Base Specification*.

If SRIS (or SRNS) is supported by both the PCIe 4.0/5.0 Platform and the PCIe 4.0/5.0 Adapter, then the PCIe 4.0/5.0 Platform is not required to provide the reference clock to the PCIe 4.0/5.0 Adapter. The PCIe 4.0/5.0 Platform is recommended to terminate the reference clock signals to GND with a pull-down resistor in that case.

Platforms and Adapters that support (PCIe 1.x, 2.x 3.x), are required to support Common Clock architecture only.

Clocking architectures supported for Retimers and Riser/Carrier cards are deemed implementation specific. For retimers, the clocking requirements will be different depending on the location of the Retimer. Similarly, for Carrier card/Riser implementations, the clocking requirements are determined by end points supported and the primary form factor supported.

Table 3-3 shows clocking details when supporting Common Clock Architecture. PCIe 1.x, 2.x, 3.x Platforms are required to source clock to the Adapters. PCIe 4.0/5.0 platforms, when supporting Common Clock Architecture, are required to source the clock to the Adapters.

CLKREQ# signal is required if L1 PM Substates are to be supported. This is applicable for both Common Clock and SRIS/SRNS modes.

Table 3-3.   M.2 Common Clock Architecture Details

Common Clock Architecture	PCIe 1.x, 2.x, 3.x		PCIe 4.0/5.0 Platform	PCIe 4.0/5.0 Adapter	Retimer	Carrier Card Riser
	Platform	Adapter				
Clock Source	Required	Not Allowed	Required	Not Allowed	Implementation specific	
SSC	Optional	N/A	Optional	N/A		
CLKREQ#	Optional	Optional	Optional	Optional		

Notes
   1. PCIe 4.0/5.0 Platforms must support one or both of these clocking Architectures.
   2. PCIe 4.0/5.0 Adapters are allowed to support any combination of SRIS and SRNS.

3.1.3.2.   REFCLK Phase Jitter Specification for 32.0 GT/s Systems

This specification details the requirements for measuring 100 MHz REFCLK for 32.0 GT/s capable systems using common clock architecture, at the M.2 connector. The phase jitter of the reference clock is to be measured using the behavioral CDR, TX and RX PLL functions specified in the *PCI Express Base Specification* for 32.0 GT/s.

The maximum allowed magnitude of the reference clock RMS Rj is given in Table 3-4. The RMS Rj requirement in Table 3-5 must be met irrespective of REFCLK having Spread Spectrum Clocking (SSC) enabled or disabled. Multiple methods can be used to measure the maximum allowed RMS Rj phase jitter value. Capture at least 160,000 clock intervals. (1.6 ms).

Table 3-4.   Maximum Allowed Reference Clock RMS Rj Phase Jitter

Data Rate	Maximum Rj RMS (fs)
32 GT/s	200

Note: Reference clock value in this table is referenced to 100 Ohm differential load at the end of an isolated (no crosstalk) 100 Ω trace.

3.1.3.3.   CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 device to request that the PCI Express reference clock be available (active clock state) to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control register (offset 010h). When

the Enable Clock Power Management bit is disabled, the CLKREQ# signal must be asserted at all times whenever power is applied to the device, with the exception that it is permitted to be de-asserted during L1 PM Substates. When the Enable Clock Power Management bit is enabled, the CLKREQ# signal is permitted to be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# is asserted by either the system or the device to initiate an L1 exit. Refer to the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Whenever dynamic clock management is enabled and when a device stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and devices must be tolerant of an active reference clock even when CLKREQ# is de-asserted by the device.

The device must drive the CLKREQ# signal low during power up, whenever the device is reset, and whenever the device requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# must be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when the device needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

Devices that do not implement a PCI Express interface must leave this CLKREQ# output unconnected.

CLKREQ# has additional electrical requirements over and above conventional open drain signals that allow it to be shared between devices that are powered off and other devices that are powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in D3$_{cold}$. This means that any component implementing CLKREQ# must be designed such that:

❑ Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-Ored" sources of CLKREQ#.

❑ When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-Ored together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.1.3.3.1. Dynamic Clock Control

If Clock Power Management is enabled in Link Control register (offset 010h) after a PCI Express device has powered up and its upstream link enters the L1 link state, it must allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}). Figure 3-1 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be considered when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state is additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.
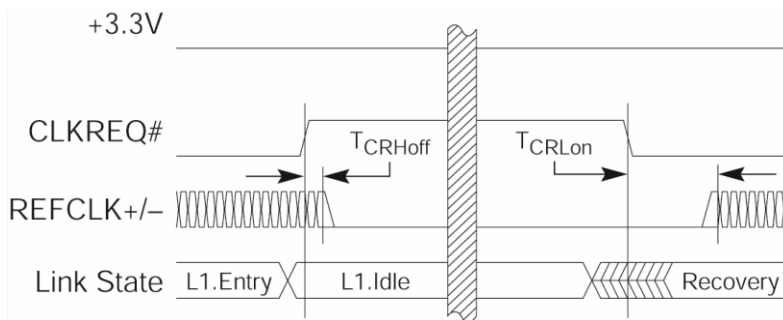
Figure 3-1.   CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the L1.Idle state before the device de-asserts CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports to minimize L1 exit latency. See Table 3-5 for CLKREQ# clock control timing.

Table 3-5.   Power-up CLKREQ# Timings

Symbol	Parameter	Min	Max	Units	Note
T_{CRHoff}	CLKREQ# de-asserted high to clock parked	0		ns	
T_{CRLon}	CLKREQ# asserted low to clock active		400	ns	See Note
Note: T_{CRLon} is allowed to exceed this value when LTR is supported and enabled for the device.					

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the system is permitted to ignore device's request to park reference clock. A device should also de-assert CLKREQ# when its link is in L2 or L3, much as it does during L1.

3.1.3.4.   Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol must be reported using the Clock Power Management bit in the Link Capabilities register (offset 00Ch). To enable dynamic clock management, the Enable Clock Power Management bit of the Link Control register (offset 010h) is provided. By default, the device must enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software subsequently disables this feature as needed. Refer to the *PCI Express Base Specification* for more information regarding these bits.

3.1.3.5.   PERST# Signal
❑ The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.
❑ PERST# must be used to initialize the card functions once power sources stabilize.
❑ PERST# is asserted when power is switched off and is used by the system to force a hardware reset on the card. The minimum assertion time for PERST# is defined as T_{PERST}.
❑ System must use PERST# to cause a warm reset of the Adapter.
❑ PERST# is asserted in advance of the power being switched off in a power-managed state like S3.
❑ PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition. The maximum delay to assert PERST# after any power level falls below minimum operating levels is defined as T_{FAIL}. M.2 Adapters and systems must comply to PERST# requirements in the *PCI Express Base Specification* and this specification.

3.1.3.6.   PEWAKE# Signal

PCI Express M.2 Cards must implement PEWAKE# if the card supports either the wakeup function or the OBFF mechanism. Refer to the WAKE# signal definition section in the *PCI Express Base Specification* for more details on the functional requirements for the PEWAKE# signal. M.2 Adapters and systems must comply to WAKE# requirements in the *PCI Express Base Specification* and PEWAKE# requirements in this specification.

> The PEWAKE# signal in this specification is referring to the PCIe WAKE# signal indicated in other PCIe-related specifications. The PE name prefix is intended to distinguish between this PCIe WAKE# and other host interface WAKE signals included in this specification.

3.1.4. Power-up Timing

Figure 3-2 shows an overview of the M.2 Adapter power-up sequence for an Adapter powered from the system power rail. Table 3-6 lists the power-up timing variable values.
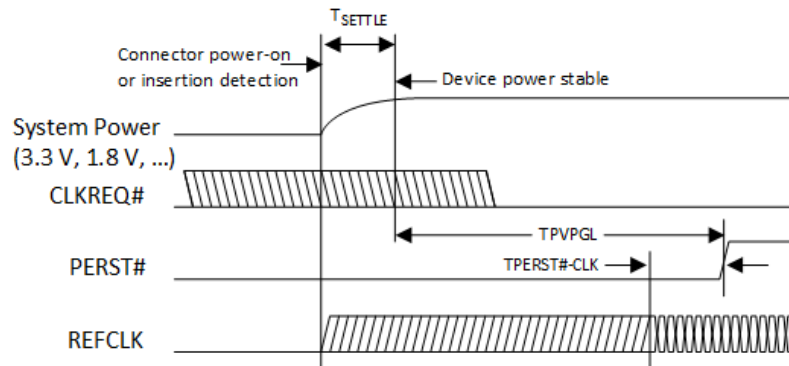
Note: T_{settle} is the time it takes all Power Rails to reach their minimum operating voltage (i.e., from all Power Rails at 0 V to the last Power Rail to reach its minimum valid operating voltage). All other PCI Express related timing events will begin once all the Power Rails have reached their minimum operating voltage. For example, a typical Adapter with a load capacitance of 330 µF and a 200 mA Soft-Start current limited ramp on the 3.3 V power rail, should settle within 5 ms.

Figure 3-2. Power-up Timing Sequence for an Adapter Powered from System Power Rail

Table 3-6. Power-up and Additional PERST Timing Variables

Symbol	Parameter	Min	Max	Units	Note
T_{PVPGL}	Power Valid to PERST# input inactive.	Note 1		ms	2
$T_{PERST\#-CLK}$	REFCLK stable before PERST# de-assertion	100		µs	
T_{FAIL}	Power level invalid to PERST# assertion		500	ns	
T_{PERST}	Assertion time of PERST#	100		µs	
$T_{PERSTSLEW}$	Slew rate of PERST# transition to de-asserted	50		mV/ns	3

Notes:
1. Implementation specific recommended 50 ms.
2. Power Valid when all the voltage supply rails have reached their respective V_{min}.
3. The slew rate of PERST# transition to de-asserted through its logic input switching range. (For VIL1 max to VIH1 min for 3.3 V signaling see Table 4-1. For VIL1 max to VIH1 min for 1.8 V signaling see Table 3-2.).

3.1.4.1. PERST# Power-up Timing

The host must delay de-assertion of PERST# for a period (T_{PVPGL}) after power is stable on the device (see Figure 3-2 and Figure 3-12). See Section 3.1.3.4 for further details on PERST#.

The value of T_{PVPGL} is left as implementation specific, with a recommended value as a guideline. In considering the value of T_{PVPGL}:

❑ Device and host implementers should consult PCI Express Reset Rules and Platform BIOS and OS requirements governing device readiness timing requirements following the de-assertion of PERST#.

❑ Host implementers should consult device vendors for their T_{PVPGL} values, based on VENDOR DEFINED device startup requirements.

3.1.4.2. REFCLK Power-up Timing

The host must ensure that the reference clock is in the active clock state for at least a period specified by $T_{PERST\#-CLK}$, prior to PERST# de-assertion. See Section 3.1.3.1 for further details on REFCLK.

3.1.4.3. CLKREQ# Power-up Timing

See Section 3.1.3.2 for details on CLKREQ#.

3.1.5. USB Interface

The USB interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). Since there is not a separate USB-controlled voltage bus, USB functions implemented on a PCI Express M.2 Adapter are expected to report as self-powered devices. All enumeration, bus protocol, and bus management features for this interface are defined by *Universal Serial Bus Specification*, Revision 2.0.

USB-based M.2 Adapters that implement a wakeup process are required to use the in-band wakeup protocol (across the USB_D+/USB_D– pins) as defined in the *Universal Serial Bus Specification*.

3.1.6. DisplayPort Interface

The DisplayPort interface supports a full-featured implementation as defined in the referenced *DisplayPort Standard Specification*. A full four lane implementation of the main link, the auxiliary channel, and hot plug detect (DP_HPD) is supported. Additionally, a system level signal, DP_MLDIR, is provided to assist in configuration of the Platform when a Display-M.2 Adapter is installed.

3.1.6.1. DP_HPD

The DP_HPD signal connects to the standard Hot Plug Detect signal of the DisplayPort interface. The intent of this signal is to indicate to the DisplayPort source that an active display is connected. The logical direction of DP_HPD is determined by the state of DP_MLDIR.

For a wireless display application, DP_HPD being asserted is an indication that the wireless link between the system and the remote display is fully operational. When DP_HPD is asserted, the host system software will know to locate and configure the remote display.

3.1.6.2. **DP_MLDIR**

The DP_MLDIR signal indicates the functional direction of the DisplayPort data and auxiliary interfaces on an M.2 Adapter (e.g., as a sink or source of the display-related interfaces). Based on the specific DisplayPort capabilities of the M.2 Adapter installed in the socket, the DP_MLDIR signal termination on the card must be as defined in Table 3-7.

For the M.2 Adapter that offers bi-directional DisplayPort capabilities, the mechanism for configuring the direction of the display interface is application and/or product-specific and not defined by this specification.

Table 3-7.   DP_MLDIR Pin Termination

Display-Capability on Display-M.2 Adapter	Example	DP_MLDIR Pin Termination on Display-M.2 Adapter
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to 3.3 V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

3.1.7.   SDIO Interface

The M.2 SDIO interface is comprised of the following Standard SDIO signals:

❑ SDIO_DATA[0:3]: Four bi-directional Data signals, each capable of data rates up to 208 Mb/s (for a total of 832 Mb/s)

❑ SDIO_CMD: One bi-directional CMD signal

❑ SDIO_CLK: One input Clock signal up to 208 MHz

These signals, supporting up to SDR104, are in accordance to standard SDIO specifications. Refer to the *SDIO 3.0 Specification* for more details on the functional requirements for the SDIO interface signals.

The M.2 SDIO interface also includes two non-standard signals in support of new features related to the SDIO interface. This includes the following signals:

❑ **SDIO_WAKE#**
This signal is an output from the Adapter (Comms Adapter) to the Platform used to trigger the wake to the host and to initiate SDIO interface communication between the Adapter and the Platform. This signal is an open drain output and needs to be pulled high by a Platform resistor to 1.8 V (recommended pull up value should be between 15 kΩ to 100 kΩ).

❑ **SDIO_RESET#**
This signal is an input to the Adapter from the Platform and it is used to reset the SDIO interface. The signal is 1.8 V at the Adapter input.

Since the SDIO_RESET# and SDIO_WAKE# are not part of the *SDIO 3.0 Specification*, the timing diagrams shown in Figure 3-3 and Figure 3-4 show their expected timing behavior. Table 3-8 lists the SDIO reset and power-up timing parameters.
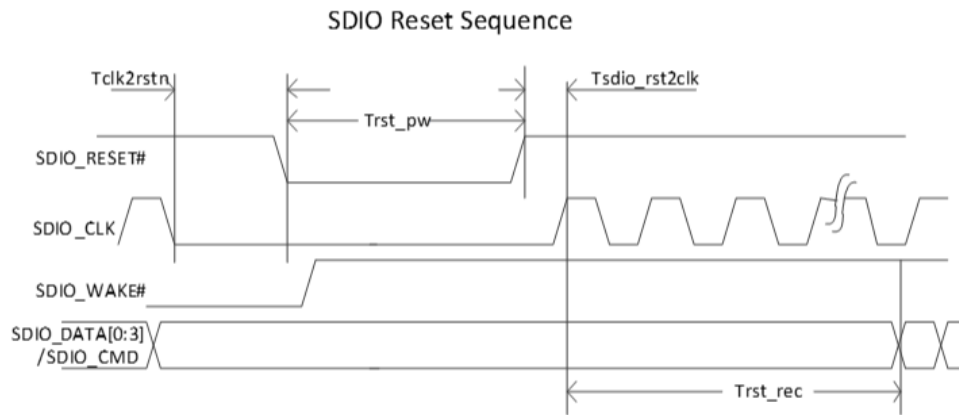
Figure 3-3.   SDIO Reset Sequence
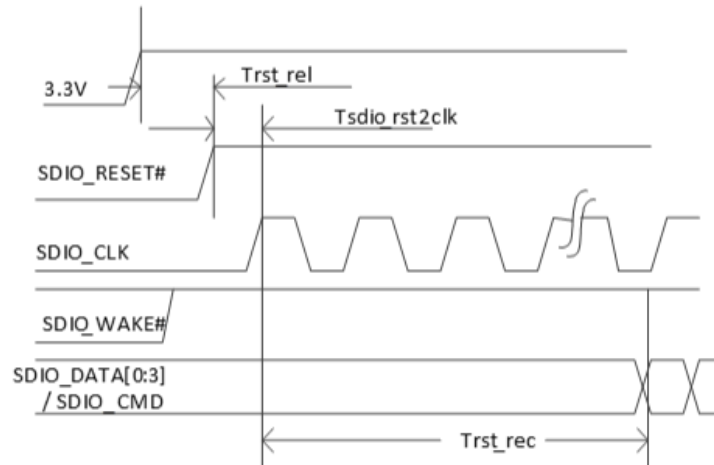
Figure 3-4.   SDIO Power-up Sequence

Table 3-8.   SDIO Reset and Power-up Timing

Symbol	Parameter	Min	Max	Unit
T_{rst_rel}	This time is measured from 3.3 V $\geq$ 2.9 V	1		μs
$T_{sdio\_rst2clk}$	10x clock cycles of 400 kHz	25		μs
T_{rst_rec}	The time needed to allow power up the DC/DC and some basic configuration operations	100		μs
$T_{clk2rstn}$		0		
T_{rst_pw}	Reset pulse width	10		μs

SDIO_WAKE# is asserted by the device at any given time and it is NOT bound by timing constraint. Yet, from functionality point of view it is expected that:

❑ The SDIO_WAKE# will be asserted (driven low) only when the host is in sleep and the device needs a service from the host.

❑ The SDIO_WAKE# will be asserted and will not de-assert before the source for the assertion is served in the device.

3.1.8. UART Interface

The Universal Asynchronous Receiver and Transmitter (UART) interface is used for communication with other host controllers or systems.

The UART handles 8-bit data frames and inserts one start and one stop bit (with/without parity). The format of the UART frame is in Figure 3-5.

| Idle | Start | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Parity | Stop | Idle |

| Idle | Start | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Stop | Idle |
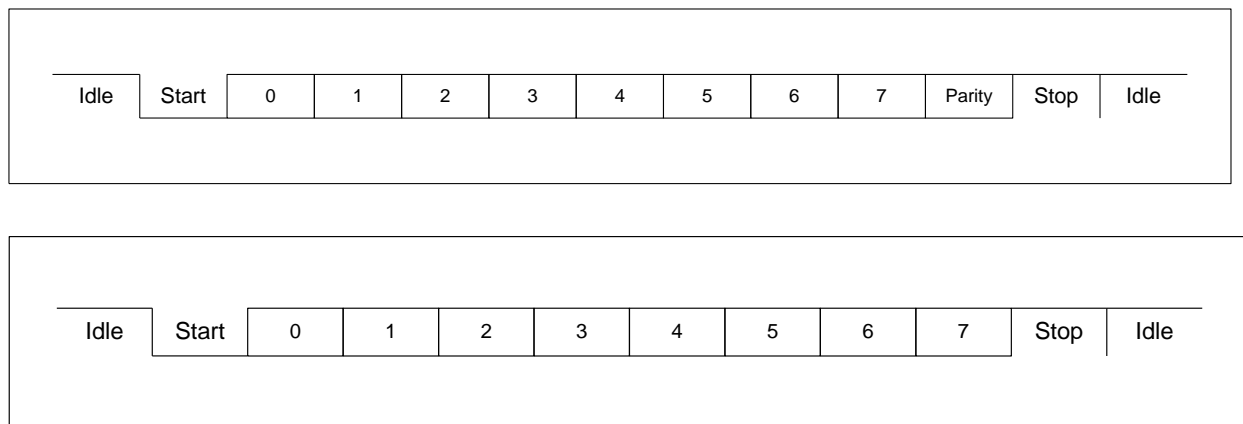
Figure 3-5. UART Frame Format

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

❑ UART_RXD (Input): Receive Data

❑ UART_TXD (Output): Transmit Data

❑ UART_RTS (Output): Request to Send (Host Flow Control)

❑ UART_CTS (Input): Clear to Send (Device Flow Control)

To enable additional power management protocols, an additional, non-standard UART interface is included:

❑ UART_WAKE# (Output): Host wake-up line is optional Out of Band in case the host does not support in band wake-up messaging.

3.1.8.1. UART_WAKE#

The UART_WAKE# signal is an Open Drain, Active Low signal used to Wake the Host or enable the Host to go into Sleep modes. The UART_WAKE# is used as an Out of Band signal to the Host in case the host does not support in-band wake up using an In-Band message. The UART_WAKE#

signal requires a pull up on the host side (recommended pull up value should be between 15 kΩ to 100 kΩ).

There are potentially many ways to make use of this Out of Band Wake signal and they are VENDOR DEFINED.

3.1.9.   PCM/I2S Interface

The following features are supported by the PCM interface:

- ❑ A 4-wire interface:
  - ● Clock signal
    PCM_CLK/I2S_SCK: Output if initiator, Input if target
  - ● Two frame signals
    PCM_SYNC/I2S_WS: Output if initiator, Input if target
  - ● Data in
    PCM_IN/I2S_SD_IN: Input
  - ● Data out signal
    PCM_OUT/I2S_SD_OUT: Output

- ❑ Single bidirectional PCM channels

- ❑ 16-bit and 24-bit data words

- ❑ Various PCM data sample rates including 8 kHz and 16 kHz are supported

The PCM/I2S mode is used for Standard (Narrowband) Mono speech or Wideband Mono speech. I2S will also be used for offloading of stereo audio data from the host (A2DP offload).

The PCM interface consists of four signals as shown in Figure 3-6.
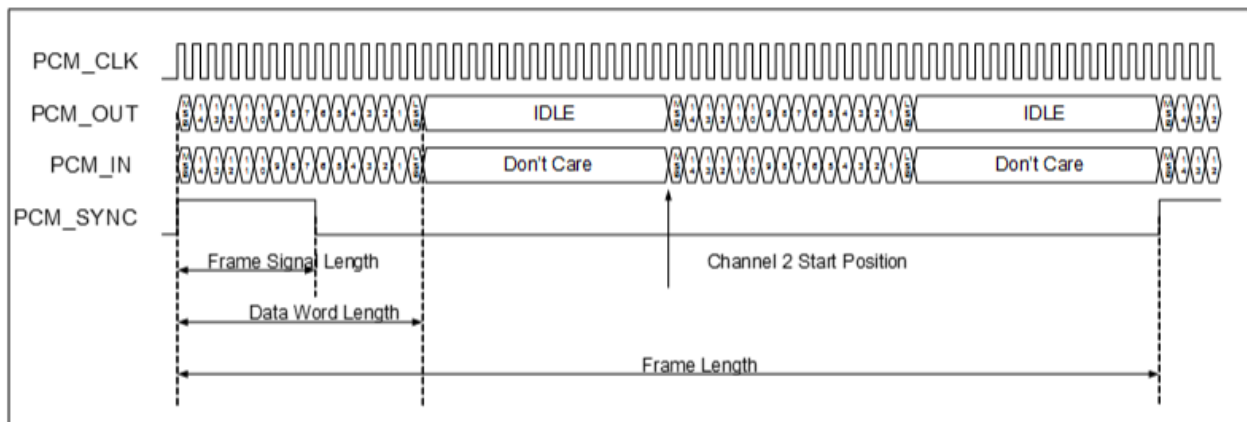
Figure 3-6.   Typical PCM Transaction Timing Diagram

The clock signal PCM_CLK is the timing base for the other signals in the PCM interface. In clock initiator mode, the Bluetooth device generates PCM_CLK from the internal system clock using a fractional divider. In clock target mode PCM_CLK is an input to the Bluetooth device and has to be supplied by an external source.

The PCM interface supports one bidirectional channel. Data is transmitted on PCM_OUT and received on PCM_IN, always with the most significant bit first. The 16-bit linear audio samples and 8-bit A-law or µ-law compressed audio samples are supported.

3.1.10. I2C Interface

3.1.10.1. ALERT# Signal

This ALERT# signal is intended to indicate to the Platform that the I2C device requires attention. This GPIO is used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.1.10.2. I2C_DATA Signal

The I2C_DATA signal is used to send the data packets from the host to the device according to the I2C protocol. The speed supported on this line depends on the host I2C_CLK signal speeds and the device processing capability.

3.1.10.3. I2C_CLK Signal

The I2C_CLK signal provides the clock signaling from the host to the device to be able to decode the data on the I2C_DATA line.

3.1.11. NFC Supplemental UIM Interface

The UIM_POWER_SRC, UIM_POWER_SNK, and UIM_SWP signals are supplemental NFC signals that are used when a UIM device is implemented as the Secure Element.

3.1.11.1. UIM_POWER_SRC

In systems where there is a WWAN device on one M.2 Adapter and an NFC solution on another M.2 Adapter, then the WWAN_UIM_PWR output must be routed to the UIM_POWER_SRC pin of the M.2 Adapter on which the NFC device is located. This UIM power signal is basically passed through the NFC device and output through the UIM_POWER_SNK signal described in the following paragraphs.

3.1.11.2. UIM_POWER_SNK

Refer to the ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements are provided by using any GND pin. Only PCI Express M.2 Adapters that support a UIM card are permitted to connect to this pin. If the Adapter has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (e.g., voltage) supported as defined in ISO/IEC 7816-3.

In this case, the UIM_POWER_SNK maps to contact number C1 as defined in ISO/IEC 7816-2.

3.1.11.3. **UIM_SWP**

NFC includes a SWP initiator using ETSI TS102.613 protocol version v7.8.0, v8.1.0, v9.1.0. SWP is a full duplex, auto-clocking interface. NFC (S1) sends using V-Domain, UICC/ SE (S2) sends using I-Domain, as described in ETSI TS102.613 in chapter 8 (Physical transmission layer).

3.1.11.4. **NFC Supplemental UIM Interface Wiring Example**

An example wiring diagram of the Supplemental NFC signals in conjunction with the Socket 2 and UIM/SIM device connections are shown in Figure 3-7.
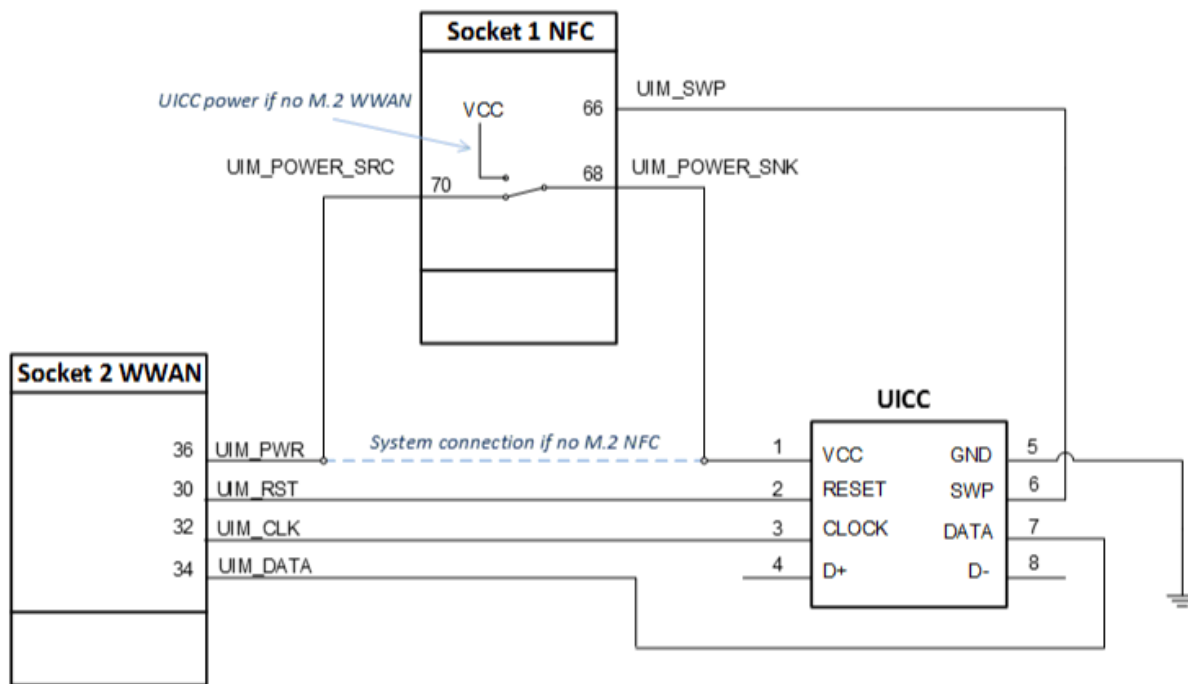
Figure 3-7.   Supplemental NFC Signal Connection Example

3.1.12.   **Communication-specific Signals**

3.1.12.1. **Suspend Clock**

The Suspend Clock (SUSCLK) is a slow clock signal running at 32.768 kHz. It is a buffered signal derived from the Platform RTC. The SUSCLK is available during Platform normal and suspend modes of operation, during which time the Adapter makes use of this SUSCLK signal as the clock source for critical keep alive circuitry as needed. The SUSCLK is not available in Platform hard shut down modes at which point, the 3.3 V power to the Adapter is also shut down. SUSCLK will have a duty cycle that is permitted to be as low as 30% or as high as 70%. Accuracy will be up to 200 ppm.

3.1.12.2. **Status Indicators**

Two LED# signals are provided to enable wireless communication Adapter to provide status indications to users via system provided indicators.

LED_1# and LED_2# output signals are active low and are intended to drive system-mounted LED indicators. These signals must be capable of sinking to ground a minimum of 9.0 mA at up to a maximum V_{OL} of 400 mV.

Figure 3-8 is an example of how such LEDs are typically connected in a Platform using 3.3 V.
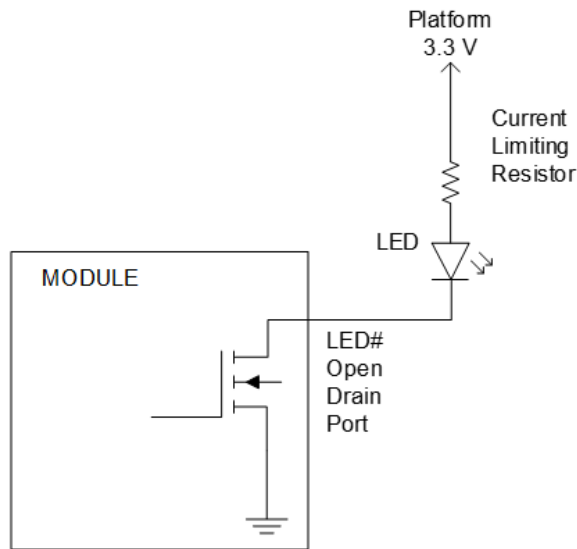
Figure 3-8.   Typical LED Connection Example in Platform/System

In a typical LED connection case, the current limiting resistor value will be in the 100 Ω range to enable the 9 mA current needed to light up the LED when tied up to a 3.3 V rail. Other Platform LED connections are possible including other alternate voltage sources. However, caution should be used to prevent back-biasing through the LED# pin in various power states.

Table 3-9 provides a simple indicator protocol for each of two defined LED states as applicable for wireless radio operation. Although the actual definition of the indicator protocol is established by the OEM system developer, the interpretations are useful in establishing a minimum common implementation across many Platforms.

Table 3-9.   Simple Indicator Protocol for LED States

State	Definition	Interpretation
OFF	The LED is emitting *no* light.	Radio is incapable of transmitting. This state is indicated when the card is not powered, a wireless disable signal is asserted to disable the radio, or when the radio is disabled by software.
ON	The LED is emitting light.	Radio is capable of transmitting.

State	Definition	Interpretation
		The LED should remain ON even if the radio is not actually transmitting. For example, the LED remains ON during temporary radio disablements performed by the M.2 Adapter of its own volition to do scanning, switching radios/bands, power management, etc.
		If the card is in a state wherein it is possible that radio begins transmitting without the system user performing any action, this LED should remain ON.

More advanced indicator protocols are allowed as defined by the OEM system developer. Advanced features are permitted to include use of blinking or intermittent ON states which are used to indicate radio operations such as scanning, associating, or data transfer activity. Also, use of blinking states might be useful in reducing LED power consumption.

3.1.12.3. W_DISABLE# Signal

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for wireless communications Adapters. These signals allow users to disable, via a system-provided switch, the Adapter's radio operation to meet public safety regulations or when otherwise desired. Implementation of wireless disable signals is applicable to systems and all Adapters that implement radio frequency capabilities. Multiple wireless disable signals are provided to ease managing multiple radios on a single Adapter. In cases where only one wireless disable signal is implemented by the system, the W_DISABLE1# signal must be used as the preferred control for collectively disabling all radios on the Adapters. By preferring W_DISABLE1# in these cases as the control for all on Adapter wireless Comms, the W_DISABLE2# is permitted to revert to a Reserved pin to be used for future assignment.

The wireless disable signals are active low signals that when asserted (driven low) by the system must disable radio operation. When implemented, a pull-up resistor between each wireless disable signal and 3.3 V is required on the card and should be in the range of 100 kΩ to 200 kΩ.

The assertion and de-assertion of each wireless disable signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by system circuitry.

When a wireless disable signal is asserted, all the radios associated with that signal must be disabled. When a wireless disable signal is not asserted, the associated radios transmit if not disabled by other means such as software. These signals are permitted to be shared between multiple M.2 Cards.

In normal operation, the card should disassociate with the wireless network and cease any further operations (transmit/receive) as soon as possible after the wireless disable signal is asserted. Given that a graceful disassociation with the wireless network fails to complete in a timely manner, the M.2 Adapter must discontinue any communications with the network and assure that its radio operation has ceased no later than 30 s following the initial assertion of the wireless disable signal. Once the disabling process is complete, the LED specific to the radio indicates the disabled condition to the user.

The card should initiate and indicate to the user the process of resuming normal operation within 1 s of de-assertion of the wireless disable signal. Due to the potential of a software disable state, the combination of both the software state and wireless disable signal assertion state must be determined

before resuming normal operation. Table 3-10 defines this requirement as a function of wireless disable signal and the software control setting such that the radio's RF operation remains disabled unless both the hardware and software are set to enable the RF features of the card.

The system is required to assure that each wireless disable signal be in a deterministic state (asserted or de-asserted) whenever power is applied to the Adapter (e.g., 3.3 V is present).

Table 3-10.   Radio Operational States

Wireless Disable	Signal SW Control Setting	Radio Operation
De-asserted (HIGH)	Enable Radio (see Note)	Enabled (RF operation allowed)
De-asserted (HIGH)	Disable Radio (see Note)	Disabled (no RF operation allowed)
Asserted (LOW)	Enable Radio (see Note)	Disabled (no RF operation allowed)
Asserted (LOW)	Disable Radio (see Note)	Disabled (no RF operation allowed)

Note: This control setting is implementation-specific and represents the collective intention of the host software to manage radio operation.

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for legacy wireless communications Adapters. It is anticipated that in the future the requirement for hardware wireless disable signals will be deprecated from use in favor of in-band mechanisms.

Specific implementations will be part of a BTO option determined specifically by the Adapter vendor and their customers. Supported options and functions are listed in Table 3-11.

Table 3-11.   Wireless Disable Pin Mode and Function Assignment

Wireless Disable	Pin Mode and Function					
	Wireless Disable Mode			Wi-Fi Bluetooth Mode		
	Function	Direction	Voltage	Function	Direction	Voltage
W_DISABLE1#	W_DISABLE1#	I	3.3 V	WI-FI_DISABLE#	I	1.8 V
W_DISABLE2#	W_DISABLE2#	I	3.3 V	BT_DISABLE#	I	1.8 V

Adapters that operate in Wi-Fi Bluetooth Mode may have additional behavior:

❑   Wi-Fi and Bluetooth disable signals are explicitly mapped to pin names.

❑   When the Wi-Fi radio is disabled it may reset the Wi-Fi feature on the Adapter.

❑   When the Bluetooth radio is disabled it may reset the Bluetooth feature on the Adapter.

3.1.12.4. Coexistence Signals

COEX_RXD, COEX_TXD and COEX3 are provided to allow for the implementation of wireless coexistence solutions between the radio(s) on the M.2 Adapter and other off-card radio(s). These other radios are either located on another M.2 Adapter located in the same host Platform or as alternate radio implementations (e.g., using a PCI Express Mini CEM or a proprietary form-factor add-in solution).

The COEX_RXD and COEX_TXD signals are for a UART communication path between the WWAN radio solution and the wireless solutions on the Connectivity Adapter. The coexistence protocol of these signals is based on the BT-SIG coexistence protocol.

❑ COEX_TXD is the UART transmit signal from the Connectivity Adapter to the WWAN solution.

❑ COEX_RXD is the UART receive signal from the WWAN solution to the Connectivity Adapter.

The pin assignment is seen in the pinout diagram and coincides with the signals in the Socket 2 pinouts.

The functional definition of the COEX3 pin is OEM-specific and should be coordinated between the host Platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host Platform.

3.1.13. Reserved Pins

It is expected that the Reserved pins are not terminated on either the Adapter or system board-side of the connector. These pins are reserved for definition in future revisions of this specification. Non-standard use of these pins may result in incompatibilities in solutions aligned with the future revisions.

3.1.14. Vendor Defined

These pins are vendor defined and fall under the BTO/CTO definitions between vendor and customer.

3.1.15. Optional Signals

3.1.15.1. VIO_CFG Signal

The VIO_CFG (IO voltage configuration) is a signal that indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. Adapters that use 3.3 V on sideband signals noted in Table 3-1must connect VIO_CFG directly to GND. Adapters that use 1.8 V sideband signaling (either through a voltage source on the Adapter or using the 1.8 V pins) must not connect the VIO_CFG pin and the affected signals on the Adapter must be 3.3 V tolerant. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters (e.g., prohibit applying power).

> **Note:** A 3.3 V only sideband signaling Adapter as indicated when VIO_CFG=GND is an indication that a 1.8 V only sideband signaling Platform should not attempt to utilize the Adapter. If an Adapter that supports 1.8 V sideband signaling as indicated by VIO_CFG=NC on the Adapter is in a 3.3 V only Platform (i.e., VIO 1.8 V is not supplied) then the Adapter has the option to either not function or locally generate 1.8 V to configure itself and be 3.3V tolerant.

3.1.16. Socket 1 Connector Pinout Definitions

All pinout tables in this section are written from the Add-in Card point of view when referencing signal directions.

The following tables illustrate signal pinouts for the **Add-in Card** edge card connector:

❑ Table 3-12. SDIO Based Add-in Card Pinouts (Key E).

❑ Table 3-13. DisplayPort Based Add-in Card Pinouts (Key A).

❑ Table 3-14. Socket 1 Add-in Card Pinouts (Key A-E).

There are also Module pinouts definitions for Type 1216, Type 2226, and Type 3026 LGA soldered down Modules in Section 3.1.17.

Table 3-12. SDIO Based Add-in Card Pinouts (Key E)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	RESERVED/REFCLKn1	73
72	3.3 V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PETn1	67
66	UIM_SWP/PERST1#	RESERVED/PETp1	65
64	VIO 1.8 V	GND	63
62	ALERT# (O)(0/1.8 V)	RESERVED/PERn1	61
60	I2C_CLK (I)(0/1.8 V)	RESERVED/PERp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (I)(0/1.8V/3.3V)	PEWAKE0# (I/O)(0/1.8V/3.3V)	55
54	W_DISABLE2# (I)(0/1.8V/3.3V)	CLKREQ0# (I/O)(0/1.8V/3.3V)	53
52	PERST0# (I)(0/1.8V/3.3V)	GND	51
50	SUSCLK (I)(0/1.8V/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	UART_CTS (I)(0/1.8V)	PERp0	35
34	UART_RTS (O)(0/1.8V)	GND	33
32	UART_RXD (I)(0/1.8V)	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	SDIO_RESET#/TX_BLANKING (I)(0/1.8V)	23
22	UART_TXD (O)(0/1.8V)	SDIO_WAKE# (O)(0/1.8V)	21
20	UART_WAKE# (O)(0/3.3V)	SDIO_DATA3 (I/O)(0/1.8V)	19
18	VIO_CFG (O)	SDIO_DATA2 (I/O)(0/1.8V)	17
16	LED_2# (O)(OD)	SDIO_DATA1 (I/O)(0/1.8V)	15
14	PCM_IN/I2S_SD_IN (I)(0/1.8V)	SDIO_DATA0 (I/O)(0/1.8V)	13
12	PCM_OUT/I2S_SD_OUT (O)(0/1.8V)	SDIO_CMD (I/O)(0/1.8V)	11
10	PCM_SYNC/I2S_WS (I/O)(0/1.8V)	SDIO_CLK/SYSCLK (I)(0/1.8V)	9
8	PCM_CLK/I2S_SCK (I/O)(0/1.8V)	GND	7
6	LED_1# (O)(OD)	USB_D-	5
4	3.3 V	USB_D+	3
2	3.3 V	GND	1

Table 3-13.   DisplayPort Based Add-in Card Pinouts (Key A)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	REFCLKn1	73
72	3.3 V	REFCLKp1	71
70	PEWAKE1# (I/O)(0/3.3V)	GND	69
68	CLKREQ1# (I/O)(0/3.3V)	PETn1	67
66	PERST1# (I)(0/3.3V)	PETp1	65
64	VIO 1.8 V	GND	63
62	ALERT# (O)(0/1.8V)	PERn1	61
60	I2C_CLK (I)(0/1.8V)	PERp1	59
58	I2C_DATA (I/O)(0/1.8V)	GND	57
56	W_DISABLE1# (I)(0/1.8V/3.3V)	PEWAKE0# (I/O)(0/1.8V/3.3V)	55
54	W_DISABLE2# (I)(0/1.8V/3.3V)	CLKREQ0# (I/O)(0/1.8V/3.3V)	53
52	PERST0# (I)(0/1.8V/3.3V)	GND	51
50	SUSCLK (I)(0/1.8V/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	GND	PERp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (I/O)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DL_ML3n	19
18	VIO_CFG (O)	DP_MLDIR GND (I)/3.3V (O)/NC (I/O)	17
16	LED_2# (O)(OD)		
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
6	LED_1# (O)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

Table 3-14.   Socket 1 Add-in Card Pinouts (Key A-E)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	RESERVED/REFCLKn1	73
72	3.3 V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PETn1	67
66	UIM_SWP/PERST1#	RESERVED/PETp1	65
64	VIO 1.8 V	GND	63
62	ALERT# (O)(0/1.8 V)	RESERVED/PERn1	61
60	I2C_CLK (I)(0/1.8 V)	RESERVED/PERp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (I)(0/1.8V/3.3V)	PEWAKE0# (I/O)(0/1.8V/3.3V)	55
54	W_DISABLE2# (I)(0/1.8V/3.3V)	CLKREQ0# (I/O)(0/1.8V/3.3V)	53
52	PERST0# (I)(0/1.8V/3.3V)	GND	51
50	SUSCLK (I)(0/1.8V/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	NC	PERp0	35
34	NC	GND	33
32	NC	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	ADD-IN CARD KEY E	
	ADD-IN CARD KEY E	NC	23
22	NC	NC	21
20	NC	NC	19
18	VIO_CFG (O)	NC	17
16	LED_2# (O)(OD)	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
	ADD-IN CARD KEY A	ADD-IN CARD KEY A	
6	LED_1# (O)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

3.1.17. Socket 1 Based Soldered-down Module Pinouts

All pinouts tables in this section are written from the Module point of view when referencing signal directions.

This section contains the Module pinouts maps for Type 2226, Type 1216, and Type 3026 LGA soldered-down Modules:

- ❑ Figure 3-9. Type 2226 SDIO Based Module-side Pinout
- ❑ Figure 3-10. Type 1216 SDIO Based Module-side Pinout
- ❑ Figure 3-11. Type 3026 DisplayPort Pinouts Extension Over an SDIO Based Module-side Pinout
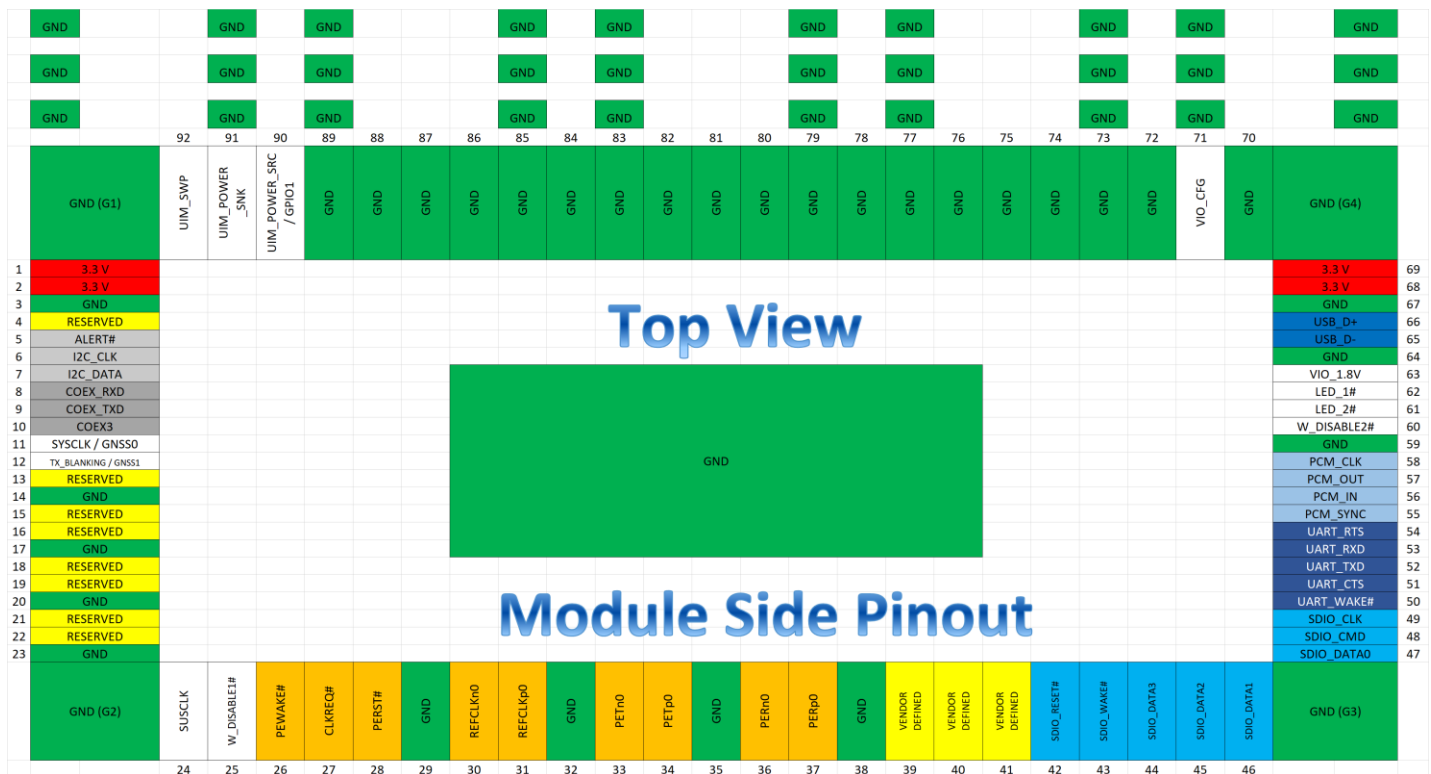
Figure 3-9. Type 2226 SDIO Based Module-side Pinout

##		96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77		
	GND (G1)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND (G4)	
1	UIM_POWER_SRC / GPIO1																					VIO_CFG	76
2	UIM_POWER_SNK																					GND	75
3	UIM_SWP																					GND	74
4	3.3 V					GND									GND							3.3 V	73
5	3.3 V																					3.3 V	72
6	GND																					GND	71
7	RESERVED																					USB_D+	70
8	ALERT#																					USB_D-	69
9	I2C_CLK																					GND	68
10	I2C_DATA					GND									GND							RESERVED	67
11	COEX_RXD																					VIO_1.8V	66
12	COEX_TXD																					LED_1#	65
13	COEX3																					LED_2#	64
14	SYSCLK / GNSS0																					W_DISABLE2#	63
15	TX_BLANKING / GNSS1																					GND	62
16	RESERVED																					PCM_CLK	61
17	GND					GND									GND							PCM_OUT	60
18	RESERVED																					PCM_IN	59
19	RESERVED																					PCM_SYNC	58
20	GND																					UART_RTS	57
21	PETn1																					UART_RXD	56
22	PETp1																					UART_TXD	55
23	GND					GND									GND							UART_CTS	54
24	PERn1																					UART_WAKE#	53
25	PERp1																					SDIO_CLK	52
26	GND																					SDIO_CMD	51
27	SUSCLK																					SDIO_DATA0	50
28	W_DISABLE1#																					SDIO_DATA1	49
	GND (G2)	PEWAKE#	CLKREQ#	PERST#	GND	REFCLKn0	REFCLKp0	GND	PETn0	PETp0	GND	PERn0	PERp0	GND	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	SDIO_RESET#	SDIO_WAKE#	SDIO_DATA3	SDIO_DATA2	GND (G3)	
		29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48		

Top View

Module Side Pinout

Figure 3-10. Type 1216 SDIO Based Module-side Pinout

Figure 3-11 — Type 3026 DisplayPort Pinouts (Top View, Module Side Pinout)

Module-side pin assignments:

Pin	Signal	Pin	Signal
93	3.3 V	1	3.3 V
94	3.3 V	2	3.3 V
95	GND	3	GND
96	RESERVED	4	RESERVED
97	RESERVED	5	ALERT#
98	RESERVED	6	I2C_CLK
99	RESERVED	7	I2C_DATA
100	RESERVED	8	COEX_RXD
101	RESERVED	9	COEX_TXD
102	GND	10	COEX3
103	PEWAKE1#	11	SYSCLK / GNSS0
104	CLKREQ1#	12	TX_BLANKING / GNSS1
105	PERST1#	13	RESERVED
106	GND	14	GND
107	REFCLKn1	15	RESERVED
108	REFCLKp1	16	RESERVED
109	GND	17	GND
110	PETn1	18	RESERVED
111	PETp1	19	RESERVED
112	GND	20	GND
113	PERn1	21	RESERVED
114	PERp1	22	RESERVED
115	GND	23	GND

Pin	Signal	Pin	Signal
69	3.3 V	142	3.3 V
68	3.3 V	141	3.3 V
67	GND	140	GND
66	USB_D+	139	RESERVED
65	USB_D-	138	RESERVED
64	GND	137	GND
63	VIO_1.8V	136	DP_AUXn
62	LED_1#	135	DP_AUXp
61	LED_2#	134	GND
60	W_DISABLE2#	133	DP_ML3n
59	GND	132	DP_ML3p
58	PCM_CLK	131	GND
57	PCM_OUT	130	DP_ML2n
56	PCM_IN	129	DP_ML2p
55	PCM_SYNC	128	GND
54	UART_RTS	127	DP_ML1n
53	UART_RXD	126	DP_ML1p
52	UART_TXD	125	GND
51	UART_CTS	124	DP_ML0n
50	UART_WAKE#	123	DP_ML0p
49	SDIO_CLK	122	GND
48	SDIO_CMD	121	DP_HPD
47	SDIO_DATA0	120	DP_MLDIR (GND/3.3 V/NC)

Bottom row:

Pin	Signal
24	SUSCLK
25	W_DISABLE1#
26	PEWAKE#
27	CLKREQ#
28	PERST#
29	GND
30	REFCLKn0
31	REFCLKp0
32	GND
33	PETn0
34	PETp0
35	GND
36	PERn0
37	PERp0
38	GND
39	VENDOR DEFINED
40	VENDOR DEFINED
41	VENDOR DEFINED
42	SDIO_RESET#
43	SDIO_WAKE#
44	SDIO_DATA3
45	SDIO_DATA2
46	SDIO_DATA1

Top/bottom GND pads: UIM_SWP, UIM_POWER_SNK, UIM_POWER_SRC/GPIO1, VIO_CFG; GND groups (G1–G8); Empty and RESERVED pads as marked. Top row pins: 146, 145, 92, 91, 90, 89, 88, 87, 86, 85, 84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73, 72, 71, 70, 144, 143. Bottom row pins: 116, 117, 118, 119.

Figure 3-11. Type 3026 DisplayPort Pinouts Extension Over an SDIO Based Module-side Pinout

In this LGA pattern, the unique pins for DisplayPort are located on the two outer columns of the pads while the center pinouts pattern is the exact same pinouts of Type 2226. This is done so that a land pattern footprint suitable for Type 3026 on the Platform also accommodates the regular Type 2226 as an alternate option (a drop-in replacement). All locations marked as Empty do not contain any ball or pad.

3.2. WWAN/SSD/Other Socket 2 Adapter Interface Signals

The Socket 2 Adapter interface signals are listed in Table 3-15.

Table 3-15. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Description	Voltage
Power Sources and Ground	3.3 V/V$_{BAT}$ (5 pins, Note 5)	I	3.3 V source when regulated by the Host. V$_{BAT}$ when connected directly to Host battery in capable WWAN specific Socket 2 Adapters.	3.3 V
	VIO 1.8 V (1 pin)	I	1.8 V I/O source (low current)	1.8 V (Note 9)
	GND (10 pins)		Return current path.	0 V
Communication-specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	3.3 V 1.8 V (Note 6)
	W_DISABLE1#	I	Active low, debounced signal when applied by the system it will disable radio operation on the Adapters that implement radio frequency applications.	3.3 V 1.8 V (Note 6)
	W_DISABLE2#	I	When implemented, these signals require a pull-up resistor on the card.	1.8 V
	LED_1# (see Note 1)	O	Open drain, active low signal. These signals are used to allow the Adapters to provide status indicators via LED devices that will be provided by the system.	3.3 V
	COEX_RXD COEX_TXD COEX3	I O I/O	Coexistence between WWAN and Wi-Fi+BT on Socket 1. UART_TXD and UART_RXD signals per BT-SIG coexistence protocol + an undefined signal.	1.8 V
Supplemental Communication-specific Signals	FULL_CARD_ POWER_OFF#	I	A single control to turn Off WWAN solution. It is Active Low. This signal is unique and only intended for WWAN specific Socket 2 Adapters working directly off V$_{BAT}$	1.8 V Nominal /3.465 V Max
	RESET#	I	A single control to Reset the WWAN solution. Active Low. This signal is unique and only intended for WWAN specific Socket 2 Adapters working directly off V$_{BAT}$	1.8 V
	GPIO_[0..11] (See Note 2)	I/O	These signals form a block of programmable signals which are used to perform various functions. See Table 26 for specific functions performed.	1.8 V
	ANTCTL[0..3]	I/O	These signals are used for Antenna Control. Two modes of operation are supported: GPIO and RFFE (see Section 3.2.12.5, Antenna Control).	1.8 V Nominal / 2.8 V Max
	IPC_[0..7]	I/O	Pins to facilitate IPC signals exchanged between the host and the card. Functions are BTO/CTO.	1.8 V

Interface	Signal Name	I/O	Description	Voltage
	AUDIO_[0..3]	I/O	Pins for the use of audio. Two modes are supported: I2S and SLIMBus (see Section 3.2.12.3.2).	1.8 V
	WAKE_ON_ WWAN#	O	Used to wake the Platform by the WWAN device.	1.8 V
	DPR	I	This signal is an input directly to the WWAN Adapter from a suitable SAR sensor. The specific implementation will be determined by the Adapter vendor and their customer.	1.8 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Base Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*.	
	PERST#	I	PCIe Reset is a functional reset to the card as defined by the *PCI Express Base Specification*.	3.3 V (Note 3) 1.8 V (Note 4, 6)
	CLKREQ#	I/O	PCIe Clock Request is a reference clock request signal as defined by the *PCI Express Base Specification*. This signal is also used by L1 PM Substates. Open Drain with pull up on Platform. Active Low.	3.3 V (Note 3) 1.8 V (Note 4, 6)
	PEWAKE#/ OBFF	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function-initiated wake event. When the Adapter supports OBFF mechanism, the PEWAKE# signal is used for OBFF signaling.	3.3 V (Note 3) 1.8 V (Note 4, 6)
M-PCIe	MPERp0, MPERn0/ MPETp0, MPETn0	I/O	M-PCIe TX/RX Differential Signals defined by the *PCI Express Base Specification*.	
	MREFCLKp/ MREFCLKn	I	M-PCIe Reference Clock Signals defined by the *PCI Express Base Specification*.	
USB	USB_D+, USB_D-	I/O	USB Data ± Differential defined in the *USB 2.0 Specification*.	
USB3.1 Gen1	USB3.1-Rx+ USB3.1-Rx- USB3.1-Tx+ USB3.1-Tx-	I/O	USB3.1 Gen1 TX/RX Differential signals defined by the *USB3.1 Specification*.	
HSIC	HSIC_DATA, HSIC_STROBE	I/O	HSIC Data and Strobe signals as functionally defined by the *HSIC Electrical Specification*.	1.2 V

Interface	Signal Name	I/O	Description	Voltage
SSIC	SSIC-RxP, SSIC-RxN SSIC-TxP, SSIC-TxN	I/O	SSIC Tx/Rx Differential signals defined in the *SSIC Specification.*	
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to the *Serial ATA Specification.*	
	DEVSLP	I		
	DAS/DSS	I/O		
SSD Specific Signals	Reserved for MFG_DATA/Reserved for MFG_CLOCK		Dedicated Data and Clock pins for SSD Manufacturing. Not to be connected to in the Platform system.	
	ALERT#	O	Alert notification to initiator. Open Drain with pull-up on Platform. Active low.	1.8 V
	SMB_CLK	I/O	SMBus Clock. Open Drain with pull-up on Platform.	1.8 V
	SMB_DATA	I/O	SMBus Data. Open Drain with pull-up on Platform.	1.8 V
User Identity Module (UIM) Signals	SIM_DETECT	I	This is an indication to the modem to detect the SIM insertion/removal. It is usually connected to the SIM reader SW pin and is card type dependent.	1.8 V
	UIM_RESET	O	UIM reset signal. Compliant to the *ISO/IEC 7816-3 specification (RST).*	
	UIM_PWR	O	Power source for the UIM. Compliant to the *ISO/IEC 7816-3 Specification (VCC).*	
	UIM_CLK	O	UIM clock signal. Compliant to the *ISO/IEC 7816-3 Specification (CLK).*	
	UIM_DATA	I/O	UIM data signal. Compliant to the *ISO/IEC 7816-3 specification (I/O).*	
Add-in Card Configuration Pins	CONFIG_0..3	O	These signals provide the means to indicate the specific configuration of the Add-in Card as well as indication of whether an Add-in Card is present or not. The meaning of each of the 16 possible decodes is shown in Table 3-19. These signals should either be grounded or left No Connect to build the decode required for a given Add-in Card type. The host must provide a pull up resistor for each of these signals to either 1.8 V or 3.3 V.	0 V (GND) or NC
Modular Vendor Defined Pins	VENDOR_PORT (A, B, C)	I/O	These signals are Vendor defined. Example definitions are shown in Section 6.10.	

Interface	Signal Name	I/O	Description	Voltage
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.	3.3 V 1.8 V (Note 6, 7)
	PLA_S2#	O	Power Loss Acknowledge. Active low signal with weak pull-down on Platforms that support power loss notification. An Adapter that supports this function must drive the signal to reflect its current power loss processing complete state.	1.8 V (Note 6, 8)
Optional Signals	VIO_CFG	O	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.	0 V/NC

Notes:

1. LED_1# is valid for SSDs as well.
2. GPIO_9 may be defined as LED_1#, IPC_7, or SATA DAS/DSS. Host systems should use the CONFIG pins (see Section 3.2.12.3), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 Adapter prior to discovery of the Adapter type.
3. Key B
4. Key C
5. V_{BAT} applies to Socket 2 Key B and Key C, as an alternative Host power option for WWAN specific Adapters.
6. PCIe-based Key B and Key B-M Adapters when biased from a locally generated 1.8 V voltage on the Adapter. Adapters based on a locally generated 1.8 V must be 3.3 V tolerant for such sideband signaling. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters.
7. PLN# is valid for Socket 2 Key B-M PCIe-based SSD Adapters. Socket 2 Key B WWAN devices use FULL_CARD_POWER_OFF# instead.
8. Socket 2 PLA_S2# functionality differs from Socket 3 and BGA PLA_S3# functionality.
9. Required for PCIe-based Adapters that support 1.8V host interface.

3.2.1.   Power Sources and Grounds

PCI Express M.2 Socket 2 utilizes a single power source (3.3 V generally, or V_{BAT} as an alternative for WWAN specific Socket 2 Adapters) to power main circuitry on the Adapter like that of Socket 1. The voltage source (3.3 V or V_{BAT}) is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In Socket 2, there is provision for five positive voltage pins to enable higher continuous current if required.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving GND pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the GND planes within a card design.

A 1.8 V supply pin called VIO 1.8 V is used to supply the on-Adapter I/O buffer circuitry operating at 1.8 V. Platforms that make use of pinouts that include VIO 1.8 V must bring this source voltage to the relevant pin in the socket connector.

3.2.2.   PCI Express Interface

The PCI Express interface supported in Socket 2 is a two-Lane interface intended for WWAN, SSD, or other devices that need this sort of host interface. See Sections 3.1.2 and 3.1.3 for more information.

3.2.3.   Power up Timing

Figure 3-12 shows an overview of the M.2 power-up sequence for a WWAN specific Adapter powered by a direct V_{BAT} connection. Direct V_{BAT} connections do not apply to other Socket-2 Adapters such as SSDs. See Table 3-6 for the power-up timing variable definitions.

In case of a direct V_{BAT} connection, the de-assertion of FULL_CARD_POWER_OFF# triggers start of the WWAN specific Adapter power-up sequence. It is assumed that V_{BAT} will be within its specified voltage range (see Section 4.6) well before FULL_CARD_POWER_OFF# becomes de-asserted. See Section 3.2.12.1 for details about the FULL_CARD_POWER_OFF# signal.
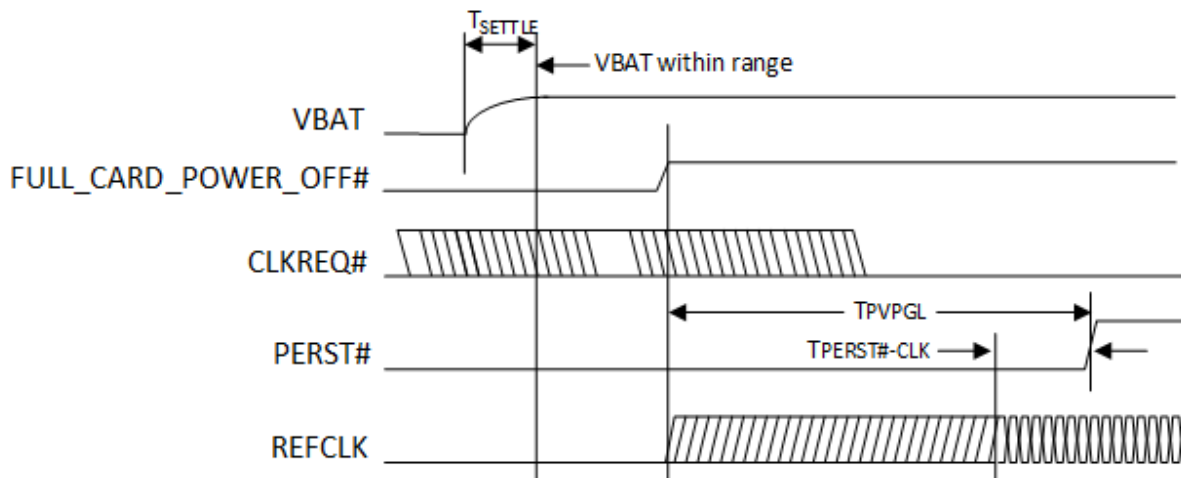
Note: T_{settle} is the time it takes all Power Rails to reach their minimum operating voltage (i.e., from all Power Rails at 0 V to the last Power Rail to reach its minimum valid operating voltage). All other PCI Express related timing events will begin once all of the Power Rails have reached their minimum operating voltage. For example, a typical Adapter with a load capacitance of 330 µF and a 200 mA Soft-Start current limited ramp on the 3.3 V power rail, should settle within 5 ms.

Figure 3-12. Power-up Timing Sequence for a WWAN Specific Adapter Powered by a Direct V_{BAT} Connection

3.2.4.   M-PCIe

M-PCIe combines the protocols of PCI Express with the physical layer based on the MIPI® Alliance M-PHY.

3.2.5.　USB Interface

See Section 3.1.5, *USB Interface,* for a detailed description of the USB signals.

3.2.6.　HSIC Interface

High-Speed Inter-Chip USB (HSIC) is a low power, chip-to-chip interconnect which is 100% host driver compatible with traditional USB cable-connected topologies. HSIC is a 2-signal (HSIC_STROBE, HSIC_DATA) serial interface which only supports the USB High-Speed 480 Mbps data rate.　HSIC may be used through a connectorized interface taking into consideration the electrical limitations identified by the HSIC standard:

❑　Data/strobe trace length (TL) < 10 cm

❑　Data/strobe trace propagation skew (TS) < 15 ps

The current version of the HSIC specification is available at: http://www.usb.org/developers/docs/

3.2.7.　SSCI Interface

SuperSpeed USB Inter-Chip (SSIC) is a chip-to-chip interconnect interface defined as a supplement to the *USB 3.0 Specification*. SSIC augments USB 3.0 in that the physical layer of the interconnect is based on the MIPI® Alliance M-PHY rather than the external cable-capable PHY of traditional SuperSpeed USB. This method better optimizes power, cost, and EMI robustness appropriate for being used for embedded inter-chip interfaces. All higher-layer aspects (software, transaction protocol, etc.) of SSIC follow the *USB 3.0 Specification*.

SSIC – Inter-Chip Supplement to the *USB 3.0 Specification*, Revision 1.0 as of May 3, 2012; available from http://www.usb.org/developers/docs/ and located within the *USB 3.0 Specification* download package.

3.2.8.　USB 3.1 Gen1 Interface

The USB3.1 interface supported on the M.2 connector is USB3.1 Gen1, 5 Gbps (refer to the *USB3.1 Specification*). This specification currently does not support USB3.1 Gen2, 10 Gbps. The *USB3.1 Specification* defines all electrical characteristics, enumeration, protocol, and management features to support USB3.1 Gen1 (SuperSpeed).

The SuperSpeed differential transmit lines (SSTX+, SSTX-) are required to implement the transmit path of a USB3.1 Gen1 SuperSpeed interface. These pins are connected to the transmitter differential pair in the system and to the receiver differential pair on the Adapter.

Likewise, SuperSpeed differential receive lines (SSRX+, SSRX-) are required to implement the receive path of a USB3.1 Gen1 SuperSpeed interface. These pins are connected to the receiver differential pair in the system and to the transmitter differential pair on the Adapter.

3.2.9. SATA Interface (Informative)

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid-state drives as defined by the *Serial ATA International Organization* (refer to the *Serial ATA Specification*).

3.2.9.1. DEVSLP

The Device Sleep (DEVSLP) pin is used to inform a SATA device that it should enter the DEVSLP Interface Power state (refer to the *Serial ATA Specification*).

3.2.9.2. DAS/DSS

The Drive Activity Signal (DAS) is driven by a SATA device to indicate that an access is occurring. Hosts use the same signal for Disable Staggered Spin-up (DSS) and other functions (refer to the Serial ATA Specification).

3.2.10. User Identity Module (UIM) Interface

The UIM interface signals are defined on the system connector to provide the interface between the UIM and an M.2 Adapter (e.g., WWAN, NFC). The UIM contains parameters necessary for the WWAN device's operation in a wireless wide area network radio environment. The UIM signals are described in the following paragraphs for M.2 Adapters that support the off-card UIM interface.

Up to two instances of UIM are permitted on an M.2 Add-in Card.

3.2.10.1. UIM_PWR

Refer to ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements are provided by using any GND pin. Only M.2 Adapters that support a UIM card are permitted to connect to this pin. If the Adapter has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (e.g., voltage) supported as defined in *ISO/IEC 7816-3*. UIM_PWR maps to contact number C1 as defined in *ISO/IEC 7816-2*.

3.2.10.2. UIM_RESET

The UIM_RESET signal provides the UIM card with the reset signal. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_RESET signal. Only M.2 Add-in Cards that support a UIM card are permitted to connect to this pin.

UIM_RESET maps to contact number C2 as defined in *ISO/IEC 7816-2*.

3.2.10.3. UIM_CLK

This signal provides the UIM card with the clock signal. Refer to *ISO/IEC 7816*-3 for more details on the functional and tolerance requirements for the UIM_CLK signal. Only M.2 Adapters that support a UIM card are permitted to connect to this pin.

UIM_CLK maps to contact number C3 as defined in *ISO/IEC 7816-2*.

3.2.10.4. **UIM_DATA**

This signal is used as output (UIM reception mode) or input (UIM transmission mode) for serial data. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_DATA signal. Only M.2 Adapters that support a UIM card are permitted to connect to this pin.

UIM_DATA maps to contact number C7 as defined in *ISO/IEC 7816-2*.

3.2.10.5. **SIM_DETECT**

This signal is used to detect the insertion and removal of a SIM device in the SIM socket. With a Normal Short SIM Card connector, PUSH-PUSH type, the detect switch is normally shorted to GND when no SIM card is inserted. When the SIM is inserted, the SIM_DETECT will transition from a logic 0 to a logic 1 state. The rising edge will indicate insertion of the SIM card. When the SIM is pulled out, the SIM_DETECT will transition from the logic 1 to a logic 0.

This falling edge will indicate the pulling out of the SIM card. The M.2 Adapter monitoring this signal will treat the rising/falling edge or the actual logic state as an interrupt, that when triggered, the Adapter will act accordingly.

This will require a weak pull-up on the Adapter tied to its 1.8 V power rail.

An example of a typical implementation is shown in Figure 3-13.
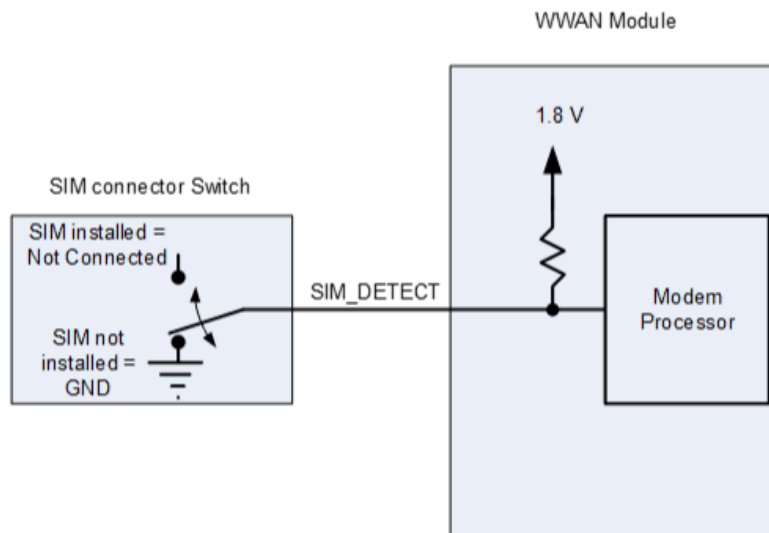
Figure 3-13. Typical SIM Detect Circuit Implementation

3.2.11. **Communication-specific Signals**

3.2.11.1. **Suspend Clock**

See Section 3.1.12.1 for a more detailed description of the SUSCLK signal.

3.2.11.2. **Status Indicators**

See Section 3.1.12.2 for a more detailed description of the LED_1# signal.

3.2.11.3. **W_DISABLE# Signals**

See Section 3.1.12.3 for a more detailed description of the W_DISABLE1# and W_DISABLE2# signals. It should be noted that this W_DISABLE2# of Socket 2 operates at 1.8 V levels.

3.2.11.4. **Coexistence Signals**

See Section 3.1.12.4 for a more detailed description of the COEX_TXD, COEX_RXD, and COEX3 signals.

3.2.12. **Supplemental Communication-specific Signals**

3.2.12.1. **FULL_CARD_POWER_OFF#**

FULL_CARD_POWER_OFF# is an active low input signal that is used to turn off the entire Adapter. If FULL_CARD_POWER_OFF# is de-asserted (i.e., driven high (≥1.19 V)) the Adapter must be enabled. If FULL_CARD_POWER_OFF# is asserted (i.e., driven low (≤0.2 V) or Tri-stated), the Adapter must be shut down.

The FULL_CARD_POWER_OFF# pin must be pulled low on the Adapter with a weak pull-down resistor of >20 kΩ. The Adapter design must ensure that the operation of this pin is asynchronous to any other interface operation.

FULL_CARD_POWER_OFF# must be 3.3 V tolerant but is permitted to be driven by either 1.8 V or 3.3 V GPIO.

3.2.12.2. **RESET#**

Asynchronous RESET# pin, active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. Care should be taken not to activate this pin unless there is a critical failure and all other methods of regaining control and/or communication with the WWAN sub-system have failed.

> **!** **CAUTION**: Triggering the RESET# signal will lead to loss of all data in the modem and the removal of system drivers. It will also disconnect the modem from the network.

3.2.12.3. **General Purpose Input Output Pins**

The GPIO_0 to GPIO_11 pins have configurable assignments. There are four possible functional pinouts configurations. These four configurations are called Port Config_0 to Port Config_3. In each Port Configuration, each GPIO is defined as a specific functional pin. The GPIO pin assignments are listed in Table 3-16.

Table 3-16.   GPIO Pin Function Assignment per Port Configuration

	Pin	Port Config_0 (See Note 1)	Port Config_1 (See Note 2)	Port Config_2 (See Note 3)	Port Config_3 (See Note 4)	Note
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DETECT2	IPC_0	
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DATA2	IPC_1	
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2	
GPIO_3	46	SYSCLK	GNSS_0	UIM_RESET2	IPC_3	
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4	
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0	
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1	
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2	
GPIO_8	28	AUDIO_3	AUDIO_3	PLA_S2#	IPC_6/AUDIO_3	
GPIO_9	10	LED_1#	LED_1#	LED_1#	DAS/DSS/IPC_7	5, 6
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE	
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA	

Notes:
1. GNSS+Audio version 1
2. GNSS+Audio version 2
3. 2nd UIM/SIM Support
4. HSIC Support
5. Platform Providers may choose to implement IPC sideband instead of the LED_1# to optimize their design
6. Some host Platforms (e.g., tablets) may not require support for SSD. In such configurations, Host Platform Providers may choose to implement IPC_7 on GPIO_9 instead of DAS/DSS.

3.2.12.3.1. GNSS Signals

❑ **GNSS_SCL**
Input clock for I2C interface for transfer of location data. External device is bus initiator . For use as a low power interface for location data when host CPU is in low power mode.

❑ **GNSS_SDA**
Bi-directional data interface for I2C. For transfer of location data to/from external device (such as a sensor hub).

❑ **GNSS_IRQ**
Interrupt signal – bi-directional to provide on demand GNSS data to/from external device (such as a sensor hub). Goal is to provide a low power interface for location data when host CPU is in low power mode.

❏ **SYSCLK**

A clock generated by the WWAN Adapter to provide a means to synchronize the internal WWAN sub system on the WWAN Adapter to an external GNSS device that is permitted to reside on the Connectivity Adapter (e.g., Socket 1) or elsewhere on the Platform. Used in conjunction with TX_BLANKING signal. Frequency of operation (and clock type) will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.

❏ **TX_BLANKING**

This signal is active high and will be asserted to indicate when the WWAN sub system is engaged in radio transmission activity which would swamp the GNSS signal being received by an off WWAN Adapter GNSS device. This signal is used in conjunction with SYSCLK signal – specific operation will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.

❏ **GNSS_0-1**

These are pins reserved for proprietary GNSS functions which will be part of BTO on a VENDOR DEFINED basis (see Figure 3-14).
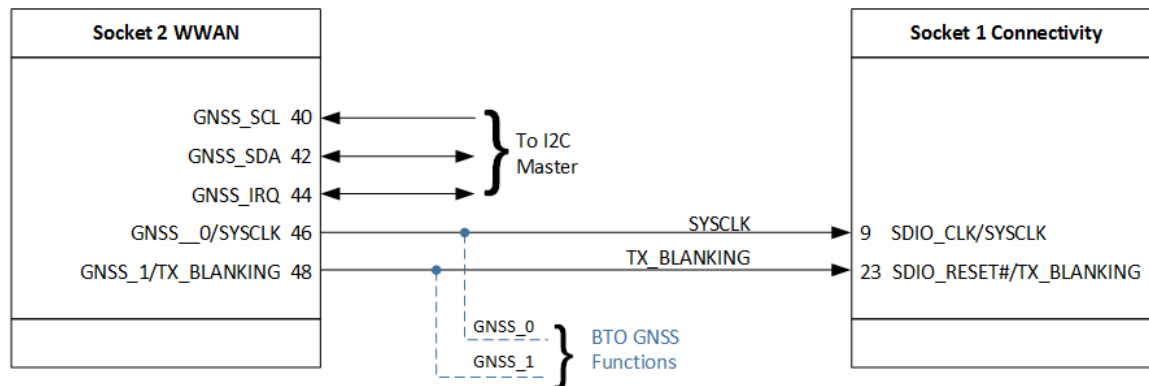
Figure 3-14. Example of a Connection of the GNSS Signals in a Platform Using M.2 Adapter

3.2.12.3.2. Audio Signals

AUDIO_0 to AUDIO_3 pins are reserved for Audio use. Specific implementations will be part of a BTO option determined specifically by the Adapter vendor and their customers. Supported options and functions are listed in Table 3-17.

Table 3-17. Audio Pin Mode and Function Assignment

| M.2 Audio Pins | Pin Mode and Function | | | | | |
| | I2S Mode | | | SLIMBus Mode | | |
Pin Name	Function	Direction	Voltage	Function	Direction	Voltage
AUDIO_0	I2S_CLK	I/O	1.8 V	SLIMBus_CLK	O	1.8 V
AUDIO_1	I2S_RX	I	1.8 V	SLIMBus_DAT	I/O	1.8 V
AUDIO_2	I2S_TX	O	1.8 V	Reserved		
AUDIO_3	I2S_WS	I/O	1.8 V	Reserved		

3.2.12.3.3. Second UIM Signals

UIM Interface is used to support Dual SIM operation and consists of the following signals:

❑ **SIM_DETECT2, UIM_DATA2, UIM_CLK2, UIM_RESET2, UIM_PWR2**
For specific pin definitions see Section 3.2.10.

3.2.12.3.4. RFU

These pins are not assigned as part of this standard but may be allocated in the future as the need arises. These pins cannot be used for any function in this configuration matrix and must be electrically No Connect.

3.2.12.3.5. IPC[0..7] Signals

These pins are used for inter-processor communications between the host and the card. The signals assigned to the pins are BTO/CTO.

3.2.12.3.6. WAKE_ON_WWAN# Signal

The WAKE_ON_WWAN# (WoWWAN#) signal is used to wake up the host. It is open drain and needs to be pulled up at the host side. When the WWAN needs to wake up the host, it will output a 1 s logic low pulse, shown in Figure 3-15.
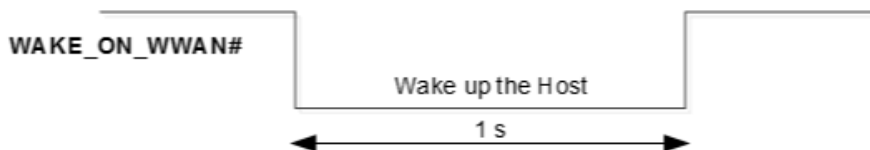
Figure 3-15. WAKE_ON_WWAN# Signal

3.2.12.4. DPR Signal

The optional Dynamic Power Reduction (DPR) signal is used by wireless devices to assist in meeting regulatory Specific Absorption Rate (SAR) requirements for RF exposure. The signal is provided by a

host system proximity sensor to the wireless device to provide an input trigger causing a reduction in the radio transmit output power.

The required value of the power reduction will vary between different host systems and is left to the host Platform OEM and card vendor to determine, along with the specific implementation details. The assertion and de-assertion of DPR is asynchronous to any system clock. All transients resulting from the proximity sensor need to be de-bounced by system circuitry.

3.2.12.5. Antenna Control

ANTCTL0 to ANTCTL3 are provided to allow for the implementation of antenna tuning solutions. The number of antenna control lines required will depend on the application and antenna/band requirements.

The functional definition of the antenna control pins is OEM-specific and should be coordinated between the host Platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host Platform. Supported options are listed in Table 3-18.

Table 3-18. Antenna Control Pin Mode and Function Assignment

| M.2 Antenna Control | Pin Mode and Function | | | | | | Note |
| | GPIO Mode | | | RFFE Mode | | | |
Pin Name	Function	Direction	Voltage	Function	Direction	Voltage	Note
ANTCTL0	GPIO_0 (LSB)	O	1.8 V	Reserved			1
ANTCTL1	GPIO_1	O	1.8 V	RFFE_SDATA	I/O	1.8 V	1
ANTCTL2	GPIO_2	O	1.8 V	RFFE_SCLK	O	1.8 V	1
ANTCTL3	GPIO_3 (MSB)	O	1.8 V	RFFE_VIO	O	1.8 V	1

Note 1: In GPIO Mode operating voltage for pins is 1.8 V Nominal, but is permitted to be up to 2.8 V to allow direct operation of antenna controllers using multiple silicon technologies.

3.2.13. SSD Specific Signals

3.2.13.1. Reserved for MFG CLOCK and DATA

There are two Adapter pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be NC on the Motherboard.

3.2.13.2. SMBus Interface

The SMBus interface supported in SSD Socket 2 is intended as optional side band management interface for SSD applications. SMBus is a three-wire interface (ALERT# signal is optional) through which various system component chips communicate with each other and with rest of the system. It

is based on the principles of operation of I2C. Refer to the *SMBus Specification* for details of the operation.

3.2.13.2.1. ALERT# Signal

The ALERT# signal is intended to indicate to the Platform that the SMBus device requires attention. This GPIO is used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.2.13.2.2. SMB_DATA Signal

The SMB_DATA signal is used to transfer the data packets between the host and the device per the SMBus protocol. The speed supported on this line depends on the host SMB_CLK signal speeds and the device processing capability.

3.2.13.2.3. SMB_CLK Signal

The SMB_CLK signal provides the clock signaling from the SMBus initiator to the SMBus target device to be able to decode the data on the SMB_DATA line.

3.2.14. Configuration Pins

Socket 2 Key B pinout incorporates four configuration pins which assist the Platform to identify the presence of an Add-in Card in the socket and identify card Type, host interface it utilizes, and, in the case of WWAN, Port Configuration for the GPIO_0 to GPIO_11 interface pins.

The operation of this configuration interface is as follows:

❑ Pins CONFIG_0..3

   These pins are grounded or left NC on the Add-in Card per the desired configuration attached to the Host device when plugged into the Socket 2. All configuration pins should be read and decoded by the host Platform to recognize the indicated Add-in Card configuration and host interface supported as listed in Table 3-19.

❑ On the Platform side, each of the CONFIG_0..3 signals need to be fitted with a pull-up resistor. Based on the state of the configuration pins on the Add-in Card, being tied to GND or left No Connect (NC), the sensed pins will create a 4-bit logic state that require decoding.

❑ This configuration scheme ensures that an Add-in Card and its configuration is always detected.

Table 3-19.   Socket 2 Add-in Card Configuration

| State # | Add-in Card Configuration Decodes | | | | Add-in Card Type and Main Host Interface (see Note 1) | Port Configuration (see Note 2) |
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1

State #	Add-in Card Configuration Decodes				Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
4	GND	GND	GND	NC	WWAN-PCIe, USB3.1 Gen1	0 Notes 4,5
5	GND	NC	GND	NC	WWAN-PCIe, USB3.1 Gen1	1 Notes 4,5
6	GND	GND	NC	NC	WWAN-PCIe, USB3.1 Gen1	2 Notes 4,5
7	GND	NC	NC	NC	WWAN-PCIe, USB3.1 Gen1	3 Notes 4,5
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	WWAN-PCIe, USB3.1 Gen1	Vendor-defined Notes 3,5
15	NC	NC	NC	NC	No Add-in Card Present	N/A

Notes:

1. USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
2. Applicable to WWAN only
3. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification*, Revision 1.1 or later, where PCIe and USB3.1 Gen1 are both present on the connector. Vendor defined choice of port configurations 0, 1, 2, 3. See Table 3-19.
4. Used by an Add-in Card where USB3.1 Gen1 is present on the connector and PCIe is No Connect. See Table 3-17. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification*, Revision 1.1 or later where PCIe and USB3.1 Gen1 are both present on the connector. See Table 3-19.
5. Only a single lane of PCIe is available in these configurations.

3.2.15.   Vendor Defined Pins

Socket 2 incorporates 14 Vendor defined pins arranged in the following three pin location groupings in the pinout:

❑ VENDOR_PORT_A (four pins)

❑ VENDOR_PORT_B (six pins)

❑ VENDOR_PORT_C (four pins)

While these ports have been grouped in the pinout to enable potential functional groupings, it should be noted that all these pins are fully vendor defined in a BTO agreement between the customer and vendor. Alternate arrangements with or without groupings are possible to enable any desired functionality using 14 vendor-defined signals.

Typically, these pins are assumed to be GPIO that are at 1.8 V I/O level. However, it is possible to define vendor defined pins as host interface signals that have other associated voltage levels with the desired signals.

Some of the vendor defined pins (specifically the VENDOR_PORT_C pins) have been placed strategically between GND pins to enable optimized differential signal operation with improved isolation from adjacent signals.

The 14 allocated vendor-defined pins provide many potential combinations of features and functions that are implemented using these signals in a BTO mode of operation and agreement between customer and vendor. Some examples are given in Section 6.10.

3.2.16.   Optional Signals

3.2.16.1. VIO_CFG Signal

The VIO_CFG (IO voltage configuration) is a signal that indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. Adapters that use 3.3 V on sideband signals noted in Table 3-19 must connect VIO_CFG directly to GND. Adapters that use 1.8 V sideband signaling (either through a voltage source on the Adapter or using the VIO 1.8 V pin) must not connect the VIO_CFG pin and the affected signals on the Adapter must be 3.3 V tolerant. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters (e.g., prohibit applying power).

> A 3.3 V only sideband signaling Adapter as indicated when VIO_CFG=GND is an indication that a 1.8 V only sideband signaling Platform should not attempt to utilize the Adapter. If an Adapter that supports 1.8 V sideband signaling as indicated by VIO_CFG=NC on the Adapter is in a 3.3 V only Platform (i.e., VIO 1.8 V is not supplied) then the Adapter has the option to either not function or locally generate 1.8 V to configure itself and be 3.3V tolerant.

3.2.17.   Power Loss Signals

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur and indicates the status of an Adapter's preparations for power loss.

3.2.17.1. PLN# Signal

TPLN# (Power Loss Notification) signal is an optional signal that informs an Adapter that a power loss event is expected to occur. If PLN# was asserted then is de-asserted before power is removed, the Adapter is permitted to return to normal operations. A Platform that supports this feature must assert PLN# prior to removing power from the Adapter. See Section 3.2.17.3 for timing information.

Changes to the PCIe link activity due to PLN# assertion, or any functional response to this signal are outside the scope of this specification.

3.2.17.2. PLA_S2# Signal

The PLA_S2# (Power Loss Acknowledge) signal is an optional signal under Port Config_2 that indicates the status of an Adapter's preparations for a power loss. When implemented, Adapters that are powered on must actively drive PLA_S2# regardless of the state of the PLN# signal. When implemented, Adapters always drive PLA_S2# high (de-asserted) when not in power loss processing,

and until drive it low (asserted) whenever power loss processing has completed. Implementations utilizing the optional PLN# signal (see Section 3.2.17.1) should not require the optional PLA_S2# signal to be implemented. See Section 3.2.17.3 for timing information.

Any functional actions in response to this signal are outside the scope of this specification.

> Since power loss preparation takes time (and continued power) some Platform-specific mechanism such as a timer-based delay can be used to control duration of power availability once PLN# is asserted. This shut down delay time may be minimized through the implementation of the PLA_S2# signal.

3.2.17.3. Timing Requirements for Power Loss Signals

Figure 3-16 shows the sequencing behavior for the power loss signals. The minimum response time to a change in the PLN# or in the PLA_S2# signal is 1.0 μs. Any minimum assertion time or minimum negation time is outside the scope of this specification.

Figure 3-16. Power Loss Sequencing Behavior for Socket 2

3.2.18. Socket 2 Connector Pinout Definitions

> All pinouts tables in this section are written from the Adapter point of view when referencing signal directions.

3.2.18.1. Socket 2 Key B Pinout Definitions

The following tables list the signal pinouts for the Adapter edge card connector:

- ❑ Table 3-20. Socket 2 Key B SSIC-based WWAN Adapter Pinout
- ❑ Table 3-21. Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout
- ❑ Table 3-22. Socket 2 Key B PCIe-based WWAN Adapter Pinout
- ❑ Table 3-23. Socket 2 Key B PCIe/USB3.1 Gen1-based WWAN Adapter Pinout
- ❑ Table 3-24. Socket 2 Key B-M SATA-based SSD Adapter Pinout
- ❑ Table 3-25. Socket 2 Key B-M PCIe-based SSD Adapter Pinout

❑ Table 3-26. Socket 2 Key C WWAN Adapter Pinout

All five of these WWAN pinouts also support legacy USB2.0-based WWAN solutions or optionally HSIC. See Table 3-15 for a list of Socket 2 configuration bits on the Add-in Card used to identify the desired pinouts and Port Configuration. The pinouts in Table 3-26 and Table 3-25 utilize a dual Add-in Card key scheme to enable these solutions to also plug into a Socket 3 connector if available in the Platform. The CONFIG_1 pin in these pinouts is equivalent to the PEDET signal used in Socket 3.

Table 3-20.   Socket 2 Key B SSIC-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 8, 9, 10, 11)	75
74	3.3 V/V$_{BAT}$	VIO_CFG (O)	73
72	3.3 V/V$_{BAT}$	GND	71
70	3.3 V/V$_{BAT}$	CONFIG_1 (States 8, 9, 10, 11)	69
68	SUSCLK (I)(0/1.8V/3.3V)	RESET# (I)(0/1.8 V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8 V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8 V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8 V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8 V)	59
58	NC	GND	57
56	NC	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	NC	49
48	GPIO_4 – TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V)	NC	47
46	GPIO_3 – SYSCLK/GNSS_0/UIM_RESET2/IPC_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 – GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	NC	43
42	GPIO_1 – GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V)	NC	41
40	GPIO_0 – GNSS_SCL/GNSS_SCL/SIM_ DETECT2/IPC_0 (I/O)(0/1.8V)	GND	39
38	NC	SSIC-RxP	37
36	UIM_PWR (O)	SSIC-RxN	35
34	UIM_DATA (I/O)	GND	33
32	UIM_CLK (O)	SSIC-TxP	31
30	UIM_RESET (O)	SSIC-TxN	29
28	GPIO_8 – AUDIO_3/AUDIO_3/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 – W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I) (0/1.8V) /HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 – AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11 – WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 – AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 = NC	21
20	GPIO_5 – AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	GPIO_9 – LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8V/3.3 V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V or 3.3V)	GND	5
4	3.3 V/V$_{BAT}$	GND	3
2	3.3 V/V$_{BAT}$	CONFIG_3 = GND	1

Table 3-21.　Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7)	75
74	3.3 V/V$_{BAT}$	VIO_CFG (O)	73
72	3.3 V/V$_{BAT}$		
70	3.3 V/V$_{BAT}$	GND	71
		CONFIG_1 (States 4, 5, 6, 7)	69
68	SUSCLK (I)(0/1.8V/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)		
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
		ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC		
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	GPIO_4 – TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V)	NC	49
46	GPIO_3 – SYSCLK/GNSS_0/UIM_RESET2/IPC_3 (I/O)(0/1.8V)	NC	47
44	GPIO_2 – GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	GND	45
42	GPIO_1 – GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V)	NC	43
40	GPIO_0 – GNSS_SCL/GNSS_SCL/SIM_DETECT2/IPC_0 (I/O)(0/1.8V)	NC	41
38	NC	GND	39
36	UIM_PWR (O)	USB3.1-Rx+	37
34	UIM_DATA (I/O)	USB3.1-Rx-	35
32	UIM_CLK (O)	GND	33
30	UIM_RESET (O)	USB3.1-Tx+	31
		USB3.1-Tx-	29
28	GPIO_8 – AUDIO_3/AUDIO_3/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 – W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I) (0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 – AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11-WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 – AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)		
20	GPIO_5 – AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 = GND	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	GPIO_9 – LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
8	W_DISABLE1# (I)(0/1.8V/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	USB_D+	7
4	3.3 V/V$_{BAT}$	GND	5
2	3.3 V/V$_{BAT}$	GND	3
		CONFIG_3 = NC	1

Table 3-22. Socket 2 Key B PCIe-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
74	3.3 V/V$_{BAT}$	CONFIG_2 (States 2, 3, 12, 13)	75
72	3.3 V/V$_{BAT}$	VIO_CFG (O)	73
70	3.3 V/V$_{BAT}$	GND	71
68	SUSCLK (I)(0/1.8V/3.3V)	CONFIG_1 (States 2, 3, 12, 13)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
		ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V)	GND	51
50	PERST# (I)(0/1.8V/3.3V)	PERp0	49
48	GPIO_4 – TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERn0	47
46	GPIO_3 – SYSCLK/GNSS_0/UIM_RESET2/IPC_3 (I/O)(0/1.8V*)	GND	45
44	GPIO_2 – GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	PETp0	43
42	GPIO_1 – GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETn0	41
40	GPIO_0 – GNSS_SCL/GNSS_SCL/SIM_DETECT2/IPC_0 (I/O)(0/1.8V*)	GND	39
38	NC	PERp1	37
36	UIM_PWR (O)	PERn1	35
34	UIM_DATA (I/O)	GND	33
32	UIM_CLK (O)	PETp1	31
30	UIM_RESET (O)	PETn1	29
28	GPIO_8 – AUDIO_3/AUDIO_3/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 – W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I) (0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 – AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O)(0/1.8V)	GPIO_11 – WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 – AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)		
20	GPIO_5 – AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 (States 2, 3, 12, 13)	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	GPIO_9 – LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
		USB_D-	9
8	W_DISABLE1# (I)(0/1.8V/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	GND	5
4	3.3 V/V$_{BAT}$	GND	3
2	3.3 V/V$_{BAT}$	CONFIG_3 (States 2, 3, 12, 13)	1

Table 3-23. Socket 2 Key B PCIe/USB3.1 Gen1-based WWAN Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7, and 14)	75
74	3.3 V/VBAT	VIO_CFG (O)	73
72	3.3 V/VBAT	GND	71
70	3.3 V/VBAT	CONFIG_1 (States 4, 5, 6, 7, and 14)	69
68	SUSCLK (I)(0/1.8 V /3.3 V)	RESET# (I)(0/1.8 V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8 V)	65
64	COEX_TXD (O)(0/1.8 V)	ANTCTL2 (O)(0/1.8 V)	63
62	COEX_RXD (I)(0/1.8 V)	ANTCTL1 (O)(0/1.8 V)	61
60	COEX3 (I/O)(0/1.8 V)	ANTCTL0 (O)(0/1.8 V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8 V/3.3 V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8 V/3.3 V)	GND	51
50	PERST# (I)(0/1.8 V/3.3 V)	PERp0	49
48	VENDOR DEFINED or GPIO_4 – TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERn0	47
46	VENDOR DEFINED or GPIO_3 – SYSCLK/GNSS_0/UIM_RESET2/IPC_3 (I/O)(0/1.8V*)	GND	45
44	VENDOR DEFINED or GPIO_2 – GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	PETp0	43
42	VENDOR DEFINED or GPIO_1 – GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETn0	41
40	VENDOR DEFINED or GPIO_0 – GNSS_SCL/GNSS_SCL/SIM_DETECT2/IPC_0 (I/O)(0/1.8V*)	GND	39
38	NC	USB3.1-Rx+	37
36	UIM_PWR (O)	USB3.1-Rx-	35
34	UIM_DATA (I/O)	GND	33
32	UIM_CLK (O)	USB3.1-Tx+	31
30	UIM_RESET (O)	USB3.1-Tx-	29
28	VENDOR DEFINED or GPIO_8 – AUDIO_3/AUDIO_3/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	VENDOR DEFINED or GPIO_10 – W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8 V)	25
24	VENDOR DEFINED or GPIO_7 – AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	VENDOR DEFINED or GPIO_11 – WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	VENDOR DEFINED or GPIO_6 – AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 (States 4, 5, 6, 7, and 14)	21
20	VENDOR DEFINED or GPIO_5 – AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	VENDOR DEFINED or GPIO_9 – LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V)/IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8 V /3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	GND	5
4	3.3 V/VBAT	GND	3
2	3.3 V/VBAT	CONFIG_3 (States 4, 5, 6, 7, and 14)	1

Table 3-24.   Socket 2 Key B-M SATA-based SSD Adapter Pinout

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 = GND	75
72	3.3 V	GND	73
70	3.3 V	GND	71
		CONFIG_1 = GND	69
68	SUSCLK (I)(0/3.3V)	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
		ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	SATA-A+	49
48	NC	SATA-A-	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	SATA-B-	43
42	SMB_DATA (I/O)(0/1.8V)	SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (I)	NC	37
36	NC	NC	35
34	NC	GND	33
32	NC	NC	31
30	NC	NC	29
28	NC	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	CONFIG_0 = GND	21
20	NC	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	NC	11
10	DAS/DSS (I/O)	NC	9
8	NC	NC	7
6	NC	NC	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 = GND	1

Table 3-25.   Socket 2 Key B-M PCIe-based SSD Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 = GND	75
74	3.3 V		
72	3.3 V	VIO_CFG (O)	73
70	3.3 V	GND	71
		CONFIG_1 = NC	69
68	SUSCLK (I)(0/1.8V/3.3V)	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
		ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V)	GND	51
50	PERST# (I)(0/1.8V/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	NC	PERp1	37
36	NC	PERn1	35
34	NC	GND	33
32	NC	PETp1	31
30	NC	PETn1	29
28	PLA_S2# (O) (0/1.8V))	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	CONFIG_0 = GND	21
20	NC	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B		
10	LED_1# (O)(OD)	NC	11
8	PLN# (I) (O/1.8V/3.3V)	NC	9
6	NC	NC	7
4	3.3 V	NC	5
2	3.3 V	GND	3
		CONFIG_3 = GND	1

3.2.18.2. Socket 2 Key C Pinout Definitions

Table 3-26.   Socket 2 Key C WWAN Adapter Pinout

Pin	Signal	Signal	Pin
74	3.3 V/V$_{BAT}$	GND	75
72	3.3 V/V$_{BAT}$	GND	73
70	ANTCTL3 (O)/ GPIO_3 (O)/RFFE_VIO (O) (0/1.8V)	RESET# (I) (0/1.8V)	71
68	ANTCTL2 (O)/ GPIO_2 (O)/RFFE_SCLK (O) (0/1.8V)	COEX_TXD (O) (0/1.8V)	69
66	ANTCTL1 (O)/ GPIO_1 (O)/RFFE_SDATA (I/O) (0/1.8V)	COEX_RXD (I) (0/1.8V)	67
64	ANTCTL0 (O)/ GPIO_0 (O) (0/1.8V)	GND	65
62	RESERVED	VENDOR_PORT_C_3	63
60	VENDOR_PORT_B_5	VENDOR_PORT_C_2	61
58	VENDOR_PORT_B_4	GND	59
56	RESERVED	VENDOR_PORT_C_1	57
54	VENDOR_PORT_B_3	VENDOR_PORT_C_0	55
52	VENDOR_PORT_B_2	GND	53
50	VENDOR_PORT_B_1	M/REFCLKP	51
48	VENDOR_PORT_B_0	M/REFCLKN	49
46	PEWAKE# (I/O) (0/1.8V)	GND	47
44	CLKREQ# (I/O) (0/1.8V)	M/PERp0; SSIC-RxP; USB3.1-Rx+	45
42	PERST# (I) (0/1.8V)	M/PERn0; SSIC-RxN; USB3.1-Rx-	43
40	SIM_DETECT2 (I) (0/1.8V)	GND	41
38	UIM2_PWR (O)	M/PETp0; SSIC-TxP; USB3.1-Tx+	39
36	UIM2_DATA (I/O)	M/PETn0; SSIC-TxN; USB3.1-Tx-	37
34	UIM2_CLK (O)	GND	35
32	UIM2_RESET (O)	SIM_DETECT1 (I) (0/1.8V)	33
30	AUDIO1 I2S_WS (I/O) (0/1.8V)	UIM1_PWR (O)	31
28	AUDIO1 I2S_TX (O) (0/1.8V)	UIM1_DATA (I/O)	29
26	AUDIO1 I2S_RX (I) SLIMUS_DAT (I/O) (0/1.8V)	UIM1_CLK (O)	27
24	AUDIO1 I2S_CLK (I/O) SLIMUS_CLK (I/O) (0/1.8V)	UIM1_RESET (O)	25
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
20	VENDOR_PORT_A_3	VIO 1.8 V	15
12	VENDOR_PORT_A_2	FULL_CARD_POWER_OFF# (I) (0/1.8V)	13
10	VENDOR_PORT_A_1	DPR (I) (0/1.8V)	11
8	VENDOR_PORT_A_0	GND	9
6	3.3 V/V$_{BAT}$	USB_D-	7
4	3.3 V/V$_{BAT}$	USB_D+	5
2	3.3 V/V$_{BAT}$	GND	3
		GND	1

3.3. SSD Socket 3 Adapter Interface Signals

Table 3-27 contains a list of the Socket 3 Adapter interface signals.

Table 3-27. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Description	Voltage
Power Sources and Grounds	3.3 V (9 pins)	I	PWR_1 source.	3.3 V
	VIO 1.8 V (1 pin)	I	I/O source (low current)	1.8 V (Note 1)
	GND (15 pins)		Return current path.	0 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Base Specification*.	
	REFCLKp / REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*.	
	PERST#	I	PCIe Reset is a functional reset to the card as defined by the *PCI Express Base Specification*.	3.3 V 1.8 V (Note 2)
	CLKREQ#	I/O	PCIe Clock Request is a reference clock request signal as defined by the *PCI Express Base Specification*, also used by L1 PM Substates. Open Drain with pull up on Platform. Active Low.	3.3 V 1.8 V (Note 2)
	PEWAKE#	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function-initiated wake event. When the Adapter supports OBFF mechanism, the PEWAKE# signal is used for OBFF signaling.	3.3 V 1.8 V (Note 2)
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to the *Serial ATA Specification*.	
	DEVSLP	I		
	DAS/DSS	I/O		

Interface	Signal Name	I/O	Description	Voltage
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	3.3 V 1.8 V (Note 2)
	PEDET	O	Host interface Indication; to be grounded for SATA. No Connect for PCIe.	0 V or NC
	Reserved for MFG_DATA		Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.	
	Reserved for MFG_CLOCK		Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in Platform Socket.	
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3 V
	ALERT#	O	Alert notification to initiator. Open Drain with pull up on Platform. Active Low	1.8 V
	SMB_CLK	I/O	SMBus clock. Open Drain with pull up on Platform	1.8 V
	SMB_DATA	I/O	SMBus data. Open Drain with pull up on Platform	1.8 V
Optional Signals	VIO_CFG	O	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.	0 V/NC
	PWRDIS	I	Active high with weak pull-down on Adapters. Power Disable notifies the Adapter to disable the power on the Adapter.	3.3 V 1.8 V (Note 2)
USB	USB_D+, USB_D-	I/0	USB Data ± Differential serial data interface compliant to the *USB 2.0 Specification*.	

Interface	Signal Name	I/O	Description	Voltage
Power Loss Signals (Note 3)	PLN#	I	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.	3.3 V 1.8 V (Note 2)
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.	3.3 V 1.8 V (Note 2, 4)

Notes:

1. Required for PCIe-based Adapters that support 1.8 V sideband signaling.
2. Must be 3.3 V tolerant for Adapters that support 1.8 V sideband signaling. See Section 3.3.5.1 for more details. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters.
3. Power Loss Signals PLN# and PLA_S3# are valid for Socket 3 Key M PCIe-based SSD Adapters.
4. Note Socket 3 PLA_S3# functionality differs from Socket 2 PLA_S2# functionality. Socket 3 allows a host to tie together the PLA_S3# signal such that the signal remains low until all connected Adapters have indicated completing power loss preparations by releasing PLA_S3# (i.e., wired-or functionality).

3.3.1.   Power Sources and Grounds

PCI Express M.2 Socket 3 utilizes a single 3.3 V power source similar to that of Socket 1 and 2. The voltage source, 3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In Socket 3, there is provision for nine PWR_1 pins to enable high continuous current, the same as in Socket 2 if required. The higher number of pins will help to reduce further the current resistance (IR) drop on the connector.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving GND pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

The VIO 1.8 V power source is provided to supply the Adapter I/O buffer circuitry operating at 1.8 V sideband signaling. This power source is required for Adapters that support 1.8 V sideband signaling. Platforms that support 1.8 V sideband signaling must provide this power source. Adapters may provide 1.8 V sideband signaling based on the detection of this power source.

3.3.2.   PCI Express Interface

The PCI Express interface supported in Socket 3 is a four lane PCI Express interface intended for premium SSD devices that need this sort of host interface. Socket 3 also supports SSD devices that

make use of only two lanes PCI Express and are plugged in to Socket 2 with the aid of a Dual Add-in Card key. See Section 3.1.2 and Section 3.1.3 for more information.

3.3.3. SATA Interface (Informative)

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid-state drives as defined by the Serial ATA International Organization (refer to the *Serial ATA Specification*).

3.3.3.1. DEVSLP

The DEVSLP pin is used to inform a SATA Device that it should enter a DEVSLP Interface Power state (refer to the *Serial ATA Specification*).

3.3.3.2. DAS/DSS

The DAS is driven by the SATA device to indicate that an access is occurring. Hosts are also permitted to use the same signal for DSS and other functions (refer to the *Serial ATA Specification*).

3.3.4. SSD Specific Signals

3.3.4.1. SUSCLK

See Section 3.1.12.1 for a detailed description of the SUSCLK signal.

3.3.4.2. PEDET

The interface detect is used by the host computer to determine the communication protocol that the M.2 Adapter uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a Platform located pull-up resistor.

3.3.4.3. Reserved for MFG Clock and Data

There are two Adapter pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be No Connect on the motherboard.

3.3.4.4. Status Indicators (LED_1#)

See Section 3.1.12.2 for a more detailed description of the LED_1# signal.

3.3.4.5. SMBus Interface

The SMBus interface supported in SSD Socket 3 is intended as optional side band management interface for SSD applications. See Section 3.2.13.2 in this specification for more information.

3.3.5.   Optional Signals

3.3.5.1.   VIO_CFG Signal

The VIO_CFG (IO voltage configuration) is a signal that indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. Adapters that use 3.3 V on sideband signals noted in Table 36 must connect VIO_CFG directly to GND. Adapters that use 1.8 V sideband signaling (either through a voltage source on the Adapter or using the VIO 1.8 V pin) must not connect the VIO_CFG pin and the affected signals on the Adapter must be 3.3 V tolerant. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters (e.g., prohibit applying power).

> A 3.3 V only sideband signaling Adapter as indicated when VIO_CFG=GND is an indication that a 1.8 V only sideband signaling Platform should not attempt to utilize the Adapter. If an Adapter that supports 1.8 V sideband signaling as indicated by VIO_CFG=NC on the Adapter is in a 3.3 V only Platform (i.e., VIO 1.8 V is not supplied) then the Adapter has the option to either not function or locally generate 1.8 V to configure itself and be 3.3 V tolerant.

3.3.5.2.   PWRDIS

The Power Disable (PWRDIS) signal is an optional signal used to disable the power on the M.2 Adapter. When this signal is asserted, the Adapter shall disable the power to the circuits on the Adapter. The PCIe link may not be functional during this time. The host may provide power when PWRDIS is asserted. When this signal is de-asserted the Adapter shall allow power to the circuits on the Adapter.

The Power Disable (PWRDIS) AC characteristics are provided in Table 3-28.

Table 3-28.   PWRDIS AC Characteristic

Parameter	Min	Max	Unit	Note
PWRDIS asserted hold time when Power Disable Supported is 01b	5		s	1, 2
PWRDIS asserted hold time when Power Disable Supported is 10b	0.1		s	1, 2
PWRDIS de-asserted hold time	0.1		s	1

Notes:
1. The hold time is the length of time PWRDIS is asserted or de-asserted. This timing shall include time of 1 us to recognize a change on PWRDIS (de-bounce time).
2. The Power Disable Supported field is defined in the Power Budget Capability register, which is defined in the *Combined Power* ECN.

> **IMPLEMENTATION NOTE: Using PWRDIS to Enter/Exit D3$_{cold}$**
>
> Entering or exiting D3$_{cold}$ (defined in the *PCI Express Base Specification*) is possible by using either power switching hardware on the platform side or by asserting/de-asserting PWRDIS. Using PWRDIS to enter/exit D3$_{cold}$ allows the platform hardware to be simplified by eliminating the need for power switching hardware on the platform.
> - For the use case of recovering an unresponsive device, PWRDIS may be asserted/de-asserted to apply a Fundamental Reset to the device.
> - For the controlled shutdown of a PCIe device, there are both PCIe and device specific protocols to consider. Some devices have device specific protocols defined to prepare for a controlled device entry into D3$_{cold}$, (e.g., as defined in *NVM Express*,) before beginning the PCIe shutdown process.
> - For PCIe, system software should first ensure transition to the L2/L3 Ready state (defined in the *PCI Express Base Specification*) is initiated by platform power management software to begin the process of removing main power and clocks from the device. After the Link transitions to L2/L3 Ready, PWRDIS assertion results in the device transitioning to D3$_{cold}$. Once in the D3$_{cold}$ state, a transition to the D0$_{uninitialized}$ state is possible by de-asserting PWRDIS and asserting Fundamental Reset.

3.3.6.   USB Interface

See Section 3.1.5 for a detailed description of the USB signals.

3.3.7.   Power Loss Signals

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur and indicates the status of an Adapter's preparations for power loss.

3.3.7.1.   PLN# Signal

See Section 3.2.17.1 for a more detailed description of PLN# and Section 3.2.17.3 for timing information.

3.3.7.2.   PLA_S3# Signal

The PLA_S3# (Power Loss Acknowledge) signal is an optional signal that indicates the status of an Adapter's preparations for a power loss. The open-drain requirement on the Adapter allows a host to tie together the PLA_S3# signal from multiple Adapters such that the signal remains low (asserted) until all connected Adapters have completed power loss preparation (i.e., wired-or functionality). Implementations utilizing the optional PLN# signal (see Section 3.2.17.2) should not require the optional PLA_S3# signal to be implemented. See Section 3.3.7.3 for timing information.

Any functional actions in response to this signal are outside the scope of this specification.

> Since power loss preparation takes time (and continued power) some Platform-specific mechanism such as a timer-based delay can be used to control duration of power availability once PLN# is asserted. This shut down delay time may be minimized through the implementation of the PLA_S3# signal.

3.3.7.3.   Timing Requirements for Power Loss Signals

Figure 3-17 shows the sequencing behavior for the power loss signals. The minimum response time to a change in the PLN# or in the PLA_S3# signal is 1.0 μs. Any minimum assertion time or minimum negation time is outside the scope of this specification.
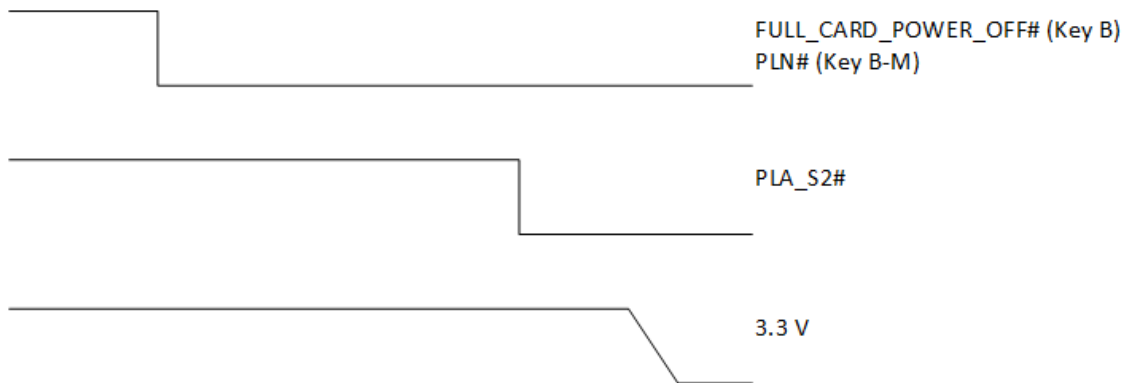

PLN#

PLA_S3#

3.3 V
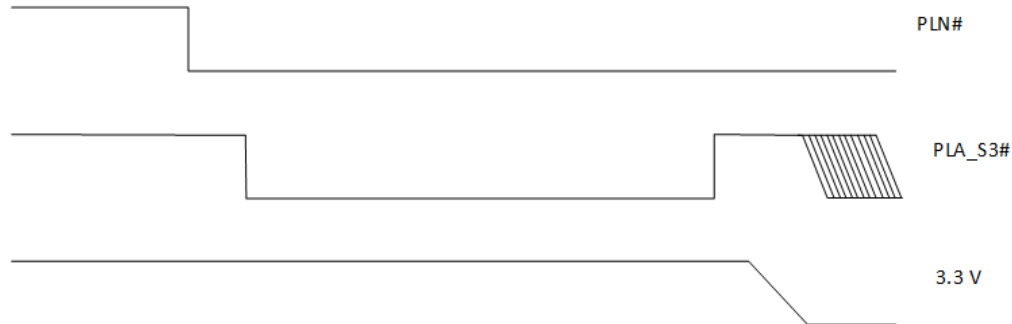
Figure 3-17. Power Loss Sequencing Behavior for Socket 3

3.3.8.   Socket 3 Connector Pinout Definitions

> All pinouts tables in this section are written from the Adapter point of view when referencing signal directions.

Table 3-29 and Table 3-30 list the signal pinouts for the Add-in Card edge card connector. Table 3-29 lists the SATA based solution pinouts. Table 3-30 lists the PCIe Multi-lane-based solution pinouts.

Table 3-29.   Socket 3 SATA-based Adapter Pinouts (Key M)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	PEDET = GND (SATA)	69
68	SUSCLK (I)(0/3.3V)	NC	67
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
		ADD_IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	SATA-A+	49
48	NC	SATA-A-	47
46	NC	GND	45
44	ALERT# (O) (0/1.8V)	SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	SATA-B+	41
40	SMB_CLK (I/O) (0/1.8V)	GND	39
38	DEVSLP (I)	NC	37
36	NC	NC	35
34	NC	GND	33
32	NC	NC	31
30	NC	NC	29
28	NC	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	GND	21
20	NC	NC	19
18	3.3 V	NC	17
16	3.3 V	GND	15
14	3.3 V	NC	13
12	3.3 V	NC	11
10	DAS/DSS (I/O)	GND	9
8	NC	NC	7
6	NC	NC	5
4	3.3 V	GND	3
2	3.3 V	GND	1

Table 3-30. Socket 3 PCIe-based Adapter Pinouts (Key M)

Pin	Signal	Signal	Pin
74	3.3 V	GND	75
72	3.3 V	VIO_CFG (O)	73
70	3.3 V	GND	71
70	3.3 V	PEDET = NC (PCIe)	69
68	SUSCLK (I)(0/1.8V/3.3V)	NC	67
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V)	GND	51
50	PERST# (I)(0/1.8V/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	GND	PERp1	37
36	USB_D-	PERn1	35
34	USB_D+	GND	33
32	GND	PETp1	31
30	PLA_S3# (O)(0/1.8/3.3V)	PETn1	29
28	NC	GND	27
26	NC	PERp2	25
24	NC	PERn2	23
22	VIO 1.8 V	GND	21
20	NC	PETp2	19
18	3.3 V	PETn2	17
16	3.3 V	GND	15
14	3.3 V	PERp3	13
12	3.3 V	PERn3	11
10	LED_1# (O)(OD)	GND	9
8	PLN# (I)(0/1.8/3.3V)	PETp3	7
6	PWRDIS (I)(0/1.8/3.3V)	PETn3	5
4	3.3 V	GND	3
2	3.3 V	GND	1

3.4.　　BGA SSD Interface Signals

Table 3-31 and Table 3-32 contain a list of the system interface signals defined for BGA SSD Types 1620, 2024, 2228 and 2828. The I/O direction indicated is from BGA Module's perspective. Table 3-32 contains a list of BGA SSD system interface signals for the Type 1113.

Table 3-31.　BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, and 2828

Interface	Signal Name	I/O	Description	Voltage
Power Sources and Grounds	PWR_1[1] (8 pins)	I	+3.3 V or +2.5 V supply	
	PWR_2[1] (12 pins)	I	+1.8 V or +1.2 V supply	
	PWR_3[1] (12 pins)	I	+1.2 V, +1.1 V, +1.0 V, +0.9 V, +0.8 V, or +0.75 V supply	
	GND (106 pins)		Return current path	
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Base Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*.	
	PERST#	I	PCIe Reset is a functional reset to the card as defined by the *PCI Express Base Specification*.	1.8 V
	CLKREQ#	I/O	PCIe Clock Request is a reference clock request signal as defined by the *PCI Express Base Specification*. It is also used by L1 PM Substates. Open Drain. Active Low.	1.8 V
	PEWAKE#	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Module supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function-initiated wake event. When the Module supports OBFF mechanism, the PEWAKE# signal is used by the system for OBFF signaling.	1.8 V

Interface	Signal Name	I/O	Description	Voltage
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to *Serial ATA Specification*.	
	DEVSLP	I		
	DAS/DSS	I/O		
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the Platform chipset to reduce power and cost for the Module. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	PEDET	O	Host interface Indication; to be grounded for SATA. No Connect for PCIe.	0 V or NC
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Module to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	
	XTAL_OUT	O	Connection to crystal unit.	
	CAL_P	N/A	PHY calibration resistor.	
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	
	JTAG_TRST#	I	Refer to *JTAG Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TDO	O		
	SMB_CLK	I/O	SMBus Clock. Open Drain with pull up on Platform.	1.8 V
	SMB_DATA	I/O	SMBus Data. Open Drain with pull up on Platform.	1.8 V
	ALERT#	O	Alert notification to initiator. Open Drain with pull up on Platform. Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	

Interface	Signal Name	I/O	Description	Voltage
	PWR_ID[0:4]	O	Voltage requirement indication to Platform. The Platform uses the combination of these 5 signals to determine the BGA module voltage requirements for each of the PWR_1, PWR_2, and PWR_3 power supplies. If any of these signals are implemented then all PWR_ID signals must be implemented.	0 V or NC
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.	PWR_2
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.	PWR_2

1 The voltage sources are given symbolic names to allow a choice of voltages for the power rails. In earlier revisions of this specification the voltage sources for Types 1620, 2024, 2228, and 2828 were defined as fixed values. Henceforth, the voltage sources are given symbolic names, allowing a choice of voltages for each of the mandatory power rails.

Table 3-32. BGA SSD System Interface Signal Table for Type 1113

Interface	Signal Name	I/O	Description	Voltage
Power Sources and Grounds	PWR_1 (10 pins)	I	+3.3 V or +2.5 V supply	
	PWR_2 (20 pins)	I	+1.8 V or +1.2 V supply	
	PWR_3 (10 pins)	I	+1.2 V, +1.1 V, +1.0 V, +0.9 V, +0.8 V, or +0.75 V supply	
	GND (75 pins)		Return current path	
	NCTF (40 pins)		Non-Critical To Function pins. Redundant ground that shall be electrically connected to the common host and device ground plane allowing for mechanical failure but not functional failure.	
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Base Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Base Specification*.	
	PERST#	I	PCIe Reset is a functional reset to the card as defined by the *PCI Express Base Specification*.	1.8 V

Interface	Signal Name	I/O	Description	Voltage
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Base Specification*. Also used by L1 PM Substates.	1.8 V
	PEWAKE#	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Module supports wakeup, this signal is used to request the system return from a sleep/suspend state to service a function-initiated wake event. When the Module supports OBFF mechanism, the PEWAKE# signal is used for OBFF signaling.	1.8 V
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the Platform chipset to reduce power and cost for the Module. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm.	1.8 V
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Module to provide status indication via LED device that will be provided by the system.	3.3 V
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
	HSB		Host-specific balls	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	
	XTAL_OUT	O	Connection to crystal unit.	
	CAL_P	N/A	PHY calibration resistor.	
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	
	JTAG_TRST#	I	Refer to *JTAG Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TDO	O		
	SMB_CLK	I/O	SMBus Clock. Open Drain with pull up on Platform.	1.8 V
	SMB_DATA	I/O	SMBus Data. Open Drain with pull up on Platform.	1.8 V
	ALERT#	O	Alert notification to initiator. Open Drain with pull up on Platform. Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	

Interface	Signal Name	I/O	Description	Voltage
	WP#	I	Write protect signal to prevent writes from occurring to SPI NOR. Active low.	1.8 V
	SPI_CLK	I	SPI clock. Max frequency is 50 MHz.	1.8 V
	SPI_MOSI	I	Initiator Out Target In signal for SPI NOR.	1.8 V
	SPI_MISO	O	Initiator In Target Out signal for SPI NOR	1.8 V
	SPI_CS#	I	Chip select for SPI NOR. Active low.	1.8 V
	SPI_18	I	+1.8 V supply. Optional voltage supply if SPI NOR included in package.	1.8 V
	REG_01	N/A	Connection to internal power rail. Value and usage are vendor specific.	N/A
	REG_02	N/A	Connection to internal power rail. Value and usage are vendor specific.	N/A
	REG_03	N/A	Connection to internal power rail. Value and usage are vendor specific.	N/A
	V_ID[0:4]	O	Voltage requirement indication to Platform. The Platform uses the combination of these 5 signals to determine the 1113 BGA module voltage requirements for each of the PWR_1, PWR_2, and PWR_3 power supplies. If any of these signals are implemented then all V_ID signals must be implemented.	0 V/NC
Power Loss Signals	PLN#	I	Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.	PWR_2
	PLA_S3#	O	Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.	PWR_2

3.4.1. Power Sources and Grounds

In the BGA SSD, the PWR_1, PWR_2, PWR_3, and GND balls must tolerate a continuous load of up to 200 mA.

For Type 1113 only, the optional balls REG_01, REG_02, and REG_03 are for devices that require external components for voltage regulation inside the device. Values and components are defined by the device vendor.

> **Note:** While the maximum current that is possible to be passed to the BGA is calculated by multiplying the number of power pins by 200 mA, actual power system requirements will be determined between the Platform and BGA SSD vendors.

3.4.2. PCI Express Interface

The PCI Express interface supported in BGA SSD is a two-Lane interface for Type 1113 and a four Lane interface for the other BGA module types. See Section 3.3.2 for a detailed description of the PCIe signals.

3.4.2.1. PCI Express Auxiliary Signals

Definitions for PERST#, CLKREQ#, and PEWAKE# signals are the same as that in Section 3.1.3, except that these signals are defined to be at signal levels of 1.8 V.

3.4.3. SATA Interface (Informative)

See Section 3.3.3 for a detailed description of the SATA signals.

3.4.4. SSD Specific Signals

3.4.4.1. SUSCLK

Definition for this signal is the same as that in Section 3.1.12.1, except that this signal is defined to be at signal levels of 1.8 V.

3.4.4.2. PEDET

The interface detect is used by the host computer to determine the communication protocol that the M.2 Adapter uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a Platform located pull-up resistor.

> This signal is not applicable to Type 1113, which supports only the PCIe interface.

3.4.4.3. Status Indicator (LED_1#)

See Section 3.1.12.2 for a detailed description of the LED_1# signal.

3.4.4.4. RFU

Signals documented as RFU are reserved for future use. These balls must be soldered to a Platform but must be electrically No Connect on the Host and the Module. These balls are reserved for future assignment as a functional signal.

3.4.4.5. DNU

Signals documented as Do Not Use (DNU) are for manufacturing only. These balls must be soldered to a Platform but must be electrically No Connect on the Host. Signals documented as DNU are for manufacturing only.

3.4.4.6. HSB (Host-Specific Balls)

Signals documented as HSB are not defined as a functional signal. These balls must be soldered to a platform but must be electrically No Connect on the Module. A host's use of this signal is undefined.

3.4.4.7. Non-Critical To Function (NCTF)

Signals documented as NCTF are redundant ground balls. They are connected to host ground and redundant to other device grounds, so the loss of the solder joint continuity due to mechanical failure at end of life conditions will not affect the overall product functionality.

3.4.5. SSD Specific Optional Signals

Note: Physical balls need to be present on the package for these signals even if they are not being implemented.

3.4.5.1. CAL_P

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the Platforms. It is used as impedance reference for controller calibration.

3.4.5.2. RZQ_1 and RZQ_2

These signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the Platforms. These signals are used as impedance reference for calibrating DRAM or NAND memory interface.

3.4.5.3. XTAL_OUT

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the Platforms. It connects to optional crystal output from BGA SSD Module. Crystal unit characteristics are vendor specific.

3.4.5.4. XTAL_IN

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the Platforms. It connects to optional crystal output from the Platform. Crystal unit characteristics are vendor specific.

3.4.5.5. JTAG Signals

This group of signals is optional. It is not required to be connected on the SSD BGA component and is not required to be implemented on the Platforms. IEEE Standard 1149.1 specifies the rules and permissions for designing an 1149.1-compliant interface. Inclusion of a *Test Access Port* (TAP) on an Module allows boundary scan to be used for testing of the Module on which it is installed. The TAP is comprised of five signals (the JTAG_TRST# signal is optional within the set of JTAG signals) that are used to interface serially with a TAP controller within the BGA based SSD device. The Module vendor must specify TDO drive strength.

3.4.5.6. SMBus Pins

ALERT#, SMB_DATA and SMB_CLK signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the Platforms.

3.4.5.6.1. ALERT#

For a description of this signal, see Section 3.2.13.2.1.

3.4.5.6.2. SMB_DATA

For a description of this signal, see Section 3.2.13.2.2.

3.4.5.6.3. SMB_CLK

For a description of this signal, see Section 3.2.13.2.3.

3.4.5.7. DIAG0, DIAG1

The DIAG0 and DIAG1 signals are optional for engineering or production implementation, are not required to be present on the SSD BGA component and are not required to be implemented on the Platforms.

3.4.5.8. Serial Peripheral Interface (SPI) Pins

The WP#, SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS#, and SPI_18 signals are optional and define an interface for an optional SPI storage device in the Module. These signals are defined only for the Type 1113. The implementation and details of SPI is dependent on the vendor.

3.4.5.9. PWR_ID[0:4]

The PWR_ID[0:4] signals are optional signals. When supported by the BGA module, the combination of the five signals together are used to inform the Platform which voltage level is required on each of the PWR_1, PWR_2, and PWR_3 power supplies (see Table 3-33).

> Platforms that support BGA voltage indication must support a mechanism for sensing the state of all PWR_ID[0:4] pins before or in conjunction with enabling the voltage rail that supplies each of the PWR_1, PWR_2, and PWR_3 power supply domains to ensure the BGA module is not damaged (e.g., direct Platform voltage regulation subsystem connection to influence output levels, pin state decoding using pull-ups and logic located on the Platform, or alternative Platform implementation approach).

Table 3-33. PWR_ID[0:4] Signal Definitions

Voltage Indication Signal Configuration					Voltage		
PWR_ID0	PWR_ID1	PWR_ID2	PWR_ID3	PWR_ID4	PWR_1	PWR_2	PWR_3
NC	NC	NC	NC	NC	RFU	RFU	RFU
GND	NC	NC	NC	NC	2.5 V	1.2 V	0.9 V
NC	GND	NC	NC	NC	2.5 V	1.2 V	1.1 V
GND	GND	NC	NC	NC	2.5 V	1.2 V	RFU
NC	NC	GND	NC	NC	2.5 V	1.2 V	1.2 V
GND	NC	GND	NC	NC	2.5 V	1.2 V	1.0 V
NC	GND	GND	NC	NC	2.5 V	1.2 V	0.8 V
GND	GND	GND	NC	NC	2.5 V	1.2 V	0.75 V
NC	NC	NC	GND	NC	RFU	RFU	RFU
GND	NC	NC	GND	NC	2.5 V	1.8 V	0.9 V
NC	GND	NC	GND	NC	2.5 V	1.8 V	1.1 V
GND	GND	NC	GND	NC	2.5 V	1.8 V	RFU
NC	NC	GND	GND	NC	2.5 V	1.8 V	1.2 V
GND	NC	GND	GND	NC	2.5 V	1.8 V	1.0 V
NC	GND	GND	GND	NC	2.5 V	1.8 V	0.8 V
GND	GND	GND	GND	NC	2.5 V	1.8 V	0.75 V
NC	NC	NC	NC	GND	RFU	RFU	RFU
GND	NC	NC	NC	GND	3.3 V	1.2 V	0.9 V
NC	GND	NC	NC	GND	3.3 V	1.2 V	1.1 V
GND	GND	NC	NC	GND	3.3 V	1.2 V	RFU
NC	NC	GND	NC	GND	3.3 V	1.2 V	1.2 V
GND	NC	GND	NC	GND	3.3 V	1.2 V	1.0 V
NC	GND	GND	NC	GND	3.3 V	1.2 V	0.8 V
GND	GND	GND	NC	GND	RFU	RFU	RFU
NC	NC	NC	GND	GND	RFU	RFU	RFU
GND	NC	NC	GND	GND	3.3 V	1.8 V	0.9 V
NC	GND	NC	GND	GND	3.3 V	1.8 V	1.1 V
GND	GND	NC	GND	GND	3.3 V	1.8 V	RFU
NC	NC	GND	GND	GND	3.3 V	1.8 V	1.2 V
GND	NC	GND	GND	GND	3.3 V	1.8 V	1.0 V
NC	GND	GND	GND	GND	3.3 V	1.8 V	0.8 V
GND	GND	GND	GND	GND	RFU	RFU	RFU

3.4.5.10.   **V_ID[0:4]**

The V_ID[0:4] signals are optional signals. When supported by the BGA module, the combination of the five signals together are used to inform the Platform which voltage level is required on each of the PWR_1, PWR_2, and PWR_3 power supplies (see Table 3-34).

> Platforms that support BGA voltage indication must support a mechanism for sensing the state of all V_ID[0:4] pins before or in conjunction with enabling the voltage rail that supplies each of the PWR_1, PWR_2, and PWR_3 power supply domains to ensure the BGA module is not damaged (e.g., direct Platform voltage regulation subsystem connection to influence output levels, pin state decoding using pull-ups and logic located on the Platform, or alternative Platform implementation approach). The decode for the V_ID[0..4] is different than the PWR_ID[0..4] decode used in Section 3.4.5.9

Table 3-34.   V_ID[0..4] Signal Definitions

Voltage Indication Signal Configuration					Voltage		
V_ID0	V_ID1	V_ID2	V_ID3	V_ID4	PWR_1	PWR_2	PWR_3
NC	NC	NC	NC	NC	2.5 V	1.2 V	RFU
GND	NC	NC	NC	NC	2.5 V	1.2 V	0.75 V
NC	GND	NC	NC	NC	2.5 V	1.2 V	0.8 V
GND	GND	NC	NC	NC	2.5 V	1.2 V	0.9 V
NC	NC	GND	NC	NC	2.5 V	1.2 V	1.0 V
GND	NC	GND	NC	NC	2.5 V	1.2 V	RFU
NC	GND	GND	NC	NC	2.5 V	1.2 V	1.1 V
GND	GND	GND	NC	NC	2.5 V	1.2 V	1.2 V
NC	NC	NC	GND	NC	2.5 V	1.8 V	RFU
GND	NC	NC	GND	NC	2.5 V	1.8 V	0.75 V
NC	GND	NC	GND	NC	2.5 V	1.8 V	0.8 V
GND	GND	NC	GND	NC	2.5 V	1.8 V	0.9 V
NC	NC	GND	GND	NC	2.5 V	1.8 V	1.0 V
GND	NC	GND	GND	NC	2.5 V	1.8 V	RFU
NC	GND	GND	GND	NC	2.5 V	1.8 V	1.1 V
GND	GND	GND	GND	NC	2.5 V	1.8 V	1.2 V
NC	NC	NC	NC	GND	3.3 V	1.2 V	RFU
GND	NC	NC	NC	GND	3.3 V	1.2 V	RFU
NC	GND	NC	NC	GND	3.3 V	1.2 V	0.8 V
GND	GND	NC	NC	GND	3.3 V	1.2 V	0.9 V
NC	NC	GND	NC	GND	3.3 V	1.2 V	1.0 V

Voltage Indication Signal Configuration					Voltage		
V_ID0	V_ID1	V_ID2	V_ID3	V_ID4	PWR_1	PWR_2	PWR_3
GND	NC	GND	NC	GND	3.3 V	1.2 V	RFU
NC	GND	GND	NC	GND	3.3 V	1.2 V	1.1 V
GND	GND	GND	NC	GND	3.3 V	1.2 V	1.2 V
NC	NC	NC	GND	GND	3.3 V	1.8 V	RFU
GND	NC	NC	GND	GND	3.3 V	1.8 V	RFU
NC	GND	NC	GND	GND	3.3 V	1.8 V	0.8 V
GND	GND	NC	GND	GND	3.3 V	1.8 V	0.9 V
NC	NC	GND	GND	GND	3.3 V	1.8 V	1.0 V
GND	NC	GND	GND	GND	3.3 V	1.8 V	RFU
NC	GND	GND	GND	GND	3.3 V	1.8 V	1.1 V
GND	GND	GND	GND	GND	3.3 V	1.8 V	1.2 V

3.4.6.   Power Loss Signals

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur and indicates the status of an Adapter's preparations for power loss.

3.4.6.1.   PLN# Signal

See Section 3.2.16 for a more detailed description of PLN# and Section 3.3.7.3 for timing information.

3.4.6.2.   PLA_S3# Signal

See Section 3.3.7.2 for a more detailed description of PLA_S3#.

3.4.7.   BGA SSD Soldered-Down Module Pin-out

All pinout tables in this section are written from the Module point of view when referencing signal directions. This section contains the Module-side pinout map for Type 1620 BGA Module.

Figure 3-18 shows Module-side ballmap for Type 1620 BGA. Figure 3-19 shows Type 1620 BGA Module-side ballmap surrounded by Type 2024, Type 2228, and Type 2828 module-side ballmaps (Top View).

Ballmaps for Types 2024, 2228, and 2828 have additional DNU balls for mechanical stability. See Section 2.3.6 for details on the location of these DNU balls for various BGA package sizes.

Figure 3-20 shows the Type 1113 BGA ballmap.

Optional signals are shown in blue. The optional signals are CAL_P, XTAL_OUT, XTAL_IN, RZQ_1, RZQ_2, DIAG0, DIAG1, JTAG_TRST#, JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, SMB_CLK, SMB_DATA, ALERT#, WP#, SPI_CLK, SPI_MOSI, SPI_MISO, SPI_CS#, SPI_18, REG_01, REG_02, and REG_03.

The optional signals are handled as follows for the host and Module.

❑ Host:
- If not implemented, the landing pads must not be electrically connected to the host.
- If implemented, the host routes the signals as described in this specification.

❑ Module
- If not implemented, the balls must not be electrically connected to the Module.
- If implemented, the module routes the signals as described in this specification.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	PWR_ID4	PWR_ID3	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	PWR_1	PWR_1	GND	DNU	DIAG1	SUSCLK	PWR_ID0			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	PWR_1	PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A-/ PERn0	GND							PEDET	PWR_ID1				
G	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+/ PETp0	SATA-B-/ PETn0		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3	PWR_ID2	PLN#				
J	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND	RFU		PLA_S3#			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU	RFU	RFU				
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND	RFU	RFU				
R	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2	RFU	RFU				
U	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PERp3	PETn3								RFU	RFU				
W	GND	GND	GND	GND	GND	GND	LED_1#/ DAS	RFU	PWR_1	PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	PWR_1	PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

☐ = No Solder Ball

Figure 3-18. Type 1620 BGA Module-side Ballmap (Top View)

Figure 3-19. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP#	SPI_CLK	SPI_CS#	GND	GND
C	GND	GND	GND	DNU	DNU	V_ID0	V_ID2	V_ID4	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	V_ID1	V_ID3	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PETp0	PETn0	GND	PERp0	PERn0	GND	PETp1	PETn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	PERp1	PERn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND	PETp1	PETn1	GND	GND	GND+D11: W25

☐ = No Solder Ball

Figure 3-20. Type 1113 BGA Module-side Ballmap (Top View)

3.5. Add-in Card IL Target for 16 GT/s

Insertion loss on the top of the edge finger to the Silicon pad for both Receiver and Transmitter interconnect must not exceed 6.5 dB at 8 GHz for SSDs. Other applications are not required to follow this Insertion loss limit but need to make sure that the total Insertion loss at 8 GHz does not exceed 8 dB. This loss includes PCB routing, vias, AC coupling caps, and Silicon package.

3.6. Add-in Card IL Target for 32 GT/s

The insertion loss from the top of the edge finger to the silicon die pad must not exceed -7.5 dB at 16 GHz. This requirement applies to both the transmitter and receiver interconnect. The total loss includes PCB insertion loss, vias (if any), AC Caps (applicable to transmitter interconnect), and silicon package including the effective die capacitance.

4. Electrical Requirements

> **!** **CAUTION**: M.2 Add-in Cards are not designed or intended to support Hot-Swap or Hot-Plug connections. Performing Hot-Swap or Hot-Plug poses danger to the M.2 Add-in Card, to the system Platform, and to the person performing this act.

4.1. 3.3 V Logic Signal Requirements

The 3.3 V card logic levels for single-ended digital signals (PEWAKE#, CLKREQ#, PERST#, SUSCLK, W_DISABLE#, UART_WAKE#, DP_MLDIR, LED#, PWRDIS) are given in Table 4-1. When used in the BGA SSD applications, the logic levels for PEWAKE#, CLKREQ#, PERST#, ALERT#, and SUSCLK are those shown in Table 4-1.

Table 4-1.   DC Specification for 3.3 V Logic Signaling

Parameter	Description	Condition	Min	Max	Unit	Notes
3.3 V	Supply Voltage		3.135	3.465	V	6
V_{IH}	Input High Voltage		2.0	3.6	V	5
V_{IL}	Input Low Voltage		-0.5	0.8	V	5
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	1
$I_{OL\text{-}LED}$	Output Low Current for LED open-drain signals	0.4 V	9		mA	2
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	µA	5
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	µA	5
C_{IN}	Input Pin Capacitance			20	pF	4, 5
C_{OUT}	Output Pin Capacitance			30	pF	4
$R_{PULL\text{-}UP}$	Pull-up Resistance		9	60	kΩ	3

Notes:
1. Not applicable to LED# and DAS/DSS pins.
2. Applies to the LED# pins.
3. Applies to CLKREQ# and PEWAKE# pull-up on host system.
4. As measured at the Add-in Card edge finger, or at the BGA or LGA solder-down component.
5. Applies to PERST#, W_DISABLE1#, W_DISABLE2#, DP_MLDIR (when applicable) and PEWAKE# (when used for OBFF signaling).
6. The 3.3 V regulated power rail can be replaced with a direct V_{BAT} connection for Socket 2 WWAN-specific Adapters only. This type of power connection is optional. See Table 4-7 in Section 4.4 for V_{BAT} voltage conditions.

4.2. 1.8 V Logic Signal Requirements

The 1.8 V Adapter logic levels for single-ended digital signals (PEWAKE#, CLKREQ#, PERST#, SDIO, UART, I2C, PCM/I2S, SMBus, SPI, PWRDIS, PLN#, PLA_S2#, PLA_S3#, etc.) are given in Table 4-2. This table also defines the signaling levels for BGA SSD defined single-ended signals PERST#, CLKREQ#, PEWAKE#, SUSCLK, SMBus, ALERT#, PLN#, and PLA_S3#.

Table 4-2. DC Specification for 1.8 V Logic Signaling

Parameter	Description	Condition	Min	Max	Unit	Notes
V_{DD18}	Supply Voltage		1.7	1.9	V	
V_{IH}	Input High Voltage		$0.7*V_{DD18}$	$V_{DD18}+0.3$	V	
V_{IL}	Input Low Voltage		-0.3	$0.3*V_{DD18}$	V	
V_{OH}	Output High Voltage	I_{OH} = -1mA V_{DD18} Min	$V_{DD18}-0.45$		V	
V_{OL}	Output Low Voltage	I_{OL} = 1mA V_{DD18} Min		0.45	V	1
I_{IN}	Input Leakage Current	0 V to V_{DD18}	-10	+10	µA	
I_{LKG}	Output Leakage Current	0 V to V_{DD18}	-50	+50	µA	
C_{IN}	Input Pin Capacitance			20	pF	3, 4
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	2

Notes:
1. The listed IOL may not meet some SMBus designs and an isolation buffer may be required. Refer to the SMBus Specification for timing and loading details.
2. Applies to CLKREQ# pull-up and PEWAKE# pull-up on host system.
3. As measured at the Add-in Card edge-finger, or at the BGA or LGA soldered-down component pad.
4. Applies to PERST#, and PEWAKE# (when used for OBFF signaling).

4.3. Electrical Requirements for M.2 Adapters

4.3.1. Voltage Supply Power-on Sequencing

It is recommended that the host should apply the following power rail sequencing for Platforms that implement the VIO 1.8 V supply. During power-on:

❑ After the voltage on either the 3.3 V supply or the voltage on the VIO 1.8 V supply reach 300 mV, the voltage on the 3.3 V supply should remain greater than the VIO 1.8 V by at least 200 mV.

❑ If the power-on sequencing is not followed, there is a risk that the Adapter may not power-on correctly or the Adapter may be damaged. These results are vendor specific.

4.3.2. Voltage Supply Power-off Sequencing

It is recommended that the host should apply the following power rail sequencing for Platforms that implement the VIO 1.8 V supply. During power-off:

❑ The PWR_2 and PWR_3 voltage selections requested by the BGA SSD may not support a 200 mV voltage differential at the tolerance extremes, e.g., for PWR_2 = 1.14 V (1.2 V) and PWR_1 = 0.98 V (0.9 V), the minimum voltage difference may only be 160 mV.

BGA SSDs designed for such voltage selections are responsible for supporting a smaller difference of the possible voltages considering voltage tolerances.

Systems that support such voltage selections are recommended to keep the voltage difference as large as practical.

❑ After the voltage on both the 3.3 V supply and the VIO 1.8 V supply are below 300 mV, there is no specified relationship between them.

❑ The voltage on all supplies should remain below 100 mV for at least 1 ms before the power-on sequence is attempted.

If the power-off sequencing is not followed, there is a risk that the Adapter may not power-off correctly or the Adapter may be damaged. These results are vendor specific.

4.4. Electrical Requirements for BGA SSDs

4.4.1. BGA SSD Voltage Supply Power-on Sequencing

The host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, the PWR_2 supply, and the PWR_3 supply during power-on:

❑ After the voltage on the PWR_2 supply or the voltage on the PWR_3 supply reach 300 mV, the voltage on the PWR_2 supply should remain greater than the voltage on the PWR_3 supply by at least 200 mV.

❑ The voltage on the PWR_1 supply has no timing relationship relative to the voltage on the PWR_3 supply or the voltage on the PWR_2 supply.

If the power-on sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 4-1 shows three power-on ramp examples that follow the recommendations of this section for the case where each of the power rails is assigned a different voltage. The first example shows PWR_2 reaching 300 mV before PWR_3 reaches 100 mV. The second example shows PWR_2 well above 300 mV by the time PWR_3 reaches 100 mV. The third case shows PWR_2 reaching 300 mV at the same time as PWR_3. Note that the PWR_1 rail is not shown since it has no timing relationship to the other rails.
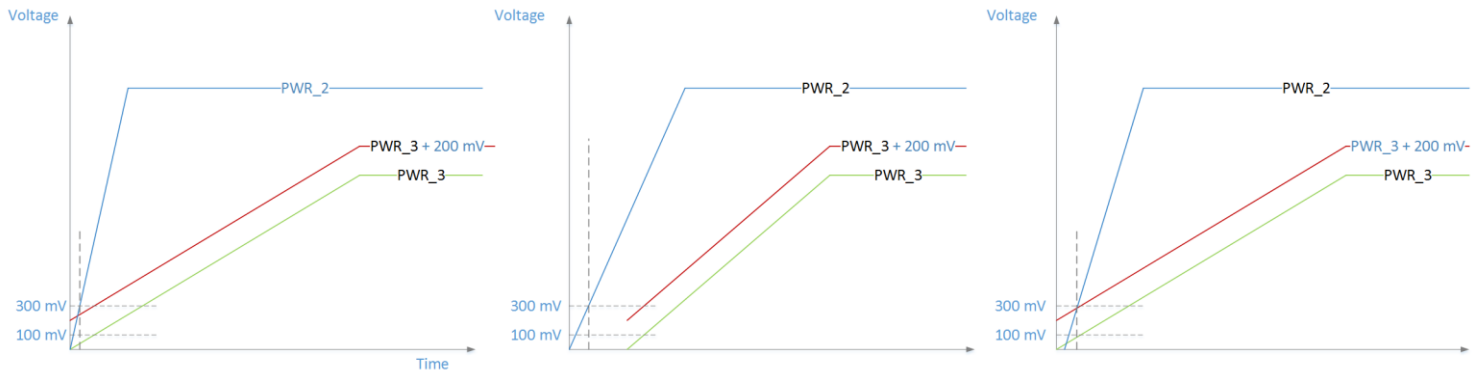
Figure 4-1.   Power-on Sequencing Examples

4.4.2.   BGA SSD Voltage Supply Power-off Sequencing

The host should apply the following recommendations for sequencing the voltages on the PWR_1 supply, the PWR_2 supply, and the PWR_3 supply during power-off:

❑ Before the voltage on the PWR_3 supply and the voltage on the PWR_2 supply reach 300 mV, the voltage on the PWR_2 supply should remain greater than voltage on the PWR_3 supply by at least 200 mV.

❑ After both the voltage on the PWR_2 supply and the voltage on the PWR_3 supply is below 300 mV, there is no specified relationship between them.

❑ The voltage on the PWR_1 supply has no timing relationship relative to the voltage on the PWR_3 supply or the voltage on the PWR_2 supply.

❑ The voltage on all supplies must remain below 100 mV for at least 1 ms before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 4-2 shows two power-off ramp examples that follow the recommendations of this section for the case where each of the power rails is assigned a different voltage. Note that the PWR_1 rail is not shown since it has no timing relationship to the other rails.
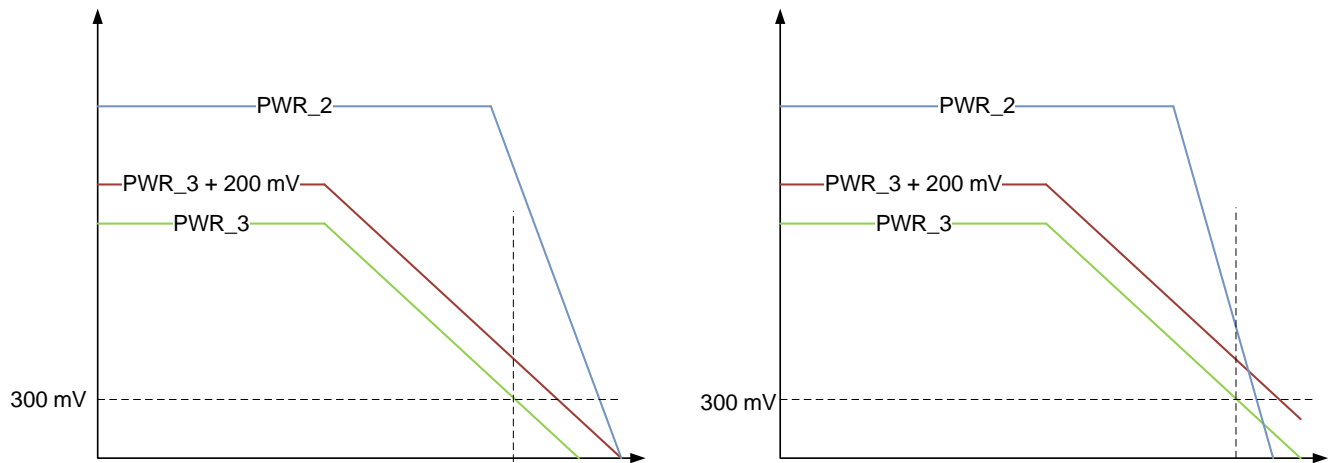
Figure 4-2.   Power-off Sequencing Examples

4.4.3.   BGA SSD Power Ramp Timing

The power ramp timing is defined as the time the power rail needs to ramp to a valid voltage (see Table 4-3). This timing is recommended for power-on only.

Table 4-3.   Power Ramp Timing

Supply Voltage	Max*
3.3 V	35 ms
2.5 V	30 ms
1.8 V	25 ms
1.2 V	20 ms
1.1 V	20 ms
1.0 V	20 ms
0.9 V	20 ms
0.8 V	20 ms
0.75 V	20 ms
* The minimum timing may be calculated from the maximum slew rate recommendation in Table 4-4.	

4.4.4.   BGA SSD Power Rail Slew Rate

The maximum power rail slew rate is shown in Table 4-4. These values are only defined for ESD protection purpose. They are not meant for inrush current control.

Table 4-4.   Power Rail Slew Rate

Parameter	Description	Max	Condition
$T_{SLEW\_3.3}$	Voltage slew rate of the 3.3 V power rail	100 kV/s	No Load
$T_{SLEW\_2.5}$	Voltage slew rate of the 2.5 V power rail	100 kV/s	No Load
$T_{SLEW\_1.8}$	Voltage slew rate of the 1.8 V power rail	100 kV/s	No Load
$T_{SLEW\_1.2}$	Voltage slew rate of the 1.2 V power rail	100 kV/s	No Load
$T_{SLEW\_1.1}$	Voltage slew rate of the 1.1 V power rail	100 kV/s	No Load
$T_{SLEW\_1.0}$	Voltage slew rate of the 1.0 V power rail	100kV/s	No Load
$T_{SLEW\_0.9.}$	Voltage slew rate of the 0.9 V power rail	100 kV/s	No Load
$T_{SLEW\_0.8.}$	Voltage slew rate of the 0.8 V power rail	100 kV/s	No Load
$T_{SLEW\_0.75}$	Voltage slew rate of the 0.75 V power rail	100 kV/s	No Load

4.4.5. BGA SSD Power Rail Parameters

All supply voltages and tolerances referenced for BGA SSD devices in this specification are considered to be measured at the component ball or pin. Supply tolerances are assumed to incorporate any superposition of AC, DC and system transient effects measured at the component ball or pin.

Table 4-5 describes the characteristics of the regulated power rails for BGA SSDs.

Table 4-5. Regulated Power Rail Parameters for BGA SSD Types

Nominal Voltage	Voltage Range	Platform Rail Type
+3.3 V	2.8 V to 3.6 V*	Always On
+2.5 V	2.45 V to 2.75 V	Always On
+1.8 V	1.7 V to 1.9 V	Always On
+1.2 V	1.14 V to 1.26 V	Always On
+1.1 V	1.06 V to 1.17 V	Always On
+1.0 V	0.95 V to 1.05 V	Always On
+0.9 V	0.86 V to 0.98 V	Always On
+0.8 V	0.76 V to 0.88 V	Always On
+0.75 V	0.71 V to 0.81 V	Always On
Note*: +3.3 V tolerance for BGA SSD differs from the tolerance in Table 4-21.		

4.5. Compliance Eye Limits at the M.2 Connector

The compliance eye limits defined in this section must be met for both M.2 Add-in Card and a Platform interfacing with such an Add-in Card. The specific measurement requirements (probe test

points, calibrated system board specifics, etc.) for compliance of physical components are to be specified in the *PCI Express Architecture, PHY Test Specification* document. A minimum sample size of 1.5×10^6 UI is required at 8.0 GT/s.

For connector heights not listed in Section 2.4, designers must exercise due diligence to confirm the channel requirements defined in this document are met.

4.5.1.   Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s

Eye Height (V_{TXA}, V_{TXA_d}) and Eye Width (T_{TXA}) limits for the M.2 Key-M based Add-in Card's Transmitter path compliance at 8.0 GT/s are defined in Table 4-6.

The Add-in Card shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral receiver Equalization Algorithm defined in the *PCI Express Base Specification* are applied.

A worst-case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must be greater than or equal to T_{TXA}.

The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately three inches of 85 Ω trace followed by 12.1 dB of 85 Ω trace, all behind a standard M.2 connector. This channel shall be referenced as the 8.0 GT/s M.2 Add-in Card Test Channel. This test channel is similar to the CEM 3.0 8.0 GT/s Add-in Card Test Channel but has additional 2" trace added to the Motherboard side to account for the differences in worse case CEM Add-in Card routing (4") and M.2 Add-in Card routing (2"). S-parameters for the 8.0 GT/s M.2 Add-in Card Test Channel are provided with this specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant motherboard. Figure 4-3 show the 8.0 GT/s M.2 Add-in Card Transmitter Path Compliance Eye Diagram.

Table 4-6. M.2 Key-M based Add-in Card Transmitter Path Compliance Eye Limits at 8.0 GT/s

Parameter	Min	Max	Units	Comments
V_{TXA}	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	1300	mV	
V_{TXA_d}	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	1300	mV	
T_{TXA}	41.25 (at 10^{-12} BER)		ps	Note 1
Notes: 1. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 1.5×10^6 UI.				
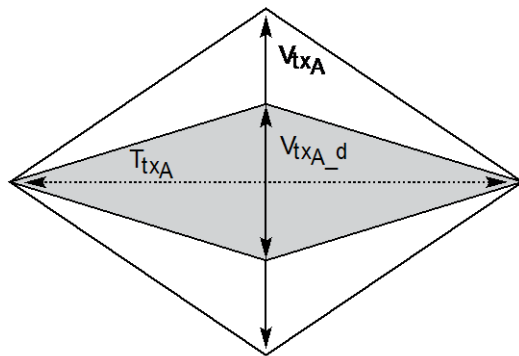
OM14758A

Figure 4-3. 8.0 GT/s M.2 Add-in Card Transmitter Path Compliance Eye Diagram

4.5.2. Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 8.0 GT/s are defined in Table 4-7 and Table 4-8. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's transmitter equalization may be adjusted using the setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters –then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case crosstalk that would be present with all lanes active, the additional crosstalk must be accounted for in some other way. The test is performed with two different test channels, a long test channel and a short test channel. While the receiver's capacity to adapt its own equalization is part of the test, its ability to request the link partner's transmitter to change its transmitter equalization is tested by applying a signal whose equalization level is suboptimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the receiver under test is more capable than the reference (CTLE+DFE) receiver, the receiver under test may not require the transmitter to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure must be used for the receiver test and if the receiver requires the transmitter equalization to change, such change must be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment for specific methodology details.

The 128/130b compliance pattern must be used during eye height and eye width calibration for this test. Modified compliance pattern is used when the receiver test is run.

Table 4-7. Long Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Calibration	Unit	Comments
$V_{RX-EH-8G}$ Eye Height	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	mV	Notes 1, 2, 3, 4, 7
$T_{RX-EH-8G}$ Eye Width	41.25 (at 10^{-12} BER)	ps	Notes 1, 2, 3, 7
Rj (Random Jitter)	3	Ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	12.5	ps PP	Notes 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	14	mV PP	Notes 3, 7

Notes:

1. An ideal reference clock without jitter is assumed for this specification.
2. The values in Table c-d are initially calibrated with a reference channel consisting of an 8.0 GT/s M.2 Add-in Card Test Channel followed by 8.0 GT/s M.2 System-Board Test Channel at the transmitter SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 8.0 GT/s transmitter test. After reference calibration, the 8.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into the M.2 connector.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.
7. This is target parameter for Receiver calibration. Allowable tolerances around this nominal number, when doing the calibration are specified in the *PCI Express Architecture, PHY Test Specification*.

Table 4-8.   Short Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Units	Comments
$V_{RX-EH-8G}$ Eye Height	N/A	N/A	mV	Notes 1, 2, 5
$T_{RX-EH-8G}$ Eye Width	N/A	N/A	ps	Notes 1, 2, 5
Rj (Random Jitter)	3		ps RMS	Note 4
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification.
2. The values in Table 4-8 are initially calibrated with a reference channel consisting of a M.2 Add-in Card short Test Channel followed by M.2 System-Board short Test Channel at the transmitter SMP connectors on the System-Board Short Test Channel. The calibration is done with M.2 compliance test fixtures without any additional ISI board or channel embedding. After reference calibration, the M.2 System-board short Test Channel is removed and the Add-in Card to be tested is placed into a M.2 connector.
3. Eye height and width are specified after application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

4.5.3.   System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification* are applied.

The system board Transmitter path measurements at 8.0 GT/s are made using a two-port measurement methodology. Refer to *PCI Express CEM Specification* for the details of the two-port methodology.

All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.

Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

This calculated eye width at BER 10^{-12} must be greater than or equal to T_{TXS}.

The values in Table 4-9 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 2.0 inches of 85 Ω trace, followed by a reference receiver package (3.5 dB) behind a standard PCI Express edge-finger. Figure 4-4 shows the 8.0 GT/s System Board transmitter path composite compliance eye diagram. This test channel shall be referenced as the 8.0 GT/s M.2 System-Board Test Channel. The S-parameters for the channel are provided with this specification. Additional loss from the measurement set-up must be removed. The M.2 System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant Add-in Card.

Table 4-9. System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Units	Comments
V_{TXS}	34 (10^{-12} BER) 46 (10^{-6} BER)	1300	mV	
T_{TXS_d}	34 (10^{-12} BER) 46 (10^{-6} BER)	1300	mV	
T_{TXS}	41.25 (10^{-12} BER)		ps	Note 1
Notes:				
1. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 1.5×10^6 UI.				
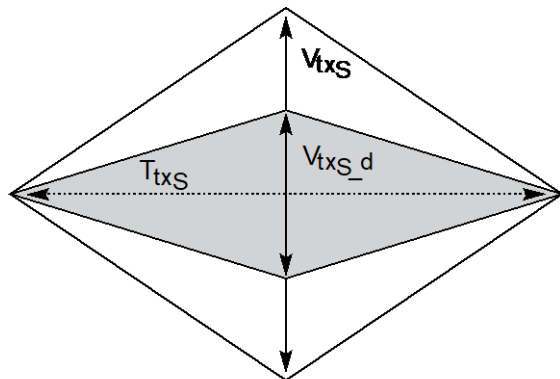
A-0335

Figure 4-4. 8.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

4.5.4. System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 8.0 GT/s are defined in Table 4-10. The receiver path shall be tested with a worst-case eye to verify that it

achieves a BER $< 10^{-12}$. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case crosstalk that would be present with all lanes active, the additional crosstalk must be accounted for in some other way.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the receiver under test is more capable than the reference (CTLE+DFE) receiver, the receiver may not require the transmitter to change its equalization levels to achieve a BER $< 10^{-12}$. In any case, equalization settings resulting from this procedure shall be used for the above receiver test and, if the receiver requires the transmitter equalization to change, the change accommodates the test set-up used. A specific methodology for this procedure is outside the scope of this specification.

The 128/130b compliance pattern must be used during eye height and eye width calibration for this test. Modified compliance pattern is used when the receiver test is run.

Table 4-10. System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Calibration	Max	Unit	Comments
$V_{RX-EH-8G}$ Eye Height	34 (at 10^{-12} BER)	34	mV	Notes 1, 2, 3, 4, 7
$T_{RX-EH-8G}$ Eye Width	41.25 (at 10^{-12} BER)	41.25	ps	Notes 1, 2, 3, 7
Rj (Random Jitter)	3		Ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Notes 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Notes 3, 7

Notes:
1. The system board reference clock is assumed for this specification. Eye height and width values refer to BER at 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s M.2 System Board Test Channel followed by 8.0 GT/s M.2 Add-in Card Test Channel at the TX SMP connectors on the M.2 Add-in Card Test Channel. The calibration is done with the same post processing as the M.2 Add-in Card 8.0 GT/s transmitter test. After reference calibration, the 8.0 GT/s M.2 Add-in Card Test Channel is removed, and the M.2 System Board Test Channel is connected to the System Board to be tested.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.
7. This is target parameter for Receiver calibration. Allowable tolerances around this nominal number, when doing the calibration are specified in the *PCI Express Architecture, PHY Test Specification*.

4.5.5.   Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s

The eye diagrams for the M.2 Add-in Card's Transmitter path compliance at 16.0 GT/s are defined in Table 4-11. The M.2 Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification*, are applied.

A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.

Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR4 trace with an insertion loss of 16.5 dB at Nyquist, followed by a root reference package all behind a standard M.2 connector. This test channel shall be referenced as the 16.0 GT/s M.2 Add-in Card Test Channel. S-parameters for the channel are provided with this specification (see Section 4.5.10). Additional loss from the measurement set-up must be removed. The M.2 Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant motherboard.

Table 4-11. M.2 Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s

Parameter	Min	Max	Units	Comments
V_{TXA}	23.75	1300	mV	Note 1
V_{TXA_d}	23.75	1300	mV	Note 1
T_{TXA}	25.31		ps	Note 2
Notes:				
1. The voltage measurements are done at a BER of 10^{-12}.				
2. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 2×10^6 UI.				

4.5.6.   Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the Add-in Card Receiver path compliance at 16.0 GT/s are defined in Table 4-12. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters –then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run.

Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-16G}$ and $T_{RX-EH-16G}$ are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s Add-in Card Test Channel portion of the channel.

The Eye Height and Eye Width values in Table 4-12 are initially calibrated with a reference channel consisting of an 16.0 GT/s M.2 Add-in Card Test Channel followed by an 16.0 GT/s M.2 System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 16.0 GT/s TX test. After reference calibration, the 16.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into a standard PCI Express connector. The end to end M.2 calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 16.0 GT/s calibration channel in the *PCI Express Base Specification*.

Table 4-12. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Units	Comments
$V_{RX-EH-16G}$ Eye Height	15	15	mV	Notes 1 and 2
$T_{RX-EH-16G}$ Eye Width	0.3	0.3	UI	Note 1
Rj (Random Jitter)	1.0		ps RMS	Notes 3 and 4
Sj (Sinusoidal Jitter) 100 MHz	6.25		Ps PP	Note 4
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	

Notes:
1. An ideal reference clock without jitter is assumed for this specification. Eye height and width values refer to BER of 10^{-12}.
2. Eye height limits do not account for limitations in test equipment voltage resolution.
3. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
4. Rj and Sj are measured without post-processing filters.

4.5.7. System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral receiver equalization algorithm defined in the *PCI Express Base Specification* are applied.

The system board Transmitter path measurements at 16.0 GT/s are made using a two-port measurement methodology. Refer to the *PCI Express CEM Specification* for the details of the two-port methodology.

All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.

Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

The values in Table 4-13 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 3.5 dB of 85 Ω trace, at 8 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This test channel shall be referenced as the 16.0 GT/s M.2 System-Board Test Channel. The S-parameters for the channel are provided with this specification (see Section 4.5.10). Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on an M.2 compliant Add-in Card. Figure 4-5 shows the 16.0 GT/s System Board Transmitter path composite compliance eye diagram.

Table 4-13.   System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Units	Comments
V_{TXS}	18.25	1300	mV	Note 1
V_{TXS_d}	18.25	1300	mV	Note 1
T_{TXS}	21.44		ps	Note 2
Notes:				
1. The voltage measurements are done at a BER of 10^{-12}.				
2. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2×10^6 UI.				
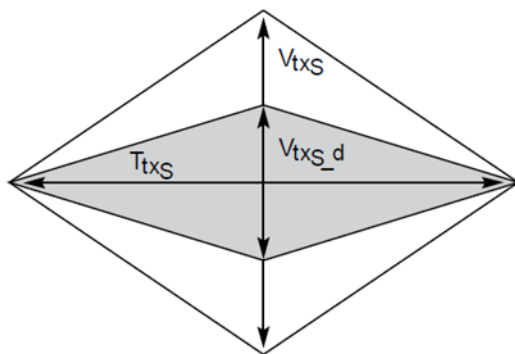
Figure 4-5.   16.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

4.5.8. System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 16.0 GT/s are defined in Table 4-14. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters, then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run.

The Eye Height and Eye Width values in Table 4-14 are initially calibrated with a reference channel consisting of a 16.0 GT/S M.2 System Board Test Channel followed by a 16.0 GT/s M.2 Add-in Card Test Channel. After reference calibration, the 16.0 GT/s M.2 Add-in Card Test Channel is removed, and the 16.0 GT/s M.2 System Board Test Channel is connected to the system board to be tested. The end to end M.2 calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 16.0 GT/s calibration channel in the PCI Express Base Specification.

Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-16G}$ and TRX-EH-16G are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s System Board Test Channel portion of the channel.

Table 4-14.   System Board Minimum Receiver Path Sensitivity
             Requirements at 16.0 GT/s

Parameter	Min	Max	Units	Comments
$V_{RX-EH-16G}$ Eye Height	15	15	mV	Notes 1 and 2
$T_{RX-EH-16G}$ Eye Width	0.3	0.3	UI	Note 1
Rj (Random Jitter)	1.0		ps RMS	Notes 3 and 4
Sj (Sinusoidal Jitter) 100 MHz	6.25		Ps PP	Note 4
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	

Notes:
1. An ideal reference clock without jitter is assumed for this specification. Eye height and width values refer to BER of 10^{-12}.
2. Eye height limits do not account for limitations in test equipment voltage resolution.
3. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
4. Rj and Sj are measured without post-processing filters.

4.5.9.   Add-in Card Transmitter Path Pulse Width Jitter (PWJ) limits at 16.0GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 4-15. The Add-in Card shall pass the timing requirements with the Jitter Measurement Pattern defined in the *PCI Express Base Specification*. The pulse width jitter requirements are evaluated after the -12 dB CTLE curve from the behavioral reference equalizer defined in the *PCI Express Base Specification*, is applied.

Table 4-15.   Add-in Card Transmitter Path Uncorrelated Pulse Width
             Jitter Requirements at 16.0 GT/s

Parameter	Min	Max	Units	Comments
$T_{TX-UPW-TJ}$	0	12.5	Ps PP @ BER 10^{-12}	
$T_{TX-UPW-DJDD}$	0	5.0	Ps PP @ BER 10^{-12}	

4.5.10.   Add-in Card Transmitter Path Compliance Eye Diagrams at 32.0 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 32.0 GT/s are defined in Table 4-16. The Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification*, are applied.

Table 4-16.   Add-in Card Transmitter Path Compliance Eye
Requirements at 32.0 GT/s

Parameter	Min	Max	Units	Comments
V_{TXA}	25.5	1300	mV	Notes 1, 2, 4
T_{TXA}	13.28		ps	Notes 1, 3, 4

Notes:
1. A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test. The eye limits in this Table are different than *PCIe Express Base Specification* to account for system board crosstalk that is not present during measurement.
2. V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12}.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 19.25 dB at 16 Hz, followed by a root reference package all behind a standard M.2 connector. This channel shall be referenced as the 32.0 GT/s M.2 Add-in Card Test Channel. S-parameters for the channel are provided with the specification. The M.2 Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a compliant motherboard.

4.5.11.   Add-in Card Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 32.0 GT/s are defined in Table 4-17. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

This adjustment is done through running the PCI Express training protocol. If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values. If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-17. M.2 Add-in Card Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

Parameter	Nominal	Units	Comments
$V_{RX-EH-32G}$ Eye Height	15	mV	Notes 1, 2, 4, 7
$T_{RX-EW-32G}$ Eye Width	0.3	UI	Notes 1, 2, 7
Rj (Random Jitter)	0.5	ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	3.125	ps PP	Notes 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	10	Mv PP	Notes 3, 7

Notes:
1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are calculated at BER of 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of a 32.0 GT/s M.2 Add-in Card Test Channel followed by a 32.0 GT/s System-Board Test Channel at the TX MMPX connectors on the System Board Test Channel. After reference calibration, the 32.0 GT/s System Board Test Channel is removed and the M.2 Add-in Card to be tested is placed into an M.2 connector. The end-to-end M.2 calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 32.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-32G}$ and $T_{RX-EW-32G}$ are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 32.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 32.0 GT/s stressed eye calibration process the variation must occur in the 32.0 GT/s M.2 Add-in Card Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
6. Rj and Sj are measured without post-processing filters.
7. Refer to *PCI Express Architecture Phy Test Specification* for allowed tolerances around nominal values.

4.5.12. System Board Transmitter Path Compliance Eye Diagram at 32.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification* are applied. The eye diagrams for the system board's Transmitter path compliance at 32.0 GT/s are defined in Table 4-18.

Table 4-18. System Board Transmitter Path Compliance Eye Requirements for 32.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Units	Comments
V_{TXS}	21	1300	mV	Notes 1, 2, 4
T_{TXS}	12.5		ps	Notes 1, 3, 4

Notes:
1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test. The eye limits in this Table are different than *PCIe Express Base Specification* to account for Add-in Card crosstalk that is not present during measurement.
2. V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. The sample size for this measurement is required to be at least 2×10^6 UI.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 3.3 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameters for the channel are provided with the specification. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on an M.2 Add-in Card.

4.5.13. System Board Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 32.0 GT/s are defined in Table 4-19. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER $< 10^{-12}$. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

This adjustment is done through running the PCI Express training protocol. If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values. If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-19.   System Board Minimum Receiver Path Sensitivity Requirements for 32.0 GT/s

Parameter	Nominal	Units	Comments
$V_{RX-EH-32G}$ Eye Height	15	mV	Notes 1, 2, 4, 7
$T_{RX-EW-32G}$ Eye Width	0.3	UI	Notes 1, 2, 7
Rj (Random Jitter)	0.5	ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	3.125	ps PP	Notes 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	10	Mv PP	Notes 3, 7

Notes:
1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to BER of 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of a 32.0 GT/s M.2 System Board Test Channel followed by a 32.0 GT/s M.2 Add-in Card Test Channel. After reference calibration, the 32.0 GT/s Add-in Card Test Channel is removed and the System Board Test Channel is connected to the system board to be tested. The end to end CEM calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 32.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-32G}$ and $T_{RX-EW-32G}$ are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 32.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 32.0 GT/s stressed eye calibration process the variation must occur in the 32.0 GT/s System Board Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
6. Rj and Sj are measured without post-processing filters.
7. Refer to *PCI Express Architecture Phy Test Specification* for allowed tolerances around nominal values.

4.5.14.   Test Channels

❑ The 4-port S-parameters for the System Test Channel with connector/edge-finger model and reference Add-in Card package are distributed with this specification in the following files:
  - System_board_test_channel_withpkg_8G_SE.s4p
  - System_board_test_channel_withpkg_16G_SE.s4p
  - System_board_test_channel_withpkg_32G_SE.s4p

❑ The 4-port s-parameters for the Add-in Card Test Channel without a standard connector/edge-finger model and with reference root package are distributed with this specification in the following file:
  - Add_in_Card_test_channel_withpkg_8G_SE.s4p
  - Add_in_Card_test_channel_withpkg_16G_SE.s4p
  - Add_in_Card_test_channel_withpkg_32G_SE.s4p

4.5.15. Transmitter De-emphasis and Equalization

De-emphasis is required for Add-in Cards and system boards to reduce ISI. For 5.0 GT/s and lower data rates, refer to the *PCI Express Base Specification* for de-emphasis requirements. For 8.0 GT/s and higher data rates, refer to the *PCI Express Base Specification* for equalization preset requirements. For implementation details, refer to the *PCI Express Base Specification*. A motherboard must meet eye diagram requirements defined in the *PCI Express Base Specification* at 8.0 GT/s and higher data rates on each lane with one or more preset equalization settings (Figure 4-6).
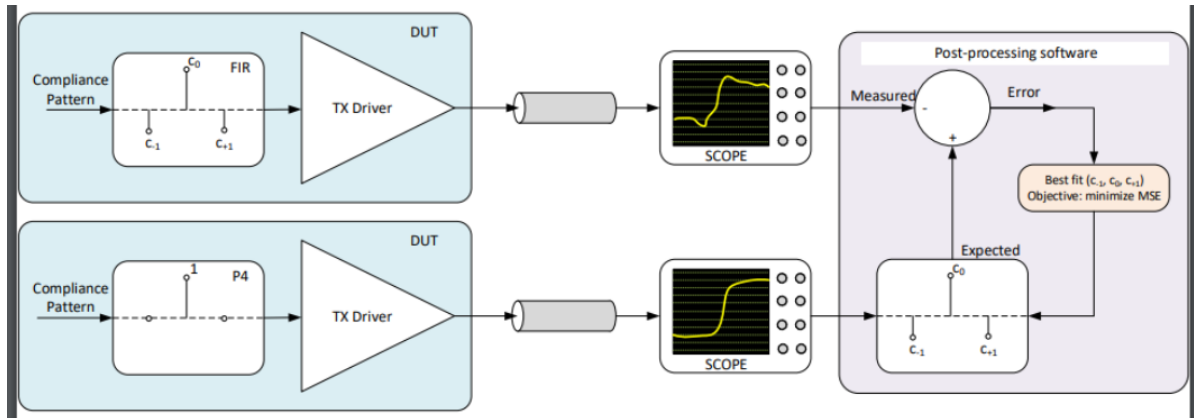
Note: Difference between best fit (c_{-1}, c_0, c_{+1}) coefficients and expected coefficients is used to compute equalization errors for pre-emphasis, de-emphasis, boost, and voltage swing.

Figure 4-6. TX Equalization Based on AC Fit Method

> **IMPLEMENTATION NOTE: Preset Test Requirements at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s**
>
> All Add-in Cards and system boards operating at 8.0 GT/s and 16.0 GT/s are required to meet the preset test as described in the *PCI Express Base Specification*. The test consists of acquiring the Tx compliance waveforms from the device under test for each preset then analyzing the waveforms together to confirm that the preset requirements have been met. For 32.0 GT/s, post-processing for Preset test will be done differently than defined in the *PCI Express Base Specification*, using AC fitting method (see Figure 4-6).

A system board shall meet the following additional rules for this specification:

- The system board initial TX preset at 8.0 GT/s shall be P1, P7, or P8, unless the next point applies.
- If the equivalent of the ps21TX parameter defined in the *PCI Express Base Specification*, measured at data rates of 8.0 GT/s at the end of the 8.0 GT/s System-Board Test Channel without de-embedding shows a loss of more than 12 dB, then the system board initial TX preset at 8.0 GT/s shall be P7 or P8. The system board initial TX preset at 16.0 GT/s shall be P7 if the Add-in Card does not request an initial preset.
- The system board initial TX preset at 32.0 GT/s shall be P5 if the Add-in Card does not request an initial preset.

An Add-in Card shall meet the following additional rules for this specification:

❑ If the system board loss is less than 12 dB the Add-in Card shall receive with a BER of less than 10^{-4} at 8.0 GT/s with presets P1, P7, and P8.

❑ If the system board loss is more than 12 dB, the Add-in Card shall receive with a BER of less than 10^{-4} at 8.0 GT/s with presets P7 and P8.

❑ The Add-in Card shall receive with a BER of less than 10^{-4} at 16.0 GT/s with preset P7 if it does not request a specific initial preset at 16.0 GT/s. If the Add-in Card does request an initial preset at 16.0 GT/s it must be able to receive with a BER of less than 10^{-4} at the request preset.

❑ The Add-in Card shall receive with a BER of less than 10^{-4} at 32.0 GT/s with preset P5 if it does not request a specific initial preset at 32.0 GT/s. If the Add-in Card does request an initial preset at 32.0 GT/s it must be able to receive with a BER of less than 10^{-4} at the requested preset.

4.5.16. System Board and Add-in Card Transmitter Jitter at 32.0 GT/s

The Total Uncorrelated Pulse Width Jitter, Uncorrelated Deterministic Pulse Width Jitter, Uncorrelated Total Jitter, and Uncorrelated Deterministic Jitter (TTX-UPW-TJ, TTX-UPW-DJDD, TTX-UTJ, and TTX-UDJDD) requirements at a BER of 10^{-12} are defined in Table 4-20.

The system board and the Add-in Card must pass the jitter requirements with the Jitter Measurement Pattern defined in the *PCI Express Base Specification*. Select one of Setting #47 through #54 depending on the lane being tested. Lane under test must transmit Jitter Measurement Pattern and all other lanes must transmit Compliance Pattern. The jitter requirements are evaluated after the optimal CTLE curve ranging from -5 dB to -15 dB from the behavioral reference equalizer, defined in the *PCI Express Base Specification*, is applied. Either the CTLE curve or no CTLE, whichever gives the lowest value of TTX-UPW-TJ, is used for all jitter measurements.

Table 4-20. System Board and Add-in Card Transmitter Jitter Requirements at 32.0 GT/s

Parameter	Description	Max	Units	Comments
$T_{TX-UPW-TJ}$	Total Uncorrelated Pulse Width Jitter	6.25	ps PP at 10^{-12}	See Note
$T_{TX-UPW-DJDD}$	Deterministic DjDD Uncorrelated Pulse Width Jitter	2.5	ps PP	
T_{TX-UTJ}	TX Uncorrelated Total Jitter	6.25	ps PP at 10^{-12}	
$T_{TX-UDJDD}$	TX Uncorrelated Deterministic Jitter	3.125	ps PP	
Notes: The transmitter must meet the indicated limits in presence and absence of reference clock SSC.				

4.6. Power

4.6.1. M.2 Adapter Power

The M.2 Adapter (excluding BGA SSDs and M.2-1A) utilizes a single regulated power rail of 3.3 V provided by the Platform. See Table 4-5 for power requirements for BGA SSDs. In some pinout Adapters, there is a dedicated VIO supply pin called VIO 1.8 V that is intended to only bias the I/O circuitry of the Adapter. Signals that are powered by VIO 1.8 V in Key M PCIe-based Adapters or by an internal voltage source for Key B and Key B-M specifically must be 3.3 V tolerant in the event that

VIO 1.8 V is not provided by the Platform. The main 3.3 V and the VIO voltage rail sources on the Platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

❑ Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.

❑ Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and support up to 2 A continuous.

❑ The Socket 2 board types have five power pins in their pinouts and support up to 2.5 A continuous. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.

❑ The Socket 3 board types, with a single Add-in Card Key, have nine power pins and support up to 3.5 A continuous. Continuous current requires sufficient power dissipation capability (e.g., airflow, heat sink, etc.). This capability is outside the scope of this specification. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.

❑ The extra power pins, beyond the number of pins that support the continuous current, enable reduced IR-drop for these devices.

> **Note:** The power rail voltage tolerance listed in Table 4-21 is ±5% for 3.3 V rail. This is different from the +9% -5% tolerance allowed in the *PCI Express Mini CEM Specification*.
>
> Table 4-25 does not apply to BGA SSD (see Table 4-21)

Table 4-21.   M.2 Key Regulated Power Rail Parameters

Power Rail	Pin Name	Voltage Tolerance	Platform Rail Type
3.3 V	3.3 V	±5%	Always On
1.8 V	VIO 1.8 V	±5.55% (see Note)	Always On
Note: 1.7 V to 1.9 V Range			

4.6.2.   M.2-1A Add-in Card

For M.2-1A Add-in Card designs, the number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2-1A connector current handling capability per pin. The M.2-1A connector pin is defined as needing to support 1000 mA/pin continuous. This yields the required number of power rail pins per pinout.

> **Note: For all M.2-1A Add-in Card types and sockets**
>
> M.2-1A sockets with continuous current exceeding 0.5A per pin requires analysis to determine the sufficient power dissipation requirements (e.g., airflow, heat sink, etc.). This capability is outside the scope of this specification.
>
> All adapters should contain a method to ensure safe operating device temperatures are not exceeded

❑ Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and support up to 4 A continuous. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.

❑ The Socket 2 board types have five power pins in their pinouts and support up to 5 A continuous. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.

❑ The Socket 3 board types, with a single Add-in Card Key, have nine power pins and support up to 9 A continuous. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.

> **Note: For all M.2-1A Add-in Card types**
>
> System vendors should have the capabilities to provide full continuous power to M.2-1A Add-in Card sockets as described in section 4.6.2. See Table 4-25 regulated power rail parameters.

Table 4-22.   M.2-1A Key Regulated Power Rail Parameters

Power Source	Pin Number	Voltage Tolerance	Platform Rail Type
3.3 V	3.3 V	+5/-vlow% (see Note 2)	Always On
1.8 V	VIO 1.8 V	±5.5% (see Note 1)	Always On
Notes:			
1. 1.7 V to 1.9 V Range			
2. Vlow% requirements are defined in Section 4.6.3			

4.6.3.   M.2-1A vlow Tolerance Specification

Power supply IR loss needs to be accounted for in the connector contacts which affects the module minimum supply voltage. These connector IR losses reduce the voltage minimum seen by the modules after passing thru the connector contact pins. This IR loss has an effect on the voltage supply to M.2-1A Add-in Cards due to the increased current of M.2-1A connectors pins. Each module supplier has to account for this voltage loss based on the maximum current needs of the specific module design, Table 4-23 outlines the new module voltage supply minimums.

Table 4-23.   M.2-1A vlow% Requirements

Current (A) (Per Pin)	Device	Socket	Key	Primary Interface Used	Number of Power Pins (Input Current)	Number of GND Pins (Out Current)	Number of GND Stand-offs (Out Current)	Equivalent Input Pin Resistance (0.075 Ω per Pin-max)	GND Pin Equivalent Resistance	GND Stand-off Resistance (0.003 Ω Max Peer Stand-off)	Total Connector Equivalent Resistance (R)	Total Voltage Drop	% Additional Drop of 3.3 V	Calculated Min Voltage vlow (V)	Calculated total vlow (%)	Approx Max Total Current (Module)	Approx Max Total Watt (Module)
0.10	M.2-1A	1	A-E	All	4	10	1	0.0188	0.0075	0.0030	0.0209	0.0084	-0.3%	3.127	-5.3%	0.40	1.32
0.20												0.0167	-0.5%	3.118	-5.5%	0.80	2.64
0.30												0.0251	-0.8%	3.110	-5.8%	1.20	3.96
0.40												0.0334	-1.0%	3.102	-6.0%	1.60	5.28
0.50												0.0418	-1.3%	3.093	-6.3%	2.00	6.60
0.60												0.0501	-1.5%	3.085	-6.5%	2.40	7.92
0.70												0.0585	-1.8%	3.077	-6.8%	2.80	9.24
0.80												0.0669	-2.0%	3.068	-7.0%	3.20	10.56
0.90												0.0752	-2.3%	3.060	-7.3%	3.60	11.88
1.00												0.0836	-2.5%	3.051	-7.5%	4.00	13.20
0.10	M.2-1A	2	B-M	PCIe-SSD	5	8	1	0.0150	0.0094	0.0030	0.0173	0.0086	-0.3%	3.126	-5.3%	0.50	1.65
0.20												0.0173	-0.5%	3.118	-5.5%	1.00	3.30
0.30												0.0259	-0.8%	3.109	-5.8%	1.50	4.95
0.40												0.0345	-1.0%	3.100	-6.0%	2.00	6.60
0.50												0.0432	-1.3%	3.092	-6.3%	2.50	8.25
0.60												0.0518	-1.6%	3.083	-6.6%	3.00	9.90
0.70												0.0605	-1.8%	3.075	-6.8%	3.50	11.55

Current (A) (Per Pin)	Device	Socket	Key	Primary Interface Used	Number of Power Pins (Input Current)	Number of GND Pins (Out Current)	Number of GND Stand-offs (Out Current)	Equivalent Input Pin Resistance (0.075 Ω per Pin-max)	GND Pin Equivalent Resistance	GND Stand-off Resistance (0.003 Ω Max Peer Stand-off)	Total Connector Equivalent Resistance (R)	Total Voltage Drop	% Additional Drop of 3.3 V	Calculated Min Voltage vlow (V)	Calculated total vlow (%)	Approx Max Total Current (Module)	Approx Max Total Watt (Module)
0.80												0.0691	-2.1%	3.066	-7.1%	4.00	13.20
0.90												0.0777	-2.4%	3.057	-7.4%	4.50	14.85
1.00												0.0864	-2.6%	3.049	-7.6%	5.00	16.50
0.10	M.2-1A	2	B-M	SATA	5	9	1	0.0150	0.0083	0.0030	0.0172	0.0086	-0.3%	3.126	-5.3%	0.50	1.65
0.20												0.0172	-0.5%	3.118	-5.5%	1.00	3.30
0.30												0.0258	-0.8%	3.109	-5.8%	1.50	4.95
0.40												0.0344	-1.0%	3.101	-6.0%	2.00	6.60
0.50												0.0430.	-1.3%	3.092	-6.3%	2.50	8.25
0.60												0.0516	-1.6%	3.083	-6.6%	3.00	9.90
0.70												0.0602	-1.8%	3.075	-6.8%	3.50	11.55
0.80												0.0688	-2.1%	3.066	-7.1%	4.00	13.20
0.90												0.0774	-2.3%	3.058	-7.4%	4.50	14.85
1.00												0.0860	-2.6%	3.049	-7.6%	5.00	16.50
0.10	M.2-1A	2	B	USB 3.1 GEN-1, PCIe WWAN	5	10	1	0.0150	0.075	0.030	0.0071	0.0086	-0.3%	3.126	-5.3%	0.50	1.65
0.20												0.0171	-0.5%	3.118	-5.5%	1.00	3.30
0.30												0.0257	-0.8%	3.109	-5.8%	1.50	4.95
0.40												0.0343	-1.0%	3.101	-6.0%	2.00	6.60
0.50												0.0429.	-1.3%	3.092	-6.3%	2.50	8.25
0.60												0.0514	-1.6%	3.084	-6.6%	3.00	9.90
0.70												0.0600	-1.8%	3.075	-6.8%	3.50	11.55
0.80												0.0686	-2.1%	3.066	-7.1%	4.00	13.20
0.90												0.0771	-2.3%	3.058	-7.4%	4.50	14.85
1.00												0.0857	-2.6%	3.049	-7.6%	5.00	16.50
0.10	M.2-1A	3	M	All	9	13	1	0.0083	0.058	0.030	0.0103	0.0093	-0.3%	3.126	-5.3%	0.90	2.97
0.20												0.0186	-0.6%	3.116	-5.6%	1.80	5.94
0.30												0.0278	-0.8%	3.107	-5.8%	2.70	8.91
0.40												0.0371	-1.1%	3.198	-6.1%	3.60	11.88
0.50												0.0464	-1.4%	3.089	-6.4%	4.50	14.85
0.56												0.0515	-1.6%	3.083	-6.6%	5.00	16.50
0.60												0.0557	-1.7%	3.079	-6.7%	5.40	17.82
0.60												0.0557	-1.7%	3.079	-6.7%	5.40	17.82
0.80				N/A See Note								0.0742	-2.2%	3.061	-7.2%	7.20	23.76
0.90												0.0835	-2.5%	3.052	-7.5%	8.10	26.73
1.00												0.0928	-2.8%	3.042	-7.8%	9.00	29.70

Note. Module max peak current allowed would not permit this current number to exist per pin

4.6.4.   M.2-1A Adapter Power Rating

The power rating of each M.2-1A Add-in Card type is different based on the technology that is enabled and defined by the M.2-1A connector key. All adapters should contain a method to ensure safe operating device temperatures are not exceeded. A list of connector keys and the power rating enabled for those keys is given in Table 4-24.

Table 4-24.   Power Rating Table for M.2-1A Add-in Cards

Key	Power Rail	Voltage Tolerance Note 5, 6	Current Consumption Limit	
			Peak(Note 1, 4) mA Max Avg @ 100 µs	Norma (Note 2) mA Max Avg @ 1 s
A	3.3 V	vlow to 3.465 V	4800	4000
B	3.3 V	vlow to 3.465 V	6000	5000
B	V_{BAT} (Note 3)	vlow to 4.4 V	6000	5000
E	3.3 V	vlow to 3.465 V	4800	4000
M	3.3 V	vlow to 3.465 V	7000	5000
M, B, A	VIO 1.8 V	±5.55% (Note 7)	70	

Notes:

1.   Peak is the maximum highest averaged current value over any 100 µs period.

2.   Normal is the maximum highest averaged current value over any 1 s period.

3.   Power Rail connection alternative for WWAN specific Adapters only. Not supported by other Socket 2 Adapter types such as SSDs.

4.   The peak current's duty cycle shall ensure that the normal current is not violated.

5.   The measurement location of voltage is at the Add-in Card gold finger.

6.   See the Calculated Min Voltage Vlow(V) column in Table 4-23. (Note 3)

7.   1.7 to 1.9 V range.

The operation of the 3.3 V power source must conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document.

4.6.5.   Direct VBAT Connection Option for WWAN Adapters (M.2 and M.2-1A)

The 3.3 V regulated power rail can be replaced with a direct V_{BAT} connection for Socket 2 WWAN-specific Adapters only. This type of power connection is optional and primarily for Tablet platforms. Direct V_{BAT} connections are not supported by other Socket 2 Adapter types such as SSDs. In the case of a WWAN-specific Adapter with a direct V_{BAT} connection, the Adapter needs to produce any and all required voltages to support those Adapters and meet the host interface voltage levels defined in Section 3.2. The current limit per pin of 500 mA/power pin for M.2 and 1 A/power pin for M.2-1A would still apply even if connected to V_{BAT}. Note that the requirements in Table 4-25 only apply to Socket 2 WWAN-specific Adapter pinouts.

Table 4-25.   Key V$_{BAT}$ Power Rail Parameters

Power Source	V$_{MIN}$	V$_{MAX}$	Cell Type
V$_{BAT}$	3.135 V	4.4 V	One cell Li-ion battery

4.6.6.   Adapter Power Rating

The power rating of each M.2 Adapter type is different based on the technology that is enabled and defined by the M.2 connector key. A list of connector keys and the power rating enabled for those keys is given in Table 4-26.

Table 4-26.   Power Rating Table for M.2 Add-in Cards

Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak (Note 1) mA Max Avg @ 100 µs	Normal (Note 2) mA Max Avg @ 1 s
A	3.3 V	± 5%	2000	
B	3.3 V	± 5%	5000 (Note 6)	2500 (Note 5)
B	V$_{BAT}$ (Note 3)	3.135 V to 4.4 V	2500	
C	3.3 V	± 5%	2500	
C	V$_{BAT}$	3.135 V to 4.4 V	2500	
C	VIO 1.8 V	± 5.55% (Note 4)	70	
D	RFU	RFU	RFU	RFU
E	3.3 V	± 5%	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
M	3.3 V	± 5%	7000 (Note 6)	3500 (Note 5)
M	VIO 1.8 V	± 5.55% (Note 4)	70	

Notes:
1. Peak is the maximum highest averaged current value over any 100 µs period
2. Normal is the maximum highest averaged current value over any 1 s period
3. Power Rail connection alternative for WWAN specific Adapters only. Not supported by other Socket 2 Adapter types such as SSDs
4. 1.7 V to 1.9 V Range
5. Normal currents assume sufficient power dissipation capability by the Platform. This capability is outside the scope of this specification. The maximum power of device may be controlled through function specific capabilities (e.g., for SSDs see NVMe).
6. The peak current's duty cycle shall ensure that the normal current is not violated.

The operation of the 3.3 V power source must conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document.

5

5. Platform Socket Pinout and Key Definitions

> All pinouts tables in this section are written from the platform/system point of view when referencing signal directions.

In all pinouts, the Power Rail referred to in the M.2 connectors is the 3.3 V rail unless otherwise indicated.

The M.2 pinouts are primarily intended to allocate specific pin functionalities that need to be routed on the Platform side to the respective Edge Card Slot Connector. Although many Host I/Fs are supported in the various pinouts, it does not necessarily imply that all I/F needs to be supported by the Adapter at the same time. However, the assigned allocations will enable each vendor and Platform to design their circuits with the aligned pin assignment.

In some cases, multiple Host I/Fs and other signals are overlaid using the same pin assignment. In these cases, there are sense pins that clearly identify what assignment is supported by the Adapter so that automatic multiplexing/routing would be possible on the Platform.

A mechanical connector key/Add-in Card key scheme is introduced to distinguish between different pinouts and functionalities because of the various connectorized pinout assignments needed in support of the multiple add-in functions and to prevent wrongful insertions. However, all these connectors share the same basic connection scheme of a Gold Finger Edge Card that plugs into a slot connector mounted on the Platform side. Connector mating occurs when the Connector Key and Add-in Card key align to the same location.

The connector key/Add-in Card key system used in conjunction with the M.2 75-position connector enables up to 12 unique key locations and assignments. Different Keys are needed when the family of host interfaces differ significantly from each other in support of the different types of Sockets in a Platform. Connector Keys are associated with the Socket Connector on Platform while Add-in Card Keys are associated with the Card Edge connection on the Add-in Card side.

The initial Key assignments are listed in Table 5-1. Key ID assignment must be approved by the PCI-SIG. Unauthorized use of Key IDs render this use as non-compliant to M.2 specifications.

Table 5-1.   Mechanical Key Assignments

Key ID	Pin Location	Key Definition
A	8-15	DisplayPort Based Connectivity
B	12-19	WWAN/SSD/Others Primary Key
C	16-23	WWAN Key
D	20-27	RFU
E	24-31	SDIO Based Connectivity
F	28-35	Future Memory Interface
G	39-46	Generic (Not used for M.2)
H	43-50	RFU
J	47-54	RFU
K	51-58	RFU
L	55-62	RFU
M	59-66	SSD 4 Lane PCIe

5.1.   Connectivity Socket; Socket 1

Connectivity Socket 1 will have two Key and Pinouts variations in support of multiple Connectivity Add-In functions (such as Wi-Fi + BT) along with some additional wireless solutions such as GNSS, NFC, or WiGig. The different Keys will support variations of the functional Host I/Fs as listed in Table 5-2.

Table 5-2.   Socket 1 Versions

	Socket Version	
	Socket 1 – SDIO Based	Socket 1 – DisplayPort Based
Mechanical Key	E	A
Wi-Fi	PCIe	
	SDIO	(see Note 1)
BT	USB	
	PCM/UART	(see Note 1)
WiGig	PCIe	
	(see Note 1)	DP x4
NFC	I2C (or USB or UART) (see Note 2)	
Adapter Types	1630, 2230, 3030	2230, 3030

Notes: 1. Not supported
2. Function to host interface allocation is a preferred example. Alternative function to host interface allocations are possible if using the host interfaces supported in the pinout and in agreement between Customer ←→ Vendor.

Since several of the interfaces listed in Table 5-2 have common signals located at the exact same pin locations with only some interfaces and mechanical keys trading places, it is possible to create Adapters with a dual Add-in Card Key that plugs into two different Connector Keys.

5.1.1. DisplayPort Based Socket 1 (Mechanical Key A) On Platform

❑ DisplayPort Based Socket 1 pinouts Key A is intended to support Wireless Connectivity devices including combinations of Wi-Fi, BT, NFC, and/or WiGig. Other Combos are possible provided they use the defined Host I/Fs in the pinouts.

❑ PCIe Lane 0 is intended for use with the Wi-Fi.

❑ PCIe Lane 1 is intended for use with the WiGig if the PCIe Lane 0 is not shared with the Wi-Fi.

❑ Four Lane DisplayPort with assorted sideband signaling is also intended for use with the WiGig.

❑ LED_1# and W_DISABLE1# are intended for use with the Wi-Fi and WiGig.

❑ USB and LED_2# are intended for use with the BT. There is only one W_DISABLE# supported by default. An adjacent Reserved pin (Pin 54) is used alternatively as W_DISABLE2# for the BT.

❑ I2C and ALERT are intended for use with NFC.

❑ COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to the Socket 2 COEX signals for coexistence with the WWAN solution.

❑ Other Comm/host interface combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor⬅➡Customer.

Table 5-3 provides a list of pin assignments on Socket 1 with mechanical key A.

Table 5-3. DisplayPort Based Socket 1 Pinout Diagram (Mechanical Key A) On Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	REFCLKn1	73
72	3.3 V	REFCLKp1	71
70	PEWAKE1# (I/O)(0/3.3V)	GND	69
68	CLKREQ1# (I/O)(0/3.3V)	PERn1	67
66	PERST1# (O)(0/3.3V)	PERp1	65
64	VIO 1.8 V	GND	63
62	ALERT# (I)(0/1.8 V)	PETn1	61
60	I2C_CLK (O)(0/1.8 V)	PETp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (O)(0/1.8V/3.3V)	PEWAKE0# (I/O)(0/1.8V/3.3V)	55
54	W_DISABLE2# (O)(0/1.8V/3.3V)	CLKREQ0# (I/O)(0/1.8V/3.3V)	53
52	PERST0# (O)(0/1.8V/3.3V)	GND	51
50	SUSCLK (O)(0/1.8V/3.3V)	REFCLKn0	49
48	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
46	COEX_RXD (I)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	GND	PETp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (I/O)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DP_ML3n	19
18	VIO_CFG (I)	DP_MLDIR (I)	17
16	LED_2# (I)(OD)	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	GND	7
6	LED_1# (I)(OD)	USB_D-	5
4	3.3 V	USB_D+	3
2	3.3 V	GND	1

5.1.2. SDIO Based Socket 1 (Mechanical Key E) On Platform

❑ SDIO Based Socket 1 pinouts Key E is intended to support Wireless Connectivity devices including combinations of Wi-Fi, BT, NFC, and/or GNSS. Other Combos are possible provided they use the defined Host I/Fs.

❑ PCIe Lane 0 or SDIO, LED_1#, and W_DISABLE1# are intended for use with Wi-Fi.

❑ USB or UART+PCM, LED_2# is intended for use with BT. There is only one W_DISABLE# supported by default. An adjacent Reserved pin (Pin 54) is used alternatively as W_DISABLE2# for the BT.

❑ PCIe Lane 1 is intended for future expansion in case a two Lane PCIe is needed (e.g., with WiGig Combo).

❑ I2C and ALERT# are intended for use with NFC.

❑ COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to Socket 2 COEX signals for coexistence with the WWAN solution.

❑ Other Comm or host interface combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor⬅➡Customer.

The pin assignments on SDIO Based Socket 1 with mechanical key E are given in Table 5-4.

Table 5-4.   SDIO Based Socket 1 Pinout Diagram (Mechanical Key E) On Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	RESERVED/REFCLKn1	73
72	3.3 V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PERn1	67
66	UIM_SWP/PERST1#	RESERVED/PERp1	65
64	VIO 1.8 V	GND	63
62	ALERT# (I)(0/1.8 V)	RESERVED/PETn1	61
60	I2C_CLK (O)(0/1.8 V)	RESERVED/PETp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (O)(0/1.8V/3.3V)	PEWAKE0# (I/O)(0/1.8V/3.3V)	55
54	W_DISABLE2# (O)(0/1.8V/3.3V)	CLKREQ0# (I/O)(0/1.8V/3.3V)	53
52	PERST0# (O)(0/1.8V/3.3V))	GND	51
50	SUSCLK (O)(0/1.8V/3.3V)	REFCLKn0	49
48	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
46	COEX RXD (I)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART_RTS (O)(0/1.8V)	PETp0	35
34	UART_CTS (I)(0/1.8V)	GND	33
32	UART_TXD (O)(0/1.8V)	CONNECTOR KEY E	
	CONNECTOR Key E	CONNECTOR KEY E	
	CONNECTOR Key E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	SDIO_RESET#/_TX_BLANKING (O)(0/1.8V)	23
22	UART_RXD (I)(0/1.8V)	SDIO_WAKE# (I) (0/1.8V)	21
20	UART_WAKE# (I)(0/3.3V)	SDIO_DATA3 (I/O) (0/1.8V)	19
18	VIO_CFG (I)	SDIO_DATA2 (I/O) (0/1.8V)	17
16	LED_2# (I)(OD)	SDIO_DATA1 (I/O) (0/1.8V)	15
14	PCM_OUT/I2S_SD_OUT (O)(0/1.8V)	SDIO DATA0 (I/O) (0/1.8V)	13
12	PCM_IN/I2S_SD_IN (I)(0/1.8V)	SDIO_CMD (I/O) (0/1.8V)	11
10	PCM_SYNC/I2S_WS (I/O)(0/1.8V)	SDIO_CLK/SYSCLK (O) (0/1.8V)	9
8	PCM_CLK/I2S_SCK (I/O)(0/1.8V)	GND	7
6	LED_1# (I)(OD)	USB_D-	5
4	3.3 V	USB_D+	3
2	3.3 V	GND	1

5.1.3. Dual Key Add-in Card: Supports SDIO Based Socket 1 and DisplayPort Based Socket 1

In cases where the Connectivity type solutions adopt the Dual Add-in Card Key scheme, where the solution use only PCIe, USB, and I2C host interfaces, they are capable of being inserted into both SDIO Based Socket 1 and DisplayPort Based Socket 1.

See Table 3-10 for an example of an Add-in Card-side pinouts that makes use of the Dual Add-in Card Key option.

5.2. WWAN+GNSS/SSD/Other Socket; Socket 2

Socket 2 supports various WWAN+GNSS (Global Navigation Satellite System that includes GPS, GLONASS, and/or Galileo), SSD, and other functional Adapters. Key B supports different types of functional Adapters while Key C is primarily targeting WWAN+GNSS functional Adapters. In Key B, this is done by overlaying functional pins that are identified with the aid of Configuration pins and/or having functional pins at different pin allocations in the pinout. In Key C, this is done by overlaying functional pins that are set/defined in a specific implementation in a BTO/CTO agreement between customer and vendor.

Socket 2 is primarily targeted for board types 2230, 2242, 3042, 3052 3060, 2260, 2280, and 22110 board sizes. See Table 2-1 for board sizes associated with different functional Adapter types.

5.2.1. Socket 2 Module Key B

5.2.1.1. Socket 2 Key B – Configuration Pin Definitions

The Socket 2 Key (Mechanical Key B) is unique in that it enables five major pinouts configurations and four variants for each of the three WWAN configurations. The five major configurations supported are:

❑ WWAN that is PCIe Based

❑ WWAN that is SSIC Based

❑ WWAN that is USB3.1 Gen1 or PCIe/USB3.1 Gen1 Based

❑ SSD that is PCIe (2 lane) Based

❑ SSD that is SATA Based

All Socket 2 WWAN pinouts configurations (1, 2, and 3) support USB2.0 and USB HS with the generic USB_D+/USB_D- pins as a baseline. All three have four alternate functional pins, with the aid of twelve GPIO pin allocations, in support of various secondary functions such as GNSS interface and coexistence pins, second UIM support, Audio support, and RFU pins.

The Platform must read all four Configuration pins so it clearly identifies which unique configurations needed to be supported. The Platform is capable of identifying when no Add-in Card is plugged into the slot.

It is mandatory that the Add-in Card side maintain the Configuration Pin states correctly to enable interoperability between the systems that make use and do not make use of these Configuration Pins. The Configuration Pins are:

❑ Pin 21 – CONFIG_0
❑ Pin 69 – CONFIG_1
❑ Pin 75 – CONFIG_2
❑ Pin 1 – CONFIG_3

For the Platform to read these Configuration bits, it must pull-up these four pins to an appropriate power rail. If designed properly, the Platform is capable of reading these configuration bits even if the Add-in Card is not powered up.

Table 5-5 shows all the variant configurations as a function of the configuration bits. The Platform adjusts its host interface connection and supports signal connections to the proper setting to work with the Add-in Card.

Table 5-5.   Socket 2 Add-in Card Configuration Table

Add-in Card Configuration Decodes				Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD – SATA	N/A
0	1	0	0	SSD – PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN – PCIe, USB3.1 Gen1	0 [Notes 4, 5]
0	1	0	1	WWAN – PCIe, USB3.1 Gen1	1 [Notes 4, 5]
0	0	1	1	WWAN – PCIe, USB3.1 Gen1	2 [Notes 4, 5]
0	1	1	1	WWAN – PCIe, USB3.1 Gen1	3 [Notes 4, 5]
1	0	0	0	WWAN – SSIC	0
1	1	0	0	WWAN – SSIC	1
1	0	1	0	WWAN – SSIC	2
1	1	1	0	WWAN – SSIC	3
1	0	0	1	WWAN – PCIe	2
1	1	0	1	WWAN – PCIe	3
1	0	1	1	WWAN – PCIe, USB3.1 Gen1	Vendor-defined [Notes 3, 5]
1	1	1	1	No Add-in Card Present	N/A

Notes:
1. USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
2. Applicable to WWAN only
3. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification*, Revision 1.1 or later, where PCIe and USB3.1 Gen1 are both present on the connector. Vendor defined choice of port configurations 0, 1, 2, 3. See Table 3-19.
4. Used by an Add-in Card where USB3.1 Gen1 is present on the connector and PCIe is No Connect. See Table 3-17. Permitted for use by an Add-in Card built to the *PCI Express M.2 Specification*, Revision 1.1 or later where PCIe and USB3.1 Gen1 are both present on the connector. See Table 3-19.
5. Only a single lane of PCIe is available in these configurations.

The four configuration pins listed in Table 5-5 need to be set to NC or GND on the Add-In Card side as listed in Table 3-12. By sensing and decoding these pins the Platform configures the pinout configuration and functionality.

5.2.1.2. Socket 2 Pinout (Mechanical Key B) On Platform

❑ Socket 2 pinouts is intended to support WWAN+GNSS, SSD, and Other types of Add-In solutions with the defined and configurable Host I/Fs.

❑ WWAN makes use of USB2.0, USB3.1 Gen1, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Add-in Card side. LED_1# and W_DISABLE1# are intended for use with the WWAN solution. There are additional WWAN and GNSS related pins including W_DISABLE2#, DPR, and WAKE_ON_WWAN#.

❑ The UIM and SIM Detect pins are used in conjunction with a SIM device in support of the WWAN solution.

❑ COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to Socket 1 COEX signals for coexistence with the Connectivity solution.

❑ The ANTCTL[0..3] pins are placeholders for future expansion and definition of these functions.

❑ The GPIO_0 to GPIO_11 pins are configurable with four different variants. These variants support the GNSS interface, second UIM/SIM, Audio interfaces, HSIC and IPC sidebands. The exact definition is determined by the configuration identified by decoding the four Configuration pins.

❑ The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into Platforms that provide a direct connection to V_{BAT} (and not a regulated 3.3 V) such as Tablet Platforms. They are not used in NB and very thin notebooks type Platforms that provide a regulated 3.3 V power rail. The FULL_CARD_POWER_OFF# signal should be tied to the 3.3 V power rail and the RESET# signal should be tied to the 1.8 V power rail on the NB/very thin Platform.

❑ The SSD makes use of the PCIe two Lanes or overlaid SATA host interface. The actual implemented I/F is identified through the CONFIG_1 pin state (1 or 0) in conjunction with the other three Configuration pin states that are all 0. DAS/DSS (overlaid on the LED_1#) and DEVSLP are intended for use with the SATA SSD solution. The SMBus interface is used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

❑ The SUSCLK pin provides a slow clock signal of 32.768 kHz to enable Low Power States.

❑ Pins labeled NC must not be connected.

Table 5-6 lists the pinouts for Socket 2 (mechanical key B).

Table 5-6. Socket 2 Pinout Diagram (Mechanical Key B) On Platform

Pin	Signal	Signal	Pin
		CONFIG_2	75
74	3.3 V/VBAT	VIO_CFG (I) or GND	73
72	3.3 V/VBAT		
70	3.3 V/VBAT	GND	71
		CONFIG_1	69
68	SUSCLK (O)(0/1.8V/3.3V)	RESET# (O)(0/1.8V)	67
66	SIM DETECT (O)		
64	COEX_RXD (I)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
		ANTCTL2 (I)(0/1.8V)	63
62	COEX_TXD (O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (I)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8V/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8V/3.3V)	GND	51
50	PERST# (O)(0/1.8V/3.3V)	PETp0/SATA-A+	49
48	GPIO_4 (I/O)(0/1.8V)	PETn0/SATA-A-	47
46	GPIO 3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 (I/O)/ALERT# (I)/(0/1.8V)	PERp0/SATA-B-	43
42	GPIO_1 (I/O)/SMB_DATA (I/O)/(0/1.8V)	PERn0/SATA-B+	41
40	GPIO_0 (I/O)/SMB_CLK (I/O)/(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1/USB3.1-Tx+/SSIC-TxP	37
36	UIM_PWR (I)	PETn1/USB3.1-Tx-/SSIC-TxN	35
34	UIM_DATA (I/O)	GND	33
32	UIM_CLK (I)	PERp1/USB3.1-Rx+/SSIC-RxP	31
30	UIM_RESET (I)	PERn1/USB3.1-Rx-/SSIC-RxN	29
28	PLA_S2# (I)/GPIO_8 (I/O) (0/1.8V)	GND	27
26	GPIO_10 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
24	GPIO_7 (I/O) (0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
22	GPIO_6 (I/O)(0/1.8V)		
20	GPIO_5 (I/O)(0/1.8V)	CONFIG_0	21
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
10	GPIO_9/DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/1.8V/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	USB_D+	7
		GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3	1

5.2.2. Socket 2 Key C

5.2.2.1. Socket 2 Pinout (Mechanical Key C) On Platform

- ❑ Socket 2 pinout is intended to support WWAN+GNSS types of add-in solutions with BTO/CTO defined Host I/Fs.

- ❑ WWAN makes use of USB 2.0, USB 3.1 Gen1, PCIe, M-PCIe, or SSIC host I/Fs. The actual implemented I/F is BTO/CTO defined between customer and vendor.

- ❑ The UIM and SIM Detect pins are used in conjunction with a SIM device in support of the WWAN solution.

- ❑ The DRP, AUDIO, COEX, and ANTCTL pins are supplemental functional pins in support of WWAN. Their functionality and pin definitions are described in Section 3.2.

- ❑ The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into Platforms that provide a direct connection to V_{BAT} (and not a regulated 3.3 V) such as tablet Platforms. They are not used in Notebook Platforms and very thin Platforms that provide a regulated 3.3 V power rail. The FULL_CARD_POWER_OFF# signal should be tied to the 3.3 V power rail and the RESET# signal should be tied to the 1.8 V power rail on the Notebook/very thin Platforms.

- ❑ The Vendor Defined pins are BTO/CTO defined between customer and vendor. See Section 6.10 for definitions.

- ❑ Pins labeled RESERVED must not be connected.

Table 5-7 lists the pinout for Socket 2 (Mechanical Key C).

Table 5-7. Socket 2 Pinout Diagram (Mechanical Key C) On Platform

Pin	Signal	Signal	Pin
74	3.3 V/VBAT	GND	75
72	3.3 V/VBAT	GND	73
		RESET# (O) (0/1.8V)	71
70	GPIO_3 (I)/ANTCTL3 (I)/RFFE_VIO (I) (0/1.8V)	COEX_RXD (I) (0/1.8V)	69
68	GPIO_2 (I)/ANTCTL2 (I)/RFFE_SCLK (I) (0/1.8V)	COEX_TXD (O) (0/1.8V)	67
66	GPIO_1 (I)/ANTCTL1 (I)/RFFE_SDATA (I/O) (0/1.8V)		
		GND	65
64	GPIO_0 (I)/ANTCTL0(I) (1.8V)	VENDOR_PORT_C_3	63
62	RESERVED	VENDOR_PORT_C_2	61
60	VENDOR_PORT_B_5	GND	59
58	VENDOR_PORT_B_4	VENDOR_PORT_C_1	57
56	RESERVED	VENDOR_PORT_C_0	55
54	VENDOR_PORT_B_3	GND	53
52	VENDOR_PORT_B_2	M/REFCLKP	51
50	VENDOR_PORT_B_1	M/REFCLKN	49
48	VENDOR_PORT_B_0	GND	47
46	PEWAKE# (I/O) (0/1.8V))	M/PETp0; SSIC-TxP; USB3.1-Tx+	45
44	CLKREQ# (I/O) (0/1.8V)	M/PETn0; SSIC-TxN; USB3.1-Tx-	43
42	PERST# (O) (0/1.8V)	GND	41
40	SIM_DETECT2 (O) (1.8V)	M/PERp0; SSIC-RxP; USB3.1-Rx+	39
38	UIM2_PWR (I)	M/PERn0; SSIC-RxN; USB3.1-Rx-	37
36	UIM2_DATA (I/O)	GND	35
34	UIM2_CLK (I)	SIM_DETECT1 (O) (0/1.8V)	33
32	UIM2_RESET (I)	UIM1_PWR (I)	31
30	AUDIO1 I2S_WS (I/O) (0/1.8V)	UIM1_DATA (I/O)	29
28	AUDIO1 I2S_RX (I) (0/1.8V)	UIM1_CLK (I)	27
26	AUDIO1 I2S_TX (O) SLIMBUS_DAT (I/O) (0/1.8V)	UIM1_RESET (I)	25
24	AUDIO1 I2S_CLK (I/O) SLIMBUS_CLK (I/O) (0/1.8V)	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
14	VENDOR_PORT_A_3	VIO 1.8 V	15
12	VENDOR_PORT_A_2	FULL_CARD_POWER_OFF# (O) (1.8V)	13
10	VENDOR_PORT_A_1	DRP (O) (1.8V)	11
8	VENDOR_PORT_A_0	GND	9
6	3.3 V	USB_D-	7
		USB_D+	5
4	3.3 V	GND	3
2	3.3 V	GND	1

5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinouts and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the Platform which I/F of these two is connected. Table 5-8 lists the Socket 3 SSD pinout.

Although the pinouts in Table 5-8 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the Adapter without sufficient power dissipation capability from the Platform. This capability is outside the scope of this specification. The intention is to further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. For higher power applications, the resistance between any two 3.3 V pins on the host and device shall be less than 15 mΩ. The maximum power consumption of this socket remains as identified in Section 3.3. This Socket also accepts SSD devices Add-in Cards that employ a Dual Module key on Module scheme. The SMBus interface available on Socket 3 may be used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

If the Platform provides USB_D+/USB_D- (pins 34 and 26), then the ground pins at pin 30 and pin 38 must be used.

Table 5-8. Socket 3 SSD Pinout (Mechanical Key M) On Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	VIO_CFG (I) or GND	73
72	3.3 V		
70	3.3 V	GND	71
		PEDET = GND (SATA), PEDET = NC (PCIe)	69
68	SUSCLK (O)(0/1.8V/3.3V)	NC	67
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
58	NC		
56	NC	GND	57
54	PEWAKE# (I/O)(0/1.8V/3.3V) or NC	REFCLKp	55
52	CLKREQ# (I/O)(0/1.8V/3.3V) or NC	REFCLKn	53
50	PERST# (O)(0/1.8V/3.3V) or NC	GND	51
48	NC	PETp0/SATA-A+	49
46	NC	PETn0/SATA-A-	47
44	ALERT# (I) (0/1.8V)	GND	45
42	SMB_DATA (I/O) (0/1.8V)	PERp0/SATA-B-	43
		PERn0/SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (O) (SATA) or GND (USB)	PETp1	37
36	USB_D- or NC	PETn1	35
34	USB_D+ or NC	GND	33
32	NC or GND (USB)	PERp1	31
30	PLA_S3# (I)(0/1.8/3.3V) or NC	PERn1	29
28	NC		
26	NC	GND	27
24	NC	PETp2	25
22	VIO 1.8 V or NC	PETn2	23
20	NC	GND	21
18	3.3 V	PERp2	19
16	3.3 V	PERn2	17
14	3.3 V	GND	15
		PETp3	13
12	3.3 V	PETn3	11
10	DAS/DSS (I/O)/LED_1# (I)(0/3.3V)	GND	9
8	PLN# (O)(0/1.8/3.3V) or NC		
6	PWRDIS (O)(0/1.8/3.3V) or NC	PERp3	7
4	3.3 V	PERn3	5
2	3.3 V	GND	3
		GND	1

5.4.　　Soldered Down Pinouts Definitions

The soldered-down pinouts definitions are shown in the following figures:

- ❑ Figure 5-1.　Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform
- ❑ Figure 5-2.　Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform
- ❑ Figure 5-3.　Type 3026 LGA Pinout Using SDIO Based Socket 1 and DisplayPort Based Socket 1 Pinout on Platform
- ❑ Figure 5-4.　Type 1620 BGA Pinout on Platform (Top View)
- ❑ Figure 5-5.　Type 1620 BGA Module-side Pinout Surrounded by Type 2024, Type 2228, and Type 2828 Platform-side Pinout (Top View)
- ❑ Figure 5-6.　Type 1113 BGA Socket Map on Platform (Top View)

Top View — Platform Side Pinout

Top edge (pins 92–70): GND (G1), UIM_SWP (91), UIM_POWER_SNK (90), UIM_POWER_SRC/GPIO_1 (89), GND (88–72), VIO_CFG (71), GND (70), GND (G4)

Left column (pins 1–23):

Pin	Signal
1	3.3 V
2	3.3 V
3	GND
4	RESERVED
5	ALERT#
6	I2C_CLK
7	I2C_DATA
8	COEX_TXD
9	COEX_RXD
10	COEX3
11	SYSCLK / GNSS_0
12	TX_BLANKING / GNSS_1
13	RESERVED
14	GND
15	RESERVED
16	RESERVED
17	GND
18	RESERVED
19	RESERVED
20	GND
21	RESERVED
22	RESERVED
23	GND

Right column (pins 69–47):

Pin	Signal
69	3.3 V
68	3.3 V
67	GND
66	USB_D+
65	USB_D-
64	GND
63	VIO_1.8V
62	LED_1#
61	LED_2#
60	W_DISABLE2#
59	GND
58	PCM_CLK
57	PCM_IN
56	PCM_OUT
55	PCM_SYNC
54	UART_CTS
53	UART_TXD
52	UART_RXD
51	UART_RTS
50	UART_WAKE#
49	SDIO_CLK
48	SDIO_CMD
47	SDIO_DATA0

Bottom edge (pins 24–46):

Pin	Signal
24	SUSCLK(32kHz)
25	W_DISABLE1#
26	PEWAKE0#
27	CLKREQ0#
28	PERST0#
29	GND
30	REFCLKn0
31	REFCLKp0
32	GND
33	PERn0
34	PERp0
35	GND
36	PETn0
37	PETp0
38	GND
39	VENDOR DEFINED
40	VENDOR DEFINED
41	VENDOR DEFINED
42	SDIO_RESET#
43	SDIO_WAKE#
44	SDIO_DATA3
45	SDIO_DATA2
46	SDIO_DATA1

Ground zones: GND (G1), GND (G2), GND (G3), GND (G4)

Figure 5-1.　Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform

Figure 5-2.   Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout on Platform

Top View

GND

Platform Side Pinout

Pin	Signal		Pin	Signal
93	3.3 V	1	3.3 V	
94	3.3 V	2	3.3 V	
95	GND	3	GND	
96	RESERVED	4	RESERVED	
97	RESERVED	5	ALERT#	
98	RESERVED	6	I2C_CLK	
99	RESERVED	7	I2C_DATA	
100	RESERVED	8	COEX_RXD	
101	RESERVED	9	COEX_TXD	
102	GND	10	COEX3	
103	PEWAKE1#	11	SYSCLK / GNSS0	
104	CLKREQ1#	12	TX_BLANKING / GNSS1	
105	PERST1#	13	RESERVED	
106	GND	14	GND	
107	REFCLKn1	15	RESERVED	
108	REFCLKp1	16	RESERVED	
109	GND	17	GND	
110	PERn1	18	RESERVED	
111	PERp1	19	RESERVED	
112	GND	20	GND	
113	PETn1	21	RESERVED	
114	PETp1	22	RESERVED	
115	GND	23	GND	

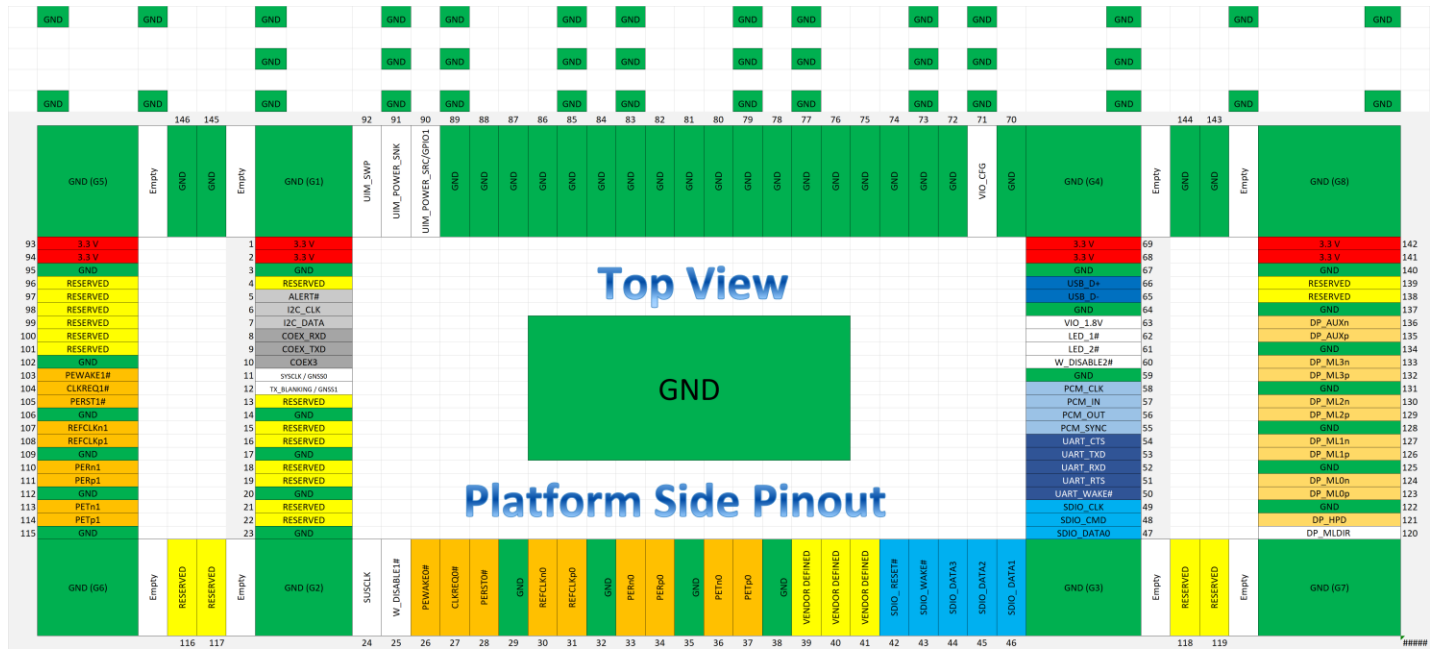| Pin	Signal	Pin	Signal
69	3.3 V	142	3.3 V
68	3.3 V	141	3.3 V
67	GND	140	GND
66	USB_D+	139	RESERVED
65	USB_D-	138	RESERVED
64	GND	137	GND
63	VIO_1.8V	136	DP_AUXn
62	LED_1#	135	DP_AUXp
61	LED_2#	134	GND
60	W_DISABLE2#	133	DP_ML3n
59	GND	132	DP_ML3p
58	PCM_CLK	131	GND
57	PCM_IN	130	DP_ML2n
56	PCM_OUT	129	DP_ML2p
55	PCM_SYNC	128	GND
54	UART_CTS	127	DP_ML1n
53	UART_TXD	126	DP_ML1p
52	UART_RXD	125	GND
51	UART_RTS	124	DP_ML0n
50	UART_WAKE#	123	DP_ML0p
49	SDIO_CLK	122	GND
48	SDIO_CMD	121	DP_HPD
47	SDIO_DATA0	120	DP_MLDIR

Figure 5-3. Type 3026 LGA Pinout Using SDIO Based Socket 1 and DisplayPort Based Socket 1 Pinout on Platform

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	PWR_1	PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	PWR_1	PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+/PETp0	SATA-A-/PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B-/PERn0		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1#/DAS	RFU	PWR_1	PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	PWR_1	PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

☐ = No Solder Ball

Figure 5-4.   Type 1620 BGA Pinout on Platform (Top View)
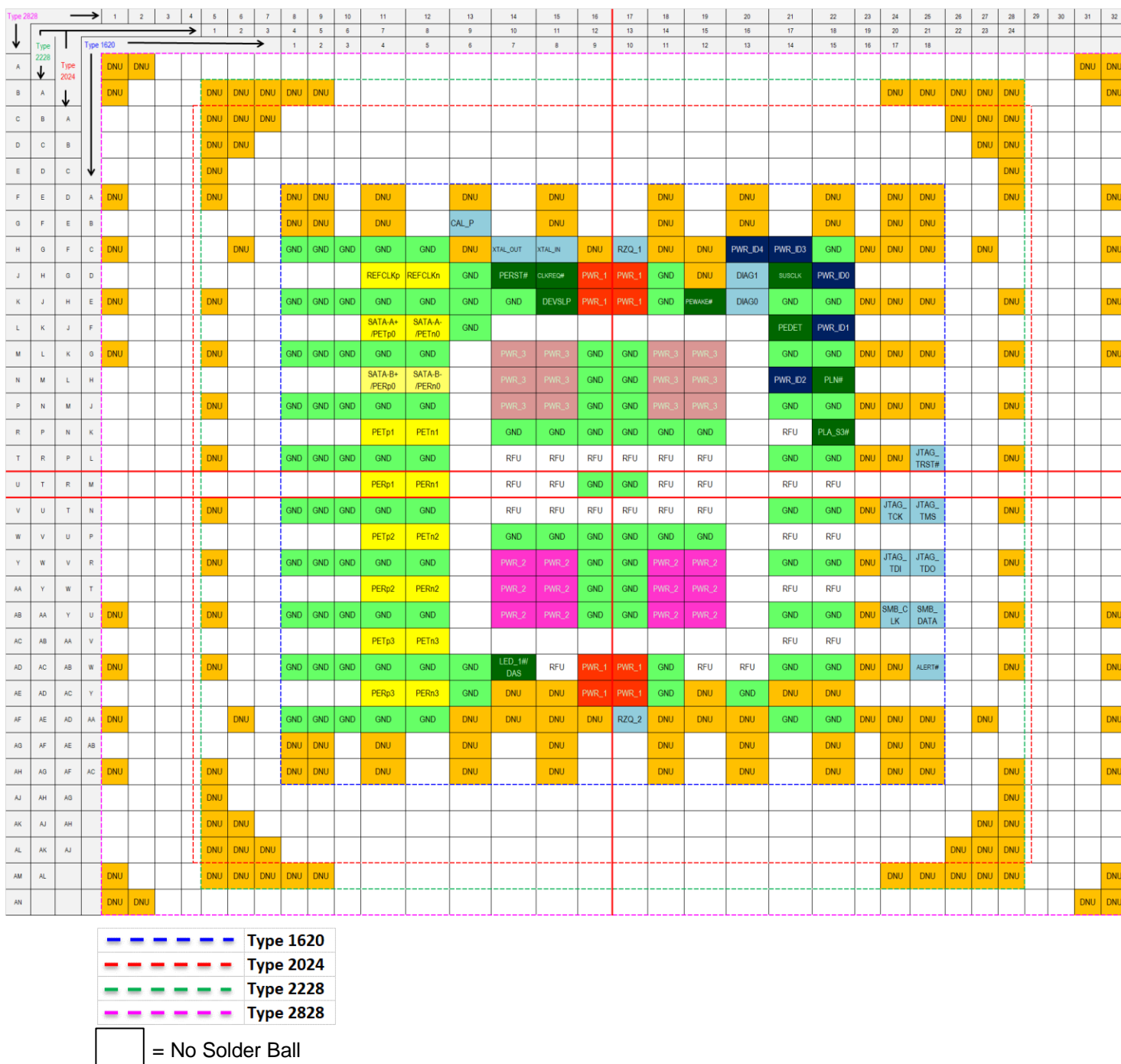
Figure 5-5. Type 1620 BGA Module-side Pinout Surrounded by Type 2024, Type 2228, and Type 2828 Platform-side Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP#	SPI_CLK	SPI_CS#	GND	GND
C	GND	GND	GND	DNU	DNU	V_ID0	V_ID2	V_ID4	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	V_ID1	VID3	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		RFU	CAL_P	XTAL_OUT	XTAL_IN
Y	GND	LED_1#	GND	GND	GND	GND	PERp0	PERn0	GND	PETp0	PETn0	GND	PERp1	PERn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND	PETp0	PETn0	GND	PERp0	PERn0	GND	PETp1	PETn1	GND	PETp1	PETn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND	PERp1	PERn1	GND	GND	GND+W10: W25

☐ = No Solder ball

Figure 5-6.   Type 1113 BGA Socket Map on Platform (Top View)

6

6. Annex

6.1.   Glossary

A	Amperage or Amp	**NB**	Notebook
BGA	Ball Grid Array	**NIC**	Network Interface Card
BIOS	Basic Input Output System	**NC**	Not Connected
BT	Bluetooth	**OD**	Open Drain
BTO	Build-to-Order	**OEM**	Original Equipment Manufacturer
CEM	Card Electromechanical	**OS**	Operating System
CTO	Configure To Order	**PCI Express**	Peripheral Component Interconnect Express
DC	Direct Current	**SATA**	Serial Advanced Technology Attachment or Serial ATA
DNU	Do Not Use	**PCM**	Pulse Code Modulation
DPR	Dynamic Power Reduction	**RF**	Radio Frequency
GND	Ground	**RFU**	Reserved for Future Use
GNSS	Global Navigation Satellite System (GPS+GLONASS)	**RMS**	Root Mean Square
HDR	Hybrid Digital Radio	**RoHS**	Restriction of Hazardous Substances Directive
HSIC	High Speed Inter-Chip	**RSS**	Root Sum Square
I/F	Interface	**RTC**	Real Time Clock
I/O (O/I)	Input/Output (Output/Input)	**SDIO**	Secure Digital Input Output
IR	Current x Resistance = Voltage	**SIM**	Subscriber Identity Module
I²C	Inter-Integrated Circuit	**SSD**	Sold-State Drive
I2S	Integrated Interchip Sound	**SSIC**	Super Speed USB Inter-Chip
LED	Light Emitting Diode	**RF**	Radio Frequency
LGA	Land Grid Array	**USB**	Universal Serial Bus
M-PCIe	PCIe over MIPI Alliance M-PHY	**UART**	Universal Asynchronous Receive Transmit
mm	millimeter	**V**	Voltage
mΩ	milliohm	**W**	Wattage or Watts
mA	milliamp	**WiGig**	60 GHz multi-gigabit speed wireless communication
mV	millivolt	**WLAN**	Wireless Local Area Network
NFC	Near Field Communications	**WPAN**	Wireless Personal Area Network
M.2	Formerly called Next Generation Form Factor (NGFF)	**WWAN**	Wireless Wide Area Network

6.2. M.2 Signal Directions

This section describes the directionality of some of the interface signals incorporated in the various pinouts. Since some signals have directionality associated with them, their names and locations may be different between the Platform side and the Adapter side.

The Adapter pinouts are described in Chapter 3 and Platform pinouts are described in Chapter 5, *Platform Socket Pinout and Key Definitions*.

The main differences between Platform-side pinouts and Add-in Card-side pinouts are shown in Figure 6-1 and Figure 6-2.
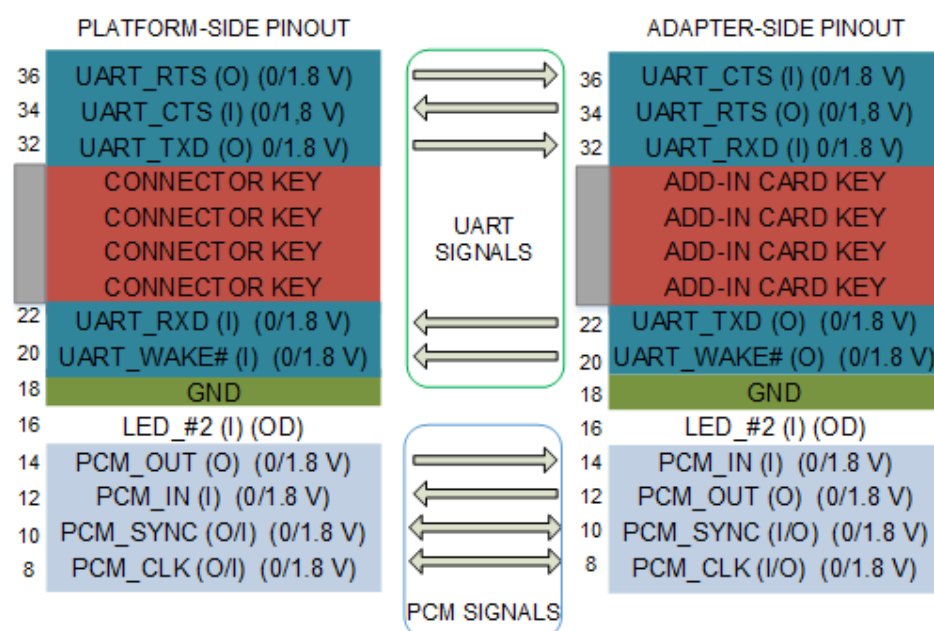
Figure 6-1.   UART and PCM Signal Direction and Signal Name Changes
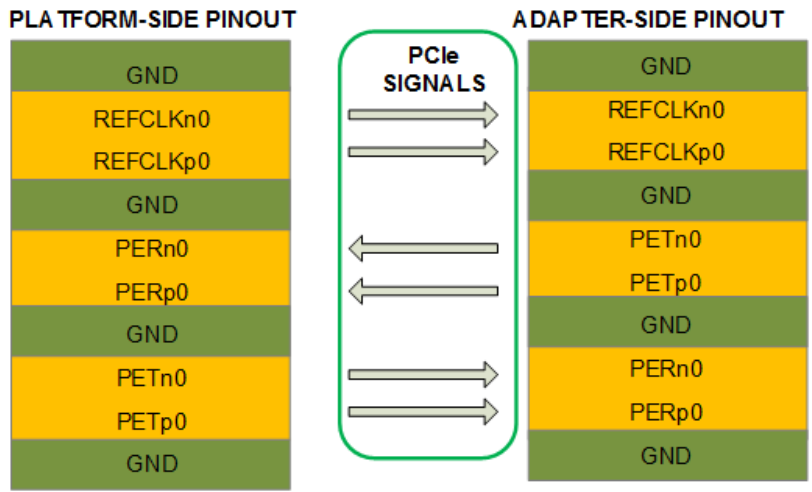
Figure 6-2. PCIe Signal Direction and Signal Name Changes

PCIe Pin order shown in Figure 6-2 coincides with Socket 1 pinouts. Alternate PCIe pin order exists in Socket 2 and 3.

Figure 6-1 and Figure 6-2 are examples of signaling directions and name changes from Platform to Adapter. The example shown in Figure 6-2 uses default lane polarity. Other cases exist for other signals in various Sockets, such as the USB3.1 Tx and Rx, SSIC Tx and Rx.

The first two COEX signals between the WWAN device on Socket 2 and the Connectivity device on Socket 1 have defined directions. At the Platform, the three COEX signals should be connected pin-to-pin as shown in Figure 6-3.
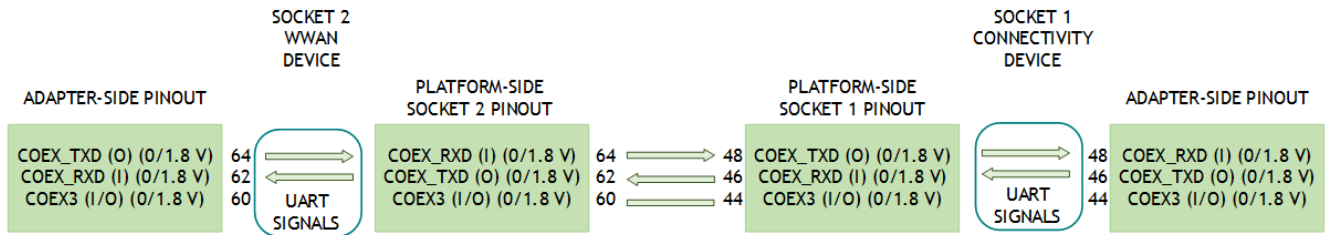
Figure 6-3. COEX_TXD and COEX_RXD Signal Direction

6.3. Signal Integrity Requirements 8.0 GT/s

Table 6-1 follows the 8.0 GT/s requirements in the *PCI Express Card Electromechanical Specification*. The measurement includes connector solder pads of main board and gold finger pads of the Add-in Card.

It is recommended to use an electrical test fixture for evaluating connector signal integrity.

Table 6-1. Signal Integrity Parameters and Test Procedures for M.2 Connectors

Parameter	Procedure	Recommendations
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5) + 0.5] dB for 2.5 GHz < f ≤ 5 GHz (e.g., ≥ -2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5) + 2.5] dB for 5 GHz < f ≤ 12 GHz (e.g., ≥ -10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≤ -15 dB up to 3 GHz; ≤ 5*f – 30 dB for 3 GHz < f ≤ 5 GHz; ≤ -1 dB for 5 GHz < f ≤ 12 GHz
Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. • This is a differential crosstalk between a victim differential signal pair and all adjacent differential signal pairs. The measured differential S-parameter shall be referenced to 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5 GHz; ≤ -20 dB for 5 GHz < f ≤ 10 GHz < -10 dB for 10 GHz < f ≤ 12 GHz

Note 1: The specified S-parameters recommendations are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

6.3.1.   Test Fixture Recommendations

The test fixture for connector S-parameter measurement shall be designed and built to the following recommendations:

❑ The test fixture shall be an FR4-based PCB of the microstrip structure where the dielectric thickness of this structure shall be approximately 0.102 mm (4 mils).

❑ The total thickness of the test fixture PCB shall be 0.8 mm (31.5 mils) and the test Add-in Card should be a break-out card fabricated in the same PCB panel for the fixture.

❑ The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1,800 mils). The trace lengths between the connector and measurement port on the test baseboard and test Add-in Card shall be equal. Note that the gold finger pad is not counted as the trace of the Add-in Card; it is considered as a part of the connector interface.

❑ All of the traces on the test main board and test Add-in Card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7%, and they should be uncoupled.

❑ Use of SMA connectors as measurement ports is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 30 ps rise time is recommended to be within 50 Ω ±7 Ω

Figure 6-4, Figure 6-5, and Figure 6-6 show the recommended pad and anti-pad guideline for Signal Integrity modeling.
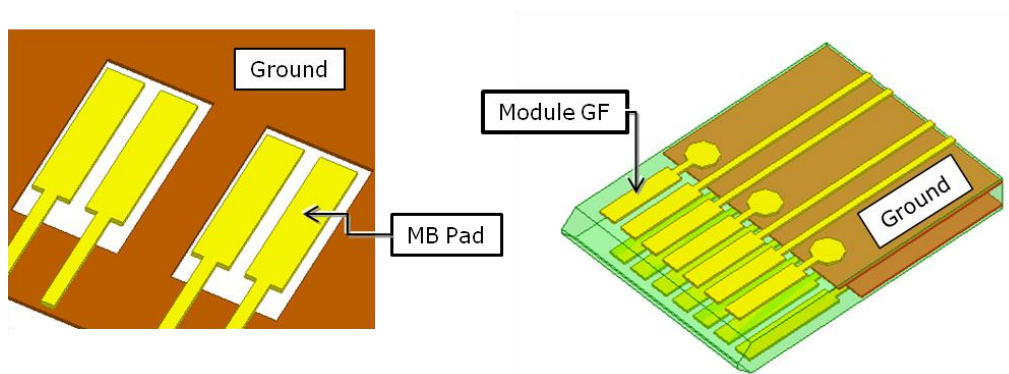

Figure 6-4.   Suggested Motherboard and Add-in Card Signals and Ground Pad Layout Guideline
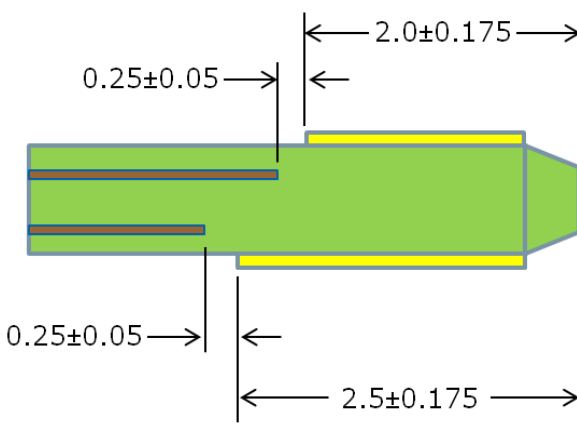
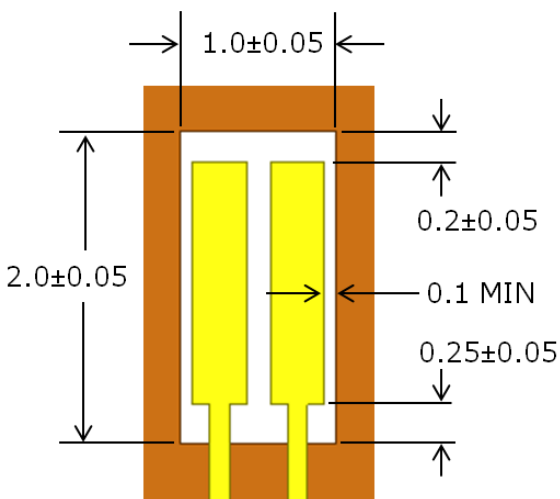Figure 6-5.   Suggested Ground Void for Add-in Card Simulation

Figure 6-6.   Suggest Ground Void for Main Board

6.3.2.   Suggested Top Mount Signal Integrity PCB Layout

Suggested PCB layouts for the test Add-in Card and test baseboard side used to test the M.2 Top Mount Connector are given in Figure 6-7 and Figure 6-8.
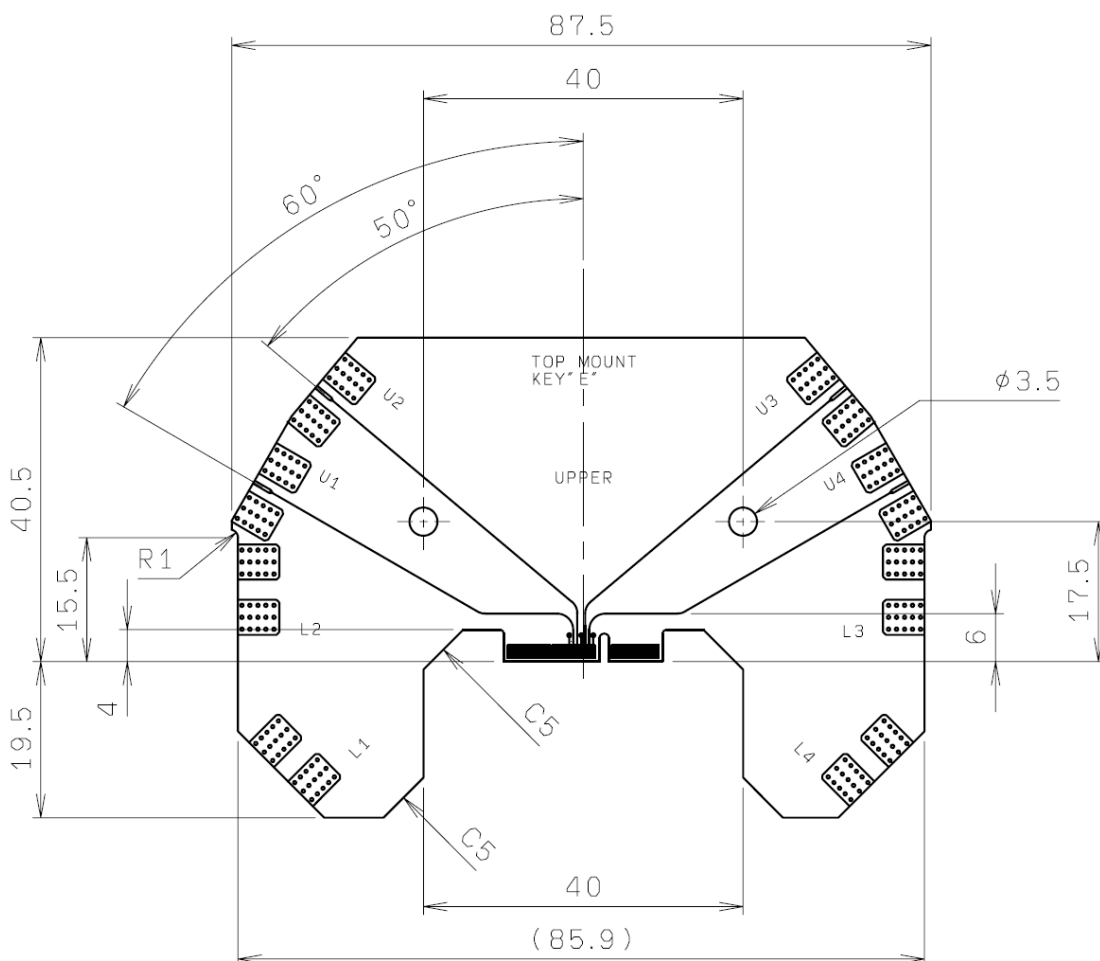
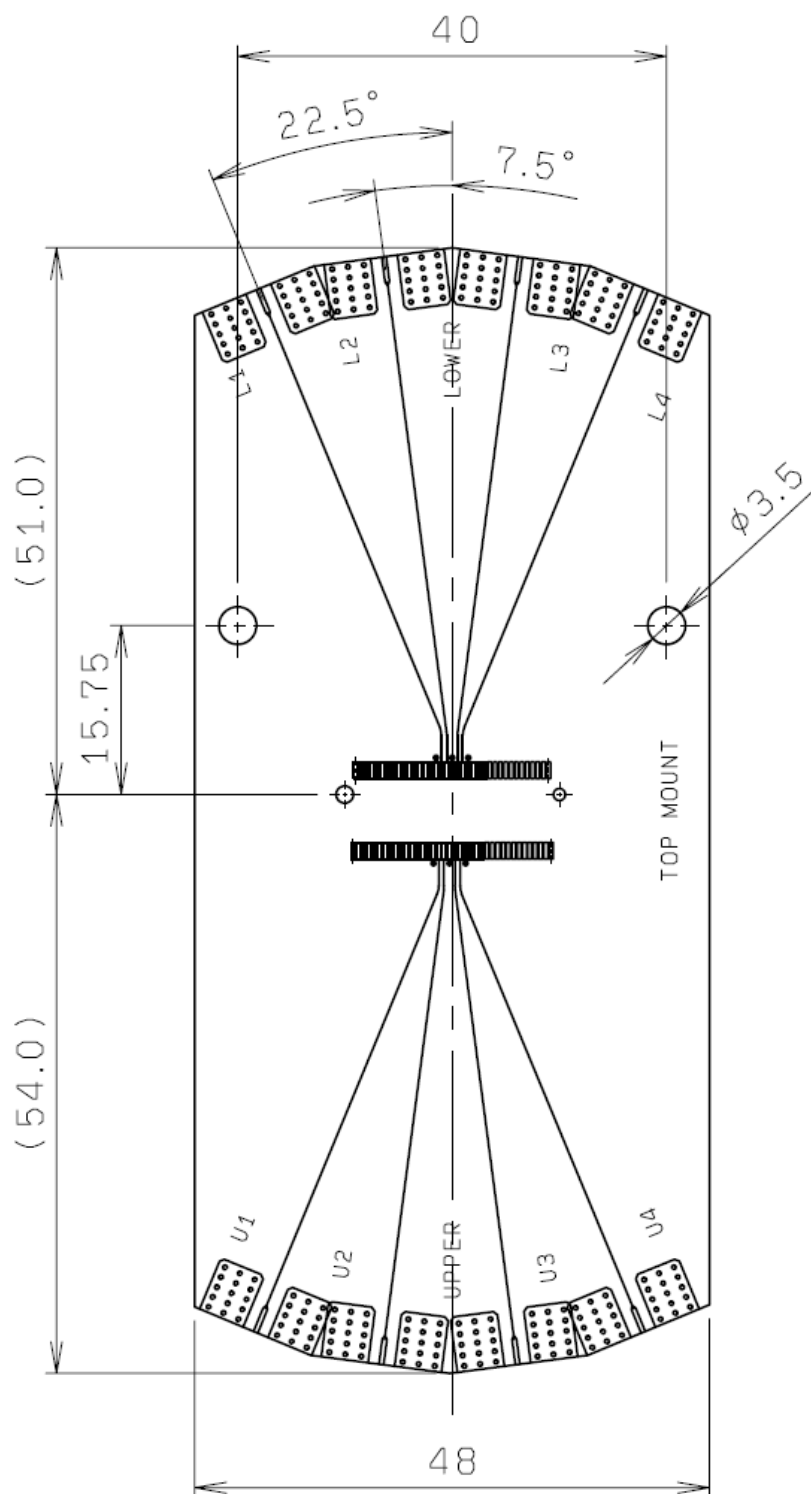Figure 6-7.　Top Mount Add-in Card Test Fixture PCB Layout

Figure 6-8.   Top Mount Motherboard Test Fixture PCB

6.3.3. Suggested Mid-mount Signal Integrity PCB Layout

Suggested PCB layouts for the test Add-in Card and test baseboard side used to test the M.2 Mid-mount Connector are shown in the following figure:

❑ Figure 6-9. Top Mount Connector Test Fixture

❑ Figure 6-10. Mid-mount Connector Test Fixture

❑ Figure 6-11. Mid-mount Add-in Card Test Fixture PCB Layout

❑ Figure 6-12. Mid-mount Motherboard Test Fixture PCB

❑ Figure 6-13. Detail of Top-side SMA End Launch Connector Pad

❑ Figure 6-14. Ground Void on Backside

❑ Figure 6-15. Detail of Mid-mount Vias on Top-side Motherboard

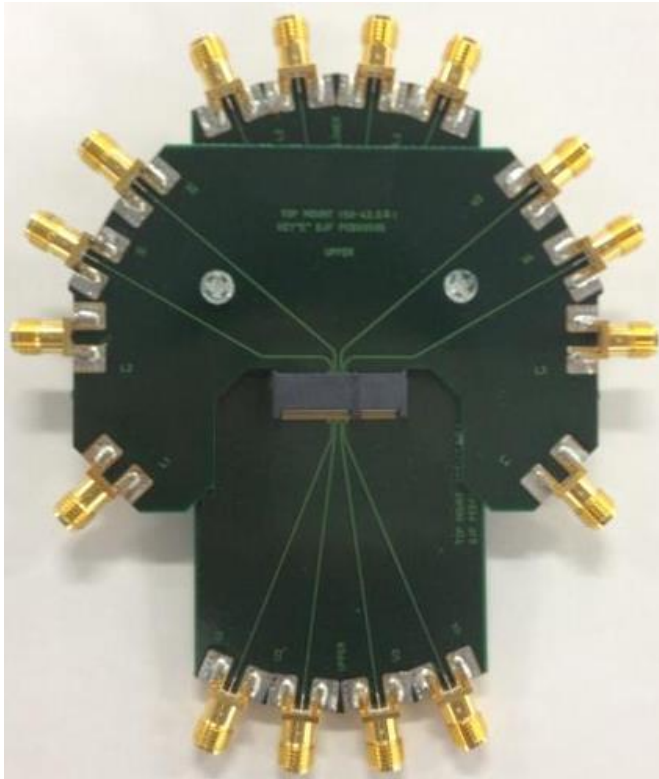❑ Figure 6-16. Detail of Ground Void on Mid-mount Bottom Side Motherboard

Figure 6-9.   Top Mount Connector Test Fixture
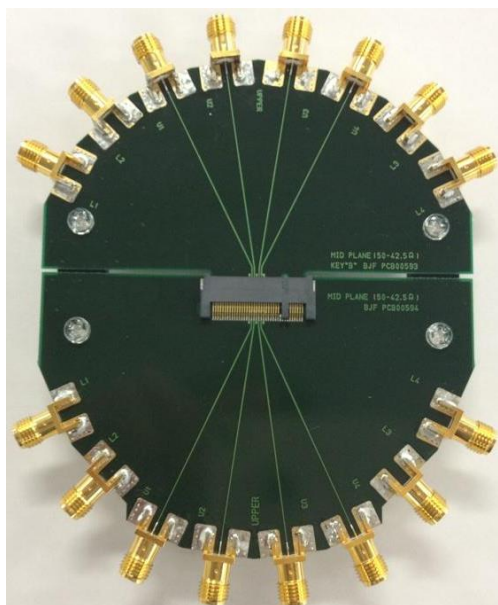
Figure 6-10. Mid-mount Connector Test Fixture

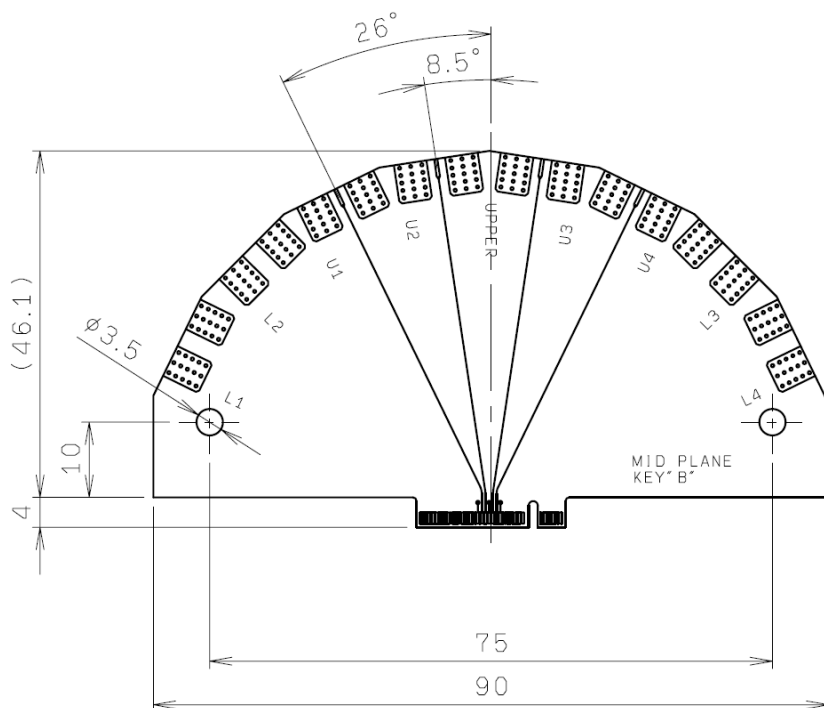PCB stack-up and Trace Impedance should be designed for 85 Ω MSL

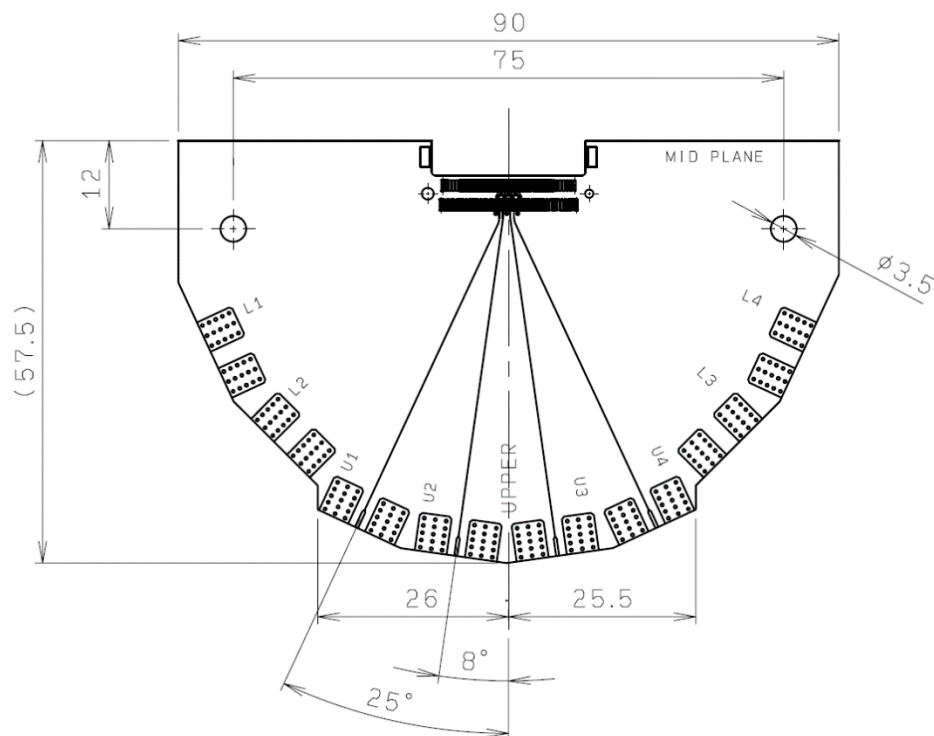## Figure 6-11. Mid-mount Add-in Card Test Fixture PCB Layout
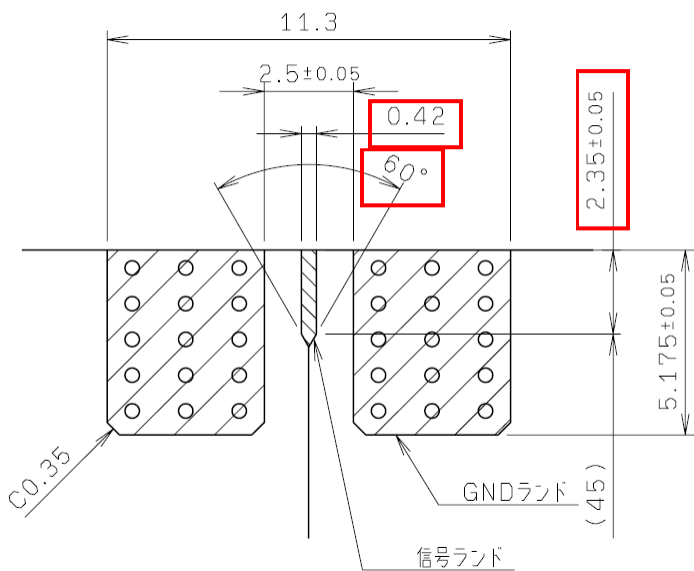
Figure 6-12. Mid-mount Motherboard Test Fixture PCB

Figure 6-13. Detail of Top-side SMA End Launch Connector Pad
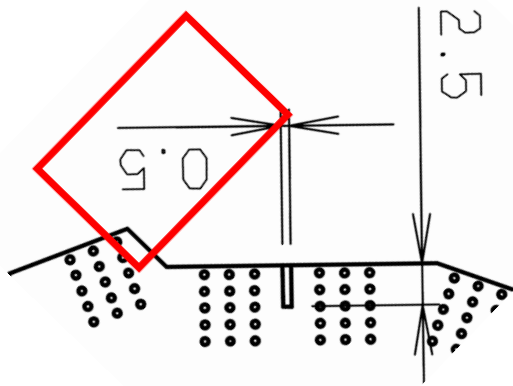
SMA pad designed for 42.5 Ω
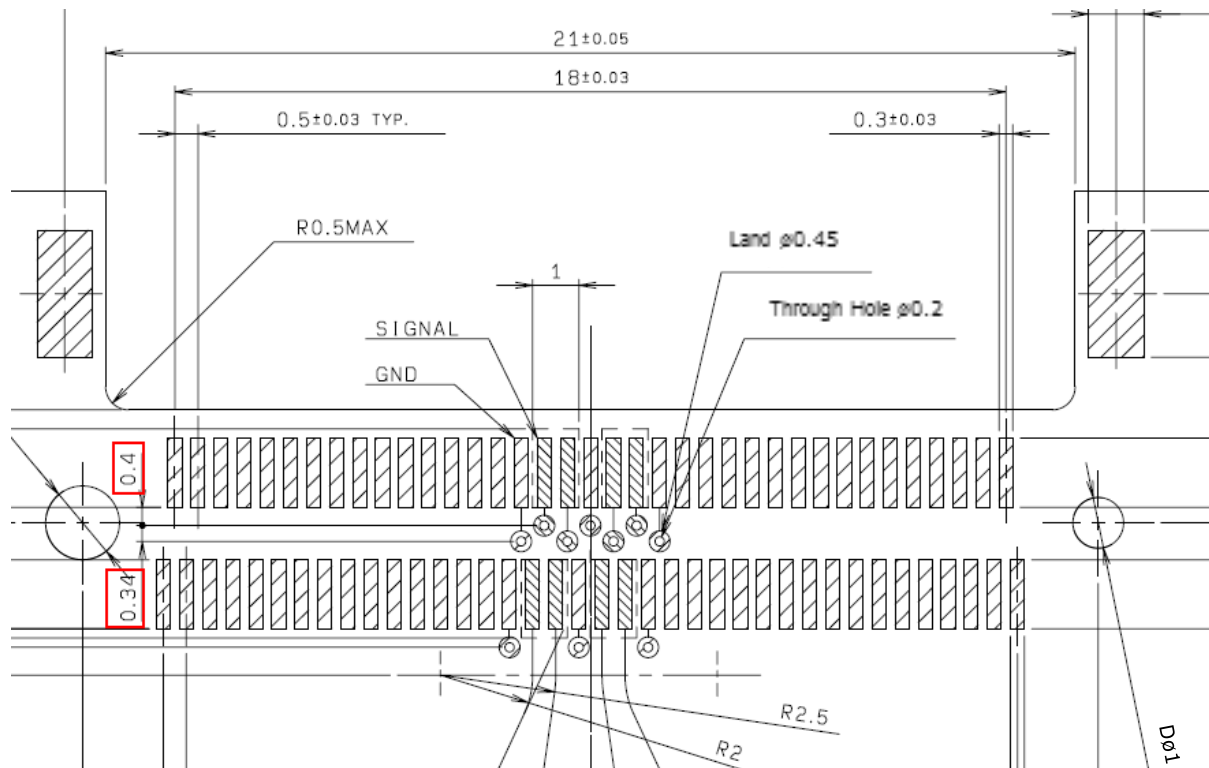

Figure 6-14. Ground Void on Backside

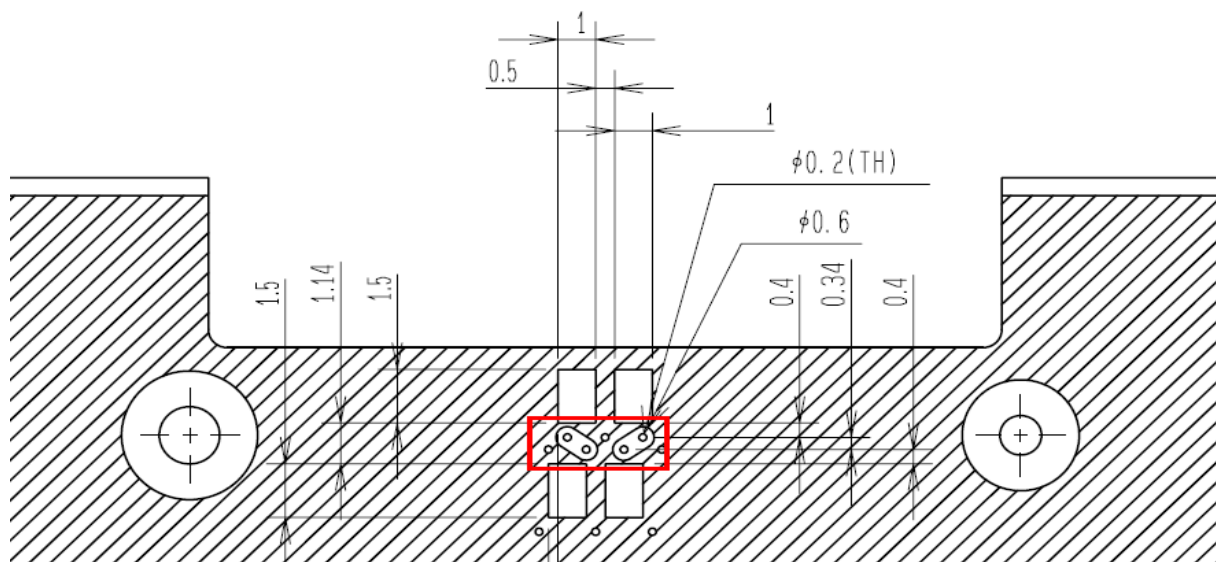Figure 6-15. Detail of Mid-mount Vias on Top-side Motherboard

Figure 6-16. Detail of Ground Void on Mid-mount Bottom Side
Motherboard

6.4.　　Signal Integrity Requirements 16.0 GT/s

Table 6-2 follows the 16.0 GT/s requirements in the *PCI Express Card Electromechanical Specification*. The measurement includes connector solder pads of main board and gold finger pads of the Add-in Card.

It is recommended to use an electrical test fixture for evaluating connector signal integrity.

Table 6-2.　　Signal Integrity Parameters and Test Procedures for 16.0 GT/s M.2 Connectors

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture requirements defined in Section 6.6.2. • The test fixture effect shall be removed from the measured S-parameters. See Note 1. See Figure 6-17 for the 16.0 GT/s differential Insertion Loss requirements.	≥ -0.5 dB up to 4 GHz; ≥ -[0.25*f + 0.5] dB for 4 GHz < f < 8 GHz (e.g., -1.5 dB at 8 GHz); ≥ -[0.75*f+4.5] dB for 8 GHz < f < 10 GHz (e.g., -3.0 dB at 10 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture requirements defined in Section 6.6.2. • The test fixture effect shall be removed from the measured S-parameters. See Note 1. See Figure 6-18 for 16.0 GT/s differential Return Loss requirements.	≤ -15 dB up to 3 GHz; ≤ [5*f – 30] dB for 3 GHz < f < 4.4 GHz (e.g., -10 dB at 4 GHz) ≤ -8 dB from 4.4 GHz to 10 GHz
Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max

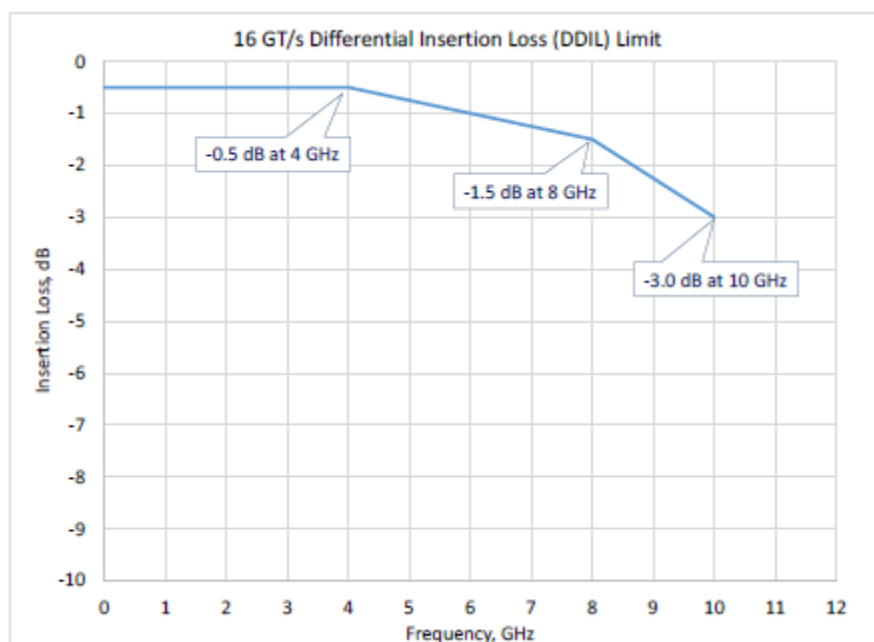| Parameter	Procedure	Requirements
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • See Section 6.6.1 for Victim-Aggressor pair arrangement to be used for connector NEXT measurement for various sockets. • See Section 6.6.1 for Victim-Aggressor pair arrangement to be used for connector FEXT measurement for various sockets. • This is a differential power sum crosstalk between a victim differential signal pair and indicated differential signal pairs aggressors. The measured differential S-parameter shall be referenced to 85 Ω differential impedance.	≤ -32 dB up to 8 GHz and -20 dB up to 8 GHz to 10 GHz
Note 1: The specified S-parameters recommendations are for connector only, not including the test fixture effect. It is recommended to use 2x Thru de-embedding method. Other methods for calibration and fixture removal are allowed.		

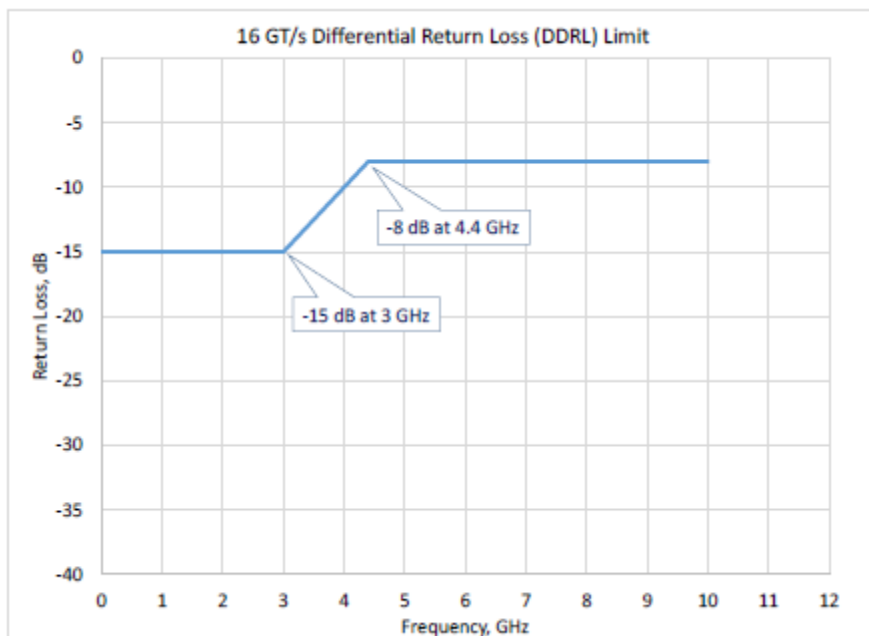Figure 6-17. Differential Insertion Loss Limits for 16.0 GT/s Operation

Figure 6-18. Differential Return Loss Limits for 16.0 GT/s Operation
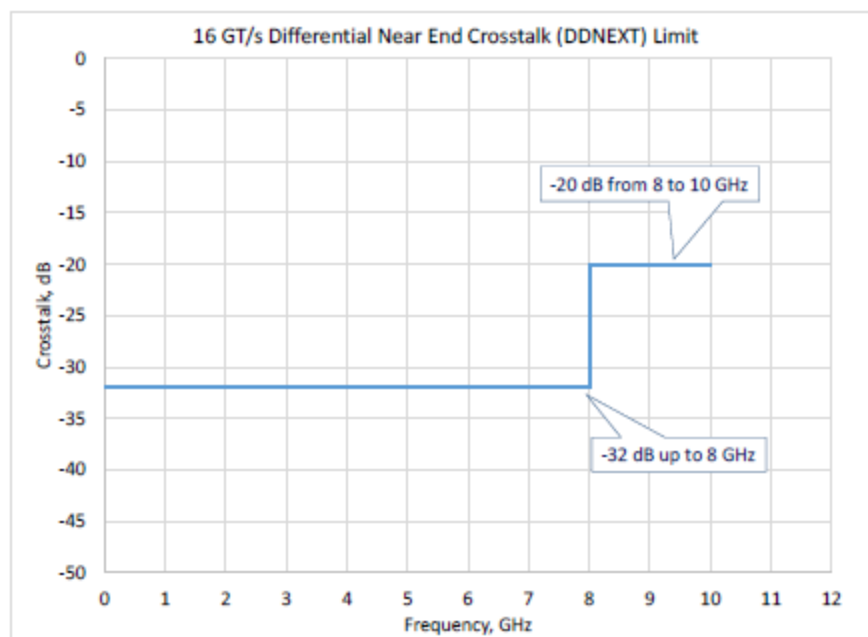

Figure 6-19. Differential Near End and Far End Crosstalk Limits for 16.0 GT/s Operation

6.5. Signal Integrity Requirements for 32.0 GT/s

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects are de-embedded from measurements. Test fixture requirements and recommendations are provided in Section 6.3.1. Table 6-3 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-3. Signal Integrity Requirements and Test Procedures for 32.0 GT/s M.2 Connectors

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture requirements defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1. • See Figure 6-20 for the 32.0 GT/s differential Insertion Loss requirements.	[-0.034375*Freq (GHz) – 0.2] for Freq ≤ 16 [-0.15625*Freq (GHz) + 1.75] for 16 < Freq ≤ 24
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture requirements defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1. • See Figure 6-21 for the 32.0 GT/s differential Return Loss requirements.	[0.625*Freq (GHz) – 20] for Freq ≤ 16 GHz [0.875*Freq (GHz) – 24] for 16 < Freq ≤ 24 GHz
Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on M.2 Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard shall be used with the following considerations: • The Near End Crosstalk is the power sum crosstalk with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as shown in Figure 6-22. • This is a differential crosstalk between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	[0.3125*Freq (GHz) – 45] for Freq ≤ 16 [0.625*Freq (GHz) – 50] for 16 < Freq ≤ 24 $ccICN_{NEXT}$ ≤ 1200 µV for fmax = 24 GHz

Parameter	Procedure	Requirements
	• If this frequency based DDNEXT requirement is not met, ccICN$_{NEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 6-1 and must be less than the value indicated under the requirements column. A connector that meets the ccICN$_{NEXT}$ requirement is considered compliant to the DDNEXT specification.	
Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard shall be used with the following considerations: • The Far End Crosstalk is the power sum crosstalk with respect to all pins 2-pairs away from opposite sides of the connector channel, as shown in Figure 6-23. • This is a differential crosstalk between a victim differential signal pair and all the differential signal pins two pairs away. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. •If this frequency based DDFEXT requirement is not met, ccICN$_{FEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 6-2 and must be less than the value indicated under the requirements column. A connector that meets the ccICN$_{FEXT}$ requirement is considered compliant to the DDFEXT specification.	[0.833*Freq (GHz) - 60] for Freq ≤ 24 ccICN$_{FEXT}$ ≤ 60 µV for $f$max = 24 GHz

Note 1: The specified S-parameter requirements are for connector only, not including the test fixture effect. It is recommended to use 2x Thru de-embedding method. Other methods for calibration and fixture removal are allowed.

Equation 6-1. Component Contribute Integrated Crosstalk Noise – ccICN$_{NEXT}$

$$ccICN_{NEXT} = \sqrt{\frac{1}{2}df \sum_{k=1}^{N_{max}} (\frac{A_{NT}^2}{f_b})sinc^2(k \cdot df/f_b)10^{(2\frac{IL_{post-channel}(k)}{10})}\left[\frac{1}{1+(\frac{k \cdot df}{f_t})^4}\right]\left[\frac{1}{1+(\frac{k \cdot df}{f_r})^8}\right]10^{\frac{MDNEXT(k)}{10}}}$$

Equation 6-2. Component Contribute Integrated Crosstalk Noise – ccICN$_{FEXT}$

$$ccICN_{FEXT} = \sqrt{\frac{1}{2}df \sum_{k=1}^{N_{max}} (\frac{A_{FT}^2}{f_b})sinc^2(k \cdot df/f_b)10^{(\frac{IL_{pre-channel}(k)}{10}+\frac{IL_{post-channel}(k)}{10})}\left[\frac{1}{1+(\frac{k \cdot df}{f_t})^4}\right]\left[\frac{1}{1+(\frac{k \cdot df}{f_r})^8}\right]10^{\frac{MDFEXT(k)}{10}}}$$

❑ $IL_{pre-channel}(k) = -(\frac{27.75}{f_{b/2}}) k. df$, $IL_{post-channel}(k) = -(\frac{7.5}{f_{b/2}}) k. df$

❑ f_{max} = 24 GHz, f_{min}=10 MHz, df = 10 MHz, f_b = 32 GHz

- A_{FT} = 800 mVpp, A_{NT} = 800 mVpp
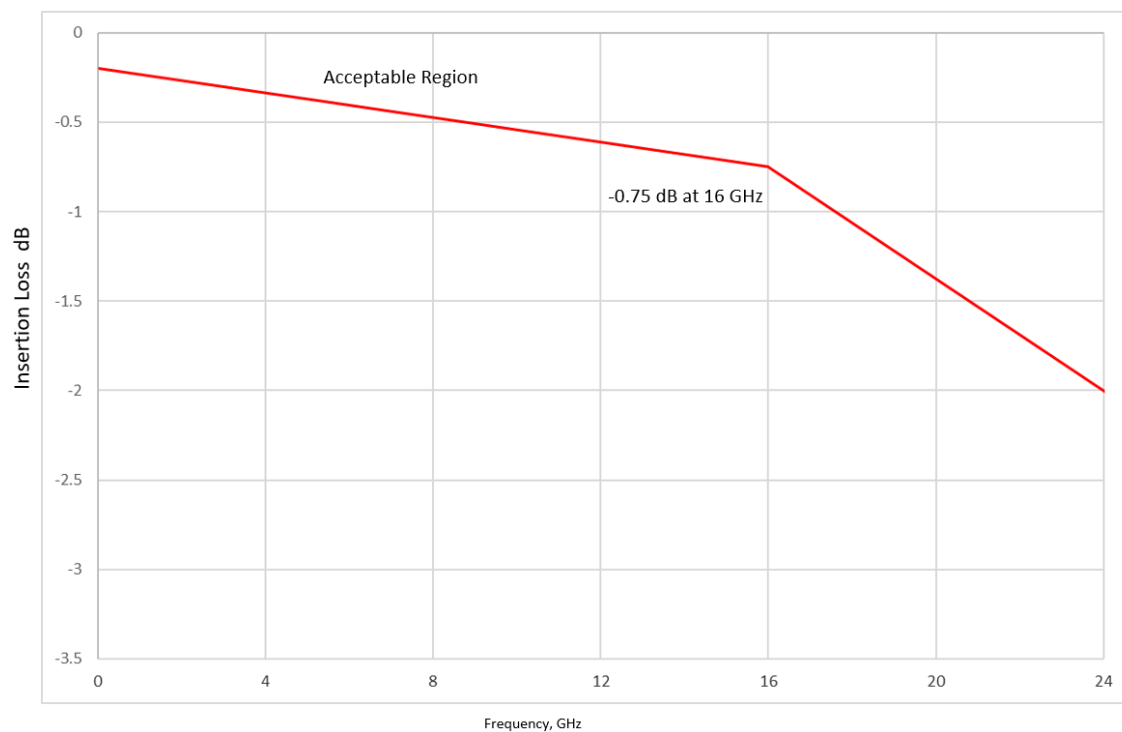- f_t = 31.53 GHz, f_r = 24 GHz

Figure 6-20. Differential Insertion Loss Limits for 32.0 GT/s Operation
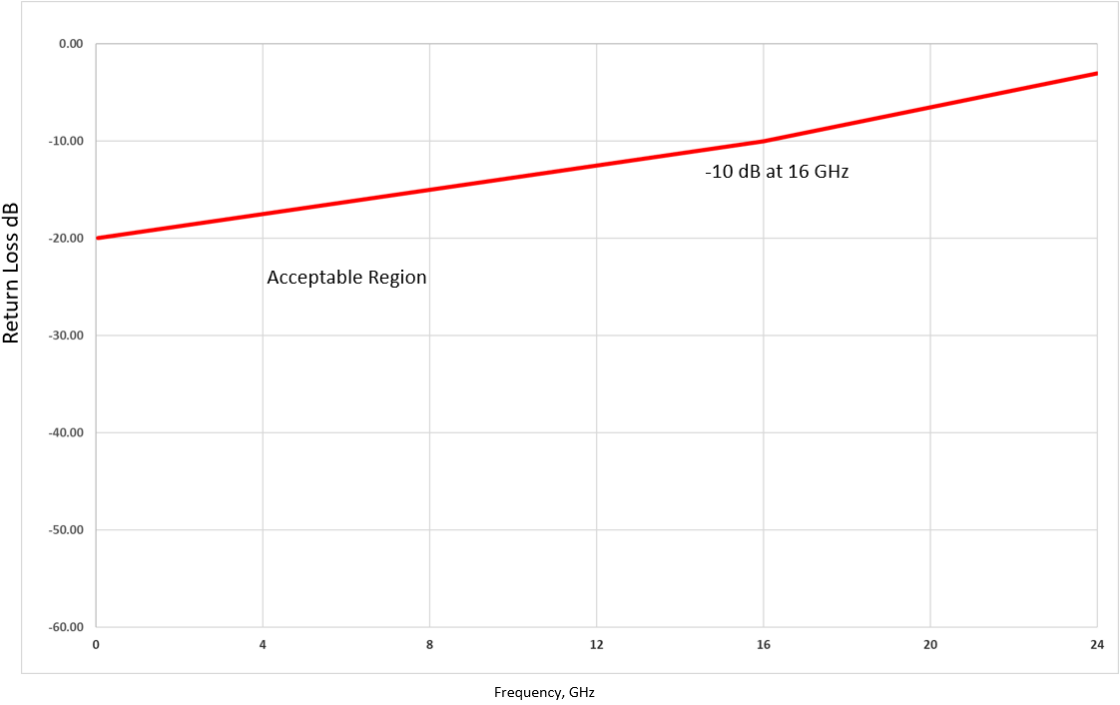
Figure 6-21. Differential Return Loss Limits for 32.0 GT/s Operation
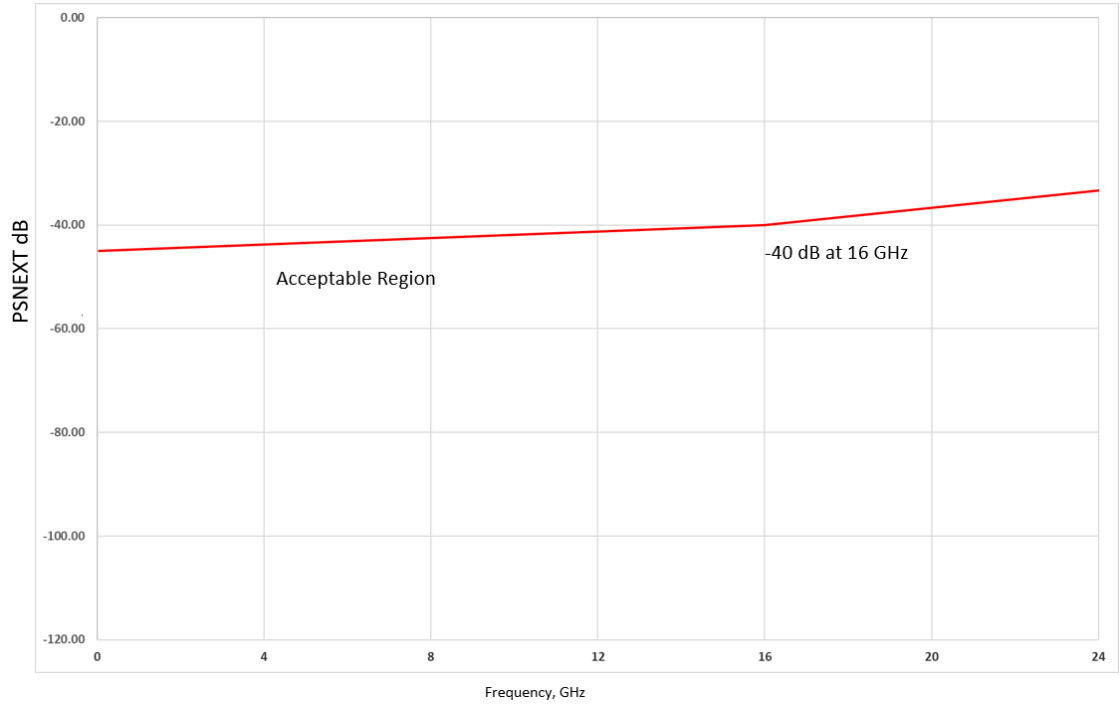
Figure 6-22. Differential Near End Crosstalk Limits for 32.0 GT/s Operation
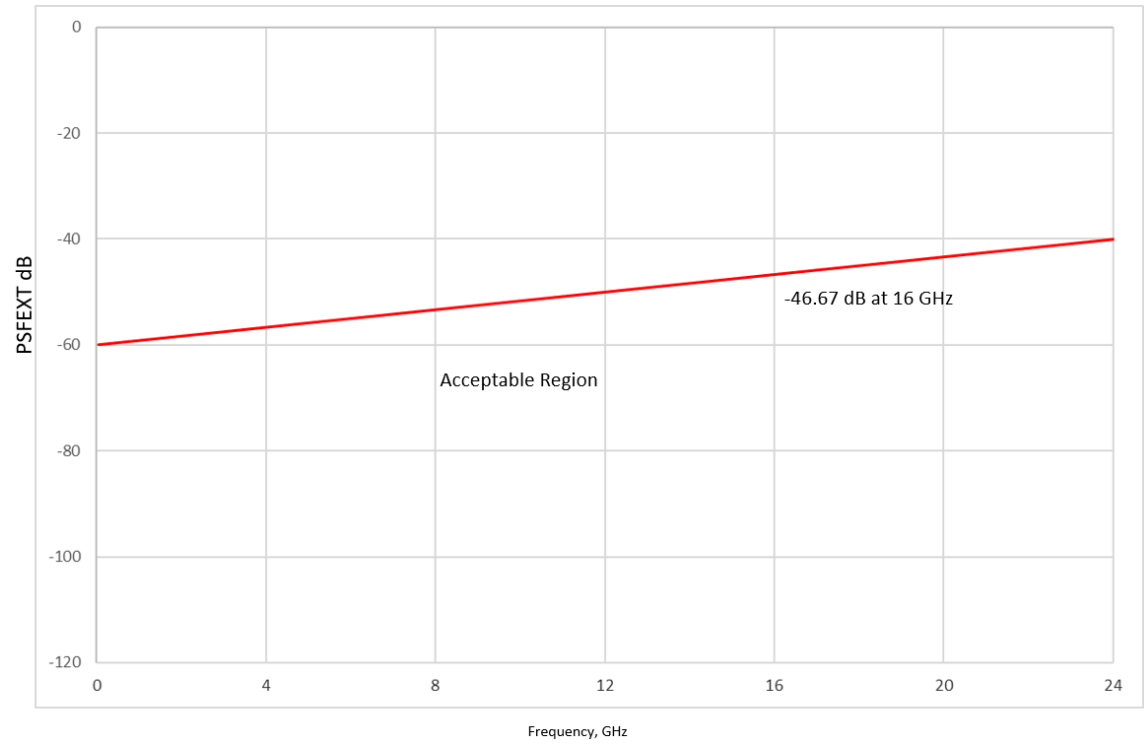
Figure 6-23. Differential Far End Crosstalk Limits for 32.0 GT/s Operation

6.6. Standalone Connector Test Guidelines, Test Fixture Recommendations, and PCB Layout for 16.0 GT/s and 32.0 GT/s

6.6.1. Standalone Connector Test Guidelines

This section describes the proposed Victim-Aggressor pattern for separate FEXT and NEXT measurements to characterize the interface signals incorporated pinouts on the 16.0 GT/s and 32 GT/s M.2 connectors, based on the directionality associated with them.

The effective Near End crosstalk (Figure 6-24) and Far End crosstalk (Figure 6-25) are plotted by calculating the power-sum of the crosstalk from the NEXT or FEXT aggressors, in a given pinout, using the following formulas:

$$DDNEXT = 10 \log 10 \left(\sum_i^N 10^{DDNEXT_i/10} \right)$$

$$DDFEXT = 10 \log 10 \left(\sum_i^N 10^{DDFEXT_i/10} \right)$$
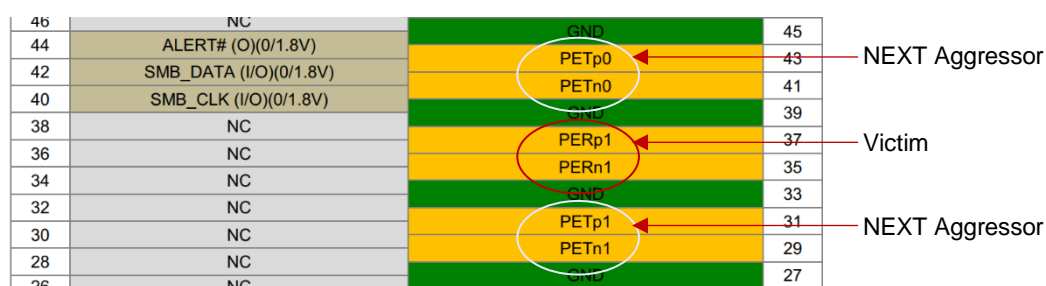
Figure 6-24. Near End Crosstalk Victim and Aggressors for the PCIe Based Pinout (Socket 2 & 3)

Figure 6-25. Far End Crosstalk Victim and Aggressors for the PCIe Based Pinout

6.6.2.   Test Fixture Recommendations and Gold Finger Ground Voiding Guidelines to support 16.0 GT/s and 32.0 GT/s

A test fixture for connector S-parameter measurement must be designed and built to the following:

❑ The test fixture used for measuring S-parameters will comprise a baseboard and mating Add-in Card fabricated from the same PCB panel. The total thickness of the boards, measured across the Add-in Card edge fingers, must be 0.8 mm (31.5 mil).

❑ For 16.0 GT/s, the PCB test fixture must be an FR-4 based material, or of a lower loss material with a relative permittivity of 3.6 or greater. Dielectric loss factor is not specified.
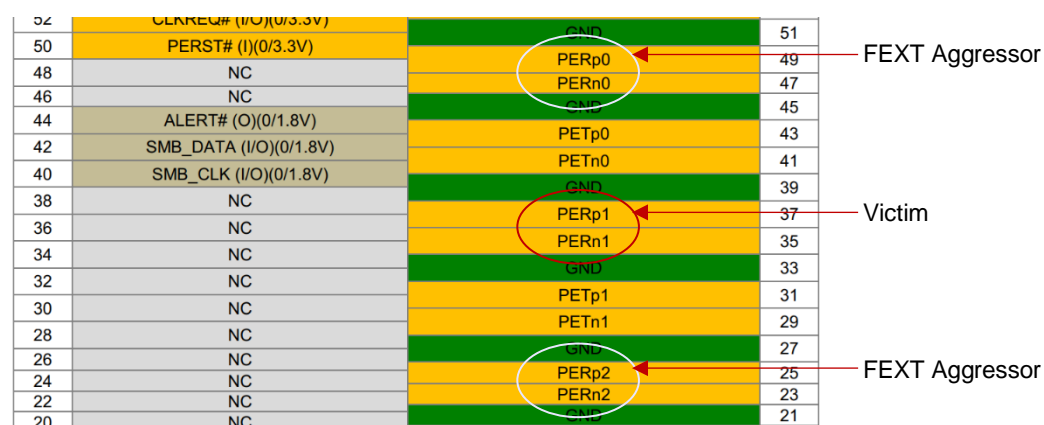
❑ For 32 GT/s, the PCB test fixture must be Meg-6 based material, or of a lower loss material with a relative permittivity of 3.6 or greater. Dielectric loss factor is not specified.

❑ The test PCB must have a microstrip structure; the microstrip's dielectric thickness or stack-up are recommended to be approximately 0.102 mm (4 mil).

❑ The interconnect traces on all boards must be routed uncoupled (single-ended) where possible. Some method of mitigating fiber weave effects must be applied. This can include off axis routing or board rotation on the PCB panel.

❑ The trace lengths between the connector and measurement port must be minimized. The maximum trace length must not exceed 45.72 mm (1.8 inches). The trace length delta between the connector and measurement port on the test baseboard and that on the Add-in Card must be less than 0.5 mil. The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector.

❑ Separate PCB structures must be included to support de-embedding of the feeds to isolate the performance of the connector interface. These structures may support Thru-Reflect-Line, the 2x thru procedure, or a similar de-embedding method. The de-embedding structures' signal launch and traces must match those of the test fixture.

❑ The baseboard, and Add-in Card must be on the same PCB panel during fabrication, and the de-embedding structures must lie on one or both test boards, or on a third adjacent PCB card. Silkscreen serialization of the test cards during manufacturing may aid in tracking adjacent PCB sets.

❑ The pin field must replicate the pin assignments of Socket 3. The pin pairs measured correspond to high-speed pairs Tx0, Tx1, and Tx2, as well as Rx0, Rx1, and Rx2, as shown in Table 6-3. The high-speed pins in Table 6-3 labeled 42.5 Ω, such as Tx3, must be terminated with 42.5 Ω ± 2 Ω resistors to emulate the termination of an operating high-speed pair. The trace between the high-speed edge fingers or baseboard pin and the termination must have a characteristic impedance of 42.5 Ω.

❑ The clock pair, pins 55 and 53 (Table 6-3), must be terminated single-ended with resistors whose values are 50 Ω ± 2 Ω. This termination is applied on the baseboard side only; the Add-in Card REFCLK nets are left open circuited at the end of the edge fingers.

- ❑ Compression-fit (bolt-on) PCB mount coaxial connectors are recommended, but not required, for the PCB test ports. The signal launch of the test port connectors must be optimized for lowest return loss across the band of interest.
- ❑ Via stubs, both in the test port feeds and in the pin field, must be avoided.
- ❑ Test port feeds marked "MEASURE" in Table 6-4 must be optimized to a characteristic impedance of either 42.5 Ω or 50 Ω. All the traces on the test board and Add-in Card must be held to the specified characteristic impedance 42.5 Ω or 50 Ω with a tolerance of ±7%.
- ❑ The pin field must replicate the pin assignments of Socket 3. The pin pairs measured correspond to highspeed pairs Tx0, Tx1, and Tx2, as well as Rx0, Rx1 and Rx2, as shown in Table 6-4.
- ❑ The pin field in Table 6-4 requires a Socket 3 connector and its companion card.
- ❑ Scattering parameters must be obtained over a range spanning 100 MHz to 10 GHz, with a frequency spacing of no greater than 10 MHz.
- ❑ Compression-fit (bolt-on) PCB mount coaxial connectors are recommended, but not required, for the PCB test ports. The signal launch of the test port connectors must be optimized for lowest return loss across the band of interest.

Table 6-4.   Pin Connectivity for the 16.0 GT/s and 32.0 GT/s Connector Characterization Board

Pin	Signal Assignment	Baseboard Termination	Add-in Card Termination
57	GND	GND	GND
55	REFCLK	50 Ω	OPEN
53	REFCLK	50 Ω	OPEN
51	GND	GND	GND
49	Tx0p	MEASURE	MEASURE
47	Tx0n	MEASURE	MEASURE
45	GND	GND	GND
43	Rx0p	MEASURE	MEASURE
41	Rx0n	MEASURE	MEASURE
39	GND	GND	GND
37	Tx1p	MEASURE	MEASURE
35	Tx1n	MEASURE	MEASURE
33	GND	GND	GND
31	Rx1p	MEASURE	MEASURE
29	Rx1n	MEASURE	MEASURE
27	GND	GND	GND
25	Tx2p	MEASURE	MEASURE
23	Tx2n	MEASURE	MEASURE
21	GND	GND	GND
19	Rx2p	42.5 Ω	42.5 Ω
17	Rx2n	42.5 Ω	42.5 Ω
15	GND	GND	GND

Pin	Signal Assignment	Baseboard Termination	Add-in Card Termination
13	Tx3p	42.5 Ω	42.5 Ω
11	Tx3n	42.5 Ω	42.5 Ω
9	GND	GND	GND
7	Rx3p	42.5 Ω	42.5 Ω
5	Rx3n	42.5 Ω	42.5 Ω

Figure 6-26, Figure 6-27, Figure 6-28, and Figure 6-29 show Test Fixture Recommendations and Gold Finger Ground Voiding Guidelines to support 16.0 GT/s and 32.0 GT/s.
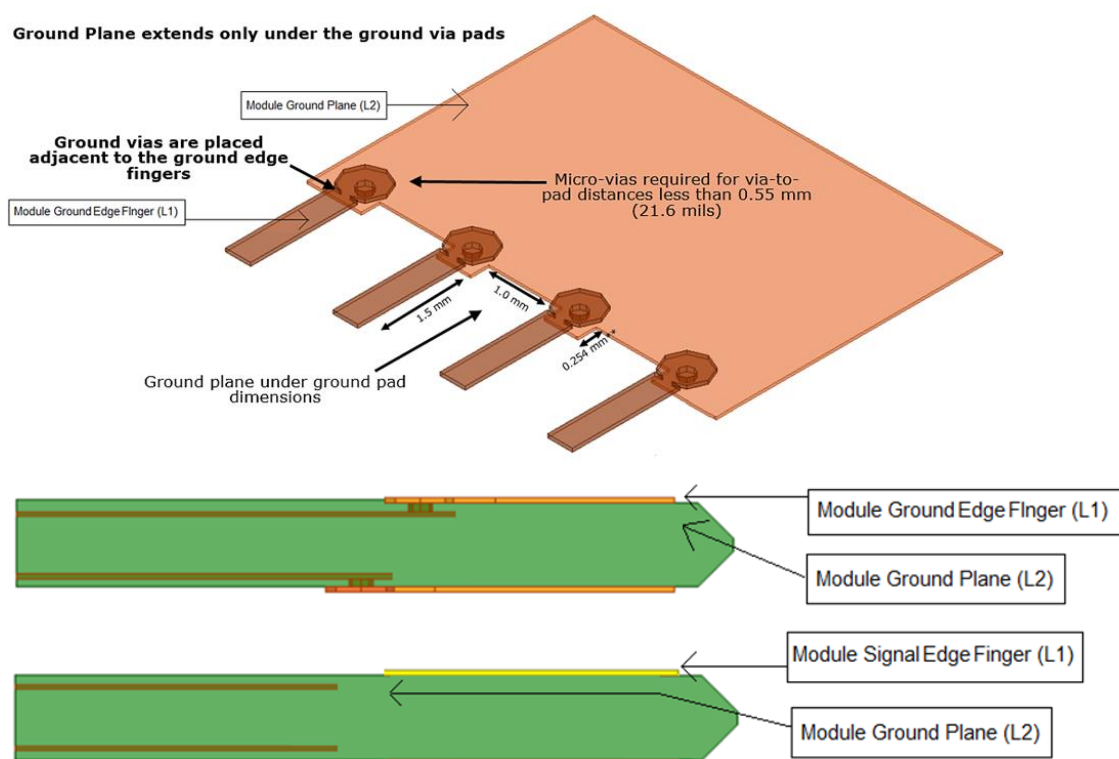
Figure 6-26. Suggested Add-in Card Signals and Ground Pad Layout Guideline (Top View and Side Cross-section View)
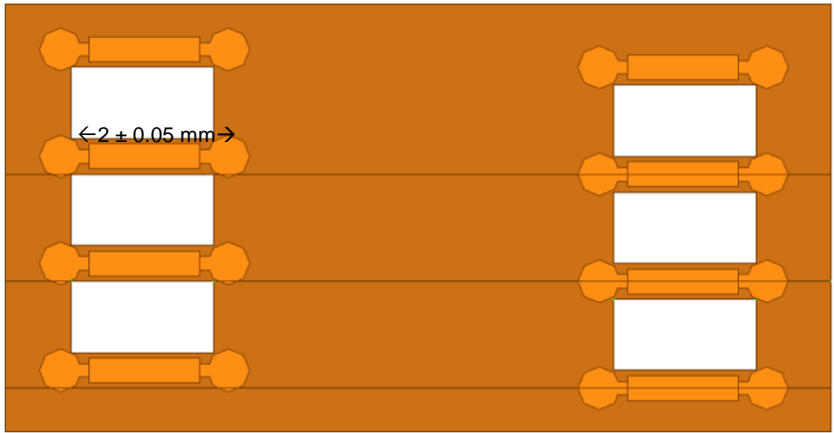
A recommendation for the baseboard, is using Toe and Heel ground vias as shown in Figure 6-26, to increase the resonant frequency; and broaden the traces to vias as much as possible without violating trace-to-trace spacing requirements.

Figure 6-27. Suggested Ground Void for Add-in Card Simulation
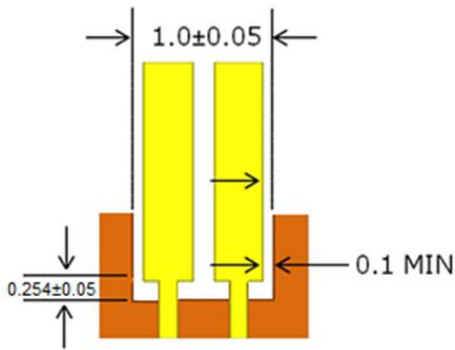
Figure 6-28. Suggested Ground Void for Add-in Card
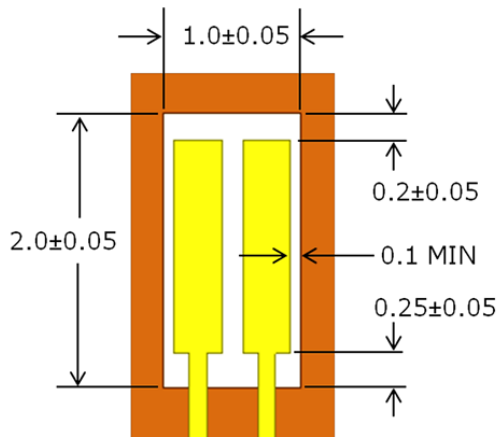
Figure 6-29. Suggested Ground Void for Main Board

6.6.3. Suggested Top Mount Signal Integrity PCB Layout

Suggested PCB layouts for the test Add-in Card and test baseboard side used to test the M.2 Top Mount Connector are given in Figure 6-30 and Figure 6-31.
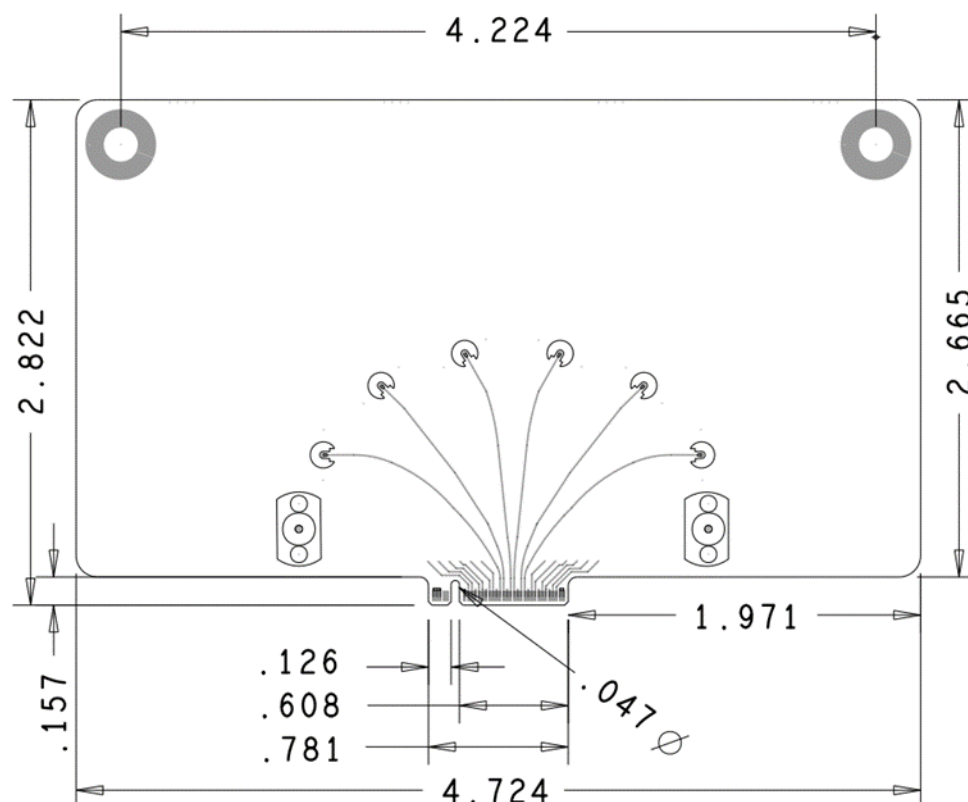
Figure 6-30. Top Mount Add-in Card Test Fixture PCB Layout
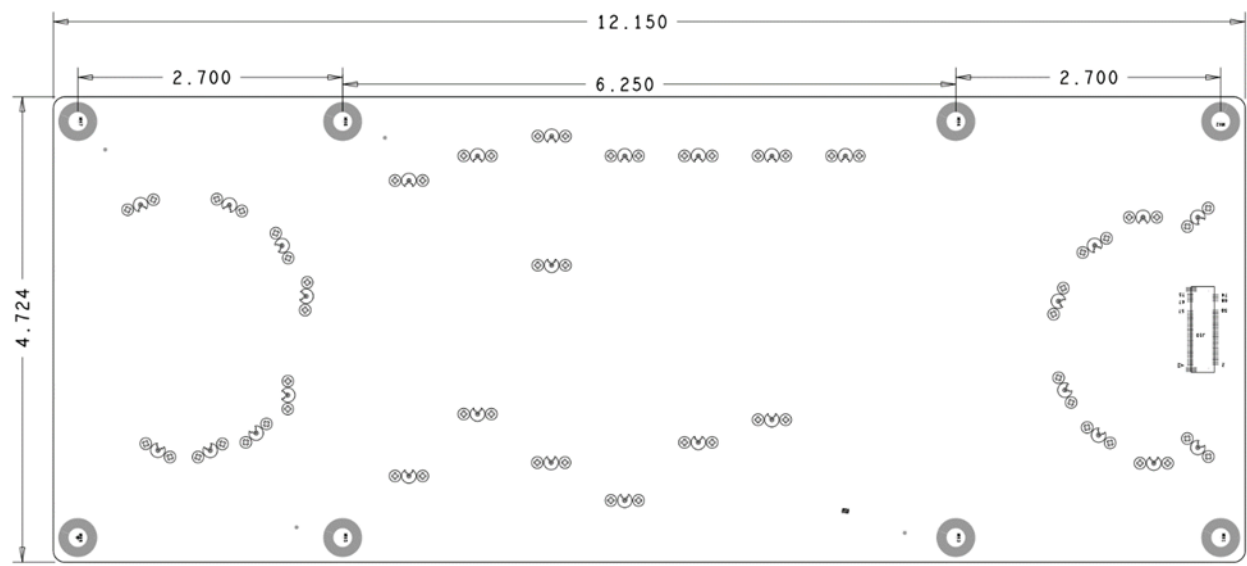
Top View with Connector
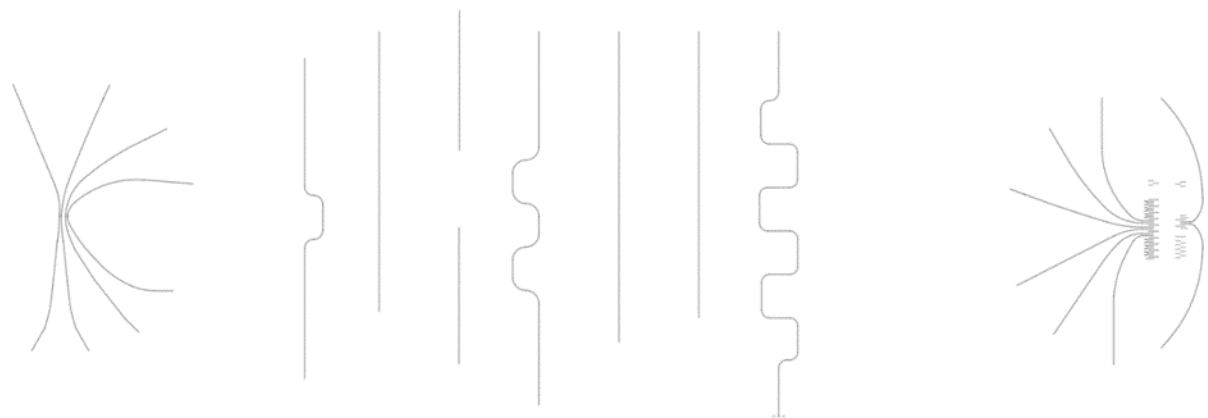
Bottom View with Trace

Figure 6-31. Top Mount Motherboard Test Fixture PCB

6.7. RF Connector Related Test Setups

6.7.1. VSWR Test Set-up Method for RF Connector Receptacles

Measure the VSWR of the receptacle as shown in Figure 6-32 with the aid of a Network Analyzer. Measure between 100 MHz and 6 GHz or alternatively for the optional enhanced connector from 100 MHz and 12 GHz.
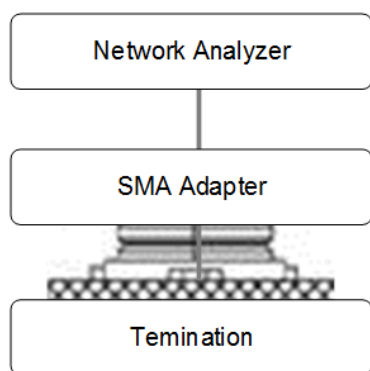
Figure 6-32. VSWR Test Setup for Receptacle RF Connector

6.7.2. Contact Resistance Measurement Setup and Test Procedure Example

Contact resistance measurement definitions are given in Figure 6-33.

Inner Contact = A-B
Ground Contact = D-C
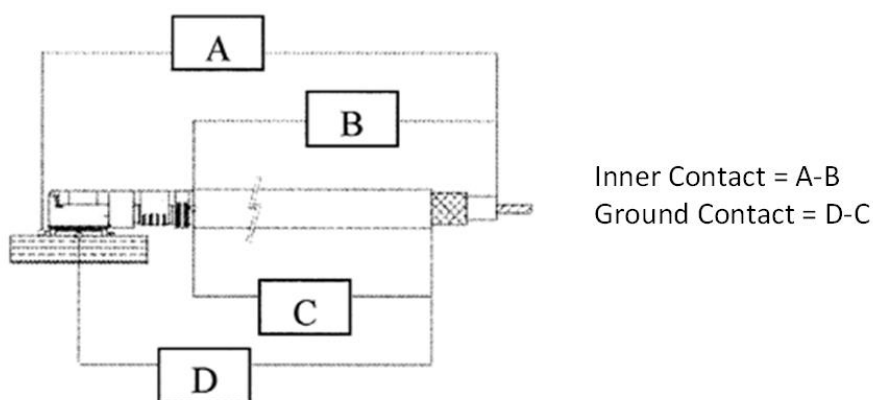
Figure 6-33. Contact Resistance Measurement Definitions

Step 1: Measure ten 50 mm length wire samples (prepared for plugs but un-terminated, (Figure 6-34).
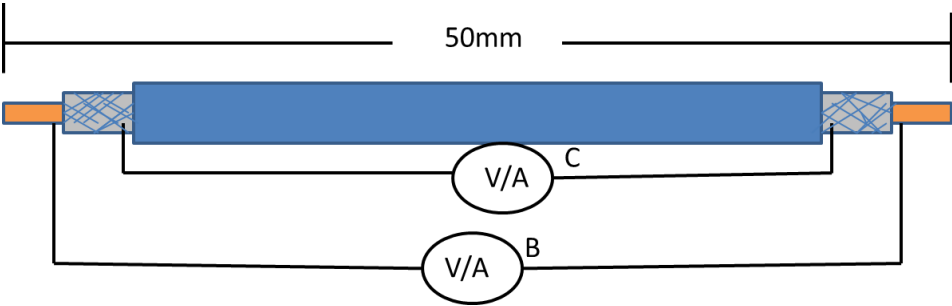
Figure 6-34. Prepared Wires

Example results: n=10, Unit: mΩ

	Main (B)	GND (C)
Conductor Resistance (Average)	59.020	10.920

There are variations in Center Conductor Preparation and Braid Conductor Materials. Therefore, the average of 10 wires at a length 50 mm are used for the Contact Resistance Measurements. Another variation is that this exact wire is not used when measuring the terminated mated set Cable Connector to Receptacle in the next step.

Step 2: Measurement with Plug (Figure 6-35).
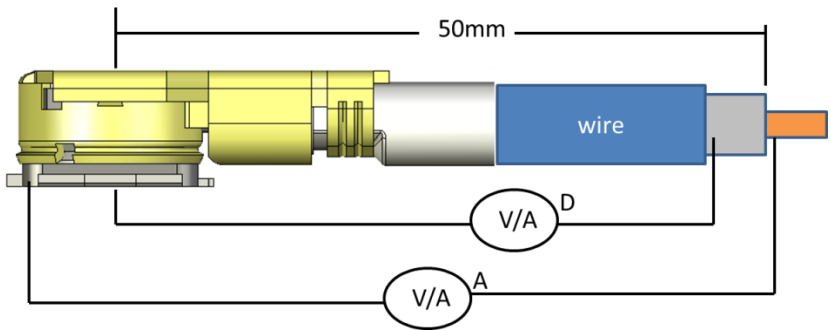
Figure 6-35. Prepared Wire with Plug

A = Total Measurement of the Cable Center conductor + the Connector Set Contact Resistance
D = Total Measurement of the Ground Braid conductor + the Connector Set Gnd. Resistance

Examples of measured results of the wire with plug are given in Table 6-5.

Table 6-5.   Example of Prepared Wire with Plug

	Main (A)	GND (D)	Units
Sample 1	67.36	21.64	mΩ
Sample 2	67.61	18.61	mΩ
Sample 3	68.41	20.22	mΩ
Sample 4	68.82	19.54	mΩ
Sample 5	73.50	19.65	mΩ
Sample 6	66.41	18.76	mΩ
Sample 7	70.07	24.77	mΩ
Sample 8	68.60	19.67	mΩ
Sample 9	68.29	19.98	mΩ
Sample 10	69.37	17.52	mΩ
Average	68.845	20.036	mΩ
Maximum	73.50	24.77	mΩ
Minimum	66.41	17.52	mΩ
s (Standard Deviation)	1.934	1.987	mΩ
+3s	74.647	25.996	mΩ

Note: Not the exact same wire is used to determine the average resistance of the wire. Variations in materials cause the resistance measurements to have various values.
Slight differences in plating may cause the resistance measurements to have various values.

Step 3: Calculate the Contact Resistance

Subtract the measured results, A-B and D-C to find the Contact Resistance for the sample wires/plugs. Example results are given in Table 6-6.

Table 6-6.   Contact Resistance for the Sample Wires/Plugs

	Main	GND (C)	Units
Sample 1	8.34	10.72	mΩ
Sample 2	8.59	7.69	mΩ
Sample 3	9.39	9.30	mΩ
Sample 4	9.80	8.62	mΩ
Sample 5	14.48	8.73	mΩ
Sample 6	7.39	7.84	mΩ
Sample 7	11.05	13.85	mΩ
Sample 8	9.58	8.75	mΩ
Sample 9	9.27	9.06	mΩ
Sample 10	10.35	6.60	mΩ
Average	9.825	9.116	mΩ
Maximum	14.48	13.85	mΩ
Minimum	7.39	6.60	mΩ
s (Standard Deviation)	1.934	1.987	mΩ
+3s	15.627	15.076	mΩ
Spec	20.0 Max		
Judge	OK	OK	

Based on the sample results, the Initial Contact Resistance is defined as 20 mΩ to make sure wire/plug variations are covered.

6.8.   Thermal Guideline Annex

This section details examples of Adapter and system skin (casing) thermal response to thermal and dissipation boundary conditions in systems. The boundary conditions vary by system, as do the skin temperature limits.

6.8.1.   Assumptions

6.8.1.1.   Die Thermal Dissipation Overview

Assumptions for typical components and dissipation for several Adapter types are given in Table 6-7. Keep in mind the definition of TDP given in Section 2.6.2.1. Note that the maxima given here do not necessarily correspond to their actual use in a system; these values are, from the die perspective, what they would dissipate when running all the time at their maximum capacity. The system use-case scenarios make assumptions about how much of the time the devices would run and scale the dissipation accordingly. The TDP therefore is different from the thermal dissipation given in Table 6-8.

Table 6-7.   Assumptions for Typical Components and Dissipation

Adapter Type	Die #	Function	Thermal Dissipation Estimates	Adapter Total Dissipation (Not Necessarily TDP)	Power Allocation	Power Map
Wi-Fi/BT	1	Wi-Fi/BT	2	2	100%	Wi-Fi/BT
WWAN	1	Baseband	1.2	1.9 Typical 3.25 Worst	32%	Uniform
	2	Power Mgmt			14%	
	3	RF Transceiver	0.4		11%	
	4	PA	0.3 Typ / 1.65 Worst		43%	
SSD	1	ASIC	1.5	1.74	86%	Uniform
	2	DRAM	0.05		3%	
	3	NAND1	0.03 Typ / 0.25 Worst		2%	
	4	NAND2	0.03 Typ / 0.25 Worst		2%	
	5	NAND3	0.03 Typ / 0.25 Worst		2%	
	6	NAND4	0.03 Typ / 0.25 Worst		2%	
	7	POWER	0.07		4%	
WiGig	1	Wi-Fi/BT	2	3	67%	Wi-Fi/BT
	2	WiGig	1		33%	Wi-Fi no BT

Note: For comparison, maximum dissipations for WWAN components vary by technology, and are shown in Table 6-8. Most of these are in the 3 W range.

Table 6-8.   Maximum Dissipation for WWAN Adapters

WWAN Technology	Maximum Dissipation, W (not necessarily TDP)
W-CDMA HSDPA 1900 @ 22 dBm	3.0 ± 0.1
W-CDMA HSDPA 850 @ 22 dBm	2.9 ± 0.1
W-CDMA HSDPA 2100 @ 22 dBm	2.7
CDMA 1xEVDO @ 24 dBm	2.8 ± 0.1
GPRS Class 10 @ 32 dBm	1.8
LTE @ 22 dBm	3.1 ± 0.1

6.8.1.2.   **Component Overview**

Generic assumptions for package designations and types expected to populate Adapters are listed in Table 6-9.

Table 6-9.   Generic Assumptions for Package Designations and Types Expected to Populate Adapters

Type	Layers 1 oz	Function	Die #	Type	Package	Package Size (mm x mm)	Die Size (mm x mm)	Via Array (mm x mm)	Via Pitch (mm)
2230	4	Wi-Fi/BT	1	Wi-Fi/BT	QFN	9x9	6x6	6x6	1
3042	8	WWAN	1	Baseband	PBGA	10x10	5.5x5.5	4x4	1.27
			2	Power Mgmt.	PBGA	4x4	2x2	2x2	1.27
			3	RF Transceiver	PBGA	5x5	3x3	2x2	1.27
			4	PA	LGA	5x7	1.3x2	2x6	1
2280 Double-sided	6	SSD	1	ASIC	BGA	20x20	12x12	9x9	1.27
			2	DRAM	BGA	11x10	7x7		
			3	NAND1	BGA	15x18	10x12		
			4	NAND2	BGA	15x18	10x12		
			5	NAND3	BGA	15x18	10x12		
			6	NAND4	BGA	15x18	10x12		
			7	POWER	DFN	6x5	4.125x3.75		
3030	6	Wi-Fi/BT + WiGig	1	Wi-Fi/BT	QFN	9x9	6x6	6x6	1
			2	WiGig	PBGA	9x9	6x6	4x4	1.27

6.8.2. Generic System Environment Categories (Assumptions)

Table 6-10 gives assumptions for each generic system environment. These are meant to be slightly aggressive targets at the time of writing.

Table 6-10.   Assumptions for Generic System Environments

Type	Notebook		Thin Platform Notebook With Fan		Tablet Fanless	Units
Case Size	325 x 225		325 x 225 (14")		250 x 170	
Total /Base Thickness	28/18		15/10		8	mm
Case Material	Resin		Mg		Mg	
Case Thickness	1.1		0.8		0.8	mm
Case Exterior Emissivity	High		High		High	
Case Interior Emissivity	High		Low		Low	
External Ambient	25	35 (see Note 1)	25	35 (see Note 1)	25	°C
Skin T Limit Top ("Forehead")	37	55	37	46	40 (display)	°C
Skin T Limit Bottom	48	58	42	46	38	°C
Gap Adapter to Case	> 2		> 1		< 0.5	mm
Motherboard Size	180 x 83 x 1.2		180 x 83 x 1		140 x 45 x 0.9	mm
Adapter Orientation	Table		Table		Back	
Inlet Vent Area	30 x 30 + 83 x 16 + 2 edge vents 20 x 2.5		60 x 30 + 2 edge vents 20 x 5		N/A	
Outlet Vent Area	60 x 10 grille		60 x 10 grille		N/A	mm
Fan Flow Rate	2.4 68		0.6 17		N/A	cfm (see Note 2) lpm (see Note 3)

Notes:
1. Shown for example purposes only
2. Cubic feet per minute
3. Liter per minute

6.8.2.1.   Adapter Slot Definitions by System

The following assumptions apply to the results and discussions of the examples in this document.

❑ 25 °C ambient is assumed for skin temperature compliance

❑ Socket 1 = Wi-Fi/BT OR Wi-Fi/WiGig

❑ Socket 2 = WWAN

❑ Socket 3 if present = SSD

❑ Wi-Fi/BT and WWAN operation are mutually exclusive; (i.e., the system is connected to one or the other, but not both)

❑ If Socket 3 is present, Socket 2 is WWAN

❑ Skin temperature limits are OEM dependent and sometimes market sector dependent

❑ Global skin temperature levels are system dependent (heat exchanger design, fan flow rate, board layout, system TDP distribution)

❑ Local skin temperatures and Adapter TDP values are given assuming no special thermal management techniques have been applied to either the Adapter or the nearby casing

❑ Thermally advantageous placement of Adapter is assumed

6.8.2.1.1.   Systems with Fans

Table 6-11 lists the system slot definitions with fans.

Table 6-11.   Slot Definitions, Systems with Fans

	Notebook		Thin Platform Notebook with Fan		
Socket #	1	2	1	2	3
Adapter Size	2230	3042	3030	3042	2280
Function	Wi-Fi/BT	WWAN	Wi-Fi/BT + WiGig	WWAN	SSD

6.8.2.1.2.   Systems without Fans

Table 6-12 lists the system slot definitions without fans.

Table 6-12.   Slot Definitions, Systems without Fans

	Tablet	
Scenario		
Socket #	1	2
Adapter Size	2230	3042
Function	Wi-Fi/BT	WWAN LTE

6.8.3. Assessing Thermal Design Power Capability

6.8.3.1. Use Cases

Assumptions for the distribution of thermal dissipation throughout the system are needed for each system type. These are known as "use cases" and are established by defining a scenario for what the user is asking the system to do. In many cases, there are simultaneous active applications taxing different areas of the system. The use cases in this document are intended for illustration only; an analogous process should be carried out by system designers for each system.

6.8.3.2. Extended Use Cases

To evaluate system and Adapter response to TDP variations, a use case baseline is established, and the Adapter dissipation varied around the nominal value for the use case. In this document, the "extended use case" (the use case plus a higher dissipation for the Adapter in question) is analyzed for skin temperature response. Hypothetical example systems are modeled with use cases relevant to dissipation in the Adapters. The Adapter dissipation is varied over the range 0 – use case TDP – 3 W to obtain the sensitivity of skin temperature to Adapter dissipation.

6.8.3.3. Unpowered Adapter

For Adapter designers, the use cases are valuable background to establishing potential Adapter environments. Particularly helpful for them should be the system skin and module temperatures when there is an unpowered Adapter, which is meant to give an idea of the starting point for any thermal excursion due to the Adapter's own power.

6.8.3.4. Use Case Flexibility

It is worthwhile to note that in some instances, the stated assumptions about use case do not result in a system that meets its specifications. Including power management features in the Adapter components will give system designers maximum flexibility to manage power dissipation. This flexibility applies to many of the system's components to meet specifications. It should be noted again that for skin temperature limits, the time scale of interest is of the order of several minutes, while the time scale for many system tasks is much shorter.

Most business applications enable the wireless communications Adapters to go dormant, thereby lowering the average thermal dissipation. Applications that perform data streaming such as VOIP, video streaming from an attached camera or streaming audio prevent the communications Adapters from going dormant. The host should support the USB Selective Suspend feature to reduce electrical power consumption and thermal dissipation by the wireless Adapters.

6.8.4. Adapter Placement Advice

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the Adapters should be located away from areas of concentrated heat on the motherboard, and as far as possible from any heat exchanger.

For systems with fans, place inlet vents near Adapters to flush the inside surface of the casing and use the bottom vent to act as a thermal break if needed.

Address global hot spots via general system layout and use case assumptions.

6.8.5. Skin Temperature Sensitivity to Adapter Power

Skin temperatures in the vicinity of Adapters depend on the Adapter power and the total system power and its arrangement. Systems with low flow rates will have higher sensitivity than systems with higher flow rates. Systems without ventilation are most sensitive, up to 3 °C skin temperature increase per Watt of Adapter power in the example systems shown in Section 6.8.8. This value may not be generally applicable – thermal studies should be carried out at the system level.

6.8.6. General Applicability

The examples shown in Section 6.5.8 are not intended to be generally applicable. They are only meant to show the potential range of responses, and to determine sensible advice for Adapter placement and other approaches to thermal management. The TDP response is established by the design team for each system design. Thermal analysis by computational and physical (experimental) modeling is strongly encouraged at the system level.

6.8.7. Generic Assumptions for Adapter Arrangement

Adapters may represent a significant portion of the total system dissipation and may be a major contributor to system skin temperature. It is a good idea to place them in thermally advantageous locations. Examples shown throughout this document indicate such thermally advantageous placements, but of course are only meant to show the possibilities, and do not represent actual final designs. Nor have all the model assumptions been completely tested, so the accuracy of any predictions is within several degrees at best.

For systems with fans, vents upstream help to cool both the Adapter and the nearby casing to minimize skin temperature. They may also have a "thermal break" effect, protecting the local surface near the Adapters from the larger global maximum surface temperature.

For systems without fans, concentrations of high heat density should be avoided, since the thin metal skin achieves only a limited level of heat spreading. In addition, it is well known that placing heat sources near edges or corners of a heat spreader cause higher temperatures than placing them in a central location on the spreader.

6.8.8. Examples

6.8.8.1. Notebook Category

Many assumptions are used in this document. Table 6-13 lists examples of cases applicable to Adapters for notebooks.

Table 6-13.   Example Use Case Applicable to Adapters for Notebooks

Component	TDP (W)
Scenario	Comms Excursion
Application Mix	Local Network (Wi-Fi) File Transfer+ Device (BT) File Copy+ Netflix (Chrome) 1080p [+Wi-Fi]
Motherboard CPU	26
Motherboard VR, chipset, etc.	8.2
Memory	1.5
HDD+SSD Cache	1.1
HDD	0.1
SSD Cache	1.0
Comms: WLAN/BT	2.2
Comms: WWAN	0.0
ODD	0.1
Fan	0.9
Platform Total	**40**

6.8.8.1.1. Generic Motherboard Assumptions

The bottom view of a single-sided motherboard (all components facing the table within the system) with a thermal solution applied to CPU is shown in Figure 6-36. The Adapters are installed in top mount connectors at one edge of the board, as far from the CPU as possible. There are several memory Adapters and two areas of clustered small heat sources, each shown as a rectangular heated area. The motherboard heat sources form a thermal boundary condition for the Adapters.
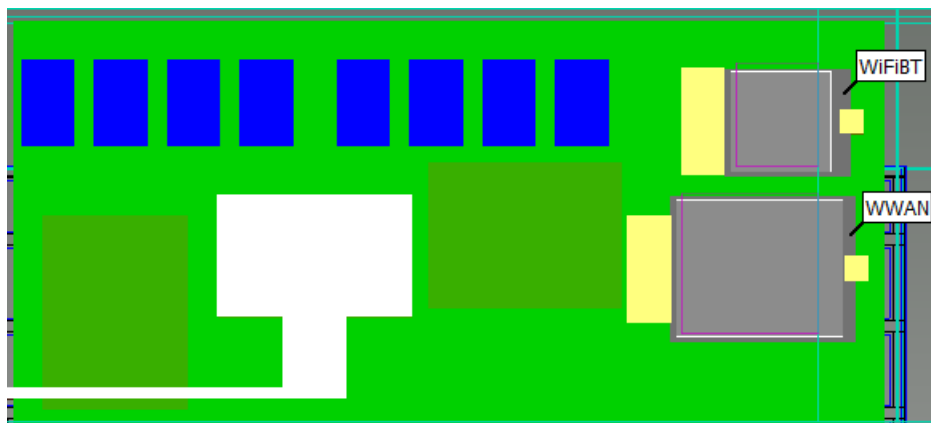
Figure 6-36. Example View of Notebook Motherboard

6.8.8.1.2.   System Layout Assumptions

Flow related assumptions include a fan at 68 l/min (2.4 cfm), a vent opening near the cards, and small slot vents in the system's side (Figure 6-37 shows edge vents and Figure 6-38 shows bottom vents).
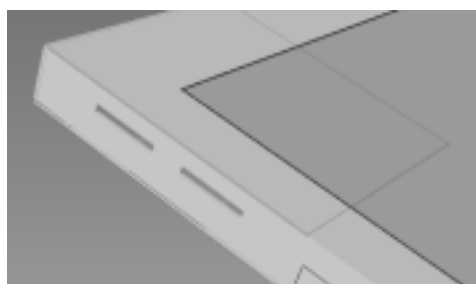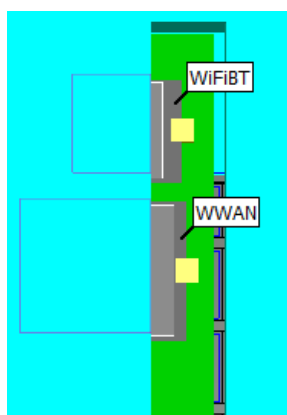

Figure 6-37. Example View of Edge Vents

Figure 6-38. Example View of Bottom Vents (vent opening where inside boards are visible through the opening)

6.8.8.1.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is only very slightly dependent on the Adapter dissipation, as in this system category the Adapter makes up a relatively small fraction of the total system TDP.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 6-39 and Figure 6-40, a region of interest is defined near the Adapters, and the region maximum obtained. Another method might be to track a single consistent point over each Adapter.
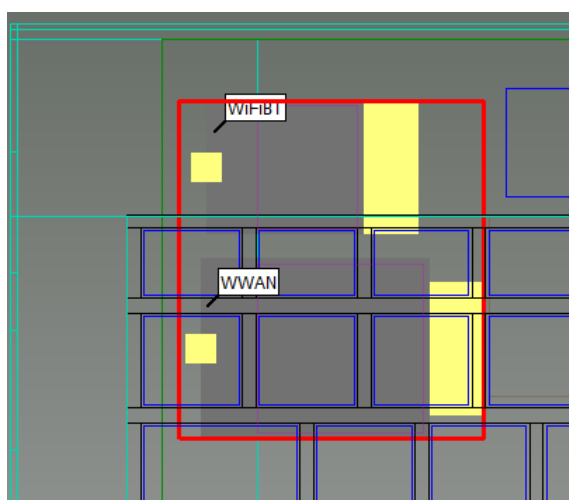

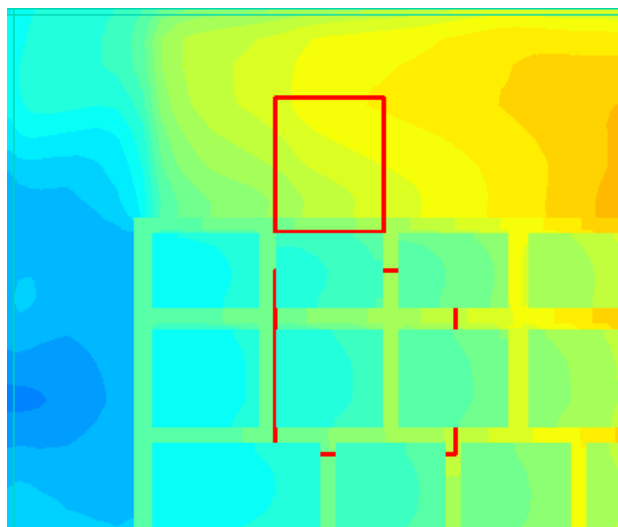Figure 6-39. Example View of Region Over Adapters

Figure 6-40. Example View of Hot Spot Over Adapters

6.8.8.1.4. Thermal Design Power Response – Notebook Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to 3 W in the use case. Results are shown in Table 6-14, Table 6-15, and Table 6-16. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the Adapter) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any Adapter dissipation. Although the Adapters do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide guidance about sensible system design for Adapter effects on skin temperature. The particulars of the keyboard model especially determine the skin temperature of Adapters below the keyboard area.

Table 6-14. Thermal Design Power Response – Notebook Category

	Notebook	Notebook	Units
Socket #	1	2	
Adapter Size	2230	3042	
Function	Wi-Fi/BT	WWAN	
Use case	Comms exc	Comms exc WWAN	
System Dissipation W/O Adapter	37.8	37.8	W
Adapter Off	0	0	W
Mean Card T	32	34	°C
Local Skin T Top	30	28	°C
Local Skin T Bottom	28	30	°C
Global Skin Hot Spot (HX)	47	47	°C
Use Case TDP	2.2	2.2	W
Local Skin T Top	31	28	°C
Local Skin T Bottom	30	31	°C
Global Skin Hot Spot (HX)	47	47	°C
Extended Case TDP	3	3	W
Local Skin T Top	31	29	°C
Local Skin T Bottom	31	31	°C
Fan Flow Rate	2.4	2.4	cfm

Table 6-15.   Skin Temperature Limit Assumptions, Notebook

	Value	Units
Ext Ambient	25	°C
Skin T Limit Top	37	°C
Skin T Limit Bottom	48	°C

Table 6-16.   Skin Temperature Effect of Adapter Position

Adapter Switched Places	Notebook		Units
Socket #	1	2	
Adapter Size	3042	2230	
Function	WWAN	Wi-Fi/BT	
Use Case	Comms exc WWAN	Comms exc	
Use Case TDP	2.2	2.2	W
Local Skin T Top	28	31	°C
Local Skin T Bottom	31	30	°C

6.8.8.2.   **Thin Platform Notebook with Fan Category**

Many assumptions are used in this document. Table 6-17 shows the use cases applicable to Adapters for thin Platform notebook with fan.

Table 6-17.   Use Cases Applicable to Adapters for Thin Platform Notebook with Fan

Component	Thermal Design Power (W) by Scenario	
Scenario	Platform Chipset Excursion	Comms Excursion
Application Mix	Skype+ Windows Media Player+ OS File Transfers+ SS Storage File Copy	Local Network (Wi-Fi) File Transfer+ Device (BT) File Copy+ Netflix(Chrome) 1080p [+Wi-Fi]
Motherboard CPU + Chipset	13.5	12.8
Motherboard Distributed	4.2	3.7
Memory	1.5	1.5
SSD	2.4	0.5
Comms: WLAN/BT or WWAN	0.9	1.4
Platform Total	23.4	20.8

6.8.8.2.1.   Generic Motherboard Assumptions

The bottom view of a single-sided motherboard (all components facing the table within the system) with thermal solution applied to CPU is shown in Figure 6-41. The cards are installed in mid-mount connectors at one edge of the board, as far from the CPU as possible. There are several memory Adapters and two areas of clustered small heat sources, each shown as a rectangular heated area. The motherboard heat sources form a thermal boundary condition for the Adapters.
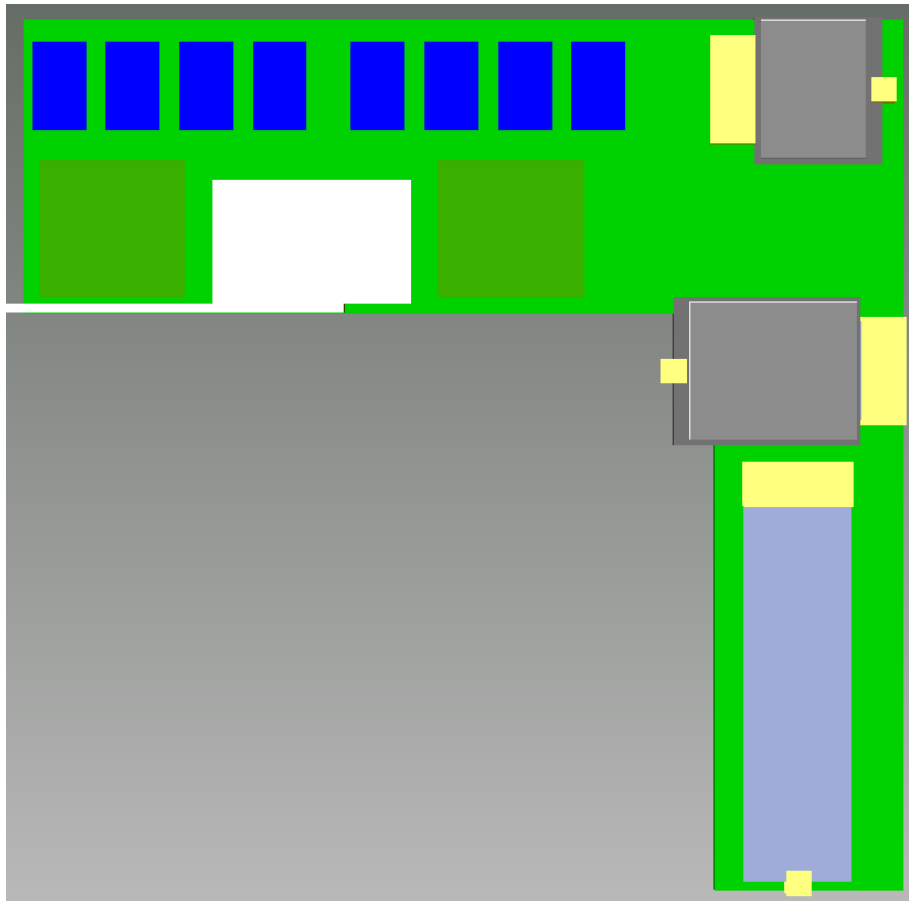
Figure 6-41. Example View of Motherboard for Thin Platform Notebook with Fan

6.8.8.2.2.   System Layout Assumptions

Flow related assumptions include a fan at 17 l/min (0.6 cfm), a vent opening below the Adapters, and small slot vents in the system's side (see Figure 6-42). The vent opening below the cards reduces the local surface temperature.
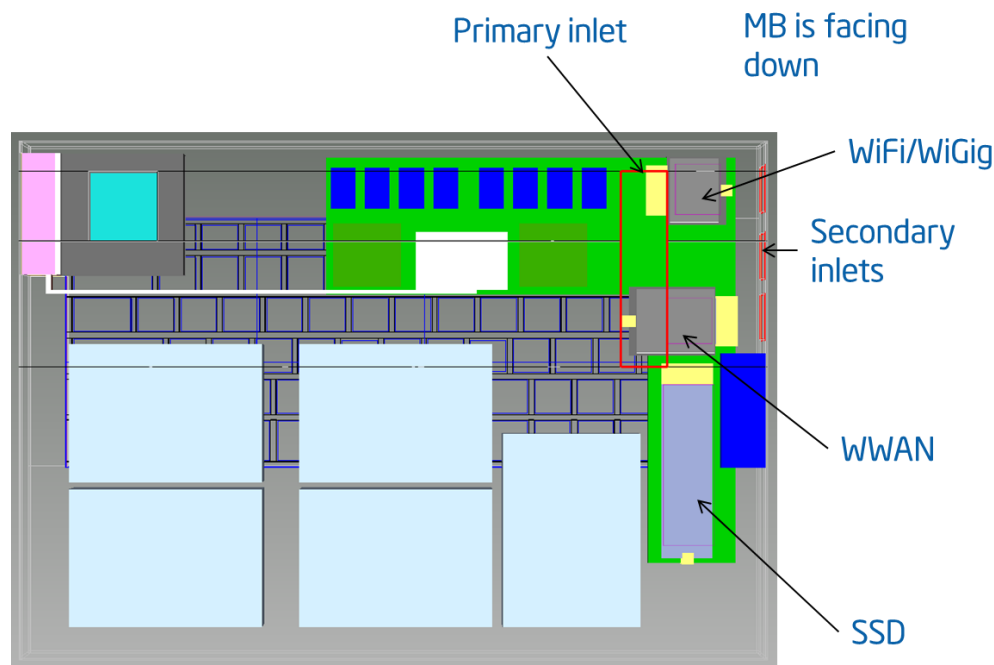
Figure 6-42. Thin Platform Notebook Layout with Vents and Key Components

6.8.8.2.3. Adapter Placement Advice – Thin Platform Notebook

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the Adapters should be located away from areas of concentrated heat on the motherboard, and especially as far as possible from the heat exchanger. Place inlet vents near Adapters to flush the inside surface of the casing and use the bottom vent to act as a thermal break if needed. Address global hot spots via general system layout and use case assumptions.

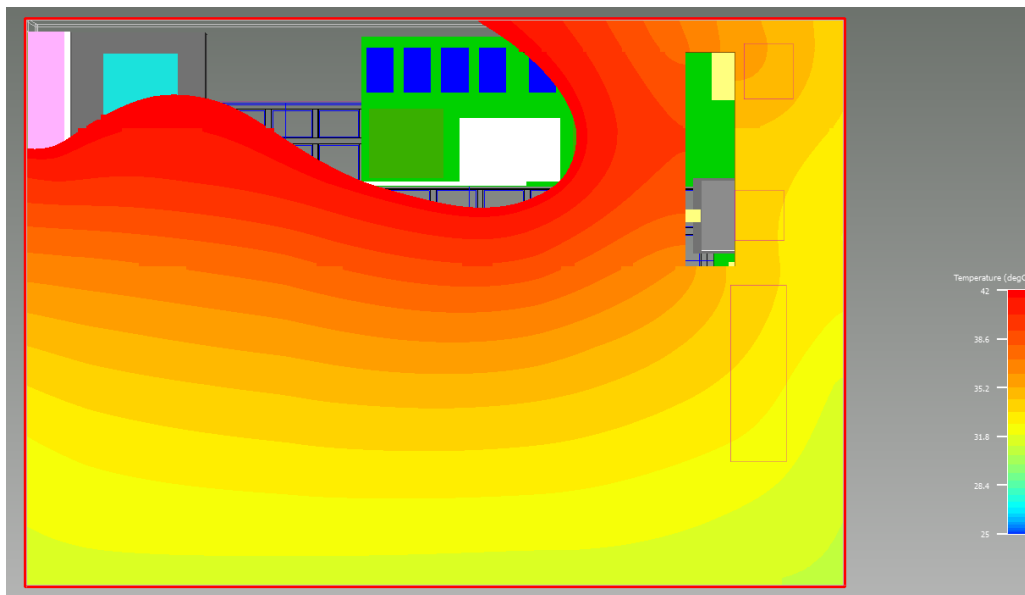### 6.8.8.2.4. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is somewhat dependent on the Adapter dissipation. In addition, the fan flow rate is quite low, so that the casing needs to transfer a larger fraction of the total heat.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 6-43 and Figure 6-44, a region of interest is defined in the vicinity of the Adapters, and the region maximum obtained. Another method might be to track a single consistent point over each Adapter.
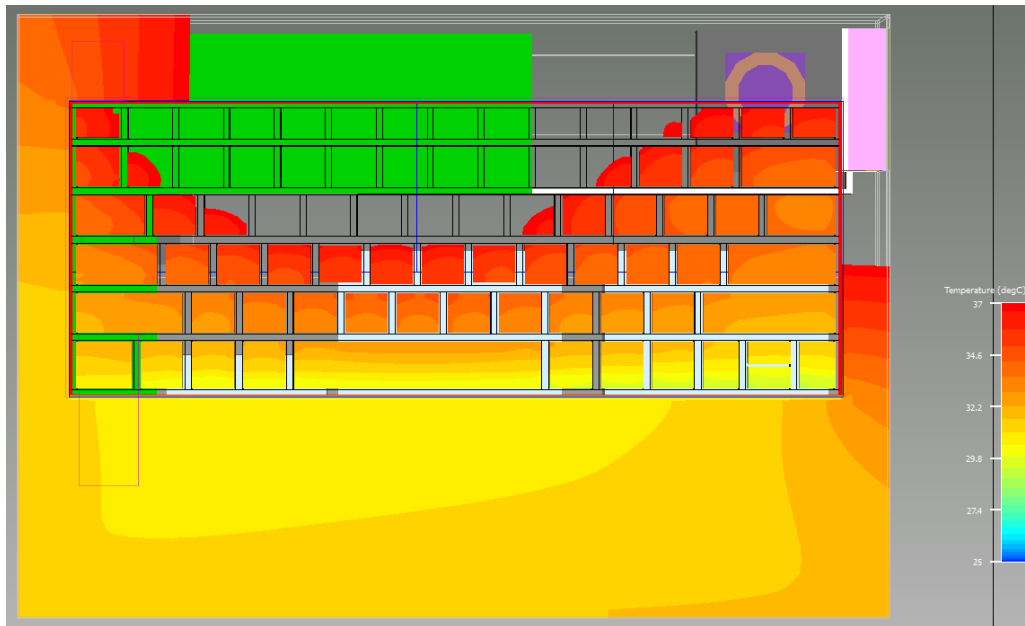
- Rectangles indicate local card areas
- Irregularly unshaded areas indicate surface above the maximum scale temperature
- Note scale corresponds to maximum skin temperature assumptions

Figure 6-43. Example View of Region and Hot Spots Over Adapters

- Rectangles indicate local card areas
- Irregularly unshaded areas indicate surface above the maximum scale temperature
- Note scale corresponds to max skin temperature assumptions

Figure 6-44. Example View of Region and Hot Spots Under Adapters

6.8.8.2.5. Thermal design Power Response – Thin Platform Notebook with Fan Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to ~3+ W in the use case. The results in Table 6-18 and Table 6-19 are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the Adapter) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any Adapter dissipation. Although the Adapters do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide an example of Adapter effects on skin temperature. The flow rate of the fan and particulars of the keyboard model especially determine the skin temperature of Adapters below the keyboard area.

Table 6-18. Thermal Design Power Response – Thin Platform Notebook with Fan Category

	Thin Platform Notebook with Fan				Units
Socket #	1	1	2	3	
Adapter Size	3030	3030	3042	2280	
Function	Wi-Fi/BT + WiGig	Wi-Fi/BT + WiGig	WWAN	SSD	
Use Case	Comms exc	Comms exc 50% power	Comms exc WWAN	Platform Chipset exc	
Sys Dissipation W/O Adapter	19.4	9.7	19.4	21	W
Adapter Off	0	0	0	0	W
WMean Card T	42	31	38	33	°C
Local Skin T Top	33	29	34	32	°C
Local Skin T Bottom	32	29	32	33	°C
Global Skin Hot Spot (HX)	46	36	47	47	°C
Use Case TDP	1.4	0.7	1.4	2.4	W
Local Skin T Top	35	30	39	37	°C
Local Skin T Bottom	36	30	36	38	°C
Global Skin Hot Spot	47	37	48	49	°C
Extended Case TDP	3	3	3	3	W
Local Skin T Top	38	35	41	39	°C
Local Skin T Bottom	38	36	37	39	°C
Fan Flow Rate	0.6	0.6	0.6	0.6	cfm

Table 6-19. Skin Temperature Limit Assumptions, Thin Platform Notebook with Fan

	Value	Units
Ext Ambient	25	°C
Skin T Limit Top	37	°C
Skin T Limit Bottom	42	°C

6.8.8.3.   Tablet without Fan Category

Many assumptions are used in this document. Table 6-20 lists the use cases applicable to Adapters for tablet without fan.

Table 6-20.   Use Cases Applicable to Adapters for Tablet without Fan

Component Dissipation (W)	Estimate I Skype—Over 3G Steady State	Estimate II Skype + 19x10 Display + 3G	Units
SOC Package	1.16	1.5	W
POP Memory (2 GB)	0.29	0.4	W
3G Comms	0.80	1.4	W
Camera	--	0.25	W
Storage (eMMC)	0.05	--	W
PMIC	0.86	0.7	W
Audio LPE	0.05	0.1	W
MIPI to LVDS	0.13	--	W
Display (10", 200 nits)	2.46	1.935	W
Battery Discharge	0.14	0.1	W
Others (system VR, LEDs, etc.)	0.43	0.1	W
Platform Total	6.37	6.485	W

6.8.8.3.1. Generic Motherboard Assumptions

The bottom view of a single-sided motherboard (all components facing the back within the system) is shown in Figure 6-45. The cards are installed in Mid-mount connectors at one edge of the U-shaped board. There are several memory Adapters, a power management IC (PMIC), and two areas of clustered individual small heat sources (each shown as a rectangular heated area). The motherboard heat sources form a thermal boundary condition for the Adapters.
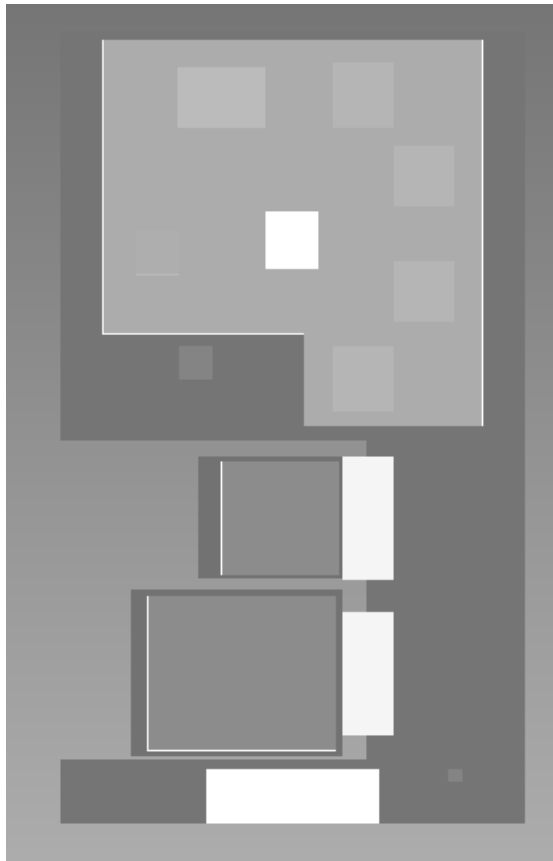

Figure 6-45. Example View of Tablet Motherboard

6.8.8.3.2. System Layout Assumptions

It is assumed that there is neither a fan nor venting in a tablet—a high emissivity surface has been assumed on the outside surface of the magnesium enclosure. In addition, the heat spreader under the backlight assembly is 0.2 mm thick copper since copper will reduce the hot spot compared to an aluminum spreader.

The motherboard is centrally located, between banks of batteries. This arrangement allows the heat to spread in all directions; concentrating heat sources in a corner restricts their heat spreading ability (see Figure 6-46).
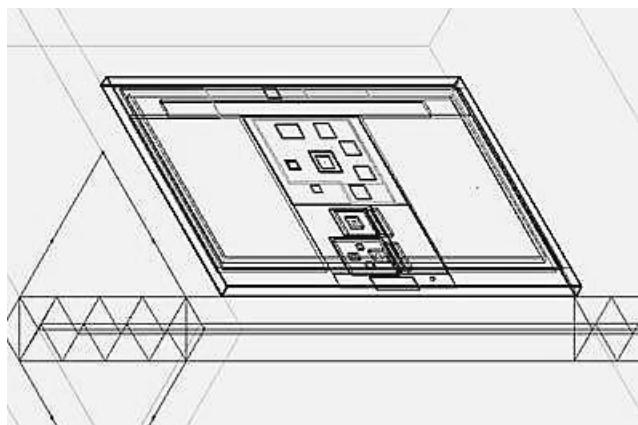
Figure 6-46. Example View of System Layout, Including Table

6.8.8.3.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. The global maximum is likely to be over the main dies (SoC and PMIC). The temperature in this region is somewhat dependent on the Adapter dissipation, as in this system category it makes up a significant fraction of the total system TDP. As there is no flow at all, the casing needs to transfer all the heat dissipated inside (see Figure 6-47 and Table 6-21).

Local maxima are trickier to identify if they are lower than the global maximum. The global maximum point was chosen because with no ventilation possible, any hot spots interact; all heat must spread and dissipate off the surface.
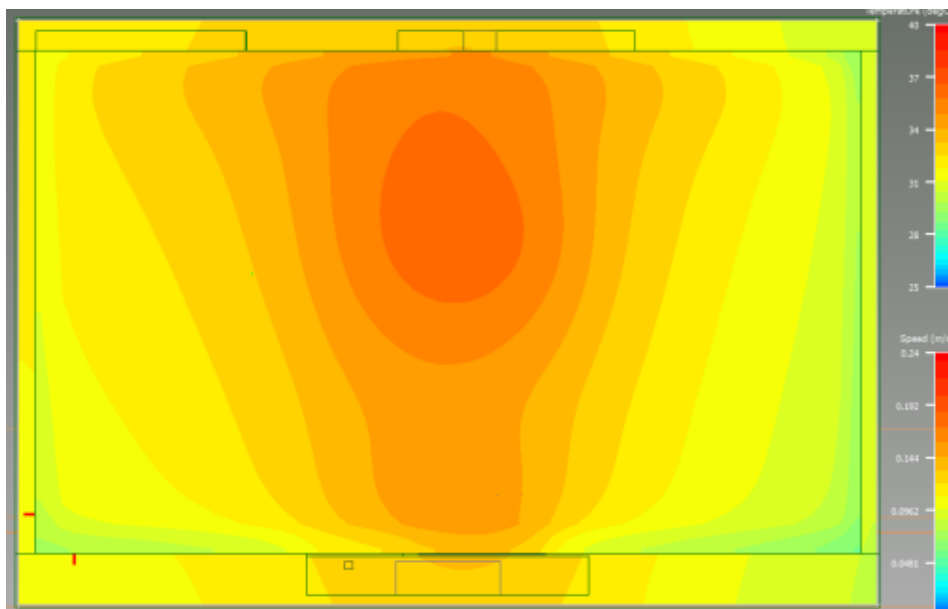
Figure 6-47. Example View of Display Surface Temperature with WWAN Use Case Estimate II

Table 6-21.   Thermal Design Power Response—Tablet Category

	Tablet		Units
Socket #	1	2	
Adapter Size	2230	3042	
Function	Wi-Fi/BT	WWAN LTE	
Use Case	Estimate II		
Sys Dissipation W/O Adapter	5.1	5.1	W
Adapter Off	0	0	W
Mean Card T	31	31	°C
Local Display T	35	35	°C
Max Back T	32	32	°C
Use Case TDP	1.4	1.4	W
Local Display T	37	37	°C
Max Back T	34	34	W
Extended Case TDP	3	3	W
Local Display T	39	38	°C
Max Back T	39	37	°C

6.8.8.3.4. Thermal Design Power Response—Tablet Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to ~3+ W in the use case. Results in the table are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree Celsius.

Also note that with so many assumptions in each analysis, the results shown in Table 6-22 are not intended as accurate predictions, but only to provide an example of Adapter dissipation effects on skin temperature.

Table 6-22. Skin Temperature Limit Assumptions, Tablet without Fan

Ext Ambient	Skin T Limit Display	Skin T Limit Back	Units
25	40	38	°C

6.9. Examples of FULL_CARD_POWER_OFF# Sequences (Informative)

6.9.1. Example of Power On/Off Sequence

Following is an example of a full-card power On/Off sequence:

1. Modem power on:
   High level will trigger modem power on sequence.

2. Modem power off:
   The modem is powered off first via an AT command, subsequently there is a handshaking between host and modem.

3. FULL_CARD_POWER_OFF# pin will turn to LOW level or Tri-state to shutdown modem's PMU.

6.9.2. Example of Tablet Power On/Off Sequence

The following example sequences are for illustrative purposes only, as Adapter vendors offers alternate solutions and requirements.

1. Battery always connected to modem.

2. Host triggers GPIO to High on the FULL_CARD_POWER_OFF# pin.

3. Modem turns On.

4. Host issue AT command to switch off modem.

5. Handshaking between modem and host.

6. Host sets GPIO to LOW (or Tri-state) on FULL_CARD_POWER_OFF# pin which will switch off modem PMU.

6.9.3.   Shutdown Handshaking Process

Following is the proper Shutdown Handshaking Process.

1. PC Host sends AT+CFUN=0 to Modem.

2. Modem responds OK.
   Modem will do the essential shutdown tasks before sending OK:
   a) Proper detaching from cellular network.
   b) SW clean up functions, saving necessary NVM parameters and etc.
   c) Activate SIM/EBU shutdown sequences.
   d) Above task may need few milliseconds to couple of seconds depending on the state of the modem.

3. Modem sends OK to AP upon completion of essential tasks.

4. If AP receives ERROR, it should try again for AT+CFUN=0.

5. Modem completes PMU power off sequences/register access after sending OK.
   The following process takes less than one second:
   a) Disable all regulators (except VPMU and VRTC LDOs).
   b) Assert reset signals.
   c) Release the 26 MHz system clock request signal.

6. AP cuts off power supply or pull-on/off pin LOW /Tri-state after fixed delay of one second.
   In a rare case, if AP did not receive any response within _*_ seconds of issuing AT+CFUN=0, AP will assume that it is OK. There may be times when USB may be over loaded and by the time it is ready to send OK, the driver shutdown will already have started and OK may not reach AP.

> **Note:** *The response time _*_ is to be decided by the host.

6.9.4.   Example of Very Thin Notebooks Power On/Off Sequence

Very thin notebooks do not use the FULL_CARD_POWER_OFF# signal. Following is the power On/Off sequence example for very thin notebooks:

1. Modem gets 3.3 V once the Platform switches on the 3.3 V Always On supply for the modem.

2. Modem turns On since the FULL_CARD_POWER_OFF# pin is pulled   high by the host (pin 6 connected to 1.8 V or 3.3 V).

3. Host issues AT command to switch off modem.

4. Handshaking between modem and host. Once the handshake has been complete, the host is permitted to shut off supply to the modem.

6.10. Socket 2 Key C - Vendor Defined Pinout Examples

Table 6-23 lists examples of Vendor Defined pinouts for Adapters.

Table 6-23.   Socket 2 Key C - Vendor Defined Pinout Examples

Pin	Pin Name in Pinout	Generic Example	Example 1	Example 2
63	VENDOR_PORT_C_3 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO2 I2S_WS (I/O) (0/1.8V)	IPC_5 (I/O) (0/1.8V)
61	VENDOR_PORT_C_2 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO2 I2S_TX (O) (0/1.8V)	SERIAL S/B DATA_TX (O) (0/1.8V)
57	VENDOR_PORT_C_1 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO2 I2S_RX (I) SLIMBUS_DAT (I/O) (0/1.8V)	SERIAL S/B DATA_RX (I) (0/1.8V)
55	VENDOR_PORT_C_0 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO2 I2S_CLK (I/O) SLIMBUS_CLK (I/O) (0/1.8V)	SERIAL S/B CLK (I) (0/1.8V)
60	VENDOR_PORT_B_5 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	FINE TIME ADJUSTMENT (O) (0/1.8V)	IPC_7 (I/O) (0/1.8V)
58	VENDOR_PORT_B_4 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	TX_BLANKING (O) (0/1.8V)	IPC_6 (I/O) (0/1.8V)
54	VENDOR_PORT_B_3 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	SYSCLK (O) (0/1.8V)	IPC_4 (I/O) (0/1.8V)
52	VENDOR_PORT_B_2 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_IRQ (O) (0/1.8V)	IPC_3 (I/O) (0/1.8V)
50	VENDOR_PORT_B_1 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_SDA (I/O) (0/1.8V)	IPC_2 (I/O) (0/1.8V)
48	VENDOR_PORT_B_0 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_SCL (I) (0/1.8V)	IPC_1 (I/O) (0/1.8V)
14	VENDOR_PORT_A_3 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)
12	VENDOR_PORT_A_2 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)
10	VENDOR_PORT_A_1 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	LED_1# (O) (OD)	VENDOR DEFINED (I/O) (0/1.8V)
8	VENDOR_PORT_A_0 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	W_DISABLE# (I) (0/1.8V)	IPC_0 (I/O) (0/1.8V)

Pin	Pin Name in Pinout	Example 3	Example 4	Example 5
63	VENDOR_PORT_C_3 (Top)	UART_TXD (O) (0/1.8V)	#2 M/PERp0; SSIC-RxP; USB3.1-Rx+	#2 M/PERp0; SSIC-RxP; USB3.1-Rx+
61	VENDOR_PORT_C_2 (Top)	UART_RTS (O) (0/1.8V)	#2 M/PERn0; SSIC-RxN; USB3.1-Rx-	#2 M/PERn0; SSIC-RxN; USB3.1-Rx-
57	VENDOR_PORT_C_1 (Top)	UART_RXD (I) (0/1.8V)	#2 M/PETp0; SSIC-TxP; USB3.1-Tx+	#2 M/PETp0; SSIC-TxP; USB3.1-Tx+
55	VENDOR_PORT_C_0 (Top)	UART_CTS (I) (0/1.8V)	#2 M/PETn0; SSIC-TxN; USB3.1-Tx-	#2 M/PETn0; SSIC-TxN; USB3.1-Tx-
60	VENDOR_PORT_B_5 (Bottom)	FINE TIME ADJUSTMENT (O) (0/1.8V)	FINE TIME ADJUSTMENT (O) (0/1.8V)	#2 M/REFCLKP
58	VENDOR_PORT_B_4 (Bottom)	TX_BLANKING (O) (0/1.8V)	TX_BLANKING (O) (0/1.8V)	#2 M/REFCLKN
54	VENDOR_PORT_B_3 (Bottom)	SYSCLK (O) (0/1.8V)	SYSCLK (O) (0/1.8V)	#2 PEWAKE# (I/O) (0/1.8V)
52	VENDOR_PORT_B_2 (Bottom)	GNSS_IRQ (O) (0/1.8V)	GNSS_IRQ (O) (0/1.8V)	#2 CLKREQ# (I/O) (0/1.8V)
50	VENDOR_PORT_B_1 (Bottom)	GNSS_SDA (I/O) (0/1.8V)	GNSS_SDA (I/O) (0/1.8V)	#2 PERST# (I) (0/1.8V)
48	VENDOR_PORT_B_0 (Bottom)	GNSS_SCL (I) (0/1.8V)	GNSS_SCL (I) (0/1.8V)	SERIAL S/B CLK (I) (0/1.8V)
14	VENDOR_PORT_A_3 (Bottom)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)
12	VENDOR_PORT_A_2 (Bottom)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)
10	VENDOR_PORT_A_1 (Bottom)	LED_1# (O) (OD)	LED_1# (O) (OD)	SERIAL S/B DATA_TX (O) (0/1.8V)
8	VENDOR_PORT_A_0 (Bottom)	W_DISABLE# (I) (0/1.8V)	W_DISABLE# (I) (0/1.8V)	SERIAL S/B DATA_RX (I) (0/1.8V)

6.11. High Speed Differential Pair AC Coupling Capacitor Values and Capacitor Location Examples

This section summarizes the defined High-Speed Differential Pair AC Coupling Capacitor values and illustrate examples of where the AC Coupling Capacitors must be located based on the definitions outlined in the following document:

❑   PCI Express Base Specification

❑   PCI Express Card Electromechanical (CEM) Specification

❑   Universal Serial Bus Specification, Revision 3.1

❑   Serial ATA Specification

This chapter does not cover the SATA-IO DC Coupled scheme referred to as DC coupled Gen1i.

The content of this section is for information only. For detailed information, refer the original specifications listed in Section 1.3.

6.11.1. AC Coupling Capacitor Values Per Respective Specification Definitions

The PCIe and USB3.1 specifications call out for the AC Coupling Capacitor values as a function of interface signal transmission rate (e.g., Gen Speed).

PCIe and USB3.1 call out for AC Coupling Capacitor values given in Table 6-24 and Table 6-25 respectively. Table 6-26 lists the SATA-IO specification call outs for AC Coupling Capacitor values. Note that the SATA-IO specification calls out for AC Coupling Capacitor for both RX and TX.

Table 6-24.   PCIe AC Coupling Capacitor Values

Designation	Description	Gen1	Gen2	Gen3	Units
C_{TX}	AC Coupling Capacitor	75 (Min) 265 (Max)	75 (Min) 265 (Max)	176 (Min) 265 (Max)	nF

Table 6-25.   USB3.1 AC Coupling Capacitor Values

Designation	Description	Gen1	Units
C_{TX}	AC Coupling Capacitor	75 (Min) 200 (Max)	nF

Table 6-26.   SATA-IO AC Coupling Capacitor Values

Designation	Description	Gen1/2/3	Units
C_{TX}	AC Coupling Capacitor	12 (Max)	nF
C_{RX}	AC Coupling Capacitor	12 (Max)	nF

6.11.2.   AC Coupling Capacitor Location Examples

The PCIe, USB3.1, and SATA-IO specifications all call out for the need to incorporate AC Coupling Capacitors on the high-speed differential signals.

6.11.2.1.   PCIe and USB3.1 AC Coupling Capacitor Location Examples

The PCIe and USB3.1 specifications call out for the AC Coupling Capacitors to be located adjacent to the Transmitter. However, the specifications distinguish between two basic cases:

❑   Pluggable Add-in Card

❑   All On the Same Board

For the Pluggable Add-in Card, the specification clearly indicates that AC Coupling Capacitors must be placed on the Transmitter side of an interface that permits adaptors to be plugged and unplugged. Visually, this is shown in Figure 6-48. This convention is applicable to all the connectorized/pluggable M.2 form factors.
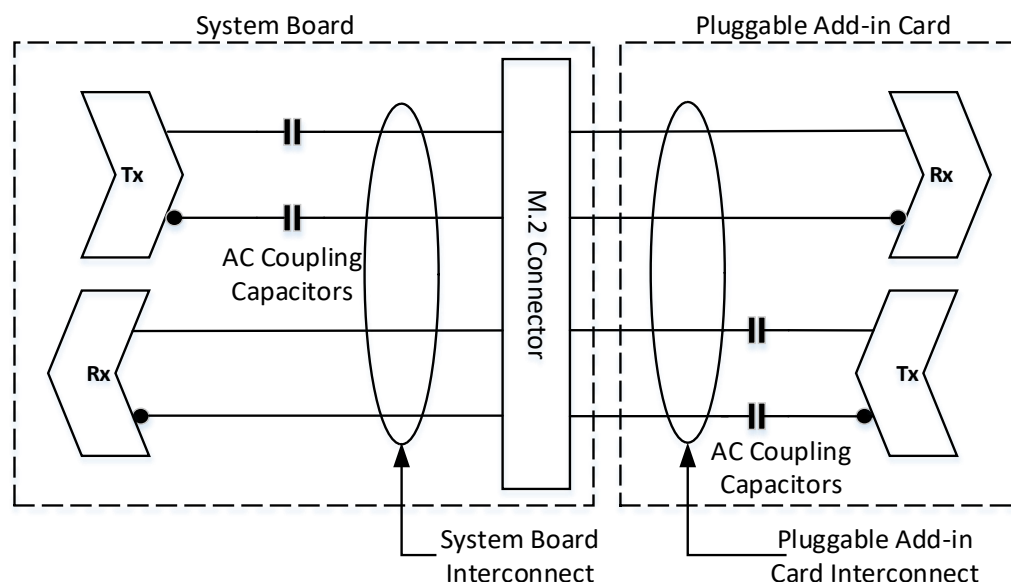
Figure 6-48.   AC Coupling Capacitor Location – PCIe and USB3.1 Pluggable Add-in Card Example

Due to the integrated component nature of the M.2 family of LGA soldered down Modules, this pluggable Add-in Card convention should also be applied to the M.2 Type 1216, Type 2226, and Type 3026 soldered down Modules even though there is not an actual connector. In this case the LGA footprint on the system board shows the connection point. The AC Coupling Capacitors are adjacent to the transmitters with a set on the system board interconnect near the transmitter and a set on the LGA module interconnect near its transmitter, as shown in Figure 6-49.
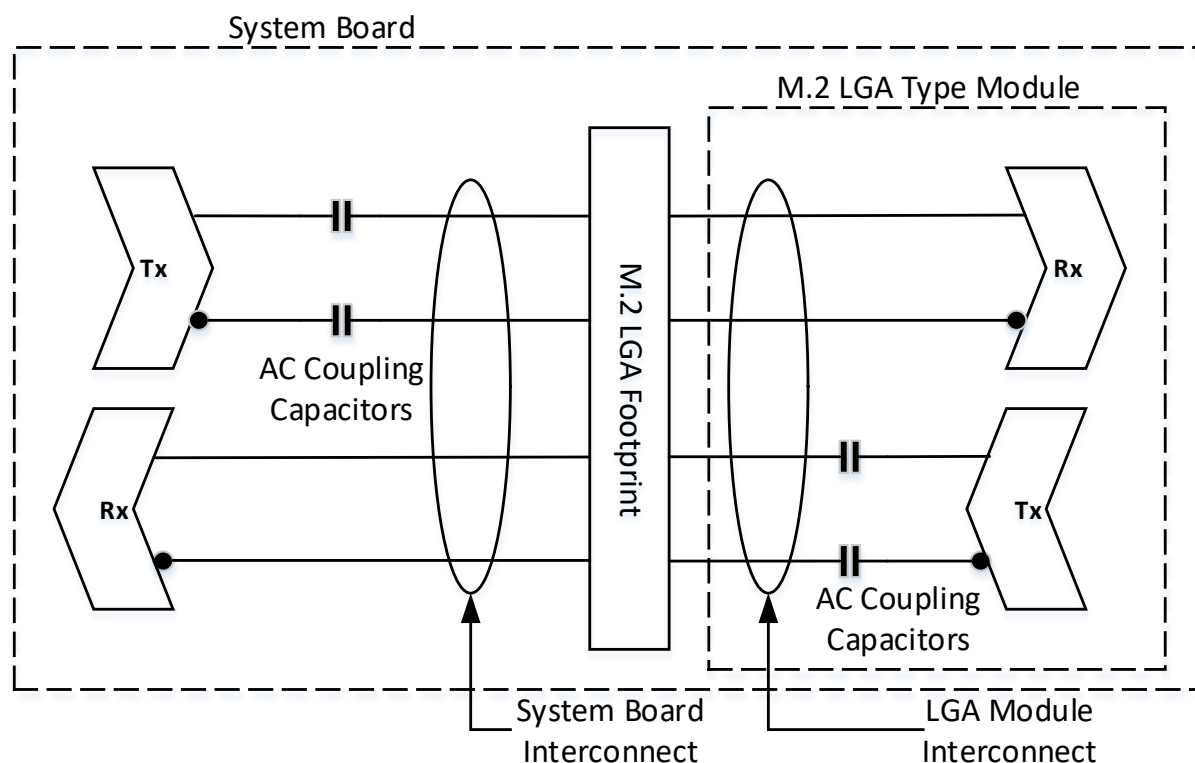
Figure 6-49. AC Coupling Capacitor Location – Soldered Down LGA Module on System Board Example

For the All-On-Same-Board case, the PCIe and USB3.1 specifications indicate that when both the transmitters and both receivers are all on the same board, the AC Coupling Capacitors are permitted to be placed anywhere along the signal lines. This definition is applicable to the M.2 family of SSD BGA Packaged devices. In this case, the AC Coupling Capacitors need to be somewhere along the signals paths as shown in Figure 6-50.
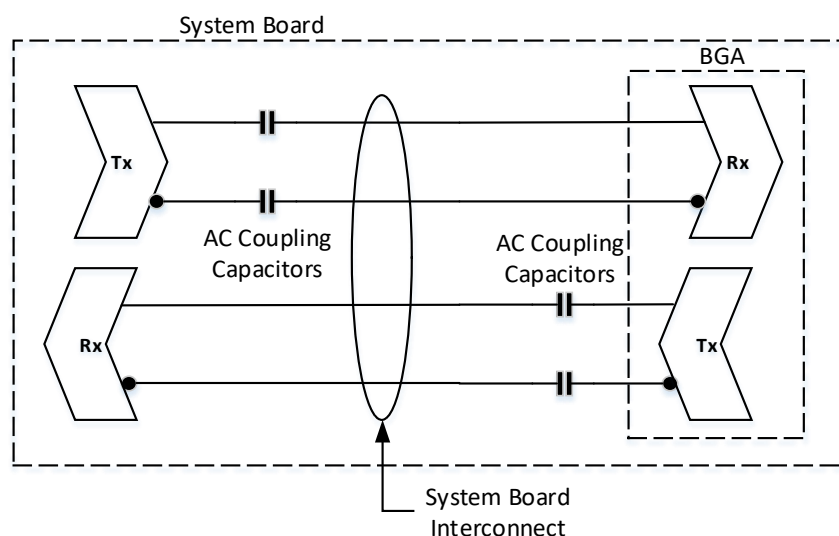
Figure 6-50. AC Coupling Capacitor Location – All-On-Same-Board Example

When an M.2 SSD BGA package device is mounted on an M.2 pluggable form factor, then the Pluggable Case should be applied. In this case, the AC Coupling Capacitor pair will be near the system board transmitter and the other pair will be on the M.2 Add-in Card on which the M.2 SSD BGA package is mounted, as shown in Figure 6-51. Since these are High Speed Differential Pair signals, it is highly recommended that Differential Line layout design rules be applied to the traces and the AC Coupling Capacitor for optimal signal integrity.
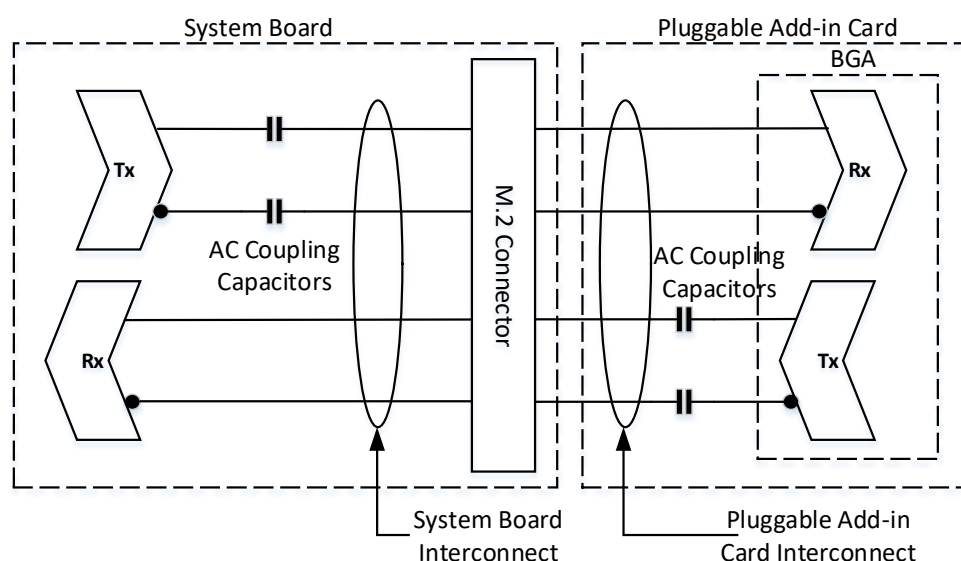
Figure 6-51. AC Coupling Capacitor Location - SSD BGA on Pluggable M.2 Form Factor Example

6.11.2.2.   **SATA-IO AC Coupling Capacitor Location Examples**

It should be noted that the SATA-IO specification defines the location of the AC Coupling Capacitors differently compared with the PCIe and USB3.1 specifications. The SATA-IO calls for all the AC Coupling Capacitors to be placed on the Add-in Card. When applying this to the M.2 connection scheme, as shown in Figure 6-52.
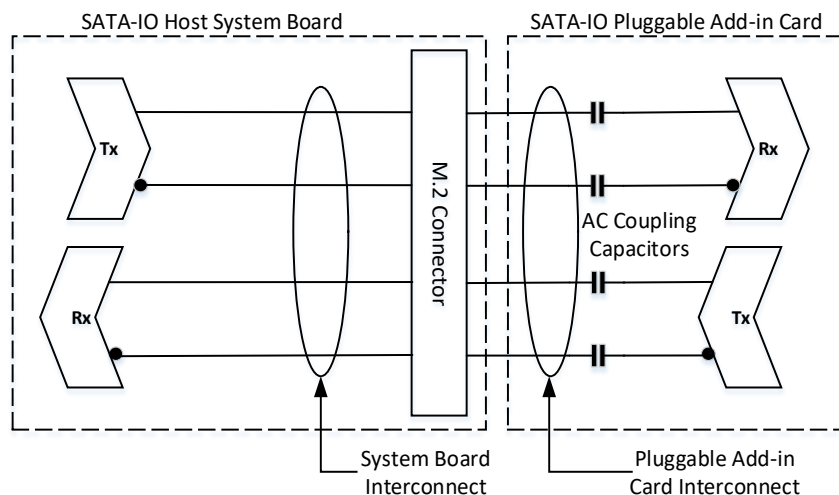
Figure 6-52.   SATA-IO AC Coupling Capacitor Location – SATA Pluggable Add-in Card Example

Based on this convention, when an SSD BGA package is mounted on an M.2 Add-in Card form factor, the AC Coupling Capacitors are located on the pluggable Add-in Card but off the SSD BGA Package (see Figure 6-53).
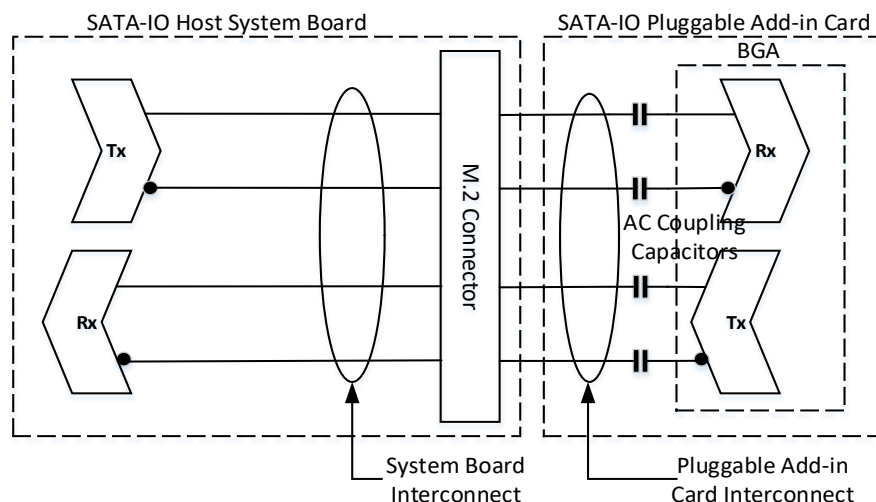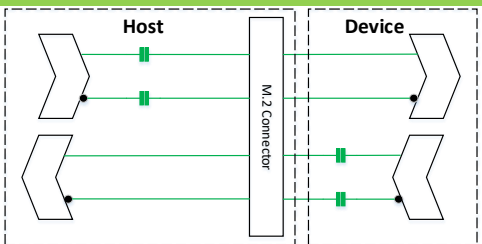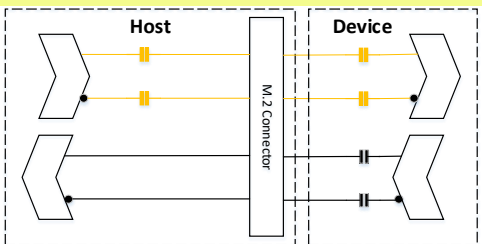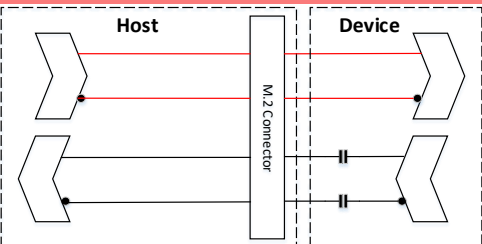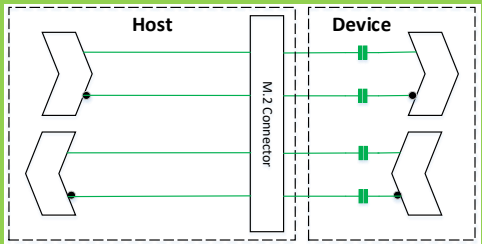
Figure 6-53.   SATA-IO AC Coupling Capacitor Location - SSD BGA On Pluggable Add-in Card Example

6.11.3. AC Coupling Capacitor Scheme Compatibility Matrix

It is recommended that Host and Device AC Coupling Capacitor schemes match each other per the appropriate specification. SATA-IO and PCIe AC Coupling schemes differ from each other. System Board maybe designed to support PCIe and SATA-IO pluggable Add-in Cards.

The matrix given in Table 6-27 shows the potential compatibilities and incompatibilities for all combinations.

Table 6-27. AC Coupling Capacitor Scheme Compatibility Matrix

[1] Electrically, this case has two capacitors in series yielding a total capacitance which is still within SATA-IO specifications. However, the side-effects of serial capacitors may affect optimal signal integrity.

[2] DC coupling makes this incompatible for the both SATA-IO and PCIe/USB3.1.

6.12. Eye Limits for SSIC at the M.2 Connector

Transmitter Eye Height and Eye Width limits at the M.2 connector for the SSIC Host and the SSIC Device transmitter are defined in Table 6-28. This helps to test the interoperability between SSIC host and SSIC device at the M.2 connector. The eye diagrams are evaluated after the behavioral CDR defined in the *PHY Test Specification* is applied. The eye limits given in Table 6-28 are recommendations only.

Table 6-28. SSIC Transmitter Eye Limits at the Connector

	Eye Height at M.2 Socket	Eye Width at M.2 Socket	Notes
SSIC Device Transmitter	140 mV	0.61 UI$_{HS}$	1 to 6
SSIC Host Transmitter	95 mV	0.55 UI$_{HS}$	1 to 6

Notes:

1. Assumes the signal has been captured using a break-out fixture that is approximately 1-inch long (approximately -0.33 dB loss at 1.455 GHz).
2. The recommended sample size for this measurement is at least 10^6 UI.
3. Eye measurements require that CRPAT (refer to *MIPI Alliance Specification for M-PHY*) is being transmitted during the test.
4. The measurements are applicable to Terminated HS mode of MPHY.
5. The Eye Width limits are applicable at Target BER of 10^{-10}.
6. The eye limits are applicable to the MPHY HS gears G1, G2, and G3.

A

Appendix A. Acknowledgments

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In Memoriam

This specification is dedicated to the memory of Marc Noblitt and Ed Poh, friends and colleagues of many past and present members of this committee. Marc and Ed were key contributors to this specification and to many other industry efforts to which both were actively engaged. They will be missed.