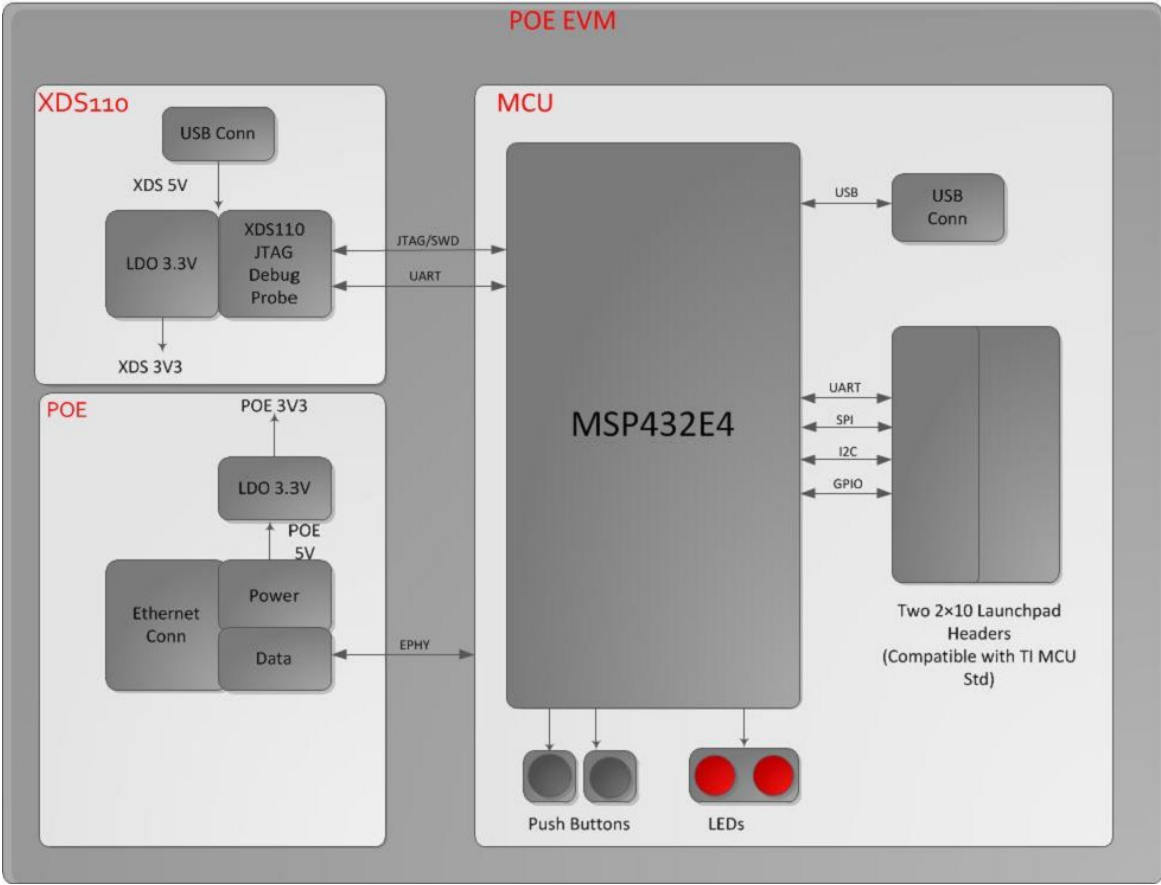


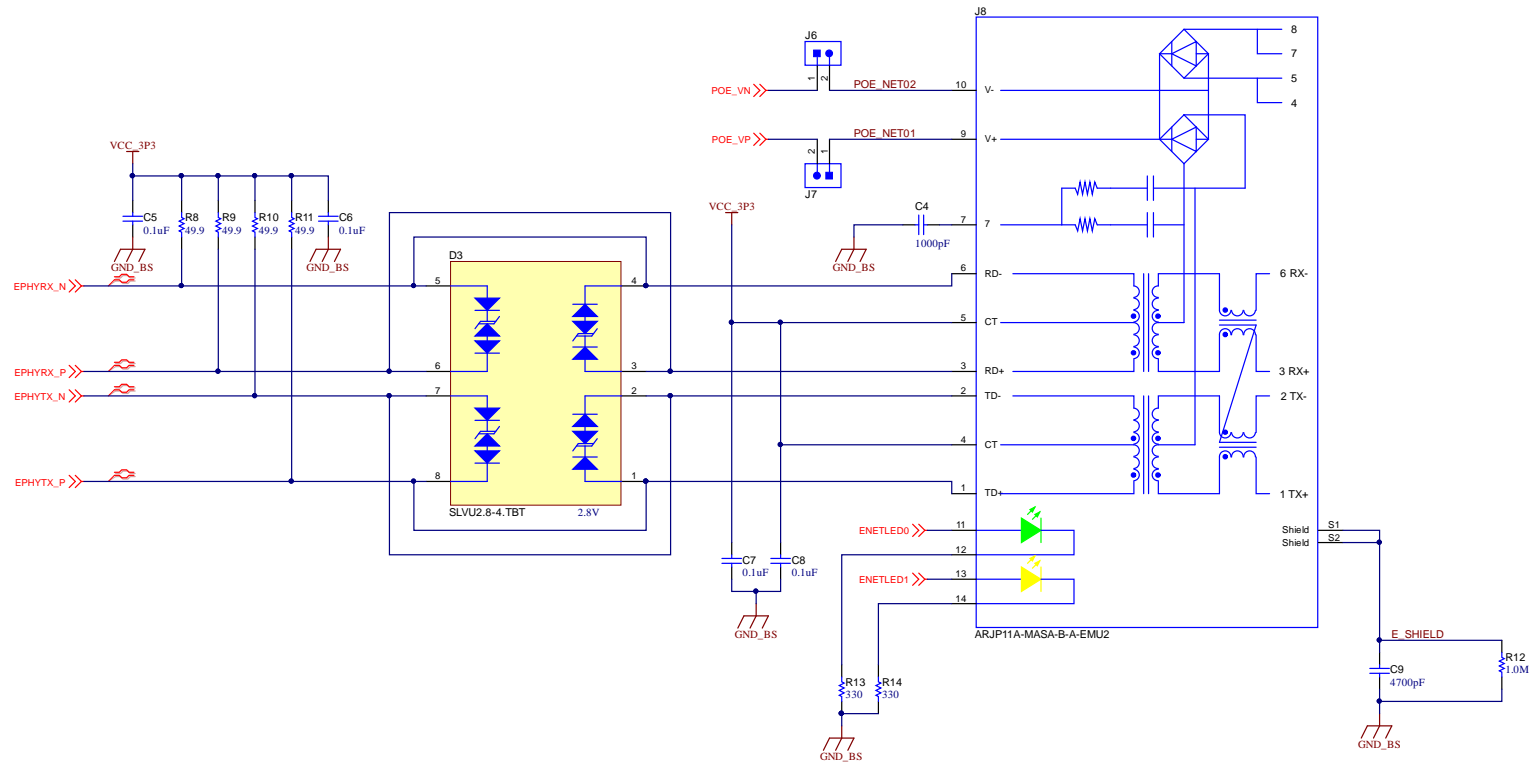
TABLE OF CONTENTS


SHEET NO.	SHEET NAME
1	Table of Contents
2	Block diagram
3	Micro
4	Ethernet
5	Power Stage
6	Connectors
7	XDS110 Debug Probe
8	XDS110 Target Interface
9	XDS110 USB Power
10	EVM Hardware

Block Diagram



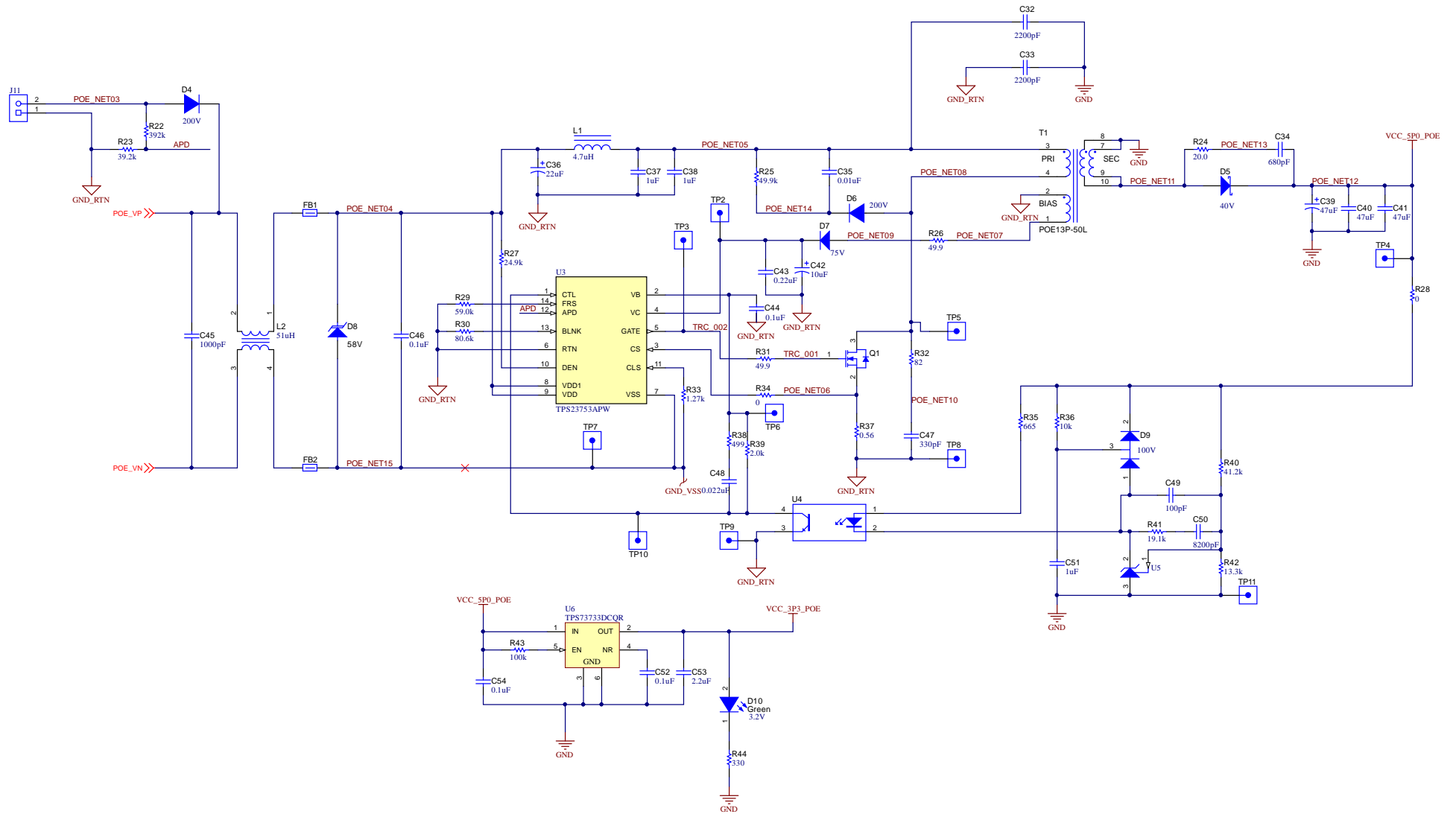
ETHERNET



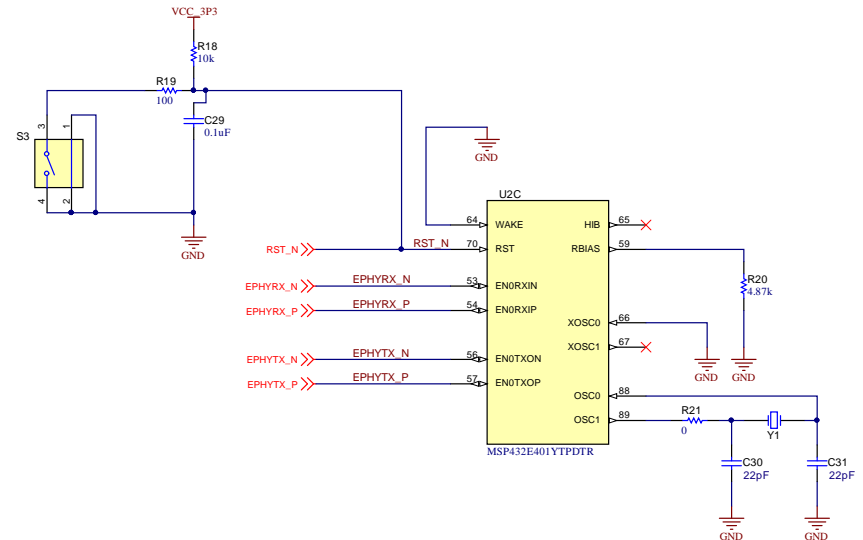
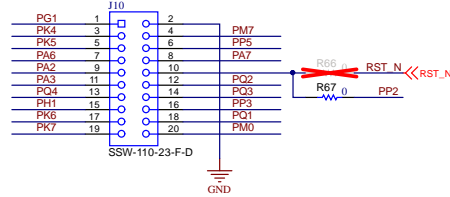
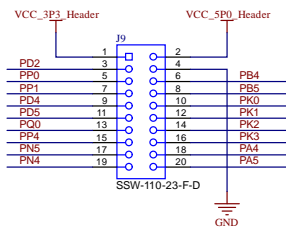
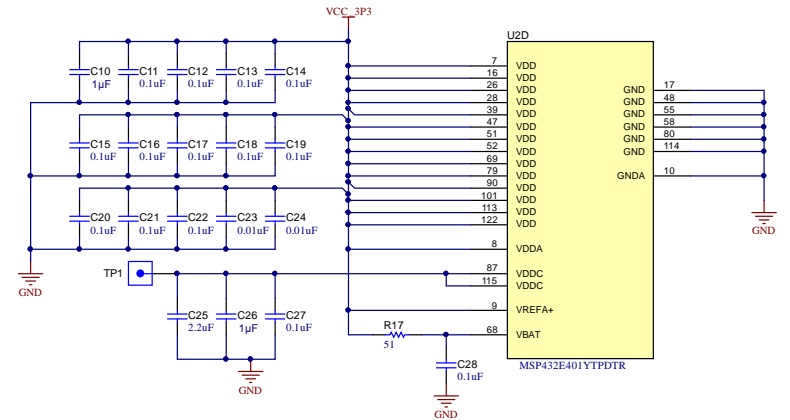
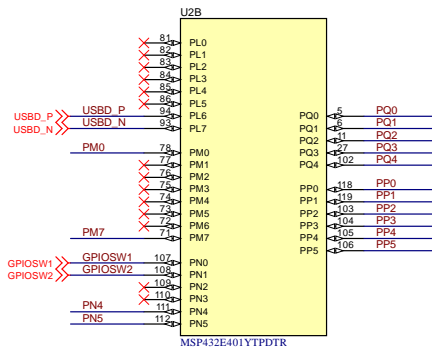
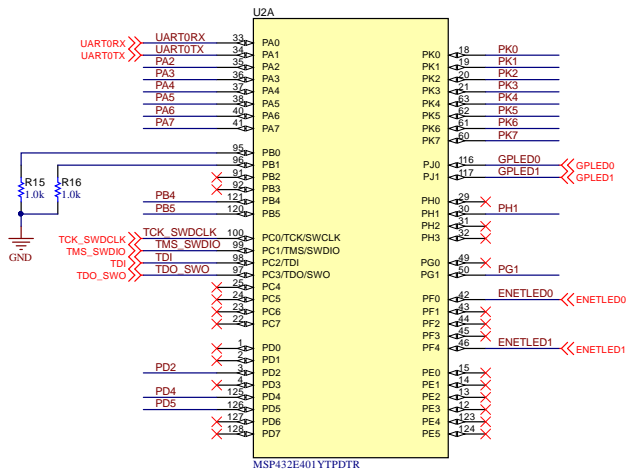
Orderable: MMWAVE0PE0VM	Designed for: Public Release	Mod. Date: 10/21/2018
TID #: N/A	Project Title: MMWAVE0PE0VM	 TEXAS INSTRUMENTS
Number: PROC0076 Rev: A	Sheet Title: Ethernet	
Version: Rev: Not in version control	Assembly Variant: 001	
Drawn by: Charles Oladimeji	File: PROC0076A Ethernet_SchDoc	
Checker: Charles Oladimeji	Contact: http://www.ti.com/support	Sheet: 3 of 10 Size: B
		http://www.ti.com © Texas Instruments 2018

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

POWER STAGE



MICRO



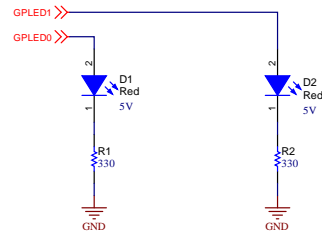
Orderable: MMWAVEPOEEVM	Designed for: Public Release	Mod. Date: 10/21/2018
TID #: N/A	Project Title: MMWAVEPOEEVM	
Number: PROC076	Rev: A	Sheet Title: Micro
SWID Rev: Not in version control	Assembly Variant: 001	Sheet: 5 of 10
Drawn By: Charles Oladimeji	File: PROC076A_Micro_SchDoc	Size: B
Engineer: Charles Oladimeji	Contact: http://www.ti.com/support	



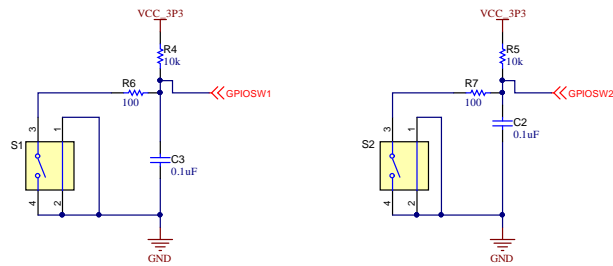
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

CONNECTOR

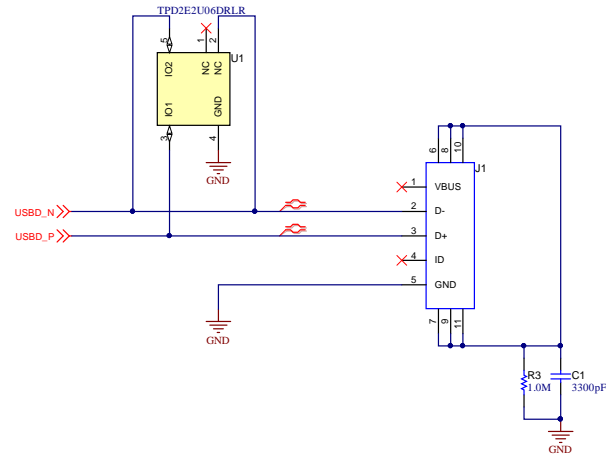
LED



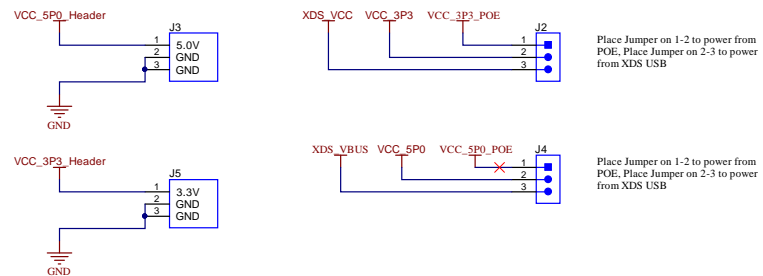
Switches



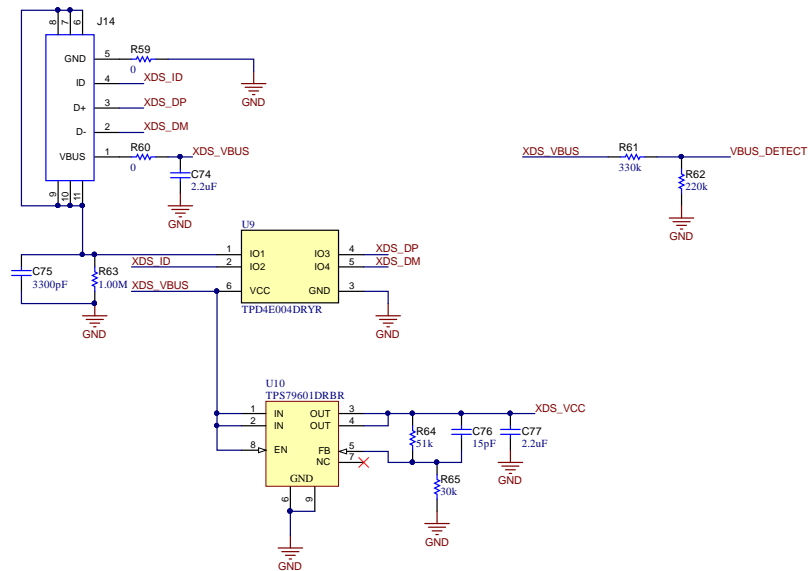
USB Connector



Power Headers



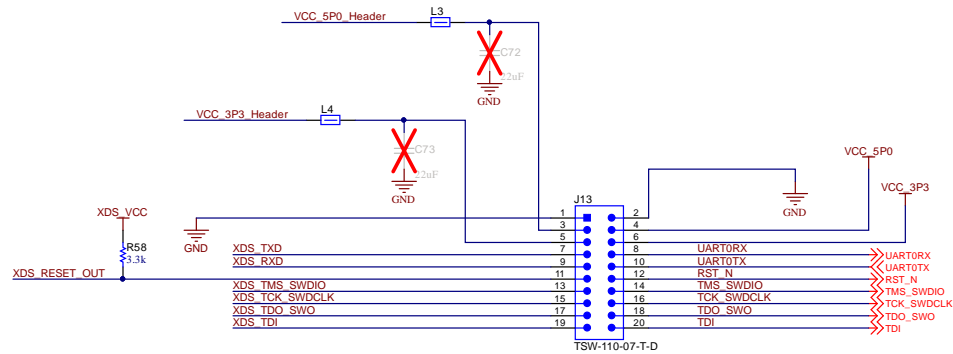
XDS110 USB POWER



[illegible]

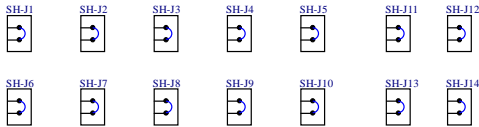
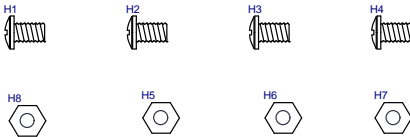
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors warrant that this design will meet the specifications, will be suitable for your application or for any other particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

XDS110 TARGET INTERFACE



EVM HARDWARE

Variant/Label Table	
Variant	Label Text
001	MMWAVEPOEEVM



PCB Number: PROC076
PCB Rev: A

PCB
LOGO
Texas Instruments

PCB
LOGO
ESD Susceptible

PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo



LBL1
PCB Label



CAUTION HOT SURFACE

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

2

FAB NOTES:

1. THE SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED AS PER THE MANUFACTURING CAPABILITIES BUT NOT BEYOND 0.08MM PER SIDE OR 0.15MM OVERALL. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE MODIFIED.
2. TOP LAYER 4.99 MIL WIDE, 6.01 MIL SPACE TRACES REQUIRE 90 OHM +/-10% DIFFERENTIAL IMPEDANCE
3. EXTERNAL LAYER 5.01 MIL WIDE, 8.99 MIL SPACE TRACES REQUIRE 100 OHM +/-10% DIFFERENTIAL IMPEDANCE.

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

D