LP5867 7 × 6 LED マトリクス ドライバ、8 ビット アナログおよび 8/16 ビット PWM 調光付き

1 特長

- LED マトリクスのトポロジ:
  - 42 の LED ドットに対する 7 のスキャン スイッチを備えた 6 個の定電流シンク
  - 1～7 に構成できるスキャン スイッチ
- 動作電圧範囲:
  - V_{CC}/V_{LED} 範囲:2.7V～5.5V
  - 1.8V、3.3V、5V 互換のロジック ピン
- 6 個の高精度定電流シンク:
  - 電流シンクあたり 0.1mA-50mA (V_{CC} ≥ 3.3V)
  - デバイス間誤差:チャネル電流 = 50mA のとき ±3%
  - チャネル間誤差:チャネル電流 = 50mA のとき ±3%
  - 位相シフトによる過渡電力の平衡化
- 極めて低い消費電力:
  - シャットダウン モード:I_{CC} ≦ 1µA (EN = Low 時)
  - スタンバイ モード:I_{CC} ≦ 10µA (EN = High かつ CHIP_EN = 0 (データ保持) 時)
  - アクティブ モード:I_{CC} = 4.2mA (標準値)、チャネル電流 = 5mA
- 柔軟な調光オプション:
  - 各 LED ドットを個別にオン / オフ制御
  - アナログ調光法 (電流ゲイン制御)
    - すべての LED ドットに対するグローバル 7 ステップ最大電流 (MC) 設定
    - 3 グループの 7 ビット カラー電流 (CC) RGB 設定
    - 各 LED ドットに対する個別の 8 ビット ドット電流 (DC) 設定
  - 可聴ノイズが発生しない周波数を使った PWM 調光
    - すべての LED ドットに対するグローバル 8 ビット PWM 調光法
    - LED ドットを任意に割り当てるための 3 つのプログラム可能な 8 ビット PWM 調光法グループ
    - 各 LED ドットに対する個別の 8 ビットまたは 16 ビット PWM 調光法
- データ通信量を最小限に抑えるための完全にアドレス指定可能な SRAM
- 個別の LED ドット開放 / 短絡検出
- ゴースト除去および低輝度補償機能
- インターフェイス オプション
  - 1MHz (最大値) の I^2C インターフェイス (IFS = Low 時)
  - 12MHz (最大値) の SPI インターフェイス (IFS = High 時)

2 アプリケーション

- LED アニメーションおよび表示:
  - 携帯電子機器
  - ウェアラブル
  - モノのインターネット (IoT)

3 概要

電子機器がスマート化するにつれて、アニメーションと表示のためにより多くの LED を使う必要性が高まっており、小さなソリューション サイズでユーザー体験を向上させる高性能 LED マトリクスドライバが求められています。

LP5867 は、高性能の LED マトリクス ドライバです。本デバイスは N × 6 の LED ドットまたは N × 2 の RGB LED をサポートするための N 個 (N = 7) のスイッチング MOSFET を備えた 6 個の定電流シンクを内蔵しています。LP5867 は、最大 42 の LED ドットまたは 14 の RGB LED のための 7 の MOSFET を内蔵しています。

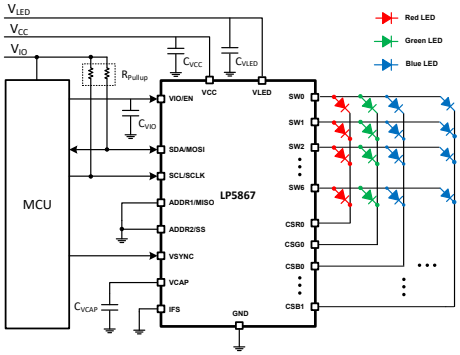
LP5867 はアナログ調光法と PWM 調光法の両方をサポートしています。アナログ調光法の場合、各 LED ドットを 256 ステップで調整できます。PWM 調光法の場合、内蔵の 8 ビットまたは 16 ビット構成可能 PWM ジェネレータが、滑らかで可聴ノイズの発生しない調光制御を実現します。各 LED ドットを 8 ビット グループ PWM に任意に割り当てることで、調光制御をまとめて行うこともできます。

LP5867 デバイスは、データ通信量を最小限に抑えるために、完全にアドレス指定可能な SRAM を実装しています。上側と下側のゴーストを除去するため、ゴースト キャンセル回路を内蔵しています。LP5867 は LED 開放 / 短絡検出機能もサポートしています。LP5867 では、1MHz (最大値) の I^2C と 12MHz (最大値) の SPI が使用できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
LP5867	YBH (DSBGA、24)	2.55mm × 1.80mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図

Table of Contents

4 Device Comparison

PART NUMBER	MATERIAL	LED DOT NUMBER	MAX CURRENT PER CS	PACKAGE(2)	SOFTWARE COMPATIBLE
LP5861T	LP5861TRSMR	18 × 1 = 18	125mA	VQFN-32	Yes
	LP5861TMRSMR(1)				
LP5866T	LP5866TRKPR	18 × 6 = 108	100mA	VQFN-40	
	LP5866TMRKPR(1)				
LP5868T	LP5868TRKPR	18 × 8 = 144			
	LP5868TMRKPR(1)				
LP5860T	LP5860TRKPR	18 × 11 = 198			
	LP5860TMRKPR(1)				
LP5861	LP5861RSMR	18 × 1 = 18	50mA	VQFN-32	
LP5862	LP5862RSMR	18 × 2 = 36		VQFN-32	
	LP5862DBTR			TSSOP-38	
LP5864	LP5864RSMR	18 × 4 = 72		VQFN-32	
	LP5864MRSMR(1)				
LP5866	LP5866RKPR	18 × 6 = 108		VQFN-40	
	LP5866DBTR			TSSOP-38	
	LP5866MDBTR(1)				
LP5867	LP5867YBHR	6 × 7 = 42		WCSP-24	
LP5868	LP5868RKPR	18 × 8 = 144		VQFN-40	
LP5860	LP5860RKPR	18 × 11 = 198		VQFN-40	
	LP5860MRKPR(1)				

(1) Extended Temperature devices, supporting –55°C to approximately 125°C operating ambient temperature.
(2) The same packages are hardware compatible.

5 Pin Configuration and Functions

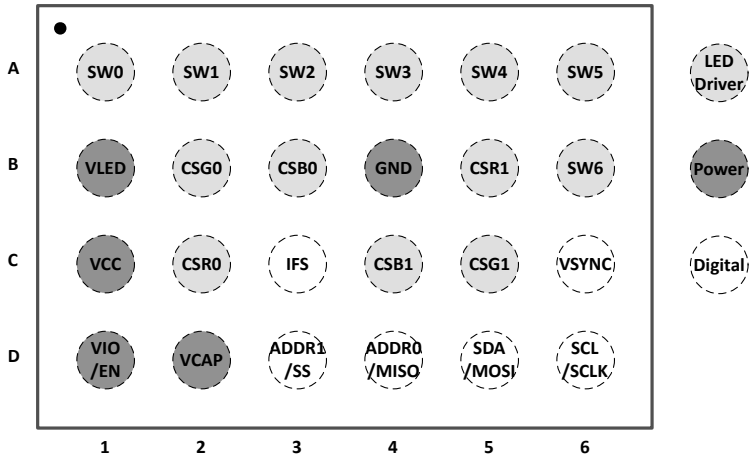


図 5-1. LP5867 YBH Package 24-Pin WCSP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
C2	CSR0	O	Current sink 0. If not used, this pin must be floating.
B2	CSG0	O	Current sink 1. If not used, this pin must be floating.
B3	CSB0	O	Current sink 2. If not used, this pin must be floating.
B5	CSR1	O	Current sink 3. If not used, this pin must be floating.
C5	CSG1	O	Current sink 4. If not used, this pin must be floating.
C4	CSB1	O	Current sink 5. If not used, this pin must be floating.
A1	SW0	O	High-side PMOS switch output for scan line 0. If not used, this pin must be floating.
A2	SW1	O	High-side PMOS switch output for scan line 1. If not used, this pin must be floating.
A3	SW2	O	High-side PMOS switch output for scan line 2. If not used, this pin must be floating.
A4	SW3	O	High-side PMOS switch output for scan line 3. If not used, this pin must be floating.
A5	SW4	O	High-side PMOS switch output for scan line 4. If not used, this pin must be floating.
A6	SW5	O	High-side PMOS switch output for scan line 5. If not used, this pin must be floating.
B6	SW6	O	High-side PMOS switch output for scan line 6. If not used, this pin must be floating.
B1	VLED	Power	Power input for high-side switches.
B4	GND	Ground	Must be connected to common ground plane.
D2	VCAP	O	Internal LDO output. An 1µF capacitor must be connected between this pin with GND. Place the capacitor as close to the device as possible.
C3	IFS	I	Interface type select. I^2C is selected when IFS is low. SPI is selected when IFS is high. A resistor must be connected between VIO and this pin.
C6	VSYNC	I	External synchronize signal for display mode 2 and mode 3.
D6	SCL/SCLK	I	I^2C clock input or SPI clock input. Pull up to VIO when configured as I^2C.
D5	SDA/MOSI	I/O	I^2C data input or SPI leader output follower input. Pull up to VIO when configured as I^2C.
D4	ADDR0/MISO	I/O	I^2C address select 0 or SPI leader input follower output.
D3	ADDR1/SS	I	I^2C address select 1 or SPI follower select.
D1	VIO/EN	Power,I	Power supply for digital circuits and chip enable. An 1nF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
C1	VCC	Power	Power supply for device. A 1µF capacitor must be connected between this pin with GND and be placed as close to the device as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on V_{CC} / V_{LED} / VIO / EN / CS / SW / SDA / SCL / SCLK / MOSI / MISO / SS / ADDR0 / ADDR1 / VSYNC / IFS		–0.3	6	V
Voltage on VCAP		–0.3	2	V
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage on V_{CC}	Supply voltage	2.7		5.5	V
Input voltage on V_{LED}	LED supply voltage	2.7		5.5	V
Input voltage on VIO_EN		1.65		5.5	V
Voltage on SDA / SCL / SCLK / MOSI / MISO / SS / ADDRx / VSYNC / IFS				VIO	V
T_A	Operating ambient temperature	–40		85	°C
T_A	Operating ambient temperature - LP5860TMRKPR, LP5866TMRKPR and LP5868TMRKPR	–55		125	°C

6.4 Thermal Information

THERMAL METRIC		LP5867 YBH (DSBGA) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.3	°C/W

6.5 Electrical Characteristics

VCC = 3.3V, VLED = 3.8V, VIO = 1.8V and TA = –40°C to +85°C (TA = –55°C to +125°C for LP5860MRKPR, LP5864MRKPR, and LP5866MDBTR); Typical values are at TA = 25°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supplies						
V_{CC}	Device supply voltage		2.7		5.5	V
V_{UVR}	Undervoltage restart	V_{CC} rising, Test mode			2.5	V
V_{UVF}	Undervoltage shutdown	V_{CC} falling, Test mode	1.9			V
V_{UV_HYS}	Undervoltage shutdown hysteresis			0.3		V
V_{CAP}	Internal LDO output	V_{CC} = 2.7V to 5.5V		1.78		V
I_{CC}	Shutdown supply current $I_{SHUTDOWN}$	V_{EN} = 0, CHIP_EN = 0 (bit), ADDx = 0; measure the total current from V_{CC} and V_{LED}		0.2	1	µA
	Standby supply current $I_{STANDBY}$	V_{EN} = 3.3V, CHIP_EN = 0 (bit), measure the total current from V_{CC} and V_{LED}		7	10	µA
	Active mode supply current I_{NORMAL}	V_{EN} = 3.3V, CHIP_EN = 1 (bit), all channels I_{OUT} = 5mA (MC = 1, CC = 127, DC = 256), measure the current from V_{CC}		4.2	6	mA
V_{LED}	LED supply voltage		2.7		5.5	V
V_{VIO}	VIO supply voltage		1.65		5.5	V
I_{VIO}	VIO supply current	Interface idle			5	µA
Output Stages						
I_{CS}	Constant current sink output range (CSR0(CS0) – CSB1(CS5))	2.7 <= V_{CC} < 3.3V, PWM = 100%	0.1		40	mA
		V_{CC}≥ 3.3V PWM = 100%	0.1		50	mA
I_{LKG}	Leakage current (CSR0(CS0) – CSB1(CS5))	channels off, up_deghost = 0, V_{CS}=5V		0.01	1	µA
I_{ERR_DD}	Device to device current error, I_{ERR_DD} = (I_{AVE}-I_{SET})/I_{SET}×100%	All channels ON. Current set to 0.1mA. MC = 0 CC = 42 DC = 25 PWM = 100%	–5		5	%
		All channels ON. Current set to 1mA. MC = 2 CC = 127 DC = 25 PWM = 100%	–5		5	%
		All channels ON. Current set to 10mA. MC = 2 CC = 127 DC = 255 PWM = 100%	-3.5		3.5	%
		All channels ON. Current set to 25mA. MC=7 CC=64 DC=255 PWM=100%	-3		3	%
		All channels ON. Current set to 50mA. MC = 7 CC = 127 DC = 255 PWM = 100%	–3		3	%
I_{ERR_CC}	Channel to channel current error, I_{ERR_CC} = (I_{OUTX}-I_{AVE})/I_{AVE}×100%	All channels ON. Current set to 0.1mA. MC = 0 CC = 42 DC = 25 PWM = 100%	-5		5	%
		All channels ON. Current set to 1mA. MC = 2 CC = 127 DC = 25 PWM = 100%	-5		5	%
		All channels ON. Current set to 10mA. MC = 2 CC = 127 DC = 255 PWM = 100%	–3.5		3.5	%
		All channels ON. Current set to 25mA. MC = 7 CC = 64 DC = 255 PWM = 100%	-3		3	%
		All channels ON. Current set to 50mA. MC = 7 CC = 127 DC = 255 PWM = 100%	-3		3	%
f_{PWM}	LED PWM frequency	PWM_Fre = 1, PWM = 100%		62.5		KHz
		PWM_Fre = 0, PWM = 100%		125		KHz

VCC = 3.3V, VLED = 3.8V, VIO = 1.8V and TA = –40°C to +85°C (TA = –55°C to +125°C for LP5860MRKPR, LP5864MRKPR, and LP5866MDBTR); Typical values are at TA = 25°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SAT}	Output saturation voltage	I_{OUT} = 50mA, decreasing output voltage, when the LED current has dropped 5%			0.45	V
		I_{OUT} = 30mA, decreasing output voltage, when the LED current has dropped 5%			0.4	V
		I_{OUT} = 10mA, decreasing output voltage, when the LED current has dropped 5%			0.35	V
R_{SW}	High-side PMOS ON resistance	V_{LED} = 2.7V, I_{SW} = 200mA		450	750	mΩ
		V_{LED} = 2.7V, I_{SW} = 200mA, LP5860MRKPR and LP5864MRSMR		450	570	mΩ
		V_{LED} = 3.8V, I_{SW} = 200mA		380	650	mΩ
		V_{LED} = 3.8V, I_{SW} = 200mA, LP5860MRKPR and LP5864MRSMR		380	520	mΩ
		V_{LED} = 5V, I_{SW} = 200mA		310	600	mΩ
		V_{LED} = 5V, I_{SW} = 200mA, LP5860MRKPR and LP5864MRSMR		310	490	mΩ
Logic Interfaces						
V_{LOGIC_IL}	Low-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDRx, VSYNC, IFS				0.3 x VIO	V
V_{LOGIC_IH}	High-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDRx, VSYNC, IFS		0.7 x VIO			V
V_{EN_IL}	Low-level input voltage of EN				0.4	V
V_{EN_IH}	High-level input voltage of EN	When V_{CAP} powered up	1.4			V
I_{LOGIC_I}	Input current, SDA, SCL, SCLK, MOSI, SS, ADDRx		–1		1	µA
V_{LOGIC_OL}	Low-level output voltage, SDA, MISO	I_{PULLUP} = 3mA			0.4	V
V_{LOGIC_OH}	High-level output voltage, MISO	I_{PULLUP} = –3mA	0.7 x VIO			V
Protection Circuits						
V_{LOD_TH}	Thershold for channel open detection			0.25		V
V_{LSD_TH}	Thershold for channel short detection			V_{LED} – 1		V
T_{TSD}	Thermal-shutdown junction temperature			150		°C
T_{HYS}	Thermal shutdown temperature hysteresis			15		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
MISC. Timming Requirements					
f_{OSC}	Internal oscillator frequency		31.2		MHz
f_{OSC_ERR}	Device to device oscillator frequency error	–3%		3%	
t_{POR_H}	Wait time from UVLO disactive to device NORMAL			500	µs
t_{CHIP_EN}	Wait time from setting Chip_EN (Register) =1 to device NORMAL			100	µs
t_{RISE}	LED output rise time		10		ns
t_{FALL}	LED output fall time		15		ns
t_{VSYNC_H}	The minimum high-level pulse width of VSYNC	200			µs
SPI timing requirements					
f_{SCLK}	SPI Clock frequency			12	MHz

		MIN	NOM	MAX	UNIT
1	Cycle time	83.3			ns
2	SS active lead-time	50			ns
3	SS active leg time	50			ns
4	SS inactive time	50			ns
5	SCLK low time	36			ns
6	SCLK high time	36			ns
7	MOSI set-up time	20			ns
8	MOSI hold time	20			ns
9	MISO disable time			30	ns
10	MISO data valid time			35	ns
C_b	Bus capacitance	5		40	pF
I²C fast mode timing requirements					
f_{SCL}	I²C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	600			ns
2	Clock low time	1300			ns
3	Clock high time	600			ns
4	Setup time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data setup time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Setup time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			µs
I²C fast mode plus timing requirements					
f_{SCL}	I²C clock frequency	0		1000	KHz
1	Hold time (repeated) START condition	260			ns
2	Clock low time	500			ns
3	Clock high time	260			ns
4	Setup time for a repeated START condition	260			ns
5	Data hold time	0			ns
6	Data setup time	50			ns
7	Rise time of SDA and SCL			120	ns
8	Fall time of SDA and SCL			120	ns
9	Setup time for STOP condition	260			ns
10	Bus free time between a STOP and a START condition	0.5			µs

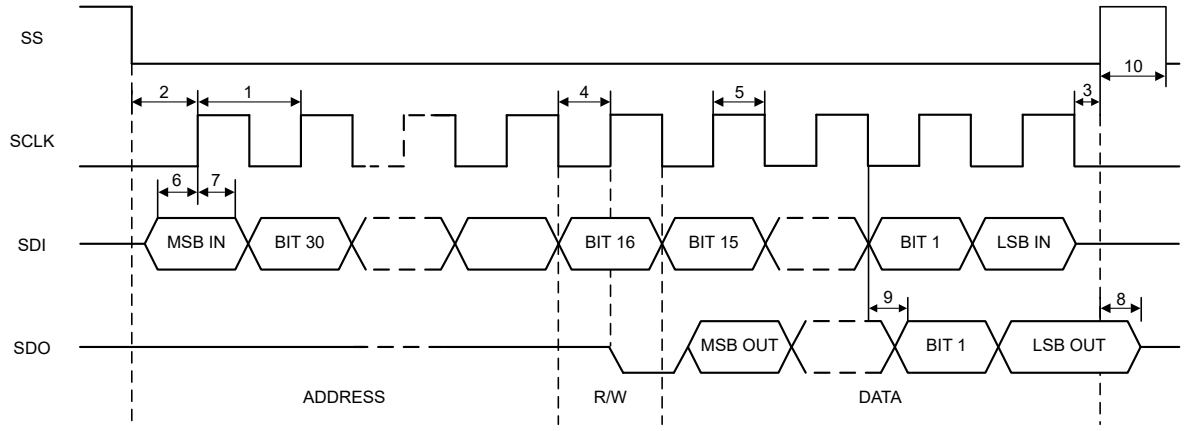


図 6-1. SPI Timing Parameters

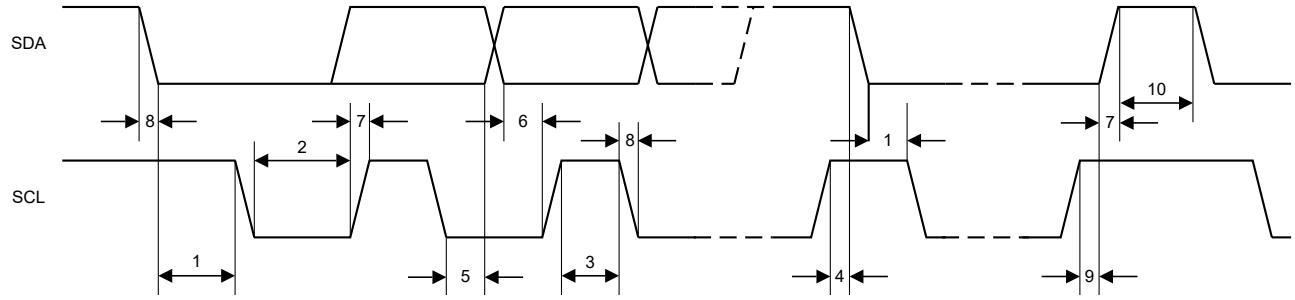


図 6-2. I²C Timing Parameters

6.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–55°C < T_A < +125°C for LP5867MRKPR, LP5864MRSMR, and LP5866MDBTR while –40°C < T_A < +85°C for the other devices), V_{CC} = 3.3V, V_{IO} = 3.3V, V_{LED} = 5V, I_{LED_Peak} = 50mA, C_{VLED} = 1µF, C_{VCC} = 1µF.

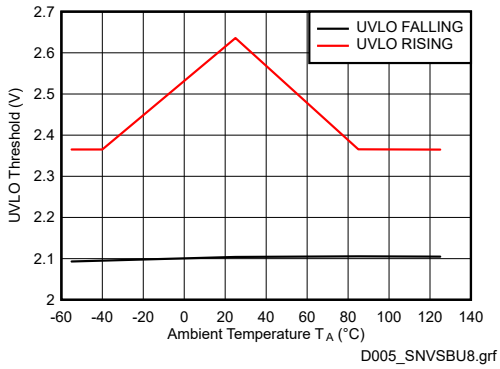


図 6-3. V_{CC} UVLO Rising and Falling Thresholds

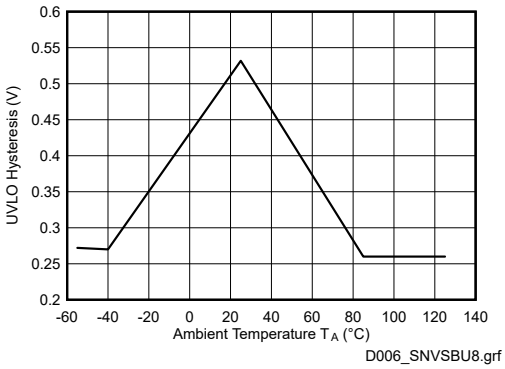


図 6-4. V_{CC} UVLO Hysteresis

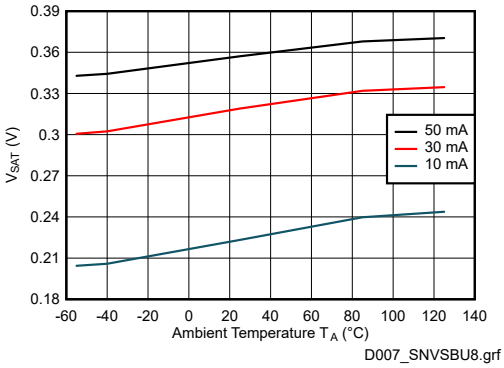


図 6-5. V_{SAT} vs Temperature

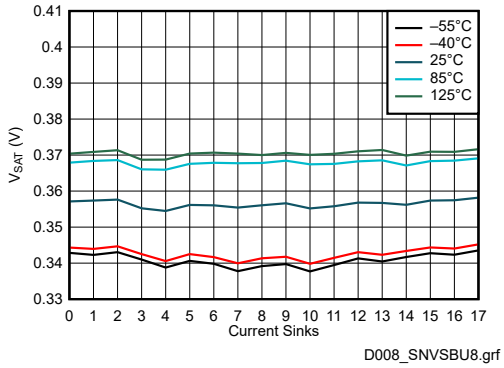


図 6-6. V_{SAT} vs Current Sinks (50mA)

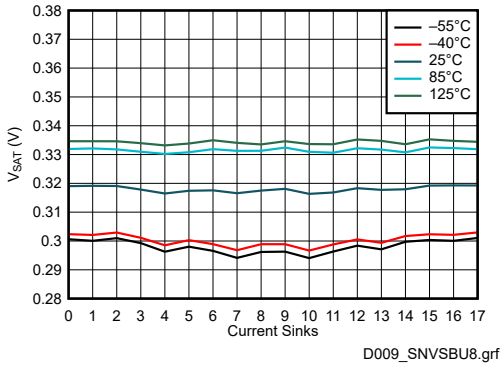


図 6-7. V_{SAT} vs Current Sinks (30mA)

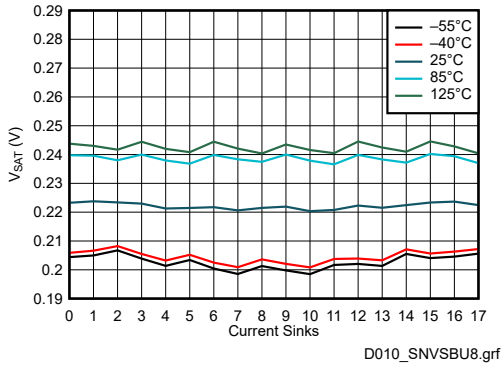
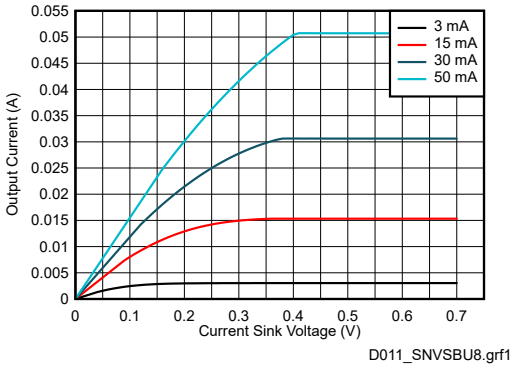


図 6-8. V_{SAT} vs Current Sinks (10mA)

6.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–55°C < T_A < +125°C for LP5867MRKPR, LP5864MRSMR, and LP5866MDBTR while –40°C < T_A < +85°C for the other devices), V_{CC} = 3.3V, V_{IO} = 3.3V, V_{LED} = 5V, I_{LED_Peak} = 50mA, C_{VLED} = 1µF, C_{VCC} = 1µF.



T_A = 25°C

図 6-9. Current Sinks Voltage vs Current

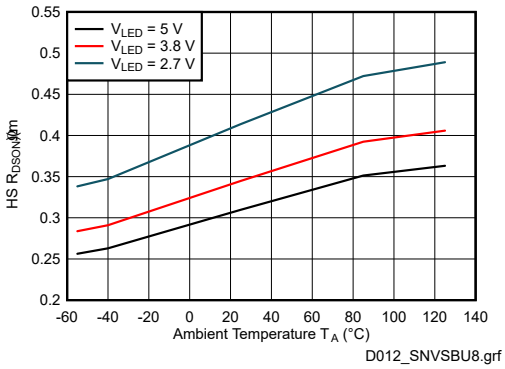


図 6-10. High Side Switch R_{DSON}

7 Detailed Description

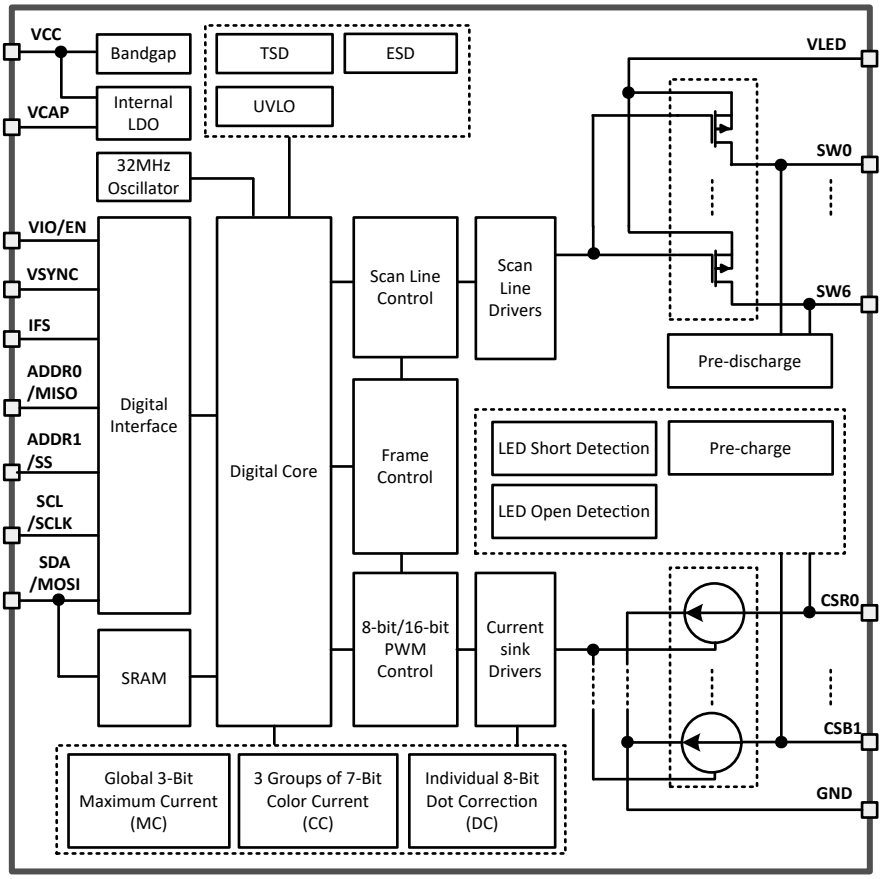
7.1 Overview

The LP5867 is an 7 × 6 LED matrix driver. The device integrates 7 switching FETs with 6 constant current sinks. One LP5867 device can drive up to 42 LED dots or 14 RGB pixels by using time-multiplexing matrix scheme.

The LP5867 supports both analog dimming and PWM dimming methods. For analog dimming, the current gain of each individual LED dot can be adjusted with 256 steps through 8-bits dot correction. For PWM dimming, the integrated 8-bits or 16-bits configurable, > 20KHz PWM generators for each LED dot enable smooth, vivid animation effects without audible noise. Each LED can also be mapped into a 8-bits group PWM to achieve the group control with minimum data traffic.

The LP5867 device implements full addressable SRAM. The device supports entire SRAM data refresh and partial SRAM data update on demand to minimize the data traffic. The LP5867 implements the ghost cancellation circuit to eliminate both upside and downside ghosting. The LP5867 also uses low brightness compensation technology to support high density LED pixels. Both 1MHz (maximum) I^2C and 12MHz (maximum) SPI interfaces are available in the LP5867.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Time-Multiplexing Matrix

The LP5867 device uses a time-multiplexing matrix scheme to support up to 42 LED dots with one chip. The device integrates 6 current sinks with 7 scan lines to drive 6 × 7 = 42 LED dots or 2 × 7 = 14 RGB pixels. In matrix control scheme, the device scans from Line 0 to Line 6 sequentially as shown in 図 7-1. Current gain and PWM duty registers are programmable for each LED dot to support individual analog and PWM dimming.

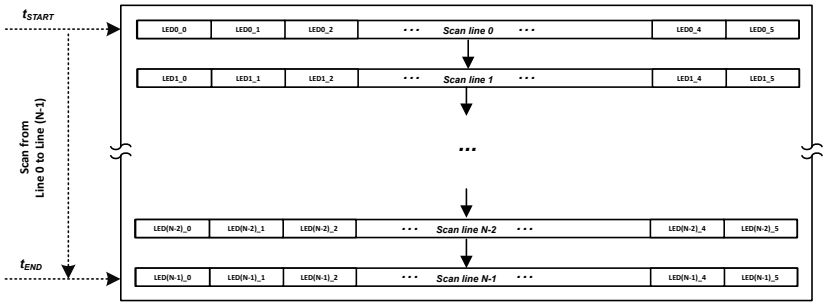


図 7-1. Scan Line Control Scheme

There are 7 high-side p-channel MOSFETs (PMOS) integrated in LP5867 device. Users can flexibly set the active scan numbers from 1 to 7 by configuring the 'Max_Line_Num' in Dev_initial register. The time-multiplexing matrix timing sequence follows the 図 7-2.

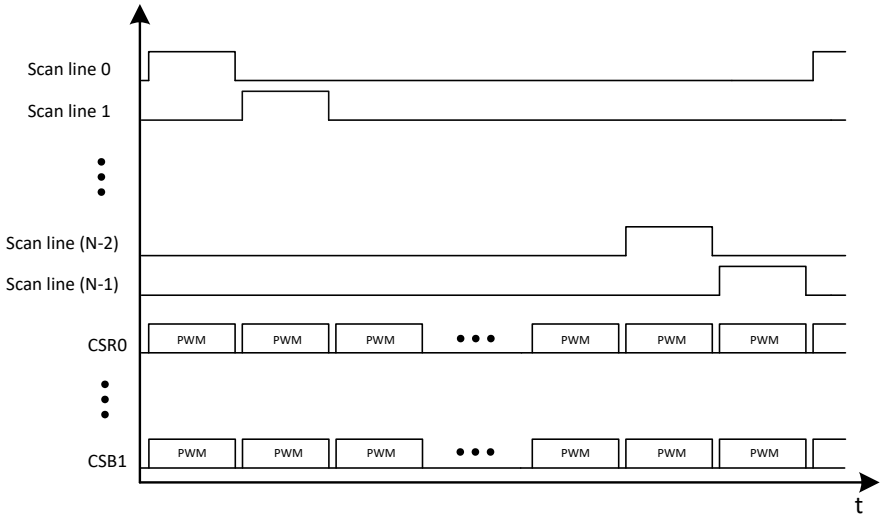


図 7-2. Time-Multiplexing Matrix Timing Sequence

One cycle time of the line switching can be calculated as below:

$$t_{line\_switch} = t_{PWM} + t_{SW\_BLK} + 2 \times t_{phase\_shift} \quad (1)$$

- t_{PWM} is the current sink active time, which equals to 8μs (PWM frequency set at 125kHz) or 16μs (PWM frequency set at 62.5kHz) by configuring 'PWM_Fre' in Dev_initial register.
- t_{SW_BLK} is the switch blank time, which equals to 1μs or 0.5μs by configuring 'SW_BLK' in Dev_config1 register.
- t_{phase_shift} is the PWM phase shift time, which equal to 0 or 125ns by configuring 'PWM_Phase_Shift' in Dev_config1 register.

Total display time for one complete sub-period is t_{sub_period} and can be calculated by the following equation:

$$t_{sub\_period} = t_{line\_switch} \times Scan\_line\# \quad (2)$$

- Scan_line# is the scan line number determined by 'Max_Line_Num' in Dev_initial register.

The time-multiplexing matrix scheme time diagram is shown in 図 7-3. The $t_{CS\_ON\_Shift}$ is the current sink turning on shift by configuring 'CS_ON_Shift' bit in Dev_config1 register.

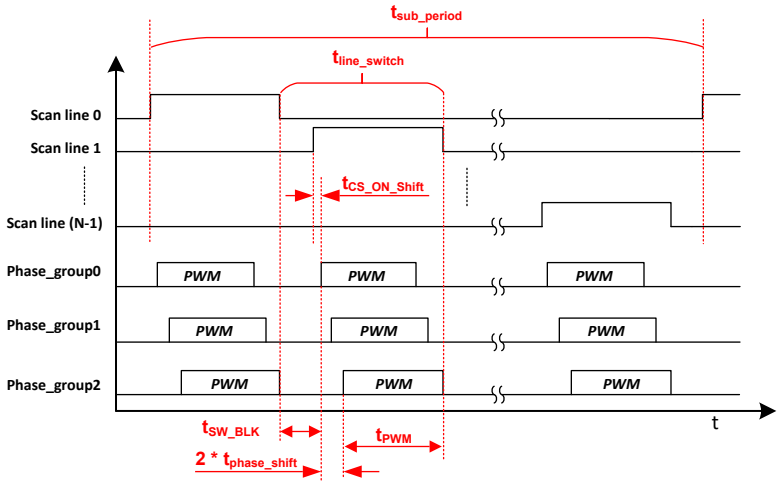


図 7-3. Time-Multiplexing Matrix Timing Diagram

The LP5867 device implements de-ghosting and low brightness compensation to remove the side effects of matrix topology:

- **De-ghosting**: Both upside de-ghosting and downside de-ghosting are implemented to eliminate the LED's unexpected weak turn-on.
  - Upside_de-ghosting: discharge each scan line during blank state. By configuring the 'Up_Deghost' in Dev_config3 register, the LP5867 discharges and clamps the scan line switch to a certain voltage.
  - Downside_deghosting: pre-charge each current sink voltage during blank state. The de-ghosting capability can be adjusted through the 'Down_Deghost' in Dev_config3 register.
- **Low Brightness Compensation**: three groups compensation are implemented to overcome the color-shift and non-uniformity in low brightness conditions. The compensation capability can be through 'Comp_Group1', 'Comp_Group2', and 'Comp_Group3' in Dev_config2 register.
  - Compensation_group 1: CSR0, CSR1.
  - Compensation_group 2: CSG0, CSG1.
  - Compensation_group 3: CSB0, CSB1.

7.3.2 Analog Dimming (Current Gain Control)

Analog dimming of LP5867 is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 3-bits Maximum Current (MC) setting without external resistor
- 3 Groups of 7-bits Color Current (CC) setting
- Individual 8-bit Dot Current (DC) setting

注

When setting to small output current in low brightness situation, adjusting MC to a small value firstly can get smaller output saturation voltage.

7.3.2.1 Global 3-Bits Maximum Current (MC) Setting

The MC is used to set the maximum current I_{OUT_MAX} for each current sink, and this current is the maximum peak current for each LED dot. The MC can be set with 7 steps from 3 mA to 50 mA. When the device is powered on, the MC data is set to default value, which is 15 mA.

For data refresh Mode 1, MC data is effective immediately after new data is updated. For Mode 2 and Mode 3, to avoid unexpected MC data change during high speed data refreshing, MC data must be changed when all channels are off and new MC data is only updated when the 'Chip_EN' bit in Chip_en register is set to 0, and after the 'Chip_EN' returns to 1, the new MC data is effective. 'Down_Deghost' and 'Up_Deghost' in Dev_config3 work in the similar way with MC.

表 7-1. Maximum Current (MC) Register Setting

3-BITS MAXIMUM_CURRENT REGISTER		I_{OUT_MAX}
Binary	Decimal	mA
000	0	3
001	1	5
010	2	10
011 (Default)	3 (Default)	15 (Default)
100	4	20
101	5	30
110	6	40
111	7	50

7.3.2.2 3 Groups of 7-Bits Color Current (CC) Setting

The LP5867 device is able to adjust the output current of three color groups separately. For each color, the device has 7-bits data in 'CC_Group1', 'CC_Group2', and 'CC_Group3'. Thus, all color group currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OUT_MAX}.

The 18 current sinks have fixed mapping to the three color groups:

- CC-Group 1: CSR0, CSR1.
- CC-Group 2: CSG0, CSG1.
- CC-Group 3: CSB0, CSB1.

表 7-2. 3 Groups of 7-bits Color Current (CC) Setting

7-BITS CC_GROUP1/CC_GROUP2/CC_GROUP3 REGISTER		RATIO OF OUTPUT CURRENT TO I_{OUT_MAX}
Binary	Decimal	%
000 0000	0	0
000 0001	1	0.79
000 0010	2	1.57
- - -	- - -	- - -
100 0000 (default)	64 (default)	50.4 (default)
- - -	- - -	- - -
111 1101	125	98.4
111 1110	126	99.2
111 1111	127	100

7.3.2.3 Individual 8-bit Dot Current (DC) Setting

The LP5867 can individually adjust the output current of each LED by using dot current function through DC setting. The device allows the brightness deviations of the LEDs to adjusted be individually. Each output DC is programmed with an 8-bit depth, so the value can be adjusted with 256 steps within the range from 0% to 100% of (I_{OUT_MAX} × CC/127).

表 7-3. Individual 8-bit Dot Current (DC) Setting

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO I_{OUT_MAX} × CC/127
Binary	Decimal	%
0000 0000	0	0
0000 0001	1	0.39
0000 0010	2	0.78
- - -	- - -	- - -
1000 0000 (Default)	128 (Default)	50.2 (Default)
- - -	- - -	- - -
1111 1101	253	99.2
1111 1110	254	99.6
1111 1111	255	100

In summary, the current gain of each current sink can be calculated as below:

$$I_{OUT}\ (mA) = I_{OUT\_MAX} \times (CC/127) \times (DC/255) \quad (3)$$

For time-multiplexing scan scheme, if the scan number is N, each LED dot's average current I_{AVG} is shown as below:

$$I_{AVG}\ (mA) = I_{OUT}/N = I_{OUT\_MAX} \times (CC/127) \times (DC/255)/N \quad (4)$$

7.3.3 PWM Dimming

There are several methods to control the PWM duty cycle of each LED dot.

7.3.3.1 Individual 8-Bit / 16-Bit PWM for Each LED Dot

Every LED has an individual 8-bit or 16-bit PWM register that is used to change the LED brightness by PWM duty. The LP5867 uses an enhanced spectrum PWM (ES-PWM) algoithm to achieve 16-bit depth with high refresh rate and this can avoid flicker under high speed camera. Comparing with conventional 8-bit PWM, 16-bit PWM can help to achieve ultimate high dimming resolution in LED animation applications.

7.3.3.2 Programmable Groups of 8-Bit PWM Dimming

The group PWM Control is used to select LEDs into 1 to 3 groups while each group has a separate register for PWM control. Every LED has 2-bit selection in LED_DOT_GROUP Registers (x = 0, 1, … , 34) to select whether the LED dot belongs to one of the three groups or not:

- 00: not a member of any group
- 01: member of group 1
- 10: member of group 2
- 11: member of group 3

7.3.3.3 8-Bit PWM for Global Dimming

The Global PWM Control function affects all LEDs simultaneously.

The final PWM duty cycle can be calculated as below:

$$PWM\_Final(8\text{-bit}) = PWM\_Individual(8\text{-bit}) \times PWM\_Group(8\text{-bit}) \times PWM\_\ Global(8\text{-bit}) \quad (5)$$

$$PWM\_Final(16\text{-bit}) = PWM\_Individual(16\text{-bit}) \times PWM\_Group(8\text{-bit}) \times PWM\_\ Global(8\text{-bit}) \quad (6)$$

The LP5867 supports 125kHz or 62.5kHz PWM output frequency. The PWM frequency is selected by configuring the 'PWM_Fre' in Dev_initial register. An internal 32MHz oscillator is used for generating PWM outputs. The oscillator's high accuracy design (f_{OSC_ERR} ≤ ± 3%) enables a better synchronization if multiple LP5867 devices are connected together.

A PWM phase-shifting scheme is implemented in each current sink to avoid the current overshot when turning on simultaneously. As the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. This scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases. By configuring the 'PWM_Phase_Shift' in Dev_config1 register, which is default off, the LP5867 supports t_{phase_shift} = 125ns shifting time shown in 図 7-4.

- Phase 1: CSR0, CSR1.
- Phase 2: CSG0, CSG1.
- Phase 3: CSB0, CSB1.

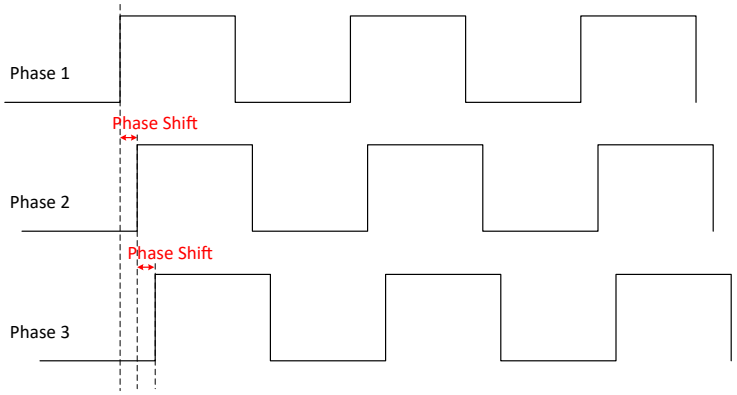


図 7-4. Phase Shift

To avoid high current sinks output ripple during line switching, current sinks can be configured to turn on with 1 clock delay (62.5ns or 31.25ns according to the PWM frequency) after lines turn on, as shown in 図 7-3. This function can be configured by 'CS_ON_Shift' in Dev_config1 register.

The LP5867 allows users to configure the dimming scale either exponentially (Gamma Correction) or linearly through the 'PWM_Scale_Mode' in Dev_config1 register. If a human-eye-friendly dimming curve is desired, using the internal fixed exponential scale is an easy approach. If a special dimming curve is desired, using the linear scale with software correction is recommended. The LP5867 supports both linear and exponential dimming curves under 8-bit and 16-bit PWM depth. 図 7-5 is an example of 8-bit PWM depth.

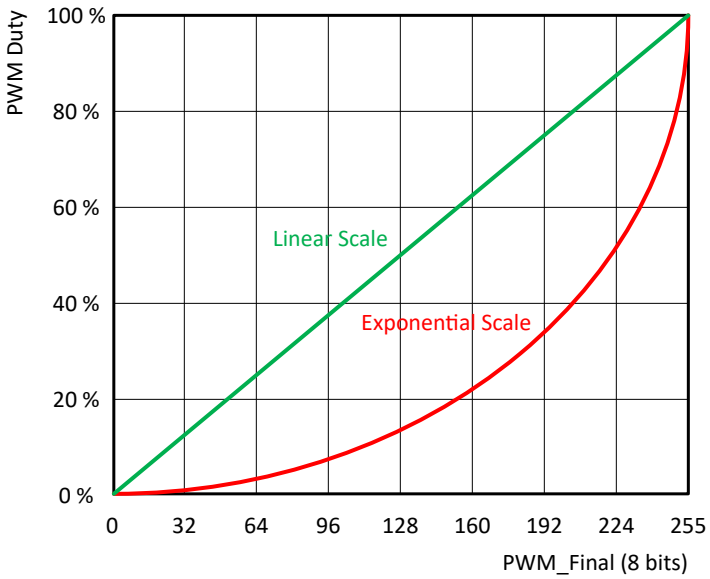


図 7-5. Linear and Exponential Dimming Curves

In summary, the PWM control method is illustrated as 図 7-6:

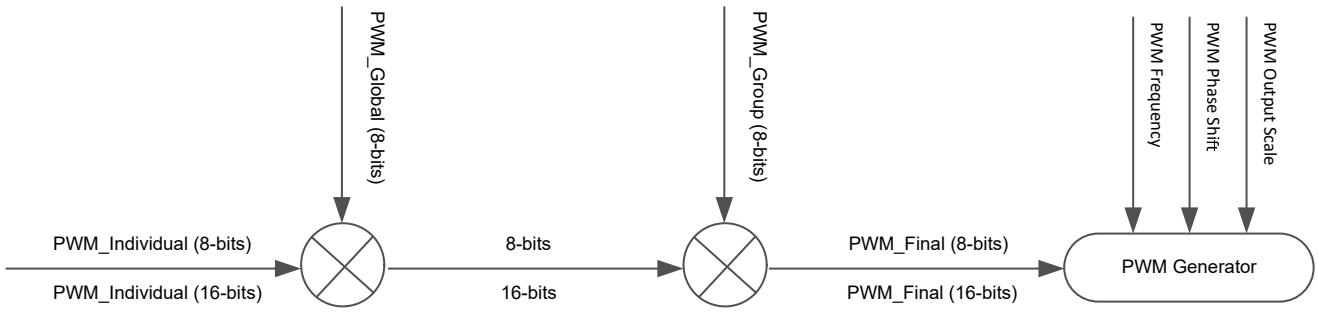


図 7-6. PWM Control Scheme

7.3.4 ON and OFF Control

The LP5867 device supports the individual ON and OFF control of each LED. For indication purpose, users can turn on and off the LED directly by writing 1-bit ON and OFF data to the corresponding Dot_onoffx (x = 0, 1, … ,) register.

7.3.5 Data Refresh Mode

The LP5867 supports three data refresh modes: Mode 1, Mode 2, and Mode 3, by configuring 'Data_Ref_Mode' in Dev_initial register.

Mode 1: 8-bit PWM data without VSYNC command. Data is sent out for display instantly after received. With Mode1, users can refresh the corresponding dots' data only instead of updating the whole SRAM. It is called ‘on demand data refresh’, which can save the total data volume effectively. As shown in 図 7-7, the red LED dots can be refreshed after sending the corresponding data while the others kept the same with last frame.

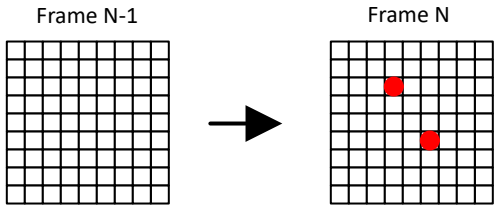


図 7-7. On Demand Data Refresh - Mode 1

Mode 2: 8-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Mode 3: 16-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Frame control is implemented in Mode 2 and Mode 3. Instead of refreshing the output instantly after data is received (Mode 1), the device holds the data and refreshes the whole frame data by a fixed frame rate, f_{VSYNC}. Usually, 24Hz, 50Hz, 60Hz, 120Hz or even higher frame rate is selected to achieve vivid animation effects. Whole SRAM Data Refresh is shown in 図 7-8, a new frame is updated after receiving the VSYNC command.

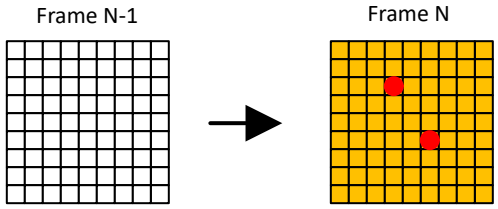


図 7-8. Whole SRAM Data Refresh

Comparing with Mode 1, Mode 2 and Mode 3 provide a better synchronization when multiple LP5867 devices used together. A high-level pulse width longer than t_{SYNC_H} is required at the beginning of each VSYNC frame. 図 7-9 shows the VSYNC connections and 図 7-10 shows the timing requirements.

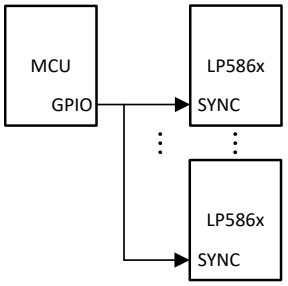


図 7-9. Multiple Devices Sync

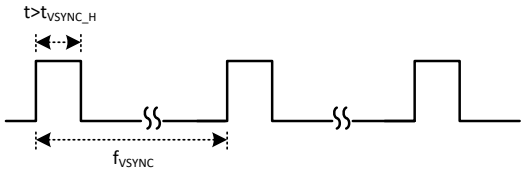


図 7-10. VSYNC Timing

Table 8-4 is the summary of the 3 data refresh modes.

表 7-4. Data Refresh Mode

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 1	8 Bits	Data update instantly	No
Mode 2	8 Bits	Data update by frame	Yes
Mode 3	16 Bits		

7.3.6 Full Addressable SRAM

SRAM is implemented inside the LP5867 device to support data writing and reading at the same time.

Although data refresh mechanisms are not the same for Mode 1 and Mode 2/3, the data writing and reading follow the same method. Uses can update partial of the SRAM data only or the whole SRAM page simultaneously. The LP5867 supports auto-increment function to minimize data traffic and increase data transfer efficiency.

Please be noted that 16-bit PWM (Mode 3) and 8-bit PWM (Mode 1 and Mode 2) are assigned with different SRAM addresses.

7.3.7 Protections and Diagnostics

7.3.7.1 LED Open Detection

The LP5867 includes LED open detection (LOD) for the fault caused by any opened LED dot. The threshold for LED open is 0.25V typical. LED open detection is only performed when PWM ≥ 25 (Mode 1 and Mode 2) or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected lower than open threshold for continuously 4 sub-periods.

図 7-11 shows the detection circuit of LOD function. When open fault is detected, 'Global_LOD' bit in Fault_state register is set to 1 and detailed fault state for each LED is also monitored in register Dot_lodx (x = 0, 1, … , 20). All open fault indicator bits can be cleared by setting LOD_clear = 0Fh after the open condition is removed.

LOD removal function can be enabled by setting 'LOD_removal' bit in Dev_config2 register to 1. This function turns off the current sink of the open channel when scanning to the line where the opened LED is included.

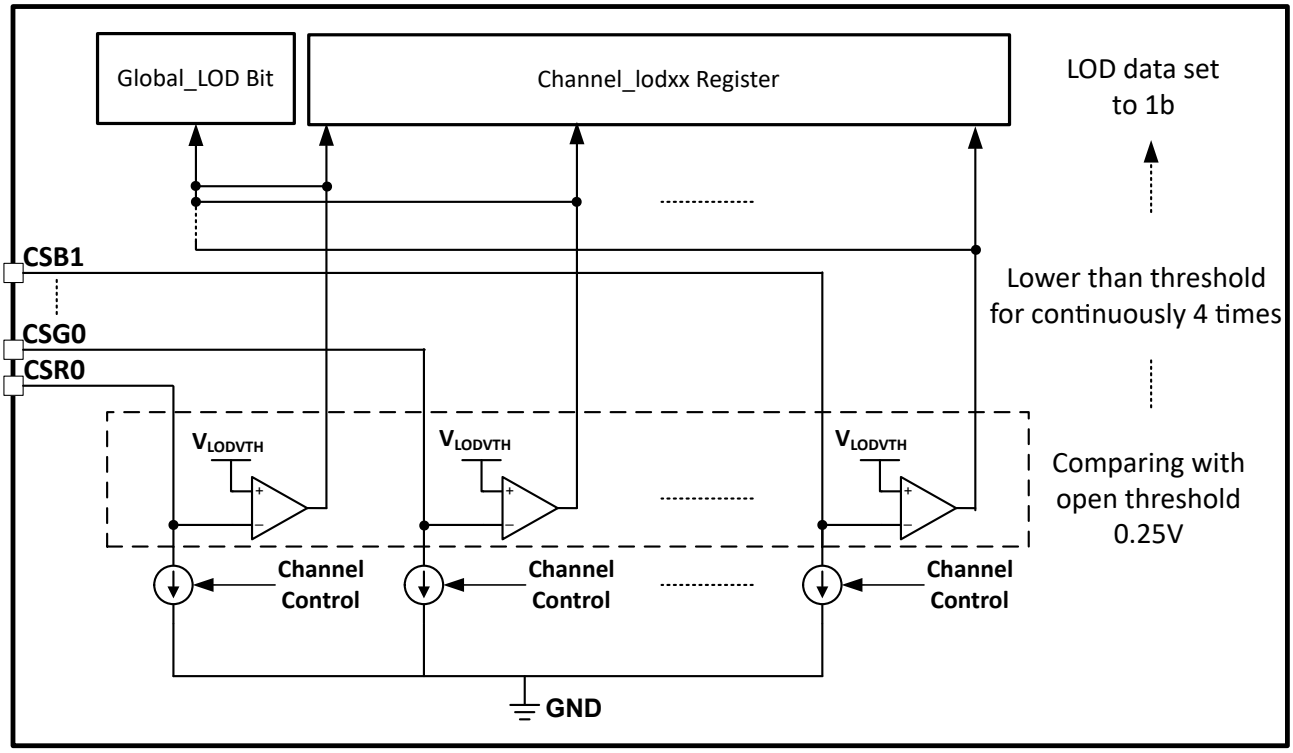


図 7-11. LOD Circuits

7.3.7.2 LED Short Detection

The LP5867 includes LED short detection (LSD) for the fault caused by any shorted LED. Threshold for channel short is (VLED – 1) V typical. LED short detection only performed when PWM ≥ 25 (Mode 1 and Mode 2) or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected higher than short threshold for continuously 4 sub-periods. As there is parasitic capacitance for the current sink, to make sure the LSD result is correct, setting the LED current higher than 0.5mA is recommended.

The image below shows the detection circuit of LSD function. When short fault is detected, 'Global_LSD bit' in Fault_state register is set to 1 and detailed fault state for every channel are also monitored in register Dot_lsdx (x = 0, 1, … , 20). All short fault indicator bits can be cleared by setting LSD_clear = 0Fh after the short condition is removed.

LSD removal function can be enabled by setting 'LSD_removal' bit in Dev_config2 register to 1. This function turns off the upside deghosting function of the scan line where short LED is included.

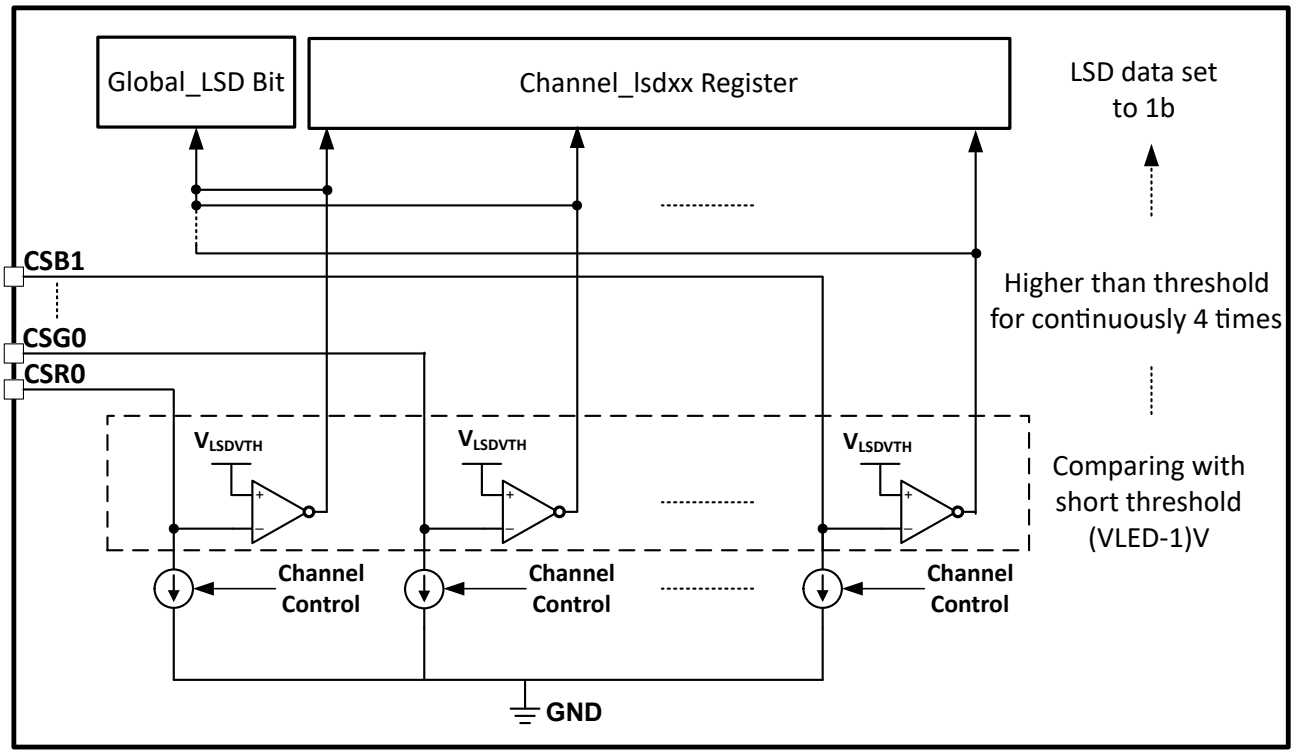


図 7-12. LSD Circuit

7.3.7.3 Thermal Shutdown

The LP5867 device implements thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160°C (typical) and above, the device switches into shutdown mode. The LP5867 exits thermal shutdown when the junction temperature of the device drops to 145°C (typical) and below.

7.3.7.4 UVLO (Under Voltage Lock Out)

The LP5867 has an internal comparator that monitors the voltage at VCC. When VCC is below V_{UVF}, reset is active and the LP5867 enters INITIALIZATION state.

7.4 Device Functional Modes

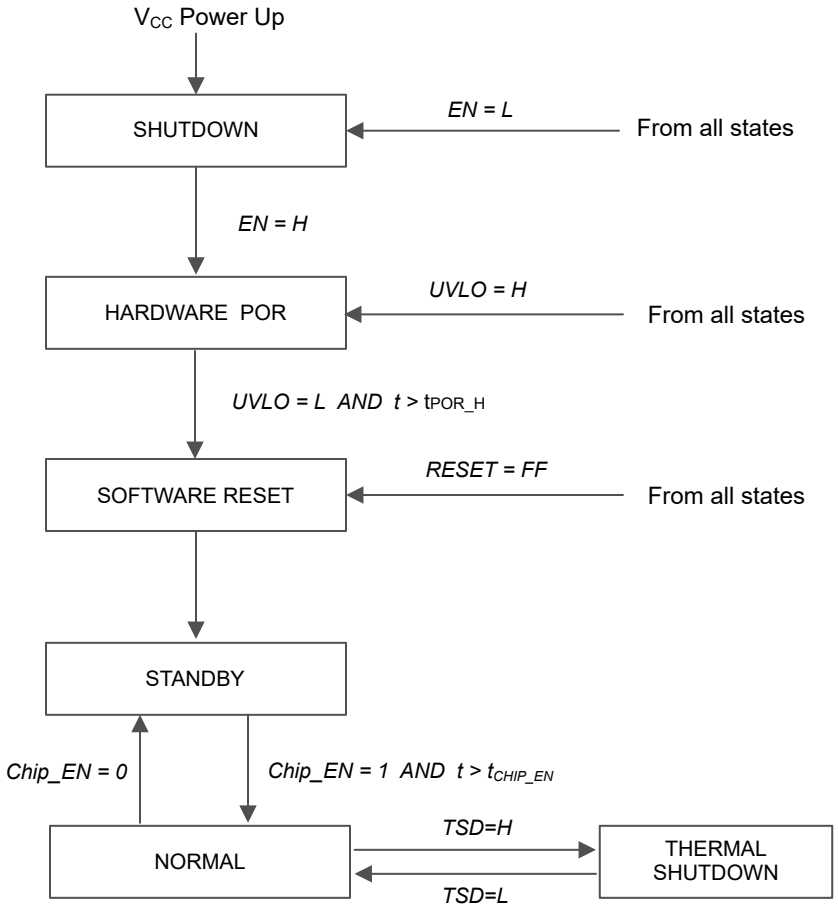


図 7-13. Device Functional Modes

- SHUTDOWN: The device enters into SHUTDOWN mode from all states on VCC power up or EN pin is low.
- HARDWARE POR: The device enters into HARDWARE POR when Enable pin is high or VCC fall under V_{UVF} causing UVLO=H from all states.
- SOFTWARE RESET: The device enters into SOFTWARE RESET mode when VCC rise higher than V_{UVR} with the time t > t_{POR_H}. In this mode, all the registers are reset. Entry can also be from any state when the RESET (register) = FFh or UVLO is low.
- STANDBY: The device enters the STANDBY mode when Chip_EN (register) = 0. In this mode, device enters into low power mode, but the I^2C/SPI are still available for Chip_EN only and the registers' data are retained.
- NORMAL: The device enters the NORMAL mode when 'Chip_EN' = 1 with the time t > t_{CHIP_EN}.
- THERMAL SHUTDOWN: The device automatically enters the THERMAL SHUTDOWN mode when the junction temperature exceeds 160°C (typical). If the junction temperature decreases below 145°C (typical), the device returns to the NORMAL mode.

7.5 Programming

7.5.1 Interface Selection

The LP5867 supports two communication interfaces: I^{2}C and SPI. If IFS is high, ithe device enters into SPI mode. If IFS is low, the device enters into I^{2}C mode.

表 7-5. Interface Selection

INTERFACE TYPE	ENTRY CONDITION
I^{2}C	IFS = Low
SPI	IFS = High

7.5.2 I^{2}C Interface

The LP5867 is compatible with I^{2}C standard specification. The device supports both fast mode (400KHz maximum) and fast plus mode (1MHz maximum).

7.5.2.1 I^{2}C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

7.5.2.2 I²C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5-bits of the chip address, 2 higher bits of the register address, and 1 read/write bit. The other 8 lower bits of register address are put in Address Byte 2.The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

表 7-6. I²C Data Format

Address Byte1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	0	ADDR1	ADDR0	9th bit	8th bit	R: 1 W: 0
Broadcast	1	0	1	0	1			
Address Byte2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7th bit	6th bit	5th bit	4th bit	3th bit	2th bit	1th bit	0th bit

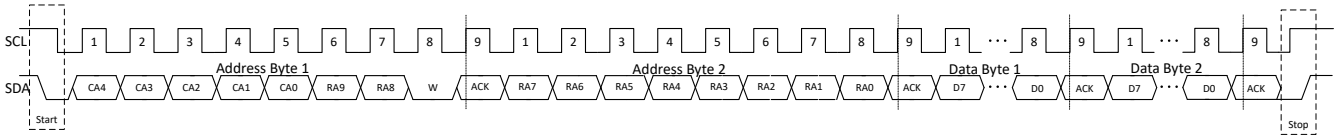


図 7-14. I²C Write Timming

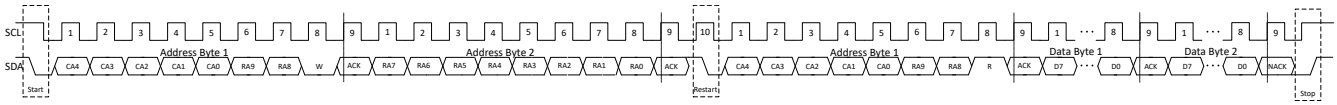


図 7-15. I²C Read Timing

7.5.2.3 Multiple Devices Connection

The LP5867 enters into I²C mode if IFS is connected to GND. The ADDR0/1 pin is used to select the unique I²C follower address for each device. The SCL and SDA lines must each have a pullup resistor (4.7KΩ for 400KHz, 2KΩ for 1MHz) placed somewhere on the line and remain HIGH even when the bus is idle. VIO_EN can either be connected with VIO power supply or GPIO. It's suggested to put one 1nF cap as closer to VIO_EN pin as possible. Up to four LP5867 follower devices can share the same I²C bus by the different ADDR configurations.

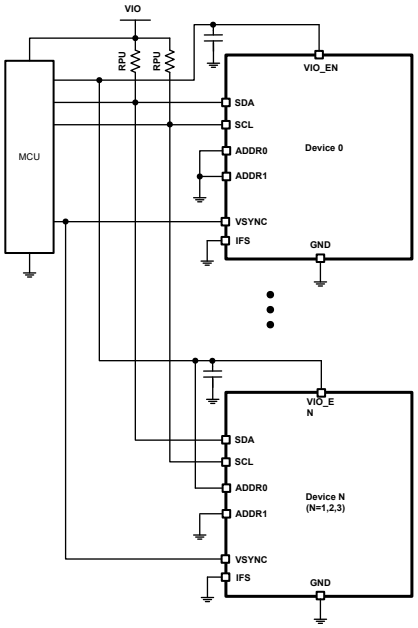


図 7-16. I²C Multiple Devices Connection

7.5.3 Programming

7.5.3.1 SPI Data Transactions

MISO output is normally in a high impedance state. When the follower-select pin SS for the device is active (low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. The follower-select signal SS must be low during the cycle transmission. SS resets the interface when high. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

7.5.3.2 SPI Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which contains 8 higher bits of the register address. The Address Byte 2 is started with 2 lower bits of the register address and 1 read/write bit. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

表 7-7. SPI Data Format

Address Byte1	**Register Address**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	9^{th} bit	8^{th} bit	7^{th} bit	6^{th} bit	5^{th} bit	4^{th} bit	3^{th} bit	2^{th} bit
Address Byte2	**Register Address**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	1^{th} bit	0^{th} bit	R: 0 W: 1	Don't Care				

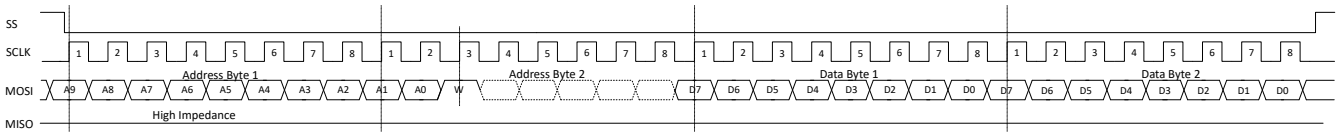


図 7-17. SPI Write Timing

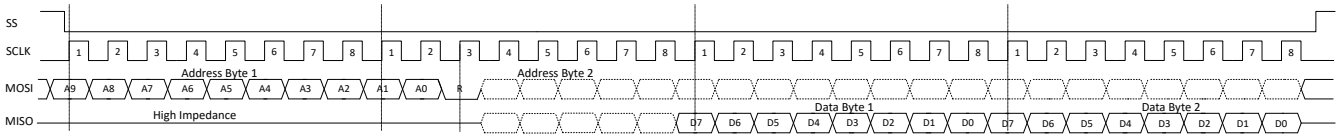


図 7-18. SPI Read Timing

7.5.3.3 Multiple Devices Connection

The device enters into SPI mode if IFS is pulled high to VIO through a pullup resistor(4.7KΩ recommended). VIO_EN can either be connected with VIO power supply or GPIO. It's suggested to put one 1nF cap as closer to VIO_EN pin as possible. In SPI mode host can address as many devices as there are follower select pins on host.

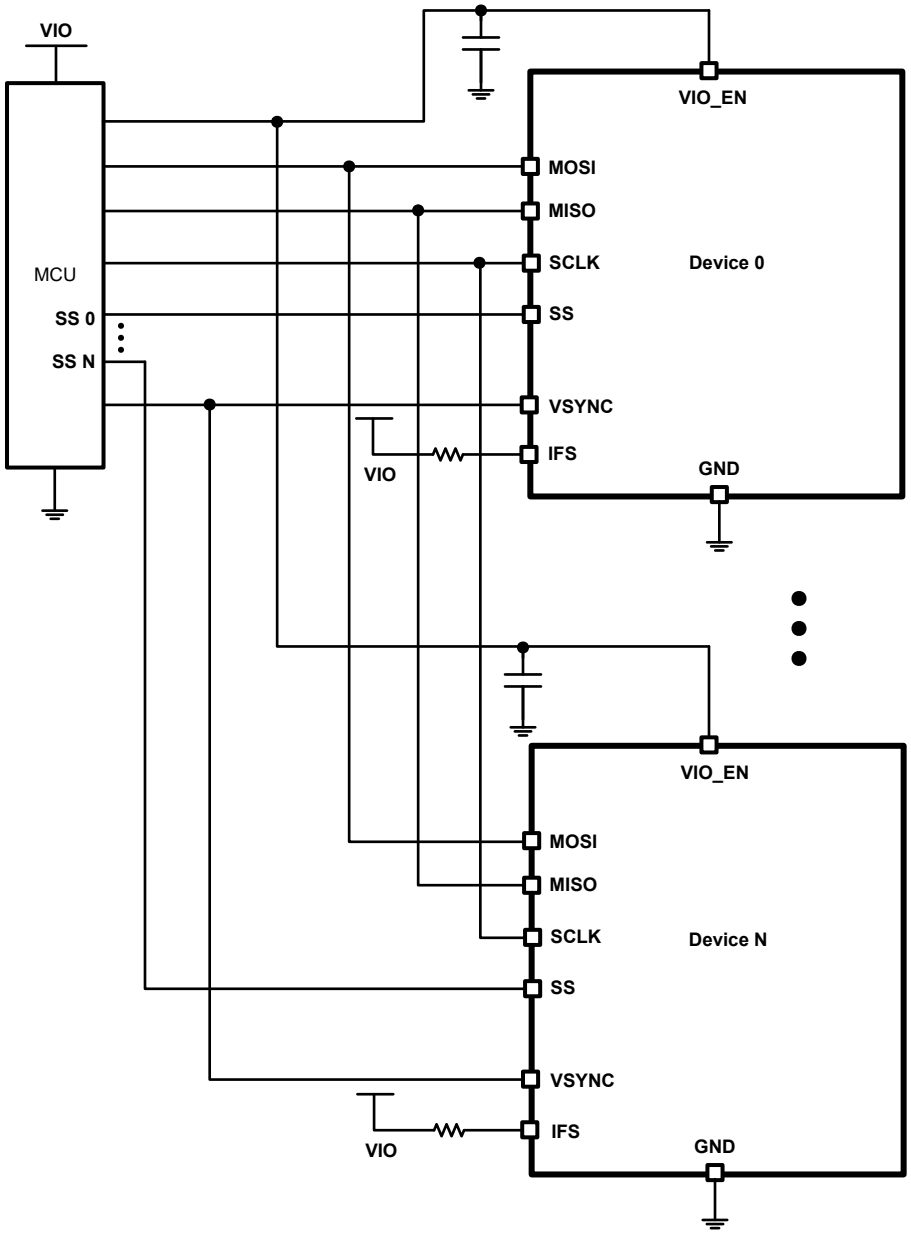


図 7-19. SPI Multiple Devices Connection

7.6 Register Maps

This section provides a summary of the register maps. For detailed register functions and descriptions, please refer to *LP5867 7x6 LED Matrix Driver Register Maps* .

表 7-8. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Chip_en	000h	R/W	Reserved							Chip_EN	00h
Dev_initial	001h	R/W	Reserved	Max_Line_Num				Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved	Reserved	Reserved	Reserved	SW_BLK	PWM_Scale_Mode	PWM_Phase_Shift	CS_ON_Shift	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		LOD_removal	LSD_removal	00h
Dev_config3	004h	R/W	Down_Deghost		Up_Deghost		Maximum_Current			Up_Deghost_enable	47h
Global_bri	005h	R/W	PWM_Global								FFh
Group0_bri	006h	R/W	PWM_Group1								FFh
Group1_bri	007h	R/W	PWM_Group2								FFh
Group2_bri	008h	R/W	PWM_Group3								FFh
R_current_set	009h	R/W	Reserved	CC_Group1							40h
G_current_set	00Ah	R/W	Reserved	CC_Group2							40h
B_current_set	00Bh	R/W	Reserved	CC_Group3							40h
Dot_grp_sel0	00Ch	R/W	Reserved				Dot L0-CSG0 group		Dot L0-CSR0 group		00h
Dot_grp_sel1	00Dh	R/W	Reserved								00h
Dot_grp_sel2	00Eh	R/W	Reserved				Dot L0-CSR1 group		Dot L0-CSB0 group		00h
Dot_grp_sel3	00Fh	R/W	Reserved								00h
Dot_grp_sel4	010h	R/W	Reserved				Dot L0-CSB1 group		Dot L0-CSG1 group		00h
Dot_grp_sel5	011h	R/W	Reserved				Dot L1-CSG0 group		Dot L1-CSR0 group		00h
Dot_grp_sel6	012h	R/W	Reserved								00h
Dot_grp_sel7	013h	R/W	Reserved				Dot L1-CSR1 group		Dot L1-CSB0 group		00h
Dot_grp_sel8	014h	R/W	Reserved								00h
Dot_grp_sel9	015h	R/W	Reserved				Dot L1-CSB1 group		Dot L1-CSG1 group		00h
Dot_grp_sel10	016h	R/W	Reserved				Dot L2-CSG0 group		Dot L2-CSR0 group		00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_grp_sel11	017h	R/W	Reserved								00h
Dot_grp_sel12	018h	R/W	Reserved				Dot L2-CSR1 group		Dot L2-CSB0 group		00h
Dot_grp_sel13	019h	R/W	Reserved								00h
Dot_grp_sel14	01Ah	R/W	Reserved				Dot L2-CSB1 group		Dot L2-CSG1 group		00h
Dot_grp_sel15	01Bh	R/W	Reserved				Dot L3-CSG0 group		Dot L3-CSR0 group		00h
Dot_grp_sel16	01Ch	R/W	Reserved								00h
Dot_grp_sel17	01Dh	R/W	Reserved				Dot L3-CSR1 group		Dot L3-CSB0 group		00h
Dot_grp_sel18	01Eh	R/W	Reserved								00h
Dot_grp_sel19	01Fh	R/W	Reserved				Dot L3-CSB1 group		Dot L3-CSG1 group		00h
Dot_grp_sel20	020h	R/W	Reserved				Dot L4-CSG0 group		Dot L4-CSR0 group		00h
Dot_grp_sel21	021h	R/W	Reserved								00h
Dot_grp_sel22	022h	R/W	Reserved				Dot L4-CSR1 group		Dot L4-CSB0 group		00h
Dot_grp_sel23	023h	R/W	Reserved								00h
Dot_grp_sel24	024h	R/W	Reserved				Dot L4-CSB1 group		Dot L4-CSG1 group		00h
Dot_grp_sel25	025h	R/W	Reserved				Dot L5-CSG0 group		Dot L5-CSR0 group		00h
Dot_grp_sel26	026h	R/W	Reserved								00h
Dot_grp_sel27	027h	R/W	Reserved				Dot L5-CSR1 group		Dot L5-CSB0 group		00h
Dot_grp_sel28	028h	R/W	Reserved								00h
Dot_grp_sel29	029h	R/W	Reserved				Dot L5-CSB1 group		Dot L5-CSG1 group		00h
Dot_grp_sel30	02Ah	R/W	Reserved				Dot L6-CSG0 group		Dot L6-CSR0 group		00h
Dot_grp_sel31	02Bh	R/W	Reserved								00h
Dot_grp_sel32	02Ch	R/W	Reserved				Dot L6-CSR1 group		Dot L6-CSB0 group		00h
Dot_grp_sel33	02Dh	R/W	Reserved								00h
Dot_grp_sel34	02Eh	R/W	Reserved				Dot L6-CSB1 group		Dot L6-CSG1 group		00h
Dot_onoff0	043h	R/W	Reserved						Dot L0-CSG0 onoff	Dot L0-CSR0 onoff	FFh
Dot_onoff1	044h	R/W	Reserved						Dot L0-CSR1 onoff	Dot L0-CSB0 onoff	FFh
Dot_onoff2	045h	R/W	Reserved						Dot L0-CSB1 onoff	Dot L0-CSG1 onoff	03h
Dot_onoff3	046h	R/W	Reserved						Dot L1-CSG0 onoff	Dot L1-CSR0 onoff	FFh
Dot_onoff4	047h	R/W	Reserved						Dot L1-CSR1 onoff	Dot L1-CSB0 onoff	FFh
Dot_onoff5	048h	R/W	Reserved						Dot L1-CSB1 onoff	Dot L1-CSG1 onoff	03h
Dot_onoff6	049h	R/W	Reserved						Dot L2-CSG0 onoff	Dot L2-CSR0 onoff	FFh
Dot_onoff7	04Ah	R/W	Reserved						Dot L2-CSR1 onoff	Dot L2-CSB0 onoff	FFh
Dot_onoff8	04Bh	R/W	Reserved						Dot L2-CSB1 onoff	Dot L2-CSG1 onoff	03h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_onoff9	04Ch	R/W	Reserved						Dot L3-CSG0 onoff	Dot L3-CSR0 onoff	FFh
Dot_onoff10	04Dh	R/W	Reserved						Dot L3-CSR1 onoff	Dot L3-CSB0 onoff	FFh
Dot_onoff11	04Eh	R/W	Reserved						Dot L3-CSB1 onoff	Dot L3-CSG1 onoff	03h
Dot_onoff12	04Fh	R/W	Reserved						Dot L4-CSG0 onoff	Dot L4-CSR0 onoff	FFh
Dot_onoff13	050h	R/W	Reserved						Dot L4-CSR1 onoff	Dot L4-CSB0 onoff	FFh
Dot_onoff14	051h	R/W	Reserved						Dot L4-CSB1 onoff	Dot L4-CSG1 onoff	03h
Dot_onoff15	052h	R/W	Reserved						Dot L5-CSG0 onoff	Dot L5-CSR0 onoff	FFh
Dot_onoff16	053h	R/W	Reserved						Dot L5-CSR1 onoff	Dot L5-CSB0 onoff	FFh
Dot_onoff17	054h	R/W	Reserved						Dot L5-CSB1 onoff	Dot L5-CSG1 onoff	03h
Dot_onoff18	055h	R/W	Reserved						Dot L6-CSG0 onoff	Dot L6-CSR0 onoff	FFh
Dot_onoff19	056h	R/W	Reserved						Dot L6-CSR1 onoff	Dot L6-CSB0 onoff	FFh
Dot_onoff20	057h	R/W	Reserved						Dot L6-CSB1 onoff	Dot L6-CSG1 onoff	03h
Fault_state	064h	R	Reserved						Global_LOD	Global_LSD	00h
Dot_lod0	065h	R	Reserved						Dot L0-CSG0 LOD	Dot L0-CSR0 LOD	00h
Dot_lod1	066h	R	Reserved						Dot L0-CSR1 LOD	Dot L0-CSB0 LOD	00h
Dot_lod2	067h	R	Reserved						Dot L0-CSB1 LOD	Dot L0-CSG1 LOD	00h
Dot_lod3	068h	R	Reserved						Dot L1-CSG0 LOD	Dot L1-CSR0 LOD	00h
Dot_lod4	069h	R	Reserved						Dot L1-CSR1 LOD	Dot L1-CSB0 LOD	00h
Dot_lod5	06Ah	R	Reserved						Dot L1-CSB1 LOD	Dot L1-CSG1 LOD	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_lod6	06Bh	R	Reserved						Dot L2-CSG0 LOD	Dot L2-CSR0 LOD	00h
Dot_lod7	06Ch	R	Reserved						Dot L2-CSR1 LOD	Dot L2-CSB0 LOD	00h
Dot_lod8	06Dh	R	Reserved						Dot L2-CSB1 LOD	Dot L2-CSG1 LOD	00h
Dot_lod9	06Eh	R	Reserved						Dot L3-CSG0 LOD	Dot L3-CSR0 LOD	00h
Dot_lod10	06Fh	R	Reserved						Dot L3-CSR1 LOD	Dot L3-CSB0 LOD	00h
Dot_lod11	070h	R	Reserved						Dot L3-CSB1 LOD	Dot L3-CSG1 LOD	00h
Dot_lod12	071h	R	Reserved						Dot L4-CSG0 LOD	Dot L4-CSR0 LOD	00h
Dot_lod13	072h	R	Reserved						Dot L4-CSR1 LOD	Dot L4-CSB0 LOD	00h
Dot_lod14	073h	R	Reserved						Dot L4-CSB1 LOD	Dot L4-CSG1 LOD	00h
Dot_lod15	074h	R	Reserved						Dot L5-CSG0 LOD	Dot L5-CSR0 LOD	00h
Dot_lod16	075h	R	Reserved						Dot L5-CSR1 LOD	Dot L5-CSB0 LOD	00h
Dot_lod17	076h	R	Reserved						Dot L5-CSB1 LOD	Dot L5-CSG1 LOD	00h
Dot_lod18	077h	R	Reserved						Dot L6-CSG0 LOD	Dot L6-CSR0 LOD	00h
Dot_lod19	078h	R	Reserved						Dot L6-CSR1 LOD	Dot L6-CSB0 LOD	00h
Dot_lod20	079h	R	Reserved						Dot L6-CSB1 LOD	Dot L6-CSG1 LOD	00h
Dot_lsd0	086h	R	Reserved						Dot L0-CSG0 LSD	Dot L0-CSR0 LSD	00h
Dot_lsd1	087h	R	Reserved						Dot L0-CSR1 LSD	Dot L0-CSB0 LSD	00h
Dot_lsd2	088h	R	Reserved						Dot L0-CSB1 LSD	Dot L0-CSG1 LSD	00h
Dot_lsd3	089h	R	Reserved						Dot L1-CSG0 LSD	Dot L1-CSR0 LSD	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_lsd4	08Ah	R	Reserved						Dot L1-CSR1 LSD	Dot L1-CSB0 LSD	00h
Dot_lsd5	08Bh	R	Reserved						Dot L1-CSB1 LSD	Dot L1-CSG1 LSD	00h
Dot_lsd6	08Ch	R	Reserved						Dot L2-CSG0 LSD	Dot L2-CSR0 LSD	00h
Dot_lsd7	08Dh	R	Reserved						Dot L2-CSR1 LSD	Dot L2-CSB0 LSD	00h
Dot_lsd8	08Eh	R	Reserved						Dot L2-CSB1 LSD	Dot L2-CSG1 LSD	00h
Dot_lsd9	08Fh	R	Reserved						Dot L3-CSG0 LSD	Dot L3-CSR0 LSD	00h
Dot_lsd10	090h	R	Reserved						Dot L3-CSR1 LSD	Dot L3-CSB0 LSD	00h
Dot_lsd11	091h	R	Reserved						Dot L3-CSB1 LSD	Dot L3-CSG1 LSD	00h
Dot_lsd12	092h	R	Reserved						Dot L4-CSG0 LSD	Dot L4-CSR0 LSD	00h
Dot_lsd13	093h	R	Reserved						Dot L4-CSR1 LSD	Dot L4-CSB0 LSD	00h
Dot_lsd14	094h	R	Reserved						Dot L4-CSB1 LSD	Dot L4-CSG1 LSD	00h
Dot_lsd15	095h	R	Reserved						Dot L5-CSG0 LSD	Dot L5-CSR0 LSD	00h
Dot_lsd16	096h	R	Reserved						Dot L5-CSR1 LSD	Dot L5-CSB0 LSD	00h
Dot_lsd17	097h	R	Reserved						Dot L5-CSB1 LSD	Dot L5-CSG1 LSD	00h
Dot_lsd18	098h	R	Reserved						Dot L6-CSG0 LSD	Dot L6-CSR0 LSD	00h
Dot_lsd19	099h	R	Reserved						Dot L6-CSR1 LSD	Dot L6-CSB0 LSD	00h
Dot_lsd20	09Ah	R	Reserved						Dot L6-CSB1 LSD	Dot L6-CSG1 LSD	00h
LOD_clear	0A7h	W	Reserved				LOD_Clear				00h
LSD_clear	0A8h	W	Reserved				LSD_Clear				00h
Reset	0A9h	W	Reset								00h
DC0	100h	R/W	LED dot current setting for Dot L0-CSR0								80h
DC1	101h	R/W	LED dot current setting for Dot L0-CSG0								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC2	102h	R/W	Reserved								80h
DC3	103h	R/W	Reserved								80h
DC4	104h	R/W	Reserved								80h
DC5	105h	R/W	Reserved								80h
DC6	106h	R/W	Reserved								80h
DC7	107h	R/W	Reserved								80h
DC8	108h	R/W	LED dot current setting for Dot L0-CSB0								80h
DC9	109h	R/W	LED dot current setting for Dot L0-CSR1								80h
DC10	10Ah	R/W	Reserved								80h
DC11	10Bh	R/W	Reserved								80h
DC12	10Ch	R/W	Reserved								80h
DC13	10Dh	R/W	Reserved								80h
DC14	10Eh	R/W	Reserved								80h
DC15	10Fh	R/W	Reserved								80h
DC16	110h	R/W	LED dot current setting for Dot L0-CSG1								80h
DC17	111h	R/W	LED dot current setting for Dot L0-CSB1								80h
DC18	112h	R/W	LED dot current setting for Dot L1-CSR0								80h
DC19	113h	R/W	LED dot current setting for Dot L1-CSG0								80h
DC20	114h	R/W	Reserved								80h
DC21	115h	R/W	Reserved								80h
DC22	116h	R/W	Reserved								80h
DC23	117h	R/W	Reserved								80h
DC24	118h	R/W	Reserved								80h
DC25	119h	R/W	Reserved								80h
DC26	11Ah	R/W	LED dot current setting for Dot L1-CSB0								80h
DC27	11Bh	R/W	LED dot current setting for Dot L1-CSR1								80h
DC28	11Ch	R/W	Reserved								80h
DC29	11Dh	R/W	Reserved								80h
DC30	11Eh	R/W	Reserved								80h
DC31	11Fh	R/W	Reserved								80h
DC32	120h	R/W	Reserved								80h
DC33	121h	R/W	Reserved								80h
DC34	122h	R/W	LED dot current setting for Dot L1-CSG1								80h
DC35	123h	R/W	LED dot current setting for Dot L1-CSB1								80h
DC36	124h	R/W	LED dot current setting for Dot L2-CSR0								80h
DC37	125h	R/W	LED dot current setting for Dot L2-CSG0								80h
DC38	126h	R/W	Reserved								80h
DC39	127h	R/W	Reserved								80h
DC40	128h	R/W	Reserved								80h
DC41	129h	R/W	Reserved								80h
DC42	12Ah	R/W	Reserved								80h
DC43	12Bh	R/W	Reserved								80h
DC44	12Ch	R/W	LED dot current setting for Dot L2-CSB0								80h
DC45	12Dh	R/W	LED dot current setting for Dot L2-CSR1								80h
DC46	12Eh	R/W	Reserved								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC47	12Fh	R/W	Reserved								80h
DC48	130h	R/W	Reserved								80h
DC49	131h	R/W	Reserved								80h
DC50	132h	R/W	Reserved								80h
DC51	133h	R/W	Reserved								80h
DC52	134h	R/W	LED dot current setting for Dot L2-CSG1								80h
DC53	135h	R/W	LED dot current setting for Dot L2-CSB1								80h
DC54	136h	R/W	LED dot current setting for Dot L3-CSR0								80h
DC55	137h	R/W	LED dot current setting for Dot L3-CSG0								80h
DC56	138h	R/W	Reserved								80h
DC57	139h	R/W	Reserved								80h
DC58	13Ah	R/W	Reserved								80h
DC59	13Bh	R/W	Reserved								80h
DC60	13Ch	R/W	Reserved								80h
DC61	13Dh	R/W	Reserved								80h
DC62	13Eh	R/W	LED dot current setting for Dot L3-CSB0								80h
DC63	13Fh	R/W	LED dot current setting for Dot L3-CSR1								80h
DC64	140h	R/W	Reserved								80h
DC65	141h	R/W	Reserved								80h
DC66	142h	R/W	Reserved								80h
DC67	143h	R/W	Reserved								80h
DC68	144h	R/W	Reserved								80h
DC69	145h	R/W	Reserved								80h
DC70	146h	R/W	LED dot current setting for Dot L3-CSG1								80h
DC71	147h	R/W	LED dot current setting for Dot L3-CSB1								80h
DC72	148h	R/W	LED dot current setting for Dot L4-CSR0								80h
DC73	149h	R/W	LED dot current setting for Dot L4-CSG0								80h
DC74	14Ah	R/W	Reserved								80h
DC75	14Bh	R/W	Reserved								80h
DC76	14Ch	R/W	Reserved								80h
DC77	14Dh	R/W	Reserved								80h
DC78	14Eh	R/W	Reserved								80h
DC79	14Fh	R/W	Reserved								80h
DC80	150h	R/W	LED dot current setting for Dot L4-CSB0								80h
DC81	151h	R/W	LED dot current setting for Dot L4-CSR1								80h
DC82	152h	R/W	Reserved								80h
DC83	153h	R/W	Reserved								80h
DC84	154h	R/W	Reserved								80h
DC85	155h	R/W	Reserved								80h
DC86	156h	R/W	Reserved								80h
DC87	157h	R/W	Reserved								80h
DC88	158h	R/W	LED dot current setting for Dot L4-CSG1								80h
DC89	159h	R/W	LED dot current setting for Dot L4-CSB1								80h
DC90	15Ah	R/W	LED dot current setting for Dot L5-CSR0								80h
DC91	15Bh	R/W	LED dot current setting for Dot L5-CSG0								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC92	15Ch	R/W	Reserved								80h
DC93	15Dh	R/W	Reserved								80h
DC94	15Eh	R/W	Reserved								80h
DC95	15Fh	R/W	Reserved								80h
DC96	160h	R/W	Reserved								80h
DC97	161h	R/W	Reserved								80h
DC98	162h	R/W	LED dot current setting for Dot L5-CSB0								80h
DC99	163h	R/W	LED dot current setting for Dot L5-CSR1								80h
DC100	164h	R/W	Reserved								80h
DC101	165h	R/W	Reserved								80h
DC102	166h	R/W	Reserved								80h
DC103	167h	R/W	Reserved								80h
DC104	168h	R/W	Reserved								80h
DC105	169h	R/W	Reserved								80h
DC106	16Ah	R/W	LED dot current setting for Dot L5-CSG1								80h
DC107	16Bh	R/W	LED dot current setting for Dot L5-CSB1								80h
DC108	16Ch	R/W	LED dot current setting for Dot L6-CSR0								80h
DC109	16Dh	R/W	LED dot current setting for Dot L6-CSG0								80h
DC110	16Eh	R/W	Reserved								80h
DC111	16Fh	R/W	Reserved								80h
DC112	170h	R/W	Reserved								80h
DC113	171h	R/W	Reserved								80h
DC114	172h	R/W	Reserved								80h
DC115	173h	R/W	Reserved								80h
DC116	174h	R/W	LED dot current setting for Dot L6-CSB0								80h
DC117	175h	R/W	LED dot current setting for Dot L6-CSR1								80h
DC118	176h	R/W	Reserved								80h
DC119	177h	R/W	Reserved								80h
DC120	178h	R/W	Reserved								80h
DC121	179h	R/W	Reserved								80h
DC122	17Ah	R/W	Reserved								80h
DC123	17Bh	R/W	Reserved								80h
DC124	17Ch	R/W	LED dot current setting for Dot L6-CSG1								80h
DC125	17Dh	R/W	LED dot current setting for Dot L6-CSB1								80h
pwm_bri0	200h	R/W	8-bits PWM for Dot L0-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSR0								00h
pwm_bri1	201h	R/W	8-bits PWM for Dot L0-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSR0								00h
pwm_bri2	202h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L0-CSG0								00h
pwm_bri3	203h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L0-CSG0								00h
pwm_bri4	204h	R/W	Reserved								00h
pwm_bri5	205h	R/W	Reserved								00h
pwm_bri6	206h	R/W	Reserved								00h
pwm_bri7	207h	R/W	Reserved								00h
pwm_bri8	208h	R/W	8-bits PWM for Dot L0-CSB0								00h
pwm_bri9	209h	R/W	8-bits PWM for Dot L0-CSR1								00h
pwm_bri10	20Ah	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri11	20Bh	R/W	Reserved								00h
pwm_bri12	20Ch	R/W	Reserved								00h
pwm_bri13	20Dh	R/W	Reserved								00h
pwm_bri14	20Eh	R/W	Reserved								00h
pwm_bri15	20Fh	R/W	Reserved								00h
pwm_bri16	210h	R/W	8-bits PWM for Dot L0-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSB0								00h
pwm_bri17	211h	R/W	8-bits PWM for Dot L0-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSB0								00h
pwm_bri18	212h	R/W	8-bits PWM for Dot L1-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSR1								00h
pwm_bri19	213h	R/W	8-bits PWM for Dot L1-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSR1								00h
pwm_bri20	214h	R/W	Reserved								00h
pwm_bri21	215h	R/W	Reserved								00h
pwm_bri22	216h	R/W	Reserved								00h
pwm_bri23	217h	R/W	Reserved								00h
pwm_bri24	218h	R/W	Reserved								00h
pwm_bri25	219h	R/W	Reserved								00h
pwm_bri26	21Ah	R/W	8-bits PWM for Dot L1-CSB0								00h
pwm_bri27	21Bh	R/W	8-bits PWM for Dot L1-CSR1								00h
pwm_bri28	21Ch	R/W	Reserved								00h
pwm_bri29	21Dh	R/W	Reserved								00h
pwm_bri30	21Eh	R/W	Reserved								00h
pwm_bri31	21Fh	R/W	Reserved								00h
pwm_bri32	220h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L0-CSG1								00h
pwm_bri33	221h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L0-CSG1								00h
pwm_bri34	222h	R/W	8-bits PWM for Dot L1-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSB1								00h
pwm_bri35	223h	R/W	8-bits PWM for Dot L1-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSB1								00h
pwm_bri36	224h	R/W	8-bits PWM for Dot L2-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSR0								00h
pwm_bri37	225h	R/W	8-bits PWM for Dot L2-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSR0								00h
pwm_bri38	226h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CSG0								00h
pwm_bri39	227h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CSG0								00h
pwm_bri40	228h	R/W	Reserved								00h
pwm_bri41	229h	R/W	Reserved								00h
pwm_bri42	22Ah	R/W	Reserved								00h
pwm_bri43	22Bh	R/W	Reserved								00h
pwm_bri44	22Ch	R/W	8-bits PWM for Dot L2-CSB0								00h
pwm_bri45	22Dh	R/W	8-bits PWM for Dot L2-CSR1								00h
pwm_bri46	22Eh	R/W	Reserved								00h
pwm_bri47	22Fh	R/W	Reserved								00h
pwm_bri48	230h	R/W	Reserved								00h
pwm_bri49	231h	R/W	Reserved								00h
pwm_bri50	232h	R/W	Reserved								00h
pwm_bri51	233h	R/W	Reserved								00h
pwm_bri52	234h	R/W	8-bits PWM for Dot L2-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSB0								00h
pwm_bri53	235h	R/W	8-bits PWM for Dot L2-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSB0								00h
pwm_bri54	236h	R/W	8-bits PWM for Dot L3-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSR1								00h
pwm_bri55	237h	R/W	8-bits PWM for Dot L3-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSR1								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri56	238h	R/W	Reserved								00h
pwm_bri57	239h	R/W	Reserved								00h
pwm_bri58	23Ah	R/W	Reserved								00h
pwm_bri59	23Bh	R/W	Reserved								00h
pwm_bri60	23Ch	R/W	Reserved								00h
pwm_bri61	23Dh	R/W	Reserved								00h
pwm_bri62	23Eh	R/W	8-bits PWM for Dot L3-CSB0								00h
pwm_bri63	23Fh	R/W	8-bits PWM for Dot L3-CSR1								00h
pwm_bri64	240h	R/W	Reserved								00h
pwm_bri65	241h	R/W	Reserved								00h
pwm_bri66	242h	R/W	Reserved								00h
pwm_bri67	243h	R/W	Reserved								00h
pwm_bri68	244h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CSG1								00h
pwm_bri69	245h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CSG1								00h
pwm_bri70	246h	R/W	8-bits PWM for Dot L3-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSB1								00h
pwm_bri71	247h	R/W	8-bits PWM for Dot L3-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSB1								00h
pwm_bri72	248h	R/W	8-bits PWM for Dot L4-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSR0								00h
pwm_bri73	249h	R/W	8-bits PWM for Dot L4-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSR0								00h
pwm_bri74	24Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L2-CSG0								00h
pwm_bri75	24Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L2-CSG0								00h
pwm_bri76	24Ch	R/W	Reserved								00h
pwm_bri77	24Dh	R/W	Reserved								00h
pwm_bri78	24Eh	R/W	Reserved								00h
pwm_bri79	24Fh	R/W	Reserved								00h
pwm_bri80	250h	R/W	8-bits PWM for Dot L4-CSB0								00h
pwm_bri81	251h	R/W	8-bits PWM for Dot L4-CSR1								00h
pwm_bri82	252h	R/W	Reserved								00h
pwm_bri83	253h	R/W	Reserved								00h
pwm_bri84	254h	R/W	Reserved								00h
pwm_bri85	255h	R/W	Reserved								00h
pwm_bri86	256h	R/W	Reserved								00h
pwm_bri87	257h	R/W	Reserved								00h
pwm_bri88	258h	R/W	8-bits PWM for Dot L4-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSB0								00h
pwm_bri89	259h	R/W	8-bits PWM for Dot L4-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSB0								00h
pwm_bri90	25Ah	R/W	8-bits PWM for Dot L5-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSR1								00h
pwm_bri91	25Bh	R/W	8-bits PWM for Dot L5-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSR1								00h
pwm_bri92	25Ch	R/W	Reserved								00h
pwm_bri93	25Dh	R/W	Reserved								00h
pwm_bri94	25Eh	R/W	Reserved								00h
pwm_bri95	25Fh	R/W	Reserved								00h
pwm_bri96	260h	R/W	Reserved								00h
pwm_bri97	261h	R/W	Reserved								00h
pwm_bri98	262h	R/W	8-bits PWM for Dot L5-CSB0								00h
pwm_bri99	263h	R/W	8-bits PWM for Dot L5-CSR1								00h
pwm_bri100	264h	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri101	265h	R/W	Reserved								00h
pwm_bri102	266h	R/W	Reserved								00h
pwm_bri103	267h	R/W	Reserved								00h
pwm_bri104	268h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L2-CSG1								00h
pwm_bri105	269h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L2-CSG1								00h
pwm_bri106	26Ah	R/W	8-bits PWM for Dot L5-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSB1								00h
pwm_bri107	26Bh	R/W	8-bits PWM for Dot L5-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSB1								00h
pwm_bri108	26Ch	R/W	8-bits PWM for Dot L6-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L3-CSR0								00h
pwm_bri109	26Dh	R/W	8-bits PWM for Dot L6-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L3-CSR0								00h
pwm_bri110	26Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSG0								00h
pwm_bri111	26Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSG0								00h
pwm_bri112	270h	R/W	Reserved								00h
pwm_bri113	271h	R/W	Reserved								00h
pwm_bri114	272h	R/W	Reserved								00h
pwm_bri115	273h	R/W	Reserved								00h
pwm_bri116	274h	R/W	8-bits PWM for Dot L6-CSB0								00h
pwm_bri117	275h	R/W	8-bits PWM for Dot L6-CSR1								00h
pwm_bri118	276h	R/W	Reserved								00h
pwm_bri119	277h	R/W	Reserved								00h
pwm_bri120	278h	R/W	Reserved								00h
pwm_bri121	279h	R/W	Reserved								00h
pwm_bri122	27Ah	R/W	Reserved								00h
pwm_bri123	27Bh	R/W	Reserved								00h
pwm_bri124	27Ch	R/W	8-bits PWM for Dot L6-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L3-CSB0								00h
pwm_bri125	27Dh	R/W	8-bits PWM for Dot L6-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L3-CSB0								00h
pwm_bri126	27Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSR1								00h
pwm_bri127	27Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSR1								00h
pwm_bri128	280h	R/W	Reserved								00h
pwm_bri129	281h	R/W	Reserved								00h
pwm_bri130	282h	R/W	Reserved								00h
pwm_bri131	283h	R/W	Reserved								00h
pwm_bri132	284h	R/W	Reserved								00h
pwm_bri133	285h	R/W	Reserved								00h
pwm_bri134	286h	R/W	8-bits PWM for Dot L7-CSB0								00h
pwm_bri135	287h	R/W	8-bits PWM for Dot L7-CSR1								00h
pwm_bri136	288h	R/W	Reserved								00h
pwm_bri137	289h	R/W	Reserved								00h
pwm_bri138	28Ah	R/W	Reserved								00h
pwm_bri139	28Bh	R/W	Reserved								00h
pwm_bri140	28Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSG1								00h
pwm_bri141	28Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSG1								00h
pwm_bri142	28Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSB1								00h
pwm_bri143	28Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSB1								00h
pwm_bri144	290h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSR0								00h
pwm_bri145	291h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSR0								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri146	292h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSG0								00h
pwm_bri147	293h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSG0								00h
pwm_bri148	294h	R/W	Reserved								00h
pwm_bri149	295h	R/W	Reserved								00h
pwm_bri150	296h	R/W	Reserved								00h
pwm_bri151	297h	R/W	Reserved								00h
pwm_bri152	298h	R/W	Reserved								00h
pwm_bri153	299h	R/W	Reserved								00h
pwm_bri154	29Ah	R/W	Reserved								00h
pwm_bri155	29Bh	R/W	Reserved								00h
pwm_bri156	29Ch	R/W	Reserved								00h
pwm_bri157	29Dh	R/W	Reserved								00h
pwm_bri158	29Eh	R/W	Reserved								00h
pwm_bri159	29Fh	R/W	Reserved								00h
pwm_bri160	2A0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSB0								00h
pwm_bri161	2A1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSB0								00h
pwm_bri162	2A2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSR1								00h
pwm_bri163	2A3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSR1								00h
pwm_bri164	2A4h	R/W	Reserved								00h
pwm_bri165	2A5h	R/W	Reserved								00h
pwm_bri166	2A6h	R/W	Reserved								00h
pwm_bri167	2A7h	R/W	Reserved								00h
pwm_bri168	2A8h	R/W	Reserved								00h
pwm_bri169	2A9h	R/W	Reserved								00h
pwm_bri170	2AAh	R/W	Reserved								00h
pwm_bri171	2ABh	R/W	Reserved								00h
pwm_bri172	2ACh	R/W	Reserved								00h
pwm_bri173	2ADh	R/W	Reserved								00h
pwm_bri174	2AEh	R/W	Reserved								00h
pwm_bri175	2AFh	R/W	Reserved								00h
pwm_bri176	2B0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSG1								00h
pwm_bri177	2B1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSG1								00h
pwm_bri178	2B2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSB1								00h
pwm_bri179	2B3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSB1								00h
pwm_bri180	2B4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSR0								00h
pwm_bri181	2B5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSR0								00h
pwm_bri182	2B6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSG0								00h
pwm_bri183	2B7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSG0								00h
pwm_bri184	2B8h	R/W	Reserved								00h
pwm_bri185	2B9h	R/W	Reserved								00h
pwm_bri186	2BAh	R/W	Reserved								00h
pwm_bri187	2BBh	R/W	Reserved								00h
pwm_bri188	2BCh	R/W	Reserved								00h
pwm_bri189	2BDh	R/W	Reserved								00h
pwm_bri190	2BEh	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri191	2BFh	R/W	Reserved								00h
pwm_bri192	2C0h	R/W	Reserved								00h
pwm_bri193	2C1h	R/W	Reserved								00h
pwm_bri194	2C2h	R/W	Reserved								00h
pwm_bri195	2C3h	R/W	Reserved								00h
pwm_bri196	2C4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSB0								00h
pwm_bri197	2C5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSB0								00h
pwm_bri198	2C6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSR1								00h
pwm_bri199	2C7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSR1								00h
pwm_bri200	2C8h	R/W	Reserved								00h
pwm_bri201	2C9h	R/W	Reserved								00h
pwm_bri202	2CAh	R/W	Reserved								00h
pwm_bri203	2CBh	R/W	Reserved								00h
pwm_bri204	2CCh	R/W	Reserved								00h
pwm_bri205	2CDh	R/W	Reserved								00h
pwm_bri206	2CEh	R/W	Reserved								00h
pwm_bri207	2CFh	R/W	Reserved								00h
pwm_bri208	2D0h	R/W	Reserved								00h
pwm_bri209	2D1h	R/W	Reserved								00h
pwm_bri210	2D2h	R/W	Reserved								00h
pwm_bri211	2D3h	R/W	Reserved								00h
pwm_bri212	2D4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSG1								00h
pwm_bri213	2D5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSG1								00h
pwm_bri214	2D6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSB1								00h
pwm_bri215	2D7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSB1								00h
pwm_bri216	2D8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSR0								00h
pwm_bri217	2D9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSR0								00h
pwm_bri218	2DAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSG0								00h
pwm_bri219	2DBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSG0								00h
pwm_bri220	2DCh	R/W	Reserved								00h
pwm_bri221	2DDh	R/W	Reserved								00h
pwm_bri222	2DEh	R/W	Reserved								00h
pwm_bri223	2DFh	R/W	Reserved								00h
pwm_bri224	2E0h	R/W	Reserved								00h
pwm_bri225	2E1h	R/W	Reserved								00h
pwm_bri226	2E2h	R/W	Reserved								00h
pwm_bri227	2E3h	R/W	Reserved								00h
pwm_bri228	2E4h	R/W	Reserved								00h
pwm_bri229	2E5h	R/W	Reserved								00h
pwm_bri230	2E6h	R/W	Reserved								00h
pwm_bri231	2E7h	R/W	Reserved								00h
pwm_bri232	2E8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSB0								00h
pwm_bri233	2E9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSB0								00h
pwm_bri234	2EAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSR1								00h
pwm_bri235	2EBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSR1								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri236	2ECh	R/W	Reserved								00h
pwm_bri237	2EDh	R/W	Reserved								00h
pwm_bri238	2EEh	R/W	Reserved								00h
pwm_bri239	2EFh	R/W	Reserved								00h
pwm_bri240	2F0h	R/W	Reserved								00h
pwm_bri241	2F1h	R/W	Reserved								00h
pwm_bri242	2F2h	R/W	Reserved								00h
pwm_bri243	2F3h	R/W	Reserved								00h
pwm_bri244	2F4h	R/W	Reserved								00h
pwm_bri245	2F5h	R/W	Reserved								00h
pwm_bri246	2F6h	R/W	Reserved								00h
pwm_bri247	2F7h	R/W	Reserved								00h
pwm_bri248	2F8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSG1								00h
pwm_bri249	2F9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSG1								00h
pwm_bri250	2FAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSB1								00h
pwm_bri251	2FBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSB1								00h

8 Register Maps

This section provides a summary of the register maps. For detailed register functions and descriptions, please refer to *LP5867 7x6 LED Matrix Driver Register Maps* .

表 8-1. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Chip_en	000h	R/W	Reserved							Chip_EN	00h
Dev_initial	001h	R/W	Reserved	Max_Line_Num				Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved	Reserved	Reserved	Reserved	SW_BLK	PWM_Scale_Mode	PWM_Phase_Shift	CS_ON_Shift	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		LOD_removal	LSD_removal	00h
Dev_config3	004h	R/W	Down_Deghost		Up_Deghost		Maximum_Current			Up_Deghost_enable	47h
Global_bri	005h	R/W	PWM_Global								FFh
Group0_bri	006h	R/W	PWM_Group1								FFh
Group1_bri	007h	R/W	PWM_Group2								FFh
Group2_bri	008h	R/W	PWM_Group3								FFh
R_current_set	009h	R/W	Reserved	CC_Group1							40h
G_current_set	00Ah	R/W	Reserved	CC_Group2							40h
B_current_set	00Bh	R/W	Reserved	CC_Group3							40h
Dot_grp_sel0	00Ch	R/W	Reserved				Dot L0-CSG0 group		Dot L0-CSR0 group		00h
Dot_grp_sel1	00Dh	R/W	Reserved								00h
Dot_grp_sel2	00Eh	R/W	Reserved				Dot L0-CSR1 group		Dot L0-CSB0 group		00h
Dot_grp_sel3	00Fh	R/W	Reserved								00h
Dot_grp_sel4	010h	R/W	Reserved				Dot L0-CSB1 group		Dot L0-CSG1 group		00h
Dot_grp_sel5	011h	R/W	Reserved				Dot L1-CSG0 group		Dot L1-CSR0 group		00h
Dot_grp_sel6	012h	R/W	Reserved								00h
Dot_grp_sel7	013h	R/W	Reserved				Dot L1-CSR1 group		Dot L1-CSB0 group		00h
Dot_grp_sel8	014h	R/W	Reserved								00h
Dot_grp_sel9	015h	R/W	Reserved				Dot L1-CSB1 group		Dot L1-CSG1 group		00h
Dot_grp_sel10	016h	R/W	Reserved				Dot L2-CSG0 group		Dot L2-CSR0 group		00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_grp_sel11	017h	R/W	Reserved								00h
Dot_grp_sel12	018h	R/W	Reserved				Dot L2-CSR1 group		Dot L2-CSB0 group		00h
Dot_grp_sel13	019h	R/W	Reserved								00h
Dot_grp_sel14	01Ah	R/W	Reserved				Dot L2-CSB1 group		Dot L2-CSG1 group		00h
Dot_grp_sel15	01Bh	R/W	Reserved				Dot L3-CSG0 group		Dot L3-CSR0 group		00h
Dot_grp_sel16	01Ch	R/W	Reserved								00h
Dot_grp_sel17	01Dh	R/W	Reserved				Dot L3-CSR1 group		Dot L3-CSB0 group		00h
Dot_grp_sel18	01Eh	R/W	Reserved								00h
Dot_grp_sel19	01Fh	R/W	Reserved				Dot L3-CSB1 group		Dot L3-CSG1 group		00h
Dot_grp_sel20	020h	R/W	Reserved				Dot L4-CSG0 group		Dot L4-CSR0 group		00h
Dot_grp_sel21	021h	R/W	Reserved								00h
Dot_grp_sel22	022h	R/W	Reserved				Dot L4-CSR1 group		Dot L4-CSB0 group		00h
Dot_grp_sel23	023h	R/W	Reserved								00h
Dot_grp_sel24	024h	R/W	Reserved				Dot L4-CSB1 group		Dot L4-CSG1 group		00h
Dot_grp_sel25	025h	R/W	Reserved				Dot L5-CSG0 group		Dot L5-CSR0 group		00h
Dot_grp_sel26	026h	R/W	Reserved								00h
Dot_grp_sel27	027h	R/W	Reserved				Dot L5-CSR1 group		Dot L5-CSB0 group		00h
Dot_grp_sel28	028h	R/W	Reserved								00h
Dot_grp_sel29	029h	R/W	Reserved				Dot L5-CSB1 group		Dot L5-CSG1 group		00h
Dot_grp_sel30	02Ah	R/W	Reserved				Dot L6-CSG0 group		Dot L6-CSR0 group		00h
Dot_grp_sel31	02Bh	R/W	Reserved								00h
Dot_grp_sel32	02Ch	R/W	Reserved				Dot L6-CSR1 group		Dot L6-CSB0 group		00h
Dot_grp_sel33	02Dh	R/W	Reserved								00h
Dot_grp_sel34	02Eh	R/W	Reserved				Dot L6-CSB1 group		Dot L6-CSG1 group		00h
Dot_onoff0	043h	R/W	Reserved						Dot L0-CSG0 onoff	Dot L0-CSR0 onoff	FFh
Dot_onoff1	044h	R/W	Reserved						Dot L0-CSR1 onoff	Dot L0-CSB0 onoff	FFh
Dot_onoff2	045h	R/W	Reserved						Dot L0-CSB1 onoff	Dot L0-CSG1 onoff	03h
Dot_onoff3	046h	R/W	Reserved						Dot L1-CSG0 onoff	Dot L1-CSR0 onoff	FFh
Dot_onoff4	047h	R/W	Reserved						Dot L1-CSR1 onoff	Dot L1-CSB0 onoff	FFh
Dot_onoff5	048h	R/W	Reserved						Dot L1-CSB1 onoff	Dot L1-CSG1 onoff	03h
Dot_onoff6	049h	R/W	Reserved						Dot L2-CSG0 onoff	Dot L2-CSR0 onoff	FFh
Dot_onoff7	04Ah	R/W	Reserved						Dot L2-CSR1 onoff	Dot L2-CSB0 onoff	FFh
Dot_onoff8	04Bh	R/W	Reserved						Dot L2-CSB1 onoff	Dot L2-CSG1 onoff	03h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_onoff9	04Ch	R/W	Reserved						Dot L3-CSG0 onoff	Dot L3-CSR0 onoff	FFh
Dot_onoff10	04Dh	R/W	Reserved						Dot L3-CSR1 onoff	Dot L3-CSB0 onoff	FFh
Dot_onoff11	04Eh	R/W	Reserved						Dot L3-CSB1 onoff	Dot L3-CSG1 onoff	03h
Dot_onoff12	04Fh	R/W	Reserved						Dot L4-CSG0 onoff	Dot L4-CSR0 onoff	FFh
Dot_onoff13	050h	R/W	Reserved						Dot L4-CSR1 onoff	Dot L4-CSB0 onoff	FFh
Dot_onoff14	051h	R/W	Reserved						Dot L4-CSB1 onoff	Dot L4-CSG1 onoff	03h
Dot_onoff15	052h	R/W	Reserved						Dot L5-CSG0 onoff	Dot L5-CSR0 onoff	FFh
Dot_onoff16	053h	R/W	Reserved						Dot L5-CSR1 onoff	Dot L5-CSB0 onoff	FFh
Dot_onoff17	054h	R/W	Reserved						Dot L5-CSB1 onoff	Dot L5-CSG1 onoff	03h
Dot_onoff18	055h	R/W	Reserved						Dot L6-CSG0 onoff	Dot L6-CSR0 onoff	FFh
Dot_onoff19	056h	R/W	Reserved						Dot L6-CSR1 onoff	Dot L6-CSB0 onoff	FFh
Dot_onoff20	057h	R/W	Reserved						Dot L6-CSB1 onoff	Dot L6-CSG1 onoff	03h
Fault_state	064h	R	Reserved						Global_LOD	Global_LSD	00h
Dot_lod0	065h	R	Reserved						Dot L0-CSG0 LOD	Dot L0-CSR0 LOD	00h
Dot_lod1	066h	R	Reserved						Dot L0-CSR1 LOD	Dot L0-CSB0 LOD	00h
Dot_lod2	067h	R	Reserved						Dot L0-CSB1 LOD	Dot L0-CSG1 LOD	00h
Dot_lod3	068h	R	Reserved						Dot L1-CSG0 LOD	Dot L1-CSR0 LOD	00h
Dot_lod4	069h	R	Reserved						Dot L1-CSR1 LOD	Dot L1-CSB0 LOD	00h
Dot_lod5	06Ah	R	Reserved						Dot L1-CSB1 LOD	Dot L1-CSG1 LOD	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_lod6	06Bh	R	Reserved						Dot L2-CSG0 LOD	Dot L2-CSR0 LOD	00h
Dot_lod7	06Ch	R	Reserved						Dot L2-CSR1 LOD	Dot L2-CSB0 LOD	00h
Dot_lod8	06Dh	R	Reserved						Dot L2-CSB1 LOD	Dot L2-CSG1 LOD	00h
Dot_lod9	06Eh	R	Reserved						Dot L3-CSG0 LOD	Dot L3-CSR0 LOD	00h
Dot_lod10	06Fh	R	Reserved						Dot L3-CSR1 LOD	Dot L3-CSB0 LOD	00h
Dot_lod11	070h	R	Reserved						Dot L3-CSB1 LOD	Dot L3-CSG1 LOD	00h
Dot_lod12	071h	R	Reserved						Dot L4-CSG0 LOD	Dot L4-CSR0 LOD	00h
Dot_lod13	072h	R	Reserved						Dot L4-CSR1 LOD	Dot L4-CSB0 LOD	00h
Dot_lod14	073h	R	Reserved						Dot L4-CSB1 LOD	Dot L4-CSG1 LOD	00h
Dot_lod15	074h	R	Reserved						Dot L5-CSG0 LOD	Dot L5-CSR0 LOD	00h
Dot_lod16	075h	R	Reserved						Dot L5-CSR1 LOD	Dot L5-CSB0 LOD	00h
Dot_lod17	076h	R	Reserved						Dot L5-CSB1 LOD	Dot L5-CSG1 LOD	00h
Dot_lod18	077h	R	Reserved						Dot L6-CSG0 LOD	Dot L6-CSR0 LOD	00h
Dot_lod19	078h	R	Reserved						Dot L6-CSR1 LOD	Dot L6-CSB0 LOD	00h
Dot_lod20	079h	R	Reserved						Dot L6-CSB1 LOD	Dot L6-CSG1 LOD	00h
Dot_lsd0	086h	R	Reserved						Dot L0-CSG0 LSD	Dot L0-CSR0 LSD	00h
Dot_lsd1	087h	R	Reserved						Dot L0-CSR1 LSD	Dot L0-CSB0 LSD	00h
Dot_lsd2	088h	R	Reserved						Dot L0-CSB1 LSD	Dot L0-CSG1 LSD	00h
Dot_lsd3	089h	R	Reserved						Dot L1-CSG0 LSD	Dot L1-CSR0 LSD	00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Dot_lsd4	08Ah	R	Reserved						Dot L1-CSR1 LSD	Dot L1-CSB0 LSD	00h
Dot_lsd5	08Bh	R	Reserved						Dot L1-CSB1 LSD	Dot L1-CSG1 LSD	00h
Dot_lsd6	08Ch	R	Reserved						Dot L2-CSG0 LSD	Dot L2-CSR0 LSD	00h
Dot_lsd7	08Dh	R	Reserved						Dot L2-CSR1 LSD	Dot L2-CSB0 LSD	00h
Dot_lsd8	08Eh	R	Reserved						Dot L2-CSB1 LSD	Dot L2-CSG1 LSD	00h
Dot_lsd9	08Fh	R	Reserved						Dot L3-CSG0 LSD	Dot L3-CSR0 LSD	00h
Dot_lsd10	090h	R	Reserved						Dot L3-CSR1 LSD	Dot L3-CSB0 LSD	00h
Dot_lsd11	091h	R	Reserved						Dot L3-CSB1 LSD	Dot L3-CSG1 LSD	00h
Dot_lsd12	092h	R	Reserved						Dot L4-CSG0 LSD	Dot L4-CSR0 LSD	00h
Dot_lsd13	093h	R	Reserved						Dot L4-CSR1 LSD	Dot L4-CSB0 LSD	00h
Dot_lsd14	094h	R	Reserved						Dot L4-CSB1 LSD	Dot L4-CSG1 LSD	00h
Dot_lsd15	095h	R	Reserved						Dot L5-CSG0 LSD	Dot L5-CSR0 LSD	00h
Dot_lsd16	096h	R	Reserved						Dot L5-CSR1 LSD	Dot L5-CSB0 LSD	00h
Dot_lsd17	097h	R	Reserved						Dot L5-CSB1 LSD	Dot L5-CSG1 LSD	00h
Dot_lsd18	098h	R	Reserved						Dot L6-CSG0 LSD	Dot L6-CSR0 LSD	00h
Dot_lsd19	099h	R	Reserved						Dot L6-CSR1 LSD	Dot L6-CSB0 LSD	00h
Dot_lsd20	09Ah	R	Reserved						Dot L6-CSB1 LSD	Dot L6-CSG1 LSD	00h
LOD_clear	0A7h	W	Reserved				LOD_Clear				00h
LSD_clear	0A8h	W	Reserved				LSD_Clear				00h
Reset	0A9h	W	Reset								00h
DC0	100h	R/W	LED dot current setting for Dot L0-CSR0								80h
DC1	101h	R/W	LED dot current setting for Dot L0-CSG0								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC2	102h	R/W	Reserved								80h
DC3	103h	R/W	Reserved								80h
DC4	104h	R/W	Reserved								80h
DC5	105h	R/W	Reserved								80h
DC6	106h	R/W	Reserved								80h
DC7	107h	R/W	Reserved								80h
DC8	108h	R/W	LED dot current setting for Dot L0-CSB0								80h
DC9	109h	R/W	LED dot current setting for Dot L0-CSR1								80h
DC10	10Ah	R/W	Reserved								80h
DC11	10Bh	R/W	Reserved								80h
DC12	10Ch	R/W	Reserved								80h
DC13	10Dh	R/W	Reserved								80h
DC14	10Eh	R/W	Reserved								80h
DC15	10Fh	R/W	Reserved								80h
DC16	110h	R/W	LED dot current setting for Dot L0-CSG1								80h
DC17	111h	R/W	LED dot current setting for Dot L0-CSB1								80h
DC18	112h	R/W	LED dot current setting for Dot L1-CSR0								80h
DC19	113h	R/W	LED dot current setting for Dot L1-CSG0								80h
DC20	114h	R/W	Reserved								80h
DC21	115h	R/W	Reserved								80h
DC22	116h	R/W	Reserved								80h
DC23	117h	R/W	Reserved								80h
DC24	118h	R/W	Reserved								80h
DC25	119h	R/W	Reserved								80h
DC26	11Ah	R/W	LED dot current setting for Dot L1-CSB0								80h
DC27	11Bh	R/W	LED dot current setting for Dot L1-CSR1								80h
DC28	11Ch	R/W	Reserved								80h
DC29	11Dh	R/W	Reserved								80h
DC30	11Eh	R/W	Reserved								80h
DC31	11Fh	R/W	Reserved								80h
DC32	120h	R/W	Reserved								80h
DC33	121h	R/W	Reserved								80h
DC34	122h	R/W	LED dot current setting for Dot L1-CSG1								80h
DC35	123h	R/W	LED dot current setting for Dot L1-CSB1								80h
DC36	124h	R/W	LED dot current setting for Dot L2-CSR0								80h
DC37	125h	R/W	LED dot current setting for Dot L2-CSG0								80h
DC38	126h	R/W	Reserved								80h
DC39	127h	R/W	Reserved								80h
DC40	128h	R/W	Reserved								80h
DC41	129h	R/W	Reserved								80h
DC42	12Ah	R/W	Reserved								80h
DC43	12Bh	R/W	Reserved								80h
DC44	12Ch	R/W	LED dot current setting for Dot L2-CSB0								80h
DC45	12Dh	R/W	LED dot current setting for Dot L2-CSR1								80h
DC46	12Eh	R/W	Reserved								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC47	12Fh	R/W	Reserved								80h
DC48	130h	R/W	Reserved								80h
DC49	131h	R/W	Reserved								80h
DC50	132h	R/W	Reserved								80h
DC51	133h	R/W	Reserved								80h
DC52	134h	R/W	LED dot current setting for Dot L2-CSG1								80h
DC53	135h	R/W	LED dot current setting for Dot L2-CSB1								80h
DC54	136h	R/W	LED dot current setting for Dot L3-CSR0								80h
DC55	137h	R/W	LED dot current setting for Dot L3-CSG0								80h
DC56	138h	R/W	Reserved								80h
DC57	139h	R/W	Reserved								80h
DC58	13Ah	R/W	Reserved								80h
DC59	13Bh	R/W	Reserved								80h
DC60	13Ch	R/W	Reserved								80h
DC61	13Dh	R/W	Reserved								80h
DC62	13Eh	R/W	LED dot current setting for Dot L3-CSB0								80h
DC63	13Fh	R/W	LED dot current setting for Dot L3-CSR1								80h
DC64	140h	R/W	Reserved								80h
DC65	141h	R/W	Reserved								80h
DC66	142h	R/W	Reserved								80h
DC67	143h	R/W	Reserved								80h
DC68	144h	R/W	Reserved								80h
DC69	145h	R/W	Reserved								80h
DC70	146h	R/W	LED dot current setting for Dot L3-CSG1								80h
DC71	147h	R/W	LED dot current setting for Dot L3-CSB1								80h
DC72	148h	R/W	LED dot current setting for Dot L4-CSR0								80h
DC73	149h	R/W	LED dot current setting for Dot L4-CSG0								80h
DC74	14Ah	R/W	Reserved								80h
DC75	14Bh	R/W	Reserved								80h
DC76	14Ch	R/W	Reserved								80h
DC77	14Dh	R/W	Reserved								80h
DC78	14Eh	R/W	Reserved								80h
DC79	14Fh	R/W	Reserved								80h
DC80	150h	R/W	LED dot current setting for Dot L4-CSB0								80h
DC81	151h	R/W	LED dot current setting for Dot L4-CSR1								80h
DC82	152h	R/W	Reserved								80h
DC83	153h	R/W	Reserved								80h
DC84	154h	R/W	Reserved								80h
DC85	155h	R/W	Reserved								80h
DC86	156h	R/W	Reserved								80h
DC87	157h	R/W	Reserved								80h
DC88	158h	R/W	LED dot current setting for Dot L4-CSG1								80h
DC89	159h	R/W	LED dot current setting for Dot L4-CSB1								80h
DC90	15Ah	R/W	LED dot current setting for Dot L5-CSR0								80h
DC91	15Bh	R/W	LED dot current setting for Dot L5-CSG0								80h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC92	15Ch	R/W	Reserved								80h
DC93	15Dh	R/W	Reserved								80h
DC94	15Eh	R/W	Reserved								80h
DC95	15Fh	R/W	Reserved								80h
DC96	160h	R/W	Reserved								80h
DC97	161h	R/W	Reserved								80h
DC98	162h	R/W	LED dot current setting for Dot L5-CSB0								80h
DC99	163h	R/W	LED dot current setting for Dot L5-CSR1								80h
DC100	164h	R/W	Reserved								80h
DC101	165h	R/W	Reserved								80h
DC102	166h	R/W	Reserved								80h
DC103	167h	R/W	Reserved								80h
DC104	168h	R/W	Reserved								80h
DC105	169h	R/W	Reserved								80h
DC106	16Ah	R/W	LED dot current setting for Dot L5-CSG1								80h
DC107	16Bh	R/W	LED dot current setting for Dot L5-CSB1								80h
DC108	16Ch	R/W	LED dot current setting for Dot L6-CSR0								80h
DC109	16Dh	R/W	LED dot current setting for Dot L6-CSG0								80h
DC110	16Eh	R/W	Reserved								80h
DC111	16Fh	R/W	Reserved								80h
DC112	170h	R/W	Reserved								80h
DC113	171h	R/W	Reserved								80h
DC114	172h	R/W	Reserved								80h
DC115	173h	R/W	Reserved								80h
DC116	174h	R/W	LED dot current setting for Dot L6-CSB0								80h
DC117	175h	R/W	LED dot current setting for Dot L6-CSR1								80h
DC118	176h	R/W	Reserved								80h
DC119	177h	R/W	Reserved								80h
DC120	178h	R/W	Reserved								80h
DC121	179h	R/W	Reserved								80h
DC122	17Ah	R/W	Reserved								80h
DC123	17Bh	R/W	Reserved								80h
DC124	17Ch	R/W	LED dot current setting for Dot L6-CSG1								80h
DC125	17Dh	R/W	LED dot current setting for Dot L6-CSB1								80h
pwm_bri0	200h	R/W	8-bits PWM for Dot L0-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSR0								00h
pwm_bri1	201h	R/W	8-bits PWM for Dot L0-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSR0								00h
pwm_bri2	202h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L0-CSG0								00h
pwm_bri3	203h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L0-CSG0								00h
pwm_bri4	204h	R/W	Reserved								00h
pwm_bri5	205h	R/W	Reserved								00h
pwm_bri6	206h	R/W	Reserved								00h
pwm_bri7	207h	R/W	Reserved								00h
pwm_bri8	208h	R/W	8-bits PWM for Dot L0-CSB0								00h
pwm_bri9	209h	R/W	8-bits PWM for Dot L0-CSR1								00h
pwm_bri10	20Ah	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri11	20Bh	R/W	Reserved								00h
pwm_bri12	20Ch	R/W	Reserved								00h
pwm_bri13	20Dh	R/W	Reserved								00h
pwm_bri14	20Eh	R/W	Reserved								00h
pwm_bri15	20Fh	R/W	Reserved								00h
pwm_bri16	210h	R/W	8-bits PWM for Dot L0-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSB0								00h
pwm_bri17	211h	R/W	8-bits PWM for Dot L0-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSB0								00h
pwm_bri18	212h	R/W	8-bits PWM for Dot L1-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSR1								00h
pwm_bri19	213h	R/W	8-bits PWM for Dot L1-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSR1								00h
pwm_bri20	214h	R/W	Reserved								00h
pwm_bri21	215h	R/W	Reserved								00h
pwm_bri22	216h	R/W	Reserved								00h
pwm_bri23	217h	R/W	Reserved								00h
pwm_bri24	218h	R/W	Reserved								00h
pwm_bri25	219h	R/W	Reserved								00h
pwm_bri26	21Ah	R/W	8-bits PWM for Dot L1-CSB0								00h
pwm_bri27	21Bh	R/W	8-bits PWM for Dot L1-CSR1								00h
pwm_bri28	21Ch	R/W	Reserved								00h
pwm_bri29	21Dh	R/W	Reserved								00h
pwm_bri30	21Eh	R/W	Reserved								00h
pwm_bri31	21Fh	R/W	Reserved								00h
pwm_bri32	220h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L0-CSG1								00h
pwm_bri33	221h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L0-CSG1								00h
pwm_bri34	222h	R/W	8-bits PWM for Dot L1-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CSB1								00h
pwm_bri35	223h	R/W	8-bits PWM for Dot L1-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CSB1								00h
pwm_bri36	224h	R/W	8-bits PWM for Dot L2-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSR0								00h
pwm_bri37	225h	R/W	8-bits PWM for Dot L2-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSR0								00h
pwm_bri38	226h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CSG0								00h
pwm_bri39	227h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CSG0								00h
pwm_bri40	228h	R/W	Reserved								00h
pwm_bri41	229h	R/W	Reserved								00h
pwm_bri42	22Ah	R/W	Reserved								00h
pwm_bri43	22Bh	R/W	Reserved								00h
pwm_bri44	22Ch	R/W	8-bits PWM for Dot L2-CSB0								00h
pwm_bri45	22Dh	R/W	8-bits PWM for Dot L2-CSR1								00h
pwm_bri46	22Eh	R/W	Reserved								00h
pwm_bri47	22Fh	R/W	Reserved								00h
pwm_bri48	230h	R/W	Reserved								00h
pwm_bri49	231h	R/W	Reserved								00h
pwm_bri50	232h	R/W	Reserved								00h
pwm_bri51	233h	R/W	Reserved								00h
pwm_bri52	234h	R/W	8-bits PWM for Dot L2-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSB0								00h
pwm_bri53	235h	R/W	8-bits PWM for Dot L2-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSB0								00h
pwm_bri54	236h	R/W	8-bits PWM for Dot L3-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSR1								00h
pwm_bri55	237h	R/W	8-bits PWM for Dot L3-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSR1								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri56	238h	R/W	Reserved								00h
pwm_bri57	239h	R/W	Reserved								00h
pwm_bri58	23Ah	R/W	Reserved								00h
pwm_bri59	23Bh	R/W	Reserved								00h
pwm_bri60	23Ch	R/W	Reserved								00h
pwm_bri61	23Dh	R/W	Reserved								00h
pwm_bri62	23Eh	R/W	8-bits PWM for Dot L3-CSB0								00h
pwm_bri63	23Fh	R/W	8-bits PWM for Dot L3-CSR1								00h
pwm_bri64	240h	R/W	Reserved								00h
pwm_bri65	241h	R/W	Reserved								00h
pwm_bri66	242h	R/W	Reserved								00h
pwm_bri67	243h	R/W	Reserved								00h
pwm_bri68	244h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CSG1								00h
pwm_bri69	245h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CSG1								00h
pwm_bri70	246h	R/W	8-bits PWM for Dot L3-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L1-CSB1								00h
pwm_bri71	247h	R/W	8-bits PWM for Dot L3-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L1-CSB1								00h
pwm_bri72	248h	R/W	8-bits PWM for Dot L4-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSR0								00h
pwm_bri73	249h	R/W	8-bits PWM for Dot L4-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSR0								00h
pwm_bri74	24Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L2-CSG0								00h
pwm_bri75	24Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L2-CSG0								00h
pwm_bri76	24Ch	R/W	Reserved								00h
pwm_bri77	24Dh	R/W	Reserved								00h
pwm_bri78	24Eh	R/W	Reserved								00h
pwm_bri79	24Fh	R/W	Reserved								00h
pwm_bri80	250h	R/W	8-bits PWM for Dot L4-CSB0								00h
pwm_bri81	251h	R/W	8-bits PWM for Dot L4-CSR1								00h
pwm_bri82	252h	R/W	Reserved								00h
pwm_bri83	253h	R/W	Reserved								00h
pwm_bri84	254h	R/W	Reserved								00h
pwm_bri85	255h	R/W	Reserved								00h
pwm_bri86	256h	R/W	Reserved								00h
pwm_bri87	257h	R/W	Reserved								00h
pwm_bri88	258h	R/W	8-bits PWM for Dot L4-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSB0								00h
pwm_bri89	259h	R/W	8-bits PWM for Dot L4-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSB0								00h
pwm_bri90	25Ah	R/W	8-bits PWM for Dot L5-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSR1								00h
pwm_bri91	25Bh	R/W	8-bits PWM for Dot L5-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSR1								00h
pwm_bri92	25Ch	R/W	Reserved								00h
pwm_bri93	25Dh	R/W	Reserved								00h
pwm_bri94	25Eh	R/W	Reserved								00h
pwm_bri95	25Fh	R/W	Reserved								00h
pwm_bri96	260h	R/W	Reserved								00h
pwm_bri97	261h	R/W	Reserved								00h
pwm_bri98	262h	R/W	8-bits PWM for Dot L5-CSB0								00h
pwm_bri99	263h	R/W	8-bits PWM for Dot L5-CSR1								00h
pwm_bri100	264h	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri101	265h	R/W	Reserved								00h
pwm_bri102	266h	R/W	Reserved								00h
pwm_bri103	267h	R/W	Reserved								00h
pwm_bri104	268h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L2-CSG1								00h
pwm_bri105	269h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L2-CSG1								00h
pwm_bri106	26Ah	R/W	8-bits PWM for Dot L5-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L2-CSB1								00h
pwm_bri107	26Bh	R/W	8-bits PWM for Dot L5-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L2-CSB1								00h
pwm_bri108	26Ch	R/W	8-bits PWM for Dot L6-CSR0 OR 16-bits PWM lower 8 bits [7:0] for Dot L3-CSR0								00h
pwm_bri109	26Dh	R/W	8-bits PWM for Dot L6-CSG0 OR 16-bits PWM higher 8 bits [15:8] for Dot L3-CSR0								00h
pwm_bri110	26Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSG0								00h
pwm_bri111	26Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSG0								00h
pwm_bri112	270h	R/W	Reserved								00h
pwm_bri113	271h	R/W	Reserved								00h
pwm_bri114	272h	R/W	Reserved								00h
pwm_bri115	273h	R/W	Reserved								00h
pwm_bri116	274h	R/W	8-bits PWM for Dot L6-CSB0								00h
pwm_bri117	275h	R/W	8-bits PWM for Dot L6-CSR1								00h
pwm_bri118	276h	R/W	Reserved								00h
pwm_bri119	277h	R/W	Reserved								00h
pwm_bri120	278h	R/W	Reserved								00h
pwm_bri121	279h	R/W	Reserved								00h
pwm_bri122	27Ah	R/W	Reserved								00h
pwm_bri123	27Bh	R/W	Reserved								00h
pwm_bri124	27Ch	R/W	8-bits PWM for Dot L6-CSG1 OR 16-bits PWM lower 8 bits [7:0] for Dot L3-CSB0								00h
pwm_bri125	27Dh	R/W	8-bits PWM for Dot L6-CSB1 OR 16-bits PWM higher 8 bits [15:8] for Dot L3-CSB0								00h
pwm_bri126	27Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSR1								00h
pwm_bri127	27Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSR1								00h
pwm_bri128	280h	R/W	Reserved								00h
pwm_bri129	281h	R/W	Reserved								00h
pwm_bri130	282h	R/W	Reserved								00h
pwm_bri131	283h	R/W	Reserved								00h
pwm_bri132	284h	R/W	Reserved								00h
pwm_bri133	285h	R/W	Reserved								00h
pwm_bri134	286h	R/W	8-bits PWM for Dot L7-CSB0								00h
pwm_bri135	287h	R/W	8-bits PWM for Dot L7-CSR1								00h
pwm_bri136	288h	R/W	Reserved								00h
pwm_bri137	289h	R/W	Reserved								00h
pwm_bri138	28Ah	R/W	Reserved								00h
pwm_bri139	28Bh	R/W	Reserved								00h
pwm_bri140	28Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSG1								00h
pwm_bri141	28Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSG1								00h
pwm_bri142	28Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L3-CSB1								00h
pwm_bri143	28Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L3-CSB1								00h
pwm_bri144	290h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSR0								00h
pwm_bri145	291h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSR0								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri146	292h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSG0								00h
pwm_bri147	293h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSG0								00h
pwm_bri148	294h	R/W	Reserved								00h
pwm_bri149	295h	R/W	Reserved								00h
pwm_bri150	296h	R/W	Reserved								00h
pwm_bri151	297h	R/W	Reserved								00h
pwm_bri152	298h	R/W	Reserved								00h
pwm_bri153	299h	R/W	Reserved								00h
pwm_bri154	29Ah	R/W	Reserved								00h
pwm_bri155	29Bh	R/W	Reserved								00h
pwm_bri156	29Ch	R/W	Reserved								00h
pwm_bri157	29Dh	R/W	Reserved								00h
pwm_bri158	29Eh	R/W	Reserved								00h
pwm_bri159	29Fh	R/W	Reserved								00h
pwm_bri160	2A0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSB0								00h
pwm_bri161	2A1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSB0								00h
pwm_bri162	2A2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSR1								00h
pwm_bri163	2A3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSR1								00h
pwm_bri164	2A4h	R/W	Reserved								00h
pwm_bri165	2A5h	R/W	Reserved								00h
pwm_bri166	2A6h	R/W	Reserved								00h
pwm_bri167	2A7h	R/W	Reserved								00h
pwm_bri168	2A8h	R/W	Reserved								00h
pwm_bri169	2A9h	R/W	Reserved								00h
pwm_bri170	2AAh	R/W	Reserved								00h
pwm_bri171	2ABh	R/W	Reserved								00h
pwm_bri172	2ACh	R/W	Reserved								00h
pwm_bri173	2ADh	R/W	Reserved								00h
pwm_bri174	2AEh	R/W	Reserved								00h
pwm_bri175	2AFh	R/W	Reserved								00h
pwm_bri176	2B0h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSG1								00h
pwm_bri177	2B1h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSG1								00h
pwm_bri178	2B2h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L4-CSB1								00h
pwm_bri179	2B3h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L4-CSB1								00h
pwm_bri180	2B4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSR0								00h
pwm_bri181	2B5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSR0								00h
pwm_bri182	2B6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSG0								00h
pwm_bri183	2B7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSG0								00h
pwm_bri184	2B8h	R/W	Reserved								00h
pwm_bri185	2B9h	R/W	Reserved								00h
pwm_bri186	2BAh	R/W	Reserved								00h
pwm_bri187	2BBh	R/W	Reserved								00h
pwm_bri188	2BCh	R/W	Reserved								00h
pwm_bri189	2BDh	R/W	Reserved								00h
pwm_bri190	2BEh	R/W	Reserved								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri191	2BFh	R/W	Reserved								00h
pwm_bri192	2C0h	R/W	Reserved								00h
pwm_bri193	2C1h	R/W	Reserved								00h
pwm_bri194	2C2h	R/W	Reserved								00h
pwm_bri195	2C3h	R/W	Reserved								00h
pwm_bri196	2C4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSB0								00h
pwm_bri197	2C5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSB0								00h
pwm_bri198	2C6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSR1								00h
pwm_bri199	2C7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSR1								00h
pwm_bri200	2C8h	R/W	Reserved								00h
pwm_bri201	2C9h	R/W	Reserved								00h
pwm_bri202	2CAh	R/W	Reserved								00h
pwm_bri203	2CBh	R/W	Reserved								00h
pwm_bri204	2CCh	R/W	Reserved								00h
pwm_bri205	2CDh	R/W	Reserved								00h
pwm_bri206	2CEh	R/W	Reserved								00h
pwm_bri207	2CFh	R/W	Reserved								00h
pwm_bri208	2D0h	R/W	Reserved								00h
pwm_bri209	2D1h	R/W	Reserved								00h
pwm_bri210	2D2h	R/W	Reserved								00h
pwm_bri211	2D3h	R/W	Reserved								00h
pwm_bri212	2D4h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSG1								00h
pwm_bri213	2D5h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSG1								00h
pwm_bri214	2D6h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L5-CSB1								00h
pwm_bri215	2D7h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L5-CSB1								00h
pwm_bri216	2D8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSR0								00h
pwm_bri217	2D9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSR0								00h
pwm_bri218	2DAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSG0								00h
pwm_bri219	2DBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSG0								00h
pwm_bri220	2DCh	R/W	Reserved								00h
pwm_bri221	2DDh	R/W	Reserved								00h
pwm_bri222	2DEh	R/W	Reserved								00h
pwm_bri223	2DFh	R/W	Reserved								00h
pwm_bri224	2E0h	R/W	Reserved								00h
pwm_bri225	2E1h	R/W	Reserved								00h
pwm_bri226	2E2h	R/W	Reserved								00h
pwm_bri227	2E3h	R/W	Reserved								00h
pwm_bri228	2E4h	R/W	Reserved								00h
pwm_bri229	2E5h	R/W	Reserved								00h
pwm_bri230	2E6h	R/W	Reserved								00h
pwm_bri231	2E7h	R/W	Reserved								00h
pwm_bri232	2E8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSB0								00h
pwm_bri233	2E9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSB0								00h
pwm_bri234	2EAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSR1								00h
pwm_bri235	2EBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSR1								00h

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
pwm_bri236	2ECh	R/W	Reserved								00h
pwm_bri237	2EDh	R/W	Reserved								00h
pwm_bri238	2EEh	R/W	Reserved								00h
pwm_bri239	2EFh	R/W	Reserved								00h
pwm_bri240	2F0h	R/W	Reserved								00h
pwm_bri241	2F1h	R/W	Reserved								00h
pwm_bri242	2F2h	R/W	Reserved								00h
pwm_bri243	2F3h	R/W	Reserved								00h
pwm_bri244	2F4h	R/W	Reserved								00h
pwm_bri245	2F5h	R/W	Reserved								00h
pwm_bri246	2F6h	R/W	Reserved								00h
pwm_bri247	2F7h	R/W	Reserved								00h
pwm_bri248	2F8h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSG1								00h
pwm_bri249	2F9h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSG1								00h
pwm_bri250	2FAh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L6-CSB1								00h
pwm_bri251	2FBh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L6-CSB1								00h

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LP5867 integrates 6 constant current sinks with 7 switching FETs and one LP5867 can drive up to 42 LED dots or 14 RGB pixels and achieve great dimming effect. In smart home, gaming keyboards, and other human-machine interaction applications, the device can greatly improve user experience with small amount of components.

9.2 Typical Application

9.2.1 Application

図 9-1 shows an example of typical application, which uses one LP5867 to drive 14 common-anode RGB LEDs through I^2C communication.

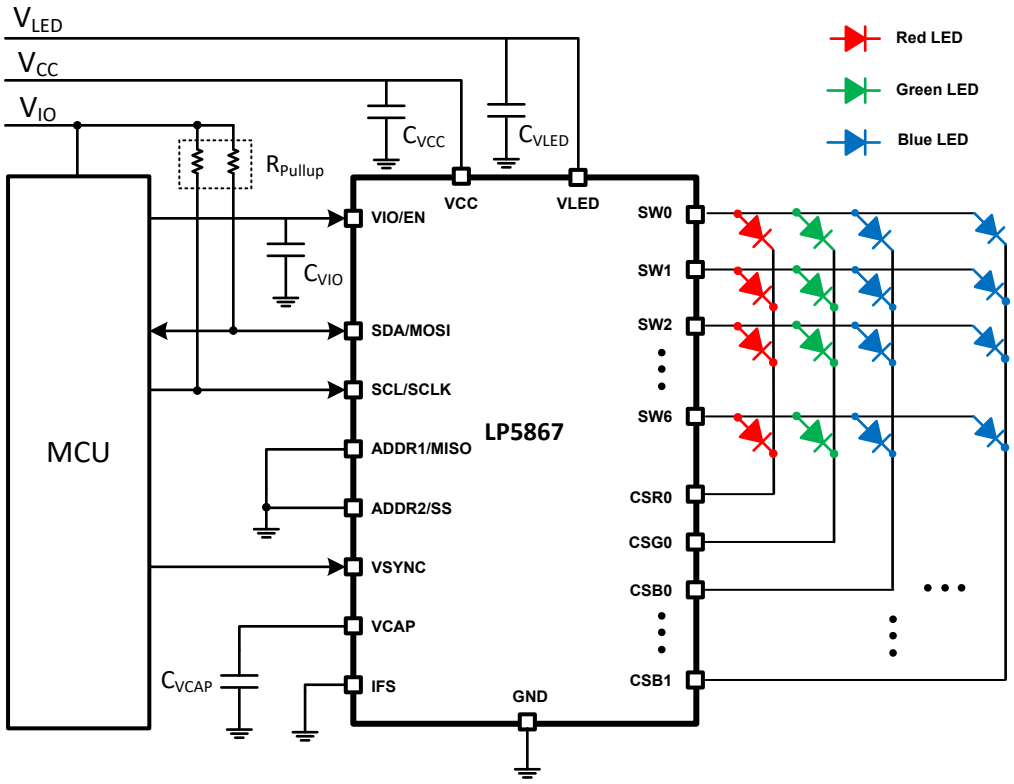


図 9-1. Typical Application - LP5867 Driving RGB LEDs (42 LED Dots)

9.2.2 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
VCC / VIO	3.3V
VLED	5V
RGB LED count	14
Scan number	7
Interface	I^2C
LED maximum average current (red, green, blue)	4mA, 3mA, 2mA
LED maximum peak current (red, green, blue)	44mA, 33mA, 22mA

9.2.3 Detailed Design Procedure

LP5867 requires an external capacitor C_{VCAP}, whose value is 1μF connected from V_{CAP} to GND for proper operation of internal LDO. The device must be placed as close to the device as possible.

TI recommends that 1-μF capacitors be placed between VCC / VLED with GND, and a 1nF capacitor placed between VIO with GND. Place the capacitors as close to the device as possible.

Pull-up resistors $R_{pull-up}$ are requirement for SCL and SDA when using I^2C as communication method. In typical applications, TI recommends 1.8kΩ to 4.7kΩ resistors.

To decrease thermal dissipation from device to ambient, resistors R_{CS} can optionally be placed in serial with the LED. Voltage drop on these resistors must left enough margins for VSAT to ensure the device works normally.

9.2.3.1 Program Procedure

When selecting data refresh Mode 1, outputs are refreshed instantly after data is received.

When selecting data refresh Mode 2/3, VSYNC signal is required for synchronized display. Programming flow is showed as 図 9-2. To display full pixel of last frame, VSYNC pulse must be sent to the device after the end of last PWM. Time between two pulses t_{SYNC} must be larger than the whole PWM time of all Dots t_{frame}. Common selection like 60Hz, 90Hz, 120Hz or even higher refresh frequency can be supported. High pulse width longer than t_{SYNC_H} is required at the beginning of each VSYNC frame, and data must not be write to PWM registers during high pulse width.

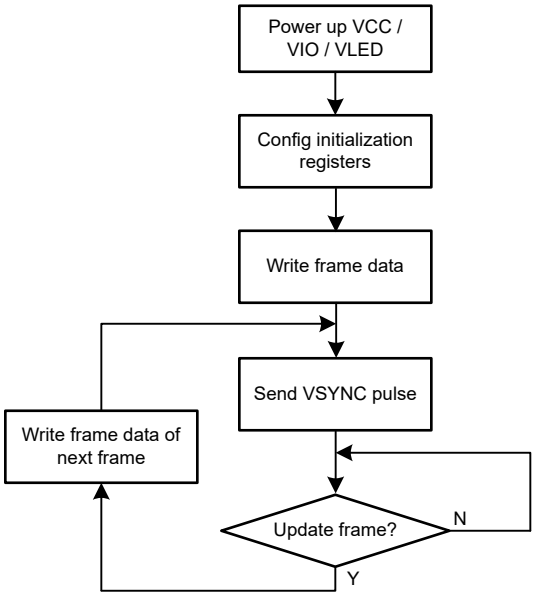


図 9-2. Program Procedure

9.2.4 Application Performance Plots

The following figures show the application performance plots.

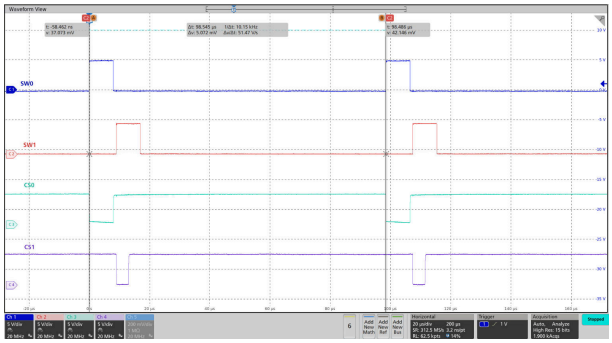
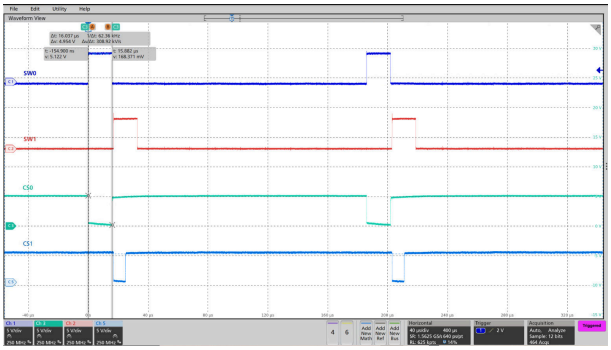
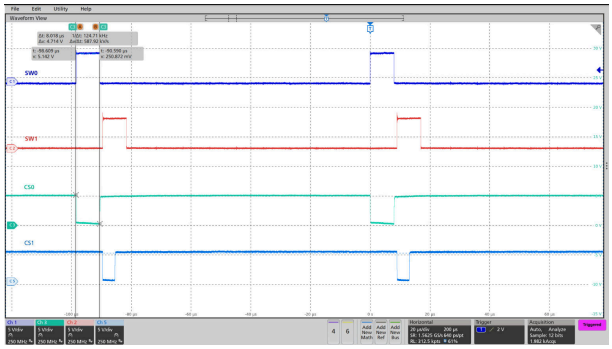


図 9-3. Scan Lines and Current Sinks Waveforms of SW0, SW1, CSR0(CS0), CSG0(CS1)



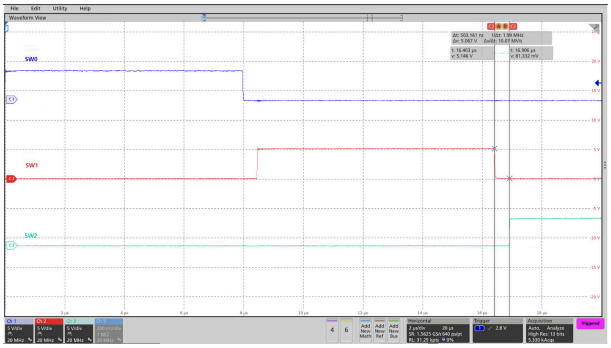
PWM frequency = 62.5kHz

図 9-4. Scan Lines and Current Sinks Waveforms of SW0, SW1, CSR0(CS0), CSG0(CS1)



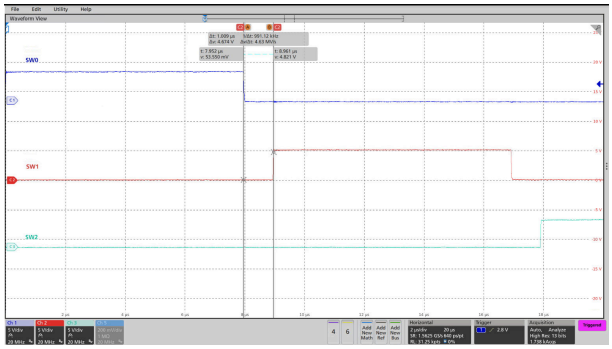
PWM frequency = 125kHz

図 9-5. Scan Lines and Current Sinks Waveforms of SW0, SW1, CSR0(CS0), CSG0(CS1)



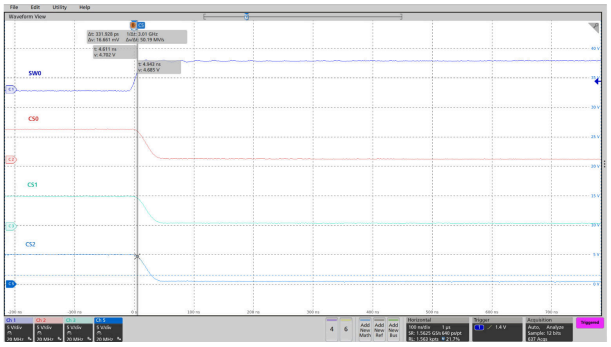
Switch blank time t_{SW_BLK} = 0.5µs

図 9-6. Scan Lines Switching Waveforms of SW0, SW1, SW2



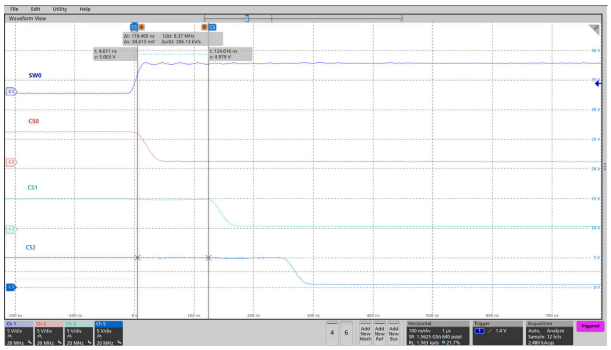
Switch blank time t_{SW_BLK} = 1µs

図 9-7. Scan Lines Switching Waveforms of SW0, SW1, SW2



PWM_Phase_Shift = 0h

図 9-8. PWM Phase Shift Disabled



PWM_Phase_Shift = 1h

図 9-9. PWM Phase Shift Enabled

9.3 Power Supply Recommendations

9.3.1 VDD Input Supply Recommendations

LP5867 is designed to operate from a 2.7V to 5.5V VDD voltage supply. This input supply must be well regulated and be able to provide the peak current required by the LED matrix. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LP5867 VDD supply voltage to drop below the maximum POR voltage.

9.3.2 VLED Input Supply Recommendations

LP5867 is designed to operate with a 2.7V to 5.5V VLED voltage supply. The VLED supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop, under load transients like start-up or rapid brightness change. The resistance of the input supply rail must be low enough so that the input current transient does not cause the VLED supply voltage to drop below LED V_f + VSAT voltage.

9.3.3 VIO Input Supply Recommendations

LP5867 is designed to operate with a 1.65V to 5.5V VIO_EN voltage supply. The VIO_EN supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients like startup or rapid brightness change.

9.4 Layout

9.4.1 Layout Guidelines

Below guidelines for layout design can help to get a better on-board performance.

- The decoupling capacitors C_{VCC} and C_{VLED} for power supply must be close to the chip to have minimized the impact of high-frequency noise and ripple from power. C_{VCAP} for internal LDO must be put as close to chip as possible. GND plane connections to C_{VLED} and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane. C_{VIO} for internal enable block also must be put as close to chip as possible.
- The exposed thermal pad must be well soldered to the board, which can have better mechanical reliability. This action can optimize heat transfer so that increasing thermal performance. The AGND pin must be connected to thermal pad and system ground.
- The major heat flow path from the package to the ambient is through copper on the PCB. Several methods can help thermal performance. Below exposed thermal pad of the device, putting much vias through the PCB to other ground layer can dissipate more heat. Maximizing the copper coverage on the PCB can increase the thermal conductivity of the board.
- Low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of VLED – SWx must be short and wide and avoid parallel wiring and narrow trace. Transient current in SWx pins is much larger than CSy pins, so that trace for SWx must be wider than CSy.

9.4.2 Layout Example

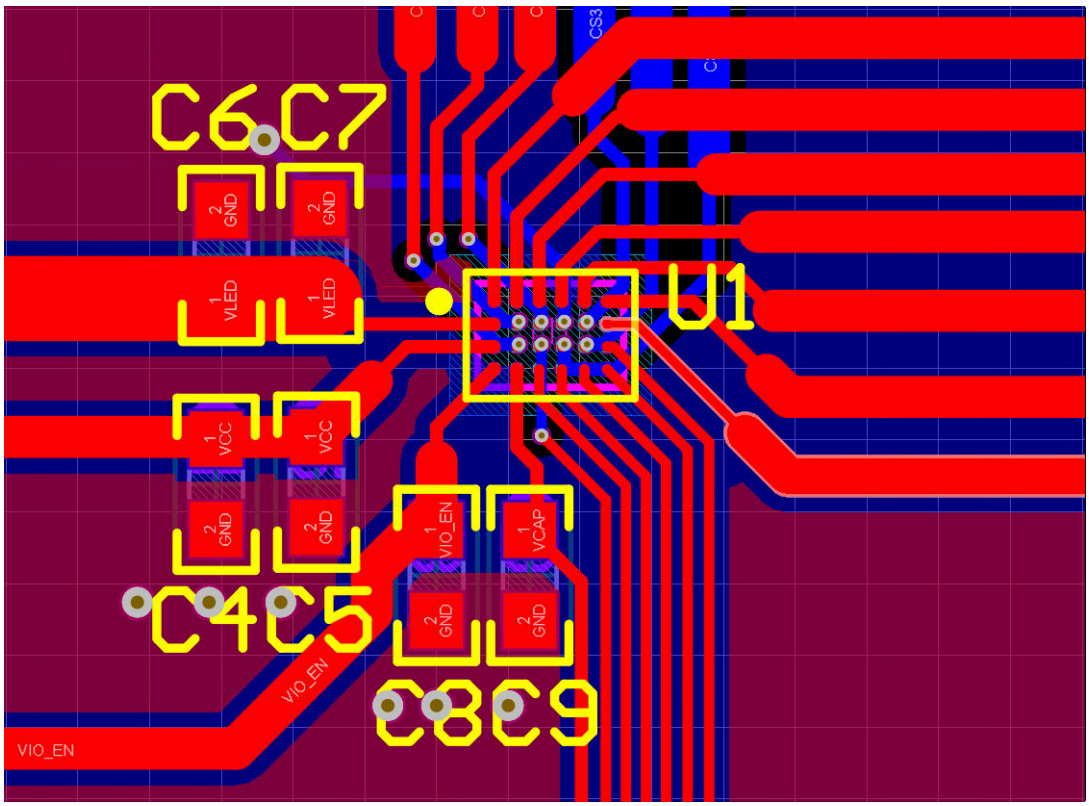


図 9-10. LP5867 Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

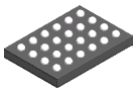
11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2024) to Revision A (April 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

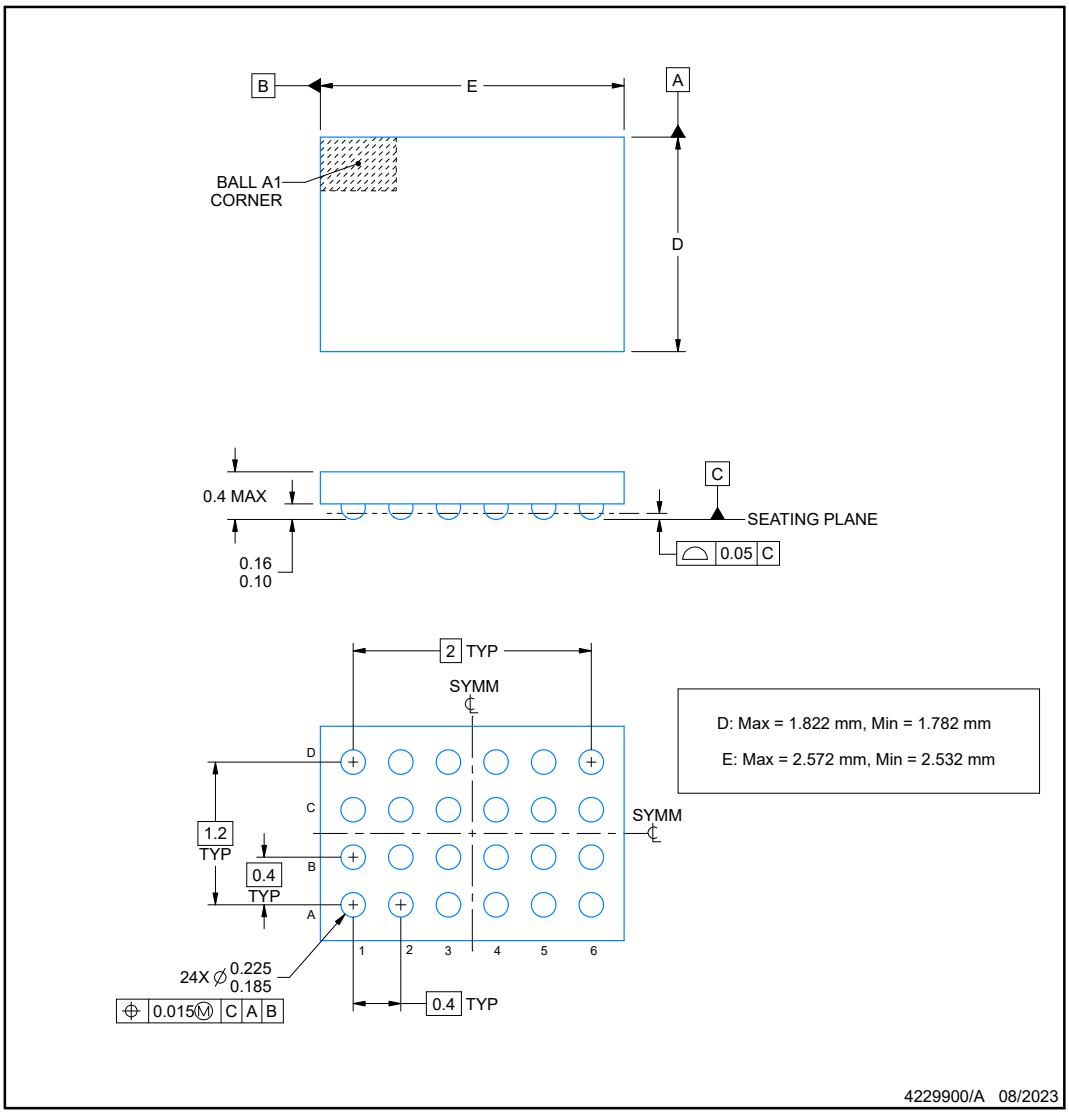


PACKAGE OUTLINE

YBH0024-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

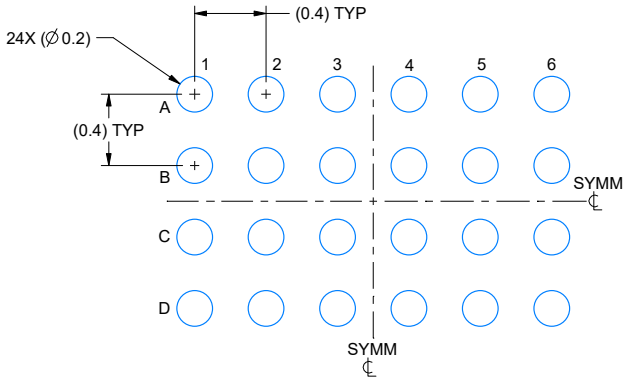
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

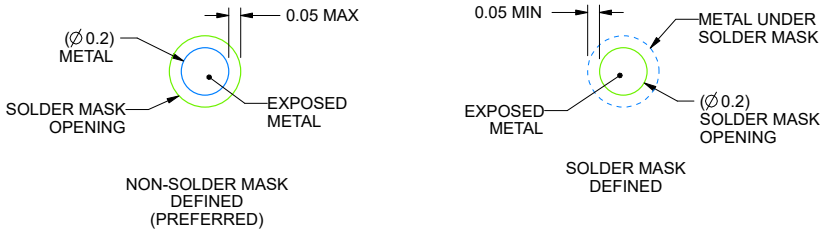
YBH0024-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4229900/A 08/2023

NOTES: (continued)

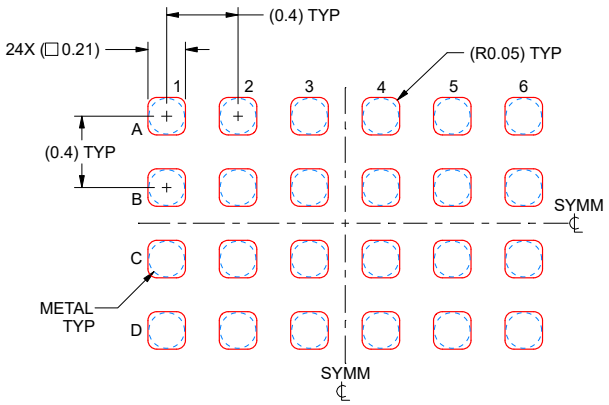
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0024-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4229900/A 08/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5867YBHR	ACTIVE	DSBGA	YBH	24	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LP5867	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265