TPS92201 1.5A 高効率同期整流降圧 LED ドライバ

1 特長

- 入力電圧範囲:2.5V～5.5V
- 定出力電流:1.5A
- 最大 95% の効率
- 0.1μA シャットダウン電流
- 220mΩ (HS) / 170mΩ (LS) MOSFET
- 最大 100% のスイッチング デューティ サイクル
- 1.5MHz のスイッチング周波数
- PWM モードを強制して低出力リップルを実現 (TPS92201)
- パワー セーブ モードでは軽負荷でも高効率を維持 (TPS92201A)
- 出力電圧範囲:0.6V～VIN
- 100mV フィードバック レギュレーション電圧
- 1%～100% の高精度アナログ調光
- PWM 入力周波数:20kHz～200kHz
- ソフト スタートアップを内蔵
- 過電流、LED の開放と短絡、FB 抵抗の開放と短絡に対する包括的な保護機能
- サーマル シャットダウン保護機能
- WSON および SOT563 パッケージ オプション

2 アプリケーション

- 試験および測定機器
- パワー デリバリー
- ビル オートメーション
  - スマート ホーム カメラ
  - ビデオ ドアベル
  - IP カメラ
  - スマート ドアロック
  - フラッシュライト

3 概要

TPS92201 は、2.5V～5.5V の入力範囲に対応する高効率の 1.5A 同期整流降圧型 LED ドライバです。ハイサイドとローサイドの MOSFET を内蔵しているため、高効率で小型のソリューションを実現できます。シャットダウン電流が 1μA と非常に低いため、バッテリ駆動アプリケーションの消費電力削減に役立ちます。

TPS92201 には、ピーク電流制御方式による適応型オフ時間が採用されています。出力リップルを最小限に抑えるため、このデバイスは電流範囲の全体にわたって、標準 1.5MHz のパルス幅変調 (PWM) モードで動作します。

TPS92201A には、ピーク電流制御方式による適応型オフ時間が採用されています。中負荷から高負荷では、デバイスはパルス幅変調 (PWM) モードで、1.5MHz のスイッチング周波数で動作します。軽負荷時には、デバイスは自動的にパルス幅変調 (PFM) へ移行し、負荷電流範囲の全体にわたって高効率を維持します。

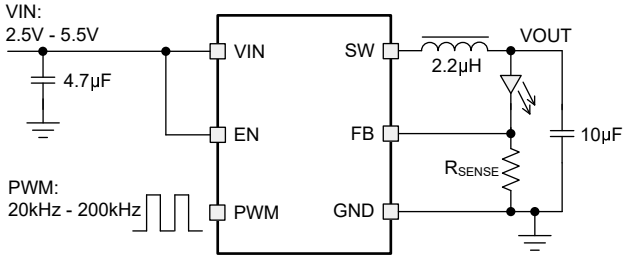
内蔵スイッチには、最大 1.5A の定電流を供給する能力があります。アナログ調光は、PWM 入力のデューティ サイクルを 1%～100% の範囲で調整することで実現されます。可聴ノイズを回避するため、20kHz～200kHz の入力 PWM 周波数に対応できます。

安全と保護のために、TPS92201 デバイスには、LED 開放、LED 短絡、FB 抵抗開放、FB 抵抗短絡とサーマル シャットダウンなど、完全な保護機能が実装されています。

製品情報 (1)

発注用製品型番	パッケージ	本体サイズ (公称)
TPS92201DRV	WSON (6)	2mm × 2mm (2)
TPS92201ADRV	WSON (6)	
TPS92201DRL	SOT563 (6)	1.6 mm × 1.6 mm
TPS92201ADRL	SOT563 (6)	

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Device Comparison Table

PART NUMBER	MATERIAL	POWER SAVE MODE	PACKAGE
TPS92200	TPS92201DRVR	No	WSON-6
	TPS92201MDRVR(1)		
	TPS92201DRLR		SOT563-6
	TPS92201MDRLR(1)		
TPS92201A	TPS92201ADRVR	Yes	WSON-6
	TPS92201AMDRVR(1)		
	TPS92201ADRLR		SOT563-6
	TPS92201AMDRLR(1)		

(1) Extended Temperature devices, supporting –55°C to approximately 125°C operating ambient temperature.

5 Pin Configuration and Functions

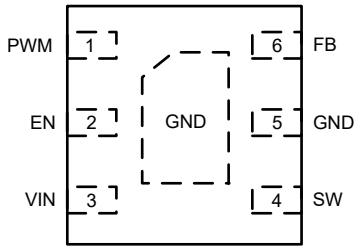


図 5-1. DRV Package 6-Pin WSON Top View

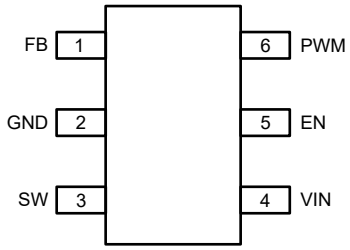


図 5-2. DRL Package 6-Pin SOT563 Top View

PIN NUMBER			I/O/PWR	DESCRIPTION
NAME	DRV	DRL		
PWM	1	6	I	PWM input. LED output current is adjusted according to the PWM input duty cycle.
EN	2	5	I	Device enable input. Logic high enables the device, logic low disables the device and turns the device into shutdown. Do not leave floating.
VIN	3	4	PWR	Power supply input.
SW	4	3	PWR	Switch pin. Connecting the internal FET switches and inductor terminal.
GND	5	2	PWR	Power ground.
FB	6	1	I	Feedback pin for the internal control loop. Connect this pin to an external resistor to set output current.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, EN, PWM	–0.3	6	V
	SW (DC)	–0.3	VIN + 0.3	V
	SW (AC, 10ns transient)	–3	9	V
	FB	–0.3	5.5	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input stage	V_{IN}	2.5	5.5	V
	V_{EN}	–0.1	6	V
	V_{PWM}	–0.1	6	V
Output stage	V_{OUT}		V_{IN}	V
	I_{OUT}		1.5	A
Peripheral component	Effective inductance	2.2	4.7	µH
	Effective capacitance			µF
Temperature	Operating Ambient temperature, T_A	-40	85	°C
	Operating Junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS92201, TPS92201A		UNIT
		DRL (SOT563)	DRV (WSON-6)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152	82.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.1	106.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.3	45.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	7.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	45.7	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 2.5V to 5.5V, T_A = –40°C to +85°C(T_A = –55°C to +125°C for TPS92201MDRVR and TPS92201AMDRVR and for the TPS92201MDRLR and TPS92201AMDRLR); Typical values are at T_A = 25°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
V_{IN_UVLO}	V_{IN} undervoltage lockout	Fallng V_{IN}	2.1	2.2		V
		Rising V_{IN}		2.3	2.4	V
	Hysteresis			0.1		V
I_{SD}	Shutdown current into V_{IN}	V_{IN} = 3.6V, V_{EN} = 0		0.1	0.5	µA
I_{SD_ET}	Shutdown current into V_{IN}	V_{IN} = 3.6V, V_{EN} = 0 (TPS92201MDRVR,TPS92201AMDRVR, TPS92201MDRLR and TPS92201AMDRLR)		0.1	1.75	µA
I_Q	Quiescent current into V_{IN}	V_{IN} = 3.6V, V_{EN} = 2V, V_{FB}=0V, Not switching (TPS92201)	450	520	600	µA
		V_{IN} = 3.6V, V_{EN} = 2V, V_{FB} = 0V, Not switching (TPS92201A)	520	630	720	µA
LOGIC INTERFACE						
V_{EN_H}	High-level threshold voltage of EN				1.2	V
V_{EN_L}	Low-level threshold voltage of EN		0.4			V
V_{IH_PWM}	High-level threshold voltage of PWM				1	V
V_{IL_PWM}	Low-level threshold voltage of PWM		0.7			V
t_{EN_ON}	EN minimum on time to enable device					µS
t_{EN_OFF}	EN minimum off time to disable device					µS
t_{PWM_ON}	PWM minimum on time when dimming the output current				5	µS
f_{PWM}	PWM input frequency		20		200	kHz
D_{PWM}	PWM input duty cycle		1		100	%
I_{LKG}	Leakage current of EN pin	V_{IN} = 5.5V, V_{EN} = 5.5V, V_{PWM} = 5.5V,			1	µA
I_{LKG}	Leakage current of PWM pin	V_{IN} = 5.5V, V_{EN} = 5.5V, V_{PWM} = 5.5V,			0.5	µA
OUTPUT STAGE						
V_{FB_REF}	FB pin regulation voltage at maximum duty cycle	PWM = 100%, I_{OUT} = 500mA	92	100	104	mV
	FB pin regulation voltage at 50% duty cycle	PWM = 50%, I_{OUT} = 0mA(TM), F_{PWM}=20KHz	-8%	50	+8%	mV
	FB pin regulation voltage at 50% duty cycle	PWM = 50%, I_{OUT} = 0mA(TM), F_{PWM}=200KHz	-10%	50	+10%	mV
	FB pin regulation voltage at 5% duty cycle	PWM = 5%, I_{OUT} = 500mA		5		mV
	FB pin regulation voltage at 1% duty cycle	PWM = 1%, I_{OUT} = 500mA		1		mV
R_{HS}	High-side FET on resistance			220	330	mΩ
R_{LS}	Low-side FET on resistance			170	300	mΩ
f_{SW}	Switching frequency			1.5		MHz
D_{max}	Maximum switching duty cycle			100		%
I_{LIM_HS}	High-side current limit		1.9	2.16		A

6.6 Typical Characteristics

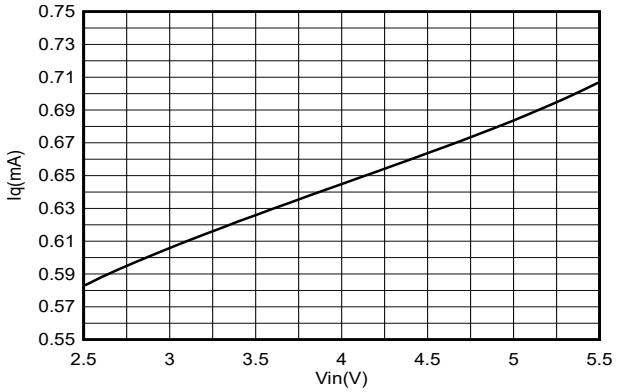


図 6-1. Quiescent Current vs Input Voltage

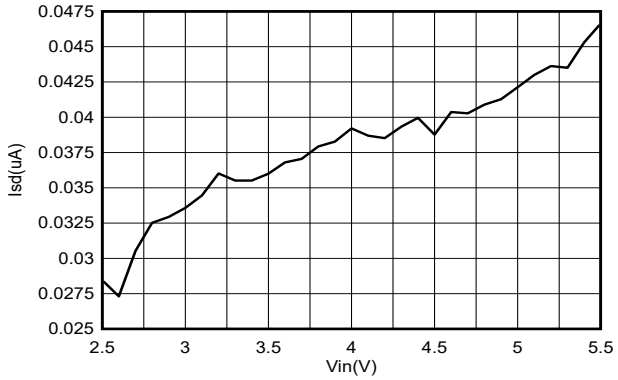


図 6-2. Shutdown Current vs Input Voltage

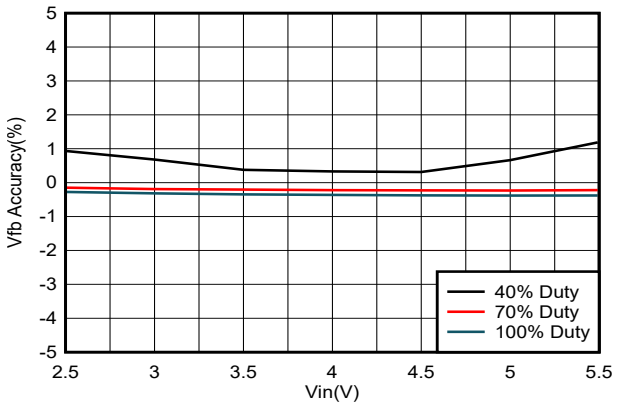


図 6-3. FB Voltage Accuracy

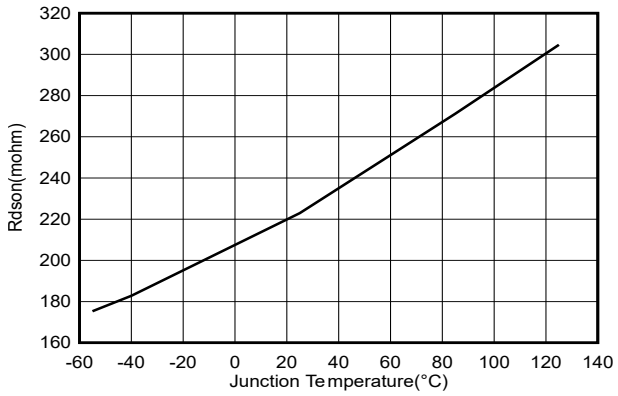


図 6-4. High-Side FET On Resistance vs Junction Temperature

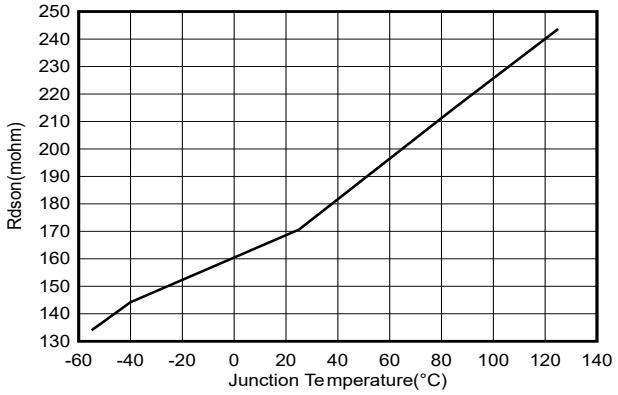


図 6-5. Low-Side FET On Resistance vs Junction Temperature

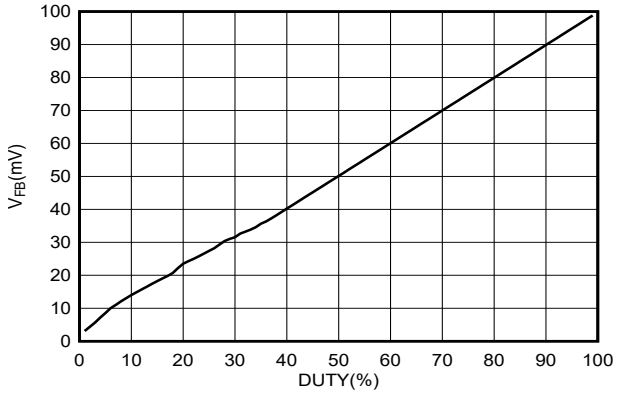


図 6-6. PWM duty cycle vs FB voltage

7 Detailed Description

7.1 Overview

The TPS92201 is a high-efficiency 1.5A synchronous buck-type LED driver with 2.5V to 5.5V input range. The device operates at typically 1.5MHz pulse width modulation (PWM) mode in full current range. In additional, TPS92201A can support Power Save Mode, the device operates in pulse width modulation (PWM) mode with 1.5MHz switching frequency at heavy load, similar as TPS92201. But at light load, the device automatically enters pulse frequency modulation (PFM) to maintain high efficiency over the entire load current range. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

The integrated switches for both deivces have the capability to deliever up to 1.5A constant current and no need for external Schottky diode. Analog dimming is achieved by adjusting the duty cycle of the PWM in 1% to 100% range. Full protection methods are implemented including LED open, LED short, FB resistor open, FB resistor short and thermal shutdown.

7.2 Functional Block Diagram

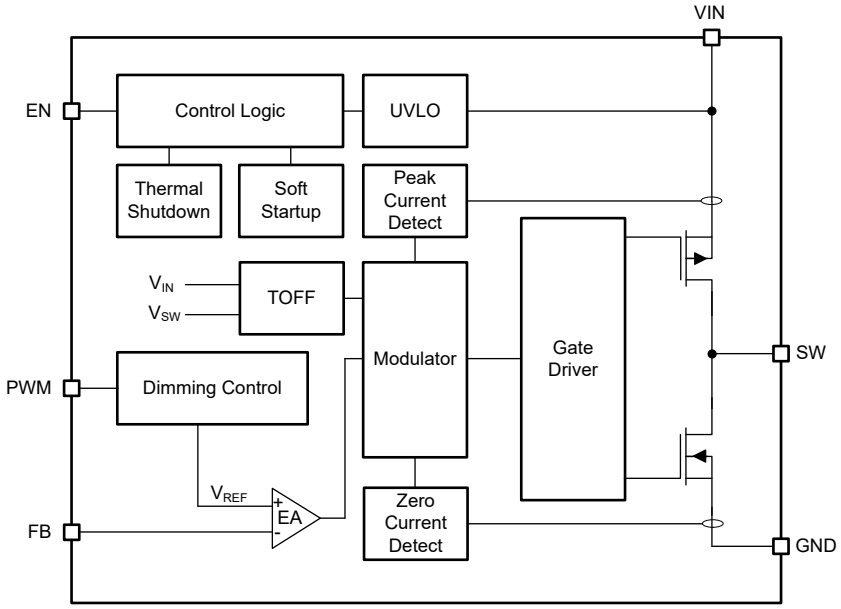


図 7-1. TPS92201 Functional Block Diagram

7.3 Feature Description

7.3.1 Adaptive Off-time Control

Adaptive off-time with peak current control scheme is used in the device. The device operates at typically 1.5MHz pulse width modulation (PWM) mode in full current range. At medium to heavy load, the device operates in pulse width modulation (PWM) mode with 1.5MHz switching frequency. At light load, the device automatically enters pulse frequency modulation (PFM) to maintain high efficiency over the entire load current range. Based on the VIN/VOUT ratio, a simple circuit sets the required off time for the low-side MOSFET. The switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.3.2 Power Save Mode

TPS92201A automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

7.3.3 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. Output current rises smoothly and excessive inrush current is avoided. In battery-power system, the soft startup prevents extra voltage drop on primary power supply with high internal impedance. The internal soft startup period is xx ms typically.

7.3.4 Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% switching duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN\_MIN} = V_{FB} + V_{F\_IOUT} + I_{OUT} \times (R_{DS\_ON} + R_L) \quad (1)$$

where

- V_{FB} is the feedback reference voltage, which is typically 100mV
- V_{F_IOUT} is the LED forward voltage at output current
- I_{OUT} is the output current setting
- R_{DS_ON} is the high-side FET resistance when turning on
- R_L is the inductor ohmic resistance DCR

7.3.5 LED Current Setting

The LED current is set by the external resistor between the FB pin and GND, calculated as:

$$I_{LED} = \frac{V_{FB}}{R_{SENSE}} \quad (2)$$

where

- V_{FB} is the feedback reference voltage, which is typically 100mV
- R_{SENSE} is the resistance between FB and GND

7.3.6 Voltage Reference

The feedback reference produces a precise ±5% voltage reference over whole temperature range when the PWM duty cycle is 100%, which is typically 100mV. In analog dimming mode, the feedback voltage is proportional to the duty cycle of PWM imput as shown in 図 7-2.

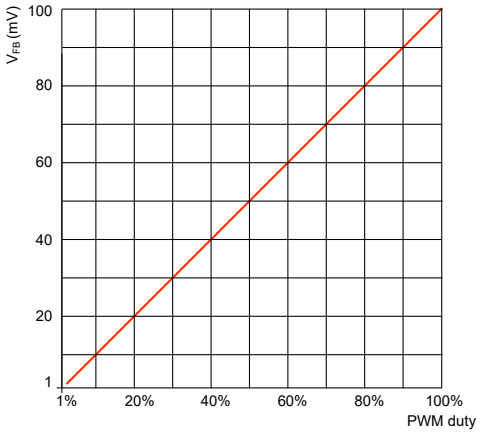


図 7-2. FB voltage with PWM duty cycle

7.3.7 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from battery or input voltage supply. Excessive current might occur with a heavy load or shorted output circuit condition. The device adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to discharge the inductor current with an adaptive off-time.

7.3.8 Fault Behaviors

The TPS92201 is protected by high-side current limitation in different fault conditions, such as LED open and short, sense resistor open and short. No matter the fault happens before startup or during operation, the device can stay safety.

表 7-1. Fault protection conditions

Fault	Condition	Behavior
LED open	V_{FB} is driven close to 0	VOUT keeps increasing to VIN. and The high-side switch keeps turn on.
LED anode short to cathode	V_{FB} is driven to VOUT quickly, then	VFB is driven to VOUT quickly, the device keeps switching by minimum on-time.
LED anode short to GND	V_{FB} is driven close to 0	high-side switch current limit triggered
FB resistor open	V_{FB} is driven to VOUT - Vf	The device keeps switching by the minimum on-time
FB short to GND	V_{FB} is driven close to 0	VFB is driven close to 0. Current limit is triggered.

7.3.9 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

7.3.10 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output current to the set value. The EN input must be terminated and should not be floating.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS92201 device is typically used as buck-type LED driver to drive IR or white LEDs from a 2.5V to 5.5V input.

8.2 Typical Application

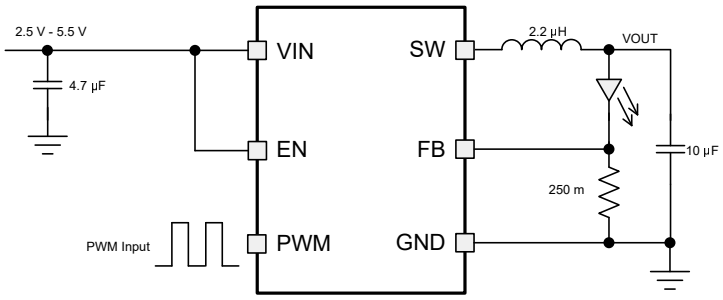


図 8-1. TPS92201 400mA Output Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5V to 5.5V
Output voltage	1.9V (1.8V Vf + 0.1V VFB)
Maximum output current	400mA

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	10µF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A106KE51L	Murata
L1	2.2µH, Power Inductor, SDER041H-2R2MS	Cyntec
R1,R2,R3	Chip resistor, 1%, size 0603	Std.
C3	Optional, 6.8pF if it is needed	Std.

(1) See *Third-party Products Disclaimer*

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS92201 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response. 6.8pF capacitance is recommended for R2 of 100kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

8.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 8-3. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)				
		4.7	10	22	2x 22	100
0.6 ≤ V_{OUT} < 1.2	1				+	
	2.2				++(3)	
1.2 ≤ V_{OUT} < 1.8	1			+	+	
	2.2			++(3)	+	
1.8 ≤ V_{OUT}	1		+	+	+	
	2.2		++(3)	+	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitor tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.4 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 4 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (4)$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

8.2.2.5 Input and Output Capacitor Selection

The architecture of the TPS92201 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The TPS92201 is designed to operate with an output capacitor of 10µF to 47µF, as outlined in 表 8-3.

8.2.3 Application Performance Curves

V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

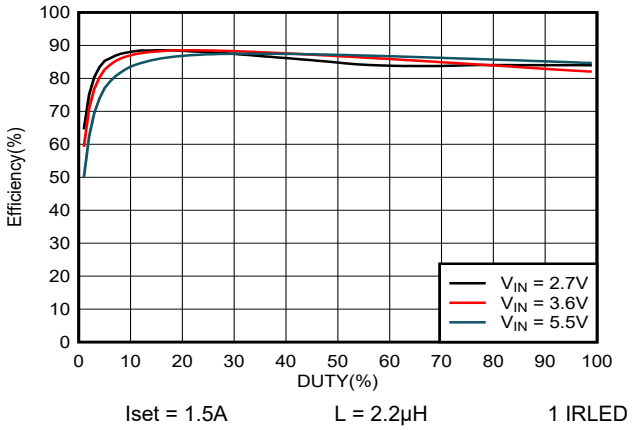


図 8-2. 1 IRLED Output Efficiency

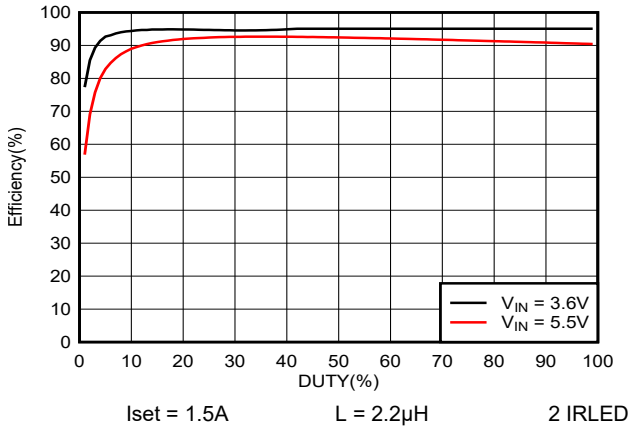


図 8-3. 2 IRLED Output Efficiency

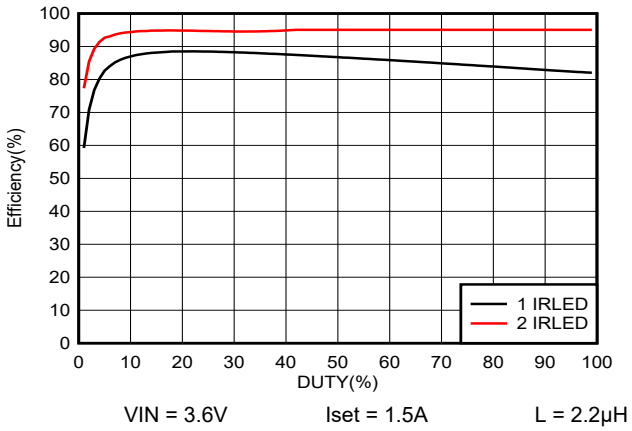


図 8-4. Output Efficiency at 3.6V Input Voltage

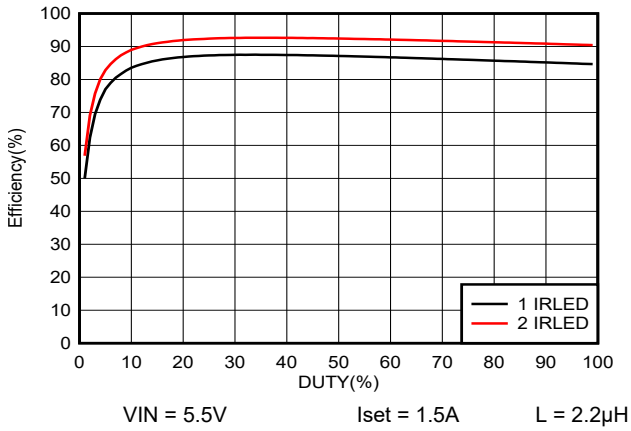


図 8-5. Output Efficiency at 5.5V Input Voltage

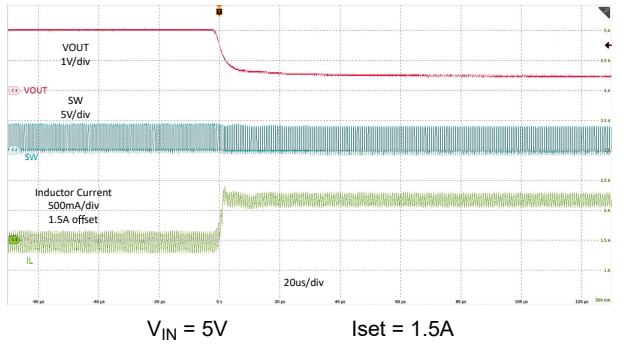


図 8-6. Vout short to GND protection

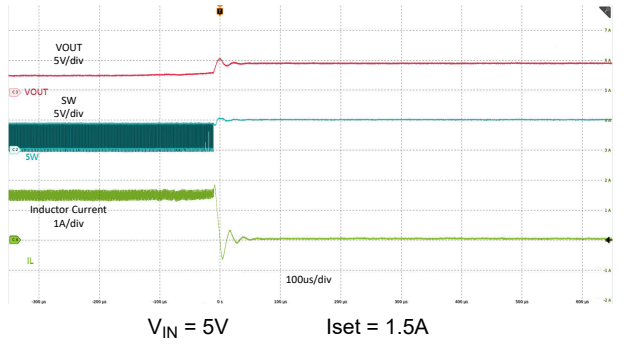
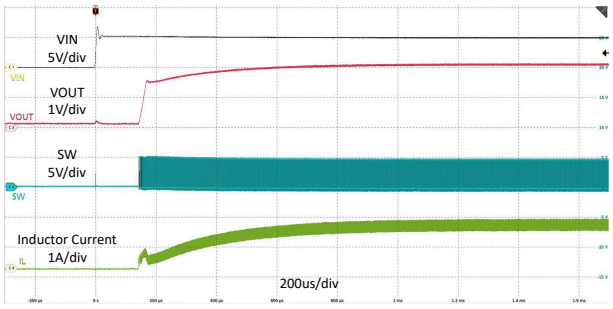
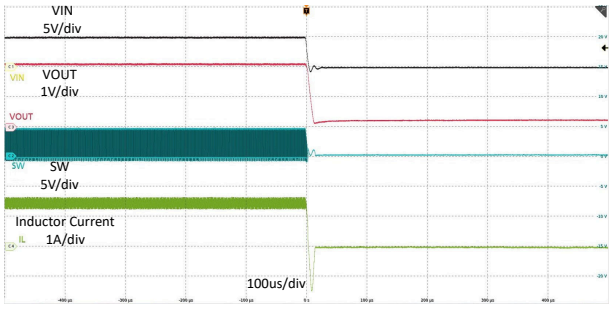


図 8-7. Vout Open Protection



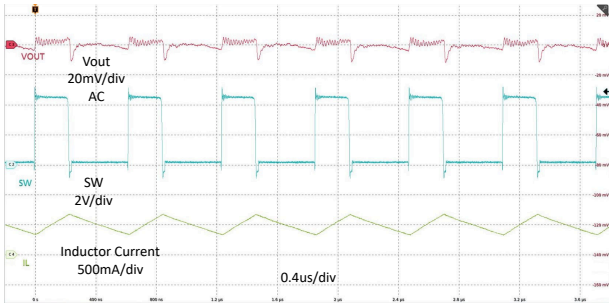
V_{IN} = 5V Iset = 1.5A L = 2.2µH

図 8-8. VIN Control Start Up with Load



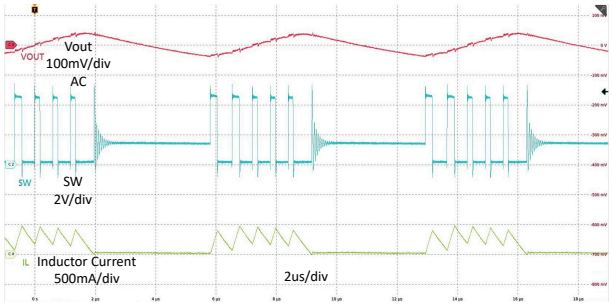
V_{IN} = 5V Iset = 1.5A L = 2.2µH

図 8-9. VIN Control Shutdown with Load



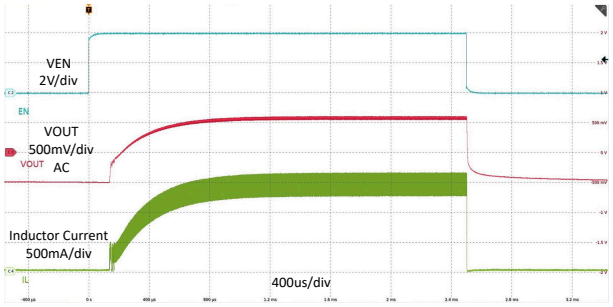
Vin = 5V I_{OUT} = 0.5A

図 8-10. PWM Operation



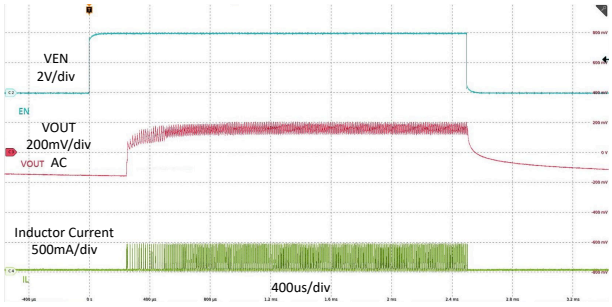
Vin = 5V I_{OUT} = 0.1A

図 8-11. Power Save Mode Operation



I_{OUT} = 1.5A L=2.2µH

図 8-12. EN Control Startup with Load



I_{OUT} = 0.1A L=2.2µH

図 8-13. EN Control Startup with Load

8.3 Power Supply Recommendations

The power supply to the TPS92201 must have a current rating according to the supply voltage, output voltage and output current.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS92201 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

8.4.2 Layout Example

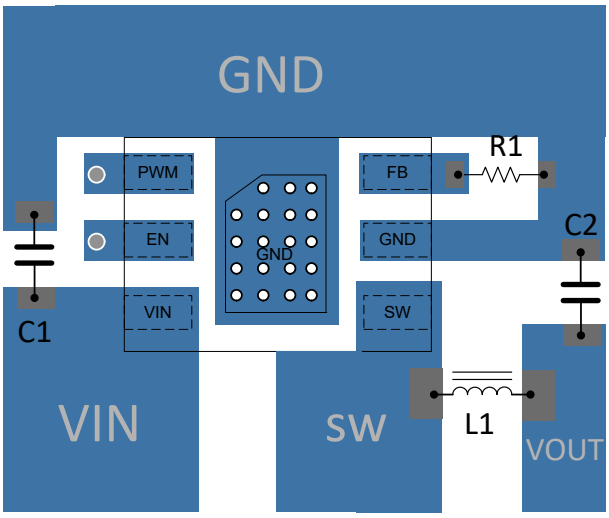


図 8-14. TPS92201WSON Layout

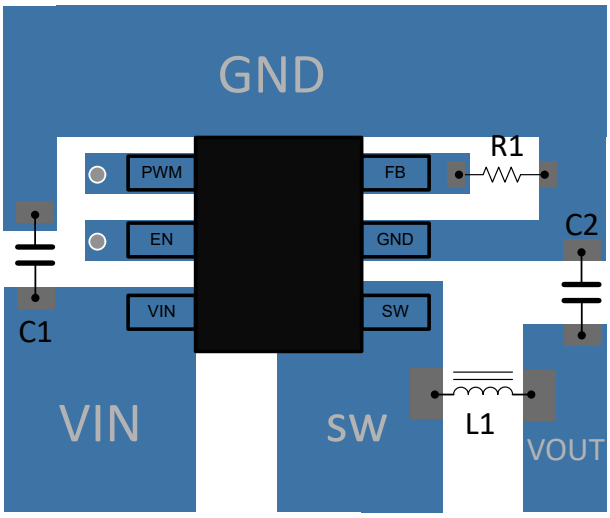


図 8-15. TPS92201SOT Layout

8.4.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS92201 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

Semiconductor and IC Package Thermal Metrics Application Report (SPRA953)

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report (SZZA017)

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2024) to Revision B (August 2024) **Page**

- SOT563-6 パッケージ オプションを記載するようにドキュメントを更新。 1

Changes from Revision * (November 2023) to Revision A (August 2024) **Page**

- 注文用型番のマーケティング ステータスを「製品プレビュー」から「量産データ」に更新..... 1
- Updated Device Comparison table to include the DRL package..... 2

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92201ADRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3GDH	Samples
TPS92201ADRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	34MH	Samples
TPS92201AMDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3CZH	Samples
TPS92201DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	34LH	Samples
TPS92201MDRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	3CXH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

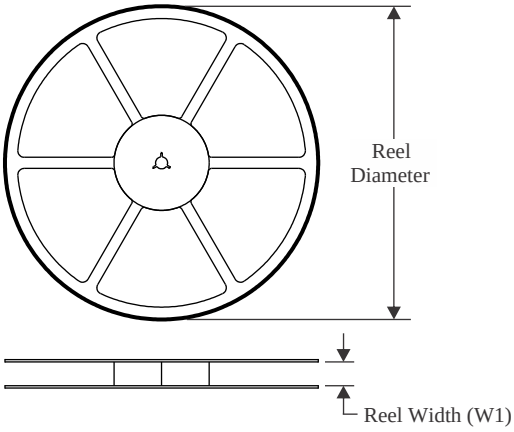
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

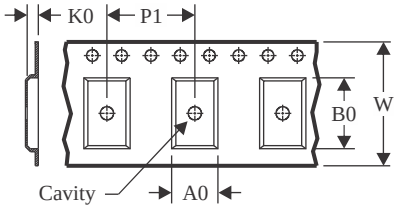
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

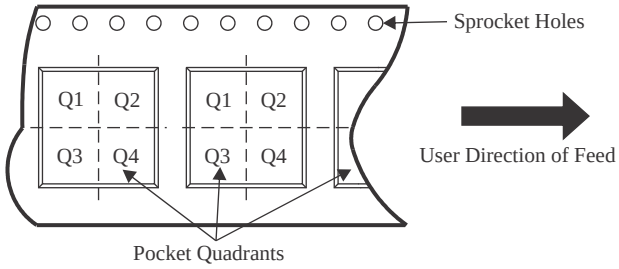


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

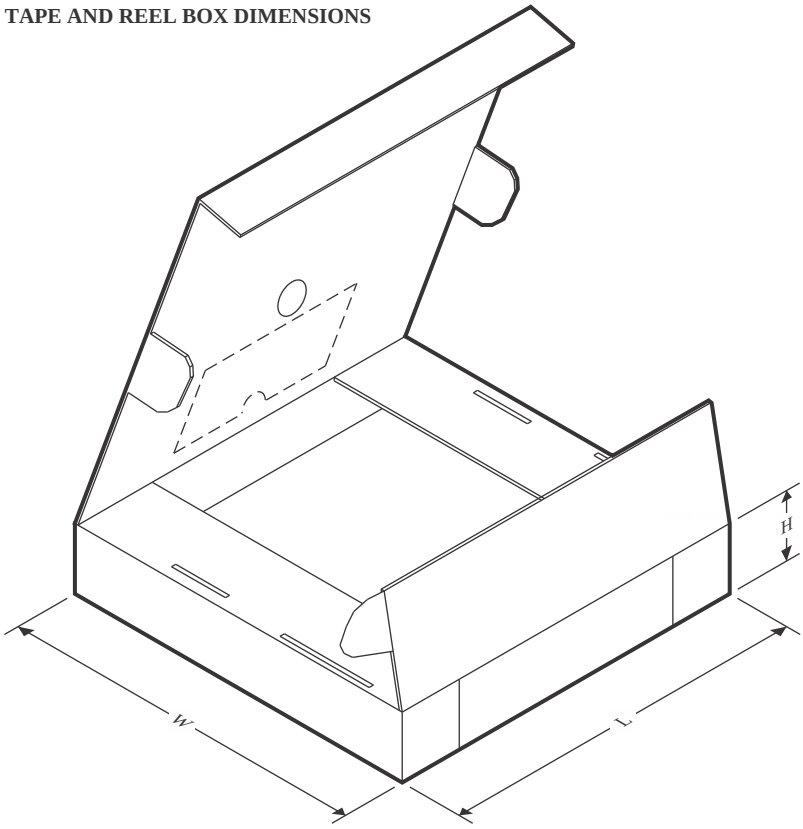
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92201ADRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS92201AMDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS92201DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS92201MDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

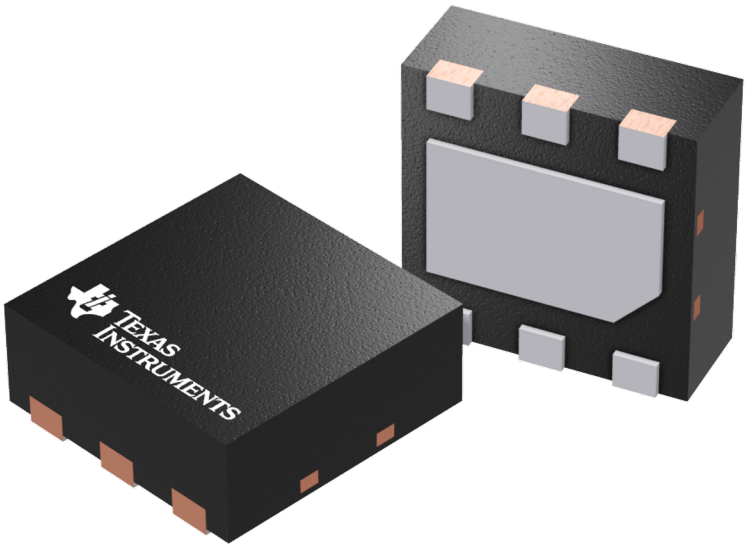


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92201ADRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS92201AMDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS92201DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS92201MDRVR	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



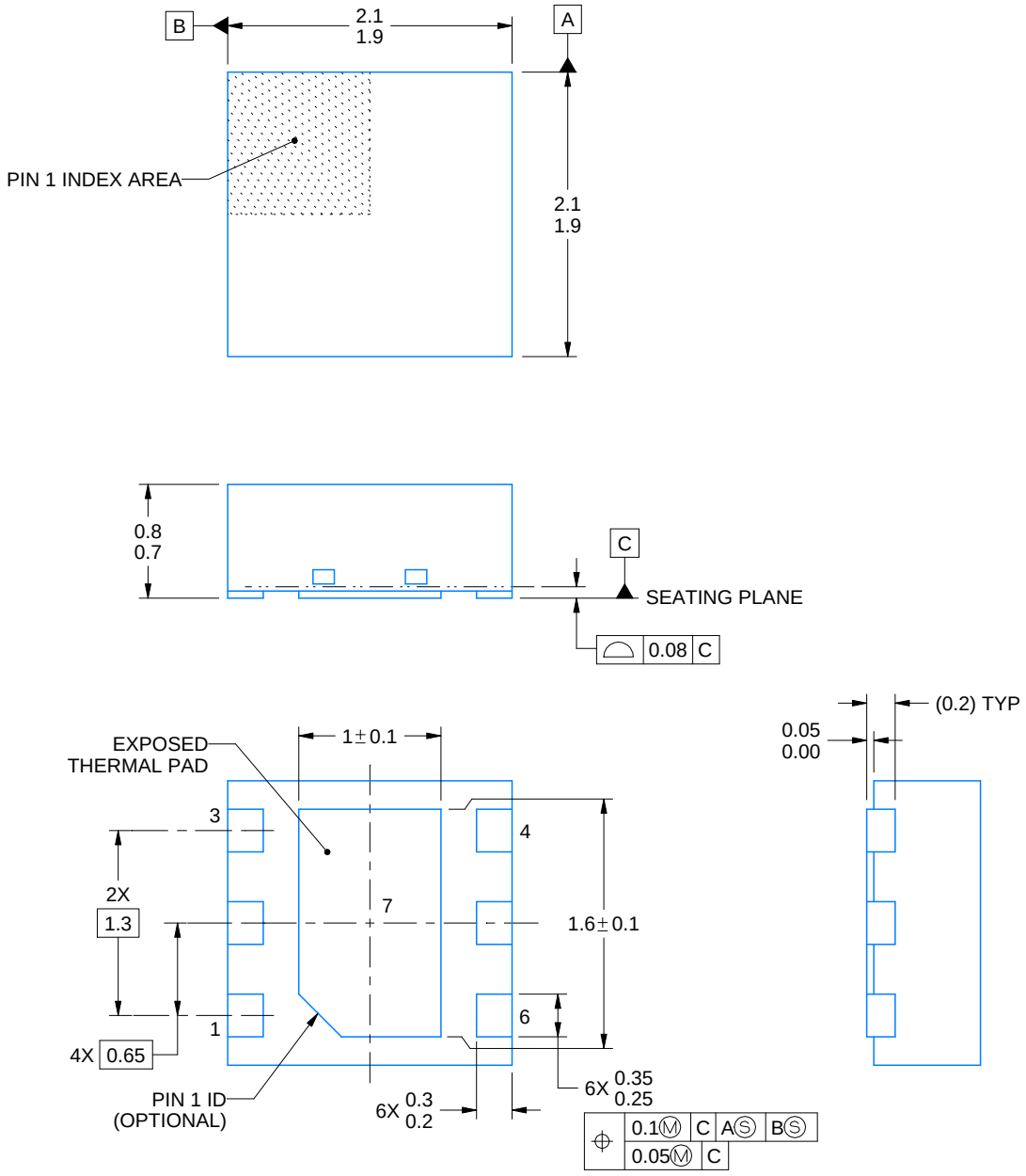
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

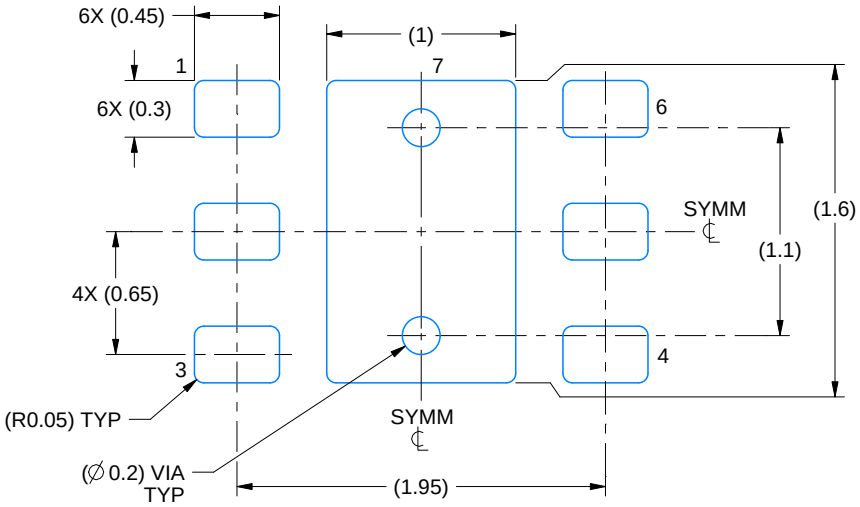
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

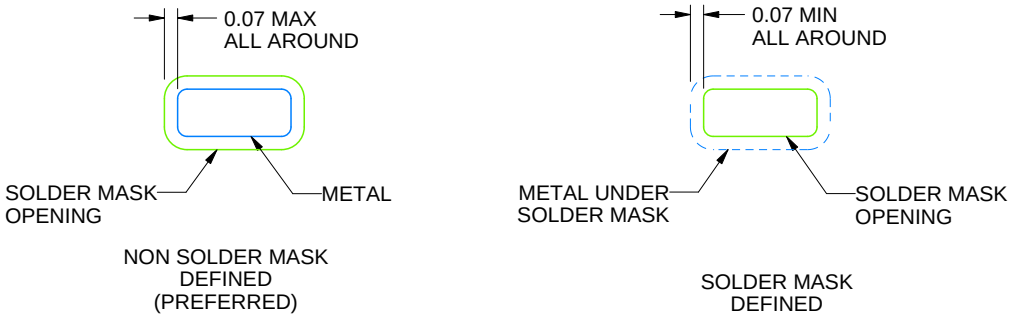


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

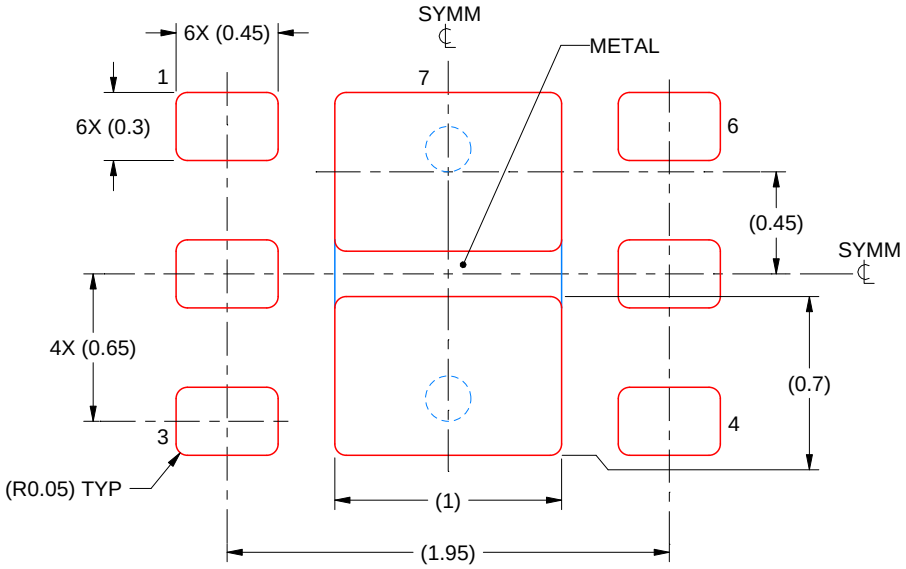
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

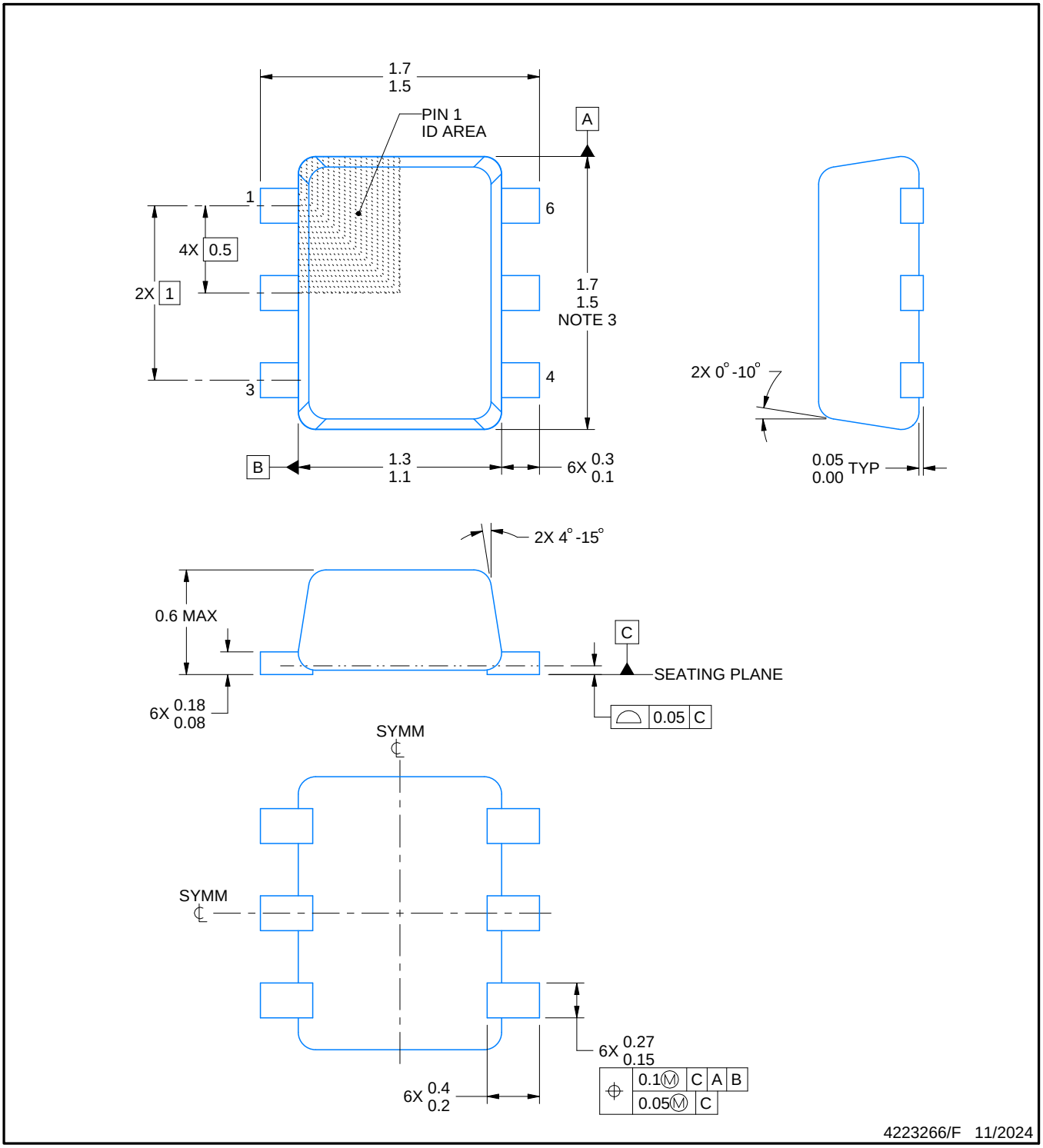
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

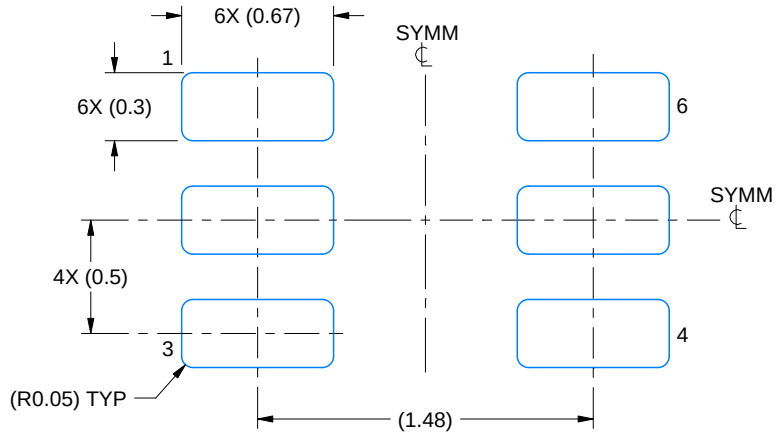
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

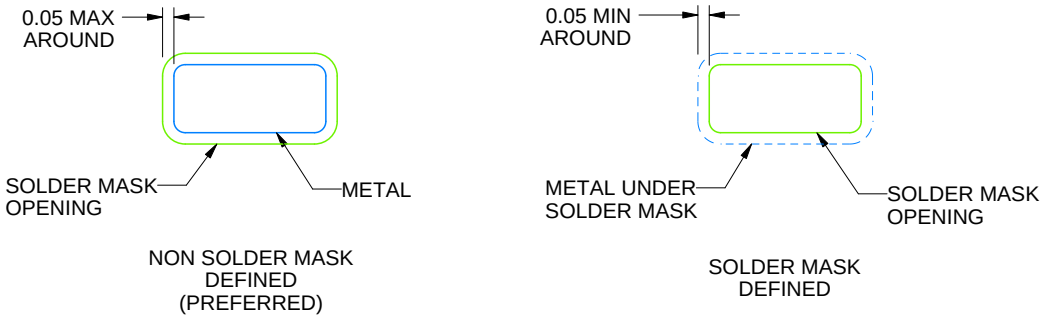
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

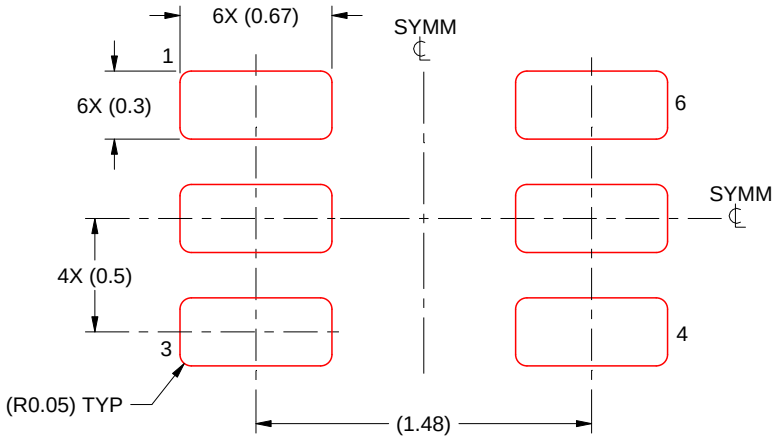
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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