# ADC10D1000QML Low-Power, 10-Bit, Dual 1-GSPS or Single 2-GSPS Analog-to-Digital Converter

## 1 Features

- Space Qualified
  - Total Ionizing Dose 100 krad(Si)
  - Single-Event Latch-Up 120 MeV-cm$^2$/mg
  - Single-Event Functional-Interrupt Immune 120 MeV-cm$^2$/mg (see *Radiation Reports*)
- Configurable to Either 1-GSPS Dual ADC or 2-GSPS Interleaved
- Low Power Consumption
- R/W SPI Interface for Extended Control Mode±
- Internally Terminated, Buffered, Differential Analog Inputs
- Test Patterns at Output for System Debug
- Programmable 15-Bit Gain and 12-Bit Plus Sign Offset Adjustments
- Option of 1:2 Demuxed or 1:1 Non-Demuxed LVDS Outputs
- Auto-Sync Feature for Multi-Chip Systems
- Single 1.9-V Power Supply
- Thermally Enhanced Column-Grid-Array Package

## 2 Applications

- Wideband Communications
- Direct RF Down Conversion
- Star Tracker

## 3 Description

The ADC10D1000 is a 10-bit, low-power, high-performance CMOS analog-to-digital converter (ADC) with sampling rates of up to 1 GSPS in dual-channel mode or 2 GSPS in single-channel mode. The ADC10D1000 achieves excellent accuracy and dynamic performance while consuming a typical 2.9 W of power.

The ADC10D1000 provides a flexible LVDS interface, which has multiple SPI-programmable options to facilitate board design and FPGA/ASIC data capture. The LVDS outputs are compatible with IEEE 1596.3-1996 and support programmable common-mode voltage.

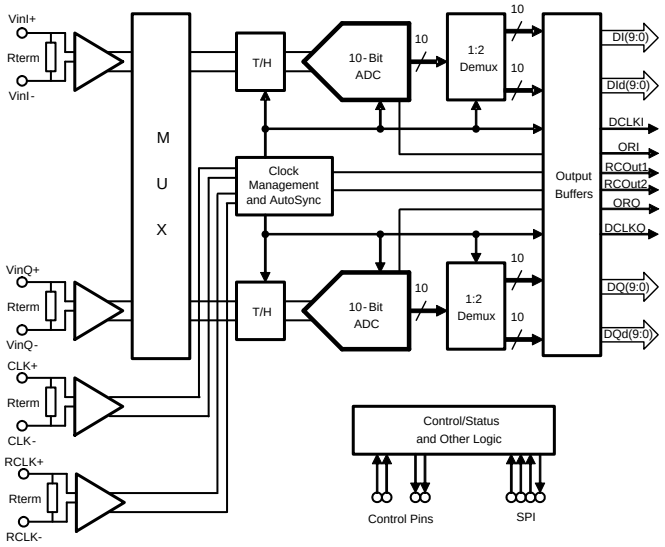
The product is packaged in a hermatic 376-pin column grid array (CCGA) that is thermally enhanced and rated over the temperature range of –55°C to +125°C.

**Device Information**(1)

| PART NUMBER | GRADE | PACKAGE |
|---|---|---|
| ADC10D1000CCMLS | Flight part 100 krad | CCGA (376) |
| ADC10D1000CCMPR | Pre-flight engineering prototype | CCGA (376) |
| ADC10D1000CVAL | Ceramic evaluation board | |
| ADC10D1000DAISY | Daisy chain, mechanical sample, no die | CCGA (376) |

(1) For all available packages, see the package orderable addendum (POA) at the end of the data sheet.

**Functional Block Diagram**



# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE RELEASED | REVISION | SECTION | CHANGES |
|---|---|---|---|
| 02/11/09 | A | Initial Release | New Product Data Sheet Release **(ECN SENT FOR APPROVAL 02/05/09 - Edit #: 16)** |
| 03/18/09 | B | Connection Diagram, Table 3. Section 8.0 - DCLK_RST± diagram, Section 18.0, paragraph 18.4.2. | Following Pin names corrected $V_A$, GND and $GND_{DR}$. Section 8.0 - Update DCLK_RST± diagram, Section 18.0 - paragraph added to 18.4.2 and new figure. Revision A will be Archived. |
| 4/20/09 | C | Features, Key Specifications, Table 10 Electricals. | Moved reference to radiation to Features from Key Specifications. Table 10 Electricals: $V_{OH}$ typo limit move to Min., Added parameters $V_{CMI\_DRST}$, $V_{ID\_DRST}$, $R_{IN\_DRST}$. Revision B will be Archived. |
| 05/28/09 | D | Absolute Maximum Ratings and Operating Ratings, Electrical Section Table 12, Section 19 Reserved Addr: Fh | Absolute Maximum Ratings added Voltage on $V_{IN}^+$, $V_{IN}^-$. Operating Ratings changed $V_{IN}^+$, $V_{IN}^-$ Voltage Range. Range. Remove Note 10 reference from Table 12 $t_{OSK}$, Correction to Reserved Addr: Fh. Revision C will be Archived. |
| 09/11/09 | E | Electrical Section Table 12 Calibration (Tcal), 17.0 Section, 19.0 Section (top register 4h) Addr: 4h (0100b) POR state: DA7Fh | Added Conditions to Tcal parameter, 17.0 Section New paragraph 17.4.3.4 and renumbered, Changed table 4h and title from Reserved to Calibration Adjust in 19.0 Section. Revision D will be Archived. |

## Revision History (continued)

| DATE RELEASED | REVISION | SECTION | CHANGES |
|---|---|---|---|
| 05/10/2010 | F | Ordering Information Table, Table 6, Table 10 Electrical Section. Sections 15.0, 17.0, 17.4.3, 19.0 Configuration Register 1 Bit 6 | Added reference to MPR and CVAL NSPN. Table 6 section 1:2 Demux Non-DES Mode, Extended Control Mode, FM (14:0) = 7FFFh SNR Limit and 1:2 Demux Non-DES Mode, Non-Extended Control Mode, FSR = VA. Table 10 Digital Control Pins. Update Figure 11, Added New Figure 12 and 13, Renumbered previous Figure 12 and 13 to Figure 14 and 15 etc. Changed paragraph 17.4.3. Configuration Register 1– Bit 6 paragraph. Revision E will be Archived. |
| 12/07/2016 | G | Added *Device Information* table, *ESD Ratings* table, *Detailed Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section; updated values in the *Thermal Information* table to align with JEDEC standards; add pin VCMOS and information regarding usage throughout data sheet; update several pin names; removed maximum supply current values in *Converter Electrical Characteristics: Power Supply Characteristics (1:2 Demux Mode)*, leaving only power consumption specifications; conform other content to match format of similar data sheets in same device family; change "Panasonic part number ECJ-0EB1A104K" to "Presidio part number SR0402X7R104KENG5" in *Power Supply*; update *Abs Max* and *ROC* tables | |

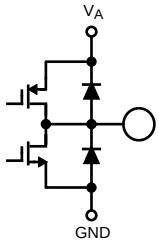
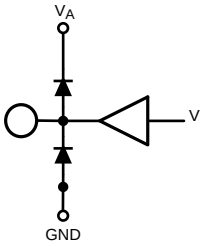
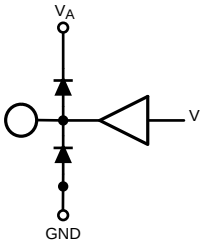
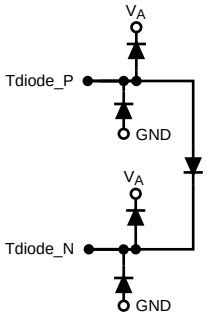
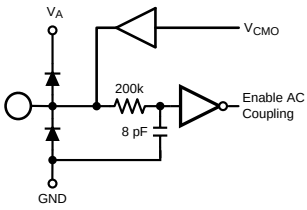
# 5 Pin Configuration and Functions

**NAA Package**
**376-Pin CPGA Package**
**Top View**

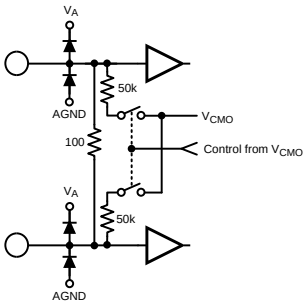
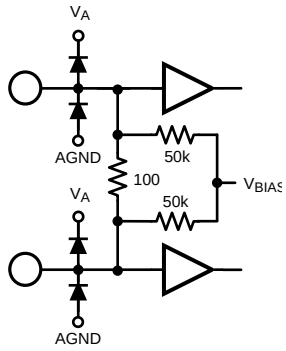
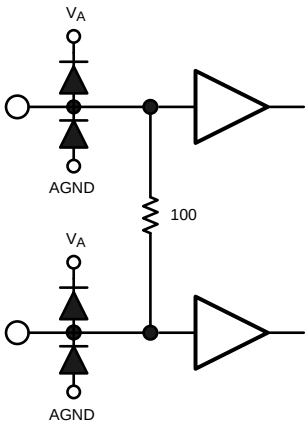
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | V_A | SDO | TPM | NDM | V_A | GND | V_E | GND_E | GND_DR | V_DR | DId1+ | GND_DR | DId4+ | V_DR | DId7+ | GND_DR | DId9+ | DId9- | GND_DR | A |
| B | Vbg | GND | $\overline{ECE}$ | SDI | CalRun | V_A | GND | GND_E | V_E | GND_DR | DId0+ | DId1- | DId3+ | DId4- | DId6+ | DId7- | DId8+ | GND_DR | GND_DR | GND_DR | B |
| C | Rtrim+ | Vcmo | Rext+ | $\overline{SCS}$ | SCLK | GND | V_A | V_E | GND_E | GND_DR | DId0- | DId2+ | DId3- | DId5+ | DId6- | DId8- | GND_DR | V_DR | DI0+ | DI0- | C |
| D | V_A | Rtrim- | Rext- | GND | GND | CAL | VbiasI | V_A | V_A | GND_DR | V_DR | DId2- | GND_DR | DId5- | V_DR | GND_DR | V_DR | DI1+ | DI2+ | DI2- | D |
| E | V_A | Tdiode+ | RSV1 | GND | | | | | | | | | | | | | GND_DR | DI1- | DI3+ | DI3- | E |
| F | V_A | GND_TC | Tdiode- | RSV2 | | | | | | | | | | | | | GND_DR | DI4+ | DI4- | GND_DR | F |
| G | V_TC | GND_TC | V_TC | V_TC | | | | | | | | | | | | | DI5+ | DI5- | DI6+ | DI6- | G |
| H | VinI+ | V_TC | GND_TC | V_A | | | | | | | | | | | | | DI7+ | DI7- | DI8+ | DI8- | H |
| J | VinI- | GND_TC | V_TC | VbiasI | | | | | | | | | | | | | V_DR | DI9+ | DI9- | V_DR | J |
| K | GND | VbiasI | V_TC | GND_TC | | | | | | | | | | | | | ORI+ | ORI- | DCLKI+ | DCLKI- | K |
| L | GND | VbiasQ | V_TC | GND_TC | | | | | | | | | | | | | ORQ+ | ORQ- | DCLKQ+ | DCLKQ- | L |
| M | VinQ- | GND_TC | V_TC | VbiasQ | | | | | | | | | | | | | GND_DR | DQ9+ | DQ9- | GND_DR | M |
| N | VinQ+ | V_TC | GND_TC | V_A | | | | | | | | | | | | | DQ7+ | DQ7- | DQ8+ | DQ8- | N |
| P | V_TC | GND_TC | V_TC | V_TC | | | | | | | | | | | | | DQ5+ | DQ5- | DQ6+ | DQ6- | P |
| R | V_A | GND_TC | V_TC | V_TC | | | | | | | | | | | | | V_DR | DQ4+ | DQ4- | V_DR | R |
| T | V_A | GND_TC | GND_TC | GND | | | | | | | | | | | | | V_DR | DQ1- | DQ3+ | DQ3- | T |
| U | GND_TC | CLK+ | PDI | GND | GND | RCOut1- | VbiasQ | V_A | V_A | GND_DR | V_DR | DQd2- | GND_DR | DQd5- | V_DR | V_DR | GND_DR | DQ1+ | DQ2+ | DQ2- | U |
| V | CLK- | DCLK_RST+ | PDQ | GND | GND | RCOut2+ | RCOut2- | V_E | GND_E | GND_DR | DQd0- | DQd2+ | DQd3- | DQd5+ | DQd6- | DQd8- | GND_DR | GND_DR | DQ0+ | DQ0- | V |
| W | DCLK_RST- | GND | RSV | DDRPh | RCLK- | V_A | GND | GND_E | V_E | GND_DR | DQd0+ | DQd1- | DQd3+ | DQd4- | DQd6+ | DQd7- | DQd8+ | GND_DR | GND_DR | GND_DR | W |
| Y | GND | V_A | FSR | RCLK+ | RCOut1+ | V_A | GND | V_E | GND_E | GND_DR | V_DR | DQd1+ | GND_DR | DQd4+ | V_DR | DQd7+ | GND_DR | DQd9+ | DQd9- | GND_DR | Y |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AA | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AB | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AC | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AE | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AF | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AG | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AH | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AJ | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AK | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |
| AL | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND |

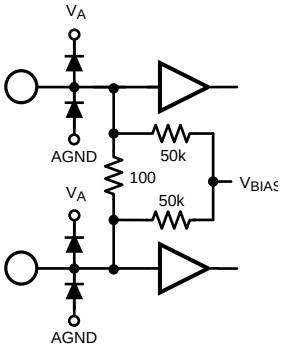
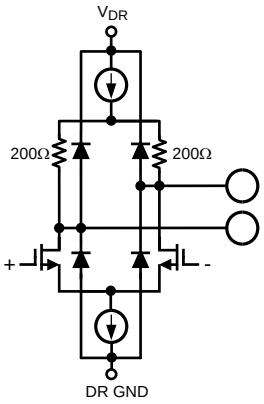
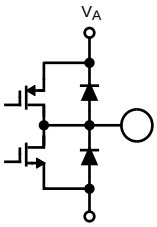
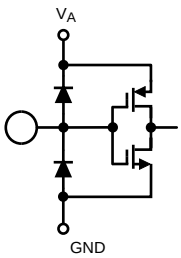
## Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| **ANALOG FRONT-END AND CLOCK PINS** | | | |
| B1 | $V_{BG}$ |  | Bandgap voltage output or LVDS common-mode voltage select. This pin provides the bandgap output voltage and is capable of sourcing/ sinking 100 µA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the higher LVDS common-mode voltage is selected. The lower value is the default. |
| C1/D2 | Rtrim+<br>Rtrim– |  | External reference and input termination trim resistor terminals. A 3.3-kΩ ±0.1% resistor must be connected between Rtrim+, Rtrim–. The Rtrim resistor is used to establish the calibrated 100-Ω input impedance of VinI+, VinI–, VinQ+, VinQ– and CLK+, CLK-. These impedances may be fine-tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not ensured for such an alternate value. |
| C3/D3 | Rext+<br>Rext– |  | Connect a 3.3-kΩ ±0.1% resistor connected between Rext+, Rext–. The Rext resistor is used for setting internal temperature-independent bias currents; the value and precision of this resistor must not be compromised. |
| E2/F3 | Tdiode+<br>Tdiode– |  | Temperature sensor diode positive (anode) and negative (cathode) terminals. This set of pins is used for die temperature measurements. |
| C2 | $V_{CMO}$ |  | Common-mode voltage output or signal coupling select. If AC-coupled operation at the analog inputs is desired, this pin must be held at logic-low level. This pin is capable of sourcing and sinking up to 100 µA. For DC-coupled operation, $V_{CMO}$, leave this pin floating or terminated into high-impedance. In DC-coupled mode, this pin provides an output voltage which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer. |

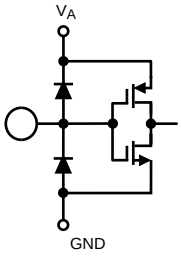
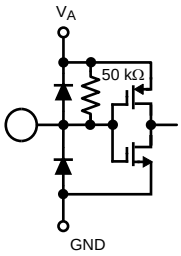
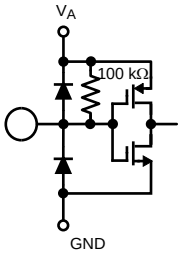
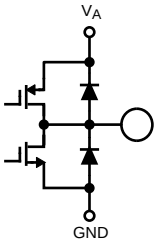
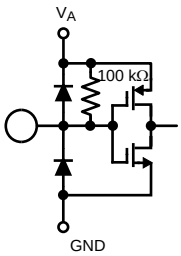
## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| H1/J1<br>N1/M1 | VinI+, VinI–<br>VinQ+, VinQ– |  | Differential signal I-channel and Q-channel inputs. In the non-dual edge sampling (non-DES) mode, each I-input and Q-input is sampled and converted by its respective channel with each positive transition of the CLK input. In non-extended control mode (non-ECM) and DES mode, both channels sample the I input. In extended control mode (ECM), the Q-channel input may optionally be selected for conversion in DES mode by the DEQ bit (Addr: 0**h**, Bit 6).<br>Each I-channel input and Q-channel input has an internal common mode bias that is disabled when DC-coupled mode is selected. Both inputs must be either AC- or DC-coupled. The coupling mode is selected by the $V_{CMO}$ pin.<br>In non-ECM, the full-scale range of these inputs is determined by the FSR pin; both I channel and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set through the Control Register (Addr: 3**h** and Addr: B**h**). The high and low full-scale input range setting in non-ECM corresponds to the mid and minimum full-scale input range in ECM.<br>The input offset may also be adjusted in ECM. |
| U2/V1 | CLK+<br>CLK– |  | Differential converter sampling clock. In the non-DES mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES mode, the Q channel is sampled on both transitions of this clock. This clock must be AC-coupled. Additional features include an LC filter on the clock input. |
| V2/W1 | DCLK_RST+<br>DCLK_RST– |  | Differential DCLK reset. A positive pulse on this input is used to reset the DCLKI+, DCLKI– and DCLKQ+, DCLKQ– outputs of two or more ADC10D1000 devices in order to synchronize them with other ADC10D1000 devices in the system. DCLKI+, DCLKI– and DCLKQ+, DCLKQ– are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST+, DCLK_RST– to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK+, CLK– inputs. This feature may still be used while the chip is in the AutoSync mode. |

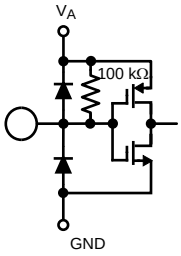
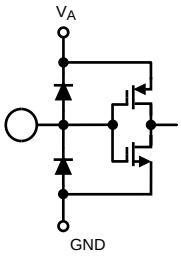
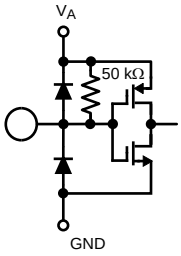
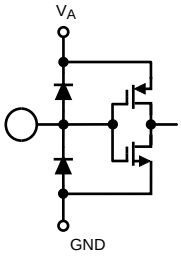
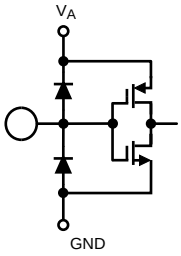
## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| Y4/W5 | RCLK+<br>RCLK– |  | Reference clock input. When the AutoSync feature is active and the ADC10D1000 is in slave mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via the Control Register (Addr: E**h**). |
| Y5/U6<br>V6/V7 | RCOut1+,<br>RCOut1–<br>RCOut2+,<br>RCOut2– |  | Reference clock output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in master or slave mode. They are used to drive the RCLK of another ADC10D1000, in order to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1+, RCOut1– and RCOut2+, RCOut2– to the RCLK+, RCLK– of another ADC10D1000 must be 100-Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: E**h**, Bit 1) to enable/ disable this feature; the default is disabled. |
| **CONTROL AND STATUS PINS** | | | |
| A3 | SDO |  | Serial data out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is in tri-state mode when $\overline{SCS}$ is de-asserted. |
| A4 | TPM |  | Test pattern mode. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the test pattern mode can only be activated through the TPM bit of the Control Register (Addr: 0**h**, Bit 12). |

## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A5 | NDM |  | Non-demuxed mode. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-demuxed mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 demuxed mode. This feature is pin-controlled only and remains active during ECM and non-ECM. |
| B3 | $\overline{\text{ECE}}$ |  | Extended control enable. Extended feature control through the SPI interface is enabled when this signal is asserted logic-low. In this case, most of the direct control pins have no effect. When this signal is de-asserted, that is, logic-high, the SPI interface is disabled and the direct control pins are enabled. |
| B4 | SDI |  | Serial data-in. In ECM, serial data is shifted into the device on this pin while the $\overline{\text{SCS}}$ signal is asserted (logic-low). |
| B5 | CalRun |  | Calibration running Indication. This output is logic-high while the calibration sequence is executing, and logic-low while the calibration sequence is not running. |
| C4 | $\overline{\text{SCS}}$ |  | Serial chip select. In ECM, when this signal is asserted logic-low, SCLK is used to clock in serial data that is present on the SDI input and to source serial data on the SDO output. When this signal is de-asserted, that is, logic-high, the SDI input is ignored and the SDO output is in tri-state mode. |

## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| C5 | SCLK |  | Serial clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, so long as timing specifications are not violated when the clock is enabled or disabled. |
| D6 | CAL |  | Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of $t_{CAL\_H}$ after having held it low a minimum of $t_{CAL\_L}$. This pin is active in both ECM and non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0**h**, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration. |
| U3<br>V3 | PDI<br>PDQ |  | Power-down I channel and Q-channel. Setting either input to logic-high powers down the respective I-channel or Q-channel converter. Setting either input to logic-low brings the respective I channel or Q-channel converter to a fully operational state after a finite time delay. This pin is active in both ECM and non-ECM. In the ECM, either this pin or the PDI and PDQ bit in the Control Register can be used to power-down the I channel and Q channel (Addr: 0**h**, Bit 11 and Bit 10), respectively. |
| W3 | RSV | NONE | Reserved: This pin is used for internal purposes and must be connected to GND through a 100-KΩ resistor. |
| W4 | DDRPh |  | DDR phase select. This input, when logic-low, selects the 0-degree data-to-DCLK phase relationship; when logic-high, the input selects the 90-degree data-to-DCLK phase relationship. This pin only has an effect when the chip is in 1:2 demuxed mode; for example, when the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the DPS bit of the Control Register (Addr: 0**h**, bit 14); the default is 0-degree data-to-DCLK phase relationship. |
| Y3 | FSR |  | Full-scale input range select. In non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I-channel and Q-channel inputs is set to the lower or higher value, respectively. In ECM, this input is ignored and the full-scale range of the I-channel and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the higher and lower FSR value in non-ECM does not precisely correspond to the maximum and minimum available selection in ECM; in ECM, the selection range is greater. |

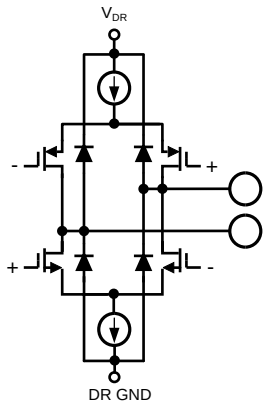
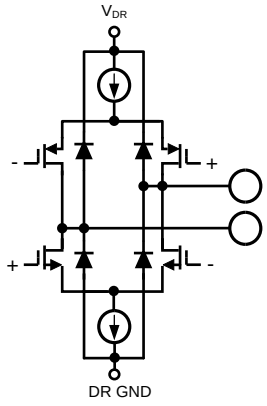
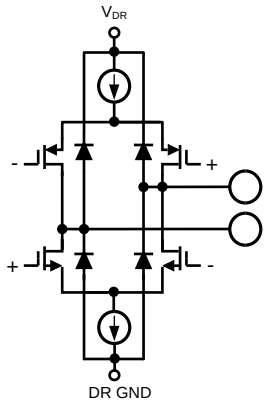
## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| **POWER AND GROUND PINS** | | | |
| A1, A7, B2, B7, C6, D4, D5, E4, K1, L1, T4, U4, U5, V4, V5, W2, W7, Y1, Y7, AA2thru AL11 | GND | NONE | Analog ground return |
| A2, A6, B6, C7, D1, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6 | $V_A$ | NONE | Analog power supply. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply. |
| A8, B9, C8, V8, W9, Y8 | $V_E$ | NONE | Power supply for the digital encoder |
| A9, B8, C9, V9, W8, Y9 | $GND_E$ | NONE | Ground return for the digital encoder |
| A10, A13, A17, A20, B10 B18, B19, B20, C10, C17, D10, D13, D16, E17, F17, F20, M17, M20, U10,U13, U17, V10, V17, V18, W10, W18, W19, W20, Y10, Y13, Y17, Y20 | $GND_{DR}$ | NONE | Ground return for the output driver |
| A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15 | $V_{DR}$ | NONE | Power supply for the output drivers |
| D7, J4, K2 | VbiasI | NONE | Bias voltage I channel. This is an externally decoupled bias voltage for the I channel. Each pin must individually be decoupled with a 100-nF capacitor via a low resistance, low inductance path to GND. |
| E3 | RSV1 | NONE | Reserved: This pin is used for internal purposes. This pin must individually be decoupled with a 100-nF capacitor via a low resistance, low inductance path to GND. |
| F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1 | $GND_{TC}$ | NONE | Analog ground return for the track-and-hold and clock circuitry |
| L2, M4, U7 | VbiasQ | NONE | Bias voltage Q channel. This is an externally decoupled bias voltage for the Q channel. Each pin must individually be decoupled with a 100-nF capacitor via a low resistance, low inductance path to GND. |
| F4 | RSV2 | NONE | Reserved: This pin is used for internal purposes. This pin must individually be decoupled with a 100-nF capacitor via a low resistance, low inductance path to GND. |

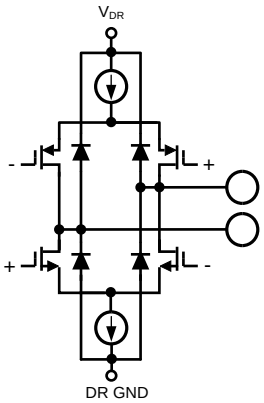
## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4 | $V_{TC}$ | NONE | Analog power supply for the track-and-hold and clock circuitry |

## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| **HIGH-SPEED DIGITAL OUTPUTS** | | | |
| A18/A19<br>B17/C16<br>A16/B16<br>B15/C15<br>C14/D14<br>A14/B14<br>B13/C13<br>C12/D12<br>A12/B12<br>B11/C11<br>.<br>Y18/Y19<br>W17/V16<br>Y16/W16<br>W15/V15<br>V14/U14<br>Y14/W14<br>W13/V13<br>V12/U12<br>Y12/W12<br>W11/V11 | DId9+, DId9–<br>DId8+, DId8–<br>DId7+, DId7–<br>DId6+, DId6–<br>DId5+, DId5–<br>DId4+, DId4–<br>DId3+, DId3–<br>DId2+, DId2–<br>DId1+, DId1–<br>DId0+, DId0–<br>.<br>DQd9+, DQId9–<br>DQd8+, DQd8–<br>DQd7+, DQd7–<br>DQd6+, DQd6–<br>DQd5+, DQd5–<br>DQd4+, DQd4–<br>DQd3+, DQd3–<br>DQd2+, DQd2–<br>DQd1+, DQd1–<br>DQd0+, DQd0– |  | Delayed I-channel and Q-channel digital data outputs. In non-demux mode, these outputs are tri-stated. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, that is, the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. Each of these outputs must always be terminated with a 100-Ω differential resistor placed as closely as possible to the differential receiver. |
| J18/J19<br>H19/H20<br>H17/H18<br>G19/G20<br>G17/G18<br>F18/F19<br>E19/E20<br>D19/D20<br>D18/E18<br>C19/C20<br>.<br>M18/M19<br>N19/N20<br>N17/N18<br>P19/P20<br>P17/P18<br>R18/R19<br>T19/T20<br>U19/U20<br>U18/T18<br>V19/V20 | DI9+, DI9–<br>DI8+, DI8–<br>DI7+, DI7–<br>DI6+, DI6–<br>DI5+, DI5–<br>DI4+, DI4–<br>DI3+, DI3–<br>DI2+, DI2–<br>DI1+, DI1–<br>DI0+, DI0–<br>.<br>DI9+, DI9–<br>DQ8+, DQ8–<br>DQ7+, DQ7–<br>DQ6+, DQ6–<br>DQ5+, DQ5–<br>DQ4+, DQ4–<br>DQ3+, DQ3–<br>DQ2+, DQ2–<br>DQ1+, DQ1–<br>DQ0+, DQ0– |  | I-channel and Q-channel digital data outputs. In non-demux mode, this LVDS data is transmitted at the sampling clock rate. In demux mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, that is, the other ½ of the data, which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. Always terminate each of these outputs with a 100-Ω differential resistor placed as closely as possible to the differential receiver |
| K17/K18<br>L17/L18 | ORI+, ORI–<br>ORQ+, ORQ– |  | Out-of-range output for the I channel and Q channel. This differential output is asserted logic-high while the over- or under-range condition exists, that is, the differential signal at each respective analog input exceeds the full-scale value. Each OR results refers to the current data, with which it is clocked out. Always terminate each of these outputs with a 100-Ω differential resistor placed as closely as possible to the differential receiver. |

**Pin Functions (continued)**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| K19/K20<br>L19/L20 | DCLKI+, DLKI–<br>DCLKQ+,<br>DLKQ– |  | Data clock output for the I-channel and Q-channel data bus. These differential clock outputs are used to latch the output data and must always be terminated with a 100-Ω differential resistor. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 demux mode or non-demux mode, this signal is at ¼ or ½ the input clock rate, respectively. DCLKI+, DLKI– and DCLKQ+, DLKQ– are always in phase with each other, unless one channel is powered down, and they do not require a pulse from DCLK_RST+, DCLK_RST– to become synchronized. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage ($V_A$, $V_{TC}$, $V_{DR}$, $V_E$) | | 2.2 | V |
| Supply difference – max($V_{A/TC/DR/E}$) – min($V_{A/TC/DR/E}$) | 0 | 100 | mV |
| Voltage on any input pin (except VinI+, VinI–, VinQ+, VinQ–) | –0.15 | ($V_A$ + 0.15) | V |
| VinI+, VinI–, VinQ+, VinQ– voltage(3) | –0.5 | 2.5 | V |
| Input current at VinI+, VinI–, VinQ+, VinQ–(4) | | 50 | mA |
| Ground difference – max($GND_{TC/DR/E}$) – min($GND_{TC/DR/E}$) | 0 | 100 | mV |
| Input current at any pin(4) | | ±50 | mA |
| Package power dissipation at $T_A \le 85°C$(4) | | 3.45 | W |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = $GND_{DR}$ = $GND_E$ = $GND_{TC}$ = 0 V, unless otherwise specified.
(3) Verified during product qualification high-temperature lifetime testing (HTOL) at $T_J$ = 150°C for 1000 hours continuous operation with $V_A$ = $V_D$ = 2.2 V.
(4) When the input voltage at any pin exceeds the power supply limits, that is, less than GND or greater than $V_A$, the current at that pin must be limited to 50 mA. In addition, overvoltage at a pin must adhere to the maximum voltage limits. Simultaneous overvoltage at multiple pins requires adherence to the maximum package power dissipation limits. These dissipation limits are calculated using JEDEC JESD51-7 thermal model. Higher dissipation may be possible based on specific customer thermal situation and specified package thermal resistances from junction to case.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±8000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |
| | | Machine model | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Ambient temperature, $T_A$ | | –55 | | 125 | °C |
| Supply voltage ($V_A$, $V_{TC}$, $V_E$) | | 1.8 | | 2 | V |
| Driver supply voltage ($V_{DR}$) | | 1.8 | | $V_A$ | V |
| VinI+, VinI–, VinQ+, VinQ– voltage(2) | DC-coupled | –0.4 | | 2.4 | V |
| VinI+, VinI–, VinQ+, VinQ– differential voltage(3) | DC-coupled at 100% duty cycle | | | 1 | V |
| | DC-coupled at 20% duty cycle | | | 2 | |
| | DC-coupled at 10% duty cycle | | | 2.8 | |
| VinI+, VinI–, VinQ+, VinQ– current(2) | AC-coupled | –50 | | 50 | mA |
| VinI+, VinI–, VinQ+, VinQ– power | Maintaining common-mode voltage AC-coupled | | | 15.3 | dBm |
| | Not maintaining common-mode voltage, AC-coupled | | | 17.1 | |
| Ground difference – max($GND_{TC/DR/E}$) – min($GND_{TC/DR/E}$) | | | | 0 | V |
| CLK+, CLK– voltage | | 0 | | $V_A$ | V |
| Differential CLK amplitude | | 0.4 | | 2 | $V_{P-P}$ |
| $V_{CMI}$ common-mode input voltage | | $V_{CMO}$ – 150 | | $V_{CMO}$ + 150 | mV |

(1) All voltages are measured with respect to GND = $GND_{DR}$ = $GND_E$ = $GND_{TC}$ = 0 V, unless otherwise specified.
(2) Proper common-mode voltage must be maintained to ensure proper output codes, especially during input overdrive.
(3) This rating is intended for DC-coupled applications; the voltages and duty cycles listed may be safely applied to $V_{IN}$± for the lifetime of the part.

## 6.4 Thermal Information

| THERMAL METRIC(1)(2) | | ADC10D1000QML-SP NAA (CCGA) 376 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 13.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 5.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 5.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.7 | °C/W |

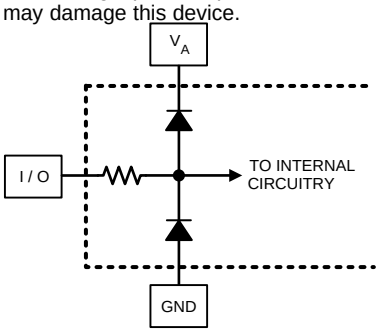
(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Solder process specifications in *Board Mounting Recommendation*.

## 6.5 Converter Electrical Characteristics: Static Converter Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q-channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| INL | Integral non-linearity | DC-coupled, 1-MHz sine wave over-ranged | [1, 2, 3] | | ±0.7 | ±1.4 | LSB |
| DNL | Differential non-linearity | DC-coupled, 1-MHz sine wave over-ranged | [1, 2, 3] | | ±0.2 | ±0.5 | LSB |
| | Resolution with no missing codes | | [1, 2, 3] | | | 10 | bits |
| $V_{OFF}$ | Offset error | | | | –2.8 | | LSB |
| $V_{OFF\_ADJ}$ | Input offset adjustment range | | | | ±45 | | mV |
| PFSE | Positive full-scale error | See(5) | [1, 2, 3] | | | ±28 | mV |
| NFSE | Negative full-scale error | See(5) | [1, 2, 3] | | | ±28 | mV |
| | Out-of-range output code | $(V_{IN}+) - (V_{IN}-) >$ + full scale | [1, 2, 3] | | | 1023 | |
| | | $(V_{IN}+) - (V_{IN}-) >$ – full scale | [1, 2, 3] | | | 0 | |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



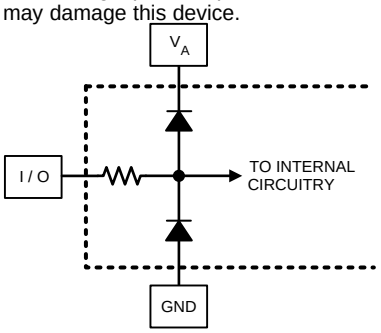

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(5) Calculation of full-scale error for this device assumes that the actual reference voltage is exactly its nominal value. Full-scale error for this device, therefore, is a combination of full-scale error and reference voltage error. For relationship between gain error and full-scale error, see gain error in *Specification Definitions*.

## 6.6 Converter Electrical Characteristics: Dynamic Converter Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q-channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| FPBW | Full-power bandwidth | Non-DES mode | | | 2.8 | | GHz |
| | | DES mode | | | 1.3 | | |
| CER | Code error rate | | | | $10^{-18}$ | | Error/Sample |
| | Gain flatness | DC to 498 MHz | | | ±0.25 | | dBFS |
| | | DC to 1 GHz | | | ±0.5 | | |
| NPR | Noise power ratio | $f_c$ = 325 MHz, notch width = 25 MHz | | | 47.5 | | dB |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.




(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

## Converter Electrical Characteristics: Dynamic Converter Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q-channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **1:2 DEMUX NON-DES MODE, EXTENDED CONTROL MODE, FM (14:0) = 7FFFh** | | | | | | | |
| ENOB | Effective number of bits | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 8.4 | 9 | | bits |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 7.8 | 9 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 8.2 | 8.9 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS, | [6] | 7.8 | 8.9 | | |
| SINAD | Signal-to-noise plus distortion ratio | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS, | [4, 5] | 52.2 | 55.8 | | dB |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 48.5 | 55.8 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 51 | 56.8 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 48.8 | 56.8 | | |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 53.2 | 56.8 | | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 49.4 | 56.8 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 52 | 56.1 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 49.4 | 56.1 | | |
| THD | Total harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | | –68 | –59 | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | | –68 | –56 | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | | –61 | –58 | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | | –61 | –57 | |
| 2nd Harm | Second harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | | | −75 | | dBc |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −68 | | |
| 3rd Harm | Third harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | | | −72 | | dBc |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −67 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 59 | 63 | | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 53 | 63 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 57.5 | 63 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 54.5 | | | |

## Converter Electrical Characteristics: Dynamic Converter Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q-channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **NON-DEMUX NON-DES MODE, NON-EXTENDED CONTROL MODE, FSR = $V_A$** | | | | | | | |
| ENOB | Effective number of bits | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 8.1 | 8.9 | | bits |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 7.8 | 8.9 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS, | [4, 5] | 8 | 8.9 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 7.7 | 8.9 | | |
| SINAD | Signal-to-noise plus distortion ratio | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 50.3 | 55.3 | | dB |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 48.5 | 55.3 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 49.8 | 55.3 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 48 | 55.3 | | |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 50.9 | 55.6 | | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 49 | 55.6 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 50.5 | 55.9 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 48.5 | 55.9 | | |
| THD | Total harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | | –67 | –59.5 | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ =–0.5 dBFS | [6] | | –67 | –58.5 | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | | –64.3 | –58.5 | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | | –64.3 | –58 | |
| 2nd Harm | Second harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | | | −75 | | dBc |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = -0.5 dBFS | | | −68 | | |
| 3rd Harm | Third harmonic distortion | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | | | −72 | | dBc |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −68 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 57.5 | 66.7 | | dBc |
| | | $f_{IN}$ = 248 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 53 | 66.7 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [4, 5] | 57.5 | 66.7 | | |
| | | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | [6] | 54.5 | 66.7 | | |

## Converter Electrical Characteristics: Dynamic Converter Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q-channel; duty-cycle stabilizer on.(1)(2)(3)

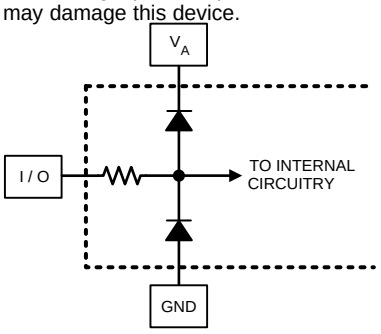
| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **NON-DEMUX NON-DES MODE, NON-EXTENDED CONTROL MODE, FSR = $V_A$** | | | | | | | |
| ENOB | Effective number of bits | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 9 | | bits |
| SINAD | Signal-to-noise plus distortion ratio | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 56.2 | | dB |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 56.7 | | dBc |
| THD | Total harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | -65.7 | | dBc |
| 2nd Harm | Second harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −75 | | dBc |
| 3rd Harm | Third harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −68 | | dBc |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 67.6 | | dBc |
| **1:4 DEMUX DES MODE (Q-CHANNEL ONLY), ECM, OFFSET/GAIN ADJUSTED ENOB EFFECTIVE NUMBER OF BITS FIN = 498 MHZ, $V_{IN}$ = –0.5 DBFS** | | | | | | | |
| ENOB | Effective number of bits | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 8.7 | | bits |
| SINAD | Signal-to-noise plus distortion ratio | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 54.2 | | dB |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 55.3 | | dBc |
| THD | Total harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 60.7 | | dBc |
| 2nd Harm | Second harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −78 | | dBc |
| 3rd Harm | Third harmonic distortion | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | −67 | | dBc |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 498 MHz, $V_{IN}$ = –0.5 dBFS | | | 63.6 | | dBc |

## 6.7 Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN\_FSR}$ | Analog differential input full-scale range | FSR pin Y3 low | [4, 5, 6] | 560 | 630 | 680 | $mV_{P-P}$ |
| | | FSR pin Y3 high | [4, 5, 6] | 750 | 820 | 890 | $mV_{P-P}$ |
| | | **EXTENDED CONTROL MODE** | | | | | |
| | | FM(14:0) = 0000**h** | | | 600 | | $mV_{P-P}$ |
| | | FM(14:0) = 4000**h** (default) | | | 790 | | $mV_{P-P}$ |
| | | FM(14:0) = 7FFF**h** | | | 980 | | $mV_{P-P}$ |
| $C_{IN}$ | Analog input capacitance, Non-DES mode(5)(6) | Differential | | | 0.02 | | pF |
| | | Each input pin to ground | | | 1.6 | | |
| | Analog input capacitance, DES mode(5)(6) | Differential | | | 0.08 | | pF |
| | | Each input pin to ground | | | 2.2 | | |
| $R_{IN}$ | Differential input resistance | | [1, 2, 3] | 100 | 103.5 | 108 | Ω |
| **COMMON-MODE OUTPUT** | | | | | | | |
| $V_{CMO}$ | Common-mode output voltage | $I_{CMO}$ = ±100 µA | [1, 2, 3] | 1.15 | 1.25 | 1.35 | V |
| $TC\_V_{CMO}$ | Common-mode output voltage temperature coefficient | $I_{CMO}$ = ±100 µA | | | 38 | | ppm/°C |
| $V_{CMO\_LVL}$ | $V_{CMO}$ input threshold to set DC-coupling mode | | | | 0.63 | | V |
| $C_L\_V_{CMO}$ | Maximum $V_{CMO}$ load capacitance | See(6) | | | | 80 | pF |
| **BANDGAP REFERENCE** | | | | | | | |
| $V_{BG}$ | Bandgap reference output voltage | $I_{BG}$ = ±100 µA | [1, 2, 3] | 1.15 | 1.25 | 1.35 | V |
| $TC\_V_{BG}$ | Bandgap reference voltage temperature coefficient | $I_{BG}$ = ±100 µA | | | 50 | | ppm/°C |
| $C_{LOAD}$ $V_{BG}$ | Maximum bandgap reference load capacitance | | | | 80 | | pF |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



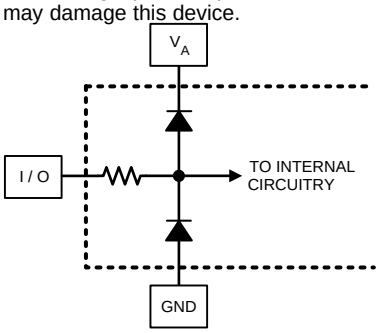

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J$ = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(5) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22 pF differential and 1.06 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(6) This parameter is ensured by design and/or characterization and is not tested in production.

## 6.8 Converter Electrical Characteristics: Channel-to-Channel Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Offset match | | | 2 | | LSB |
| | Positive full-scale match | Zero offset selected in control register | | 2 | | LSB |
| | Negative full-scale match | Zero offset selected in control register | | 2 | | LSB |
| | Phase matching (I, Q) | $f_{IN} = 1$ GHz | | < 1 | | Degree |
| X-TALK Q-channel | Crosstalk from I channel (aggressor) to Q-channel (victim) | Aggressor = 498 MHz F.S.<br>Victim = 100 MHz F.S. | | −61 | | dB |
| X-TALK I channel | Crosstalk from Q-channel (aggressor) to I channel (victim) | Aggressor = 498 MHz F.S.<br>Victim = 100 MHz F.S. | | −61 | | dB |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



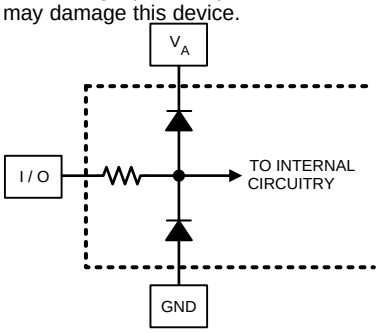

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

## 6.9 Converter Electrical Characteristics: LVDS CLK Input Characteristics

The following specifications apply after calibration for $V_A$ = $V_{DR}$ = $V_{TC}$ = V = 1.9 V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L$ = 10 pF; differential AC-coupled sine wave input clock, $f_{CLK}$ = 1 GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN\_CLK}$ | Differential clock input level | Sine wave clock | [1, 2, 3] | 0.4 | 0.6 | 2 | $V_{P-P}$ |
| | | Square wave clock | [1, 2, 3] | 0.4 | 0.6 | 2 | |
| $C_{IN\_CLK}$ | Sampling clock input capacitance(5)(6) | Differential | | | 0.1 | | pF |
| | | Each input to ground | | | 1 | | |
| $R_{IN\_CLK}$ | Sampling clock input resistance | | | | 100 | | Ω |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



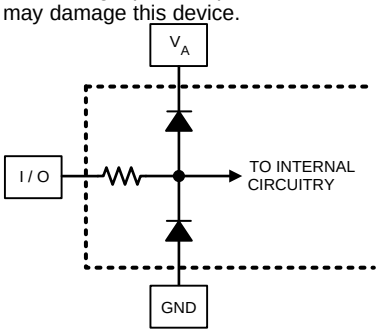

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J$ = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(5) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22-pF differential and 1.06 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(6) This parameter is ensured by design and/or characterization and is not tested in production.

## 6.10 Electrical Characteristics: AutoSync Feature

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN\_RCLK}$ | Differential RCLK input level | Differential peak-to-peak | | | 360 | | $mV_{P-P}$ |
| $C_{IN\_RCLK}$ | RCLK input capacitance | Differential | | | 0.1 | | pF |
| | | Each input to ground | | | 1 | | |
| $R_{IN\_RCLK}$ | RCLK differential input resistance | | | | 100 | | Ω |
| $I_{IH\_RCLK}$ | Input leakage current | $V_{IN} = V_A$ | [1, 2, 3] | –6 | | 6 | µA |
| $I_{IL\_RCLK}$ | Input leakage current | $V_{IN}$ = GND | [1, 2, 3] | –6 | | 6 | µA |
| $V_{O\_RCOUT}$ | Differential RCOut output voltage | | | | 360 | | mV |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



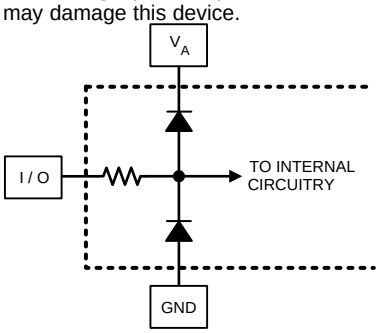

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

## 6.11 Converter Electrical Characteristics: Digital Control and Output Pin Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DIGITAL CONTROL PINS (DES, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$— unless otherwise specified)** | | | | | | | |
| $V_{IH}$ | Logic high input voltage | | [1, 2, 3] | 0.7 × $V_A$ | | | V |
| $V_{IL}$ | Logic low input voltage | | [1, 2, 3] | | | 0.3 × $V_A$ | V |
| $I_{IH}$ | Input leakage current | $V_{IN} = V_A$ | [1, 2, 3] | –6 | | –0.1 | µA |
| $I_{IL}$ | Input leakage current (DES, CAL, TPM, FSR, DDRPh) | $V_{IN}$ = GND | [1, 2, 3] | –6 | | –0.1 | µA |
| | Input leakage current (SCLK, SDI, $\overline{SCS}$) | | [1, 2, 3] | –33 | | –18 | µA |
| | Input leakage current (PDI, PDQ, $\overline{ECE}$,) | | [1, 2, 3] | –66 | | –36 | µA |
| $C_{IN\_DIG}$ | Input capacitance(5)(6) | Each input to ground | | | 1.5 | | pF |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.




(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

## Converter Electrical Characteristics: Digital Control and Output Pin Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

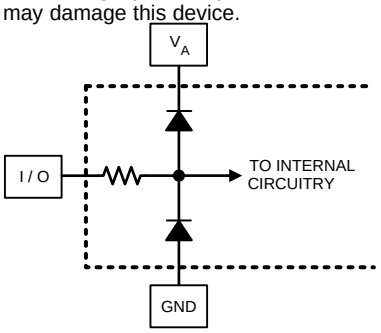
| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LVDS OUTPUT PINS (DATA, DCLKI, DCLKQ, ORI, ORQ)** | | | | | | | |
| $V_{OD}$ | LVDS differential output voltage | $V_{BG}$ = Floating, OVS = High | [1, 2, 3] | 300 | 520 | 700 | $mV_{P-P}$ |
| | | $V_{BG}$ = Floating, OVS = Low | | 160 | 374 | 540 | |
| | | $V_{BG} = V_A$, OVS = High | | 340 | 568 | 760 | |
| | | $V_{BG} = V_A$, OVS = Low | | 190 | 400 | 600 | |
| $\Delta V_{O\ DIFF}$ | Change in LVDS output swing between logic levels | | | | ±1 | | mV |
| $V_{OS}$ | Output offset voltage | $V_{BG}$ = Floating | | | 0.8 | | V |
| | | $V_{BG} = V_A$ | | | 1.2 | | V |
| $\Delta V_{OS}$ | Change in output offset voltage between logic levels | | | | ±1 | | mV |
| $I_{OS}$ | Output short-circuit current | $V_{BG}$ = Floating; D+ and D− connected to 0.8 V | | | ±3.8 | | mA |
| $Z_O$ | Differential output impedance | | | | 100 | | Ω |
| **DIFFERENTIAL DCLK RESET PINS (DCLK_RST)** | | | | | | | |
| $V_{CMI\_DRST}$ | DCLK_RST common mode input voltage | | | | 1.25 ± 0.15 | | V |
| $V_{ID\_DRST}$ | Differential DCLK_RST input voltage | | | | 0.6 | | $V_{P-P}$ |
| $R_{IN\_DRST}$ | Differential DCLK_RST input resistance(5) | | | | 100 | | Ω |
| **DIGITAL OUTPUT PINS (CalRun, SDO)** | | | | | | | |
| $V_{OH}$ | Logic high output level | CalRun, SDO $I_{OH}$ = –400 µA | [1, 2, 3] | 1.5 | 1.65 | | V |
| $V_{OL}$ | Logic low output level | CalRun, SDO $I_{OH}$ = 400 µA | [1, 2, 3] | | 0.15 | 0.3 | V |

## 6.12 Converter Electrical Characteristics: Power Supply Characteristics (1:2 Demux Mode)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_A$ | Analog supply current | PDI = PDQ = Low | | | 890 | | mA |
| | | PDI = Low; PDQ = High | | | 505 | | mA |
| | | PDI = High; PDQ = Low | | | 505 | | mA |
| | | PDI = PDQ = High | | | 2 | | mA |
| $I_{TC}$ | Track-and-hold and clock supply current | PDI = PDQ = Low | | | 358 | | mA |
| | | PDI = Low; PDQ = High | | | 220 | | mA |
| | | PDI = High; PDQ = Low | | | 220 | | mA |
| | | PDI = PDQ = High | | | 1 | | mA |
| $I_{DR}$ | Output driver supply current | PDI = PDQ = Low | | | 210 | | mA |
| | | PDI = Low; PDQ = High | | | 111 | | mA |
| | | PDI = High; PDQ = Low | | | 111 | | mA |
| | | PDI = PDQ = High | | | 10 | | µA |
| $I_E$ | Digital encoder supply current | PDI = PDQ = Low | | | 60 | | mA |
| | | PDI = Low; PDQ = High | | | 30.5 | | mA |
| | | PDI = High; PDQ = Low | | | 30.5 | | mA |
| | | PDI = PDQ = High | | | 10 | | µA |
| $P_C$ | Power consumption | PDI = PDQ = Low | [1, 2, 3] | | 2.9 | 3.22 | W |
| | | PDI = Low; PDQ = High | | | 1.64 | 1.88 | W |
| | | PDI = High; PDQ = Low | | | 1.64 | 1.88 | W |
| | | PDI = PDQ = High | | | 6 | | mW |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



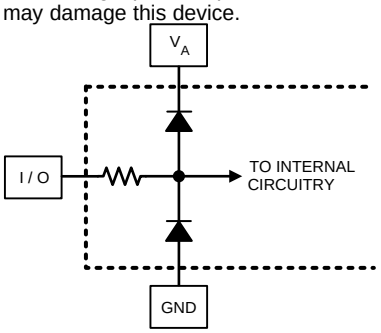

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

## 6.13 Converter Electrical Characteristics: AC Electrical Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **INPUT CLOCK (CLK)** | | | | | | | |
| $f_{CLK\ (max)}$ | Maximum input clock frequency | | [9, 10, 11] | | | 1 | GHz |
| $f_{CLK\ (min)}$ | Minimum input clock frequency | Non-DES mode | [9, 10, 11] | 200 | | | MHz |
| | | DES mode | [9, 10, 11] | | 250 | | |
| | Input clock duty cycle | $f_{CLK\ (min)} \le f_{CLK} \le f_{CLK\ (max)}$ | | 20 | 50 | 80 | % |
| $t_{CL}$ | Input clock low time | | | 200 | 500 | | ps |
| $t_{CH}$ | Input clock high time | | | 200 | 500 | | ps |
| | DCLK duty cycle | | | | 50 | | % |
| | | | | | 50 | | % |
| **DCLK_RST** | | | | | | | |
| $t_{SR}$ | Setup time DCLK_RST± | | | | 45 | | ps |
| $t_{HR}$ | Hold time DCLK_RST± | | | | 45 | | ps |
| $t_{PWR}$ | Pulse Width DCLK_RST± | | | | 5 | | Input Clock Cycles |
| **DATA CLOCK (DCLKI, DCLKQ)** | | | | | | | |
| $t_{SYNC\_DLY}$ | DCLK synchronization delay | 90° mode | | | 4 | | Input Clock Cycles |
| | | 0° mode | | | 5 | | |
| $t_{LHT}$ | Differential low-to-high transition time | 10% to 90%, $C_L = 2.5$ pF | | | 220 | | ps |
| $t_{HLT}$ | Differential high-to-low transition time | 10% to 90%, $C_L = 2.5$ pF | | | 220 | | ps |
| $t_{SU}$ | Data-to-DCLK set-up time | DDR mode, 90° DCLK | | | 850 | | ps |
| $t_H$ | DCLK-to-data hold time | DDR mode, 90° DCLK | | | 850 | | ps |
| $t_{OSK}$ | DCLK-to-data output skew | 50% of DCLK transition to 50% of data transition | | | ±75 | | ps |
| | DCLK duty cycle | | | | 50 | | % |
| | | | | | 50 | | % |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.




(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).

## Converter Electrical Characteristics: AC Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{DR} = V_{TC} = V = 1.9$ V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L = 10$ pF; differential AC-coupled sine wave input clock, $f_{CLK} = 1$ GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | TYP(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DATA INPUT-TO-OUTPUT** | | | | | | | |
| $t_{AD}$ | Sampling (aperture) delay | Input CLK+ fall to acquisition of data | | | 1.1 | | ns |
| $t_{AJ}$ | Aperture jitter | | | | 0.2 | | ps (rms) |
| $t_{OD}$ | Input clock-to data output delay (in addition to $t_{LAT}$) | 50% of input clock transition to 50% of data transition | | | 2.4 | | ns |
| $t_{LAT}$ | Latency in 1:2 demux non-DES mode(5) | DI, DQ outputs | [4, 5, 6] | 34 | | 34 | Input Clock Cycles |
| | | DId, DQd outputs | | 35 | | 35 | |
| | Latency in 1:4 demux DES mode(5) | DI outputs | [4, 5, 6] | 34 | | 34 | Input Clock Cycles |
| | | DQ outputs | | 34.5 | | 34.5 | |
| | | DId outputs | | 35 | | 35 | |
| | | DQd Outputs | | 35.5 | | 35.5 | |
| | Latency in non-demux non-DES mode(5) | DI outputs | [4, 5, 6] | 34 | | 34 | Input Clock Cycles |
| | | DQ outputs | | 34 | | 34 | |
| | Latency in non-demux DES mode(5) | DI outputs | [4, 5, 6] | 34 | | 34 | Input Clock Cycles |
| | | DQ outputs | | 34.5 | | 34.5 | |
| $t_{ORR}$ | Over-range recovery time | Differential $V_{IN}$ step from ±1.2 V to 0 V to get accurate conversion | | | 1 | | Input Clock Cycle |
| $t_{WU}$ | PD low-to-rated accuracy conversion (wake-up time) | Non-DES mode | | | 500 | | ns |
| | | DES mode | | | 1 | | µs |

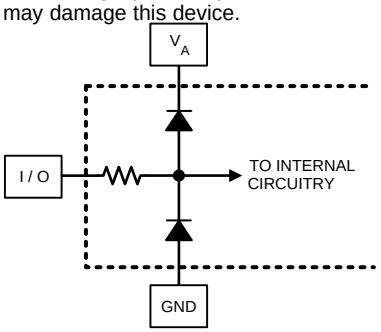
(5) This parameter is ensured by design and/or characterization and is not tested in production.

## 6.14 Timing Requirements: Serial Port Interface

over operating free-air temperature range (unless otherwise noted)
The following specifications apply after calibration for $V_A$ = $V_{DR}$ = $V_{TC}$ = V = 1.9 V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L$ = 10 pF; differential AC-coupled sine wave input clock, $f_{CLK}$ = 1 GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | NOM(4) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{SCLK}$ | Serial clock frequency | See(5) | | | 15 | | MHz |
| | Serial clock low time | | [9, 10, 11] | 30 | | | ns |
| | Serial clock high time | | [9, 10, 11] | 30 | | | ns |
| $t_{SSU}$ | Serial data-to-serial clock rising setup time | See(5) | | | 2.5 | | ns |
| $t_{SH}$ | Serial data-to-serial clock rising hold time | See(5) | | | 1 | | ns |
| $t_{SCS}$ | $\overline{SCS}$-to-serial clock rising setup time | | | | 2.5 | | ns |
| $t_{HCS}$ | $\overline{SCS}$-to-serial clock falling hold time | | | | 1.5 | | ns |
| $t_{BSU}$ | Bus turnaround time | | | | 10 | | ns |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



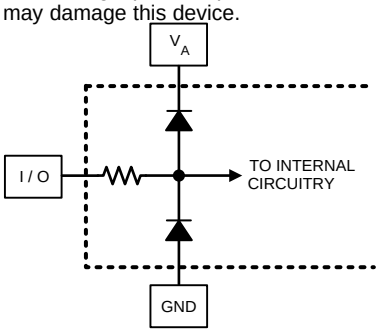

(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) Typical figures are at $T_J$ = 25°C, and represent most likely parametric norms. Test limits are ensured to Texas Instrument's average outgoing quality level (AOQL).
(5) This parameter is ensured by design and/or characterization and is not tested in production.

## 6.15 Timing Requirements: Calibration

over operating free-air temperature range (unless otherwise noted)
The following specifications apply after calibration for $V_A$ = $V_{DR}$ = $V_{TC}$ = V = 1.9 V; I-channel and Q-channel AC-coupled, FSR pin = high; $C_L$ = 10 pF; differential AC-coupled sine wave input clock, $f_{CLK}$ = 1 GHz at 0.5 $V_{P-P}$ with 50% duty cycle; $V_{BG}$ = floating; non-extended control mode; Rext = Rtrim = 3300 Ω ±0.1%; analog signal source impedance = 100-Ω differential; 1:2 demultiplex non-DES mode; I channel and Q channel; duty-cycle stabilizer on.(1)(2)(3)

| PARAMETER | | TEST CONDITIONS | SUB-GROUPS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{CAL}$ | Calibration cycle time | Non-ECM | | | | $2.4 \times 10^7$ | Clock Cycles |
| | | ECM CSS = 0b | | | | $2.3 \times 10^7$ | |
| | | ECM; CSS = 1b | | | | | |
| | | CMS(1:0) = 00b | | | | $0.8 \times 10^7$ | Clock Cycles |
| | | CMS(1:0) = 01b | | | | $1.5 \times 10^7$ | |
| | | CMS(1:0) = 10b (ECM default) | | | | $2.4 \times 10^7$ | |
| $t_{CAL\_L}$ | CAL pin low time | See(4) | [9, 10,11] | 1280 | | | Clock Cycles |
| $t_{CAL\_H}$ | CAL pin high time | See(4) | [9, 10, 11] | 1280 | | | Clock Cycles |

(1) The analog inputs are protected as shown in the following graphic. Input voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.




(2) To ensure accuracy, it is required that $V_A$, $V_{TC}$, $V_E$ and $V_{DR}$ be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.
(3) The maximum clock frequency for non-demux mode is 1 GHz.
(4) This parameter is ensured by design and/or characterization and is not tested in production.

## 6.16 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

| SUBGROUP | DESCRIPTION | TEMPERATURE (°C) |
|---|---|---|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | –55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | –55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | –55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | –55 |
| 12 | Setting time at | 25 |
| 13 | Setting time at | 125 |
| 14 | Setting time at | –55 |

## 6.17 Timing Diagrams

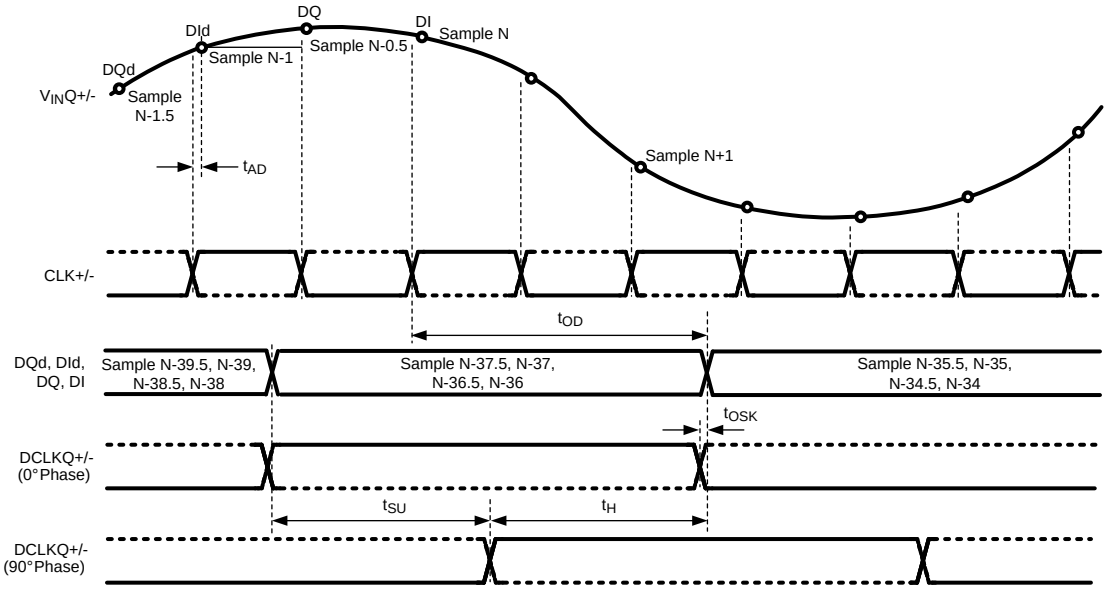



**Figure 1. Clocking in 1:4 Demux DES Mode**

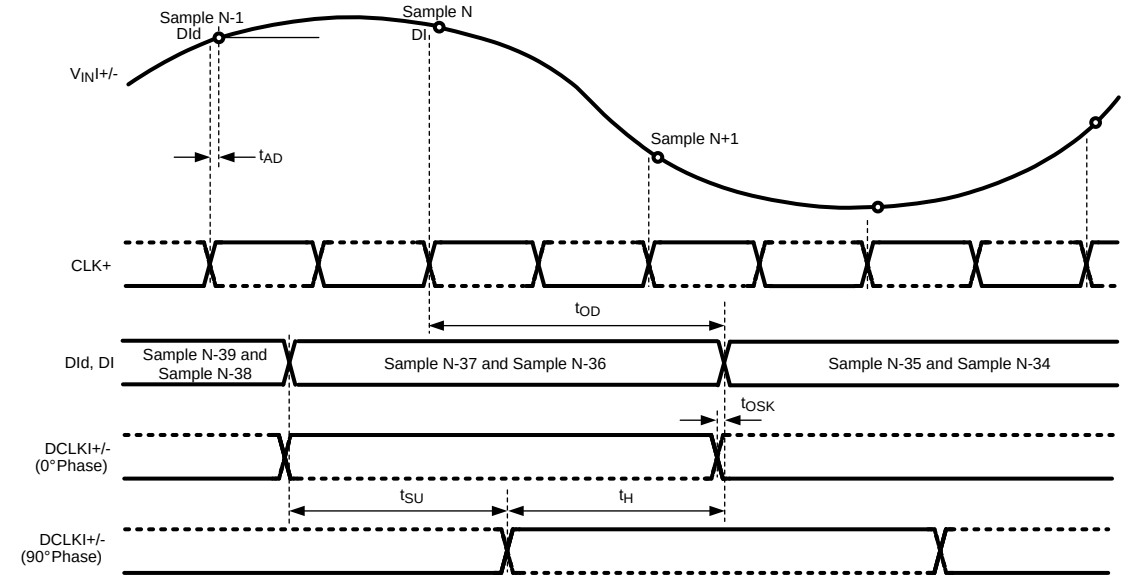



**Figure 2. Clocking in 1:2 Demux Non-DES Mode***

* The timing here is shown for the I channel only. However, the Q channel functions precisely the same as the I channel, with VinQ+, VinQ–, DCLKQ+, DCLKQ–, DQd and DQ instead of VinI+, VinI–, DCLKI+, DCLKI–, DId and DI. Both the I channel and the Q channel use the same CLK+, CLK–.

## Timing Diagrams (continued)

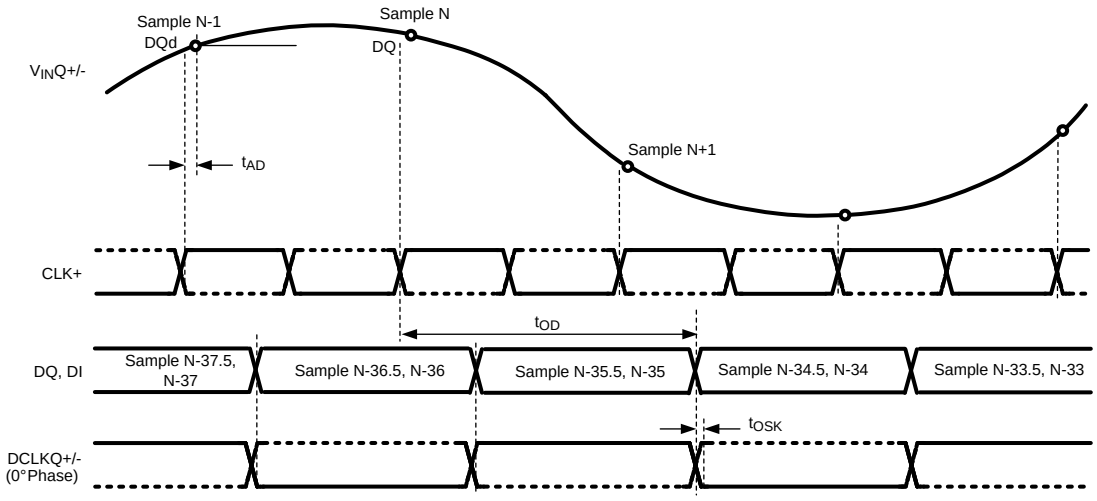



**Figure 3. Clocking in Non-Demux Mode Non-DES Mode****

** The timing here is shown for the Q channel only. However, for the non-demux non-DES node, either the I channel and the Q channel may be used as input. For this case, the I-channel functions precisely the same as those of the Q channel, with VinI+, VinI–, DCLKI+, DCLKI–, and DI instead of VinQ+, VinQ–, DCLKQ+, DCLKQ–, and DQ. Both the I channel and Q channel use the same CLK+, CLK–.

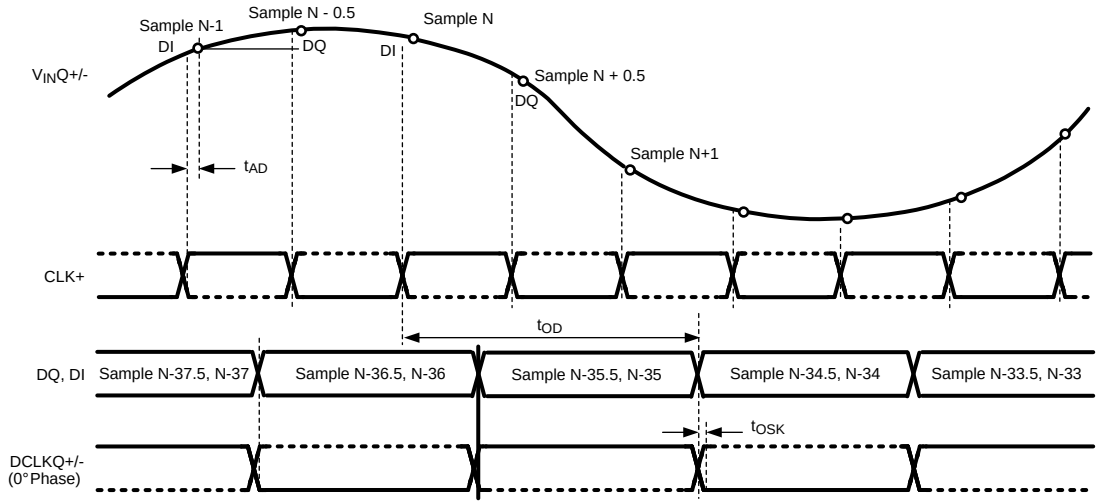



**Figure 4. Clocking in Non-Demux Mode DES Mode**

## Timing Diagrams (continued)

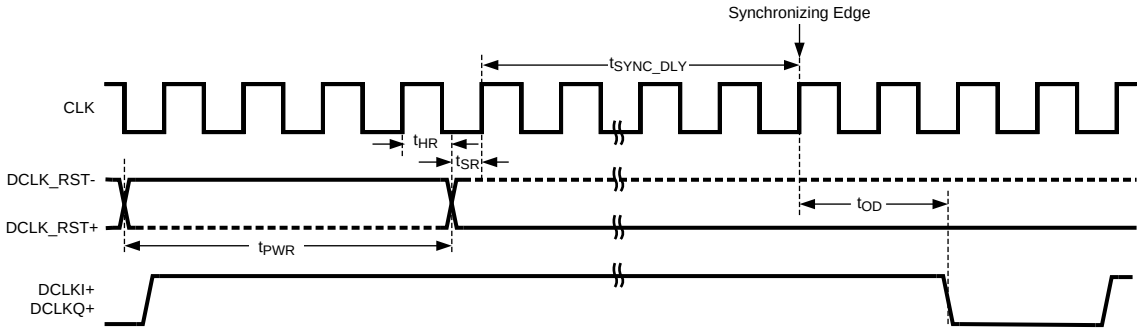



**Figure 5. Data Clock Reset Timing**

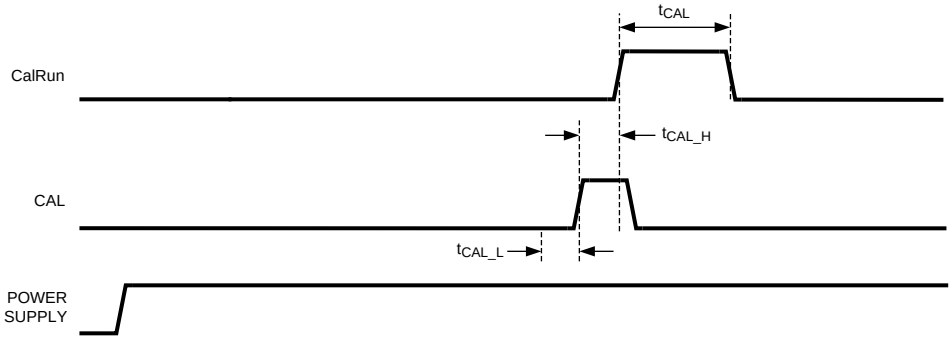



**Figure 6. On-Command Calibration Timing**

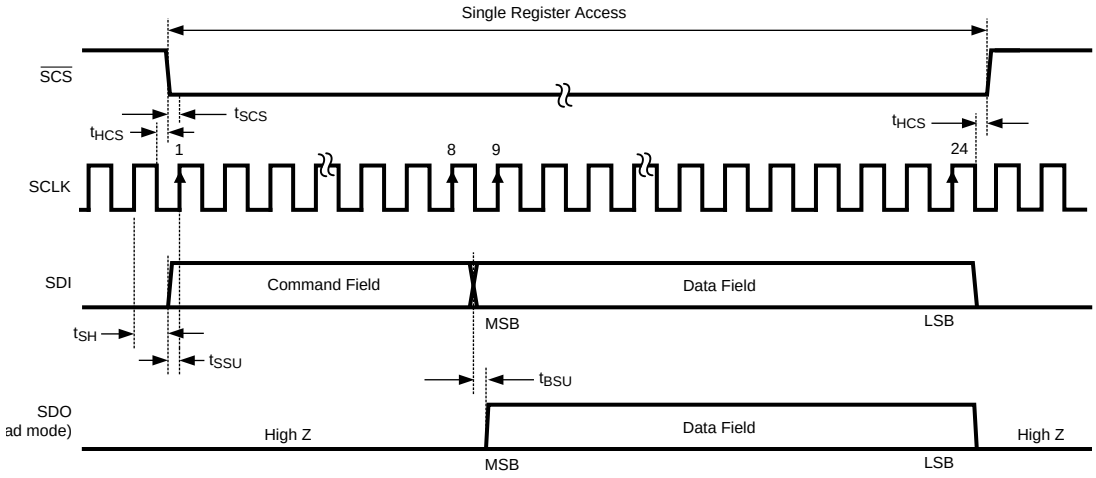



**Figure 7. Serial Interface Timing**

## 6.18 Typical Characteristics

$V_A = V_{DR} = V_{TC} = V_E = 1.9$ V, $f_{CLK} = 1000$ MHz, $f_{IN} = 498$ MHz, $T_A = 25°C$, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C = 325$ MHz and Notch width = 25 MHz.

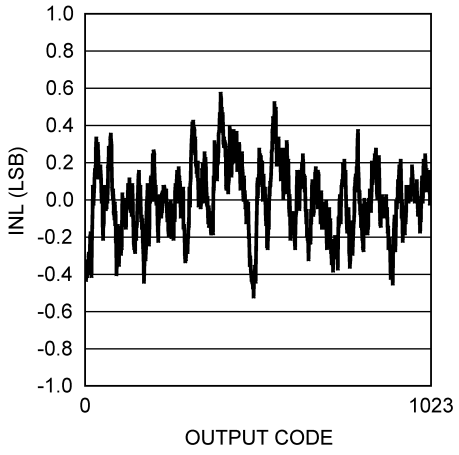



**Figure 8. INL vs Code**

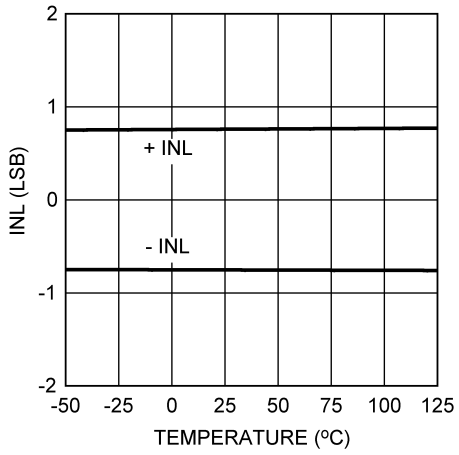



**Figure 9. INL vs Temperature**

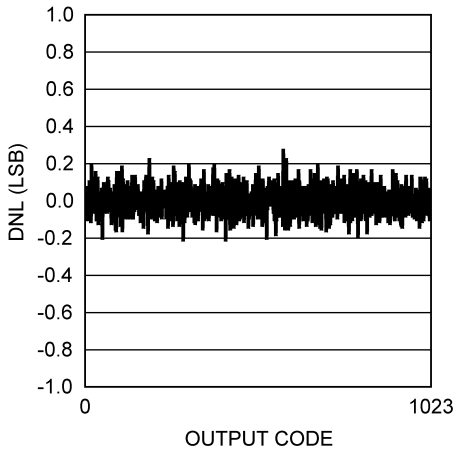



**Figure 10. DNL vs Code**

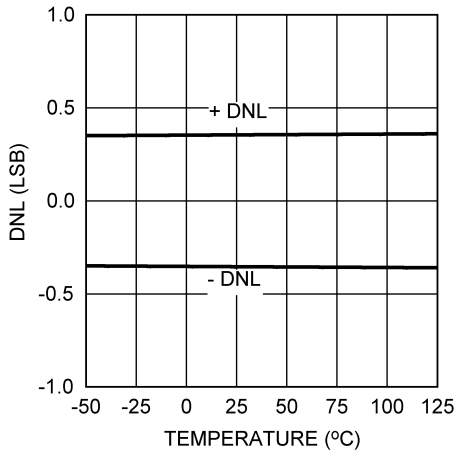



**Figure 11. DNL vs Temperature**

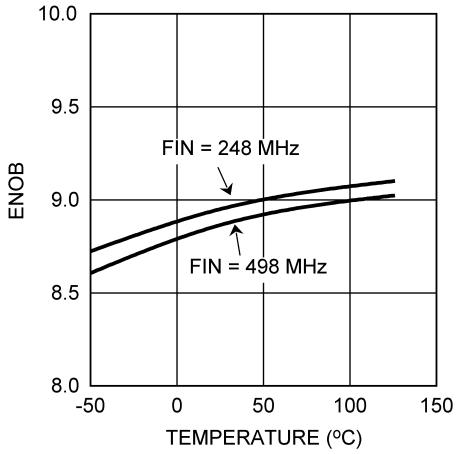



**Figure 12. ENOB vs Temperature**

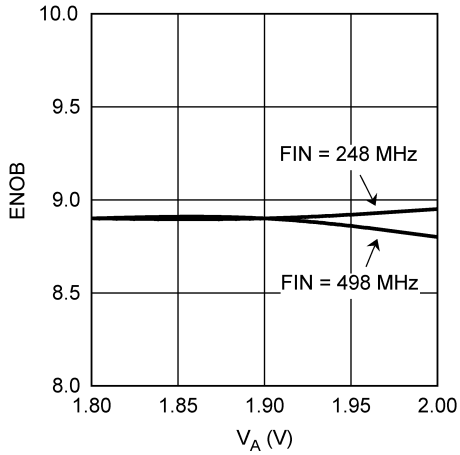



**Figure 13. ENOB vs Supply Voltage**

## Typical Characteristics (continued)

$V_A = V_{DR} = V_{TC} = V_E = 1.9$ V, $f_{CLK} = 1000$ MHz, $f_{IN} = 498$ MHz, $T_A = 25°C$, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C = 325$ MHz and Notch width = 25 MHz.

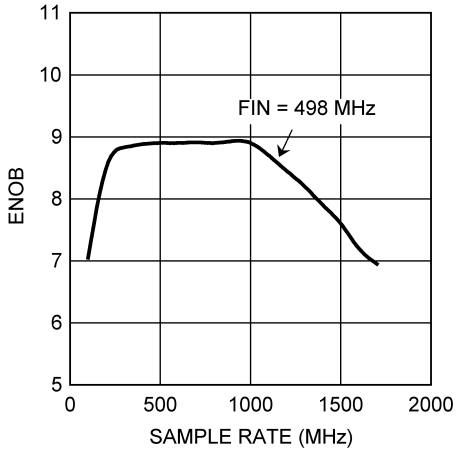



**Figure 14. ENOB vs Clock Frequency**

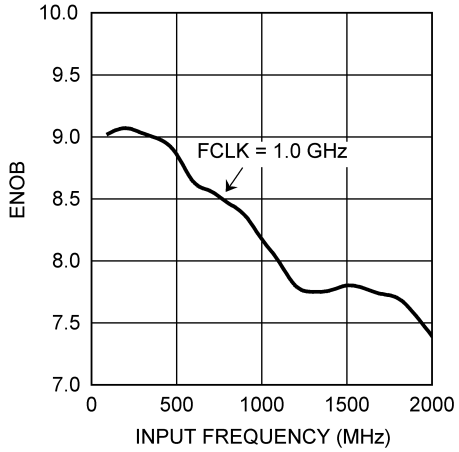



**Figure 15. ENOB vs Input Frequency**

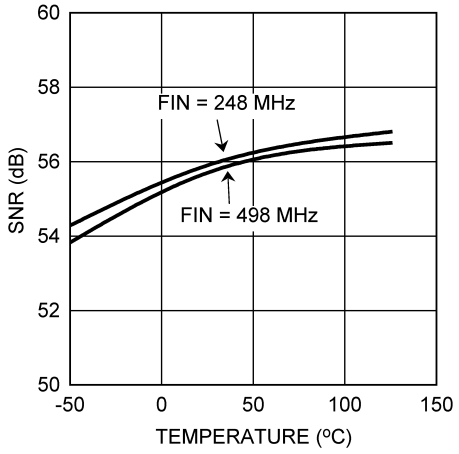



**Figure 16. SNR vs Temperature**

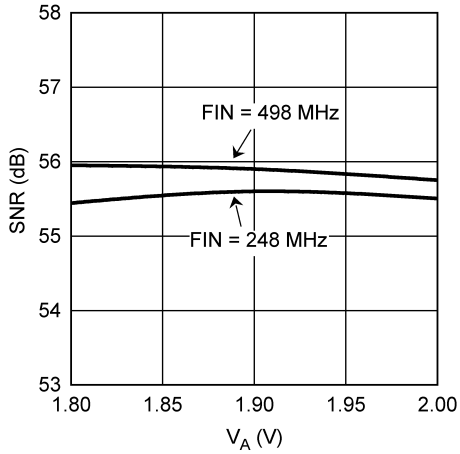



**Figure 17. SNR vs Supply Voltage**

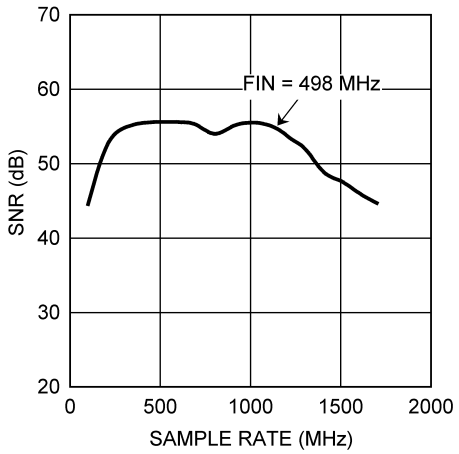



**Figure 18. SNR vs Clock Frequency**

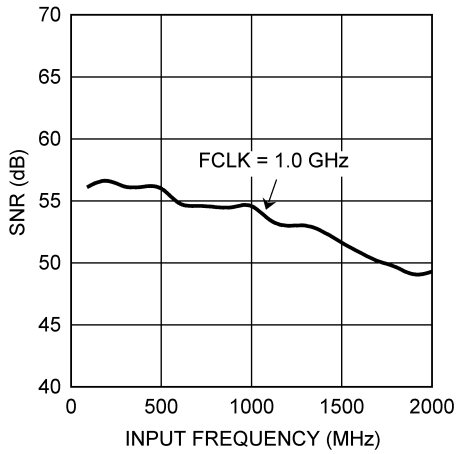



**Figure 19. SNR vs Input Frequency**

## Typical Characteristics (continued)

$V_A$ = $V_{DR}$ = $V_{TC}$ = $V_E$ = 1.9 V, $f_{CLK}$ = 1000 MHz, $f_{IN}$ = 498 MHz, $T_A$= 25°C, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C$ = 325 MHz and Notch width = 25 MHz.

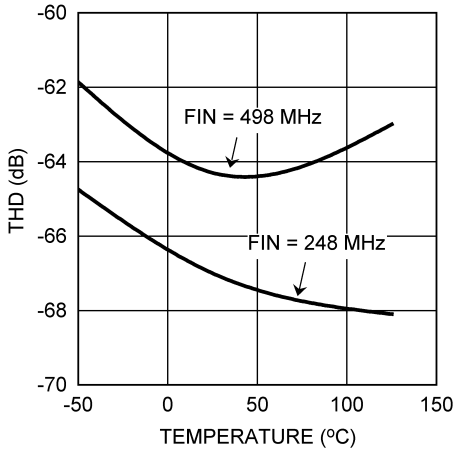



**Figure 20. THD vs Temperature**

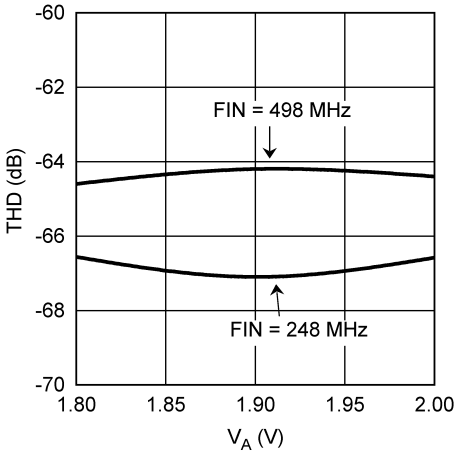



**Figure 21. THD vs Supply Voltage**

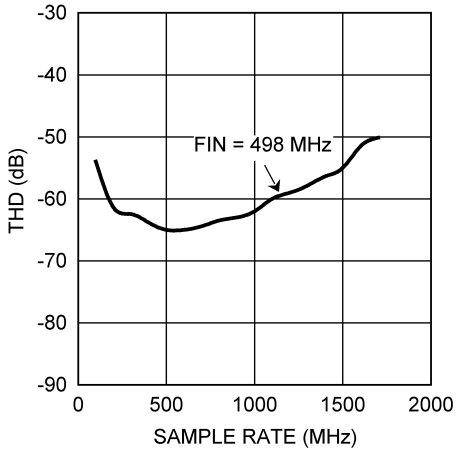



**Figure 22. THD vs Clock Frequency**

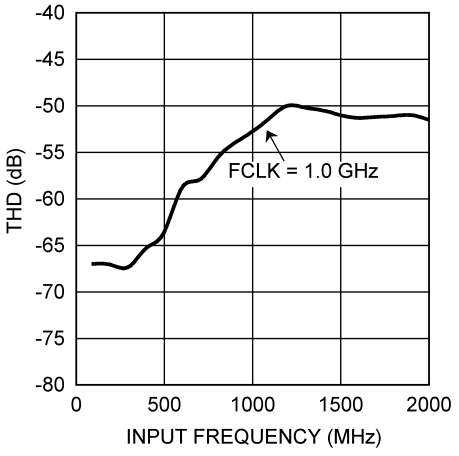



**Figure 23. THD vs Input Frequency**

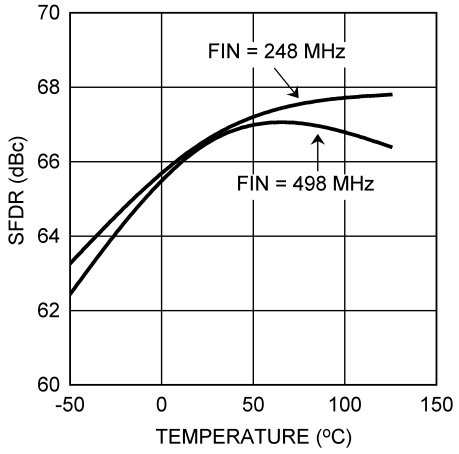



**Figure 24. SFDR vs Temperature**

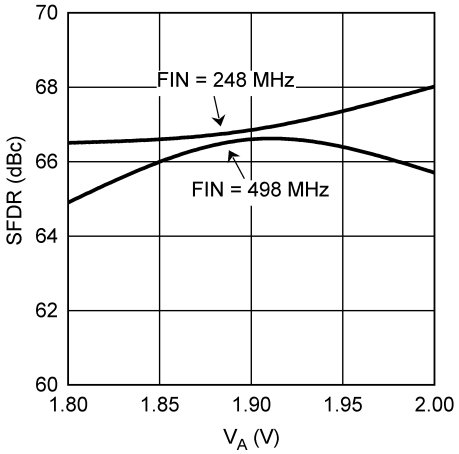



**Figure 25. SFDR vs Supply Voltage**

## Typical Characteristics (continued)

$V_A = V_{DR} = V_{TC} = V_E = 1.9$ V, $f_{CLK} = 1000$ MHz, $f_{IN} = 498$ MHz, $T_A = 25°C$, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C = 325$ MHz and Notch width = 25 MHz.

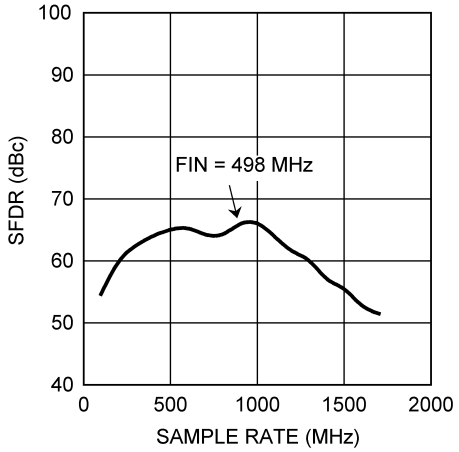



**Figure 26. SFDR vs Clock Frequency**

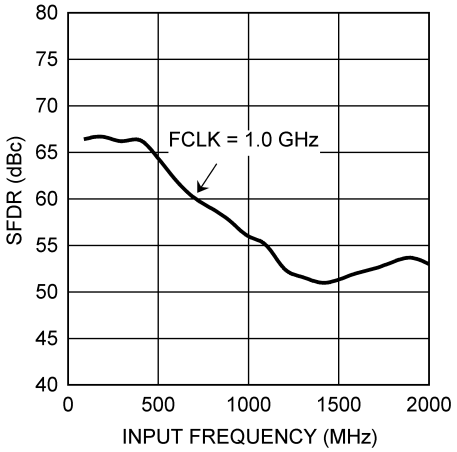



**Figure 27. SFDR vs Input Frequency**

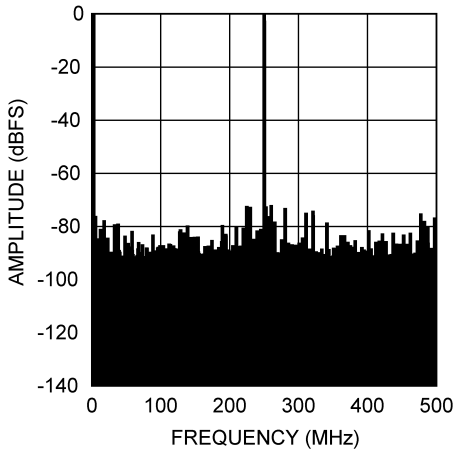



**Figure 28. Spectral Response at FIN = 248 MHz**

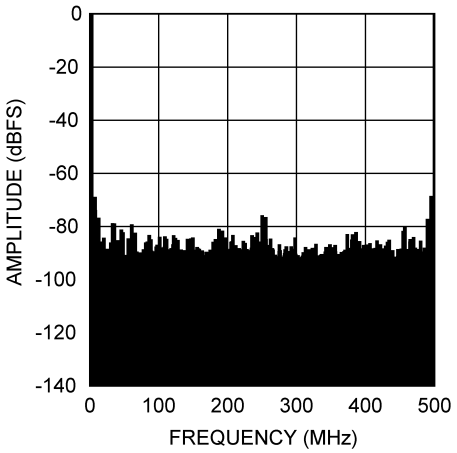



**Figure 29. Spectral Response at FIN = 498 MHz**

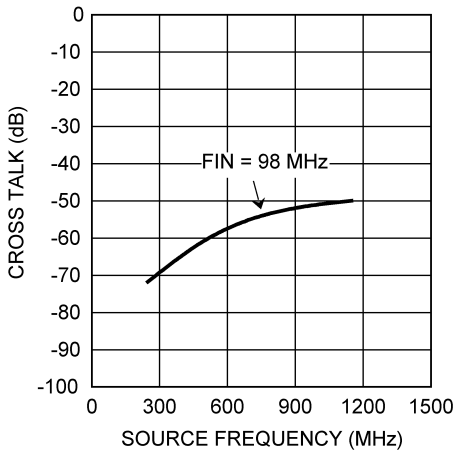



**Figure 30. Crosstalk vs Source Frequency**

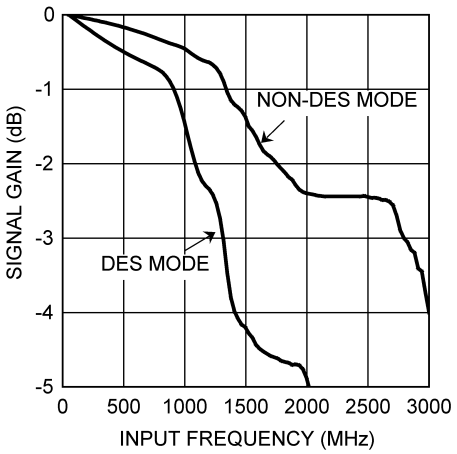



**Figure 31. Full Power Bandwidth**

## Typical Characteristics (continued)

$V_A$ = $V_{DR}$ = $V_{TC}$ = $V_E$ = 1.9 V, $f_{CLK}$ = 1000 MHz, $f_{IN}$ = 498 MHz, $T_A$= 25°C, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C$ = 325 MHz and Notch width = 25 MHz.

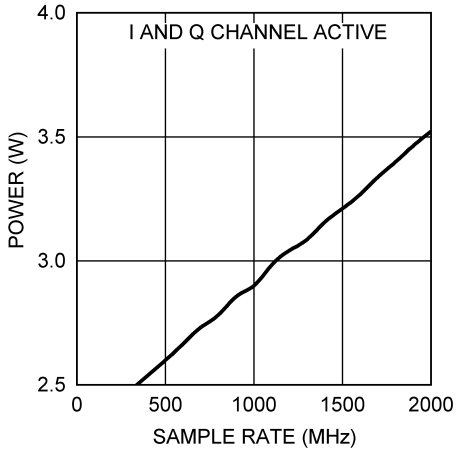



**Figure 32. Power Consumption vs Clock Frequency**

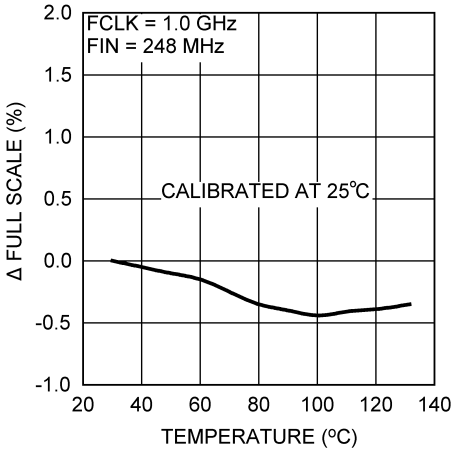



**Figure 33. Gain vs Temperature FS Percent Change**

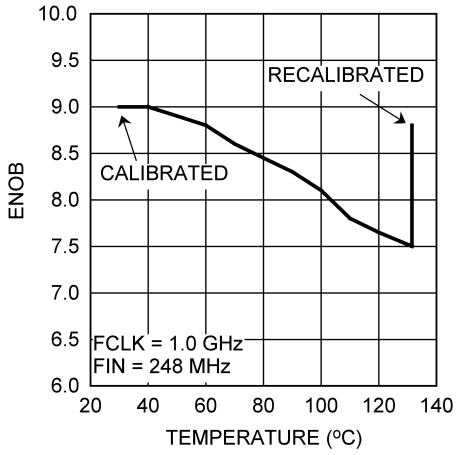



**Figure 34. Gain vs Temperature ENOB**

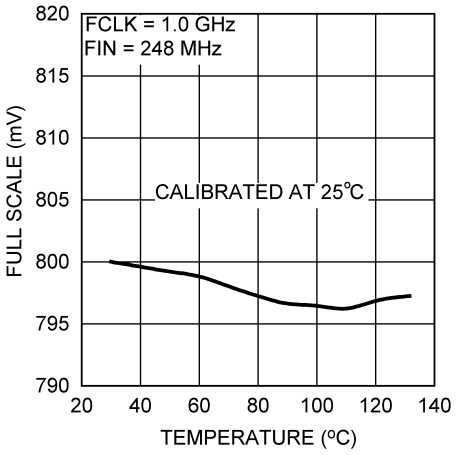



**Figure 35. Gain vs Temperature FS**

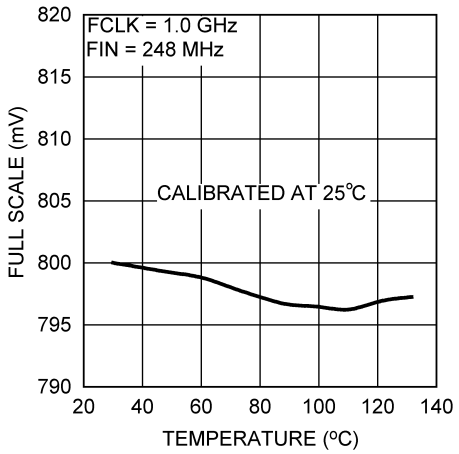



**Figure 36. NPR vs $f_C$ Notch**

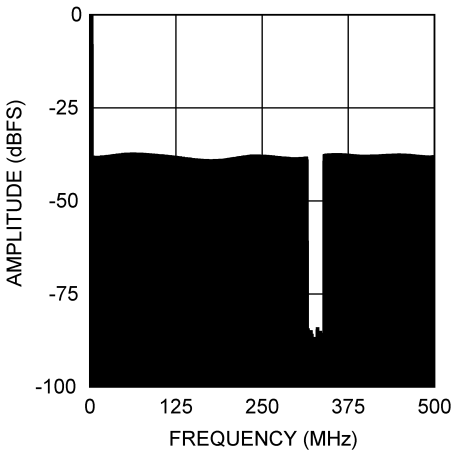



**Figure 37. Amplitude vs Frequency**

## Typical Characteristics (continued)

$V_A$ = $V_{DR}$ = $V_{TC}$ = $V_E$ = 1.9 V, $f_{CLK}$ = 1000 MHz, $f_{IN}$ = 498 MHz, $T_A$= 25°C, I channel and Q channel, unused channel terminated to AC ground and 1:2 demux non-DES mode (1:1 demux mode has similar performance), unless otherwise stated. NPR plots Notch $f_C$ = 325 MHz and Notch width = 25 MHz.

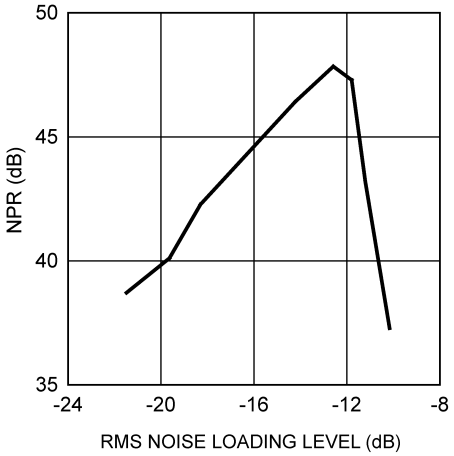



**Figure 38. NPR vs RMS Noise Loading Level**

# 7 Detailed Description

## 7.1 Overview

The ADC10D1000 is a versatile analog-to-digital converter with an innovative architecture permitting very high-speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in *Application and Implementation*. This section covers an overview and the control modes: extended control mode (ECM) and non extended control mode (non-ECM).

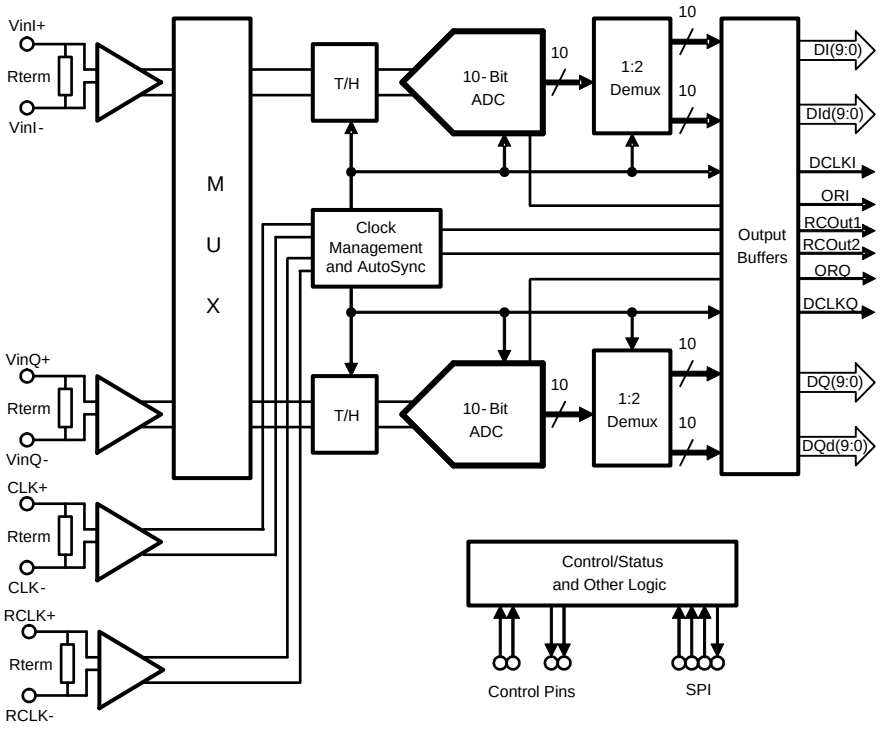
The ADC10D1000 uses a calibrated folding and interpolating architecture that achieves a high 9.0 effective number of bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high-performance, low-power converter. The calibration registers are radiation hard and are not upset by a heavy ion strike up to 120 MeV-cm$^2$/mg.

The analog input signal (which is within the input voltage range of the converter) is digitized to ten bits at speeds of 200 MHz to 1300 MHz, typical. Differential input voltages below negative full-scale cause the output word to consist of all zeroes. Differential input voltages above positive full-scale cause the output word to consist of all ones. Either of these conditions at the I- or Q-input causes the out-of-range I-channel or Q-channel output (ORI or ORQ), respectively, to output a logic-high signal.

The device may be operated in one of two control modes: ECM or non-ECM. In non-ECM, the features of the device may be accessed via simple pin control. In ECM, an expanded feature set is available via the serial interface. Important new features include AutoSync for multi-chip synchronization, programmable 15-bit input full-scale range and independent programmable 12-bit plus sign offset adjustment.

Each channel has a selectable output demultiplexer, which feeds two LVDS buses. If the 1:2 demux mode is selected, the output data rate is reduced to half the input sample rate on each bus. When non-demux mode is selected, the output data rate on each channel is at the same rate as the input sample clock and only one 10-bit bus per channel is active.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Features

The ADC10D1000 offers many features to make the device convenient to use in a wide variety of applications. Table 1 is a summary of the features available, as well as details for the control mode chosen.

**Table 1. Features and Modes**

| FEATURE | NON-ECM | CONTROL PIN ACTIVE IN ECM | ECM | DEFAULT ECM STATE |
|---|---|---|---|---|
| **INPUT CONTROL AND ADJUST** | | | | |
| Input full-scale adjust setting | Selected via FSR (pin Y3) | No | Selected via the Configuration Register (Addr: 3**h** and B**h**) | mid FSR value |
| Input offset adjust setting | Not available | Not applicable | Selected via the Configuration Register (Addr: 2**h** and A**h**) | Offset = 0 mV |
| LC filter on Clock | Not available | Not applicable | Selected via the Configuration Register (Addr: D**h**) | LC filter off |
| Sampling clock phase adjust | Not available | Not applicable | Selected via the Configuration Register (Addr: C**h** and D**h**) | Phase adjust disable |
| DES/Non-DES mode selection | Not available | No | Selected via DES bit (Addr: C**h** and D**h** | Non-DES mode |
| $V_{CMO}$ adjust | Not available | Not applicable | Selected via the Configuration Register (Addr: 1**h**) | $V_{CMO}$ |

## Feature Description (continued)

**Table 1. Features and Modes (continued)**

| FEATURE | NON-ECM | CONTROL PIN ACTIVE IN ECM | ECM | DEFAULT ECM STATE |
|---|---|---|---|---|
| **OUTPUT CONTROL AND ADJUST** | | | | |
| DDR clock phase selection | Selected via DDRPh (pin W4) | No | Selected via DPS in the Configuration Register (Addr: 0**h**; Bit: 14) | 0° mode |
| LVDS differential output voltage amplitude selection | Higher amplitude only | Not applicable | Selected via OVS in the Configuration Register (Addr: 0**h**; Bit: 13) | Higher amplitude |
| LVDS common-mode output voltage amplitude selection | Selected via $V_{BG}$ (pin B1) | Yes | Not available | Higher amplitude |
| Output formatting selection | Offset binary only | Not applicable | Selected via 2SC in the Configuration Register (Addr: 0**h**; Bit: 4) | Offset binary |
| Test pattern mode at output | Selected via TPM (pin A4) | No | Selected via TPM in the Configuration Register (Addr: 0**h**; Bit: 12) | TPM not active |
| Demux/non-demux mode selection | Selected via NDM (pin A5) | Yes | Not available | N/A |
| AutoSync | Not available | Not applicable | Selected via the Configuration Register (Addr: E**h**) | Master mode, RCOut1/2 disabled |
| DCLK RST | Not available | Not applicable | Select via the Config Reg (Addr: E**h**) | DLCK reset disabled |
| **CALIBRATION** | | | | |
| On-command calibration event | Selected via CAL (pin D6) | Yes | Selected via CAL in the Configuration Register (Addr: 0**h**; Bit: 15) | N/A (CAL = 0) |
| **POWER-DOWN** | | | | |
| Power down I channel | Selected via PDI (pin U3) | Yes | Selected via PDI in the Configuration Register (Addr: 0**h**; Bit: 11) | I channel operational |
| Power down Q channel | Selected via PDQ (pin V3) | Yes | Selected via PDQ in theConfiguration Register (Addr: 0**h**; Bit: 10) | Q channel operational |

### *7.3.1.1 Input Control and Adjust*

There are several features and configurations for the input of the ADC10D1000. This section covers input full-scale range adjust, input offset adjust, DES/non-DES modes, sampling clock phase adjust, and LC filter on the sampling clock.

#### 7.3.1.1.1 AC- and DC-Coupled Modes

The analog inputs may be AC- or DC-coupled. See *AC-DC-Coupled Mode Pin ($V_{CMO}$)* for information on how to select the desired mode; see *DC-Coupled Input Signals* and *AC-Coupled Input Signals* for applications information.

#### 7.3.1.1.2 Input Full-Scale Range Adjust

The input full-scale range for the ADC10D1000 may be adjusted via non-ECM or ECM. In non-ECM, a control pin selects a higher or lower value; see *Full-Scale Input Range Pin (FSR)*. In ECM, the input full-scale range may be selected with 15 bits of precision; see $V_{IN\_FSR}$ in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*, for details. Note that the higher and lower full-scale input range settings in non-ECM do not correspond to the maximum and minimum full-scale input range settings in ECM. It is necessary to execute a manual calibration following any change of the input full-scale range. See *Register Maps* for information about the registers.

#### 7.3.1.1.3 Input Offset Adjust

The input offset adjust for the ADC10D1000 may be adjusted with 12 bits of precision plus sign via ECM. See *Register Maps* for information about the registers.

#### 7.3.1.1.4 DES/Non-DES Mode

The ADC10D1000 is available in dual-edge sampling (DES) or non-DES mode. The DES mode allows for the device Q-channel input to be sampled by the ADCs of both channels. One ADC samples the input on the rising edge of the input clock and the other ADC samples the same input on the falling edge of the input clock. A single input is thus sampled twice per input clock cycle, resulting in an overall sample rate of twice the input clock frequency, for example, 2 GSPS with a 1-GHz input clock. See for information on how to select the desired mode.

For the DES mode, only the Q channel may be used for the input. This may be selected in ECM by using the DES bit (Addr: 0**h**, Bit 7) to select the DES mode and the DESQ bit (Addr: 0**h**, Bit: 6) to select the Q channel as input.

In this mode, the outputs must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 Demux DES mode, the data is effectively demultiplexed by 1:4. If the input clock is 1 GHz, the effective sampling rate is doubled to 2 GSPS, and each of the 4 output buses has an output rate of 500 MHz. All data is available in parallel. To properly reconstruct the sampled waveform, the four words of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI. See Figure 1. If the device is programmed into the non-demux DES mode, two bytes of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI. See Figure 4.

The performance of the ADC10D1000 in DES mode depends on how well the two channels are interleaved; that is, that the clock samples each channel with precisely a 50% duty cycle, each channel has the same offset (nominally code 511/512), and each channel has the same full-scale range. The ADC10D1000 also includes an automatic clock phase background adjustment in DES mode to automatically and continuously adjust the clock phase of the I and Q channels. This feature removes the need to adjust the clock phase setting manually and provides optimal performance in the DES mode. A difference exists in the typical offset between the I and Q channels, which can be removed via the offset adjust feature in ECM to optimize DES mode performance. To adjust the I- and Q-channel offset, measure a histogram of the digital data and adjust the offset via the control register until the histogram is centered at code 511/512. Similarly, the full-scale range of each channel may be adjusted for optimal performance.

#### 7.3.1.1.5 Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature is intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or simplify complex system functions such as beam steering for phase array antennas. A clock-jitter cleaner is available only when the CLK phase adjust feature is used. This adjustment delays all clocks, including the DCLKs and output data, and the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in the system before relying on it.

#### 7.3.1.1.6 LC Filter-On Input Clock

An LC bandpass filter is available on the ADC10D1000 sampling clock to clean jitter on the incoming clock. This feature is available when the CLK phase adjust is also used. This feature was designed to minimize the dynamic performance degradation resulting from additional clock jitter as much as possible. This feature is available in ECM via the LC filter (LCF) bits in the Control Register (Addr: D**h**, Bits 7:0).

If the clock phase adjust feature is enabled, the sampling clock passes through additional gate delay, which adds jitter to the clock signal; the LCF helps to remove this additional jitter, so it is only available when the clock phase adjust feature is also enabled. To enable both features, use SA (Addr: D**h**, Bit 8). The LCF bits are thermometer encoded and may be used to set a filter center frequency ranging from 0.8 GHz to 1.5 GHz; see Table 2.

**Table 2. LC Filter Code vs $F_C$**

| LCF(7:0) | LCF(7:0) | $f_C$ (GHz) |
|---|---|---|
| 0 | 0000 0000**b** | 1.5 |
| 1 | 0000 0001**b** | 1.4 |
| 2 | 0000 0011**b** | 1.3 |
| 3 | 0000 0111**b** | 1.2 |
| 4 | 0000 1111**b** | 1.1 |
| 5 | 0001 1111**b** | 1 |
| 6 | 0011 1111**b** | 0.92 |
| 7 | 0111 1111**b** | 0.85 |
| 8 | 1111 1111**b** | 0.8 |

The LC filter is a second-order bandpass filter, which has the following simulated bandwidth for a center frequency, $f_c$ at 1 GHz (see Table 3).

**Table 3. LC Filter Bandwidth at 1 GHz**

| BANDWIDTH [dB] | BANDWIDTH [MHz] |
|---|---|
| –3 | ±135 |
| –6 | ±235 |
| –9 | ±360 |
| –12 | ±525 |

#### 7.3.1.1.7 $V_{CMO}$ Adjust

The $V_{CMO}$ of the ADC10D1000QML is generated as a buffered version of the internal bandgap reference; see *AC-DC-Coupled Mode Pin ($V_{CMO}$)*. This pin provides an output voltage, which is the optimal common-mode voltage for the input signal and should be used to set the common-mode voltage of the driving buffer. However, in order to accommodate larger signals at the analog inputs, the $V_{CMO}$ may be adjusted to a lower value. From its typical default value, the $V_{CMO}$ may be lowered by approximately 200 mV via the VCA(2:0) bits of the Control Register (Addr: 1**h**; Bits: 7:5) in ECM. See *Register Definitions* for more information. Adjusting the $V_{CMO}$ away from its optimal value also degrades the dynamic performance; see $V_{CMO}$ in *Recommended Operating Conditions*.

### *7.3.1.2 Output Control and Adjust*

There are several features and configurations for the output of the ADC10D1000 so that it may be used in many different applications. This section covers DDR clock phase, LVDS output differential and common-mode voltage, output formatting, Demux/Non-Demux Mode, and test pattern mode.

#### 7.3.1.2.1 DDR Clock Phase

The ADC10D1000 output data is always delivered in double data rate (DDR). With DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK; see Figure 39. The DCLK-to-data phase relationship may be either 0° or 90°. For 0° mode, the data transitions on each edge of the DCLK. Any offset from this timing is $t_{OSK}$; see *Converter Electrical Characteristics: AC Electrical Characteristics* for details. For 90° mode, the DCLK transitions in the middle of each data cell. Setup and hold times for this transition, $t_{SU}$ and $t_H$, may also be found in *Converter Electrical Characteristics: AC Electrical Characteristics*. The DCLK-to-data phase relationship may be selected via the DDRPh Pin in Non-ECM (see *Dual Data-Rate Phase Pin (DDRPh)*) or the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14) in ECM.

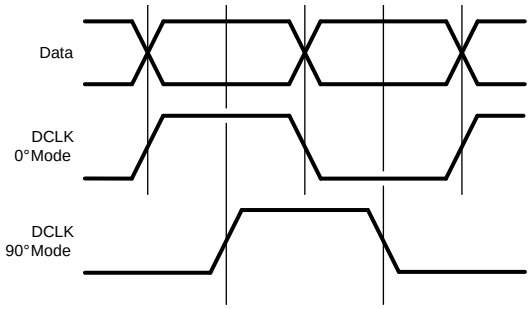



**Figure 39. DDR DCLK-to-Data Phase Relationship**

#### 7.3.1.2.2 LVDS Output Differential Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output differential voltage. This parameter is $V_{OD}$ and may be found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. The desired voltage may be selected via OVS Bit (Addr: 0**h**, Bit 13); see *Register Maps* for more information. In non-extended control mode only higher $V_{OD}$ is available.

#### 7.3.1.2.3 LVDS Output Common-Mode Voltage

The ADC10D1000 is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is $V_{OS}$ and may be found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. See *LVDS Output Common-Mode Pin ($V_{BG}$)* for information on how to select the desired voltage.

#### 7.3.1.2.4 Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The desired formatting is set via the 2SC bit of the Control Register (Addr: 0**h**; Bit: 4) in ECM; see *Register Maps* for more information.

#### 7.3.1.2.5 Demux/Non-Demux Mode

The ADC10D1000 may be in one of two demultiplex modes: demux mode or non-demux mode (also sometimes referred to as 1:1 demux mode). In non-demux mode, the data from the input is simply output at the sampling rate at which it was sampled on one 10-bit bus. In demux mode, the data from the input is output at half the sampling rate, on twice the number of buses (see *Functional Block Diagram*). Demux or non-demux mode may only be selected by the NDM pin; see *Non-Demultiplexed Mode Pin (NDM)*. In non-DES mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 demux non-DES mode). In DES mode, the output data from both channels interleaved may be demultiplexed (1:4 demux DES mode) or not demultiplexed (non-demux DES mode).

#### 7.3.1.2.6 Test Pattern Mode

The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In test-pattern mode, the ADC is disengaged, and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES mode or non-DES mode. Each port is given a unique 10-bit word, alternating between 1's and 0's. When the device is programmed into the demux mode, the order of the test pattern is as described in Table 4.

**Table 4. Test Pattern By Output Port In 1:2 Demux Mode**

| TIME | Qd | Id | Q | I | ORQ | ORI | COMMENTS |
|---|---|---|---|---|---|---|---|
| T0 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | Pattern sequence **n** |
| T1 | 3FF**h** | 3FE**h** | 3FD**h** | 3FB**h** | 1**b** | 1**b** | |
| T2 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | |
| T3 | 3FF**h** | 3FE**h** | 3FD**h** | 3FB**h** | 1**b** | 1**b** | |
| T4 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | |
| T5 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | Pattern sequence **n+1** |
| T6 | 3FF**h** | 3FE**h** | 3FD**h** | 3FB**h** | 1**b** | 1**b** | |
| T7 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | |
| T8 | 3FF**h** | 3FE**h** | 3FD**h** | 3FB**h** | 1**b** | 1**b** | |
| T9 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | |
| T10 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | Pattern sequence **n+2** |
| T11 | 3FF**h** | 3FE**h** | 3FD**h** | 3FB**h** | 1**b** | 1**b** | |
| T12 | 000**h** | 001**h** | 002**h** | 004**h** | 0**b** | 0**b** | |
| T13 | ... | ... | ... | ... | ... | ... | |

When the device is programmed into the non-demux mode, the order of the test pattern is as described in Table 5.

**Table 5. Test Pattern By Output Port In Non-Demux Mode**

| TIME | I | Q | ORI | ORQ | COMMENTS |
|---|---|---|---|---|---|
| T0 | 001**h** | 000**h** | 0**b** | 0**b** | Pattern sequence **n** |
| T1 | 001**h** | 000**h** | 0**b** | 0**b** | |
| T2 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T3 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T4 | 001**h** | 000**h** | 0**b** | 0**b** | |
| T5 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T6 | 001**h** | 000**h** | 0**b** | 0**b** | |
| T7 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T8 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T9 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T10 | 001**h** | 000**h** | 0**b** | 0**b** | Pattern sequence **n+1** |
| T11 | 001**h** | 000**h** | 0**b** | 0**b** | |
| T12 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T13 | 3FE**h** | 3FF**h** | 1**b** | 1**b** | |
| T14 | ... | ... | ... | ... | |

#### 7.3.1.3 Calibration Feature

The ADC10D1000 calibration must be run to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. The DCLK outputs are present during all phases of the calibration process. All data and over-range output bits are held at logic low during calibration. Calibration must be performed in the planned mode of operation. Calibration trims the analog input differential termination resistor, the CLK input resistor, and sets internal bias currents which affects the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, resulting in maximizing the dynamic performance as measured by SNR, THD, SINAD (SNDR), and ENOB.

##### 7.3.1.3.1 Calibration Pins

Table 6 is a summary of the pins used for calibration. See *Pin Configuration and Functions* for complete pin information and Figure 6 for the timing diagram.

**Table 6. Calibration Pins**

| PIN | NAME | FUNCTION |
|---|---|---|
| D6 | CAL<br>(calibration) | Initiate calibration event; see Calibration Pin (CAL) |
| B5 | CalRun<br>(calibration running) | Indicates when calibration is running |
| C1/D2 | Rtrim+, Rtrim–<br>(input termination trim resistor) | External resistor used to calibrate analog and CLK inputs |
| C3/D3 | Rext+, Rext–<br>(external reference resistor) | External resistor used to calibrate internal linearity |

##### 7.3.1.3.2 How to Initiate a Calibration Event

The calibration event must be initiated by holding the CAL pin low for at least $t_{CAL\_L}$ clock cycles, and then holding it high for at least another $t_{CAL\_H}$ clock cycles, as defined in *Timing Requirements: Calibration*. The minimum $t_{CAL\_L}$ and $t_{CAL\_H}$ input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as $t_{CAL}$. In ECM, either the CAL bit (Addr: 0**h**; Bit: 15) or the CAL pin may be used to initiate a calibration event.

##### 7.3.1.3.3 On-Command Calibration

An on-command calibration must be run after power up and whenever the FSR is changed. TI recommends execution of an on-command calibration whenever the settings or conditions to the device are altered significantly, in order to obtain optimal parametric performance. Some examples include: changing the FSR via either ECM or non-ECM, power-cycling either channel, and switching into or out of DES mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, relative to the specific system performance requirements.

Due to the nature of the calibration feature, TI recommends avoiding unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the serial interface or use the DCLK reset feature while calibrating the ADC. Doing so impairs the performance of the device until it is re-calibrated correctly. Also, it is recommended to not apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

##### 7.3.1.3.4 Calibration Adjust

The calibration event itself may be adjusted, for sequence and mode. This feature can be used if a shorter calibration time than the default is required; see $t_{CAL}$ in *Timing Requirements: Calibration*. However, the performance of the device, when using a shorter calibration time than the default setting, is not ensured.

The calibration sequence may be adjusted via CSS (Addr: 4**h**, bit 14). The default setting of CSS = 1**b** executes both $R_{IN}$ and $R_{IN}$_CLK calibration (using Rtrim) and internal linearity calibration (using Rext). Executing a calibration with CSS = 0b executes only the internal linearity calibration. The first time that calibration is executed, it must be with CSS = 1**b** to trim $R_{IN}$ and $R_{IN}$_CLK. However, once the device is at its operating temperature, and $R_{IN}$ has been trimmed at least one time, it does not drift significantly. To save time in subsequent calibrations, trimming $R_{IN}$ and $R_{IN}$_CLK may be skipped — that is, by setting CSS = 0**b**.

The mode may be changed, to save calibration execution time for the internal linearity calibration. See $t_{CAL}$ in *Converter Electrical Characteristics: AC Electrical Characteristics*. Adjusting the CMS(1:0) bits of the Calibration Adjust Register (Addr: 4**h**; Bits: 9:8) selects three different pre-defined calibration times. A longer of time calibrates each channel more closely to the ideal values, but choosing shorter times does not significantly impact the performance. The fourth setting, CMS(1:0) = 11**b**, is not available.

#### 7.3.1.3.5 Calibration and Power Down

If PDI and PDQ are simultaneously asserted during a calibration cycle, the ADC10D1000 immediately powers down. The calibration cycle continues when either or both channels are powered back up, but the calibration is compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration must be executed upon powering the ADC10D1000 back up. In general, the ADC10D1000 must be re-calibrated when either or both channels are powered back up, or after one channel is powered down. For best results, power back up after the device has stabilized to its operating temperature.

#### 7.3.1.3.6 Read/Write Calibration Settings

When the ADC performs a calibration, the calibration constants are stored in an array which is accessible via the Calibration Values Register (Addr: 5h). To save the time that it takes to execute a calibration, $t_{CAL}$, or if re-using a previous calibration result, these values can be read from and written to the register at a later time. For example, if an application requires the same input impedance, $R_{IN}$, this feature can be used to load a previously determined set of values. For the calibration values to be valid, the ADC must be operating under the same conditions, including temperature, at which the calibration values were originally read from the ADC.

To read calibration values from the SPI, do the following:

1. Set ADC to desired operating conditions.
2. Set SSC (Addr: 4h, Bit 7) to 1
3. Read exactly 184 times the Calibration Values Register (Addr: 5h). The register values are R0, R1, R2... R183 where R0 is a dummy value. The contents of R <183:1> must be stored.
4. Set SSC (Addr: 4h, Bit 7) to 0.
5. Continue with normal operation.

To write calibration values to the SPI, do the following:

1. Set ADC to operating conditions at which calibration values were previously read.
2. Set SSC (Addr: 4h, Bit 7) to 1.
3. Write exactly 183 times the Calibration Values Register (Addr: 5h). The registers should be written with stored register values R1, R2... R183.
4. Make two additional dummy writes of 0000h.
5. Set SSC (Addr: 4h, Bit 7) to 0.
6. Continue with normal operation.

### *7.3.1.4 Power Down*

On the ADC10D1000, the I and Q channels may be powered down individually. This may be accomplished via the control pins, PDI and PDQ, or via the PDI and PDQ bits of the Control Register (Addr: 0**h**; Bits: 11:10) in ECM. In ECM, the PDI and PDQ pins are logically OR'd with the Control Register setting. See *Power-Down I-Channel Pin (PDI)* and *Power-Down Q-Channel Pin (PDQ)* for more information.

## 7.3.2 Power-On Reset

The device power-on reset has been disabled to ensure single-effect functional interrupts do not occur during space operation. Therefore, the calibration routine at power-on is not reliable for the space version of the ADC10D1000. This means a manual calibration is always required after the device is power-on and is stable. Specifically, the device must either be in non-ECM or in ECM with the configuration registers reset or written to the correct values, and then a manual calibration must be run before the ADC can be used to digitize data correctly. See *Calibration Feature* for more information on calibration.

## 7.4 Device Functional Modes

### 7.4.1 Control Modes

The ADC10D1000 may be operated in one of two control modes: non-extended control mode (non-ECM) or extended control mode (ECM). In the simpler non-ECM (also sometimes referred to as pin-control mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers.

#### *7.4.1.1 Non-Extended Control Mode*

In non-ECM, the serial interface is not active and all available functions are controlled with various pin settings. Non-ECM is selected by setting $\overline{ECE}$ (pin B3) to logic high. Seven dedicated control pins provide a wide range of control for the ADC10D1000 and facilitate its operation. These control pins provide demux mode selection, DDR phase selection, calibration event initiation, power-down I channel, power-down Q channel, test-pattern mode selection, and full-scale input range selection. In addition to this, a one dual-purpose control pin provides for LVDS output common-mode voltage selection. See Table 7 for a summary.

**Table 7. Non-ECM Pin Summary**

| PIN NAME | LOGIC LOW | LOGIC HIGH | FLOATING |
|---|---|---|---|
| NDM | demux mode | non-demux mode | Not allowed |
| DDRPh | 0° mode | 90° mode | Not allowed |
| CAL | See *Calibration Pin (CAL)* | | Not allowed |
| PDI | I channel active | Power-down I channel | Not allowed |
| PDQ | Q channel active | Power-down Q channel | Not allowed |
| TPM | Non-test pattern mode | Test pattern mode | Not allowed |
| FSR | Lower FS input range | Higher FS input range | Not allowed |
| **DUAL-PURPOSE CONTROL PINS** | | | |
| $V_{CMO}$ | AC-coupled operation | Not allowed | DC-coupled operation |
| $V_{BG}$ | Not allowed | Higher LVDS common-mode voltage | Lower LVDS common-mode voltage |

##### 7.4.1.1.1 Non-Demultiplexed Mode Pin (NDM)

The non-demultiplexed mode (NDM) pin selects whether the ADC10D1000 is in demux mode (logic-low) or non-demux mode (logic-high). In Non-demux mode, the data from the input is produced at the data-rate at a single 10-bit output bus. In demux mode, the data from the input is produced at half the data-rate at twice the number of output buses. For non-des mode, each I or Q channel produces its data on one or two buses for non-demux mode or demux mode, respectively. For DES mode, the Q channel produces its data on two or four buses for non-demux mode or demux mode, respectively.

This feature is pin-controlled only and remains active during both non-ECM and ECM. See Table 7 for more information.

##### 7.4.1.1.2 Dual Data-Rate Phase Pin (DDRPh)

The dual data-rate-phase (DDRPh) pin selects whether the ADC10D1000 is in 0° mode (logic-low) or 90° mode (logic-high). In dual data rate (DDR) mode, the data may transition either with the DCLK transition (0° mode) or halfway between DCLK transitions (90° mode). The data is always in DDR mode on the ADC10D1000. The DDRPh pin selects 0° mode or 90° mode for both the I-channel DI- and DId-to-DCLKI phase relationship and for the Q-channel DQ- and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14). See Table 11 for more information.

#### 7.4.1.1.3 Calibration Pin (CAL)

The calibration pin (CAL) must be used to initiate an on-command calibration event. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration via the CAL pin, bring the CAL pin high for a minimum of $t_{CAL\_H}$ input clock cycles after it has been low for a minimum of $t_{CAL\_L}$ input clock cycles. Hold the CAL pin high when not in use to ensure no undesired calibrating in space environment. In ECM mode this pin remains active and is logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0**h**; Bit: 15). See *Calibration Feature* for more information.

#### 7.4.1.1.4 Power-Down I-Channel Pin (PDI)

The power-down I-channel (PDI) pin selects whether the I channel is powered down (logic-high) or active (logic-low). The digital data output pins (both positive and negative) are put into a high impedance state when the I channel is powered down. Upon return to the active state, the pipeline contains meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I channel powered down or active and may be found in *Converter Electrical Characteristics: Power Supply Characteristics (1:2 Demux Mode)*. It is recommended that the user thoroughly understand how the PDI feature functions in relationship with the Calibration feature and control them appropriately for their application.

This pin remains active in ECM. In ECM, either this pin or the PDI bit (Addr: 0**h**; Bit: 11) in the Control Register may be used to power down the I channel. See *Power Down* for more information.

#### 7.4.1.1.5 Power-Down Q-Channel Pin (PDQ)

The power-down Q-channel (PDQ) pin selects whether the Q- channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q channel. The PDI and PDQ pins function independently of each other to control whether each I channel or Q channel is powered down or active.

This pin remains active in ECM. In ECM, either this pin or the PDQ bit (Addr: 0**h**; Bit: 10) in the Control Register may be used to power-down the I channel. See *Power Down* for more information.

#### 7.4.1.1.6 Test Pattern Mode Pin (TPM)

The test-pattern mode (TPM) pin selects whether the output of the ADC10D1000 is a test pattern (logic-high) or the converted input (logic-low). The ADC10D1000 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In TPM, the ADC is disengaged, and a test pattern generator is connected to the outputs, including ORI and ORQ. See *Test Pattern Mode* for more information.

#### 7.4.1.1.7 Full-Scale Input Range Pin (FSR)

The full-scale input range (FSR) pin selects whether the full-scale input range for both the I channel and Q channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as $V_{IN\_FSR}$ in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*. In non-ECM, the full-scale input range for each I channel and Q channel may not be set independently, but it is possible to do so in ECM. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the Configuration Register (Addr: 3**h** and B**h**). See *Input Control and Adjust* for more information.

#### 7.4.1.1.8 AC-DC-Coupled Mode Pin ($V_{CMO}$)

The $V_{CMO}$ pin serves a dual purpose. When functioning as an output, it provides the optimal common-mode voltage for the DC-coupled analog inputs. When functioning as an input, it selects whether the device is AC-coupled (logic-low) or DC-coupled (floating). This pin is always active, in both ECM and non-ECM.

#### 7.4.1.1.9 LVDS Output Common-Mode Pin ($V_{BG}$)

The $V_{BG}$ pin serves a dual purpose and may either provide the bandgap output voltage or select whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as $V_{OS}$ and may be found in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. This pin is always active, in both ECM and Non-ECM. See *Output Control and Adjust* for more information.

### 7.4.2 Extended Control Mode

In extended control mode (ECM), all available functions are controlled via the serial interface. In addition to this, several of the control pins remain active. See Table 1 for details. ECM is selected by setting $\overline{ECE}$ (pin B3) to logic low.

The space version of the ADC10D1000 does not include a power-on reset. Therefore, when powered up in ECM, the registers are in an unknown, random state. There are two ways to set the ECM registers: toggling the $\overline{ECE}$ pin or writing to the registers. If the device is programmed into non-ECM (by setting $\overline{ECE}$ logic high), the registers are programmed to their default values. Thus, if the $\overline{ECE}$ pin is set to logic high, then set to logic low (ECM), the device will be in ECM, and the registers will have their default values. The second method is to simply explicitly write the default (or otherwise desired) values to the register in ECM; TI recommends the second method.

## 7.5 Programming

Four pins on the ADC10D1000 control the serial interface: $\overline{SCS}$, SCLK, SDI, and SDO. *Serial Interface* covers the serial interface. Also see *Register Maps*.

### 7.5.1 Serial Interface

The ADC10D1000 offers a serial interface that allows access to the sixteen control registers within the device. The serial interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI-type interfaces that are used on many microcontrollers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in their system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in Table 8. See Figure 7 for the timing diagram and *Converter Electrical Characteristics: AC Electrical Characteristics* for timing specification details. Control register contents are retained when the device is put into power-down mode.

**Table 8. Serial Interface Pins**

| PIN | NAME |
|---|---|
| C4 | $\overline{SCS}$ (serial chip select) |
| C5 | SCLK (serial clock) |
| B4 | SDI (serial data in) |
| A3 | SDO (serial data out) |

**$\overline{SCS}$:** Each assertion (logic-low) of this signal starts a new register access; that is, the SDI command field must be ready. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write occurs. If the $\overline{SCS}$ is asserted longer than 24 clocks, data write occurs normally through the SDI input upon the 24th clock, and the SDO output holds the D0 bit until $\overline{SCS}$ is de-asserted. Setup and hold times, $t_{SCS}$ and $t_{HCS}$, with respect to the SCLK must be observed.

**SCLK**: This signal is used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it in the low-state. There is no minimum frequency requirement for SCLK; see $f_{SCLK}$ in *Timing Requirements: Serial Port Interface* for more details.

**SDI:** Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. When in read mode, the data field is high impedance in case the bidirectional SDI/O option is used. Setup and hold times, $t_{SH}$ and $t_{SSU}$, with respect to the SCLK must be observed.

**SDO:** This output is normally tri-stated and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the 8th clock's falling edge. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is tri-stated once again. If an invalid address is accessed, the data sourced consists of all zeroes. Setup and hold times, $t_{SH}$ and $t_{SSU}$, with respect to the SCLK must be observed. If it is a READ operation, there is a bus turnaround time, $t_{BSU}$, from when the last bit of the command field was read in until when the first bit of the data field is written out.

Table 9 shows the Serial Interface bit definitions.

**Table 9. Command and Data Field Definitions**

| BIT NO. | NAMES | COMMENTS |
|---|---|---|

**Table 9. Command and Data Field Definitions (continued)**

| | | |
|---|---|---|
| 1 | Read/Write (R/W) | 1**b** indicates a read operation<br>0**b** indicates a write operation |
| 2-3 | Reserved | Bits must be set to 10**b** |
| 4-7 | A<3:0> | 16 registers may be addressed. The order is MSB first |
| 8 | X | This is a "don't care" bit |
| 9-24 | D<15:0> | Data written to or read from addressed register |

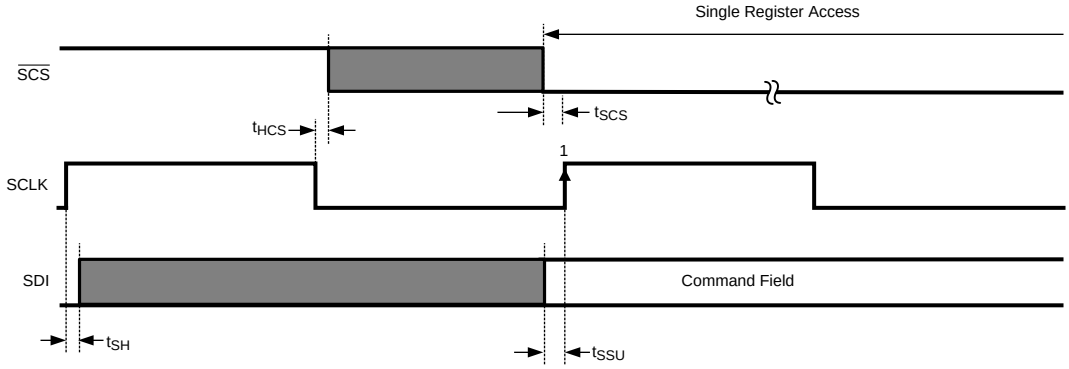



**Figure 40. Serial Interface Timing (Zoom Start)*****

***$\overline{SCS}$ transition from High to Low must occur $t_{HCS}$ after the falling edge of SCLK, and $t_{\overline{SCS}}$ before the rising edge of SCLK.

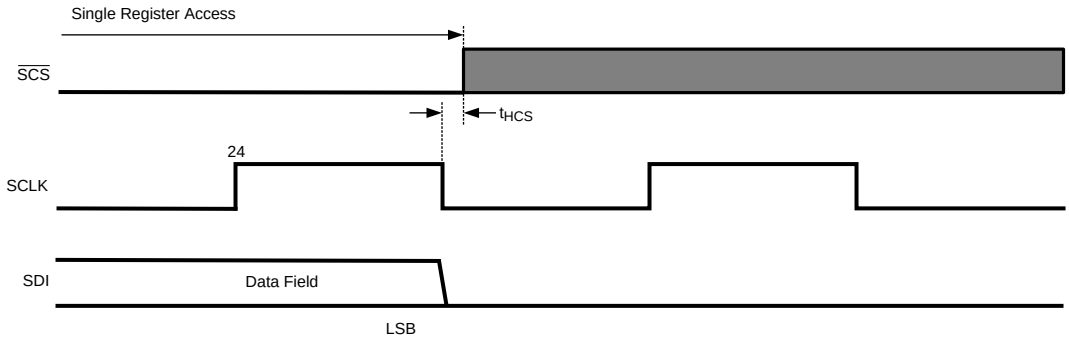



**Figure 41. Serial Interface Timing (Zoom End)******

******$\overline{SCS}$ transition from Low to High must occur $t_{HCS}$ after the 24$^{th}$ SCLK cycle during a low cycle.

The serial data protocol is shown for a read and write operation in Figure 42 and Figure 43, respectively.

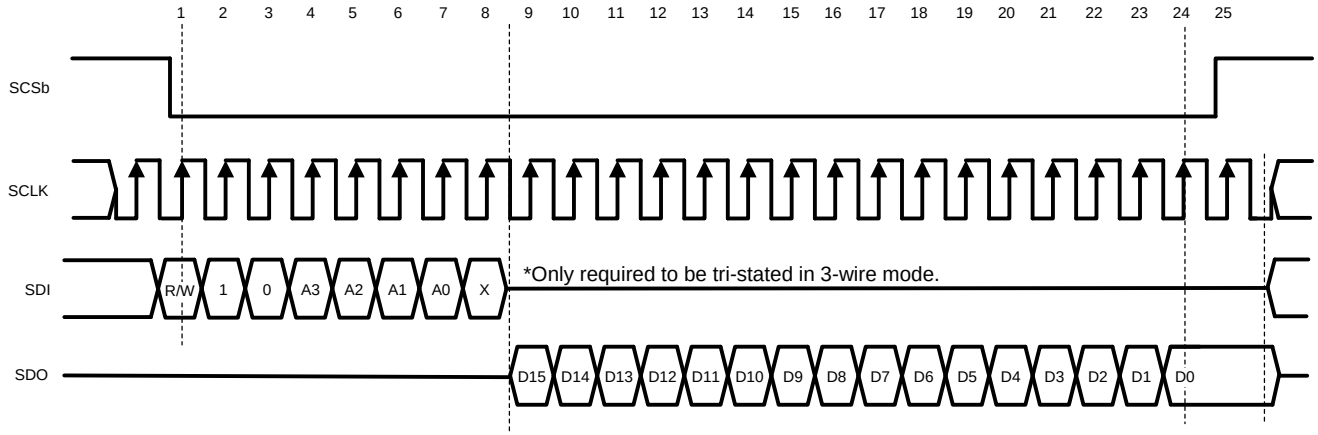



**Figure 42. Serial Data Protocol - Read Operation**

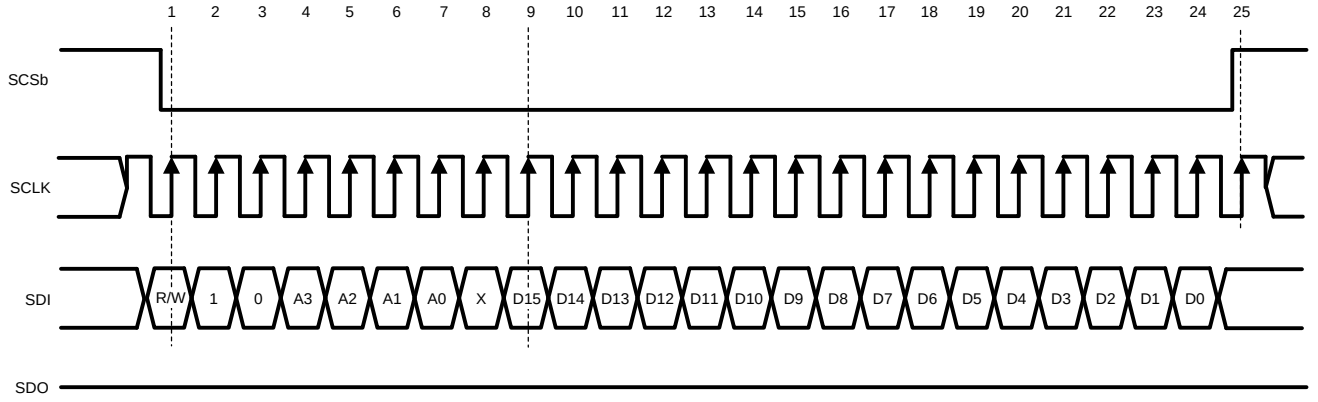



**Figure 43. Serial Data Protocol - Write Operation**

## 7.6 Register Maps

### 7.6.1 Register Definitions

Eight read/write registers provide several control and configuration options in the extended control mode. These registers have no effect when the device is in the non-extended control mode. The ADC10D1000 does not have a power-on reset. The user can write the registers with the desired values, or in extended control mode set ECE**b** Logic high setting resisters to the default values.

**Table 10. Register Addresses**

| A3 | A2 | A1 | A0 | Hex | REGISTER ADDRESSED |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0**h** | Configuration Register 1 |
| 0 | 0 | 0 | 1 | 1**h** | $V_{CMO}$ Adjust |
| 0 | 0 | 1 | 0 | 2**h** | I-channel Offset |
| 0 | 0 | 1 | 1 | 3**h** | I-channel FSR |
| 0 | 1 | 0 | 0 | 4**h** | Res |
| 0 | 1 | 0 | 1 | 5**h** | Res |
| 0 | 1 | 1 | 0 | 6**h** | Res |
| 0 | 1 | 1 | 1 | 7**h** | Res |
| 1 | 0 | 0 | 0 | 8**h** | Res |
| 1 | 0 | 0 | 1 | 9**h** | Res |
| 1 | 0 | 1 | 0 | A**h** | Q-Channel Offset |
| 1 | 0 | 1 | 1 | B**h** | Q-Channel FSR |
| 1 | 1 | 0 | 0 | C**h** | Aperture Delay Coarse Adjust |
| 1 | 1 | 0 | 1 | D**h** | Aperture Delay Fine Adjust and LC Filter Adjust |
| 1 | 1 | 1 | 0 | E**h** | AutoSync |
| 1 | 1 | 1 | 1 | F**h** | Res |

**Table 11. Configuration Register 1**

| Addr: 0**h** (0000**b**) | | | | | | | | | Default Values: 2000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | CAL | DPS | OVS | TPM | PDI | PDQ | Res | LFS | DES | DESQ | Res | 2SC | Res | | | |
| **DV** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bit 15 | CAL: Calibration Enable. When this bit is set to 1**b**, an on-command calibration cycle is initiated. This bit is not reset automatically upon completion of the cal cycle. Therefore, the user must reset this bit to 0**b** and then set it to 1**b** again to initiate another calibration event. This bit is logically OR'd with the CAL pin; both bit and pin must be set to **0b** before either is used to execute a calibration. |
| Bit 14 | DPS: DDR phase select. Set this bit to 0**b** to select the 0° Mode DDR Data-to-DCLK phase relationship and to 1**b** to select the 90° mode. This bit has no effect when the device is in Non-Demux Mode. |
| Bit 13 | OVS: Output Voltage Select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, RCOut1, RCOut2 and DCLK. 0**b** selects the lower level and 1**b** selects the higher level. See $V_{OD}$ in *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics* for details. |
| Bit 12 | TPM: Test Pattern Mode. When this bit is set to 1**b**, the device continually outputs a fixed digital pattern at the digital data and OR outputs. When set to 0**b**, the device continually outputs the converted signal, which was present at the analog inputs. See *Test Pattern Mode* for details about the TPM pattern. |
| Bit 11 | PDI: Power-down I channel. When this bit is set to 0**b**, the I channel is fully operational, but when it is set to 1**b**, the I channel is powered down. The I channel may be powered down via this bit or the PDI pin, which is active, even in ECM. |
| Bit 10 | PDQ: Power-down Q channel. When this bit is set to 0**b**, the Q channel is fully operational, but when it is set to 1**b**, the Q channel is powered down. The Q channel may be powered-down via this bit or the PDQ pin, which is active, even in ECM. |
| Bits 9 | Reserved. Must be set to 0**b**. |
| Bits 8 | LFS: Low Frequency Select. If the sampling Clock (CLK) is at or below 300 MHz, set this bit to 1**b**. |
| Bit 7 | DES: Dual-Edge-Sampling Mode Select. When this bit is set to 0b, the device operates in the non-DES mode; when it is set to 1**b**, the device operates in the DES mode. See DES/Non-DES Mode for more information about DES/non-DES mode. |
| Bit 6 | DESQ: DES Q-channel select. When the device is in DES mode; always set this bit to 1**b** selecting the Q channel. |

| | |
|---|---|
| Bit 5 | Reserved. Must be set to 0**b**. |
| Bit 4 | 2SC: Two's Complement Output. For the default setting of 0**b**, the data is output in offset binary format; when set to 1**b**, the data is output in two's complement format. |
| Bits 3:0 | Reserved. Must be set to 0**b**. |

### Table 12. $V_{CMO}$ Adjust

| Addr: 1**h** (0001**b**) | | | | | | | | | Default values: 2A00**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | VCA(2:0) | | | Reserved | | | | |
| **POR** | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bits 15:8 | Reserved. Must be set as shown. | |
| Bits 7:5 | VCA(2:0): $V_{CMO}$ Adjust. Adjusting from the default VCA(2:0) = 0**d** to VCA(2:0) = 7**d** decreases $V_{CMO}$ from its typical value (see $V_{CMO}$ in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*) to 1.05 V by increments of ~28.6 mV. | |
| | **CODE** | **$V_{CMO}$** |
| | 000 (default) | $V_{CMO}$ |
| | 100 | $V_{CMO}$ – 114 mV |
| | 111 | $V_{CMO}$ – 200 mV |
| Bits 4:0 | Reserved. Must be set as shown. | |

### Table 13. I-Channel Offset Adjust

| Addr: 2**h** (0010**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | OS | OM(11:0) | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bits 15:13 | Reserved. Must be set to 0**b**. | |
| Bit 12 | OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by bits 11:0 to the ADC output. Setting this bit to 1**b** incurs a negative offset of the set magnitude. | |
| Bits 11:0 | OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 μV. Monotonicity is ensured by design only for the 9 MSBs. | |
| | **CODE** | **OFFSET [mV]** |
| | 0000 0000 0000 (default) | 0 |
| | 1000 0000 0000 | 22.5 |
| | 1111 1111 1111 | 45 |

### Table 14. I-Channel Full Scale Range Adjust

| Addr: 3**h** (0011**b**) | | | | | | | | | Default Values: 4000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Res. | FM(14:0) | | | | | | | | | | | | | | |
| **DV** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit 15 | Reserved. Must be set to 0**b**. | |
| Bits 14:0 | FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 630 mV (0**d**) to 980 mV (32767**d**) with the default setting at 820 mV (162384**d**). Monotonicity is ensured by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in EC; that is, FSR values above 820 mV. See *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics* for characterization details. | |
| | **CODE** | **FSR [mV]** |
| | 000 0000 0000 0000 | 630 |
| | 100 0000 0000 0000 (default) | 820 |
| | 111 1111 1111 1111 | 980 |

**Table 15. Calibration Adjust**

| Addr: 4**h** (0100**b**) | | | | | | | | | Default Values: DA7F**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Res | CSS | Reserved | | | | CMS | | Reserved | | | | | | | |
| **DV** | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| Bit 15 | Reserved. Must be set to 1**b**. |
| Bit 14 | CSS: calibration sequence select. The default 1**b** selects the following calibration sequence: reset all previously calibrated elements to nominal values, do $R_{IN}$ calibration, do internal linearity calibration. Setting CSS = 0b selects the following calibration sequence: do not reset $R_{IN}$ to its nominal value, skip $R_{IN}$ calibration, do internal linearity calibration. The calibration must be completed at least one time with CSS = 1**b** to calibrate $R_{IN}$. Subsequent calibrations may be run with CSS = 0**b** (skip $R_{IN}$ calibration) or 1b (full $R_{IN}$ and internal linearity calibration). |
| Bits 13:10 | Reserved. Must be set as shown. |
| Bits 9:8 | CMS(1:0): Calibration Mode Select. These bits affect the length of time taken to calibrate the internal linearity. CMS(1:0) = 11**b** is not available. See $t_{CAL}$ in *Converter Electrical Characteristics: AC Electrical Characteristics*. |
| Bits 7:0 | Reserved. Must be set as shown. |

**Table 16. Reserved**

| Addr: 5**h** (0101**b**) | | | | | | | | | Default Values: XXXX**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

| | |
|---|---|
| Bits 15:0 | Reserved. Do not write. |

**Table 17. Reserved**

| Addr: 6**h** (0110**b**) | | | | | | | | | Default Values: 1C70**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bits 15:0 | Reserved. Must be set as shown. |

**Table 18. Reserved**

| Addr: 7**h** (0111**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bits 15:0 | Reserved. Must be set as shown. |

**Table 19. Reserved**

| Addr: 8**h** (1000**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bits 15:0 | Reserved. Must be set as shown. |

**Table 20. Reserved**

| Addr: 9**h** (1001**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bits 15:0 | Reserved. Must be set as shown. |

### Table 21. Q-Channel Offset Adjust

| Addr: A**h** (1010**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | OS | OM(11:0) | | | | | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bits 15:13 | Reserved. Must be set to 0**b**. | |
| Bit 12 | OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bit to 1**b** incurs a negative offset of the set magnitude. | |
| Bits 11:0 | OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of -11 µV. Monotonicity is ensured by design only for the 9MSBs. | |
| | **CODE** | **OFFSET [mV]** |
| | 0000 0000 0000 (default) | 0 |
| | 1000 0000 0000 | 22.5 |
| | 1111 1111 1111 | 45 |

### Table 22. Q-Channel Full-Scale Range Adjust

| Addr: B**h** (1011**b**) | | | | | | | | | Default Values: 4000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Res | FM(14:0) | | | | | | | | | | | | | | |
| **DV** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| Bit 15 | Reserved. Must be set to 0**b**. | |
| Bits 14:0 | FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 630 mV (0**d**) to 980 mV (32767**d**) with the default setting at 820 mV (16384**d**). Monotonicity is ensured by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM; that is, FSR values above 820 mV. See *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*for characterization details. | |
| | **CODE** | **FSR [mV]** |
| | 000 0000 0000 0000 | 630 |
| | 100 0000 0000 0000 (default) | 820 |
| | 111 1111 1111 1111 | 980 |

### Table 23. Aperture Delay Coarse Adjust

| Addr: C**h** (1100**b**) | | | | | | | | | Default Values: 0004**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | CAM(11:0) | | | | | | | | | | | | STA | DCC | Reserved | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| | |
|---|---|
| Bits 15:4 | CAM(11:0): Coarse Adjust Magnitude. This 12-bit value determines the amount of delay that will be applied to the input CLK signal. The range is 0 ps delay for CAM(11:0) = 0**d** to a maximum delay of 825 ps for CAM(11:0) = 2431**d** (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432**d** and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register D**h**. Either STA (Bit 3) or SA (Addr: D**h,** Bit 8) must be selected to enable this function. |
| Bit 3 | STA: Select $t_{AD}$ Adjust. Set this bit to 1**b** to enable the $t_{AD}$ adjust feature. When using this feature, make sure that SA (Addr: D**h**, Bit 8) is set to 0**b**. |
| Bit 2 | DCC: Duty Cycle Correct. This bit can be set to 0**b** to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default. |
| Bits 1:0 | Reserved. Must be set to 0**b**. |

### Table 24. Aperture Delay Fine Adjust and LC Filter Adjust

| Addr: D**h** (1101**b**) | | | | | | | | | Default Values: 0000**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | FAM(5:0) | | | | | | Res | SA | LCF(7:0) | | | | | | | |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| Bits 15:10 | FAM(5:0): Fine Aperture Adjust Magnitude. This 6-bit value determines the amount of additional delay that will be applied to the input CLK when the Clock Phase Adjust feature is enabled via STA (Addr: C**h**, Bit 3) or SA (Addr: D**h**, Bit 8). The range is straight binary from 0 ps delay for FAM(5:0) = 0**d** to 2.3 ps delay for FAM(5:0) = 63**d** (±300 fs due to PVT variation) in steps of ~36 fs. |
| Bit 9 | Reserved. Must be set to 0**b**. |
| Bit 8 | SA: Select $t_{AD}$ and LC filter adjust. Set this bit to 1**b** to enable the $t_{AD}$ and LC filter adjust features. Using this bit is the same as enabling STA (Addr: C**h**, Bit3), but also enables the LC filter to clean the clock jitter. |
| Bits 7:0 | LCF(7:0): LC tank select frequency. Use these bits to select the center frequency of the LC filter on the Clock inputs. The range is from 0.8 GHz (255**d**) to 1.5 GHz (0**d**). Note that the tuning range is not binary encoded, and the eight bits are thermometer encoded; that is, the mid value of 1.1 GHz tuning is achieved with LCF(7:0) = 0000 1111**b**. |

### Table 25. AutoSync

| Addr: E**h** (1110**b**) | | | | | | | | | Default Values: 0003**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | DRC(9:0) | | | | | | | | | | Res. | SP(1:0) | | ES | DOC | DR |
| **DV** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| | |
|---|---|
| Bits 15:6 | DRC(9:0): Delay Reference Clock (9:0). These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The minimum delay is 0s (0**d**) to 1000 ps (639**d**). The delay remains the maximum of 1000 ps for any codes above or equal to 639**d**. |
| Bit 5 | Reserved. Must be set to 0**b**. |
| Bits 4:3 | SP(1:0): Select Phase. These bits select the phase of the reference clock which is latched. The codes correspond to the following phase shift:<br>00 = 0°<br>01 = 90°<br>10 = 180°<br>11 = 270° |
| Bit 2 | ES: Enable Slave. Set this bit to 1**b** to enable the slave mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the master ADC. The master clock is applied on the input pins RCLK+ or RCLK-. If this bit is set to 0**b**, then the device is in master mode. |
| Bit 1 | DOC: Disable Output Reference Clocks. Setting this bit to 0**b** sends a CLK/4 signal on RCOut1 and RCOut2. The default setting of 1**b** disables these output drivers. This bit functions as described, regardless of whether the device is operating in master or slave mode, as determined by ES (Bit 2). |
| Bit 0 | DR: Disable Reset. The default setting of 1**b** leaves the DCLK_RST functionality disabled. Set this bit to 0**b** to enable DCLK_RST functionality. |

### Table 26. Reserved

| Addr: F**h** (1111**b**) | | | | | | | | | Default Values: XXXX**h** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | Reserved | | | | | | | | | | | | | | | |
| **DV** | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

| | |
|---|---|
| Bits 15:0 | Reserved. Do not write. |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Analog Inputs

The ADC10D1000 continuously converts any signal which is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, the reference voltage and FSR, out-of-range indication, AC-coupled signals, and single-ended input signals.

#### *8.1.1.1 Acquiring the Input*

Data is acquired at the rising edge of CLK+ in non-DES mode and both the falling and rising edge of CLK+ in DES mode. The digital equivalent of that data is available at the digital outputs a constant number of input clock cycles later for the DI, DQ, DId and DQd output buses, also known as latency, depending on the demultiplex mode which was chosen. See $t_{LAT}$ in *Converter Electrical Characteristics: AC Electrical Characteristics*. In addition to latency, there is a constant output delay, $t_{OD}$, before the data is available at the outputs. See $t_{OD}$ in *Converter Electrical Characteristics: AC Electrical Characteristics* and *Timing Diagrams*.

For demux mode, the signal which is sampled at the input will appear at the output after a certain latency, as shown in Table 27.

**Table 27. Input Channel Samples Produced at Data Outputs in Demultiplexed Mode**

| DATA OUTPUTS | NON-DES MODE | DES MODE (Q channel ONLY) |
|---|---|---|
| DI | I channel sampled with rise of CLK, 34 cycles earlier. | Q channel sampled with rise of CLK, 34 cycles earlier. |
| DQ | Q channel sampled with rise of CLK, 34 cycles earlier. | Q channel sampled with fall of CLK, 34.5 cycles earlier. |
| DId | I channel sampled with rise of CLK, 35 cycles earlier. | Q channel sampled with rise of CLK, 35 cycles earlier. |
| DQd | Q channel sampled with rise of CLK, 35 cycles earlier. | Q channel sampled with fall of CLK, 35.5 cycles earlier. |

Non-Demux Mode is similarly shown in Table 28.

**Table 28. Input Channel Samples Produced at Data Outputs in Non-Demux Mode**

| DATA OUTPUTS | NON-DES MODE | DES MODE (Q channel ONLY) |
|---|---|---|
| DI | I channel sampled with rise of CLK, 34 cycles earlier. | Q channel sampled with rise of CLK, 34 cycles earlier. |
| DQ | Q channel sampled with rise of CLK, 34 cycles earlier. | Q channel sampled with fall of CLK, 34.5 cycles earlier. |
| DId | No output; high impedance. | No output; high impedance. |
| DQd | No output; high impedance. | No output; high impedance. |

#### 8.1.1.2 Terminating Unused Analog Inputs

In the case that only one channel is used in non-des mode or that the ADC is driven in DESI or DESQ mode, the unused analog input must be terminated to reduce any noise coupling into the ADC. See Table 29 for details.

**Table 29. Unused Analog Input Recommended Termination**

| MODE | POWER DOWN | COUPLING | RECOMMENDED TERMINATION |
|---|---|---|---|
| Non-DES | Yes | AC/DC | Tie unused+ and unused– to $V_{BG}$ |
| DES/ Non-DES | No | DC | Tie unused+ and unused– to $V_{BG}$ |
| DES/ Non-DES | No | AC | Tie unused+ to unused– |

#### 8.1.1.3 Reference Voltage and FSR

The full-scale analog differential input range ($V_{IN\_FSR}$) of the ADC10D1000 is derived from an internal 1.254-V bandgap reference. In non-ECM, this full-scale range has two settings controlled by the FSR pin; see *Full-Scale Input Range Pin (FSR)*. The FSR pin operates on both the I channel and the Q channel. In ECM, the full-scale range may be independently set for each channel via the I-channel and Q-channel Full-Scale Range Adjust Registers (Addr: 3**h** and B**h**, respectively) with 15 bits of precision; see *Register Maps*. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal 1.254-V bandgap reference voltage is made available at the $V_{BG}$ pin for the user. The $V_{BG}$ pin can drive a load of up to 80 pF and source or sink up to ±100 μA; it must be buffered if more current than this is required. The pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. $V_{BG}$ is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see *LVDS Output Common-Mode Voltage*.

#### 8.1.1.4 Out-of-Range Indication

Differential input signals are digitized to 10 bits, based on the full-scale range. Signal excursions beyond the full-scale range (greater than $+V_{IN}$ / 2 or less than $–V_{IN}$ / 2) are clipped at the output. An input signal that is above the FSR results in all 1's at the output and an input signal which is below the FSR results in all 0's at the output. When the conversion result is clipped for the I-channel input, the ORI I-channel output is activated such that ORI+ goes high and ORI– goes low for the time that the signal is out of range. This output is active as long as accurate data on either or both of the buses would be outside the range of 000**h** to 3FF**h**. The Q channel has a separate ORQ which functions similarly.

#### 8.1.1.5 AC-Coupled Input Signals

The ADC10D1000QML-SP analog inputs require a precise common-mode voltage. This voltage is generated onchip when AC-coupling mode is selected. See *AC-DC-Coupled Mode Pin ($V_{CMO}$)* for more information about how to select AC-coupled mode.

In AC-coupled mode, the analog inputs must of course be AC-coupled. For an ADC10D1000QML-SP used in a typical application, this may be accomplished by on-board capacitors, as shown in Figure 44.

When the AC-coupled mode is selected, an analog input channel that is not used (for example, in DES mode) must be connected to AC ground — for example, through capacitors to ground. Do not connect an unused analog input directly to ground.

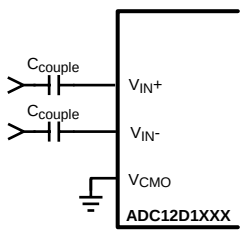



**Figure 44. AC-Coupled Differential Input**

The analog inputs for the ADC10D1000QML-SP are internally buffered, which simplifies the task of driving these inputs and the RC pole, which is generally used at sampling ADC inputs, is not required. If the user desires to place an amplifier circuit before the ADC, take care to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

#### *8.1.1.6 DC-Coupled Input Signals*

In DC-coupled mode, the ADC10D1000QML-SP differential inputs must have the correct common-mode voltage. This voltage is provided by the device itself at the $V_{CMO}$ output pin. TI recommends using this voltage because the $V_{CMO}$ output potential changes with temperature and the common-mode voltage of the driving device must track this change. Full-scale distortion performance falls off as the input common-mode voltage deviates from $V_{CMO}$. Therefore, TI recommends keeping the input common-mode voltage within 100 mV of $V_{CMO}$ (typical), although this range may be extended to ±150 mV (maximum).

#### *8.1.1.7 Single-Ended Input Signals*

It is not possible on the ADC10D1000 to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-transformer, as shown in *Figure 45*.

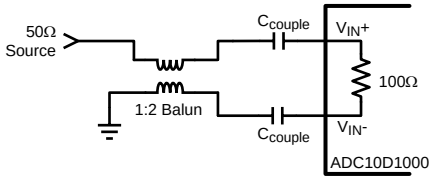



**Figure 45. Single-Ended-to-Differential Conversion Using a Balun**

When selecting a balun, it is important to understand the input architecture of the ADC. The impedance of the analog source must be matched to the ADC10D1000's on-chip 100-Ω differential input termination resistor. The range of this termination resistor is specified as $R_{IN}$ in *Converter Electrical Characteristics: Analog Input/Output and Reference Characteristics*.

### 8.1.2 Clock Inputs

The ADC10D1000 has a differential clock input, CLK+ and CLK–, which must be driven with an AC-coupled, differential clock signal. This provides the level shifting to the clock to be driven with LVDS, PECL, LVPECL, or CML levels. The clock inputs are internally terminated to 100-Ω differential and self-biased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

#### *8.1.2.1 CLK Coupling*

The clock inputs of the ADC10D1000 must be capacitively coupled to the clock pins as indicated in Figure 46.

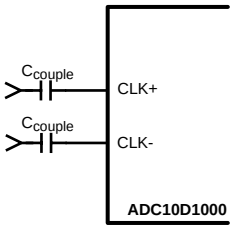



**Figure 46. Differential Input Clock Connection**

The choice of capacitor values depends on the clock frequency, capacitor component characteristics, and other system factors.

#### 8.1.2.2 CLK Frequency

Although the ADC10D1000 is tested and its performance is ensured with a differential 1-GHz clock, the device typically functions well over the input clock frequency range; see $f_{CLK\ (min)}$ and $f_{CLK\ (max)}$ in *Converter Electrical Characteristics: AC Electrical Characteristics*. Operation up to $f_{CLK\ (max)}$ is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above $f_{CLK\ (max)}$ for the maximum ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If the $f_{CLK} \leq 300$ MHz, enable LFS in control register (Addr: 0**h** Bit 8).

#### 8.1.2.3 CLK Level

The input clock amplitude is specified as $V_{IN\_CLK}$ in *Converter Electrical Characteristics: LVDS CLK Input Characteristics*. Input clock amplitudes above the maximum $V_{IN\_CLK}$ may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 511/512 when both input pins are at the same potential. Insufficient input clock levels will result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of $V_{IN\_CLK}$.

#### 8.1.2.4 CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any ADC. The ADC10D1000 features a duty-cycle-clock correction circuit, which can maintain performance over the 20%-to-80% specified clock duty cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the dual-edge sampling (DES) mode.

#### 8.1.2.5 CLK Jitter

High-speed, high-performance ADCs such as the ADC10D1000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full-scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)} / V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (1)$$

where

- $t_{J(MAX)}$ is the rms total of all jitter sources in seconds
- $V_{IN(P-P)}$ is the peak-to-peak analog input signal
- $V_{FSR}$ is the full-scale range of the ADC
- N is the ADC resolution in bits
- $f_{IN}$ is the maximum input frequency, in Hertz, at the ADC analog input

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) sum of the jitter from all sources, including the ADC input clock, system, input signals and the ADC itself. Since the effective jitter added by the ADC is beyond user control, TI recommends keeping the sum of all other externally added jitter to a mimimum.

#### 8.1.2.6 CLK Layout

The ADC10D1000 clock input is internally terminated with a trimmed 100-Ω resistor. The differential input clock line pair must have a characteristic impedance of 100 Ω and (when using a balun), be terminated at the clock source in that (100-Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals, and to treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can also introduce noise into the analog path if it is not properly isolated.

### 8.1.3 The LVDS Outputs

The Data, ORI, ORQ, DCLKI, and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips, but they are not IEEE or ANSI communications standards compliant due to the low 1.9-V supply used on this device. These outputs must be terminated with a 100-Ω differential resister placed as closely as possible to the receiver. This section covers common-mode and differential voltage, and data rate.

#### 8.1.3.1 Common-Mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, $V_{OS}$ and $V_{OD}$; see *Converter Electrical Characteristics: Digital Control and Output Pin Characteristics*. See *Output Control and Adjust* for more information.

Selecting the higher $V_{OS}$ also increases $V_{OD}$ by up to 40 mV. The differential voltage, $V_{OD}$, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be realized with the lower $V_{OD}$. This also results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC10D1000 is used is noisy, it may be necessary to select the higher $V_{OD}$.

#### 8.1.3.2 Output Data Rate

The data is produced at the output at the same rate as it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK\ (MIN)}$; see *Converter Electrical Characteristics: AC Electrical Characteristics*. However, it is possible to operate the device in 1:2 demux mode and capture data from just one 10-bit bus, for example, just DI (or DId) although both DI and DId are fully operational. This will decimate the data by two and effectively halve the data rate.

### 8.1.4 Synchronizing Multiple ADC10D1000S in a System

The ADC10D1000 has two features to assist the user with synchronizing multiple ADCs in a system: AutoSync and DCLK Reset. The AutoSync feature is new and designates one ADC10D1000 as the master ADC and other ADC10D1000s in the system as Slave ADCs. The DCLK Reset feature performs the same function as the AutoSync feature, but is the first generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For applications in which there are multiple master and slave ADC10D1000s in a system, AutoSync may be used to synchronize the slave ADC10D1000(s) to each respective master ADC10D1000, and the DCLK Reset may be used to synchronize the master ADC10D1000s with each other.

If the AutoSync or DCLK reset feature is not used, see Table 30 for recommendations about terminating unused ins.

**Table 30. Unused AutoSync and DCLK Pin Recommendations**

| PIN(s) | UNUSED TERMINATION |
|---|---|
| RCLK+, RCLK– | Do not connect. |
| RCOUT1+, RCOUT– | Do not connect. |
| RCOUT2+, RCOUT– | Do not connect. |
| DCLK_RST+ | Connect to GND with a 1-kΩ resistor. |
| DCLK_RST– | Connect to VA with a 1-kΩ resistor. |

#### 8.1.4.1 AutoSync Feature

AutoSync is a new feature, which continuously synchronizes the outputs of multiple ADC10D1000s in a system. It may be used to synchronize the DCLK and data outputs of one or more dlave ADC10D1000s to one master ADC10D1000. Several advantages of this feature include no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the master/dlave ADC10D1000s may be arranged as a binary tree so that any upset quickly propagates out of the system.

An example system, which consists of one master ADC and two slave ADCs, is shown in Figure 47. For simplicity, only one DCLK is shown; in reality, there is DCLKI and DCLKQ, but they are always in phase with one another.

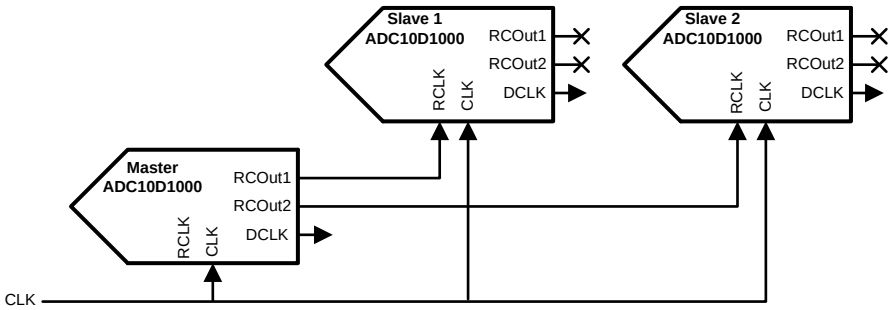



**Figure 47. AutoSync Example**

In order to synchronize the DCLK (and data) outputs of multiple ADCs, the DCLKs must transition at the same time, as well as be in phase with one another. The DCLK at each ADC is generated from the CLK after some latency, plus $t_{OD}$ minus $t_{AD}$. Therefore, in order for the DCLKs to transition at the same time, the CLK signal must reach each ADC at the same time. To tune out any differences in the CLK path to each ADC, the $t_{AD}$ adjust feature may be used. However, using the $t_{AD}$ adjust feature will also affect when the DCLK is produced at the output. If the device is in demux mode, then there are four possible phases which each DCLK may be generated on because the typical CLK = 1 GHz and DCLK = 250 MHz for this case. The RCLK signal controls the phase of the DCLK, so that each Slave DCLK is on the same phase as the Master DCLK.

The AutoSync feature may only be used via the Control Registers. For more information, see *AN-2132 Synchronizing Multiple GSPS ADCs in a System: The AutoSync Feature* (SNAA073).

### *8.1.4.2 DCLK Reset Feature*

The DCLK reset feature is available via ECM, but is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized.

The DCLK_RST signal must observe certain timing requirements, which are shown in Figure 5 of *Timing Diagrams*. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as $t_{PWR}$, $t_{SR}$ and $t_{HR}$ and may be found in *Converter Electrical Characteristics: AC Electrical Characteristics*.

The DCLK_RST signal can be asserted asynchronously to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in demux mode; in non-demux mode, the DCLK continues to function normally. Depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event When the DCLK_RST signal is de-asserted, there are $t_{SYNC\_DLY}$ CLK cycles of systematic delay, and the next CLK rising edge synchronizes the DCLK output with those of other ADC10D1000s in the system. For 90° mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0° mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of $t_{OD}$.

For both demux and non-demux modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK comes out of the reset state in a known way. Therefore, if using the DCLK reset feature, TI recommends applying one *dummy* DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered on.

When the DCLK_RST function is not going to be used TI recommends pulling the DCLK+ pin to GND through a 261-Ω resister and pulling the DCLK− pin to $V_A$ through a 261-Ω resistor (see Figure 48). This provides noise immunity and prevent false resets.

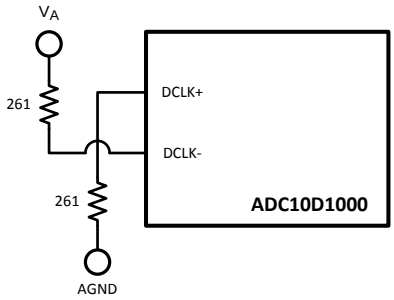



**Figure 48. DCLK RST±**

When using DCLK-RST to synchronize multiple ADC10D1000s, it is required that the select phase bits in the Control Register (Addr: E**h**, Bits 3,4) be the same for each Slave ADC10D1000.

# 9 Power Supply Recommendations

## 9.1 Power Planes

Source all supply buses for the ADC from a common linear voltage regulator. This ensures that all power buses to the ADC are turned on and off simultaneously. This single source is split into individual sections of the power plane, with individual decoupling and connection to the different power supply buses of the ADC. Due to the low voltage but relatively high supply current requirement, the optimal solution may be to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator. Refer to the documentation provided for the ADC10D1000RB for additional details on specific regulators that TI recommends for this configuration.

Provide power for the ADC through a broad plane, which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers provides low impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator must feed into the power plane through a low impedance multi-via connection. Split the power plane into individual power peninsulas near the ADC. Each peninsula should feed a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, 0-Ω resistors can be used to connect the power source net to the individual nets for the different ADC power buses. As a final step, the 0-Ω resistors can be removed, and the plane and peninsulas can be connected manually after all other error checking is completed.

### 9.1.1 Bypass Capacitors

The general recommendation is to have one 100-nF capacitor for each power/ground pin pair. The capacitors must be surface mount multi-layer ceramic chip capacitors similar to Presidio SR0402X7R104KENG5.

#### *9.1.1.1 Ground Plane*

Grounding must be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

#### *9.1.1.2 Power Supply Example*

The ADC10D1000RB uses continuous ground planes (except where clear areas are needed to provide appropriate impedance management for specific signals), see Figure 49. Power is provided on one plane, with the 1.9-V ADC supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power bus peninsulas and the adjacent power planes using vias. The capacitors are located as close to the individual power/ground pin pairs of the ADC as possible. In most cases, this means the capacitors are located on the opposite side of the PCB to the ADC.

## Power Planes (continued)

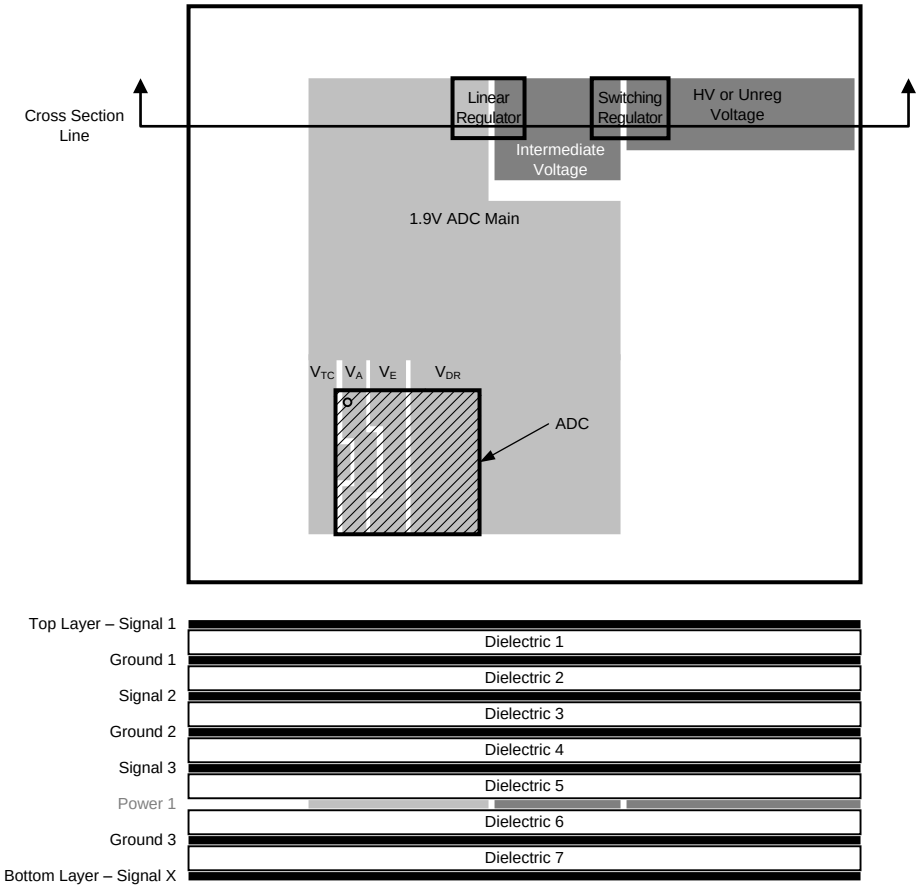



**Figure 49. Power and Grounding Example**

# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Board Mounting Recommendation

Proper thermal profile is required to establish re-flow under the package and ensure all joints meet profile specifications, See Table 31.

**Table 31. Solder Profile Specification**

| RANGE UP | PEAK TEMPERATURE ($T_{PK}$) | MAXIMUM PEAK TEMPERATURE | RAMP DOWN |
|---|---|---|---|
| ≤ 4°C/sec | 210°C ≤ $t_{PK}$ ≤ 215°C | ≤ 220°C | ≤ 5°C/sec |

The 220°C peak temperature is driven by the requirement to limit the dissolution of lead from the high-melt column to the eutectic solder. Too much lead increases the effective melting point of the board-side joint and makes it much more difficult to remove the part if module rework is required.

Cool-down rates and methods affect CCGA assemble yield and reliability. Picking up boards or opening the oven while solder joints are in molten state can disturb the solder joint. Do not pick up boards until the solder joints have fully solidified. Board warping may potentially cause the CCGA to lift off of pads during cooling and this condition can also cause column cracking when severe. This warping is a result of a high differential cooling rate between the top and bottom of the board. Both conditions can be prevented by using even top and bottom cooling.

## 10.2 Layout Example

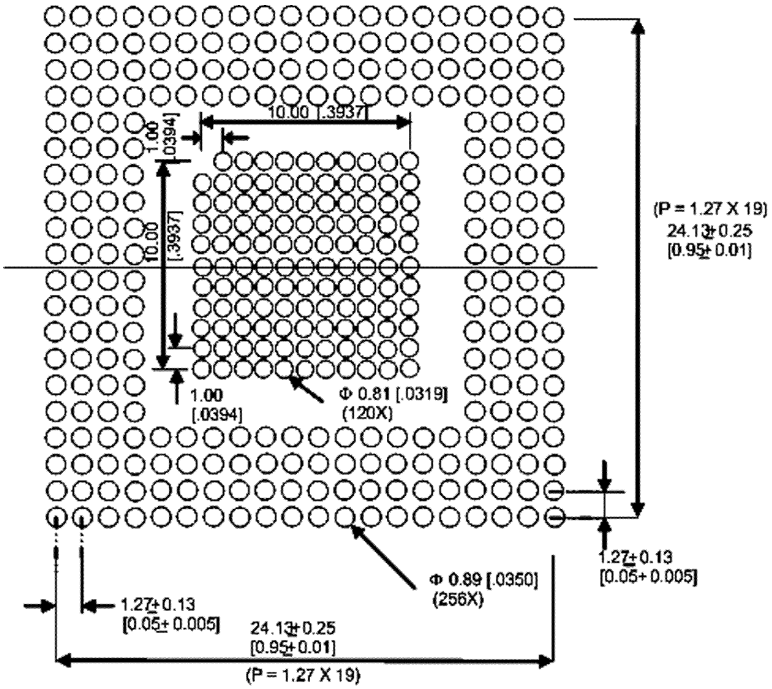



**Figure 50. Landing Pattern Recommendation**

## 10.3 Thermal Management

The ceramic column grid array (CCGA) package is a modified ceramic land grid array with an added heat sink. The signal columns on the outer edge are 1.27-mm pitch, while the columns in the center attached to the heat sink are 1 mm. The smaller pitch for the center columns is to improve the thermal resistance. The center columns of the package are attached to the back of the die through a heat sink. Connecting these columns to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the ADC. These pins must also be connected to the ground planes through low impedance path for electrical purposes.

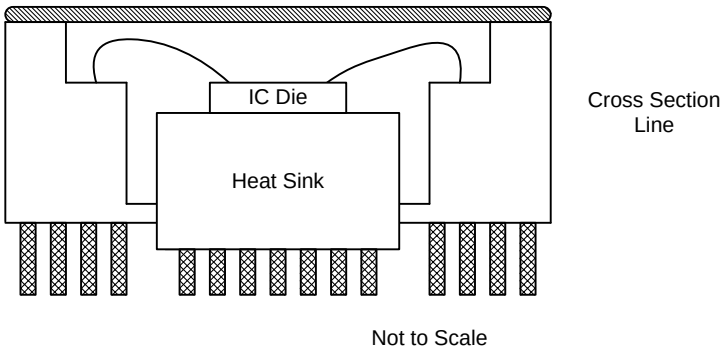



**Figure 51. CCGA Conceptual Drawing**

## 10.4 Temperature Sensor Diode

The ADC10D1000 has an on-die temperature diode connected to pins Tdiode+, Tdiode– which may be used to monitor the die temperature. Texas Instruments also provides a family of temperature sensors for this application which monitor different numbers of external devices, See Table 32.

**Table 32. Temperature Sensor Recommendation**

| NUMBER OF EXTERNAL DEVICES MONITORED | RECOMMENDED TEMPERATURE SENSOR |
|---|---|
| 1 | LM95235 |
| 2 | LM95213 |
| 4 | LM95214 |

The LM95235/13/14 is an 11-bit digital temperature sensor with a 2-wire system management bus (SMBus) interface that can monitor the temperature of one/two/four remote diodes as well as its own temperature. The LM95235/13/14 can be used to accurately monitor the temperature of up to one/two/four external devices such as the ADC10D1000, a FPGA, other system components, and the ambient temperature.

The LM95235/13/14 reports temperature in two different formats for 127.875°C range and 0°/255°C range. The LM95235/13/14 has a sigma-delta ADC core which provides the first level of noise immunity. For improved performance in a noise environment, the LM9535/13/14 includes programmable digital filters for remote diode temperature readings. When the digital filters are invoked, the resolution for the remote diode readings increases to 0.03125°C. For maximum flexibility and best accuracy, the LM95235/13/14 includes offset registers that allow calibration of other diode types.

Diode fault detection circuitry in the LM95235/13/14 can detect the absence or fault state of a remote diode: whether the D+ pin is detected as shorted to GND, D-, VDD or D+ is floating.

In the following typical application, the LM95213 is used to monitor the temperature of an ADC10D1000 as well as an FPGA. See Figure 52.

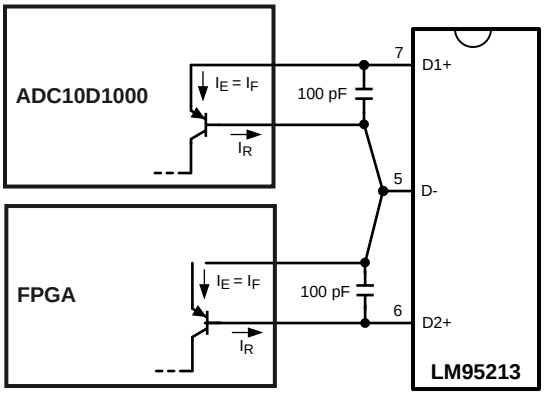



**Figure 52. Typical Temperature Sensor Application**

## 10.5 Radiation Environments

Give careful consideration to environmental conditions when using a product in a radiation environment.

### 10.5.1 Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer-level TID data is available with lot shipments.

### 10.5.2 Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in *Features* is the maximum LET tested. A test report is available upon request.

### 10.5.3 Single Event Upset

A report on single event upset (SEU) is available at www.ti.com/radiation.

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 11.1.2 Device Nomenclature

#### *11.1.2.1 Specification Definitions*

**APERTURE (SAMPLING) DELAY** is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

**APERTURE JITTER ($t_{AJ}$)** is the variation in aperture delay from sample-to-sample. Aperture jitter can be effectively considered as noise at the input.

**CODE ERROR RATE (C.E.R.)** is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A CER of $10^{-18}$ corresponds to a statistical error in one word about every four (4) years.

**CLOCK DUTY CYCLE** is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB. It is measured at sample rate = 500 MSPS with a 1-MHz input sine wave.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this many (ENOB) number of bits.

**FULL POWER BANDWIDTH (FPBW)** is a measure of the frequency at which the reconstructed output fundamental drops to 3 dB below its low frequency value for a full-scale input.

**GAIN ERROR** is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors. The Positive Gain Error is the Offset Error minus the Positive Full-Scale Error. The Negative Gain Error is the Negative Full-Scale Error minus the Offset Error. The Gain Error is the Negative Full-Scale Error minus the Positive Full-Scale Error; it is also equal to the Positive Gain Error plus the Negative Gain Error.

**INTEGRAL NON-LINEARITY (INL)** is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

**LSB (LEAST SIGNIFICANT BIT)** is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N \quad (2)$$

where $V_{FS}$ is the differential full-scale amplitude $V_{IN}$ as set by the FSR input and "N" is the ADC resolution in bits, which is 10 for the ADC10D1000.

**LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE ($V_{ID}$ and $V_{OD}$)** is two times the absolute value of the difference between the $V_D$+ and $V_D$– signals; each measured with respect to Ground.

## Device Support (continued)

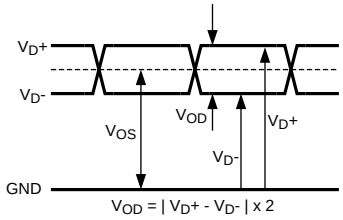



**Figure 53. LVDS Output Signal Levels**

**LVDS OUTPUT OFFSET VOLTAGE ($V_{OS}$)** is the midpoint between the D+ and D– pins output voltage with respect to ground; that is, [($V_D$+) +( $V_D$-)]/2. See Figure 53.

**MISSING CODES** are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

**MSB (MOST SIGNIFICANT BIT)** is the bit that has the largest value or weight. Its value is one half of full scale.

**NEGATIVE FULL-SCALE ERROR (NFSE)** is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN}/2$ with the FSR pin low. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

**NOISE POWER RATIO (NPR)** is the ratio of the sum of the power inside the notched bins to the sum of the power in an equal number of bins outside the notch, expressed in dB.

**OFFSET ERROR ($V_{OFF}$)** is a measure of how far the mid-scale point is from the ideal zero voltage differential input. Offset Error = Actual Input causing average of 8k samples to result in an average code of 511.5.

**OUTPUT DELAY ($t_{OD}$)** is the time delay (in addition to Pipeline Delay) after the falling edge of CLK+ before the data update is present at the output pins.

**OVER-RANGE RECOVERY TIME** is the time required after the differential input voltages goes from ±1.2 V to 0 V for the converter to recover and make a conversion with its rated accuracy.

**PIPELINE DELAY (LATENCY)** is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the $t_{OD}$.

**POSITIVE FULL-SCALE ERROR (PFSE)** is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}/2$. For the ADC10D1000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

**POWER SUPPLY REJECTION RATIO (PSRR)** is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8 V to 2 V. PSRR is expressed in dB.

**SIGNAL-TO-NOISE RATIO (SNR)** is the ratio, expressed in dB, of the RMS value of the input signal at the output to the RMS value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

**SIGNAL-TO-NOISE PLUS DISTORTION (S/(N+D) or SINAD)** is the ratio, expressed in dB, of the RMS value of the input signal at the output to the RMS value of all of the other spectral components below half the input clock frequency, including harmonics but excluding DC.

**SPURIOUS-FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the RMS values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio expressed in dB, of the RMS total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \quad (3)$$

## Device Support (continued)

where $A_{f1}$ is the RMS power of the fundamental (output) frequency and $A_{f2}$ through $A_{f10}$ are the RMS power of the first 9 harmonic frequencies in the output spectrum.

**– Second Harmonic Distortion (2nd Harm)** is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

**– Third Harmonic Distortion (3rd Harm)** is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

## 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 33. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| ADC10D1000CCMLS | Click here | Click here | Click here | Click here | Click here |
| ADC10D1000CVAL | Click here | Click here | Click here | Click here | Click here |

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Engineering Samples

Engineering samples are available for order and are identified by the *MPR* in the orderable device name (see Packaging Information in the POA). Engineering (MPR) samples meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC10D1000CCMLS | ACTIVE | CCGA | NAA | 376 | 144 | Non-RoHS & Non-Green | Call TI | Call TI | -55 to 125 | (ADC10D1000CC, ADC 10D1000CCMLS) MLS | Samples |
| ADC10D1000CCMPR | ACTIVE | CCGA | NAA | 376 | 144 | Non-RoHS & Non-Green | Call TI | Call TI | 25 to 25 | (ADC10D1000CC, ADC 10D1000CCMPR) ES | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

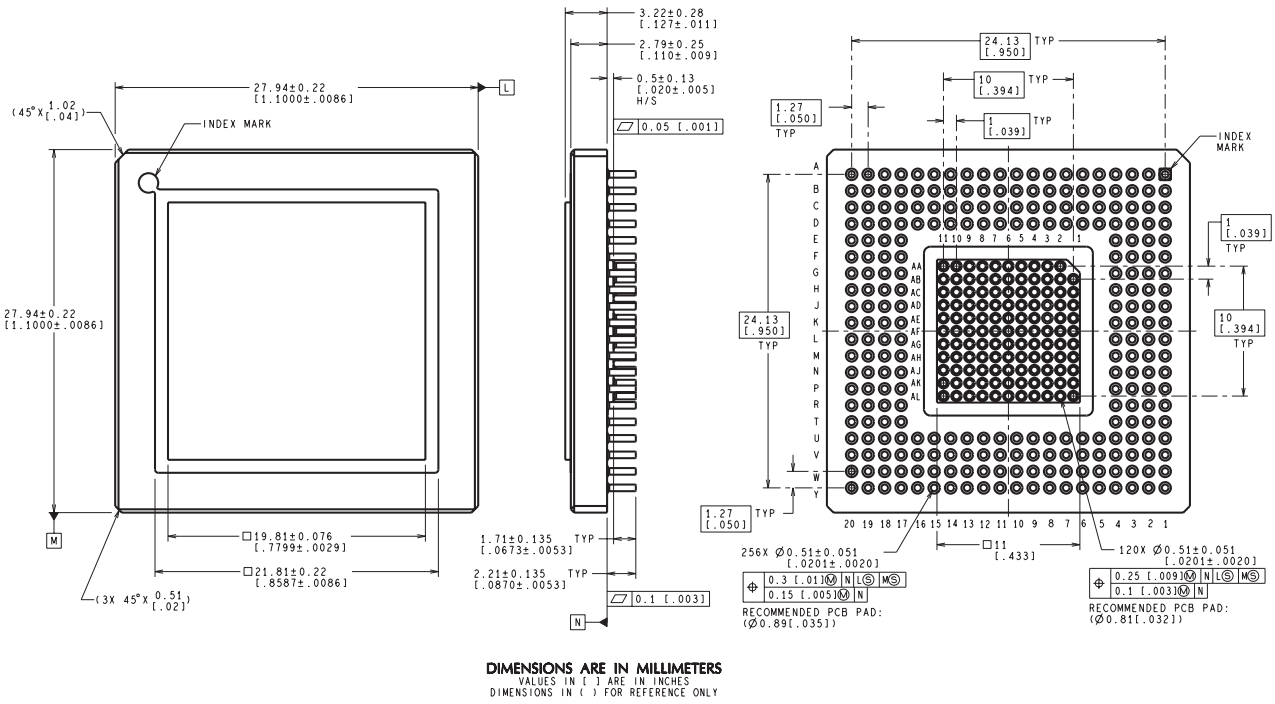
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# NAA0376A




**DIMENSIONS ARE IN MILLIMETERS**
VALUES IN [ ] ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

CCC376A (Rev D)

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