ADC168M102R-SEP 放射線耐性、8 チャネル、1MSPS、16 ビット ADC

1 特長

- 放射線耐性:
  - シングル イベント ラッチアップ (SEL) 耐性:
    LET = 43MeV-cm^2/mg (125℃) まで
  - LET = 43MeV-cm^2/mg まで、シングル イベント機能割り込み (SEFI) 特性を評価済み
  - 30krad (Si) まで、総吸収線量 (TID) RLAT/RHA 特性を評価済み
- 宇宙用強化プラスチック (宇宙用 EP):
  - 防衛および航空宇宙アプリケーションをサポート
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 長期にわたる製品ライフ サイクル
  - 製品のトレーサビリティ
  - ASTM E595 に準拠した気体排出試験実施済み
  - VID (Vendor Item Drawing) V62/24631
  - 軍用温度範囲:-55℃～+125℃
  - 金ボンド ワイヤ、NiPdAu リード仕上げ
- 8 つの擬似差動入力または 4 つの完全差動入力
- 2 チャネルの同時サンプリング
- 優れた AC 特性:
  - 信号対雑音比:93 dB
  - THD:-98 dB
- デュアル プログラマブルおよびデュアル バッファ 2.5V 基準電圧により次のことが可能:
  - 2 種類の入力電圧範囲設定
  - 2 レベル PGA 実装
- プログラマブル自動シーケンサ
- オーバーサンプリング アプリケーション向けの内蔵データ ストレージ (チャネルごとに最大 4 つ)
- 安全アプリケーション用の 2 ビットカウンタ

2 アプリケーション

- 衛星用電源システム (EPS)
- コマンドとデータの処理 (C&DH)
- 光学画像処理ペイロード
- モータ制御
- 電圧、電流、温度の監視
- 加速度計

3 概要

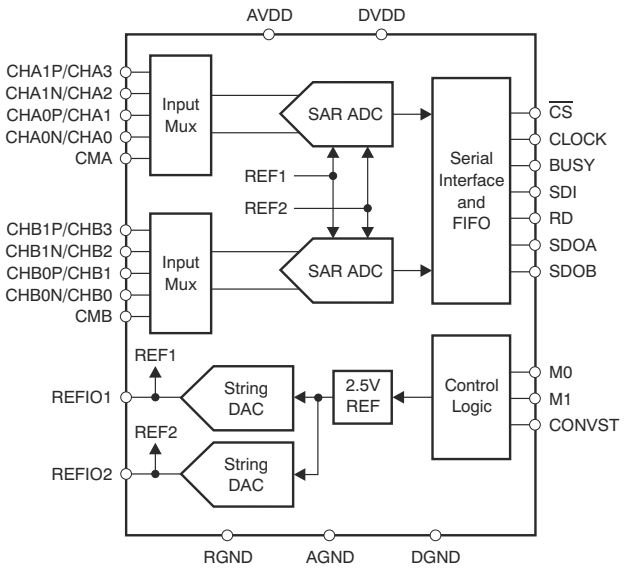
ADC168M102R-SEP はデュアル、16 ビット、1MSPS の A/D コンバータ (ADC) です。この ADC には、8 つの擬似差動入力チャネルまたは 4 つの完全差動入力チャネルがあり、同時に信号を収集するために、2 つのペアにグループ化されています。アナログ入力は、ADC の入力に対して差動で維持されます。入力マルチプレクサは、疑似差動モードまたは完全差動モードのいずれかで使用します。疑似差動モードでは、ADC ごとに最大 4 つのチャネル (4x2) をサポートし、完全差動モードでは ADC ごとに最大 2 つの入力 (2x2) を変換します。

ADC168M102R-SEP は 2 つのプログラマブル リファレンス出力、フレキシブルな電源電圧範囲、プログラマブル自動シーケンサ、複数のパワーダウン機能を備えています。また、このデバイスには、チャネルごとに最大 4 つの変換結果がデータ保存されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADC168M102R-SEP	RHB (VQFN、32)	5mm × 5mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Pin Configuration and Functions

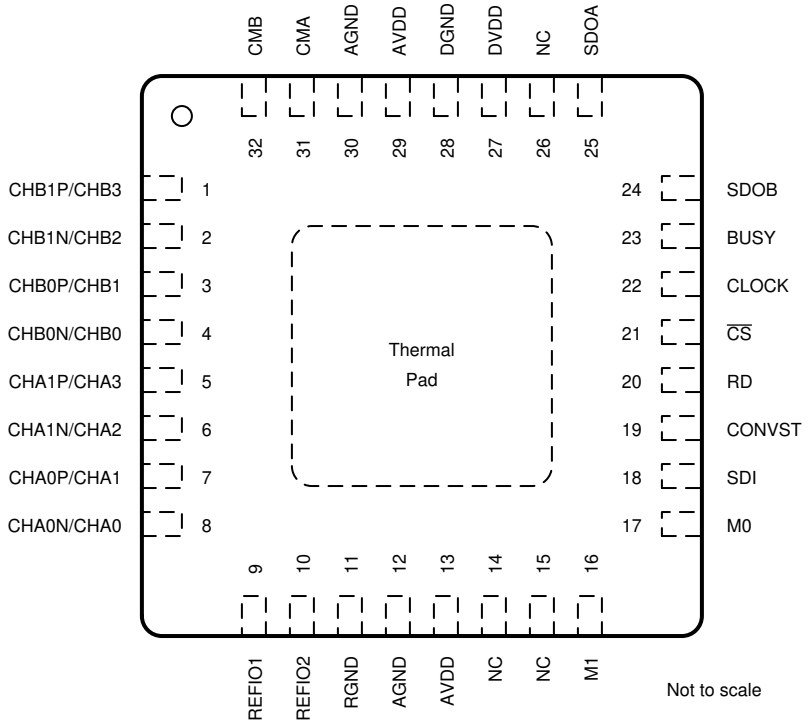


図 4-1. RHB Package, 32-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	12, 30	P	Analog ground. Connect to analog ground plane.
AVDD	13, 29	P	Analog power supply, 2.7V to 5.5V. Decouple to AGND with a 1µF ceramic capacitor.
BUSY	23	DO	Converter busy indicator. BUSY goes high when the inputs are in hold mode and returns to low after the conversion is complete.
CHA0N/CHA0	8	AI	Fully differential inverting analog input channel A1 or pseudo-differential input A0
CHA0P/CHA1	7	AI	Fully differential noninverting analog input channel A1 or pseudo-differential input A1
CHA1N/CHA2	6	AI	Fully differential inverting analog input channel A1 or pseudo-differential input A2
CHA1P/CHA3	5	AI	Fully differential noninverting analog input channel A1 or pseudo-differential input A3
CHB0N/CHB0	4	AI	Fully differential inverting analog input channel B0 or pseudo-differential input B0
CHB0P/CHB1	3	AI	Fully differential noninverting analog input channel B0 or pseudo-differential input B1
CHB1N/CHB2	2	AI	Fully differential inverting analog input channel B1 or pseudo-differential input B2
CHB1P/CHB3	1	AI	Fully differential noninverting analog input channel B1 or pseudo-differential input B3
CLOCK	22	DI	External clock input. The range is 0.5MHz to 20MHz in half-clock mode, or 1MHz to 40MHz in full-clock mode.
CMA	31	AI	Common-mode voltage input for channels Ax (in pseudo-differential mode only).
CMB	32	AI	Common-mode voltage input for channels Bx (in pseudo-differential mode only).
CONVST	19	DI	Conversion start. The ADC switches from sample into hold mode on the rising edge of CONVST. Thereafter, the conversion starts with the next rising edge of the CLOCK pin.
$\overline{CS}$	21	DI	Chip select. When this pin is low, the SDOx, SDI, and RD pins are active. When this pin is high, the SDOx outputs are tri-stated, and the SDI and RD inputs are ignored.
DGND	28	P	Digital ground. Connect to digital ground plane.
DVDD	27	P	Digital supply, 2.3V to 5.5V. Decouple to DGND with a 1µF ceramic capacitor.
M0	17	DI	Mode pin 0. Selects analog input channel mode (see 表 6-5).
M1	16	DI	Mode pin 1. Selects the digital output mode (see 表 6-5).

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	14, 15, 26	NC	This pin is not internally connected.
RD	20	DI	Read data. Synchronization pulse for the SDOx outputs and SDI input. RD only triggers when $\overline{CS}$ is low.
REFIO1	9	AIO	Reference voltage input/output 1. Connect 22µF ceramic capacitor is connected to RGND.
REFIO2	10	AIO	Reference voltage input/output 2. Connect 22µF ceramic capacitor is connected to RGND.
RGND	11	P	Reference ground. Connect this pin to analog ground plane with a dedicated via.
SDI	18	DI	Serial data input. This pin sets up the internal registers. The data on SDI are ignored when $\overline{CS}$ is high.
SDOA	25	DO	Serial data output for converter A. This pin is in tri-state when $\overline{CS}$ is high.
SDOB	24	DO	Serial data output for converter B. Active only if M1 is low. This pin is in tri-state when $\overline{CS}$ is high.

(1) AI = analog input, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output, P = power supply, NC = not connected.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, AVDD to AGND or DVDD to DGND	–0.3	6	V
Supply voltage, DVDD to AVDD	–0.3	1.2 x AVDD(2)	V
Analog and reference input voltage with respect to AGND	AGND – 0.3	AVDD + 0.3	V
Digital input voltage with respect to DGND	DGND – 0.3	DVDD + 0.3	V
Ground voltage difference, AGND – DGND	–0.3	0.3	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Exceeding the specified limit causes an increase of the DVDD leakage current and leads to malfunction of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
AVDD	Analog power supply	AVDD to AGND, half-clock mode	2.7	5.0	5.5	V
		AVDD to AGND, full-clock mode	4.5	5.0	5.5	
DVDD	Digital power supply	3V and 3.3V levels	2.3	2.5	3.6	V
		5V levels, half-clock mode only	4.5	5.0	5.5	
FSR	Full-scale analog input range	(CHxxP – CHxxN) or CHxx to CMx	$-V_{REF}$		V_{REF}	V
V_{IN}	Absolute input voltage	CHxxx to AGND	–0.1		AVDD + 0.1	V
T_A	Ambient temperature		–55	25	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		ADC168M102R-SEP	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at AVDD and DVDD supply voltage ranges specified in *Recommended Operating Conditions*, VREF = 2.5V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –55°C to 125°C; typical values at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_{DCL}	Input leakage current		–16		16	nA
C_{IN}	Input capacitance	CHxxx to AGND		45		pF
C_{ID}	Differential input capacitance	CHxxx to AGND		22.5		pF
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity	Half-clock mode	–2	±0.6	2	LSB
		Full-clock mode	–2	±0.8	4	
INL	Integral nonlinearity	Half-clock mode	–4	±1.2	4	LSB
		Full-clock mode	–5	±1.5	5	
V_{OS}	Input offset error		–2.5	±0.2	2.5	mV
	V_{OS} match	ADC to ADC	–1.5	±0.1	1.5	mV
dV_{OS}/dT	Input offset error thermal drift			1		µV/°C
G_{ERR}	Gain error		–0.15	0.01	0.15	%FSR
	G_{ERR} match	ADC to ADC	–0.15	0.01	0.15	%FSR
G_{ERR}/dT	G_{ERR} thermal drift			1		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	V_{IN} = $5V_{PP}$, f_{IN} = 10kHz	88	92		dB
SNR	Signal-to-noise ratio	V_{IN} = $5V_{PP}$, f_{IN} = 10kHz	89	93		dB
THD	Total harmonic distortion	V_{IN} = $5V_{PP}$, f_{IN} = 10kHz		–98	–90	dB
SFDR	Spurious-free dynamic range	V_{IN} = $5V_{PP}$, f_{IN} = 10kHz	89	100		dB
CMRR	Common-mode rejection ratio	Both ADCs, f_{IN} = dc to 100kHz		92		dB
PSRR	Power-supply rejection ratio			75		dB
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		2.485	2.5	2.525	V
I_{REF}	Reference input current			50		
C_{REF}	External decoupling capacitor			22		µF
INTERNAL VOLTAGE REFERENCE						
	Reference output DAC resolution		10			Bits
V_{REFOUT}	Reference output voltage	>20% to 100% of DAC range	0.2 x V_{REFOUT}		V_{REFOUT}	V
		REFIO1, DAC = 3FFh	2.485	2.500	2.515	
		REFIO2, DAC = 3FFh	2.485	2.500	2.515	
DNL_{DAC}	DAC DNL		–5	±1	5	LSB
INL_{DAC}	DAC INL		–5	±0.5	5	LSB
$PSRR_{DAC}$	Power-supply rejection ratio			73		dB
I_{REFOUT}	Output DC current			±2		mA
I_{REFSC}	Output short-circuit current[1]			50		mA
DIGITAL INPUTS						
	Input current[2]	V_{IN} = DVDD to DGND	–50		50	nA
	Digital input capacitance			5		pF
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	Input high logic level	DVDD = 4.5V to 5.5V	0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Input low logic level	DVDD = 4.5V to 5.5V	–0.3		0.3 x DVDD	V
	Logic family			LVCMOS		
V_{IH}	Input high logic level	DVDD = 2.3V to 3.6V	2		DVDD + 0.3	V

5.5 Electrical Characteristics (続き)

at AVDD and DVDD supply voltage ranges specified in *Recommended Operating Conditions*, VREF = 2.5V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –55°C to 125°C; typical values at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low logic level	DVDD = 2.3V to 3.6V	–0.3		0.8	V
DIGITAL OUTPUTS						
C_{OUT}	Output capacitance			5		pF
C_{LOAD}	Load capacitance				30	pF
	Logic family			CMOS		
V_{IH}	Output high logic level	DVDD = 4.5V, I_{LOAD} = –100uA	4.44			V
V_{IL}	Output low logic level	DVDD = 4.5V, I_{LOAD} = 100uA			0.5	V
	Logic family			LVCMOS		
V_{IH}	Output high logic level	DVDD = 2.3V, I_{LOAD} = –100uA	DVDD – 0.2			V
V_{IL}	Output low logic level	DVDD = 2.3V, I_{LOAD} = 100uA			0.2	V
POWER SUPPLY						
AIDD	Analog supply current	AVDD = 3.6V		12	18	mA
		AVDD = 5.5V		15	25	
		AVDD = 3.6V, sleep and auto-sleep modes		0.8	2	
		AVDD = 5.5V, sleep and auto-sleep modes		0.9	6.2	
		Power-down mode			0.15	
DIDD	Digital supply current	DVDD = 3.6V, C_{LOAD} = 10pF		1.1	3	mA
		DVDD = 5.5V, C_{LOAD} = 10pF		3	13	
P_D	Power-dissipation (normal operation)	AVDD = DVDD = 3.6V		47.2	66.6	mW
		AVDD = 5.5V, DVDD = 3.6V		86.5	135	

(1) Reference output current is not internally limited.
(2) Digital pins input and output characteristics specified by design; not production tested.

5.6 Timing Requirements

at AVDD and DVDD supply voltage ranges specified in *Recommended Operating Conditions*, VREF = 2.5V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –55°C to 125°C; typical values at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

			MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
f_{CLK}	Serial clock frequency	Half-clock mode			20	MHz
		Full-clock mode			40	
t_{CLK}	Serial clock period	Half-clock mode	50			ns
		Full-clock mode	25			
f_{DATA}	ADC sampling frequency		25		1000	kSPS
t_{DATA}	ADC sampling period ($1/f_{DATA}$)		1			µs
SPI INTERFACE TIMINGS						
t_{CLKL}	Clock low time		11.25			ns
t_{CLKH}	Clock high time		11.25			ns
t_1	CONVST rising to first CLOCK rising edge		12			ns
t_2	CONVST high time		10			ns
		Half-clock mode: timing modes II and IV only			1	t_{CLK}
t_3	RD high time, half-clock mode: timing modes II, IV, SII, and SIV only				1	t_{CLK}
t_{S1}	RD high to CLOCK falling edge setup time		5			ns
t_{H1}	RD high to CLOCK falling edge hold time		5			ns
t_{S2}	Input data valid to CLOCK falling edge setup time		5			ns
t_{H2}	Input data valid to CLOCK falling edge hold time		4			ns

5.7 Switching Characteristics

at AVDD and DVDD supply voltage ranges specified in *Recommended Operating Conditions*, VREF = 2.5V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –55°C to 125°C; typical values at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
t_{CONV}	Conversion time per ADC	Half-clock mode	17.5			t_{CLK}
		Full-clock mode	35			
t_{ACQ}	Acquisition time	Half-clock mode	2			t_{CLK}
		Full-clock mode	4			
t_A	Aperture delay				6	ns
	t_A match			50		ps
	Aperture jitter			50		ps
SPI INTERFACE TIMINGS						
t_{D1}	CONVST rising edge to BUSY high delay[1]	2.3V ≤ DVDD ≤ 3.6V			19	ns
		4.5V ≤ DVDD ≤ 5.5V			16	
t_{D2}	CLOCK 18th falling edge (half-clock mode) or 24th rising edge (full-clock mode) to BUSY low delay	2.3V ≤ DVDD ≤ 3.6V			25	ns
		4.5V ≤ DVDD ≤ 5.5V			20	
t_{D3}	CLOCK rising edge to next data valid delay in half-clock mode	2.3V ≤ DVDD ≤ 3.6V			14	ns
		4.5V ≤ DVDD ≤ 5.5V			12	
t_{H3}	Output data to CLOCK rising edge hold time, half-clock mode		3			ns
t_{D4}	CLOCK falling edge to next data valid delay, full-clock mode				19	ns

5.7 Switching Characteristics (続き)

at AVDD and DVDD supply voltage ranges specified in *Recommended Operating Conditions*, VREF = 2.5V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –55°C to 125°C; typical values at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{H4}	Output data to CLOCK falling edge hold time, full-clock mode		7			ns
t_{D5}	RD falling edge to first data valid	2.3V ≤ DVDD ≤ 3.6V			16	ns
		4.5V ≤ DVDD ≤ 5.5V			12	ns
t_{D6}	$\overline{CS}$ rising edge to SDOx tristate delay				6	ns
INTERNAL VOLTAGE REFERENCE						
t_{REFON}	Reference output settling time	C_{REF} = 22µF		8		ms

(1) Not applicable in auto-sleep power-down mode.

5.8 Timing Diagrams

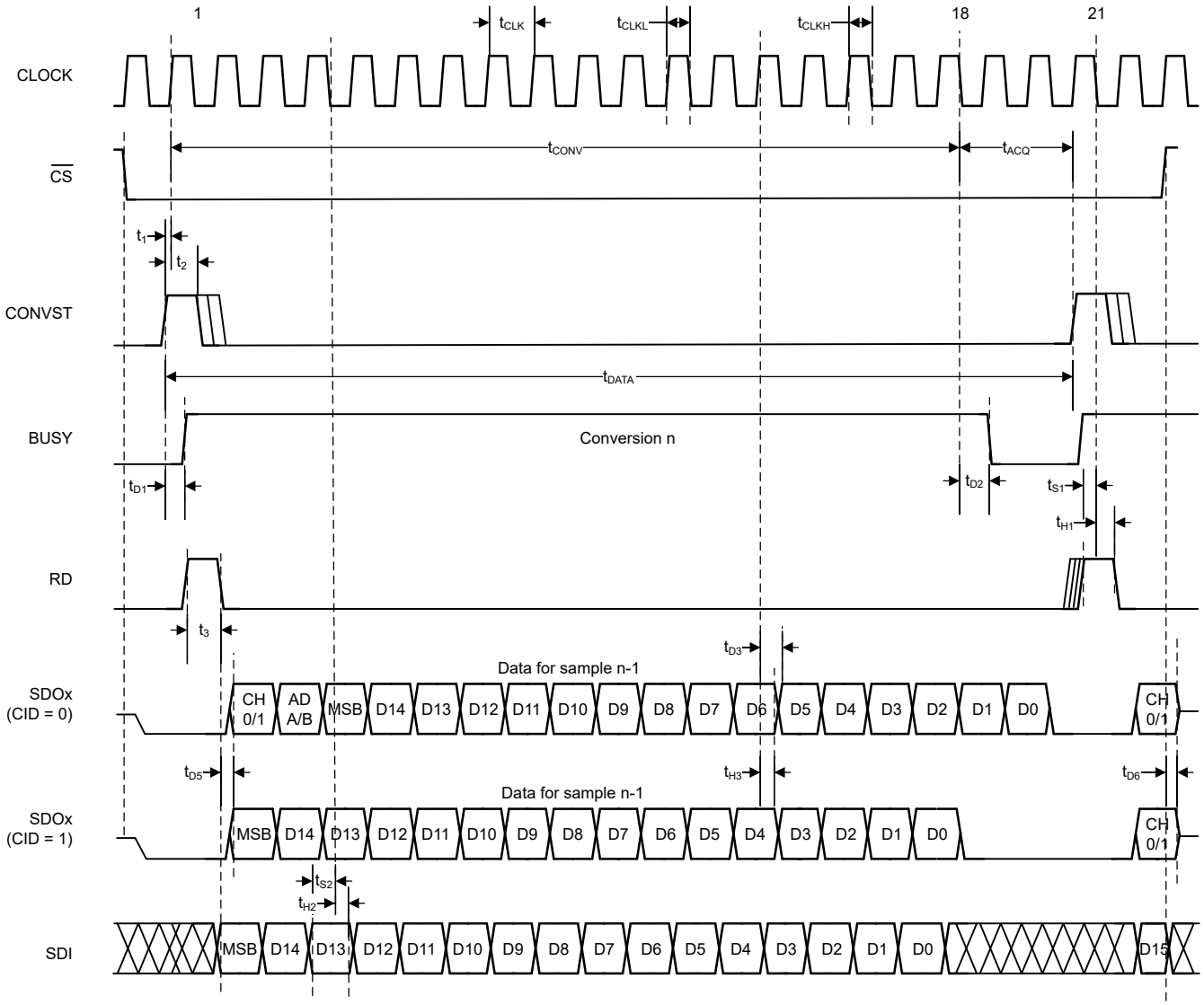


図 5-1. Detailed Timing Diagram: Half-Clock Mode

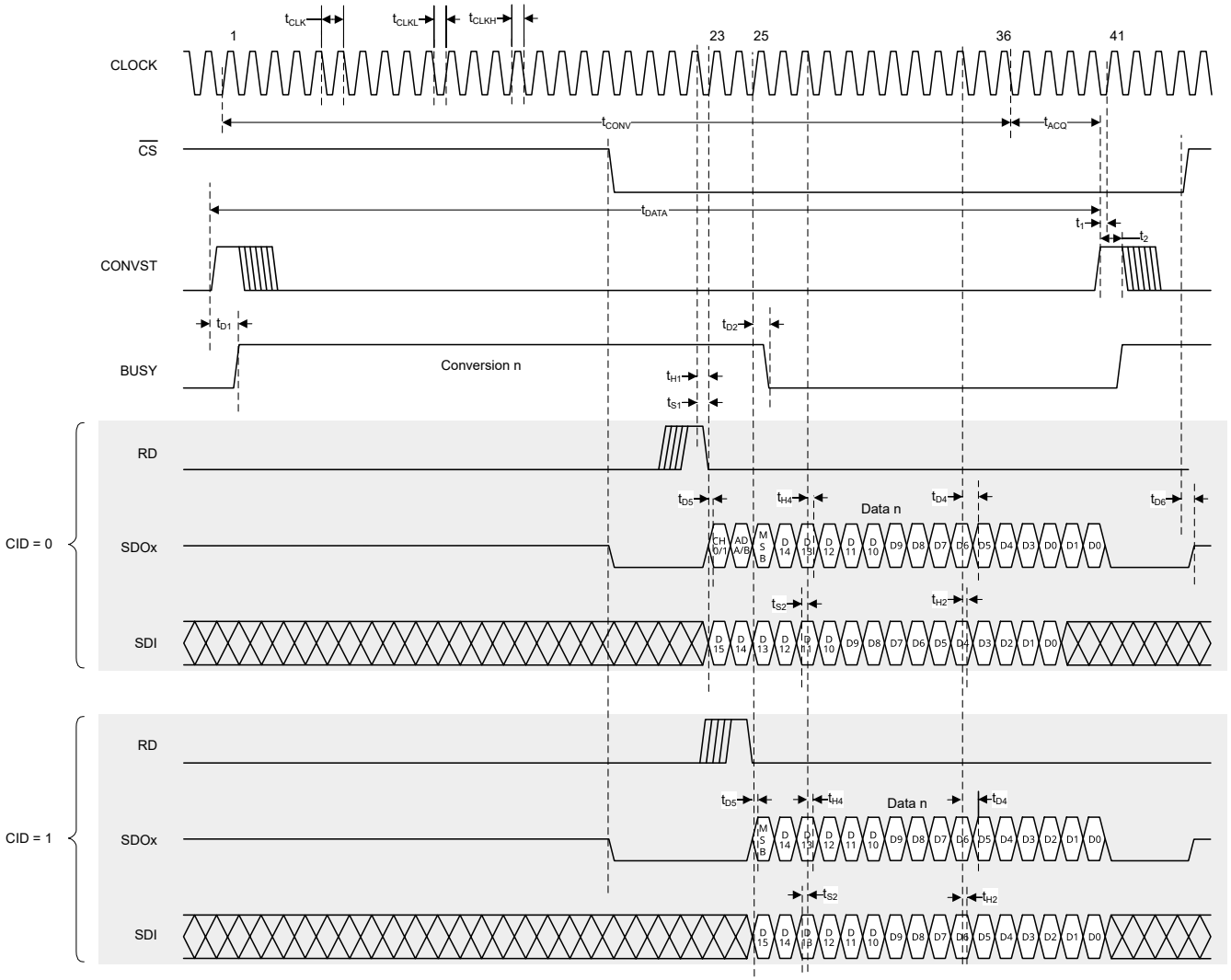


図 5-2. Detailed Timing Diagram: Full-Clock Mode

5.9 Typical Characteristics

at T_A = +25°C, AVDD = 5V, DVDD = 3.3V, V_{REF} = 2.5V (internal), and f_{DATA} = 1MSPS (unless otherwise noted)

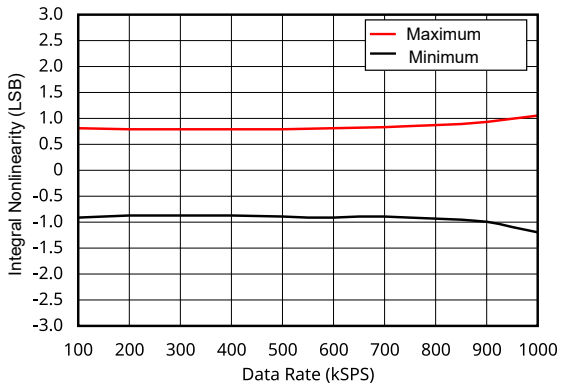


図 5-3. Integral Nonlinearity vs Data Rate

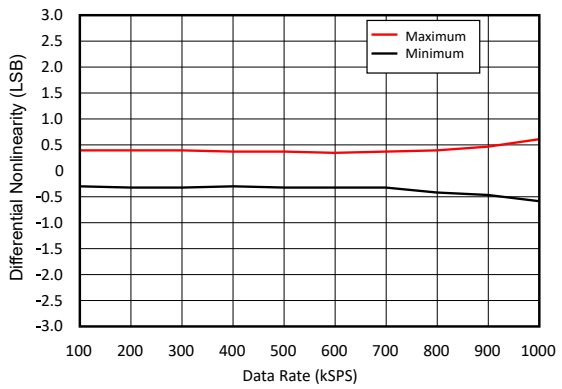


図 5-4. Differential Nonlinearity vs Data Rate

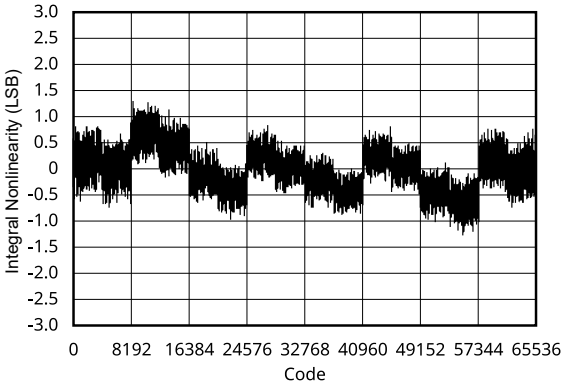


図 5-5. Integral Nonlinearity vs Code

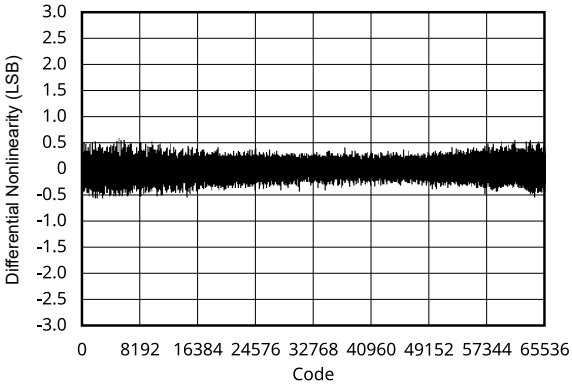


図 5-6. Differential Nonlinearity vs Code

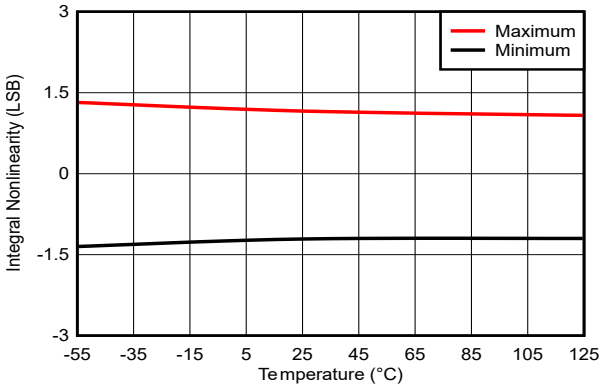


図 5-7. Integral Nonlinearity vs Temperature

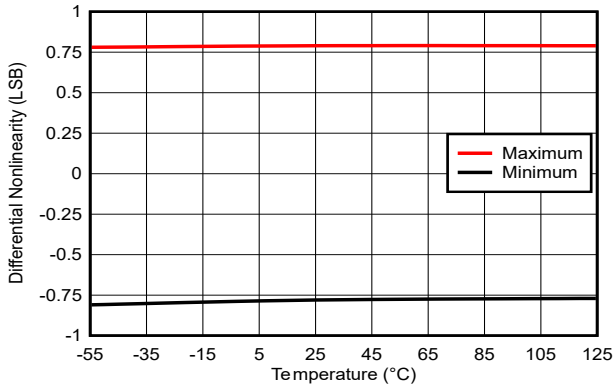


図 5-8. Differential Nonlinearity vs Temperature

5.9 Typical Characteristics (continued)

at T_A = +25°C, AVDD = 5V, DVDD = 3.3V, V_{REF} = 2.5V (internal), and f_{DATA} = 1MSPS (unless otherwise noted)

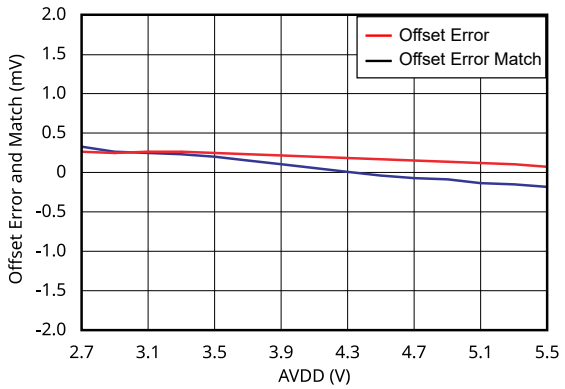


図 5-9. Offset Error and Offset Match vs Analog Supply Voltage

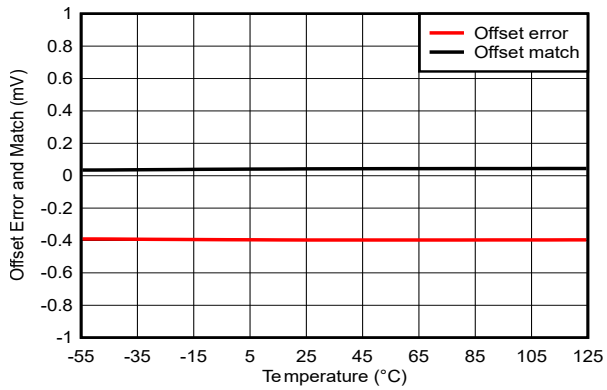


図 5-10. Offset Error and Offset Match vs Temperature

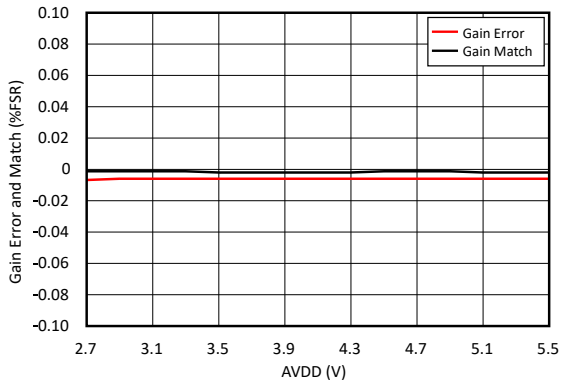


図 5-11. Gain Error and Gain Match vs Analog Supply Voltage

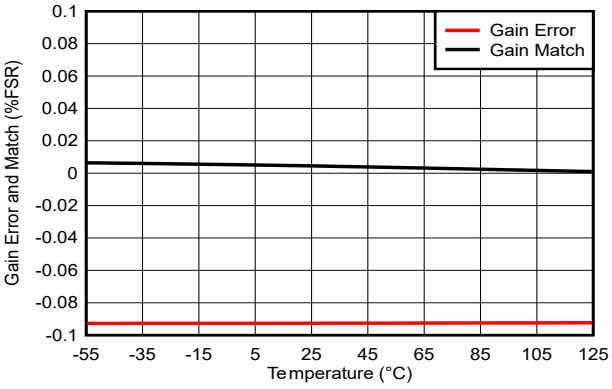


図 5-12. Gain Error and Gain Match vs Temperature

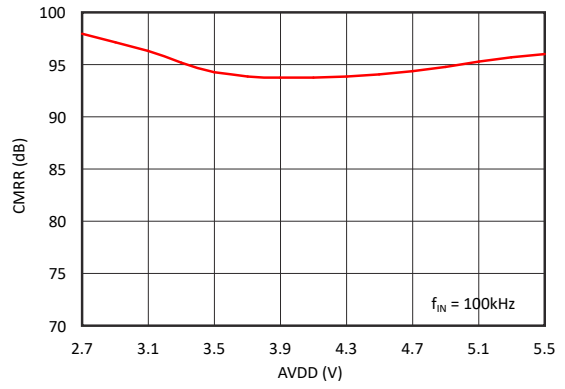


図 5-13. Common-Mode Rejection Ratio vs Analog Supply Voltage

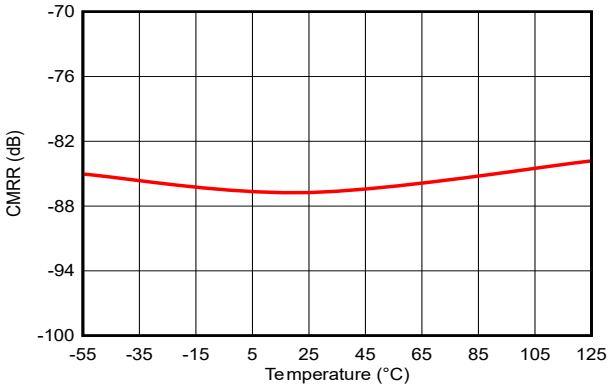


図 5-14. Common-Mode Rejection Ratio vs Temperature

5.9 Typical Characteristics (continued)

at T_A = +25°C, AVDD = 5V, DVDD = 3.3V, V_{REF} = 2.5V (internal), and f_{DATA} = 1MSPS (unless otherwise noted)

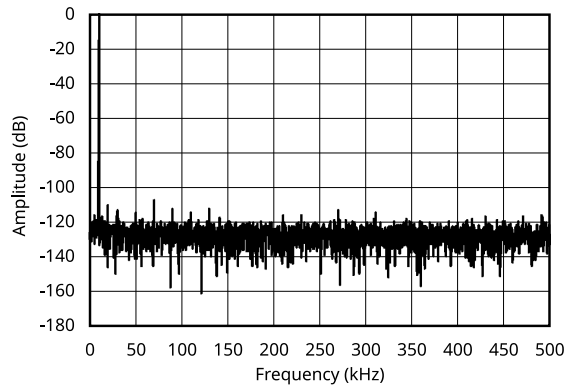


図 5-15. Frequency Spectrum (4096 Point FFT; f_{IN} = 10kHz)

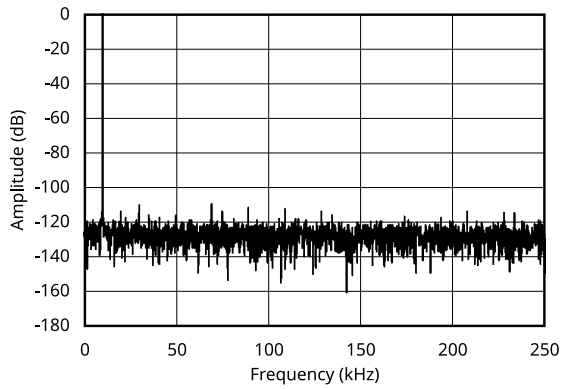


図 5-16. Frequency Spectrum (4096 Point FFT; f_{IN} = 10kHz, f_{SAMPLE} = 0.5MSPS)

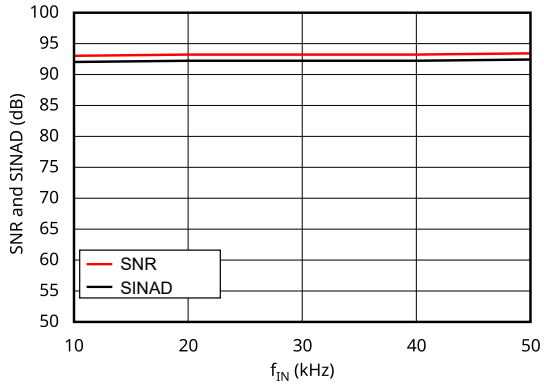


図 5-17. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

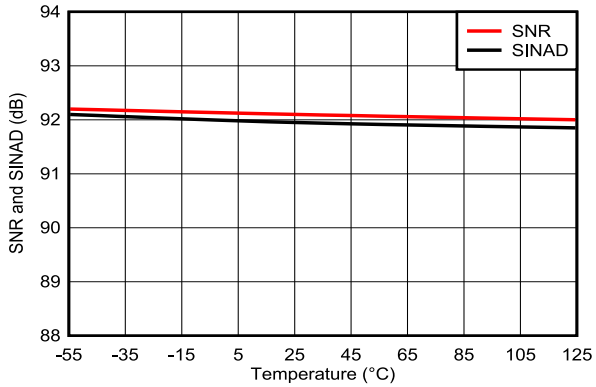


図 5-18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

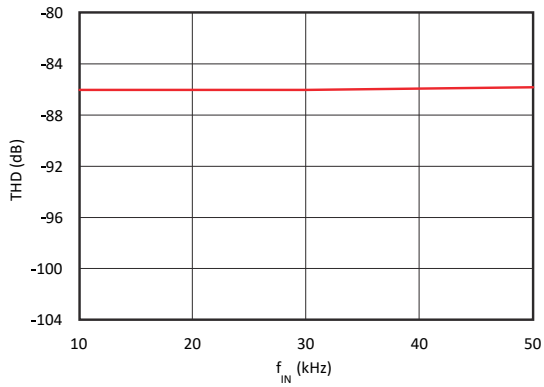


図 5-19. Total Harmonic Distortion vs Input Signal Frequency

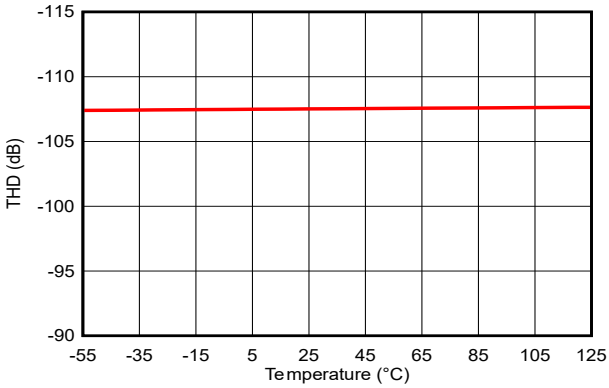


図 5-20. Total Harmonic Distortion vs Temperature

5.9 Typical Characteristics (continued)

at T_A = +25°C, AVDD = 5V, DVDD = 3.3V, V_{REF} = 2.5V (internal), and f_{DATA} = 1MSPS (unless otherwise noted)

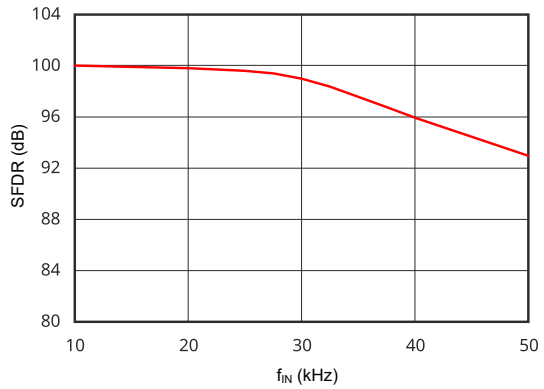


図 5-21. Spurious-Free Dynamic Range vs Input Signal Frequency

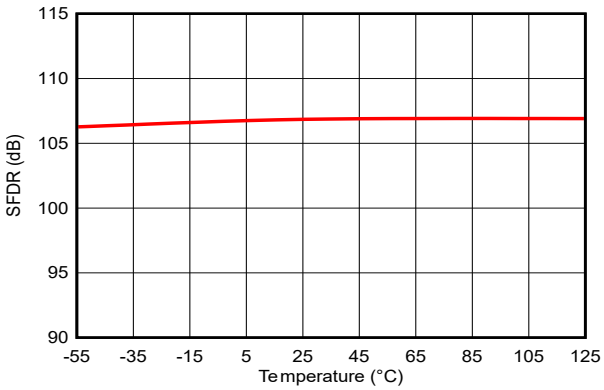


図 5-22. Spurious-Free Dynamic Range vs Temperature

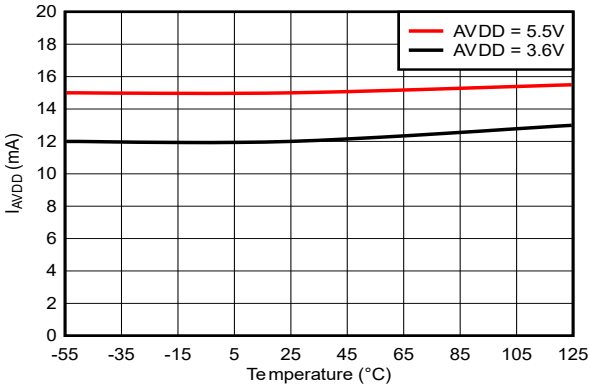


図 5-23. Analog Supply Current vs Temperature

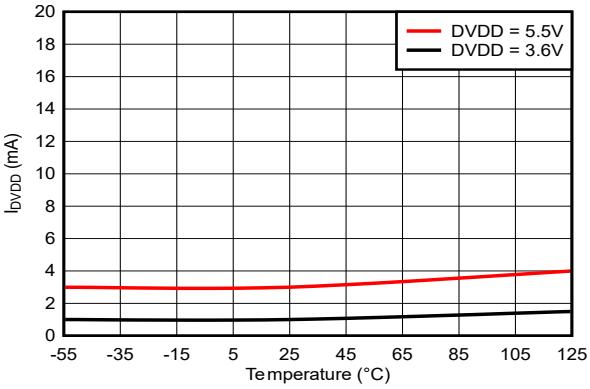


図 5-24. Digital Supply Current vs Temperature

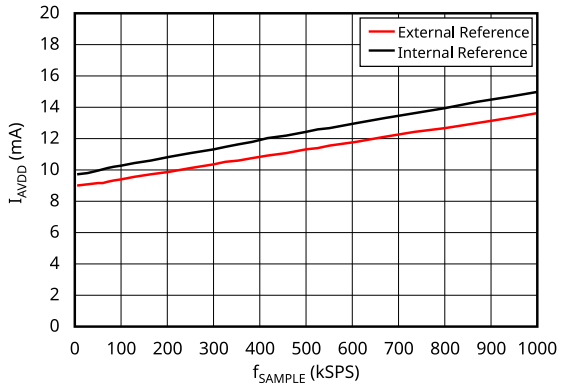


図 5-25. Analog Supply Current vs Data Rate

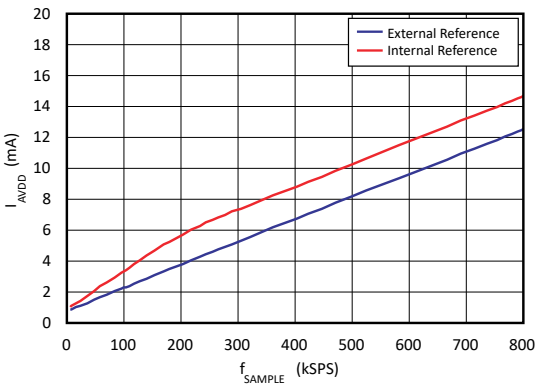


図 5-26. Analog Supply Current vs Data Rate (Auto-Sleep Mode)

6 Detailed Description

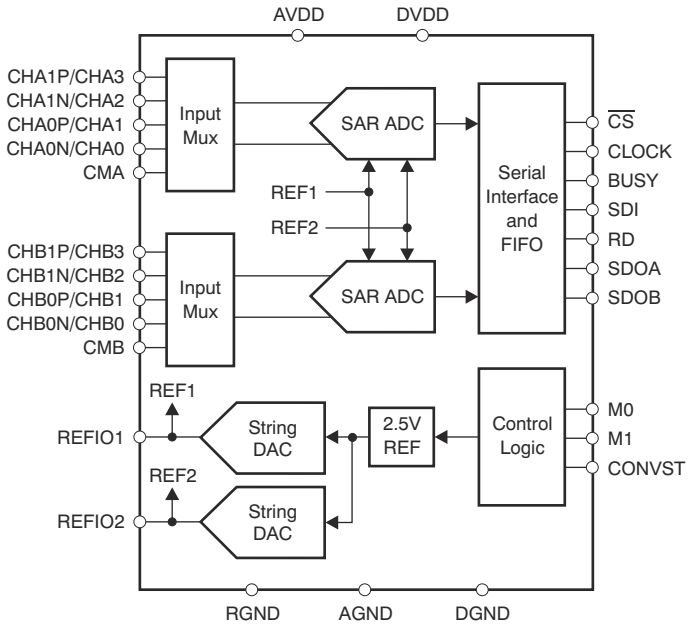
6.1 Overview

The ADC168M102R-SEP contains two 16-bit analog-to-digital converters (ADCs), that operate based on the successive approximation register (SAR) principle. These ADCs sample and convert simultaneously. Conversion time is potentially as low as 875ns. Adding a 100ns acquisition time, and a 25ns margin for propagation delay and CONVST pulse generation, results in a 1MSPS maximum conversion rate.

Each ADC has a fully differential 2:1 multiplexer front-end. In many common applications, all negative input signals remain at the same constant voltage (for example, 2.5V). For these applications, use the multiplexer in a pseudo-differential 4:1 mode. In this mode, the CM*x* pins function as common-mode pins and all four analog inputs are referred to the corresponding CM*x* pin.

The ADC168M102R-SEP also includes a 2.5V internal reference. This reference drives two independently programmable, 10-bit digital-to-analog converters (DACs). Thus, allowing the voltage at each REFIO*x* pin to be adjusted through the internal REFDAC*x* registers in 2.44mV steps. A low-noise, unity-gain operational amplifier buffers each DAC output and drives the REFIOx pin.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog

This section discusses the analog input circuit, the ADCs, and the reference design of the device.

6.3.1.1 Analog Inputs

As shown in 図 6-1, each ADC is fed by an input multiplexer. Each multiplexer is used in either a fully differential 2:1 configuration (表 6-1) or a pseudo-differential 4:1 configuration (表 6-2).

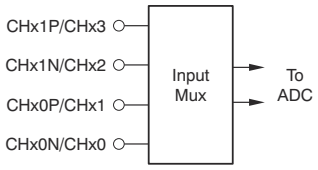


図 6-1. Input Multiplexer Configuration

Use either the external M0 pin or the C[1:0] bits in the Configuration (CONFIG) register for channel selection in fully differential mode. In pseudo-differential mode, channel selection is performed with the SEQFIFO register. In either mode, changing the multiplexer settings impacts the conversion started with the next CONVST pulse.

表 6-1. Fully Differential 2:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	x	CHx0P	CHx0N
1	x	CHx1P	CHx1N

表 6-2. Pseudo-Differential 4:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0	CMx/REFIOx
0	1	CHx1	CMx/REFIOx
1	0	CHx2	CMx/REFIOx
1	1	CHx3	CMx/REFIOx

The input path for the converter is fully differential and provides a good common-mode rejection of 92dB at 100kHz. The high CMRR also helps suppress noise in harsh industrial environments.

Each 40pF sample-and-hold capacitor (C_S in 図 6-2) is connected through switches to the multiplexer output. Opening the switches holds the sampled data during the conversion process. After the conversion completes, both capacitors are precharged for the duration of one clock cycle to the voltage present at the REFIO*x* pin. After precharging, the multiplexer outputs are connected to the sampling capacitors again. The voltage at the analog input pin is usually different from the reference voltage. Therefore, charge the sample capacitors to within one-half LSB for 16-bit accuracy during the acquisition time t_{ACQ} (see 図 5-1 and 図 5-2).

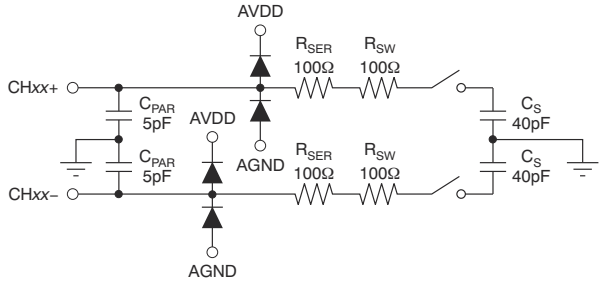


図 6-2. Equivalent Analog Input Circuit

Acquisition is indicated with the BUSY signal low. Acquisition starts by closing the input switches (after finishing the previous conversion and precharging) and finishes with the rising edge of the CONVST signal. If the device operates at full speed, the acquisition time is typically 100ns.

As shown in, 式 1 calculate the minimum –3dB bandwidth of the driving operational amplifier with *n* = 16 for the resolution of the ADC168M102R-SEP:

$$f_{-3dB} = \frac{\ln(2)(n + 1)}{2\pi t_{ACQ}} \quad (1)$$

With t_{ACQ} = 100ns, the minimum bandwidth of the driving amplifier is 19MHz for the ADC168M102R-SEP. The required bandwidth is potentially lower if the application allows a longer acquisition time.

A gain error occurs if a given application does not fulfill the settling requirement in 式 1. However, linearity and THD are not directly affected as a result of precharging the capacitors.

The OPA365 from Texas Instruments is recommended as a driver. In addition to offering the required bandwidth, the OPA365 also provides a low offset and excellent THD performance (see the *Application and Implementation* section).

The phase margin of the driving operational amplifier is usually reduced by the ADC sampling capacitor. A resistor placed between the capacitor and the amplifier limits this effect. Therefore, place an internal 100Ω resistor (R_{SER}) in series with the switch. The switch resistance (R_{SW}) is typically 100Ω; see 図 6-2).

An input driver is not required if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of 式 2:

$$R_{SOURCE} < \frac{t_{ACQ}}{C_S \ln(2)(n + 1)} - (R_{SER} + R_{SW}) \quad (2)$$

where:

- *n* = 16 is the ADC168M102R-SEP resolution
- C_S = 40pF sample capacitance
- R_{SER} = 100Ω input resistor value
- R_{SW} = 100Ω switch resistance value

With t_{ACQ} = 100ns, make sure the maximum source impedance is less than 12Ω for the ADC168M102R-SEP. The source impedance is potentially higher if the ADC is used at a lower data rate.

The differential input voltage range of the ADC is $\pm V_{REF}$, the voltage at the selected REFIO*x* pin.

Keep the voltage for all inputs within the 0.3V limit below AGND and above AVDD. Do not allow dc current to flow through the inputs. Exceeding these limits causes the internal ESD diodes to conduct, leading to increased leakage current that potentially damages the device. Current is only necessary to recharge the sample-and-hold capacitors.

Directly tie any unused inputs to AGND or RGND without the need of a pulldown resistor.

6.3.1.2 Analog-to-Digital Converters (ADCs)

The ADC168M102R-SEP includes two 1MSPS, 16-bit SAR ADCs that include sample-and-hold, respectively; see the *Functional Block Diagram*.

6.3.1.3 CONVST

The analog inputs are held with the CONVST rising edge (conversion start) signal. The setup time of CONVST referred to the next CLOCK rising edge (system clock) is 12ns (minimum). The conversion automatically starts with the rising CLOCK edge. Do not issue a rising CONVST edge during a conversion (that is, when BUSY is high).

RD (read data) and CONVST are shorted to minimize necessary software and wiring. The RD signal is triggered by the device on the falling CLOCK edge. Therefore, activate the combined signals with the rising CLOCK edge. The conversion then starts with the subsequent rising CLOCK edge. In modes with only SDOA active, the maximum length of the combined RD and CONVST signal is one clock cycle if half-clock timing is used. These modes are II, IV, SII, and SIV.

If CONVST and RD are combined, make sure $\overline{CS}$ is low whenever a new conversion starts. However, this condition is not required if RD and CONVST are controlled separately. If the first-in, first-out (FIFO) is used, control CONVST separately from RD.

After completing a conversion, the sample capacitors are automatically precharged to the reference voltage value used to significantly reduce crosstalk among the multiplexed input channels.

6.3.1.4 CLOCK

The ADC168M102R-SEP uses an external clock with an allowable frequency range that depends on the mode being used. By default (after power-up), the ADC operates in half-clock mode that supports a clock ranging from 0.5MHz to 20MHz. In full-clock mode, the ADC requires a clock ranging from 1MHz to 40MHz. For maximum data throughput, keep the clock signal continuously running. However, when using the device in burst mode, keep the clock held static low or high when read access completes and before starting a new conversion.

Keep the CLOCK duty cycle at 50%. However, the device functions properly with a duty cycle between 30% and 70%.

6.3.1.5 RESET

The ADC168M102R-SEP features an internal power-on reset (POR) function. A user-controlled reset is also issued using the SDI register bits A[3:0] (see the *Digital* section).

6.3.1.6 REFIO*x*

The ADC168M102R-SEP includes a low-drift, 2.5V internal reference source. This source feeds two, 10-bit string DACs that are controlled through registers. As a result of this architecture, the reference voltages at REFIO*x* are programmable in 2.44mV steps and adjusted to application requirements without additional external components. The actual output voltage is calculated using 式 3, with *code* being the decimal value of the REFDACx register content:

$$V_{REF} = \frac{2.5V(code + 1)}{1024} \quad (3)$$

The reference DAC has a fixed transition at code 508 (0x1FC). At this code, the DAC shows a jump of up to 10mV in the transfer function. 表 6-3 lists some examples of internal reference DAC settings. However, to provide proper performance, do not program the REFDACx output voltage below 0.5V.

表 6-3. REFDACx Setting Examples

VREFOUT (NOM)	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.5000V	205	00 1100 1101	0CDh
1.2429V	507	01 1111 1100	1FBh
1.2427V	508	01 1111 1101	1FCh
2.5000V	1023	11 1111 1111	3FFh

A minimum of 22µF capacitance is required on each REFIOx output to keep the references stable. The settling time is 8ms (maximum) with the reference capacitor connected. Smaller reference capacitance values reduce the DNL, INL, and ac performance of the device. By default, both reference outputs are disabled and the respective values are set to 2.5V after power-up.

For applications that use an external reference source, the internal reference is disabled (default) using the RPD bit in the CONFIG register (see the *Digital* section). The REFIO*x* pins are directly connected to the ADC; therefore, the internal switching generates spikes at this pin. Thus, use an external 22µF capacitor to the analog ground (AGND) to stabilize the reference input voltage.

Leave disabled REFIO*x* pins floating or directly tied to AGND or RGND.

Each reference DAC output is individually selected as a source for each channel input using the R*xx* bits in the REFCM register. 図 6-3 shows a simplified block diagram of the internal circuit.

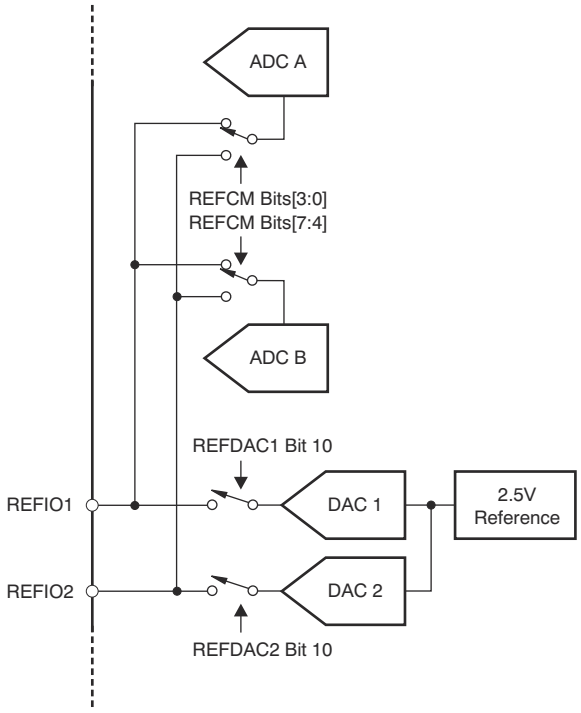


図 6-3. Reference Selection Circuit

6.3.2 Digital

This section reviews the timing and control of the serial interface.

The ADC168M102R-SEP offers a set of internal registers that allows the control of several device features and modes. See the *Register Map* section for details. 表 6-4 lists the supported device operating modes.

表 6-4. Supported Operating Modes

INPUT SIGNAL TYPE	MANUAL CHANNEL SELECTION	AUTOMATIC CHANNEL SELECTION
Fully differential (PDE bit = 0)	Operating modes: I, II, and special mode II Channel information is selectable through the CID bit FIFO: Not available	Operating modes: III, IV and special mode IV Channel information is selectable through the CID bit. FIFO: Available in mode III and special mode IV. When used, a single read pulse allows reading of all data.
Pseudo-differential (PDE bit = 1)	Operating modes: I, II and special mode II Channel information is selectable through the CID bit FIFO: Not available	Operating modes: III and special mode IV Channel information is not available (CID bit forced to 1). FIFO: Available in mode III and special mode IV. When used, a single read pulse allows reading of all data. Pseudo-differential sequencer is enabled.

6.3.2.1 Mode Selection Pins M0 and M1

As shown in 表 6-5, configure the ADC168M102R-SEP to four different operating modes using the M0 and M1 mode pins.

表 6-5. M0, M1 Truth Table

M0	M1	CHANNEL SELECTION	SDO*x* USED
0	0	Manual (through SDI)	SDOA and SDOB
0	1	Manual (through SDI)	SDOA only
1	0	Automatic	SDOA and SDOB
1	1	Automatic	SDOA only

The M0 pin sets either manual or automatic channel selection. In manual mode, the CONFIG register bits C[1:0] select between channels CH*x*0 and CH*x*1. In automatic mode, the CONFIG register bits C[1:0] are ignored and channel selection is controlled by the device after each conversion. The automatic channel selection is only performed on fully differential inputs in this case. For pseudo-differential inputs, the internal sequencer controls the input multiplexer.

The M1 pin selects how serial data are transmitted. Serial data are transmitted simultaneously on both SDOA and SDOB outputs for each channel (respectively), or only the SDOA output transmitts data from both channels. See 図 6-5 through 図 6-10 and the associated text for more information.

Additionally, the SDI pin controls device functionality through the internal register; see the *Register Map* section for details.

6.3.2.2 Half-Clock Mode (Default Mode After Power-Up and Reset)

The ADC168M102R-SEP powers up in half-clock mode. In this mode, the ADC requires at least 20 CLOCKs for a complete conversion cycle, including the acquisition phase. The conversion result is only read during the next conversion cycle. The first output bit is available with the falling RD edge, and the following output data bits are refreshed with the CLOCK rising edge.

6.3.2.3 Full-Clock Mode (Allowing Conversion and Data Readout Within 1µs, Supported In Dual Output Modes)

The full-clock mode allows converting data and reading the result within 1µs. The entire cycle requires 40 CLOCKs. The first output bit is available with the falling RD edge. The following output data bits are refreshed with the falling edge of the CLOCK in this mode.

Use the full-clock mode with a 4.5V to 5.5V AVDD power supply range and a 2.3V to 3.6V DVDD digital supply range. The internal FIFO is disabled in full-clock mode.

6.3.2.4 2-Bit Counter

This device offers a selectable 2-bit counter (activated using the CE bit in the CONFIG register) that is a useful feature in safety applications. The counter value automatically increments whenever a new conversion result is stored in the output register, indicating a new value. The counter default value after power-up is 01 (followed by 10, 11, 00, 01, and so on); see 図 7-3. The counter value increments only when new conversion results are transferred to the output register. Thus, this counter verifies the ADC performed a conversion and the data read are the new conversion result (not an old result read multiple times).

6.4 Device Functional Modes

6.4.1 Power-Down Modes and Reset

This device has a comprehensive built-in power-down feature. There are three power-down modes: power-down, sleep, and auto-sleep. All three power-down modes are activated by write access completion, during which the related bits are asserted (PD[1:0]). All modes are deactivated by deasserting the respective bits in the CONFIG register. The content of the CONFIG register is not affected by any of the power-down modes. Any ongoing conversion is finished before entering any of the power-down modes. 表 6-6 summarizes the differences among the three power-down modes.

表 6-6. Power-Down Modes

POWER-DOWN MODE	POWER-DOWN CURRENT	POWER-DOWN ENABLED BY	POWER-DOWN START BY	DELAY TIME TO POWER-DOWN	NORMAL OPERATION BY	WAKEUP TIME	POWER-DOWN DISABLED BY
Power-down	5µA	PD[1:0] = 01	Write access completed	20µs	PD[1:0] = 00	8ms	PD[1:0] = 00
Sleep	1.2mA (3.6V)	PD[1:0] = 10	Write access completed	10µs	PD[1:0] = 00	7 or 14 CLOCK cycles	PD[1:0] = 00
Auto-sleep	1.2mA (3.6V)	PD[1:0] = 11	Each end of conversion	10µs	CONVST pulse	7 or 14 CLOCK cycles	PD[1:0] = 00

6.4.1.1 Power-Down Mode

In power-down mode (PD[1:0] = 01), all functional blocks except the digital interface are disabled. In this mode, the current demand is reduced to 5µA within 20µs. The wakeup time from power-down mode is 8ms when using a reference capacitor of 22µF. The device goes into power-down mode after completing any ongoing conversions.

6.4.1.2 Sleep Mode

In sleep mode (PD[1:0] = 10), the device reduces the current demand to approximately 0.9mA within 10µs. The device goes into sleep mode after completing any ongoing conversions.

6.4.1.3 Auto-Sleep Mode

Auto-sleep mode is almost identical to sleep mode. The only differences are the method of activating the mode and waking up the device. The CONFIG register bits PD[1:0] = 11 only enable or disable this feature. If auto-sleep mode is enabled, the device automatically turns off the biasing after finishing a conversion; thus, the end of conversion actually activates auto-sleep mode. If sequencer mode is used and individual conversion start pulses are chosen (S1 = 0), the device automatically powers down after each conversion. If a single CONVST pulse starts the sequence (S1 = 1), power-down is activated when the entire sequence completes.

The device wakes up with the next CONVST pulse. However, the analog input is held in sample mode for another seven clock cycles in half-clock mode, or 14 clock cycles in full-clock mode. Thereafter (see 図 6-4), the actual conversion starts (BUSY goes high). This time is required to settle the internal circuitry to the required voltage levels. The conversion result is delayed in auto-sleep mode; see 図 6-10.

In this mode, the current demand is reduced to approximately 1.2mA within 10µs.

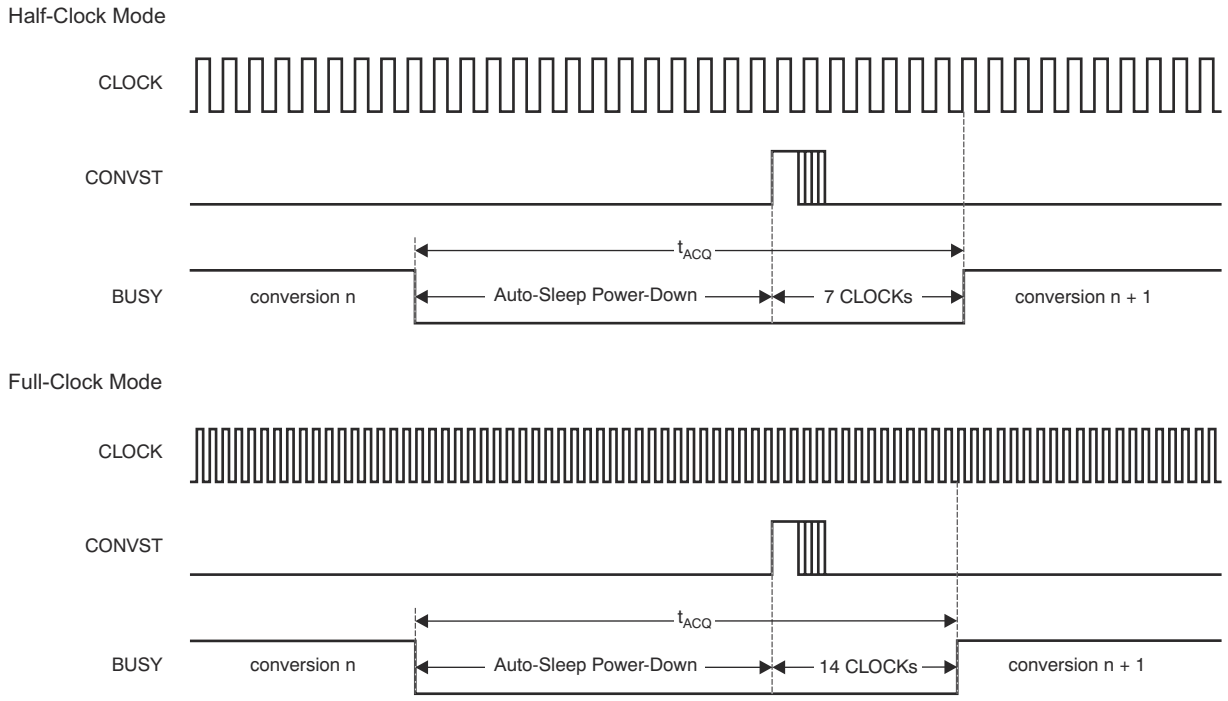


図 6-4. Actual Conversion Start In Auto-Sleep Mode

6.4.1.4 Reset

To issue a device reset, generate an RD pulse and a control word containing A[3:0] = 0100. With the completion of this write access, the entire device including the serial interface is forced into reset, interrupting any ongoing conversions. The input is set to acquisition mode, and the register contents return to the default values. After approximately 20ns, the serial interface becomes active again. The device also supports an automatic power-up reset (POR) that provides proper (default) device settings.

6.5 Programming

6.5.1 Read Data Input (RD)

The RD input controls the serial data outputs SDO*x*. The falling edge of the RD pulse triggers the output of the first bit of the output data. When CID is 0, the first bit of output data on SDOx is the analog input channel indicator. When CID is 1, the first bit of output data on SDOx is the conversion result MSB, or the 15th bit of the selected register. This bit is followed by output bits that update with the CLOCK rising edge in half-clock mode, or the CLOCK falling edge in full-clock mode.

The RD input is controlled separately or in combination with the CONVST input (see 図 8-2 for a detailed timing diagram). If RD is controlled separately, issue RD whenever a conversion process is finished (that is, after the falling BUSY edge). However, to achieve the maximum data rate, read the conversion results during an ongoing conversion. In half-clock mode, do not issue the RD pulse between the 16th and 19th clock cycle after starting the conversion. In full-clock mode, do not issue the RD pulse between the 34th and 36th clock cycle in full-clock mode after starting the conversion.

If a read access is repeated without issuing a new conversion, the result of the last conversion is presented on the outputs again. Only perform a repeated readout when BUSY is low.

In full-clock mode, only the first read access delivers the correct channel information when the following readouts contain invalid channel details. Correct channel information occurs when CID is 0 in the CONFIG register. The channel information is corrected with the next conversion.

Read access to verify the content of the internal registers is described in the *Register Map* section.

6.5.2 Serial Data Outputs (SDOx)

The following sections explain the different modes of operation in detail.

As shown in 表 6-7, the digital output code format of the ADC168M102R-SEP is binary two's complement.

Consider both detailed timing diagrams illustrated in 図 5-1 and 図 5-2. For maximum data throughput, the description and diagrams given in this document assume that the CONVST and RD pins are tied together. See 図 8-2 for timing details in this case. These pins are also able to be controlled independently.

表 6-7. Output Data Format

DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE	INPUT VOLTAGE AT CH*xx*P (CH*xx*N = V_{REF} = 2.5V)	BINARY CODE	HEXADECIMAL CODE
Positive full-scale	V_{REF}	5V	0111 1111 1111 1111	7FFF
Midscale	0V	2.5V	0000 0000 0000 0000	0000
Midscale – 1 LSB	$–2V_{REF}$ / resolution	2.499924V	1111 1111 1111 1111	FFFF
Negative full-scale	$–V_{REF}$	0V	1000 0000 0000 0000	8000

6.5.2.1 Mode I

With the M0 and M1 pins both set to 0, the device enters manual channel-control operation and outputs data on both SDOA and SDOB, accordingly. The SDI pin switches between the channels, as shown in the corresponding timing diagrams. A conversion is initiated by bringing CONVST high.

With the rising CONVST edge, the device switches asynchronously to the external CLOCK from sample to hold mode. The BUSY output pin goes high and remains high for the duration of the conversion cycle. On the falling edge of the second CLOCK cycle, the device latches in the channel for the next conversion cycle. This latching depending on the status of the CONFIG register bits C[1:0]. Bring $\overline{CS}$ low to enable both serial outputs. Data are valid on the falling edge of every 20 clock cycles per conversion. The first two bits are set to 0. As shown in 図 6-5, the subsequent data contain the 16-bit conversion result (the most significant bit is transferred first), with trailing zeroes.

This mode is used for fully- or pseudo-differential inputs; in both cases, channel information bits are 00 if the CID is 0. The FIFO is not available in this mode.

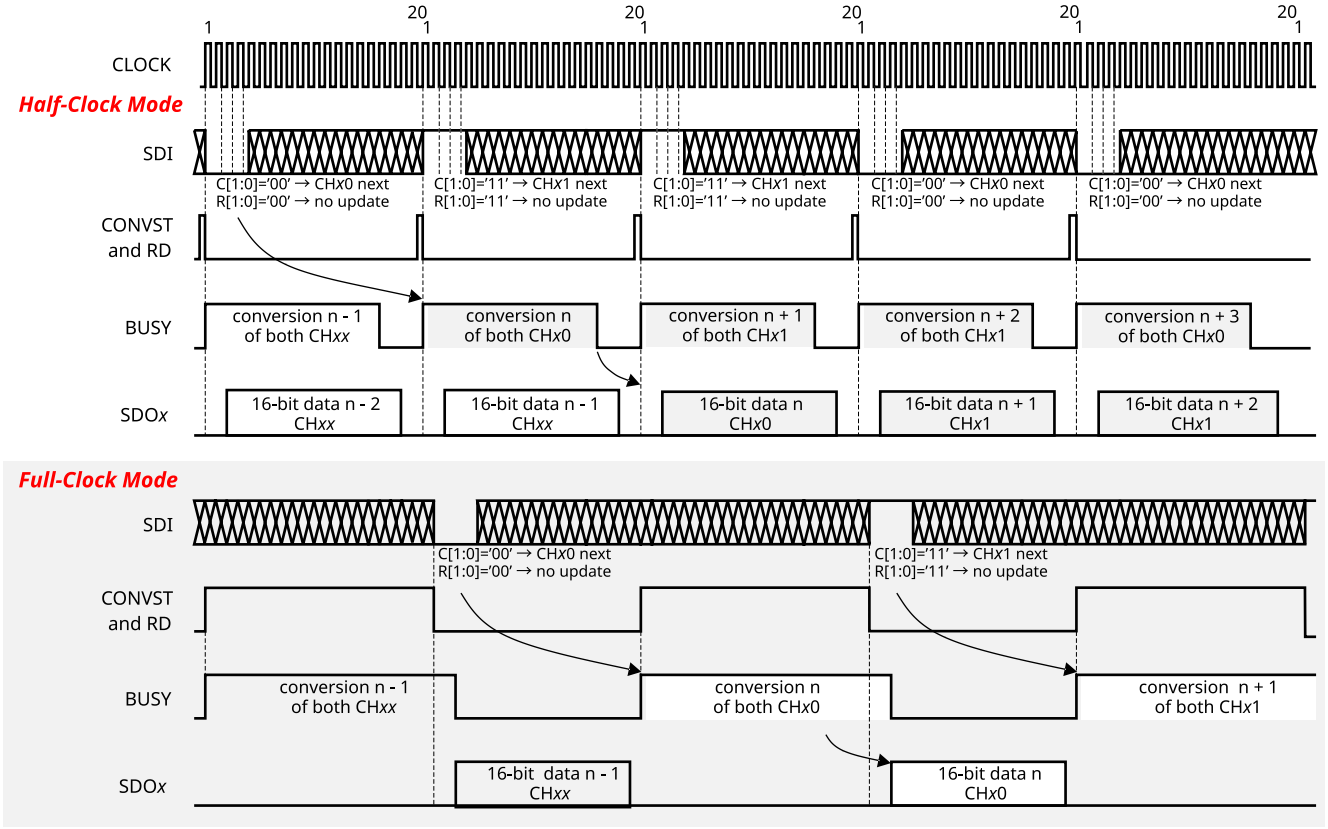


図 6-5. Mode I Timing (M0 = 0, M1 = 0, PDE = 0, CID = 1, Fully Differential Example)

6.5.2.2 Mode II (Half-Clock Mode Only)

With M0 = 0 and M1 = 1, the ADC168M102R-SEP also operates in manual channel-control mode. In this mode, the device outputs data on the SDOA pin only when SDOB is set to high impedance. All other pins function in the same manner as in mode I.

In half-clock mode, the device requires 2µs to perform a complete read cycle. This requirement is because 40 clock cycles are needed to output the results from both ADCs (instead of 20 cycles if M1 = 0). As shown in 図 6-6, if the CONVST signal is issued every 1.0µs (required for the RD signal) as in mode I, ignore every second pulse. Make sure the CONVST and RD signals are not be longer than one clock cycle to provide proper functionality and avoid output data corruption.

Full-clock mode is not supported in this operational mode.

The output data consist of a 0, an ADC indicator, and 16 bits of conversion result with any trailing zeroes. The ADC indicator is 0 for CHA*x* or 1 for CHB*x*.

This mode is used for fully- or pseudo-differential inputs. Channel information is valid in fully differential mode only if CID is 0. CID contains correct ADC information when the channel bit is invalid in pseudo-differential mode. The FIFO is not available in this mode.

Changes to the FE, SR, PDE, and CID register bits are active starting from the next conversion with a delay of one read access.

Update the register settings using every other RD pulse. As shown in 図 6-6, align these pulses either with the one starting the conversion or the one to read the conversion results of channel B.

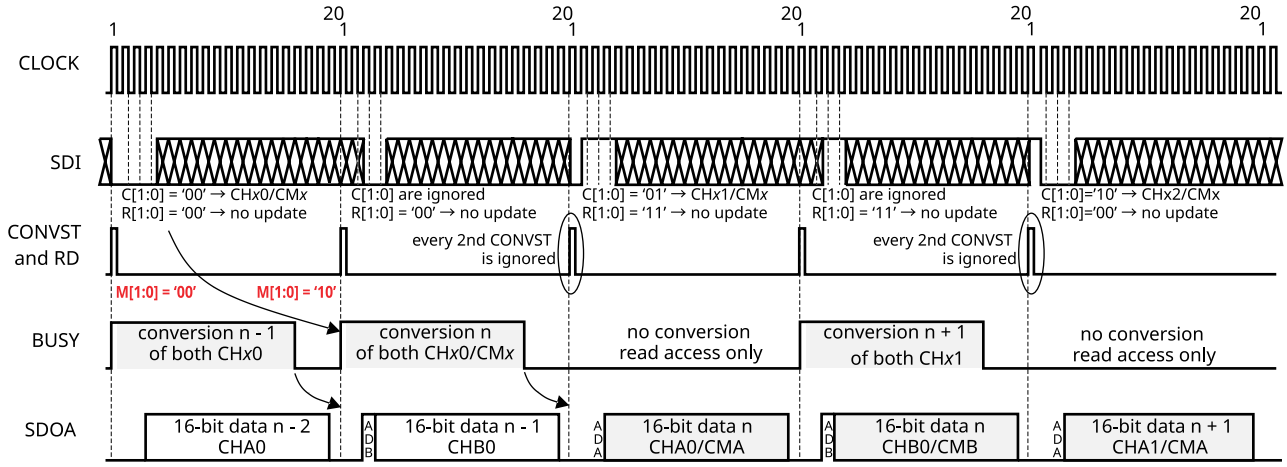


図 6-6. Mode II Timing (M0 = 0, M1 = 1, PDE = 0, CID = 0, Pseudo-Differential Example)

6.5.2.3 Special Read Mode II (Half-Clock Mode Only)

For mode II, a special read mode is available where a single RD pulse triggers both data results to be read out. 図 6-7 shows a timing diagram of this mode. To activate this mode, set the SR bit in the CONFIG register to 1 (see 表 7-1). The CONVST and RD pins are still tied together but are issued every 40 CLOCK cycles instead of 20. Output data are presented on SDOA only when SDOB is held in tri-state.

Make sure the RD signal in this mode is not longer than one clock cycle to avoid corruption of output data.

This special mode is used for fully- or pseudo-differential inputs. Channel information is valid in fully differential mode only if the CID is 0. The CID contains correct ADC information when the channel bit is invalid in pseudo-differential mode. The FIFO is not available in this mode.

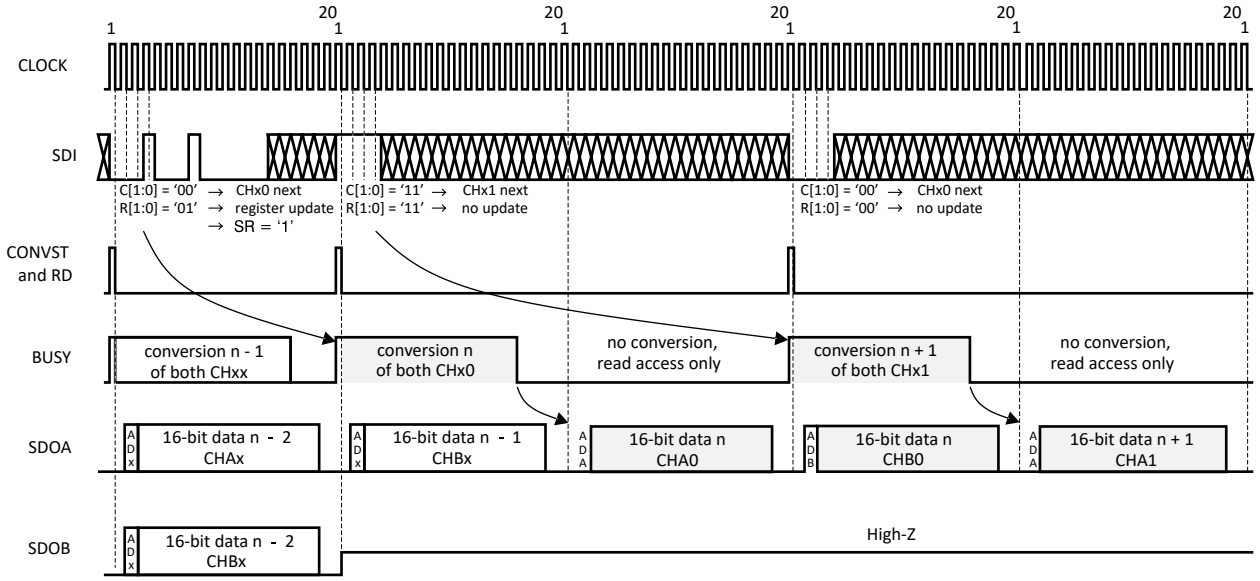


図 6-7. Special Read Mode II Timing Diagram (M0 = 0, M1 = 1, PDE = 0, SR = 1, CID = 0, Fully Differential Example)

6.5.2.4 Mode III

With M0 = 1 and M1 = 0, the device automatically cycles between the differential inputs (CONFIG register bits C[1:0] are ignored). As shown in 図 6-8, this cycling occurs when offering the conversion result of CHA*x* on SDOA and the conversion result of CHB*x* on SDOB.

Output data consist of a channel indicator, followed by a 0 and 16 bits of conversion result along with any trailing zeroes. The channel indicator is 0 for CH*x*0, or 1 for CH*x*1.

Use this mode fully- or pseudo-differential inputs (in pseudo-differential mode the sequencer controls the input multiplexer). Channel information is available in fully differential mode only if CID is 0 (CID is forced to 1 in pseudo-differential mode).

The internal FIFO is available in this mode; when used, a single read pulse allows all stored conversion data to be read. Make sure the FIFO is completely filled when used for the first time to provide proper functionality.

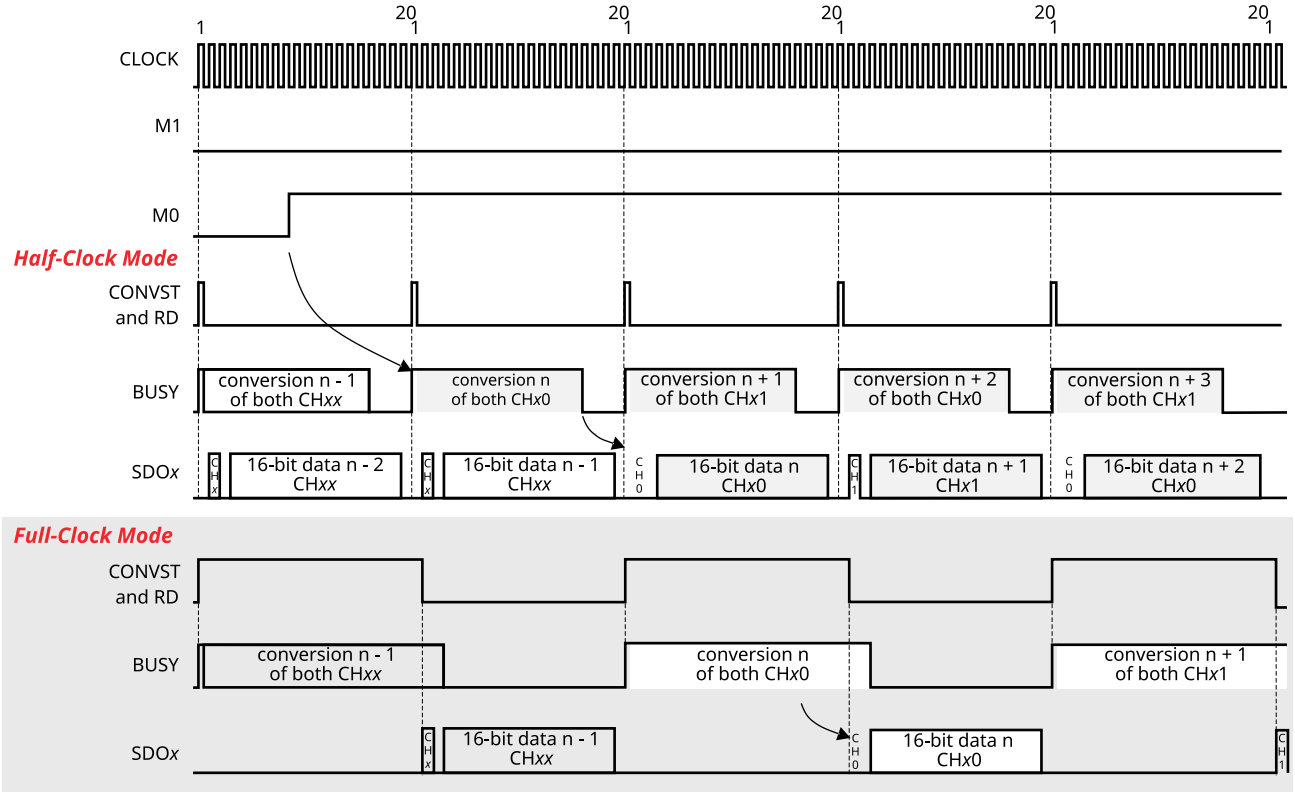


図 6-8. Mode III Timing (M0 = 1, M1 = 0, PDE = 0, CID = 0, Fully Differential Example)

6.5.2.5 Fully Differential Mode IV (Half-Clock Mode Only)

In the same way as mode II, mode IV uses the SDOA output line exclusively to transmit data when the differential channels are switched automatically. Following the first conversion after M1 goes high, as shown in 図 6-9, the SDOB output tri-states.

Output data consist of a channel indicator, followed by the ADC indicator and 16 bits of conversion result, ending with 00. The channel indicator is 0 for CH*x*0 or 1 for CH*x*1, and the ADC indicator is 0 for CHA*x* or 1 for CHB*x*.

Make sure the CONVST and RD signals are no longer than one clock cycle to provide proper functionality and avoid output data corruption.

Full-clock mode is not supported in this operational mode.

Channel information is available in fully differential mode if CID = 0. In pseudo-differential mode, the sequencer controls the channel selection in this mode. Use the SEQFIFO register to properly set the channel information. The internal FIFO is not available in this mode.

Changes to the FE, SR, PDE, and CID CONFIG register bits are active with the start of the next conversion. However, there is a delay of one read access.

Update the register using every other RD pulse. This pulse is aligned either with the pulse starting the conversion or the one that reads the channel B conversion results; compare with 図 6-6.

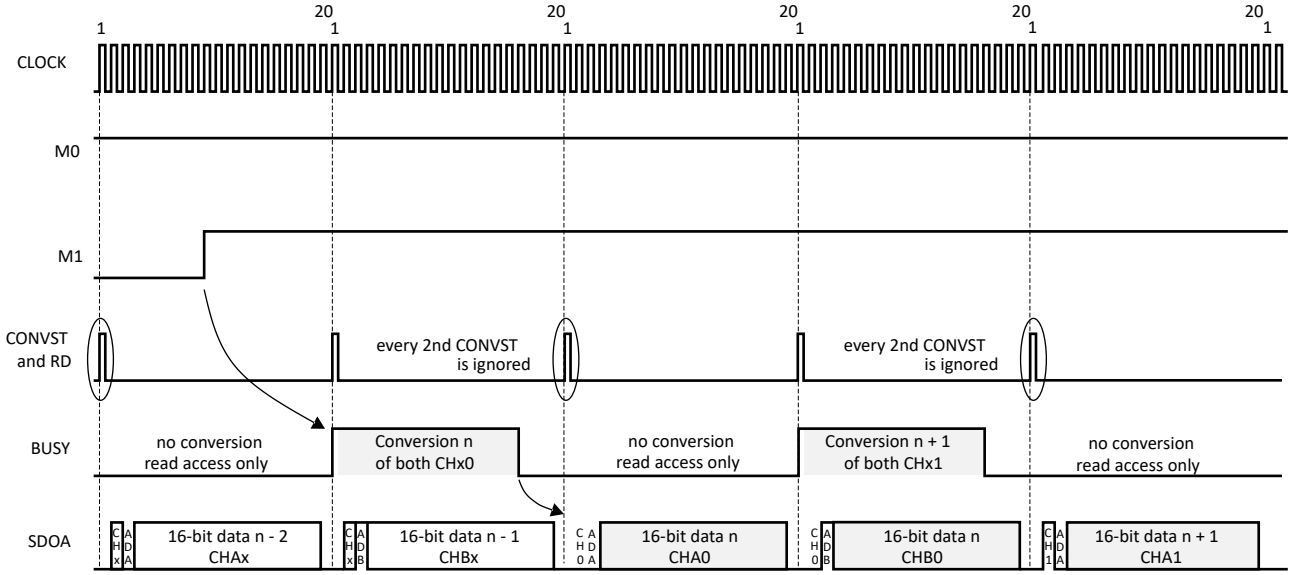


図 6-9. Fully Differential Mode IV Timing (M0 = 1, M1 = 1, PDE = 0, and CID = 0 Example)

6.5.2.6 Special Mode IV (Half-Clock Mode Only)

As with special mode II, this device also offers a special read mode for mode IV. In this mode, as shown in 図 6-10, both data results of a conversion are read by triggering a single RD pulse. In this case, set the SR bit in the CONFIG register to 1. The CONVST and RD pins are still tied together, but are issued every 40 CLOCK cycles instead of 20. Make sure the RD signal in this mode is no longer than one clock cycle to avoid output data corruption.

Data are available on the SDOA pin, accordingly.

If auto-sleep power-down mode is enabled, as shown in 図 6-10, the conversion results are presented during the next conversion.

Use this mode for fully- or pseudo-differential inputs (in pseudo-differential mode, the sequencer controls the input multiplexer). Channel information is available if the CID is 0 in fully differential mode only (CID is forced to 1 in pseudo-differential mode).

The internal FIFO is available in this mode; when used, a single read pulse allows all stored conversion data to be read. Make sure the FIFO is completely filled when used for the first time to provide proper functionality.

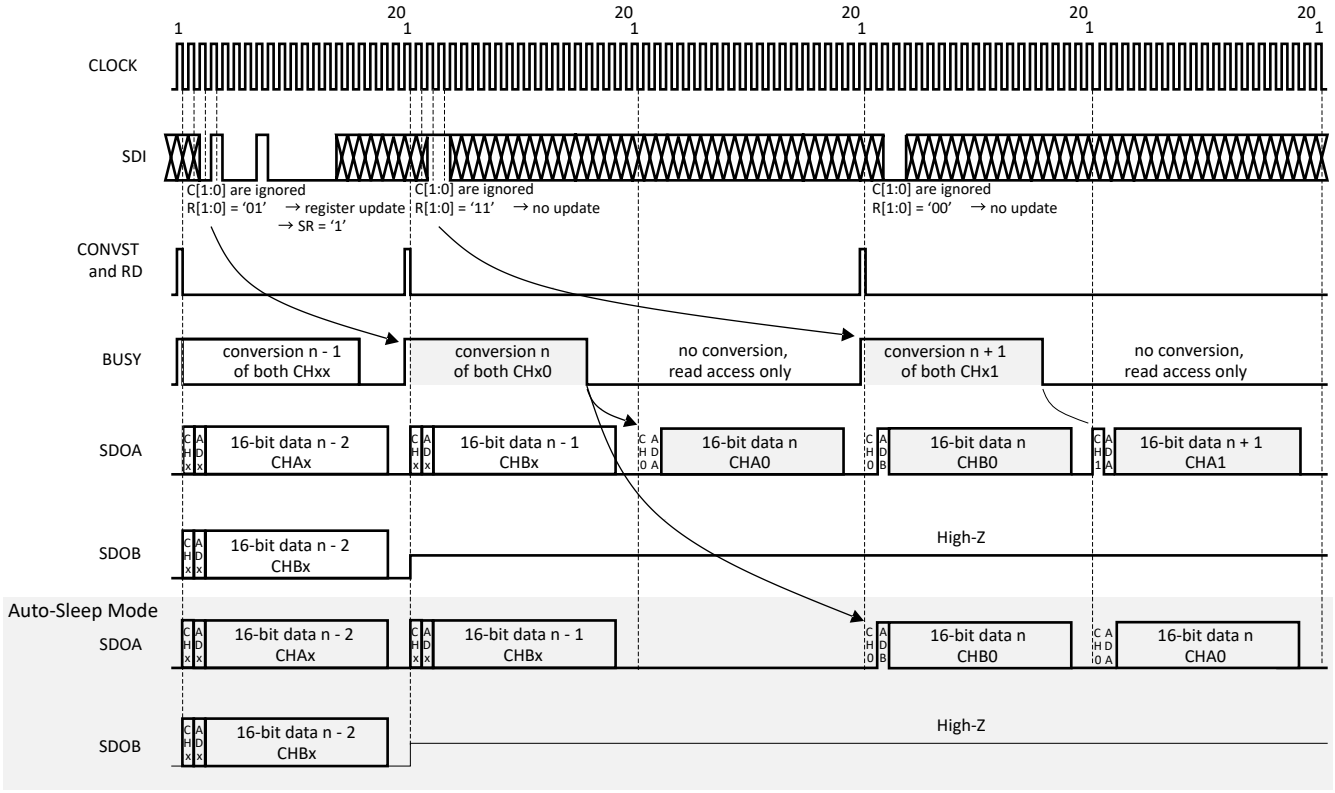


図 6-10. Special Read Mode IV Timing (M0 = 1, M1 = 1, PDE = 0, SR = 1, CID = 0, Fully Differential Example)

6.5.3 Programming the Reference DAC

Depending on which DAC is updated, the internal reference DACs is set by issuing an RD pulse. Make sure to provide a control word with R[1:0] = 01 and A[3:0] = X010 or X101. Thereafter, as shown in 図 6-11, generate a second RD pulse with a control word that starts with the first five bits ignored. The reference power control follows with the corresponding 10-bit DAC value.

To verify the DACs settings, generate an RD pulse when providing a control word containing R[1:0] = 01 and A[3:0] = 0011 or 0110. This control word initializes the read access of the appropriate DAC register. Triggering the RD line again causes the SDOA output to provide the 16-bit DAC register value followed by 0000. However, make sure channel information is disabled (CID is 1). When channel information is enabled (CID is 0), the first two bits of the data output contain the currently selected analog input channel indicator. The 16-bit DAC register contents follow with an additional 00. The channel indicator is 0 for CH*x*0 or 1 for CH*x*1. Although the register contents are valid on SDOA (図 6-11), the conversion result of channel A*x* is lost (if a conversion is performed in parallel). The conversion result of channel B*x* is valid on SDOB (if enabled), and data on SDI are ignored.

The default value of the DAC registers after power-up is 7FFh, corresponding to a disabled reference voltage of 2.5V on both REFIO*x* pins.

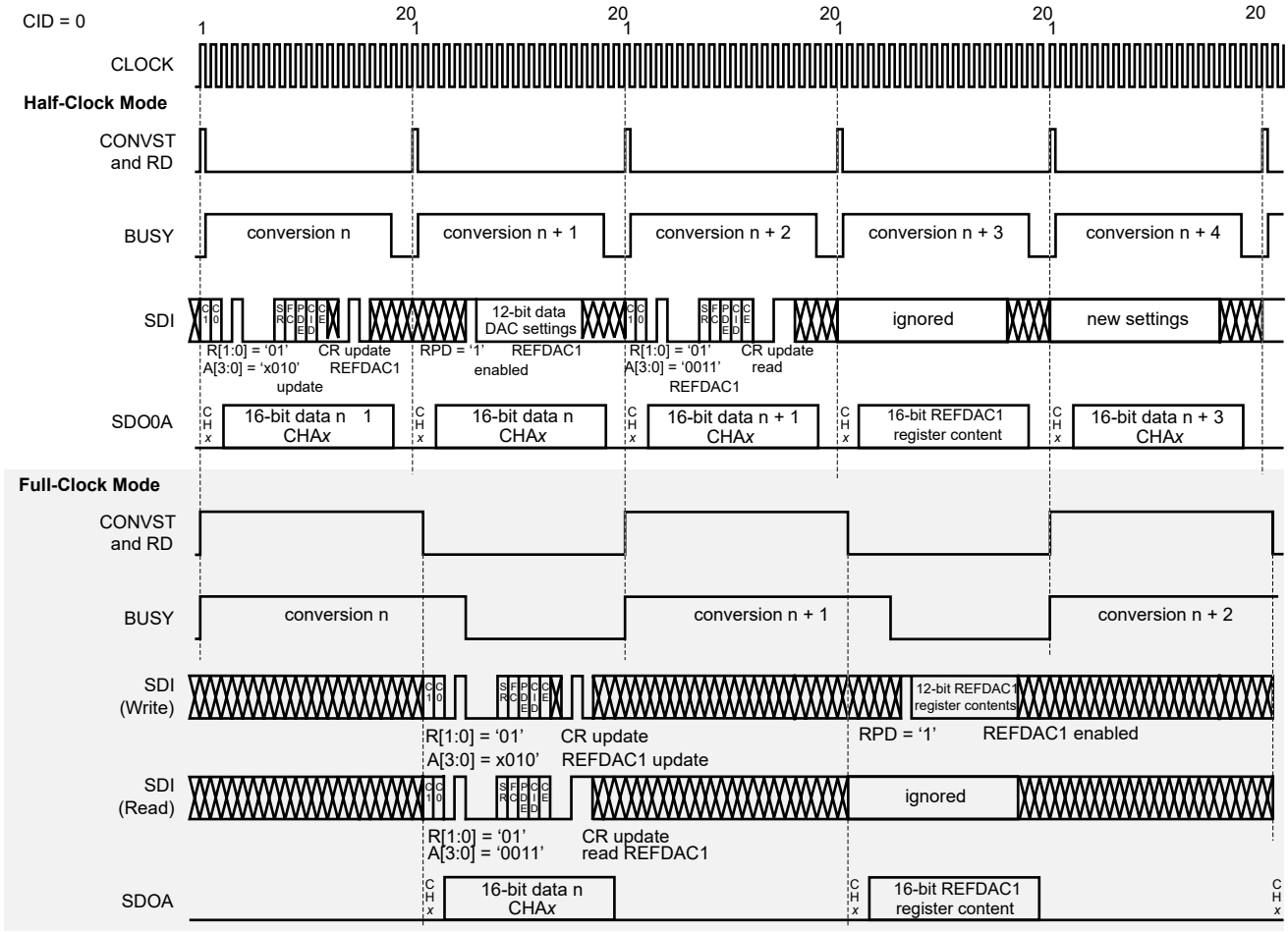


図 6-11. DAC Register Write and Read Access Timing (Both SDOx Active and CID = 0)

7 Register Map

The ADC168M102R-SEP operation is controlled through a set of registers described in this section. 表 7-1 shows the register map. Set the contents of these 16-bit registers with the serial data input (SDI) pin. This pin is coupled to RD and clocked into the device on each CLOCK falling edge. All data are transferred MSB first. All register updates become active with the CLOCK rising edge after completing the 16-clock-cycle write access operation.

表 7-1. Register Map

REGISTER	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CONFIG	C[1:0]		R[1:0]		PD[1:0]		FE	SR	FC	PDE	CID	CE	A[3:0]			
REFDAC1	Reserved					RPD	D[9:0]									
REFDAC2	Reserved					RPD	D[9:0]									
SEQFIFO	S[1:0]		SL[1:0]		C11	C10	C21	C20	C31	C30	C41	C40	SP1	SP0	FD1	FD0
REFCM	CMB[3:0]				CMA[3:0]				RB[3:0]				RA[3:0]			

To update the CONFIG register, a single write access is required. To update the contents of the other registers, a write access to the control register with the appropriate register address (bits A[3:0]) is required. A write access to the actual register follows thereafter. 図 7-1 shows a diagram of updating these registers. Update the CONFIG register contents when issuing a register read out access with a single register write access. For example, change the device mode to full-clock mode when activating the REFDAC1 register read access. A full-clock mode is active on the 16th clock cycle of the CONFIG register update. The REFDAC1 data are then presented according to the full-clock mode timing.

To verify the register contents, issue a read access with CONFIG register bits A[3:0]. This access is described in the *Programming the Reference DAC* section, based on an example of verifying the reference DAC register settings. The register contents are always available on SDOA with the next read command. For example, if the FIFO is used, the register contents are presented after the FIFO read access completes (see 表 7-5 for more details). A complete read or write access requires a total of 40 clock cycles, during which a new access to the CONFIG register is not allowed.

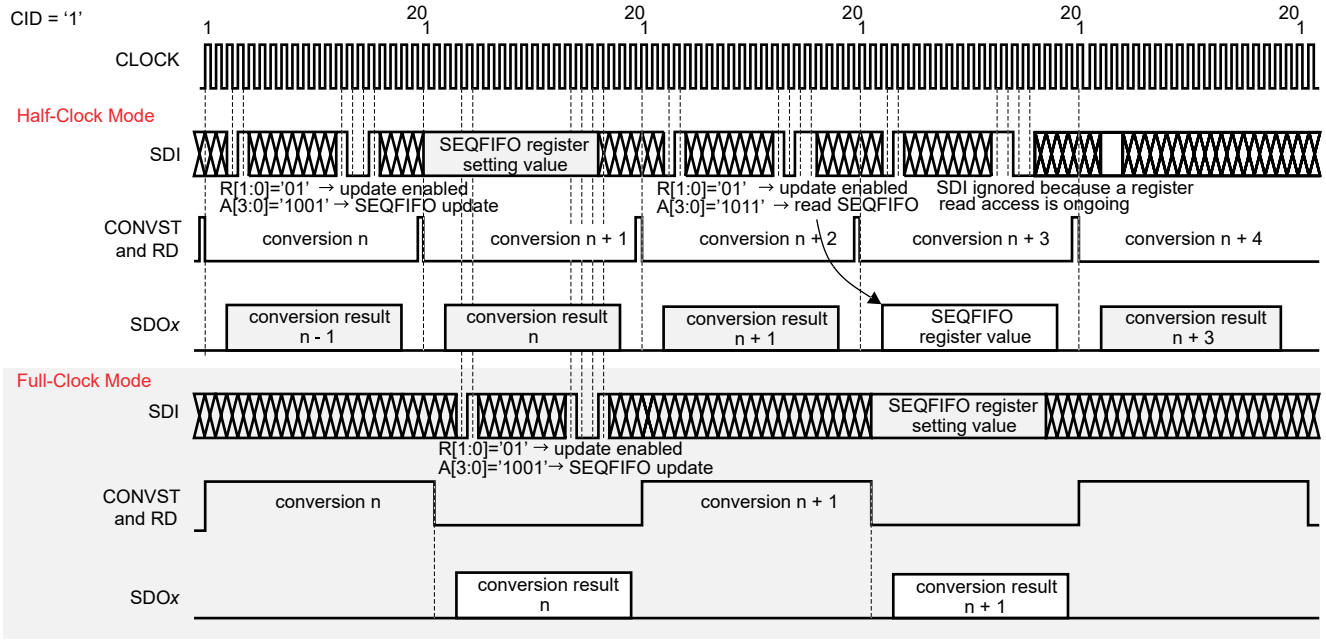


図 7-1. Updating Internal Register Settings (Example: Half-Clock Mode, CID = 1)

Configuration (Config) Register

The configuration register selects the input channel, the activation of power-down modes, and the access to the sequencer and FIFO, reference selection, and reference DAC registers.

図 7-2. Config: Configuration Register (Default = 0000h)

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
C[1:0]		R[1:0]		PD[1:0]		FE	SR	FC	PDE	CID	CE	A[3:0]			
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

表 7-2. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	C[1:0]	R/W	0h	**Input channel selection.** These bits control the multiplexer input selection depending on the status of the PDE bit. If PDE = 0 (default), the multiplexer is in fully differential mode and bits C[1:0] control the input multiplexer in the following manner: 0x = Conversion of analog signals at inputs CHx0P/CHx0N (default). 1x = Conversion of analog signals at inputs CHx1P/CHx1N. If PDE = 1, the multiplexer is in pseudo-differential mode and bits C[1:0] control the input multiplexer in the following manner: 00 = Conversion of analog signal at input CHx0 versus the selected CMx or REFIOx (default). 01 = Conversion of analog signal at input CHx1 versus the selected CMx or REFIOx. 10 = Conversion of analog signal at input CHx2 versus the selected CMx or REFIOx. 11 = Conversion of analog signal at input CHx3 versus the selected CMx or REFIOx.
13:12	R[1:0]	R/W	0h	**Configuration register update control.** These bits control the access to the CONFIG register. 00 = If M0 is 0, update of input selection bits C[1:0] only; if M0 is 1, no action (default). 01 = Update of the entire CONFIG register content enabled. 10 = Reserved for factory test; do not use. Changes potentially result in false behavior of the device. 11 = If M0 is 0, update of input selection bits C[1:0] only; if M0 is 1, no action.
11:10	PD[1:0]	R/W	0h	**Power-down control.** These bits control the different power-down modes of the device. 00 = Normal operation (default). 01 = Device is in power-down mode (see the *Power-Down Modes and Reset* section for details). 10 = Device is in sleep power-down mode (see the *Power-Down Modes and Reset* section for details). 11 = Device is in Auto-sleep power-down mode (see the *Power-Down Modes and Reset* section for details).
9	FE	R/W	0h	**FIFO enable control.** 0 = The internal FIFO is disabled (default). 1 = The internal FIFO is enabled. The depth of the FIFO is controlled by SEQFIFO register bits FD[1:0].
8	SR	R/W	0h	**Special read mode control.** 0 = Special read mode is disabled (default). 1 = Special read mode is enabled; see 図 6-7 and 図 6-10 for details.

表 7-2. Config Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
7	FC	R/W	0h	**Full clock mode operation control.** 0 = Full-clock mode operation is disabled (default); see 図 5-1 for details. 1 = Full-clock mode operation is enabled; see 図 5-2 for details.
6	PDE	R/W	0h	**Pseudo-differential mode operation enable.** 0 = 2x2 fully differential operation (default). 1 = 4x2 pseudo-differential operation.
5	CID	R/W	0h	**Channel information disable.** 0 = The channel information followed by conversion results or register contents are present on SDO*x* (default). 1 = Conversion data or register content is present on SDOx immediately after the falling edge of RD.
4	CE	R/W	0h	**2-bit counter enable (see 図 7-3).** 0: The internal counter is disabled (default). 1: The counter value is available prior to the conversion result on SDOx (active only if CID = 0).
3:0	A[3:0]	R/W	0h	**Register access control.** These bits allow reading of the CONFIG register contents and control the access to the remaining registers of the device. x000 = Update CONFIG register contents only (default) 0001 = Read CONFIG register content on SDOA with next access (see 図 7-1). x010 = Write to REFDAC1 register with next access (see 図 7-1). 0011 = Read REFDAC1 register content on SDOA with next access (see 図 7-1). 0100 = Generate software reset of the device. x101 = Write to REFDAC2 register with next access (see 図 7-1). 0110 = Read REFDAC2 register content on SDOA with next access (see 図 7-1). x111 = Update CONFIG register contents only. 1001 = Write to SEQFIFO register with next access (see 図 7-1). 1011 = Read SEQFIFO register content on SDOA with next access (see 図 7-1). 1100 = Write to REFCM register with next access (see 図 7-1). 1110 = Read REFCM register content on SDOA with next access (see 図 7-1).

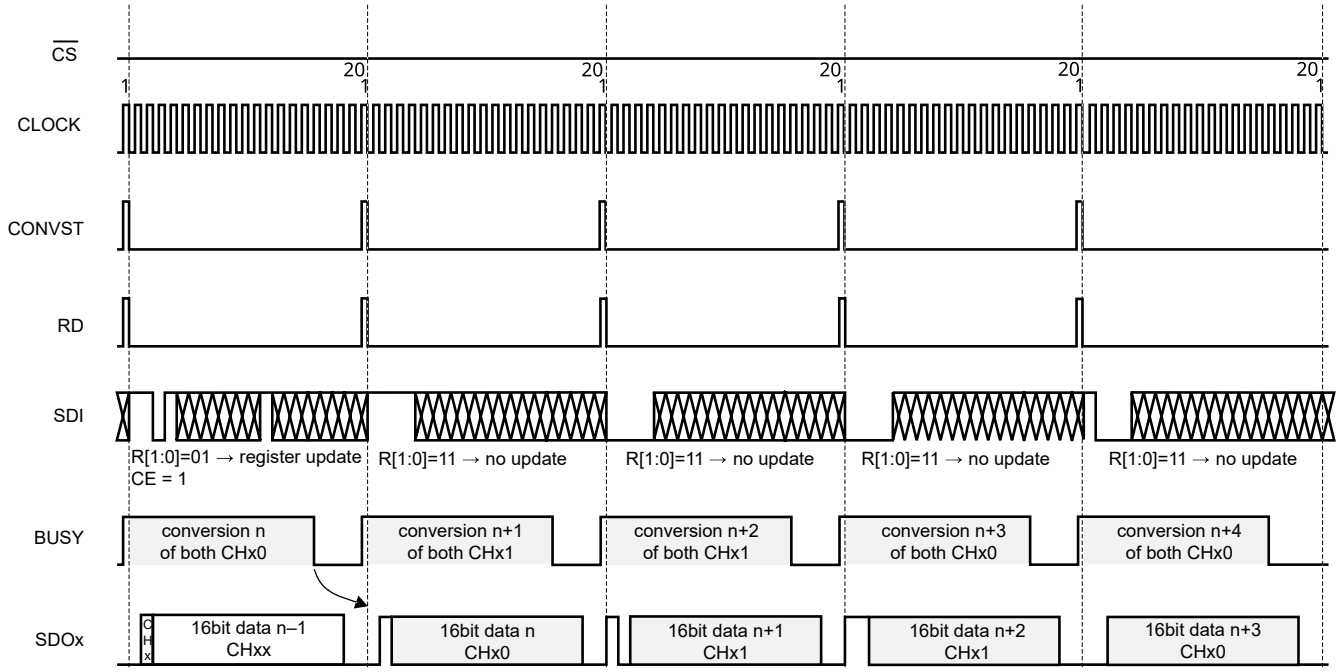


図 7-3. 2-Bit Counter Feature (Half-Clock Mode, Manual Channel Control, CID = 0)

REFDAC1 and REFDAC2 Registers

Two reference DAC registers allow for enabling and setting up the appropriate value for each of the output string DACs that are connected to the REFIO1 and REFIO2 pins.

図 7-4. REFDAC1 Control Register (Default = 07FFh)

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Reserved					RPD	D[9:0]									
R/W-0h					R/W-1h	R/W-3FFh									

表 7-3. REFDAC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	Reserved	R/W	0h	Not used; always set to 0.
10	RPD	R/W	1h	**DAC1 power down.** 0 = Internal reference path 1 is enabled and the reference voltage is available at the REFIO1 pin. 1 = The internal reference path is disabled (default).
9:0	D[9:0]	R/W	3FFh	**DAC1 setting bits.** These bits correspond to the settings of the internal reference DACs (compare REFIO section). The D9 bit is the MSB value of the DAC. Default value is 3FFh (2.5V nom).

図 7-5. REFDAC2 Control Register (Default = 07FFh)

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
Reserved					RPD	D[9:0]									
R/W-0h					R/W-1h	R/W-3FFh									

表 7-4. REFDAC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	Reserved	R/W	0h	Not used; always set to 0.
10	RPD	R/W	1h	**DAC2 power down.** 0 = Internal reference path 2 is enabled and the reference voltage is available at the REFIO2 pin. 1 = The internal reference path is disabled (default).
9:0	D[9:0]	R/W	3FFh	**DAC2 setting bits.** These bits correspond to the settings of the internal reference DACs (compare REFIO section). The D9 bit is the MSB value of the DAC. Default value is 3FFh (2.5V nom).

Sequencer/FIFO (SEQFIFO) Register

The ADC168M102R-SEP features a programmable sequencer that controls the switching of the ADC input multiplexer in pseudo-differential, automatic channel-selection mode only. When used, a single read pulse allows all stored conversion data to be read. A single CONVST is required to control the conversion of the entire sequence. If the sequencer is used, control CONVST and RD independently (see 図 7-7 and 図 7-8).

Additionally, a programmable FIFO is available on each channel that allows storing up to four conversion results. Both features are controlled using this register. If FIFO is used, contrl CONVST and RD independently. After activation of this feature, make sure the FIFO is full before being read for the first time.

If the FIFO is full and a new conversion starts, the contents are shifted by one and the oldest result is lost. Only when the sequencer is used are the entire FIFO contents lost (that is, all bits are automatically set to 0). The FIFO is used independently from the sequencer. When both are used, finish the complete sequence before reading the data out of the FIFO; otherwise, the data are potentially corrupted.

表 7-5 contains details of the data readout requirements depending on the FIFO settings in automatic channel selection mode.

表 7-5. Conversion Result Read Out In FIFO Mode

AUTOMATIC CHANNEL SELECTION		
INPUT SIGNAL TYPE	**FE = 0**	**FE = 1**
Fully differential input mode	Read cycle length = 1 word. One RD pulse required after each conversion.	Read cycle length = 2 × FIFO length. One RD pulse required for the entire FIFO content.
Pseudo-differential input mode	Read cycle length = 1 word. One RD pulse required after each conversion or after completing the sequence if S1 = 1 and S0 = 1.	Read cycle length = 2 × sequencer length × FIFO length. One RD pulse required for the entire FIFO content.

図 7-6. SEQFIFO: Sequencer and FIFO Register (Default = 0000h) (1)

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
S[1:0]		SL[1:0]		C1[1:0]		C2[1:0]		C3[1:0]		C4[1:0]		SP[1:0]		FD[1:0]	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

(1) The sequencer is used in pseudo-differential mode only. Set this register before setting the REFCM register.

表 7-6. SEQFIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	S[1:0]	R/W	0h	**Sequencer mode selection (see 図 7-7) in pseudo-differential mode only.** These bits allow for the control of the number of CONVSTs required, and the behavior of the BUSY pin in sequencer mode. 0x = An individual CONVST is required with BUSY indicating each conversion (default). 10 = A single CONVST is required for the entire sequence with BUSY indicating each conversion (half-clock mode only). 11 = A single CONVST is required for the entire sequence with BUSY remaining high throughout the sequence (half-clock mode only).
13:12	SL[1:0]	R/W	0h	**Sequencer length control.** These bits control the length of a sequence. Bits [11:6] are only active if SL > 00. 00 = Do not use; use mode I or II instead, where M0 is 0 (default). 01 = Sequencer length is 2; C1x (bits[11:10]) and C2x (bits[9:8]) define the actual channel selection. 10 = Sequencer length is 3; C1x (bits[11:10]), C2x (bits[9:8]) and C3x (bits[7:6]) define the actual channel selection. 11 = Sequencer length is 4; C1x (bits[11:10]), C2x (bits[9:8]), C3x (bits[7:6]), and C4x (bits[5:4]) define the actual channel selection.

表 7-6. SEQFIFO Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11:10	C1[1:0]	R/W	0h	First channel in sequence selection bits.
9:8	C2[1:0]	R/W	0h	Second channel in sequence selection bits.
7:6	C3[1:0]	R/W	0h	Third channel in sequence selection bits.
5:4	C4[1:0]	R/W	0h	Fourth channel in sequence selection bits. Bits [11:4] control the pseudo-differential input multiplexer channel selection in sequencer mode. 00 = CHA0 and CHB0 are selected for the next conversion (default). 01 = CHA1 and CHB1 are selected for the next conversion. 10 = CHA2 and CHB2 are selected for the next conversion. 11 = CHA3 and CHB3 are selected for the next conversion.
3:2	SP[1:0]	R/W	0h	**Sequence position bits (read only).** These bits indicate the setting of the pseudo-differential input multiplexer in sequencer mode. 00 = Inputs selected using bits C1[1:0] are converted with next rising edge of CONVST (default). 01 = Inputs selected using bits C2[1:0] are converted with next rising edge of CONVST. 10 = Inputs selected using bits C3[1:0] are converted with next rising edge of CONVST. 11 = Inputs selected using bits C4[1:0] are converted with next rising edge of CONVST.
1:0	FD[1:0]	R/W	0h	**FIFO depth control (see 図 7-8).** These bits control the depth of the internal FIFO if CONFIG register bit FE is 1. 00 = One conversion result per channel is stored in the FIFO for burst read access (default). 01 = Two conversion results per channel are stored in the FIFO for burst read access. 10 = Three conversion results per channel are stored in the FIFO for burst read access. 11 = Four conversion results per channel are stored in the FIFO for burst read access.

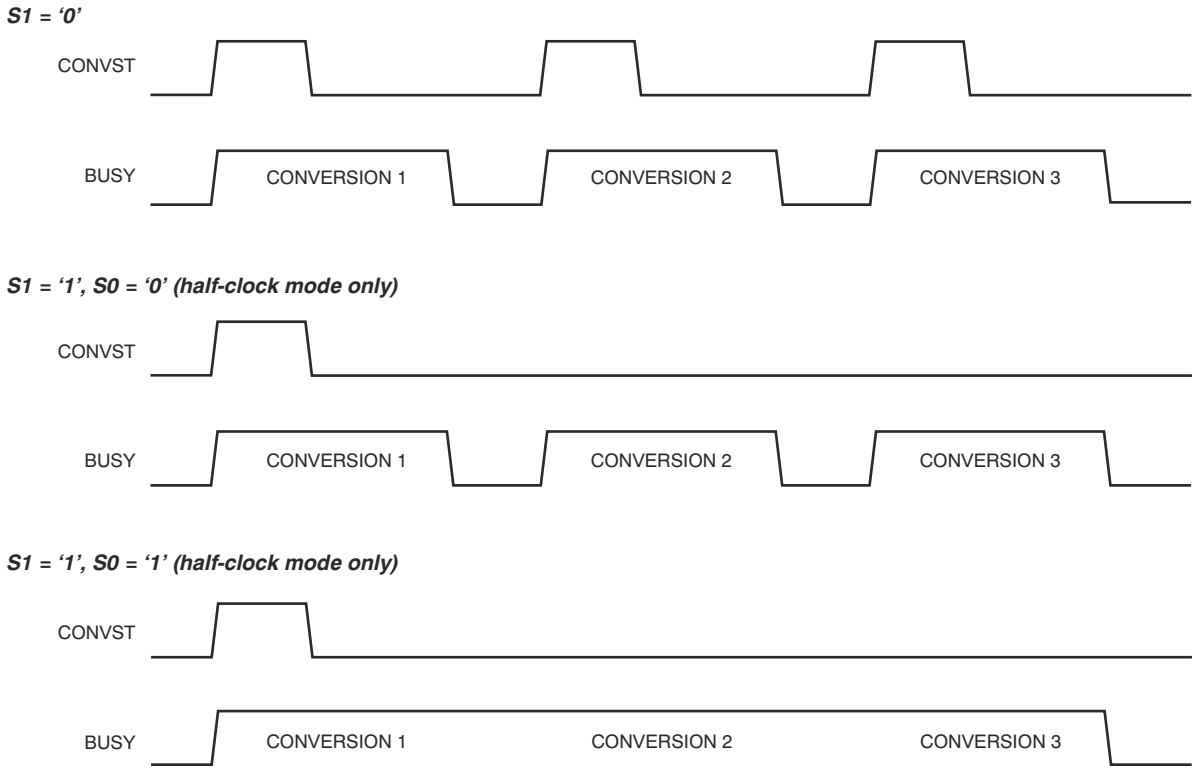


図 7-7. Sequencer Modes

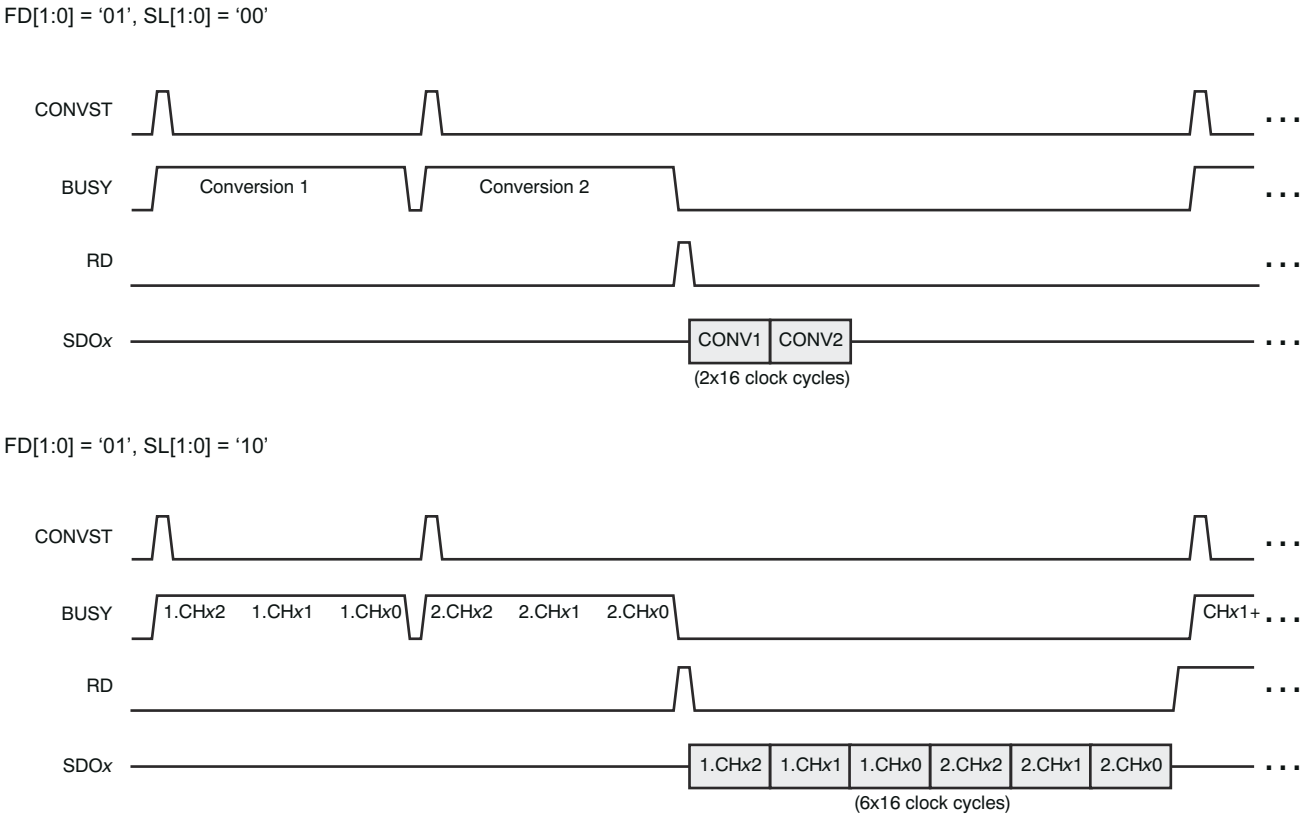


図 7-8. FIFO and Sequencer Operation Example

Reference and Common-Mode Selection (REFCM) Register

For flexible adjustment of the common-mode voltage in pseudo-differential mode when simplifying the circuit layout, the ADC168M102R-SEP provides this register. This register assigns one of the CM*x* inputs as a reference for each input signal. According to the register settings, the CM*x* signals are internally connected to the appropriate negative input of each ADC.

Additionally, this register also allows flexible assignment of one internal reference DAC output as a reference for each channel in both fully- and pseudo-differential modes.

図 7-9. REFCM: Reference and Common-Mode Selection Register (Default = 0000h) (1)

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
CMB[3:0]				CMA[3:0]				RB[3:0]				RA[3:0]			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

(1) Set this register after setting the SEQFIFO register.

表 7-7. REFCM Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CM*xx*	R/W	0h	**Common-mode source selection bits (per input channel).** These bits allow selection of the CMx input pins or the internal reference source as common-mode for pseudo-differential inputs B[3:0] and A[3:0]. The selected signal is connected to the negative input of the corresponding ADC. 0 = External common-mode source through CM*x* (default). 1 = Internal common-mode source = REFIO*x*, depending on settings of bits R*x*[3:0].
7	RB3	R/W	0h	**Internal reference DAC output selection for CHB3 in pseudo-differential mode, or channel CHB1P, CHB1N in fully differential mode.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
6	RB2	R/W	0h	**Internal reference DAC output selection for CHB2 in pseudo-differential mode only.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
5	RB1	R/W	0h	**Internal reference DAC output selection for CHB1 in pseudo-differential mode only.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
4	RB0	R/W	0h	**Internal reference DAC output selection for CHB0 in pseudo-differential mode, or channel CHB0P, CHB0N in fully differential mode.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
3	RA3	R/W	0h	**Internal reference DAC output selection for CHA3 in pseudo-differential mode, or channel CHA1P, CHA1N in fully differential mode.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
2	RA2	R/W	0h	**Internal reference DAC output selection for CHA2 in pseudo-differential mode only.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.
1	RA1	R/W	0h	**Internal reference DAC output selection for CHA1 in pseudo-differential mode only.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.

表 7-7. REFCM Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	RA0	R/W	0h	**Internal reference DAC output selection for CHA0 in pseudo-differential mode, or channel CHA0P, CHA0N in fully differential mode.** 0 = Internal reference source REFIO1 selected (default). 1 = Internal reference source REFIO2 selected.

8 Application and Implementation

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8.1 Application Information

8.2 Typical Application

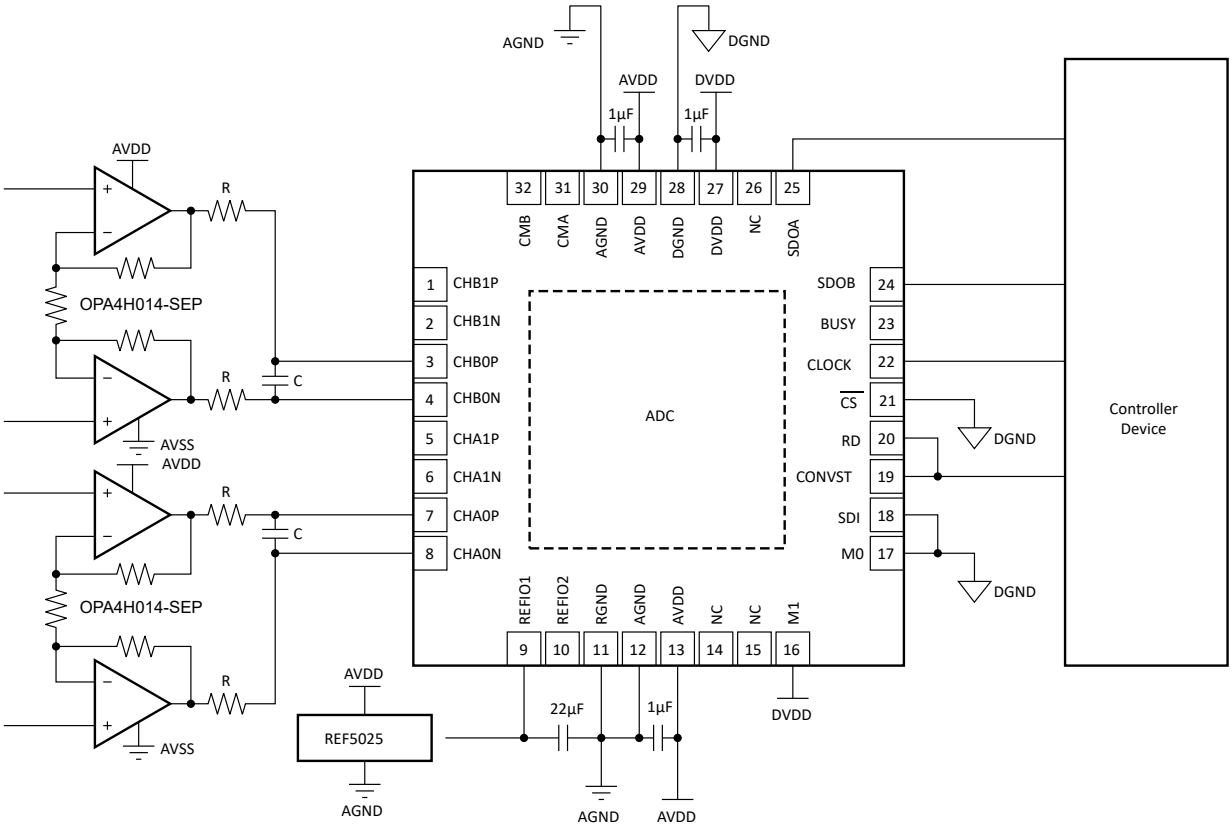

図 8-1. Four-Wire Application Configuration

8.2.1 Design Requirements

表 8-1 shows the parameters for this application example. Use a data acquisition (DAQ) system capable of digitizing up to four differential input signals ranging from 0V to 5V with BW = 10kHz. This design also requires a throughput up to 1000kSPS. Make sure the ADC168M102R-SEP interfaces to an MCU using a 4-wire interface.

表 8-1. Design Parameters

PARAMETER	VALUE
Analog input configuration	Differential
Interface configuration	4-wire

8.2.2 Detailed Design Procedure

An example of a minimum configuration for the ADC168M102R-SEP is illustrated in 図 8-1. In this case, the device is used in dual-channel, fully differential input mode with a four-wire digital interface. The digital interface is connected to the controller device and with default device settings after power up. The internal reference is disabled at power up to prevent driving against an external reference if used. Thus, an external reference source is used in this example. To use the internal reference, connect the SDI input to the controller, allowing access to the REFDAC registers. The corresponding timing diagram including the timing requirements are described in 図 8-2 and the *Switching Characteristics* table.

Make sure the input signal for the amplifiers fulfill the common-mode voltage requirements of the device in this configuration. The actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application.

式 4 calculates these values:

$$f_{FILTER} = \frac{\ln(2)(n + 1)}{2\pi 2RC} \tag{4}$$

where:

- *n* = 16 for the ADC168M102R-SEP resolution

As a good trade-off between required minimum driver bandwidth and the capacitor value, use a capacitor value of at least 1nF.

Keeping the acquisition time in mind, calculate the resistor value as shown in 式 5 for each of the series resistors:

$$R = \frac{t_{ACQ}}{\ln(2)(n + 1)2C} \tag{5}$$

where:

- *n* = Device resolution

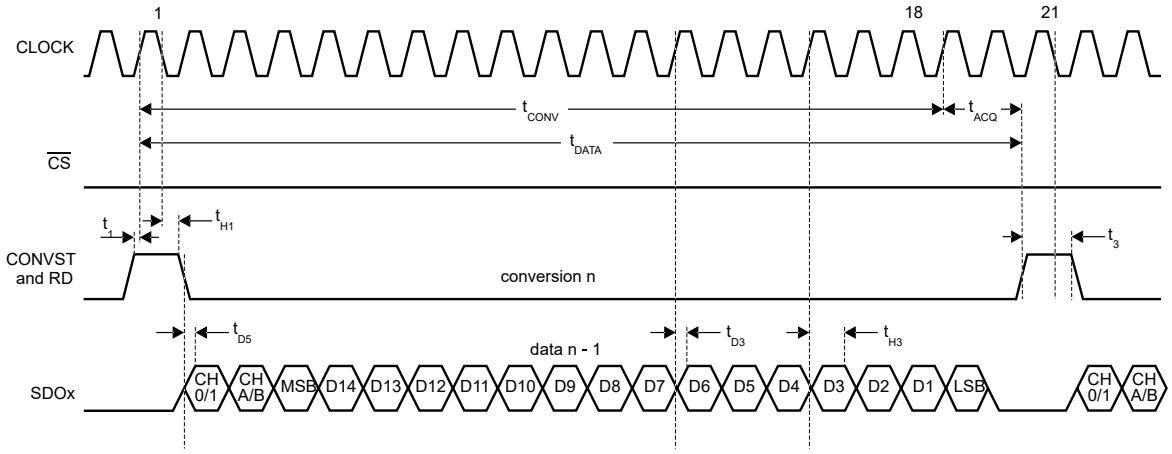

図 8-2. Four-Wire Application Timing (Half-Clock Mode)

8.2.3 Application Curve

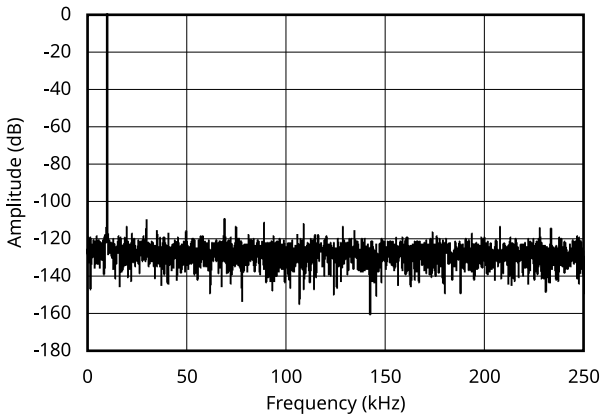

図 8-3. Frequency Spectrum (4096 Point FFT; f_{IN} = 10kHz, f_{SAMPLE} = 0.5MSPS)

8.3 Power Supply Recommendations

The ADC168M102R-SEP has two separate supplies: DVDD and AVDD. Use the DVDD pin for the buffers of the digital interface and the AVDD pin for all remaining circuits.

DVDD ranges from 2.3V to 5.5V, allowing the ADC to easily interface with processors and controllers. To limit the injection of noise energy from external digital circuitry, properly filter DVDD. Place a 1µF bypass capacitor between the DVDD pin and the digital ground plane.

AVDD supplies the internal analog circuitry. For optimum performance, a linear regulator generates the analog supply voltage in a 2.7V to 5.5V range for the ADC and the necessary analog front-end.

Connect 1µF bypass capacitors to the analog ground plane such that the current flows through the pad of these capacitors. That is, place the vias on the opposite side of the connection between the capacitor and the power-supply pin of the ADC.

8.4 Layout

8.4.1 Layout Guidelines

For optimum performance, consider the physical layout of the ADC168M102R-SEP circuitry, particularly if the device is used at the maximum throughput rate. In this case, use a fixed phase relationship between CLOCK and CONVST.

Additionally, the high-performance SAR architecture is sensitive to glitches or sudden changes that occur just before latching the output of the internal analog comparator. The power supply, reference, ground connections, and digital inputs are potential sources of such interruptions. Therefore, when operating an *n*-bit SAR converter, there are *n* windows where large external transient voltages (glitches) potentially affect the conversion result. Such glitches originate from switching power supplies, nearby digital logic, or high-power devices. The degree of impact depends on the reference voltage, layout, and the actual timing of the external event.

With this possibility in mind, make sure power to the device is clean and well-bypassed. Place a 1µF ceramic bypass capacitor at each supply pin (connected to the corresponding ground pin) as close to the device as possible.

If the reference voltage is external, make sure the operational amplifier is able to drive the 22µF capacitor without oscillation. A series resistor between the driver output and the capacitor is potentially required. To minimize any code-dependent voltage drop on this path, use a small value for this resistor (10Ω max). TI's REF50xx family is able to directly drive such a capacitive load.

8.4.1.1 Grounding

Connect the AGND, RGND, and DGND pins to a clean ground reference. Keep all connections as short as possible to minimize the inductance of these paths. Use vias to connect the pads directly to the ground plane. In designs without ground planes, keep the ground trace as wide as possible. Avoid connections close to the grounding point of a microcontroller or digital signal processor.

Use a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area. This usage depends on the circuit density of the board, placement of the analog and digital components, and the related current loops. For a separated analog ground area, provide a low-impedance connection between the analog and digital ground of the ADC. Place a bridge underneath (or next) to the ADC (see 図 8-4) to create this connection. Otherwise, even short undershoots on the digital interface less than –300mV potentially lead to ESD diode conduction. When the ESD diodes conduct, current flows through the substrate and degrades the analog performance.

During PCB layout, avoid any return currents crossing any sensitive analog areas or signals. Make sure signals do not exceed the –300mV limit with respect to the corresponding (AGND or DGND) ground plane.

8.4.1.2 Digital Interface

To further optimize device performance, use a 10Ω to 100Ω series resistor on each digital pin of the device. In this manner, the slew rate of the input and output signals is reduced, limiting the noise injection from the digital interface.

8.4.2 Layout Example

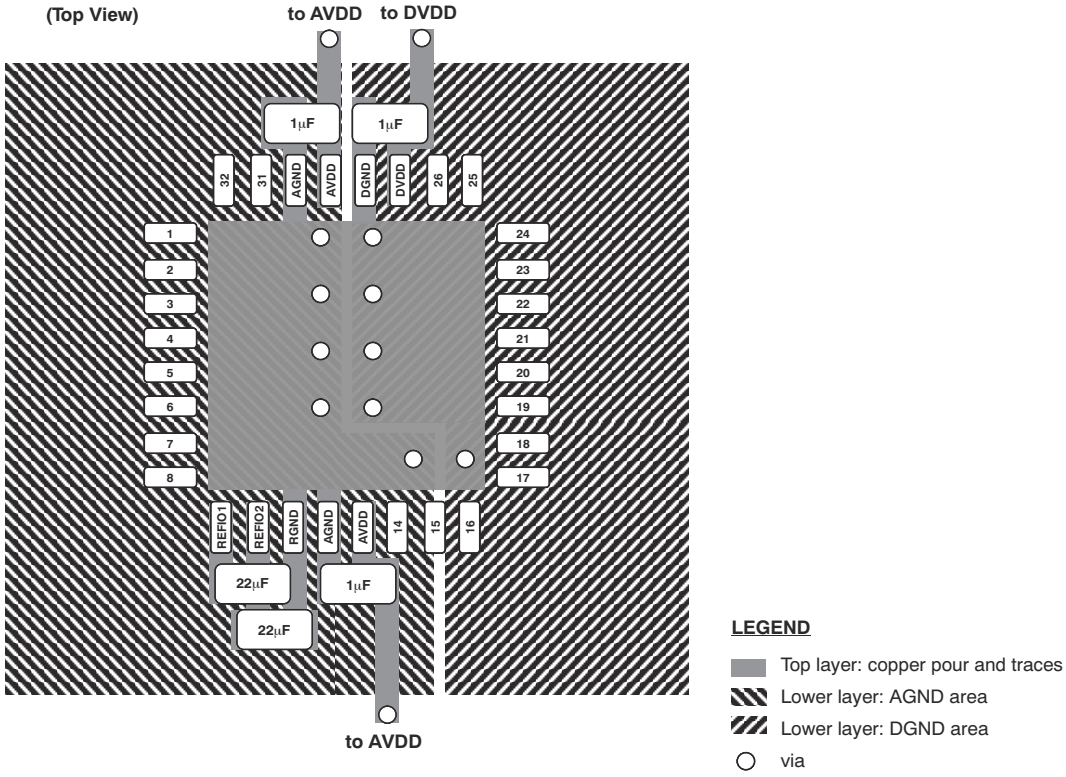

図 8-4. Optimized Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *μA78xx Fixed Positive Voltage Regulators* data sheet

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC168M102RRHBTSEP	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	(ADC168M, SEP) (102RSEP, ADC168M)
ADC168M102RRHBTSEP.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	(ADC168M, SEP) (102RSEP, ADC168M)
V62/24361-01XE	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-55 to 125	(ADC168M, SEP) (102RSEP, ADC168M)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

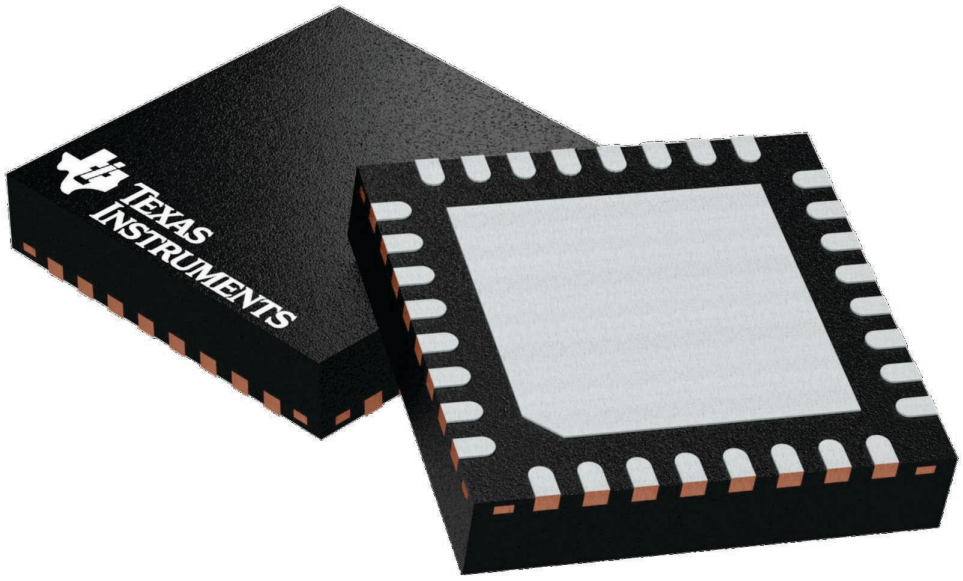
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

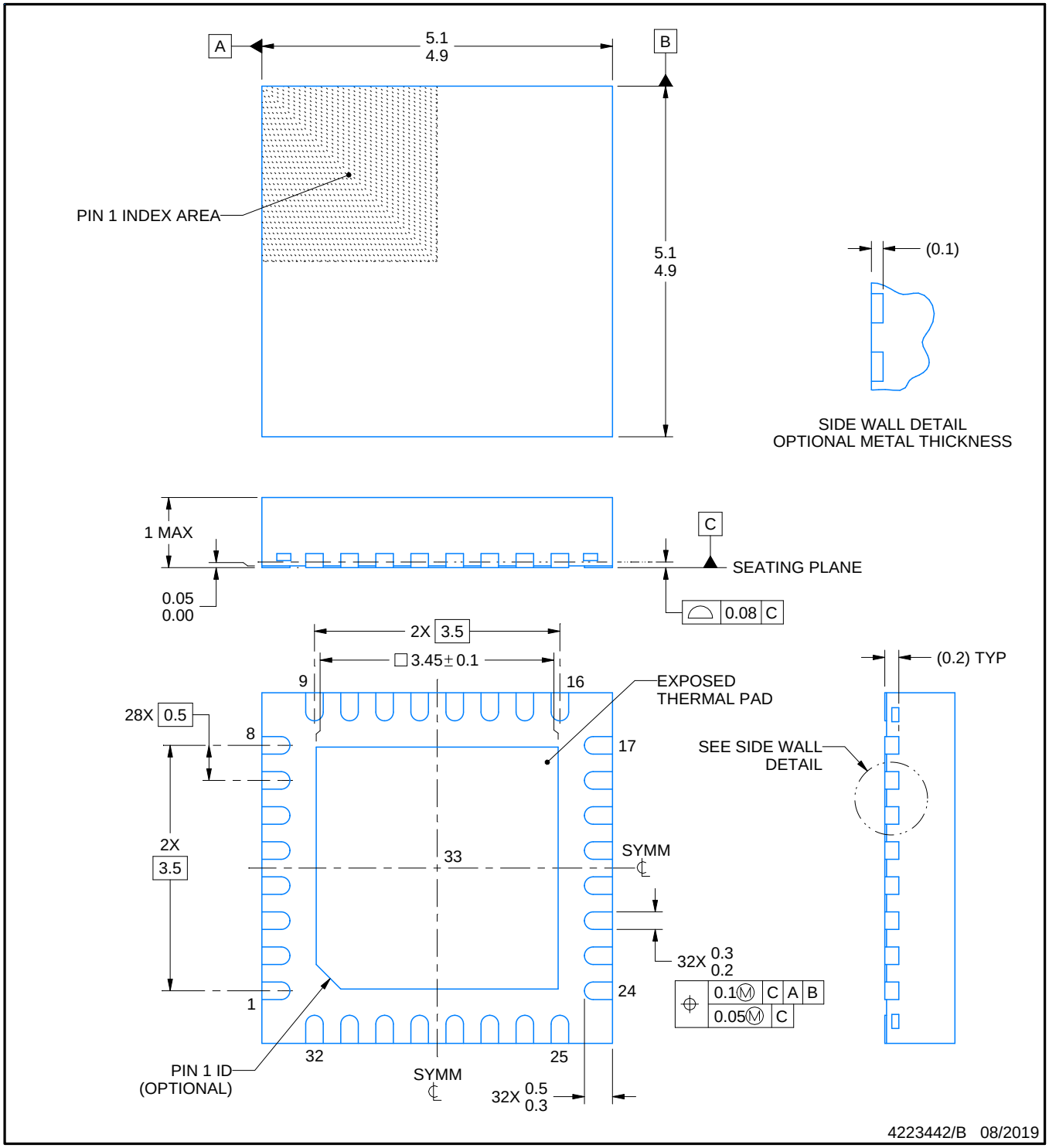
4224745/A

RHB0032E

PACKAGE OUTLINE

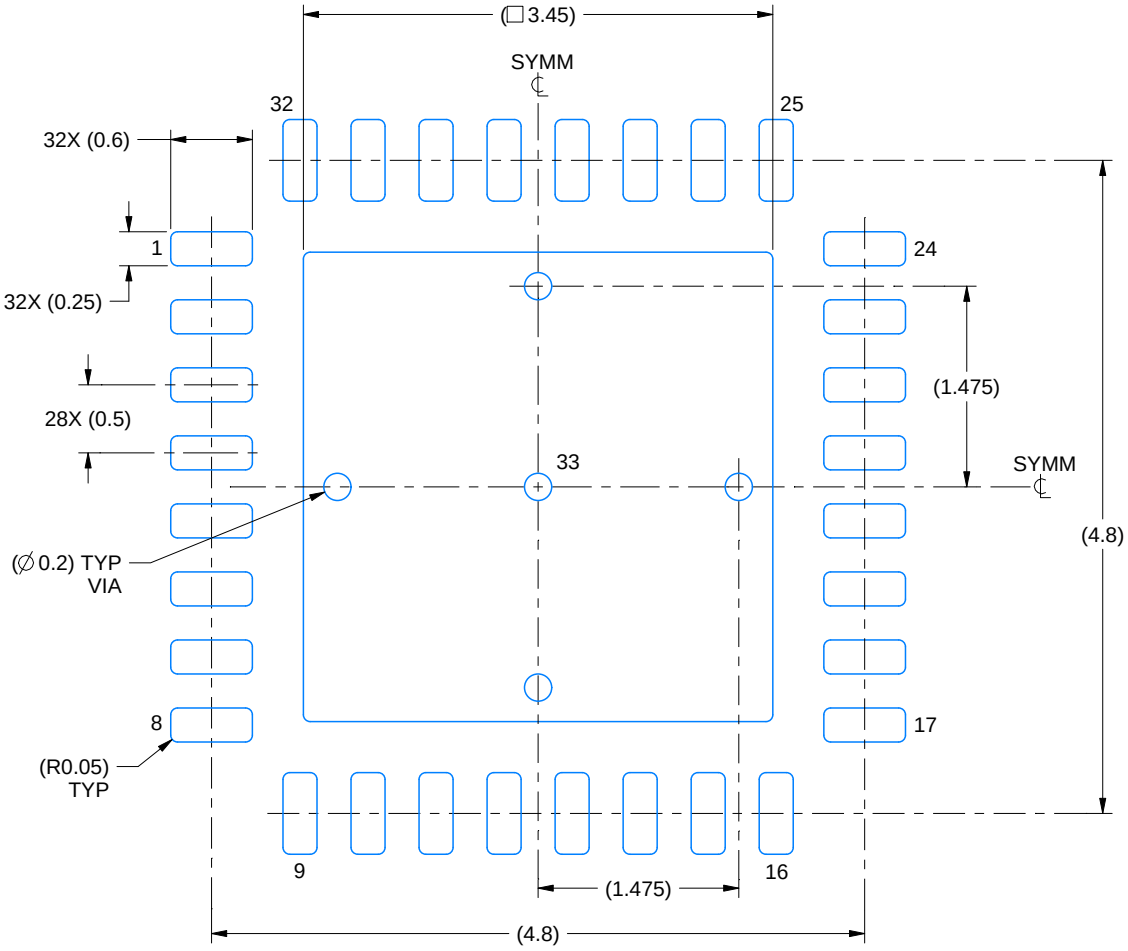
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

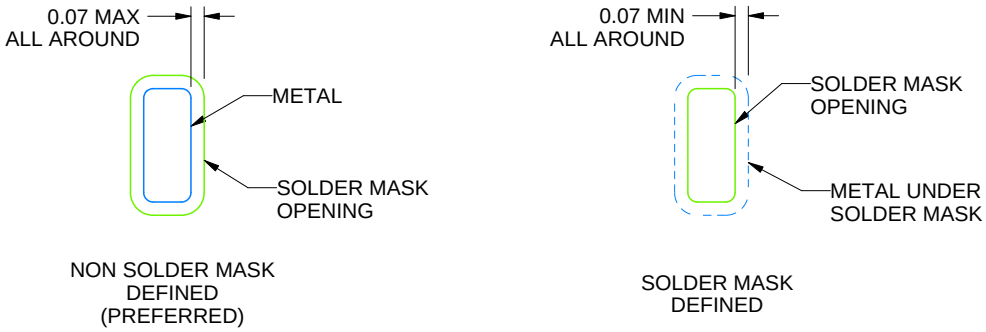


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

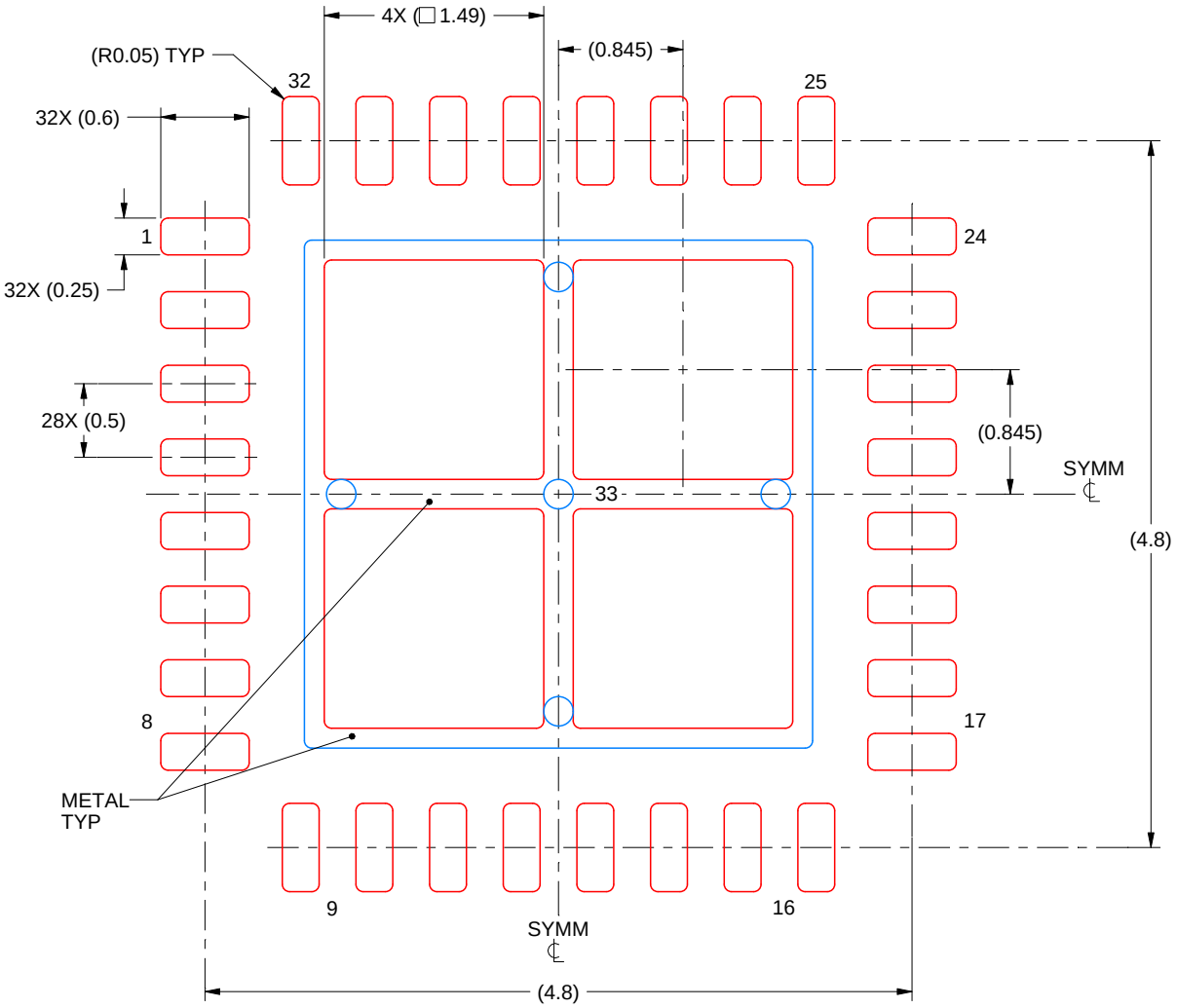


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月