TEXAS INSTRUMENTS
ADS1114L, ADS1115L
JAJSQJ6 – DECEMBER 2023

ADS111xL 超小型、低消費電力、16 ビット、PGA 搭載 860-SPS ADC、コンパレータ、1.8V I²C バス電圧に対応

1 特長

- 電源電圧範囲:2.0 V ～ 3.6 V
- 低消費電流:
  - 150µA (連続変換モード)
- データ・レートをプログラム可能:
  8SPS～860SPS
- シングルサイクルのセトリング
- 内部低ドリフト基準電圧
- 内部発振器
- アラート出力ピン付きデジタル コンパレータ
- I²C インターフェイス:
  - 4 つのピン選択可能アドレス
  - 1.8V I²C バス電圧と互換
- 動作温度範囲:
  - -40℃～+125℃

2 アプリケーション

- 一般的なシステム監視:
  - 電源電圧の監視
  - 電流測定
  - 温度測定
- ウェアラブルおよびパーソナル エレクトロニクス

製品情報

部品番号	入力チャネル	特長(1)
ADS1114L	差動 1 (シングル・エンド 1)	PGA、コンパレータ
ADS1115L	差動 2 (シングル・エンド 4)	PGA、コンパレータ

(1) 詳細については、デバイス比較表を参照してください。

3 概要

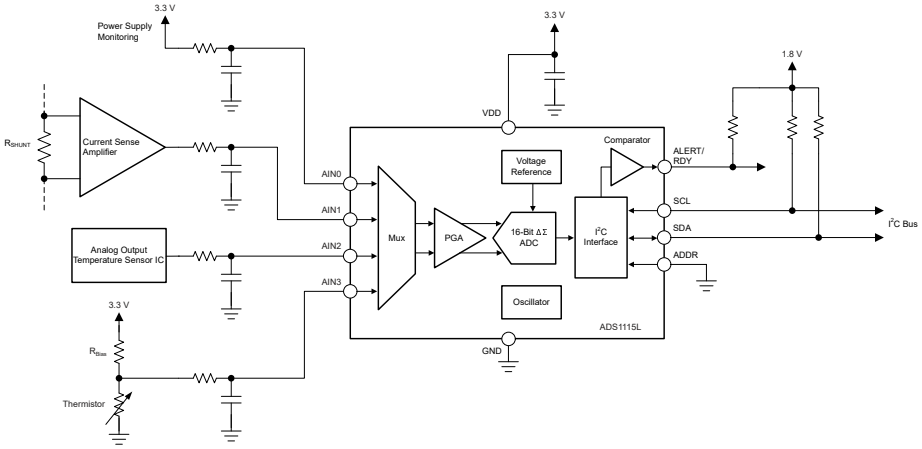
ADS1114L および ADS1115L (ADS111xL) は、高精度、低消費電力、16 ビット、I²C 互換のアナログ / デジタル コンバータ (ADC) で、超小型の 12 ピン DSBGA、10 ピン VSSOP パッケージで供給されます。ADS111xL は、低ドリフトの基準電圧と発振器を内蔵しています。ADS111xL は、プログラマブル ゲイン アンプ (PGA) およびデジタル コンパレータも内蔵しています。これらの機能を有しデバイス動作電源電圧範囲が広いため、省電力と省スペースが要求される、センサを使用した測定アプリケーションに適します。

ADS111xL は、最大 860 サンプル/秒 (SPS) のデータ レートで変換を実行できます。PGA は入力電圧範囲が ±256mV～±6.144V で、振幅の小さな信号から大きな信号まで高精度に測定できます。ADS1115L には入力マルチプレクサ (MUX) が搭載されており、2 つの差動入力または 4 つのシングルエンド入力を測定できます。過電圧や低電圧の検出には、ADS111xL のデジタル コンパレータを使用してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
ADS111xL	YCJ (DSBGA、12)	1.47 mm×1.03 mm
	DGS (VSSOP、10)	3.00 mm×4.9 mm

(1) 利用可能なすべてのパッケージについては、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



システム監視アプリケーションの例

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4 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	INTERFACE	DIGITAL INPUT LEVELS
ADS1014L	12	3300	1 (1)	I²C	Independent of VDD
ADS1015L	12	3300	2 (4)	I²C	Independent of VDD
ADS1114L	16	860	1 (1)	I²C	Independent of VDD
ADS1115L	16	860	2 (4)	I²C	Independent of VDD
ADS1014	12	3300	1 (1)	I²C	Ratiometric to VDD
ADS1015	12	3300	2 (4)	I²C	Ratiometric to VDD
ADS1114	16	860	1(1)	I²C	Ratiometric to VDD
ADS1115	16	860	2 (4)	I²C	Ratiometric to VDD

5 Pin Configuration and Functions

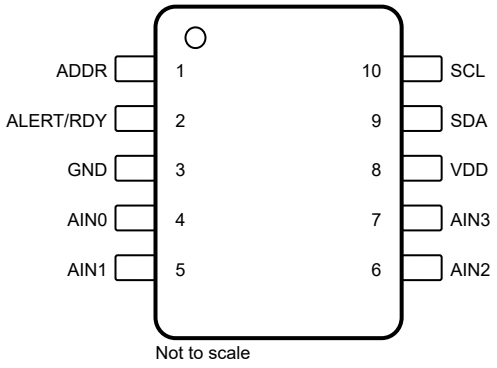


**図 5-1. DGS Package,
10-Pin VSSOP (Top View)**

表 5-1. Pin Functions: DGS Package

PIN			TYPE	DESCRIPTION(1)
NAME	ADS1114L	ADS1115L		
ADDR	1	1	Digital input	I²C target address select pin. See the *I²C Address Selection* section for details.
AIN0	4	4	Analog input	Analog input 0
AIN1	5	5	Analog input	Analog input 1
AIN2	—	6	Analog input	Analog input 2 (ADS1115L only)
AIN3	—	7	Analog input	Analog input 3 (ADS1115L only)
ALERT/RDY	2	2	Digital output	Comparator output or conversion ready. Open-drain output. Connect to VDD using a pullup resistor.
GND	3	3	Analog	Ground
NC	6, 7	—	—	No connect. Leave pin floating or connect to GND.
SCL	10	10	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
SDA	9	9	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.
VDD	8	8	Analog	Power supply. Connect a 0.1-µF, power-supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.

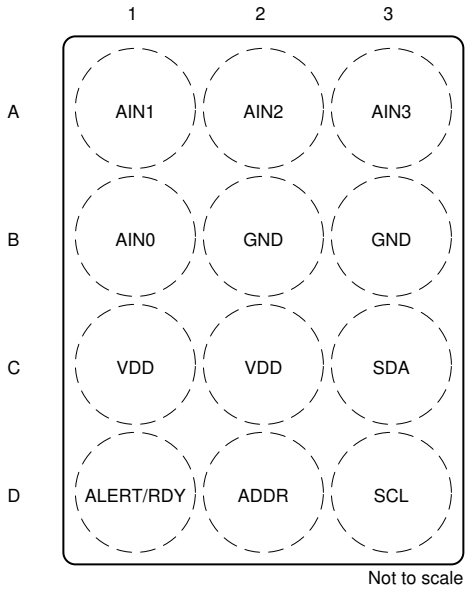


図 5-2. YCJ Package,
12-Pin DSBGA (Top View)

表 5-2. Pin Functions: YCJ Package

PIN			TYPE	DESCRIPTION(1)
ADS1114L	ADS1115L	NAME		
D2	D2	ADDR	Digital input	I²C target address select pin. See the *I²C Address Selection* section for details.
B1	B1	AIN0	Analog input	Analog input 0
A1	A1	AIN1	Analog input	Analog input 1
—	A2	AIN2	Analog input	Analog input 2 (ADS1115L only)
—	A3	AIN3	Analog input	Analog input 3 (ADS1115L only)
D1	D1	ALERT/RDY	Digital output	Comparator output or conversion ready. Open-drain output. Connect to VDD using a pullup resistor.
B2, B3	B2, B3	GND	Analog	Ground
A2, A3	—	NC	—	No connect. Leave pin floating or connect to GND.
D3	D3	SCL	Digital input	Serial clock input. Connect to VDD using a pullup resistor.
C3	C3	SDA	Digital I/O	Serial data input and output. Connect to VDD using a pullup resistor.
C1, C2	C1, C2	VDD	Analog	Power supply. Connect a 0.1-µF, power-supply decoupling capacitor to GND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	5.5	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	SCL, SDA, ADDR, ALERT/RDY	GND – 0.3	5.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Power supply	VDD to GND	2		3.6	V
ANALOG INPUTS(1)						
V_{AINx}	Absolute input voltage		GND		VDD	V
FSR	Full-scale input voltage range(2)	$V_{IN} = V_{AINP} – V_{AINN}$	±0.256		±6.144	V
DIGITAL INPUTS						
	Input voltage		GND		3.6	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the selected positive and negative inputs of the ADC. AINx denotes one of the two (ADS1114L) or four (ADS1115L) available analog inputs.
(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 3.6 V (whichever is smaller) must be applied to this device. See 表 8-1 for more information.

6.4 Thermal Information

THERMAL METRIC(1)		DGS (VSSOP)	YCJ (DSBGA)	UNIT
		10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.7	101.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.2	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	103.8	25.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	102.1	25.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale input range (FSR) = ±2.048 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Common-mode input impedance	FSR = ±6.144 V(1)		10		MΩ
		FSR = ±4.096 V(1), FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V(1)		22		MΩ
		FSR = ±4.096 V(1)		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, FSR = ±0.256 V		710		kΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		16			Bits
DR	Data rate		8, 16, 32, 64, 128, 250, 475, 860			SPS
	Data rate variation	All data rates	–10%		10%	
INL	Integral nonlinearity (best fit)	DR = 8 SPS, FSR = ±2.048 V			1	LSB
	Offset error (input referred)	FSR = ±2.048 V, differential inputs	–3	±1	3	LSB
		FSR = ±2.048 V, single-ended inputs		±3		
	Offset drift	FSR = ±2.048 V		0.005		LSB/°C
	Offset error match	Between any two inputs		3		LSB
	Gain error(2)	T_A = 25°C, FSR = ±2.048 V	–0.15%	±0.01%	0.15%	
	Gain drift(2)	FSR = ±0.256 V		7		ppm/°C
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V		5		
	Gain error match	Between any two gain settings	–0.1%	±0.02%	0.1%	
		Between any two inputs	–0.1%	±0.05%	0.1%	
CMRR	Common-mode rejection ratio	At dc, FSR = ±0.256 V		105		dB
		At dc, FSR = ±2.048 V		100		
		f_{CM} = 50 Hz or 60 Hz, DR = 8 SPS		105		
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		GND		0.25	V
V_{IH}	Logic input level, high		1		3.6	V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	GND		0.3	V
I_{OL}	Low-level output current	V_{OL} = 0.6 V	6			mA
	Input current	GND ≤ $V_{Digital\ Input}$ ≤ VDD	–10		10	µA

6.5 Electrical Characteristics (続き)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale input range (FSR) = ±2.048 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Capacitance	Each pin			10	pF
SUPPLY CURRENT AND POWER DISSIPATION						
I_{VDD}	Supply current	Power-down		1.2	5	µA
		Operating		150	300	
P_D	Power dissipation	VDD = 3.3 V		0.5		mW
		VDD = 2.0 V		0.3		

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 3.6 V (whichever is smaller) must be applied to this device. See 表 8-1 for more information.
(2) Includes all errors from onboard PGA, ADC, and voltage reference.

6.6 I²C Timing Requirements

over operating ambient temperature range, VDD = 2 V to 3.6 V, bus capacitance ≤ 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

		MIN	MAX	UNIT
STANDARD MODE				
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	4.0		µs
t_{LOW}	Pulse duration, SCL low	4.7		µs
t_{HIGH}	Pulse duration, SCL high	4.0		µs
$t_{SU;STA}$	Setup time, repeated START condition	4.7		µs
$t_{HD;DAT}$	Hold time, data	0		µs
$t_{SU;DAT}$	Setup time, data	0.25		µs
t_r	Rise time, SCL, SDA		1	µs
t_f	Fall time, SCL, SDA		0.3	µs
$t_{SU;STO}$	Setup time, STOP condition	4.0		µs
t_{BUF}	Bus free time, between STOP and START conditions	4.7		µs
$t_{VD;DAT}$	Valid time, data		3.45	µs
$t_{VD;ACK}$	Valid time, acknowledge		3.45	µs
FAST MODE				
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.	600		ns
t_{LOW}	Pulse duration, SCL low	1300		ns
t_{HIGH}	Pulse duration, SCL high	600		ns
$t_{SU;STA}$	Setup time, repeated START condition	600		ns
$t_{HD;DAT}$	Hold time, data	0		ns
$t_{SU;DAT}$	Setup time, data	100		ns
t_r	Rise time, SCL, SDA	20	300	ns
t_f	Fall time, SCL, SDA	20 × (VDD / 5.5 V)	300	ns
$t_{SU;STO}$	Setup time, STOP condition	600		ns
t_{BUF}	Bus free time, between STOP and START conditions	1300		ns
$t_{VD;DAT}$	Valid time, data		900	ns
$t_{VD;ACK}$	Valid time, acknowledge		900	ns
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter	0	50	ns

6.7 Timing Diagram

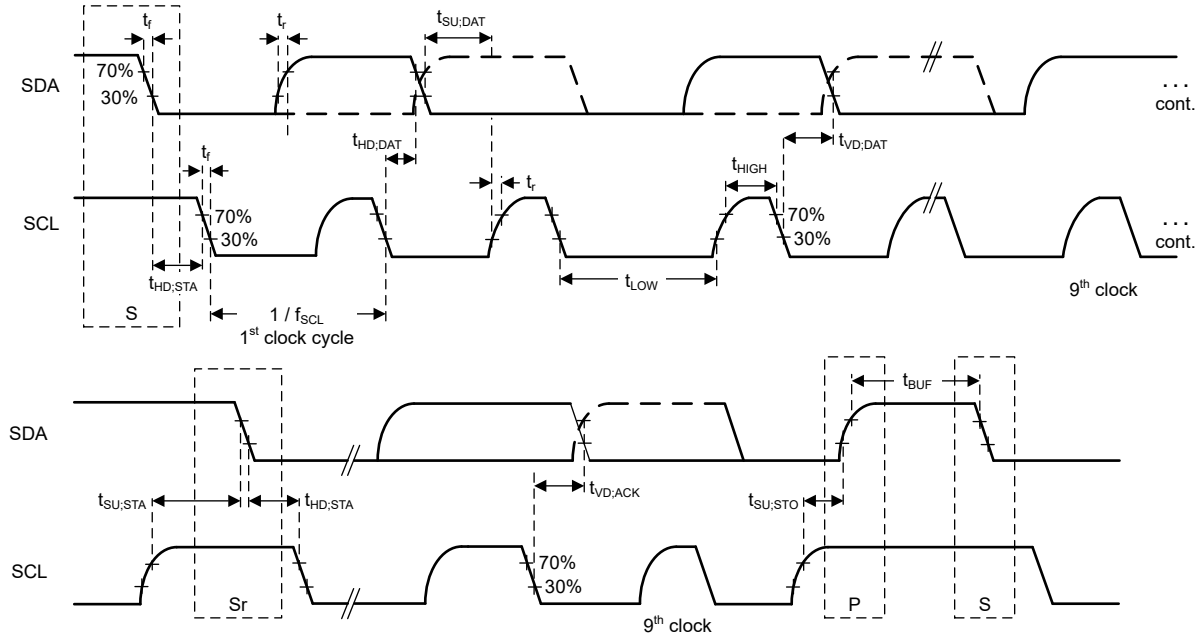
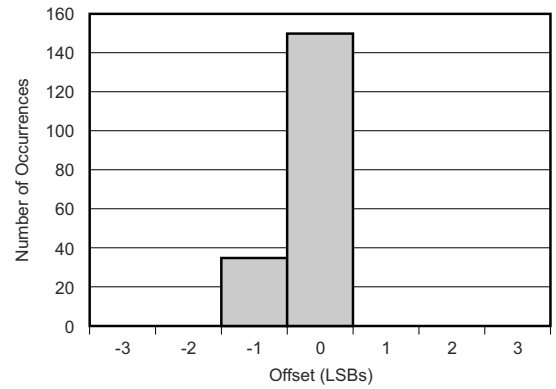


図 6-1. I²C Timing Requirements

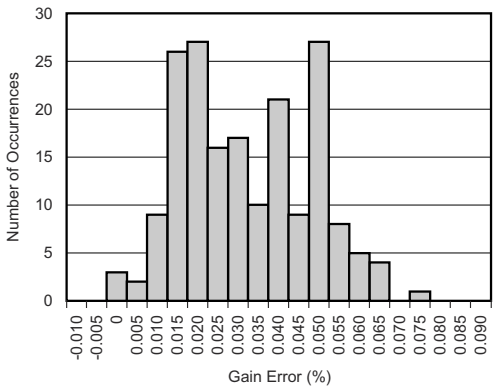
6.8 Typical Characteristics

at T_A = 25°C, VDD = 3.3 V, and DR = 8 SPS (unless otherwise noted)



FSR = ±2.048 V, 185 units

図 6-2. Offset Histogram



FSR = ±2.048 V, 185 units

図 6-3. Gain Error Histogram

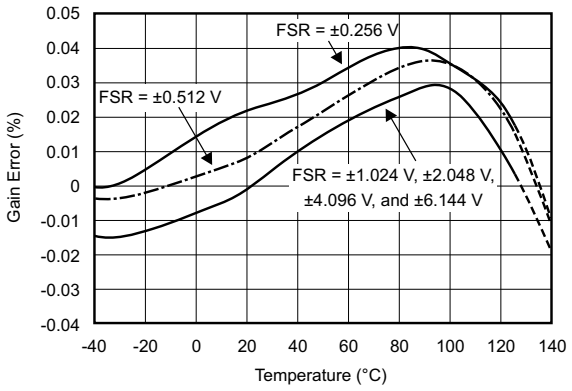
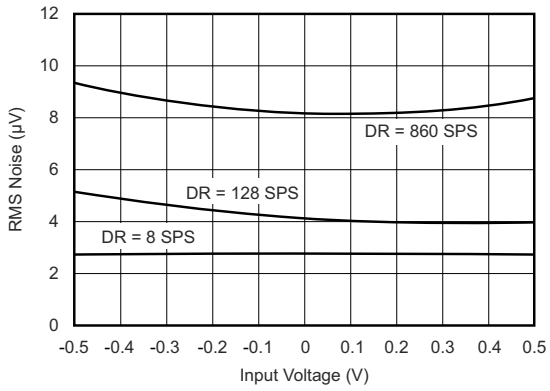


図 6-4. Gain Error vs Temperature



FSR = ±0.512 V

図 6-5. Noise vs Input Signal

7 Parameter Measurement Information

7.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

表 7-1 and 表 7-2 summarize the ADS111xL noise performance. Data are representative of typical noise performance at T_A = 25°C with the inputs shorted together externally. 表 7-1 shows the input-referred noise in units of μV_{RMS} for the conditions shown. The μV_{PP} values are shown in parenthesis. 表 7-2 shows the effective resolution calculated from μV_{RMS} values using 式 1. The noise-free resolution calculated from peak-to-peak noise values using 式 2 are shown in parenthesis.

$$\text{Effective Resolution} = \ln(\text{FSR} / V_{\text{RMS-Noise}}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln(\text{FSR} / V_{\text{PP-Noise}}) / \ln(2) \quad (2)$$

表 7-1. Noise in μV_{RMS} (μV_{PP}) at VDD = 3.3 V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
16	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
32	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
64	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (7.81)
128	187.5 (187.5)	125 (125)	62.5 (62.5)	31.25 (31.25)	15.62 (15.62)	7.81 (12.35)
250	187.5 (252.09)	125 (148.28)	62.5 (84.03)	31.25 (39.54)	15.62 (16.06)	7.81 (18.53)
475	187.5 (266.92)	125 (227.38)	62.5 (79.08)	31.25 (56.84)	15.62 (32.13)	7.81 (25.95)
860	187.5 (430.06)	125 (266.93)	62.5 (118.63)	31.25 (64.26)	15.62 (40.78)	7.81 (35.83)

表 7-2. Effective Resolution from RMS Noise (Noise-Free Resolution from Peak-to-Peak Noise) at VDD = 3.3 V

DATA RATE (SPS)	FSR (Full-Scale Range)					
	±6.144 V	±4.096 V	±2.048 V	±1.024 V	±0.512 V	±0.256 V
8	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
32	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
64	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
128	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.33)
250	16 (15.57)	16 (15.75)	16 (15.57)	16 (15.66)	16 (15.96)	16 (14.75)
475	16 (15.49)	16 (15.13)	16 (15.66)	16 (15.13)	16 (14.95)	16 (14.26)
860	16 (14.8)	16 (14.9)	16 (15.07)	16 (14.95)	16 (14.61)	16 (13.8)

8 Detailed Description

8.1 Overview

The ADS111xL are very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The ADS111xL consist of a ΔΣ ADC core with an internal voltage reference, a clock oscillator, and an I^2C interface. The ADS111xL also integrate a programmable gain amplifier (PGA) and a programmable digital comparator. 図 8-1 and 図 8-2 show the functional block diagrams of the ADS1114L and ADS1115L, respectively.

The ADS111xL ADC core measures a differential signal, V_{IN}, that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation of any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS111xL have two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request, stores the conversion value to an internal Conversion register, and then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

8.2 Functional Block Diagrams

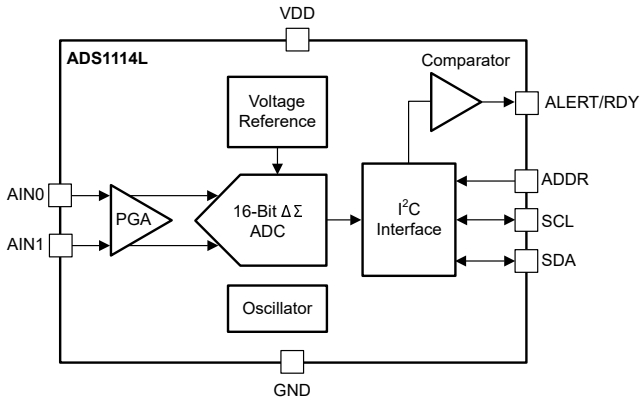


図 8-1. ADS1114L Block Diagram

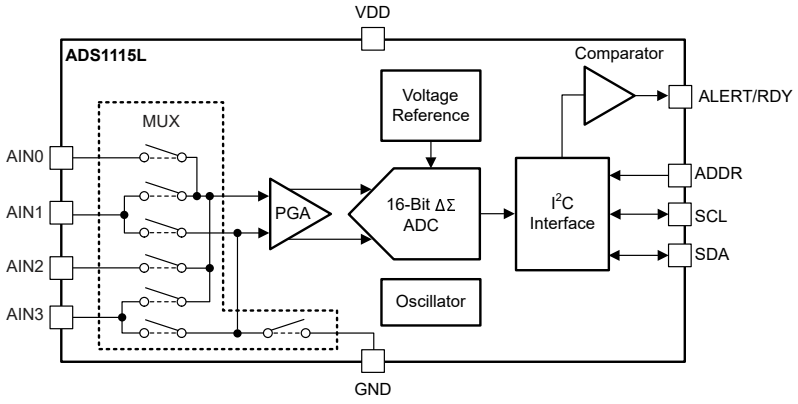


図 8-2. ADS1115L Block Diagram

8.3 Feature Description

8.3.1 Multiplexer

As shown in 図 8-3, the ADS1115L contains an input multiplexer (MUX). Either four single-ended or two differential signals can be measured. Additionally, AIN0 and AIN1 can be measured differentially to AIN3. The multiplexer is configured by the MUX[2:0] bits in the Configuration register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

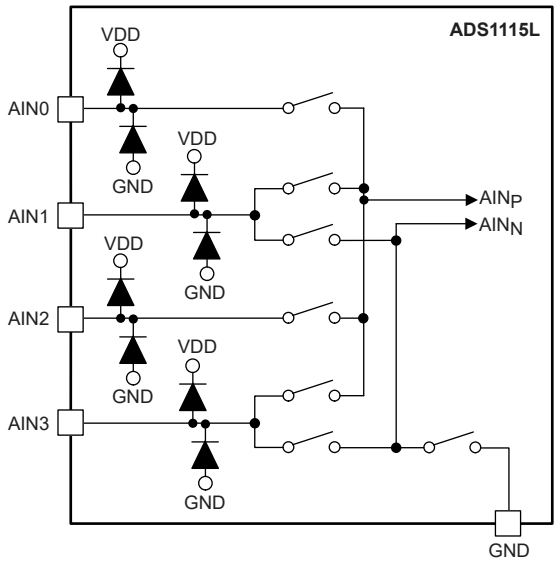


図 8-3. Input Multiplexer

The ADS1114L does not have an input multiplexer and can measure either one differential signal or one single-ended signal. For single-ended measurements, connect the AIN1 pin to GND externally. In subsequent sections of this document, AIN_P refers to AIN0 and AIN_N refers to AIN1 for the ADS1114L.

Electrostatic discharge (ESD) diodes connected to VDD and GND protect the ADS111xL analog inputs. Keep the absolute voltage of any input within the range shown in 式 3 to prevent the ESD diodes from turning on.

$$GND - 0.3\ V < V_{(AINX)} < VDD + 0.3\ V \quad (3)$$

If the voltages on the input pins can potentially violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings*). Overdriving an input on the ADS1115L can affect conversions taking place on other inputs. If overdriving an input is possible, clamp the signal with external Schottky diodes.

8.3.2 Analog Inputs

The ADS111xL use a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The frequency at which the input signal is sampled is called the *sampling frequency* or the *modulator frequency* (f_{MOD}). The ADS111xL has a 1-MHz internal oscillator that is further divided by a factor of 4 to generate f_{MOD} at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. 図 8-4 shows this structure. The capacitor values set the resistance and switching rate. 図 8-5 shows the timing for the switches in 図 8-4. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to $V_{(AINP)}$, C_{A2} to $V_{(AINN)}$, and C_B to ($V_{(AINP)} - V_{(AINN)}$). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS111xL analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

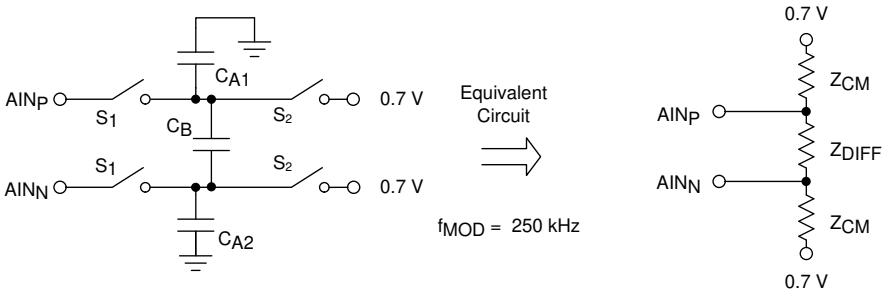


図 8-4. Simplified Analog Input Circuit

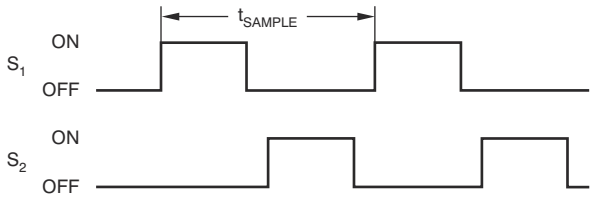


図 8-5. S_1 and S_2 Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 MΩ for the default full-scale range. In 図 8-4, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In 図 8-4, the differential input impedance is Z_{DIFF}.

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS111xL input impedance can affect measurement accuracy. For sources with high-output impedance, buffering can be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

8.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented before the ΔΣ ADC of the ADS111xL. The full-scale range is configured by the PGA[2:0] bits in the Configuration register and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, and ±0.256 V. 表 8-1 shows the FSR together with the corresponding LSB size. 式 4 shows how to calculate the LSB size from the selected full-scale range.

$$LSB = FSR / 2^{16} \quad (4)$$

表 8-1. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144 V(1)	187.5 µV
±4.096 V(1)	125 µV
±2.048 V	62.5 µV
±1.024 V	31.25 µV
±0.512 V	15.625 µV
±0.256 V	7.8125 µV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to the analog inputs of the device.

Analog input voltages must never exceed the analog input voltage limits given in the *Absolute Maximum Ratings*. The ±4.096-V and ±6.144-V full-scale range settings allow input voltages to extend up to the supply. Although in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be obtained. For example, with VDD = 3.3 V and FSR = ±4.096 V, only differential signals up to V_{IN} = ±3.3 V can be measured. The code range that represents voltages $|V_{IN}| > 3.3$ V is not used in this case.

8.3.4 Voltage Reference

The ADS111xL have an integrated voltage reference. An external reference cannot be used with these devices.

The ADS111xL do not use a traditional band-gap reference to generate the internal voltage reference. For that reason, the reference does not have an actual specified voltage value. Instead of using the reference voltage value and the gain setting to derive the full-scale range of the ADC, use the FSR values provided in 表 8-1 directly.

Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics* table.

8.3.5 Oscillator

The ADS111xL have an integrated oscillator running at 1 MHz. No external clock can be applied to operate these devices. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

8.3.6 Output Data Rate and Conversion Time

The ADS111xL offer programmable output data rates. Use the DR[2:0] bits in the Configuration register to select output data rates of 8 SPS, 16 SPS, 32 SPS, 64 SPS, 128 SPS, 250 SPS, 475 SPS, or 860 SPS.

Conversions in the ADS111xL settle within a single cycle; thus, the conversion time is equal to 1 / DR.

8.3.7 Digital Comparator

The ADS111xL features a programmable digital comparator that can issue an alert on the ALERT/RDY pin. The COMP_MODE bit in the Configuration register configures the comparator as either a traditional comparator or a window comparator. In traditional comparator mode, the ALERT/RDY pin asserts (active low by default) when conversion data exceed the limit set in the High-threshold register (Hi_thresh). The comparator then deasserts only when the conversion data falls below the limit set in the Low-threshold register (Lo_thresh). In window comparator mode, the ALERT/RDY pin asserts when the conversion data exceed the Hi_thresh register or fall below the Lo_thresh register value.

In either window or traditional comparator mode, the comparator can be configured to latch after being asserted by the COMP_LAT bit in the Configuration register. This setting causes the assertion to remain even if the input signal is not beyond the bounds of the threshold registers. This latched assertion can only be cleared by issuing an SMBus alert response or by reading the Conversion register. The ALERT/RDY pin can be configured as active high or active low by the COMP_POL bit in the Configuration register. 図 8-6 shows operational diagrams for both comparator modes.

The comparator can also be configured to activate the ALERT/RDY pin only after a set number of successive readings exceed the threshold values set in the threshold registers (Hi_thresh and Lo_thresh). The COMP_QUE[1:0] bits in the Configuration register configure the comparator to wait for one, two, or four readings beyond the threshold before activating the ALERT/RDY pin. The COMP_QUE[1:0] bits can also disable the comparator function and put the ALERT/RDY pin into a high state.

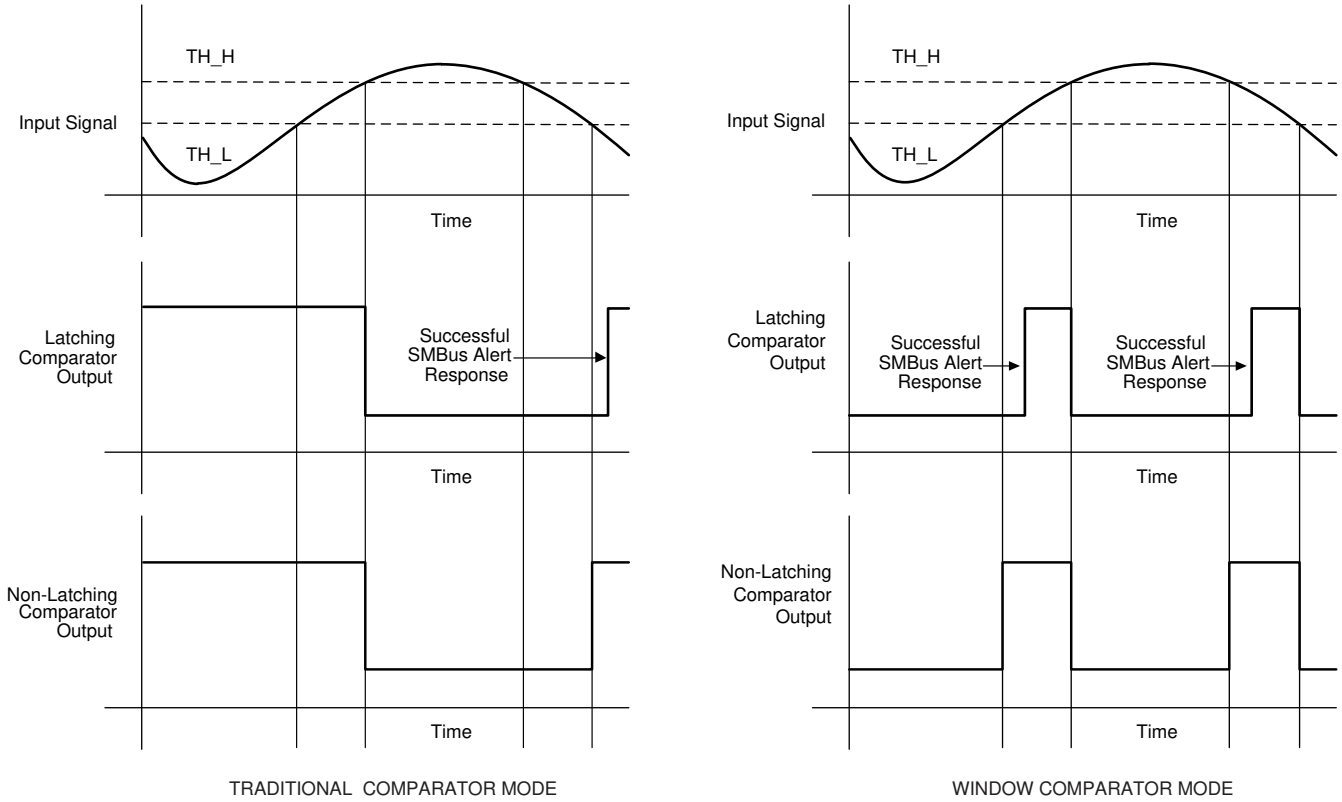


図 8-6. ALERT Pin Timing Diagram

8.3.8 Conversion-Ready Pin

The ALERT/RDY pin can also be configured as a conversion-ready pin. Set the most-significant bit of the Hi_thresh register to 1b and the most-significant bit of the Lo_thresh register to 0b to enable the pin as a conversion-ready pin. The COMP_POL bit continues to function as expected. Set the COMP_QUE[1:0] bits to any 2-bit value other than 11b to keep the ALERT/RDY pin enabled, and to allow the conversion-ready signal to appear at the ALERT/RDY pin output. The COMP_MODE and COMP_LAT bits no longer control any function. When configured as a conversion-ready pin, ALERT/RDY continues to require a pullup resistor. As shown in 図 8-7, the ADS111xL provides an approximate 8-µs conversion-ready pulse on the ALERT/RDY pin at the end of each conversion in continuous-conversion mode. In single-shot mode, the ALERT/RDY pin asserts low at the end of a conversion if the COMP_POL bit is set to 0b.

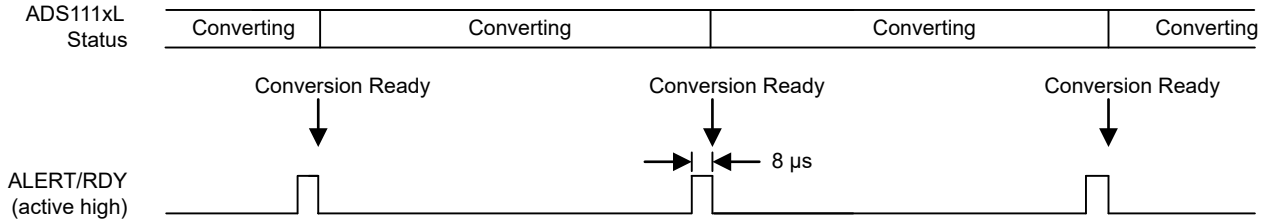


図 8-7. Conversion-Ready Pulse in Continuous-Conversion Mode

8.3.9 SMBus Alert Response

In latching comparator mode (COMP_LAT = 1b), the ALERT/RDY pin asserts when the comparator detects a conversion that exceeds the upper or lower threshold value. This assertion is latched and can be cleared only by reading conversion data, or by issuing a successful SMBus alert response and reading the asserting device I^2C address. If conversion data exceed the upper or lower threshold values after being cleared, the ALERT/RDY pin reasserts. This assertion does not affect conversions that are already in progress. The open-drain ALERT/RDY output allows several devices to share the same interface bus. When disabled, the ALERT/RDY pin holds a high state so that the pin does not interfere with other devices on the same bus line.

When the controller senses that the ALERT/RDY pin has latched, the controller issues an SMBus alert command (00011001b) to the I^2C bus. Any ADS111xL devices on the I^2C bus with the ALERT/RDY pins asserted respond to the command with the target address. If more than one ADS111xL on the I^2C bus assert the latched ALERT/RDY pin, arbitration during the address response portion of the SMBus alert determines which device clears assertion. The device with the lowest I^2C address always wins arbitration. If a device loses arbitration, the device does not clear the comparator output pin assertion. The controller then repeats the SMBus alert response until all devices have the respective assertions cleared. In window comparator mode, the SMBus alert status bit indicates a 1b if signals exceed the high threshold, and a 0b if signals exceed the low threshold.

8.4 Device Functional Modes

8.4.1 Reset and Power-Up

The ADS111xL resets on power-up and sets all bits in the Configuration register to the respective default settings. The ADS111xL enters a power-down state after the reset process completes. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS111xL relieves systems with tight power-supply requirements from encountering a surge during power-up.

The ADS111xL responds to the I^2C general-call reset commands. When the ADS111xL receives a general-call reset command (06h), an internal reset is performed as if the device is powered up.

8.4.2 Operating Modes

The ADS111xL operate in one of two modes: continuous-conversion or single-shot. The MODE bit in the Configuration register selects the respective operating mode.

8.4.2.1 Single-Shot Mode

When the MODE bit in the Configuration register is set to 1b, the ADS111xL enter a power-down state, and operate in single-shot mode. This power-down state is the default state for the ADS111xL when power is first applied. Although powered down, the devices still respond to commands. The ADS111xL remain in this power-down state until a 1b is written to the operational status (OS) bit in the Configuration register. When the OS bit is asserted, the device powers up in approximately 25 µs, resets the OS bit to 0b, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1b to the OS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0b to the MODE bit in the Configuration register.

8.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0b), the ADS111xL perform conversions continuously. When a conversion is complete, the ADS111xL place the result in the Conversion register and immediately begin another conversion. When writing new configuration settings, the currently ongoing conversion completes with the previous configuration settings. Thereafter, continuous conversions with the new configuration settings start. To switch to single-shot conversion mode, write a 1b to the MODE bit in the Configuration register or reset the device.

8.5 Programming

8.5.1 I²C Interface

The ADS111xL uses an inter-integrated circuit (I^2C) compatible interface for serial communication. I^2C is a 2-wire, open-drain communication interface that allows for communication between a controller device and multiple target devices on the same bus by using device addressing. Each target device on an I^2C bus must have a unique address. Communication on the I^2C bus always takes place between two devices: one acting as the controller and the other as the target. Both the controller and target can receive and transmit data, but the target can only read or write under the direction of the controller. The ADS111xL always acts as an I^2C target device.

An I^2C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. Devices on the I^2C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors; thus, the bus wires are always high when a device is not driving the lines low. As a result of this configuration, two devices do not conflict. If two devices drive the bus simultaneously, there is no driver contention.

See the *I^2C-Bus Specification and User Manual* from NXP Semiconductors™ for more details.

8.5.1.1 I^2C Address Selection

The ADS111xL has one address pin (ADDR) that configures the I^2C address of the device. The ADDR pin can connect to GND, VDD, SDA, or SCL (as shown in 表 8-2), which allows four different addresses to be selected with one pin. At the start of every transaction, that is between the START condition (first falling edge of SDA) and the first falling SCL edge of the address byte, the ADS111xL decodes the address configuration again.

Use the GND, VDD, or SCL connections first for address selection. If the SDA connection is used for address selection, hold the SDA line low for at least 100 ns after the SCL line goes low to make sure the device decodes the address correctly during I^2C communication.

表 8-2. ADDR Pin Connection and Corresponding Target Address

ADDR PIN CONNECTION	TARGET ADDRESS
GND	1001 000b
VDD	1001 001b
SDA	1001 010b
SCL	1001 011b

8.5.1.2 I^2C Interface Speed

The ADS111xL supports the following I^2C interface speeds: Standard-mode (Sm) with bit rates up to 100 kbit/s, and fast-mode (Fm) with bit rates up to 400 kbit/s. Fast-mode plus (Fm+) and high-speed mode (Hs-mode) are not supported.

8.5.1.2.1 Serial Clock (SCL) and Serial Data (SDA)

The serial clock (SCL) line clocks data in and out of the device. The controller always drives the clock line. The ADS111xL cannot act as a controller and, as a result, can never drive SCL.

The serial data (SDA) line allows for bidirectional communication between the host (the controller) and the ADS111xL (the target). When the controller reads from a ADS111xL device, the ADS111xL drives the data line; when the controller writes to a ADS111xL device, the controller drives the data line.

Data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the SCL line is low. One clock pulse is generated for each data bit transferred. When in an idle state, the controller should hold SCL high.

After the SDA line settles, the SCL line is brought high and then is brought low. This pulse on SCL clocks the SDA bit into the receiver shift register.

8.5.1.3 I²C Data Transfer Protocol

図 8-8 shows the format of the data transfer. The controller initiates all transactions with the ADS111xL by generating a START (S) condition. A high-to-low transition on the SDA line while SCL is high defines a START condition. The bus is considered to be busy after the START condition.

Following the START condition, the controller sends the 7-bit target address corresponding to the address of the ADS111xL that the controller wants to communicate with. The controller then sends an eighth bit that is a data-direction bit (R/$\overline{W}$). An R/$\overline{W}$ bit of 0b indicates a write operation, and an R/$\overline{W}$ bit of 1b indicates a read operation. After the R/$\overline{W}$ bit, the controller generates a ninth SCLK pulse and releases the SDA line to allow the ADS111xL to acknowledge (ACK) the reception of the target address by pulling SDA low. If the device does not recognize the target address, the ADS111xL holds SDA high to indicate a not acknowledge (NACK) signal.

Data transmission follows next in the process. If the transaction is a read (R/$\overline{W}$ = 1b), the ADS111xL outputs data on SDA. If the transaction is a write (R/$\overline{W}$ = 0b), the host outputs data on SDA. Data are transferred byte-wise, most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be acknowledged (with the ACK bit) by the receiver. If the transaction is a read, the controller issues the ACK bit. If the transaction is a write, the ADS111xL issues the ACK bit.

The controller terminates all transactions by generating a STOP (P) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The bus is considered free again t_{BUF} (bus-free time) after the STOP condition.

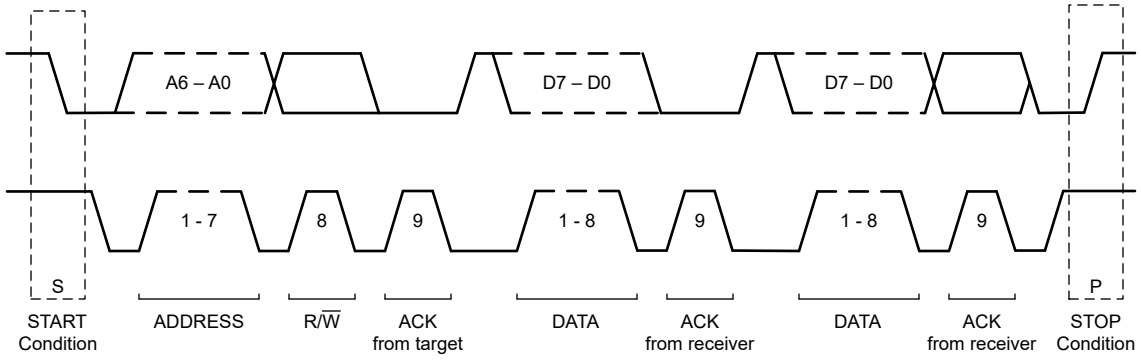


図 8-8. I²C Data Transfer Format

8.5.1.4 Timeout

The ADS111xL offer an I²C timeout feature that can be used to recover communication when a serial interface transmission is interrupted. If the host initiates contact with the ADS111xL but subsequently remains idle for 25 ms before completing a command, the ADS111xL interface is reset. If the ADS111xL interface resets because of a timeout condition, the host must abort the transaction and restart the communication again by issuing a new START condition.

8.5.1.5 I²C General-Call (Software Reset)

The ADS111xL respond to the I²C general-call address (0000 000b) if the R/$\overline{W}$ bit is 0b. The devices acknowledge the general-call address and, if the next byte is 06h, the ADS111xL reset the internal registers and enter a power-down state.

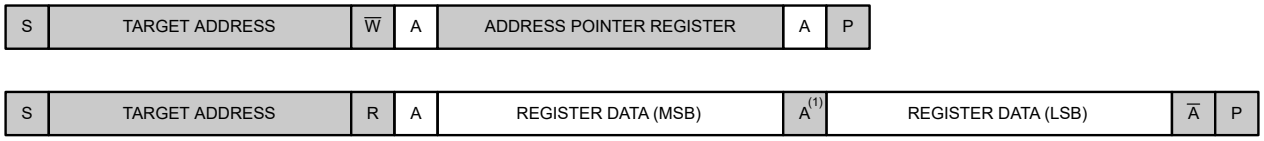
8.5.2 Reading and Writing Register Data

To access a specific register from the ADS111xL, the controller must first write an appropriate value to the register address pointer bits P[1:0] in the Address Pointer register. The Address Pointer register is written to directly after the target address byte, low R/$\overline{W}$ bit, and a successful target acknowledgment. After the Address Pointer register is written, the target acknowledges, and the controller issues a STOP or a repeated START condition.

8.5.2.1 Reading Conversion Data or the Configuration Register

Read the Conversion register or Configuration register as shown in 図 8-9 by using two I^2C communication frames. The first frame is an I^2C write operation where the R/$\overline{W}$ bit at the end of the target address is 0b to indicate a write. In this frame, the host sends the Address Pointer register that points to the register to read from. The second frame is an I^2C read operation where the R/$\overline{W}$ bit at the end of the target address is 1b to indicate a read. The ADS111xL transmits the contents of the register in this second I^2C frame. The controller can terminate the transmission after any byte by not acknowledging or issuing a START or STOP condition.

When repeatedly reading the same register, the Address Pointer register does not need to be written every time again because the ADS111xL store the value of the Address Pointer register until a write operation modifies the value.



The controller can terminate the transmission after the first byte by not acknowledging.

図 8-9. Reading Register Data

8.5.2.2 Writing the Configuration Register

Write the Configuration register (as shown in 図 8-10) using a single I^2C communication frame. The R/$\overline{W}$ bit at the end of the target address is 0b to indicate a write. The host first sends the Address Pointer register that points to the Configuration register, followed by two bytes that represent the register content to write. The ADS111xL acknowledge each received byte.

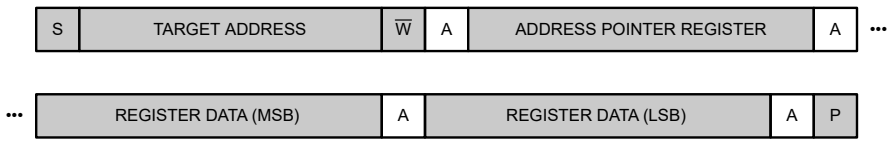


図 8-10. Writing Register Data

図 8-11 provides a legend for 図 8-9 and 図 8-10.

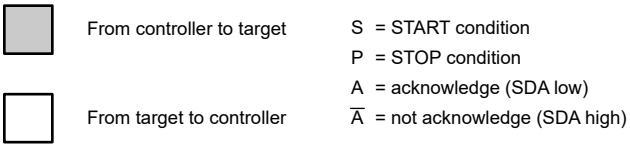


図 8-11. Legend for the I^2C Sequence Diagrams

8.5.3 Data Format

The ADS111xL provides 16 bits of data in binary two's-complement format. A positive full-scale (+FS) input produces an output code of 7FFFh and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. 表 8-3 summarizes the ideal output codes for different input signals. 図 8-12 shows code transitions versus input voltage.

表 8-3. Input Signal Versus Ideal Output Code

INPUT SIGNAL $V_{IN} = (V_{AINP} – V_{AINN})$	IDEAL OUTPUT CODE(1)
≥ +FS $(2^{15} – 1) / 2^{15}$	7FFFh
+FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

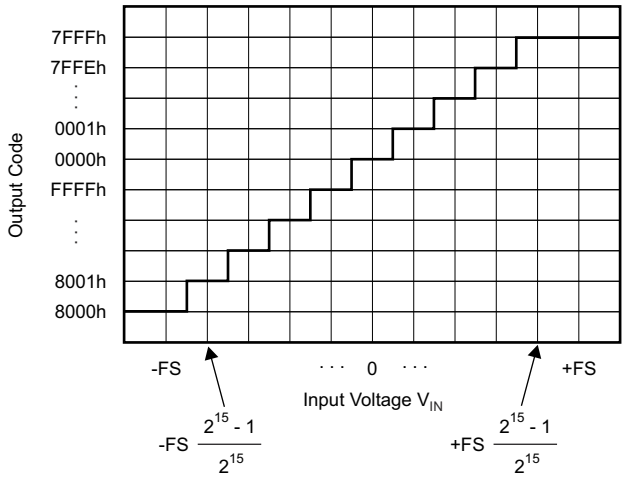


図 8-12. Code Transition Diagram

注

Single-ended signal measurements, where V_{AINN} = 0 V and V_{AINP} = 0 V to +FS, only use the positive code range from 0000h to 7FFFh. However, because of device offset, the ADS111xL can still output negative codes if V_{AINP} is close to 0 V.

9 Register Map

The ADS111xL has four registers that are accessible through the I²C interface using the Address Pointer register. The Conversion register contains the result of the last conversion. The Configuration register is used to change the ADS111xL operating modes and query the device status. The other two registers, Lo_thresh and Hi_thresh, set the threshold values used for the comparator function.

9.1 Address Pointer Register (address = N/A) [reset = N/A]

All four registers are accessed by writing to the Address Pointer register.

図 9-1. Address Pointer Register

7	6	5	4	3	2	1	0
RESERVED						P[1:0]	
W-000000b						W-00b	

表 9-1. Address Pointer Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	W	000000b	Always write 000000b
1:0	P[1:0]	W	00b	**Register address pointer** 00b : Conversion register 01b : Configuration register 10b : Lo_thresh register 11b : Hi_thresh register

9.2 Conversion Register (P[1:0] = 00b) [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary two's-complement format. Following power-up, the Conversion register is cleared to 0000h, and remains 0000h until the first conversion completes.

図 9-2. Conversion Register

15	14	13	12	11	10	9	8
D[15:8]							
R-00h							
7	6	5	4	3	2	1	0
D[7:0]							
R-00h							

表 9-2. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

9.3 Configuration Register (P[1:0] = 01b) [reset = 8583h]

The 16-bit Configuration register controls the operating mode, input selection, data rate, full-scale range, and comparator modes.

図 9-3. Configuration Register: ADS1114L

15	14	13	12	11	10	9	8
OS	RESERVED			PGA[2:0]			MODE
R/W-1b	R/W-000b			R/W-010b			R/W-1b
7	6	5	4	3	2	1	0
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-100b			R/W-0b	R/W-0b	R/W-0b	R/W-11b	

図 9-4. Configuration Register: ADS1115L

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1b	R/W-000b			R/W-010b			R/W-1b
7	6	5	4	3	2	1	0
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-100b			R/W-0b	R/W-0b	R/W-0b	R/W-11b	

表 9-3. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OS	R/W	1b	**Operational status or single-shot conversion start** This bit determines the operational status of the device. OS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0b : No effect 1b : Start a single conversion (when in power-down state) When reading: 0b : Device is currently performing a conversion 1b : Device is not currently performing a conversion
14:12	MUX[2:0]	R/W	000b	**Input multiplexer configuration (ADS1115L only)** These bits configure the input multiplexer. *These bits serve no function on the ADS1114L. The ADS1114L always uses inputs AIN_P = AIN0 and AIN_N = AIN1.* 000b : AIN_P = AIN0 and AIN_N = AIN1 001b : AIN_P = AIN0 and AIN_N = AIN3 010b : AIN_P = AIN1 and AIN_N = AIN3 011b : AIN_P = AIN2 and AIN_N = AIN3 100b : AIN_P = AIN0 and AIN_N = GND 101b : AIN_P = AIN1 and AIN_N = GND 110b : AIN_P = AIN2 and AIN_N = GND 111b : AIN_P = AIN3 and AIN_N = GND
11:9	PGA[2:0]	R/W	010b	**Programmable gain amplifier configuration** These bits set the FSR of the programmable gain amplifier. 000b : FSR = ±6.144 V(1) 001b : FSR = ±4.096 V(1) 010b : FSR = ±2.048 V 011b : FSR = ±1.024 V 100b : FSR = ±0.512 V 101b : FSR = ±0.256 V 110b : FSR = ±0.256 V 111b : FSR = ±0.256 V
8	MODE	R/W	1b	**Device operating mode** This bit controls the operating mode. 0b : Continuous-conversion mode 1b : Single-shot mode or power-down state

表 9-3. Configuration Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
7:5	DR[2:0]	R/W	100b	**Data rate** These bits control the data rate setting. 000b : 8 SPS 001b : 16 SPS 010b : 32 SPS 011b : 64 SPS 100b : 128 SPS 101b : 250 SPS 110b : 475 SPS 111b : 860 SPS
4	COMP_MODE	R/W	0b	**Comparator mode** This bit configures the comparator operating mode. 0b : Traditional comparator 1b : Window comparator
3	COMP_POL	R/W	0b	**Comparator polarity** This bit controls the polarity of the ALERT/RDY pin. 0b : Active low 1b : Active high
2	COMP_LAT	R/W	0b	**Latching comparator** This bit controls whether the ALERT/RDY pin latches after being asserted or clears after conversions are within the margin of the upper and lower threshold values. 0b : Nonlatching comparator. The ALERT/RDY pin does not latch when asserted. 1b : Latching comparator. The asserted ALERT/RDY pin remains latched until conversion data are read by the controller or an appropriate SMBus alert response is sent by the controller. The device responds with an address, and is the lowest address currently asserting the ALERT/RDY bus line.
1:0	COMP_QUE[1:0]	R/W	11b	**Comparator queue and disable** These bits perform two functions. When set to 11b, the comparator is disabled and the ALERT/RDY pin is set to a high-impedance state. When set to any other value, the ALERT/RDY pin and the comparator function are enabled, and the set value determines the number of successive conversions exceeding the upper or lower threshold required before asserting the ALERT/RDY pin. 00b : Assert after one conversion 01b : Assert after two conversions 10b : Assert after four conversions 11b : Disable the comparator and set the ALERT/RDY pin to high impedance

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to the analog inputs of the device.

9.4 Lo_thresh (P[1:0] = 10b) [reset = 8000h] and Hi_thresh (P[1:0] = 11b) [reset = 7FFFh] Registers

The upper and lower threshold values used by the comparator are stored in two 16-bit registers in two's-complement format. The comparator is implemented as a digital comparator; therefore, the values in these registers must be updated whenever the PGA settings are changed.

The conversion-ready function of the ALERT/RDY pin is enabled by setting the Hi_thresh register MSB to 1b and the Lo_thresh register MSB to 0b. To use the comparator function of the ALERT/RDY pin, the Hi_thresh register value must always be greater than the Lo_thresh register value. The threshold register formats are shown in the Lo_thresh Register and Hi_thresh Register. When set to RDY mode, the ALERT/RDY pin outputs the OS bit when in single-shot mode, and provides a continuous-conversion ready pulse when in continuous-conversion mode.

図 9-5. Lo_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh[15:8]							
R/W-80h							
7	6	5	4	3	2	1	0
Lo_thresh[7:0]							
R/W-00h							

図 9-6. Hi_thresh Register

15	14	13	12	11	10	9	8
Hi_thresh[15:8]							
R/W-7Fh							
7	6	5	4	3	2	1	0
Hi_thresh[7:0]							
R/W-FFh							

表 9-4. Lo_thresh and Hi_thresh Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Lo_thresh[15:0]	R/W	8000h	Low threshold value
15:0	Hi_thresh[15:0]	R/W	7FFFh	High threshold value

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The following sections give example circuits and suggestions for using the ADS111xL in various situations.

10.1.1 Basic Connections

図 10-1 shows the principle I²C connections for the ADS1115L.

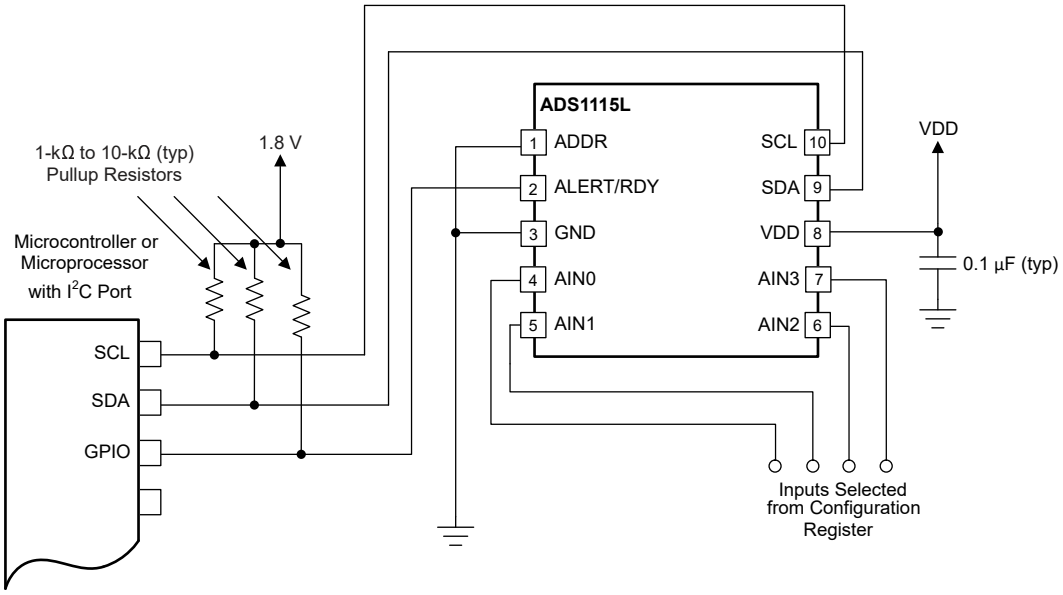


図 10-1. Typical Connections of the ADS1115L

The fully differential voltage input of the ADS111xL is designed for connection to differential sources with moderately low source impedance, such as thermocouples and thermistors. Although the ADS111xL can read bipolar differential signals, these devices cannot accept negative voltages on either input.

The ADS111xL draws transient currents during conversion. A 0.1-µF power-supply bypass capacitor supplies the momentary bursts of extra current required from the supply.

The ADS111xL interfaces directly to standard mode and fast mode I²C controllers. Any microcontroller I²C peripheral, including controller-only and single-controller I²C peripherals, operates with the ADS111xL. The ADS111xL does not perform clock-stretching (that is, the device never pulls the clock line low), so this function does not need to be provided for unless other clock-stretching devices are on the same I²C bus.

Pullup resistors are required on both the SDA and SCL lines because I²C bus drivers are open drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, thus limiting the bus speed. Lower-value resistors allow higher speed, but at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. Do not use resistors that are too small to avoid bus drivers being unable to pull the bus lines low.

10.1.2 Unused Inputs and Outputs

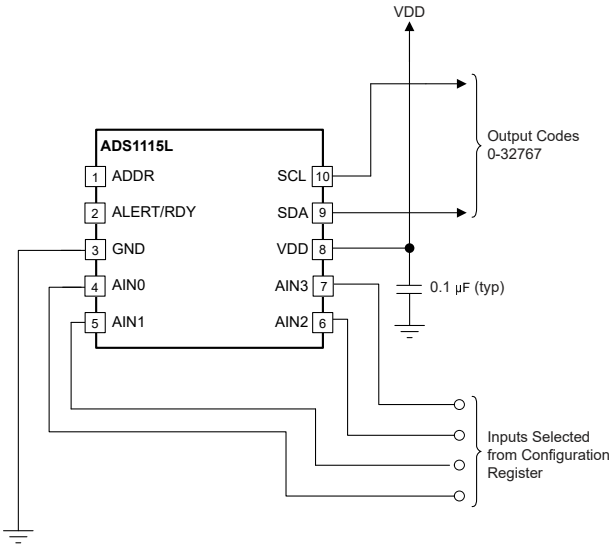
Follow the guidelines below for the connection of unused device pins:

- Either float unused analog inputs, or tie unused analog inputs to GND
- Either float NC (not connected) pins, or tie the NC pins to GND
- If the ALERT/RDY output pin is not used, leave this pin unconnected or tie this pin to VDD using a weak pullup resistor

10.1.3 Single-Ended Inputs

The ADS1114L can measure one, and the ADS1115L up to four, single-ended signals. The ADS1114L can measure single-ended signals by connecting AIN1 to GND externally. The ADS1115L measures single-ended signals by appropriate configuration of the MUX[2:0] bits in the Configuration register. 図 10-2 shows a single-ended connection scheme for the ADS1115L. The single-ended signal ranges from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to these devices because the ADS111xL can only accept positive voltages with respect to ground. The ADS111xL do not lose linearity within the input range.

The ADS111xL offer a differential input voltage range of ±FSR. Single-ended configurations use only one-half of the full-scale input voltage range. Differential configurations maximize the dynamic range of the ADC, and provide better common-mode noise rejection than single-ended configurations.



NOTE: Digital pin connections omitted for clarity.

図 10-2. Measuring Single-Ended Inputs

The ADS1115L also allows AIN3 to serve as a common point for measurements by appropriate setting of the MUX[2:0] bits. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1115L operates with inputs, where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

10.1.4 Input Protection

The ADS111xL are fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS111xL can be permanently damaged by analog input voltages that exceed approximately 300 mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS111xL analog inputs can withstand continuous currents as large as 10 mA.

10.1.5 Analog Input Filtering

Analog input filtering serves two purposes:

1. Limits the effect of aliasing during the sampling process
2. Reduces external noise from being a part of the measurement

Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter, as shown in 図 10-3, repeats at multiples of the sampling frequency, also known as the modulator frequency (f_{MOD}). Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency, or multiples thereof, are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

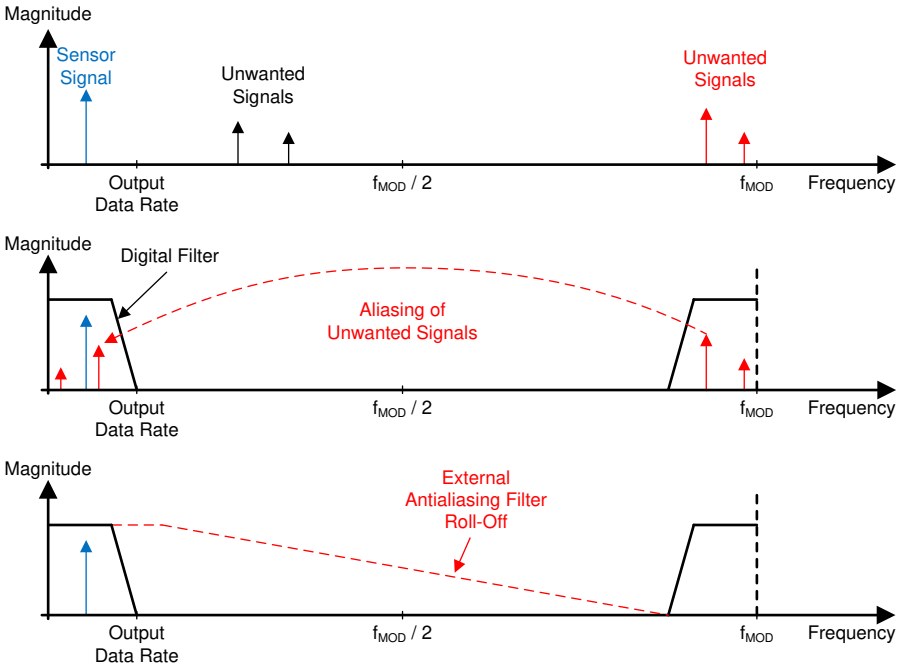


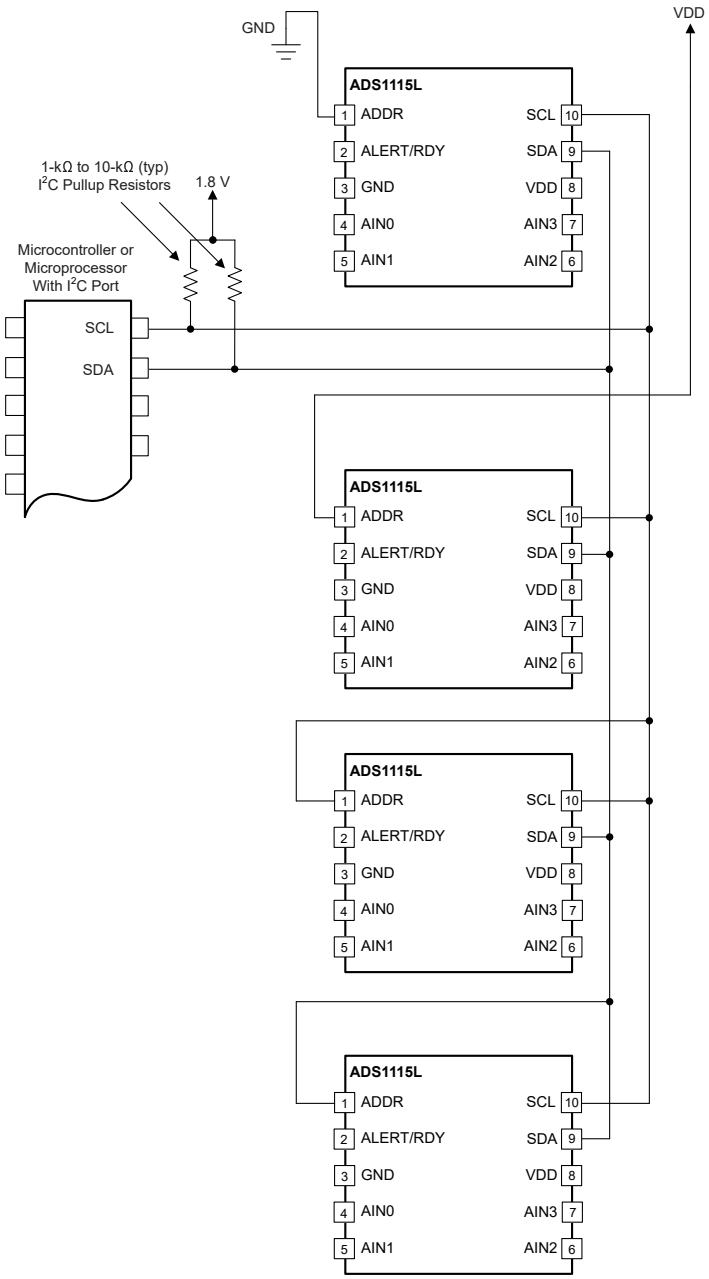
図 10-3. Effect of Aliasing

Many sensor signals are inherently band-limited (for example, the output of a thermocouple has a limited rate of change). In this case, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Generally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS111xL attenuates signals to a certain degree. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

10.1.6 Connecting Multiple Devices

Up to four ADS111xL devices can be connected to a single I²C bus using different address pin configurations for each device. Use the address pin to set the ADS111xL to one of four different I²C addresses. Use the GND, VDD, and SCL addresses first. If SDA is used as the device address, hold the SDA line low for at least 100 ns after the SCL line goes low to make sure the device decodes the address correctly during I²C communication. 図 10-4 shows an example of four ADS111xL devices on the same I²C bus. One set of pullup resistors is required per bus. If needed, lower the pullup resistor values to compensate for the additional bus capacitance presented by multiple devices and increased line length.



NOTE: The ADS111xL power and input connections are omitted for clarity. The ADDR pin selects the I²C address.

図 10-4. Connecting Multiple ADS111xL Devices

10.1.7 Duty Cycling For Low Power

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates is not always required. For these applications, the ADS111xL supports duty cycling that yields significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS111xL in power-down state with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). A conversion at 860 SPS only requires approximately 1.2 ms, so the ADS111xL enters power-down state for the remaining 123.8 ms. In this configuration, the ADS111xL consumes approximately 1/100th the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is completely arbitrary and is defined by the controller. The ADS111xL offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.

10.1.8 I²C Communication Sequence Example

This section provides an example of an I²C communication sequence between a microcontroller (the controller) and a ADS111xL (the target) configured with a target address of 1001 000b to start a single-shot conversion and subsequently read the conversion result.

1. Write the Configuration register as shown in 図 10-6 to configure the device (for example, when using the ADS1115L, write MUX[2:0] = 000b, PGA[2:0] = 010b, MODE = 1b, and DR[2:0] = 110b) and start a single-shot conversion (OS = 1b).

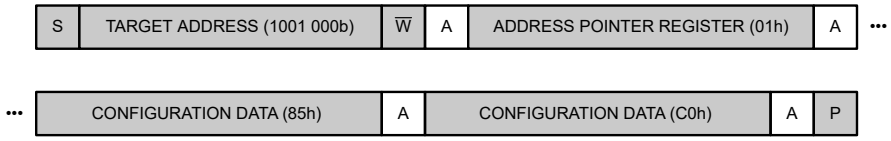


図 10-5. Write the Configuration Register

2. Wait at least t = 1 / DR ± 10% for the conversion to complete.

   Alternatively, poll the OS bit for a 1b as shown in 図 10-6 to determine when the conversion result is ready for retrieval. This option does not work in continuous-conversion mode because the OS bit always reads 0b.

図 10-6. Read the Configuration Register to Check for OS = 1b

3. Then, as shown in 図 10-7, read the Conversion register.

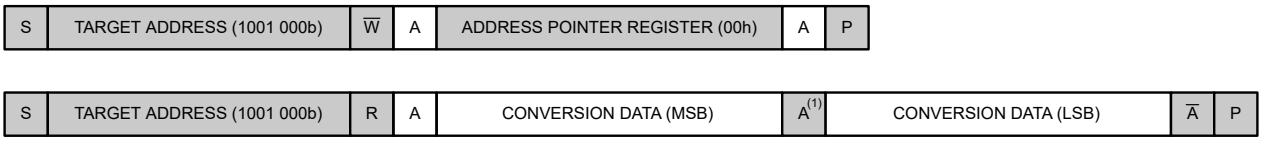


図 10-7. Read the Conversion Register

4. Start a new single-shot conversion by writing a 1b to the OS bit in the Configuration register.

   To save time, a new conversion can also be started (step 4) before reading the conversion result (step 3). 図 10-8 lists a legend for 図 10-5 to 図 10-7.

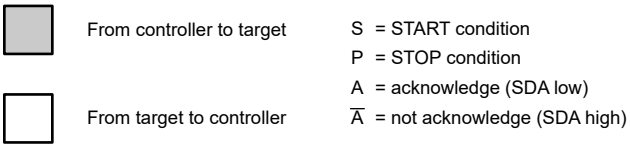


図 10-8. Legend for the I²C Sequence Diagrams

10.2 Typical Application

This application example describes how to use the ADS1115L to monitor two different supply voltage rails in a system. 図 10-9 shows a typical implementation for monitoring two supply voltage rails.

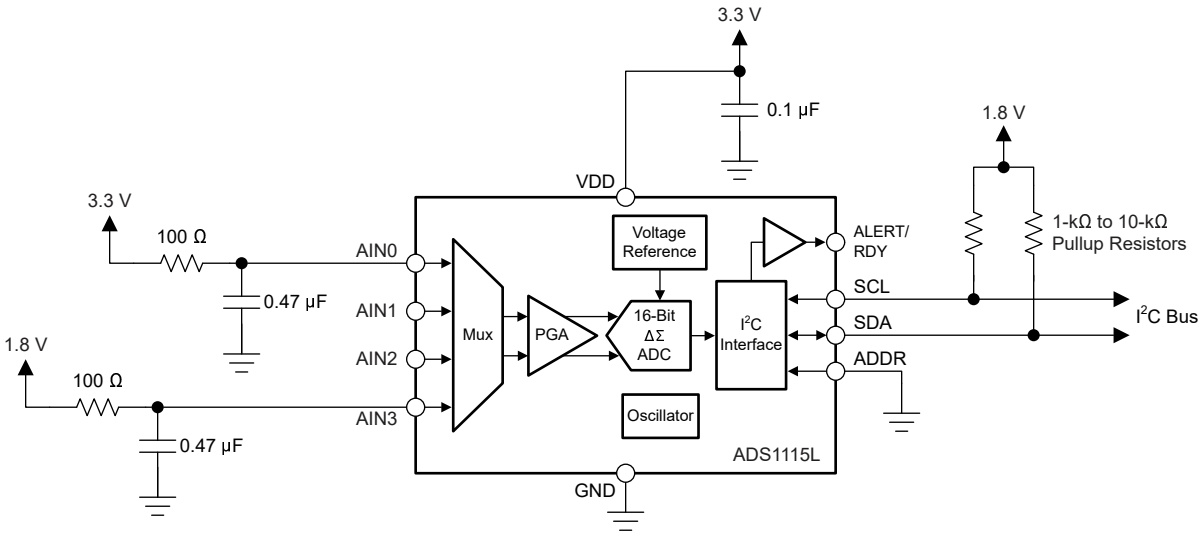


図 10-9. Monitoring Two Supply Voltage Rails Using the ADS1115L

10.2.1 Design Requirements

表 10-1 lists the design requirements for this application.

表 10-1. Design Requirements

DESIGN PARAMETER	VALUE
Device supply voltage	3.3 V
Voltage rails to monitor	1.8 V, 3.3 V
Measurement accuracy	±0.5%
Update rate	5 ms per rail

10.2.2 Detailed Design Procedure

The analog inputs, AIN0 and AIN3, connect directly to the supply voltage rails that are monitored through RC filter resistors. Small filter resistor values of 100 Ω are chosen to reduce voltage drops (and therefore offset errors) caused by the input currents of the ADS1115L to a minimum. Filter capacitors of 0.47 µF are chosen to set the filter cutoff frequencies at 3.39 kHz. To get one reading from each of the two supplies within 10 ms, a data rate of 860 SPS is selected. The device is set up for single-ended measurements using MUX[2:0] settings 100b and 101b. An FSR = ±4.096 V is selected to measure the 3.3-V rail. The same FSR can also be used to measure the 1.8-V rail or the FSR can be set to FSR = ±2.048 V.

10.2.3 Application Curve

The measurement results in 図 10-10 show that the two supplies can be measured with ±0.5% accuracy over the complete operating ambient temperature range without any offset or gain calibration.

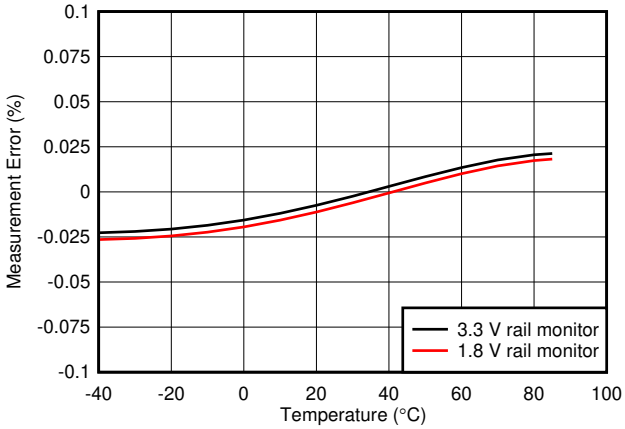


図 10-10. Measurement Error vs Temperature

10.3 Power Supply Recommendations

The device requires a single unipolar supply, VDD, to power both the analog and digital circuitry of the device.

10.3.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

10.3.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in 図 10-11, VDD must be decoupled with at least a 0.1-µF capacitor. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the device is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, do not use vias to connect capacitors to the device pins for better noise immunity. Using multiple vias in parallel lowers the overall inductance, and is beneficial for connections to ground planes.

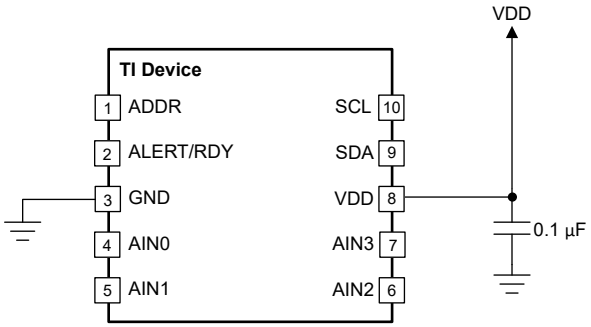


図 10-11. ADS1115L Power-Supply Decoupling

10.4 Layout

10.4.1 Layout Guidelines

Employ best design practices when laying out a printed circuit board (PCB) for both analog and digital components. For optimal performance, separate the analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. 図 10-12 shows an example of good component placement. Although 図 10-12 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

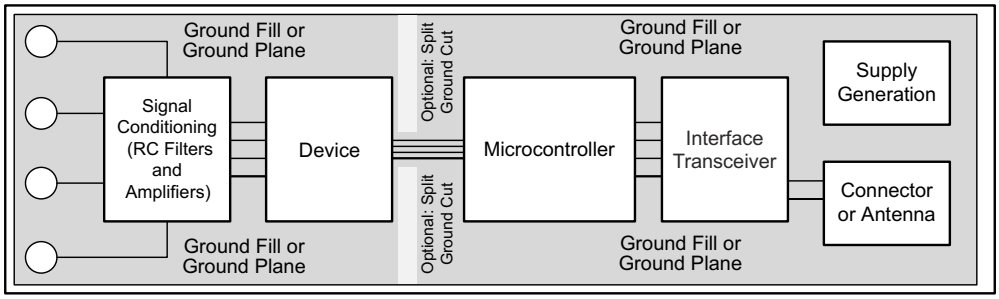


図 10-12. System Component Placement

The following outlines some basic recommendations for the layout of the ADS111xL to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This placement prevents digital noise from coupling back into analog signals.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, the current must find another path to return to the source and complete the circuit. A longer return current path increases the chance that the signal radiates. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reduce the loop area enclosed by the source signal and the return current to reduce the inductance in the path. Reduce the inductance to reduce the EMI pickup, and reduce the high-frequency impedance observed by the device.
- Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as AIN0, AIN1 and AIN2, AIN3). The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low-noise characteristics.

10.4.2 Layout Example

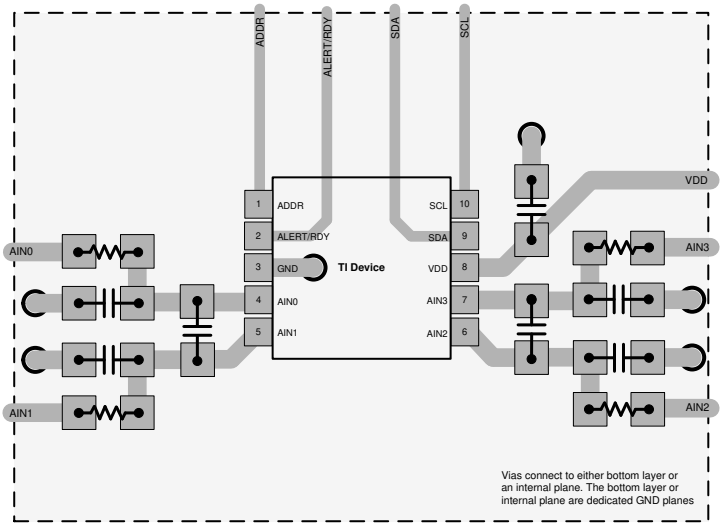


図 10-13. ADS1115L VSSOP Package

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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11.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1114LIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	114L	Samples
ADS1115LIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	115L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

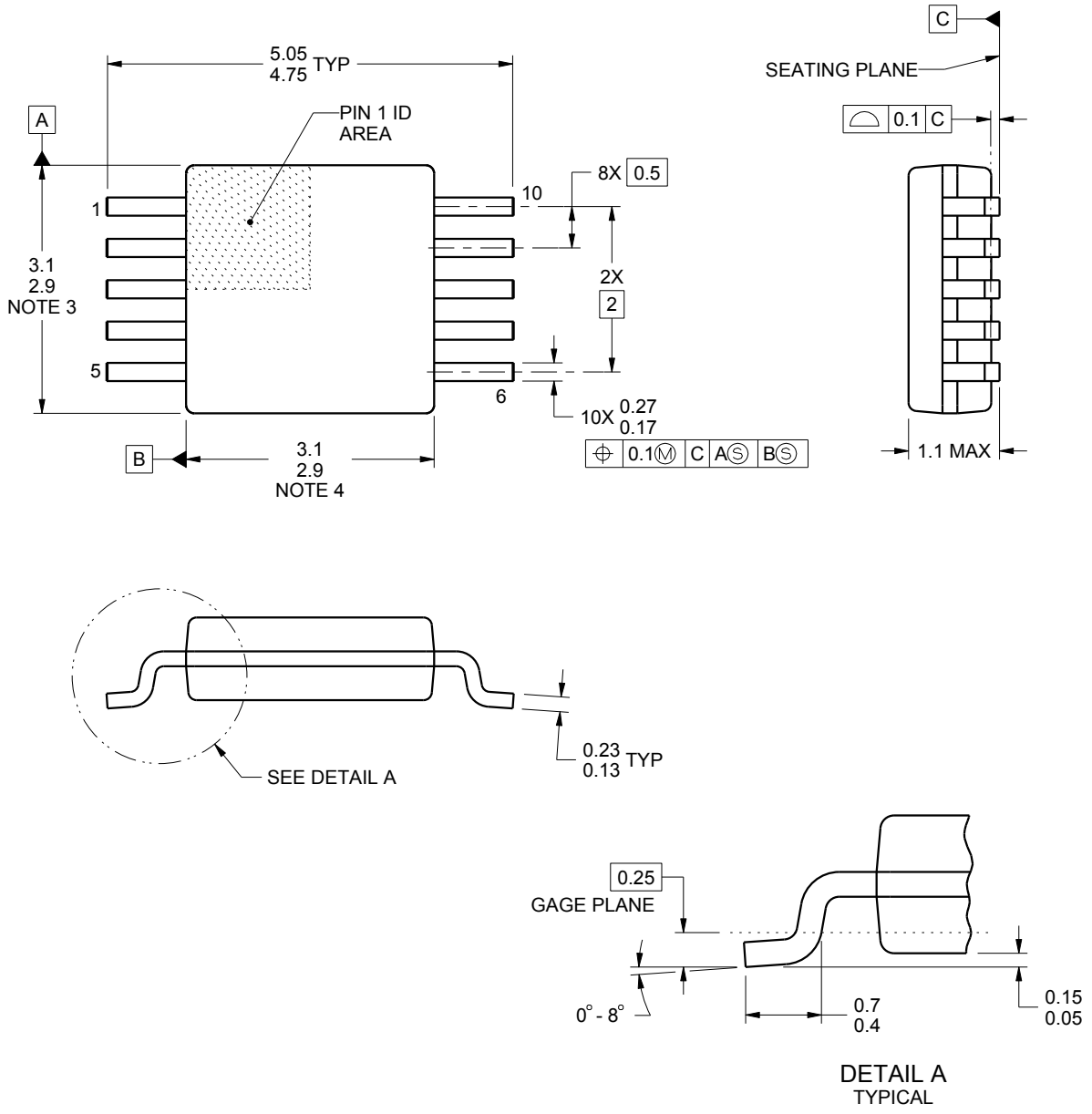
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGS0010A

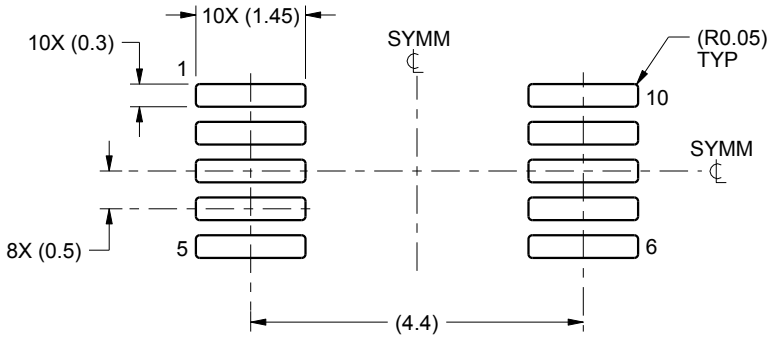
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

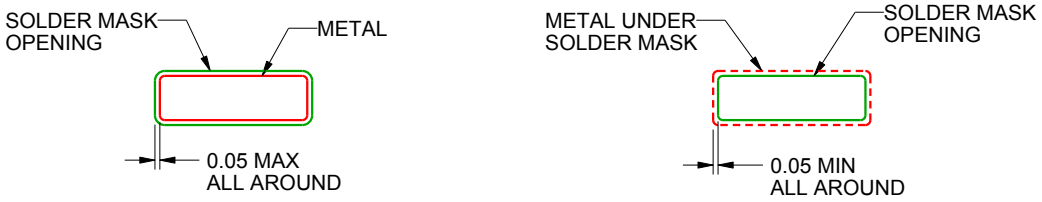


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

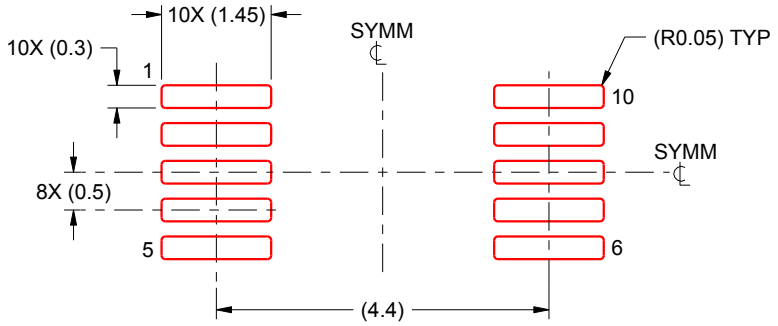


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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