

ADS1204 4つの1ビット、10 MHz、2次、デルタ-シグマ変調器

1 特長

- 16ビットの分解能
- 14ビットの直線性
- 分解能と速度のトレードオフ：
10ビットの実効分解能で10 μ sの信号遅延 (12ビットで19 μ s)
- 2.5Vで ± 2.5 Vの入力範囲
- 内部基準電圧：2%
- ゲイン誤差：0.5%
- 4つの独立したデルタ-シグマ変調器
- 4つの入力参照バッファ
- オンボードの20MHz発振器
- 内部または外部クロックを選択可能
- 動作温度範囲：
-40 $^{\circ}$ C \sim +105 $^{\circ}$ C
- パッケージ：VQFN-32 (5mm x 5mm)

2 アプリケーション

- モータ制御
- 電流測定
- 産業用プロセス制御
- スマート・トランスミッタ
- 重量計
- 圧カトランスデューサ
- 携帯型計測機器
- 計装機器

3 概要

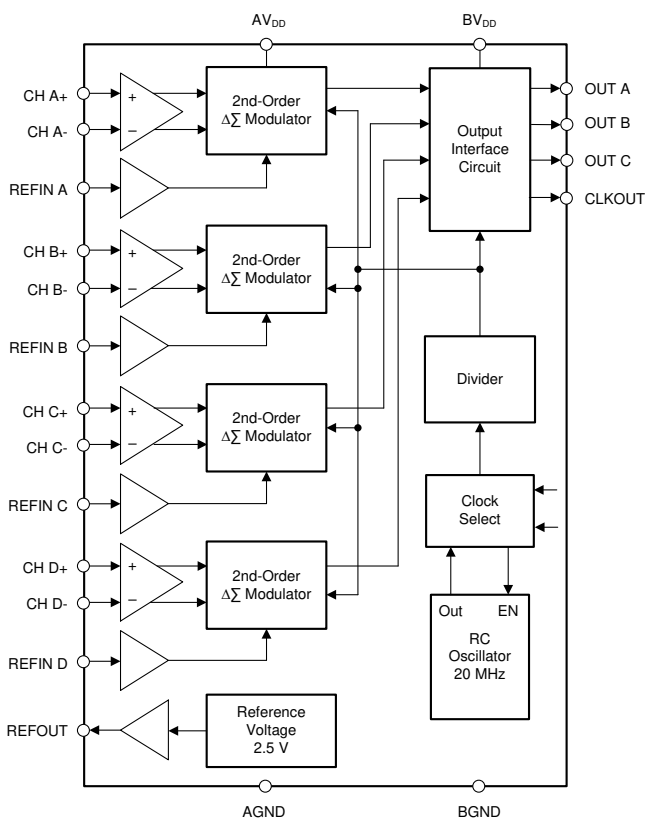
ADS1204は、100dBのダイナミックレンジを持つ4つのデルタ-シグマ ($\Delta\Sigma$) 変調器を備えた4チャンネル高性能デバイスであり、5V単一電源で動作します。差動入力、産業用環境でトランスデューサに直接接続するのに理想的です。適切なデジタル・フィルタおよび変調器レートにより、このデバイスでは、ノー・ミッシング・コードで16ビットのA/D変換を実現できます。デジタル・フィルタのデータ・レート160kHz、変調器レート10MHzにおいて12ビットの実効分解能が得られます。ADS1204は、電流測定、スマート・トランスミッタ、産業用プロセス制御、重量計、クロマトグラフィー、携帯型計測機器などの中～高分解能の測定アプリケーション向けに設計されています。このデバイスはVQFN-32 (5x5) パッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
ADS1204	VQFN (32)	5.00mmx5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (February 2009) から Revision D に変更

Page

• 「製品情報」表、ページ 1 の図、「ESD 定格」表、「熱に関する情報」表、「概要」セクション、「機能ブロック図」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• ドキュメント全体を通して QFN を VQFN に変更	1
• 「アプリケーション」セクションを変更	1
• Deleted <i>Ordering Information</i> table	5
• Changed <i>Power dissipation</i> to point to <i>Thermal Information</i> table instead, added unit	5
• Changed <i>External clock</i> maximum specification from 24 MHz to 32 MHz in <i>Recommended Operating Conditions</i> table	6
• Changed footnote in <i>Recommended Operating Conditions</i> table	6
• Deleted <i>Dissipation Ratings</i> table	6
• Changed <i>External clock frequency</i> maximum specification from 24 MHz to 32 MHz in <i>Electrical Characteristics</i> table	7
• Changed <i>CLKIN period</i> minimum specification from 41.6 ns to 31.25 ns in <i>Timing Requirements: 5.0 V</i> table	9
• Changed NOM column to MAX column in <i>Timing Requirements: 5.0 V</i> table	9
• Changed BV _{DD} from 5 V to 3 V in <i>Timing Requirements: 3.0 V</i> test conditions	9
• Changed <i>CLKIN period</i> minimum specification from 41.6 ns to 31.25 ns in <i>Timing Requirements: 3.0 V</i> table	9
• Changed <i>Layout</i> section	22

Revision B (August 2007) から Revision C に変更

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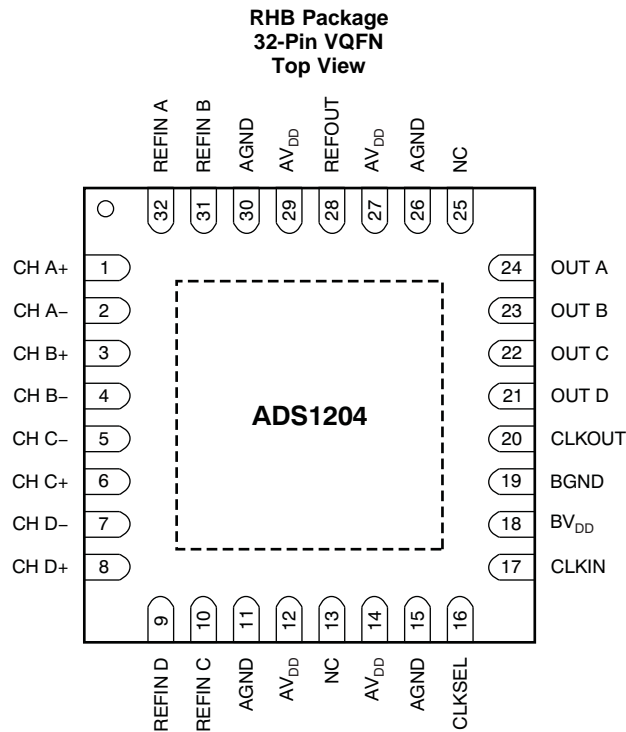
• ドキュメントの書式を更新	1
• ドキュメント全体を通して動作温度範囲を +85°C から +105°C に拡張	1
• Deleted operating free-air temperature range row from <i>Absolute Maximum Ratings</i> table	5
• Added free-air temperature range ratings to <i>Recommended Operating Conditions</i> table	6
• Changed <i>Dissipation Ratings</i> table	6
• Changed typical specification in <i>Input capacitance</i> row of <i>Analog Input</i> section of <i>Electrical Characteristics</i> table	6
• Added additional specification for Total Harmonic Distortion in <i>AC Accuracy</i> section of <i>Electrical Characteristics</i> table	6

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- Deleted test condition of V_{OUT} row in *Voltage Reference Output* section of *Electrical Characteristics* table 6
 - Updated typical characteristic graphs to reflect extended temperature range 10
-

Revision A (June 2004) から Revision B に変更**Page**

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- Added note to QFN package 4
-

5 Pin Configuration and Functions



NOTE: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
CH A+	1	AI	Analog input of channel A: noninverting input
CH A-	2	AI	Analog input of channel A: inverting input
CH B+	3	AI	Analog input of channel B: noninverting input
CH B-	4	AI	Analog input of channel B: inverting input
CH C-	5	AI	Analog input of channel C: inverting input
CH C+	6	AI	Analog input of channel C: noninverting input
CH D-	7	AI	Analog input of channel D: inverting input
CH D+	8	AI	Analog input of channel D: noninverting input
REFIN D	9	AI	Reference voltage input of channel D: pin for external reference voltage
REFIN C	10	AI	Reference voltage input of channel C: pin for external reference voltage
AGND	11	—	Analog ground
AVDD	12	P	Analog power supply; nominal 5 V
NC	13	—	No connection; this pin is left unconnected
AV _{DD}	14	P	Analog power supply; nominal 5 V
AGND	15	—	Analog ground
CLKSEL	16	I	Clock select between internal clock (CLKSEL = 1) or external clock (CLKSEL = 0)
CLKIN	17	I	External clock input
BV _{DD}	18	P	Digital interface power supply; from 2.7 V to 5.5 V
BGND	19	—	Interface ground
CLKOUT	20	O	System clock output

(1) AI = analog input; AO = analog output; I = input; O = output; P = power supply.

Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
OUT D	21	O	Bit stream from channel D modulator
OUT C	22	O	Bit stream from channel C modulator
OUT B	23	O	Bit stream from channel B modulator
OUT A	24	O	Bit stream from channel A modulator
NC	25	—	No connection; this pin is left unconnected
AGND	26	—	Analog ground
AV _{DD}	27	P	Analog power supply; nominal 5 V
REFOUT	28	AO	Reference voltage output: output pin of the internal reference source; nominal 2.5 V
AV _{DD}	29	P	Analog power supply; nominal 5 V
AGND	30	—	Analog ground
REFIN B	31	AI	Reference voltage input of channel B: pin for external reference voltage
REFIN A	32	AI	Reference voltage input of channel A: pin for external reference voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	AV _{DD} to AGND	−0.3	6	V
	BV _{DD} to BGND	−0.3	6	
Analog input voltage with respect to AGND		AGND − 0.3	AV _{DD} + 0.3	V
Reference input voltage with respect to AGND		AGND − 0.3	AV _{DD} + 0.3	V
Digital input voltage with respect to BGND		BGND − 0.3	BV _{DD} + 0.3	V
Ground voltage difference, AGND to BGND			±0.3	V
Voltage differences, BV _{DD} to AGND		−0.3	6	V
Input current to any pin except supply			±10	mA
Power dissipation		See the Thermal Information		A
Temperature	Operating virtual junction, T _J	−40	+150	°C
	Storage, T _{stg}	−65	+150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AVDD to AGND		4.75	5	5.25	V
Supply voltage, BVDD to BGND	Low-voltage levels	2.7		3.6	V
	5V logic levels	4.5	5	5.5	V
Reference input voltage		0.5	2.5	2.6	V
Operating common-mode signal		0		AV _{DD}	V
Analog inputs	+IN – (–IN)	0		±REFIN	V
External clock ⁽¹⁾		16	20	32	MHz
Operating free-air temperature range, T _A		–40		+125	°C
Specified free-air temperature range, T _A		–40		+105	°C

(1) Analog performance is degraded at clock frequencies > 20 MHz; see the [Typical Characteristics](#) section for details.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS1204	UNIT
		RHB (VQFN)	
		32 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	28.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	9.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	9.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range at –40°C to +105°C, AV_{DD} = 5 V, BV_{DD} = 3 V, CH x+ = 0.5 V to 4.5 V, CH x– = 2.5 V, REFIN = REFOUT = internal 2.5 V, CLKIN = 20 MHz, and 16-bit sinc³ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral linearity error ⁽²⁾			±1	±3	LSB
				±0.001	±0.005	% FSR
	Integral linearity match				±6	LSB
					±0.009	% FSR
DNL	Differential nonlinearity ⁽³⁾				±1	LSB
V _{OS}	Input offset error			–1.4	±3	mV
	Input offset error match				±2	mV
TCV _{OS}	Input offset error drift			±2	±8	μV/°C
G _{ERR}	Gain error ⁽⁴⁾	Referenced to V _{REF}		±0.08	±0.5	% FSR
	Gain error match			±0.185	±0.5	% FSR
TCG _{ERR}	Gain error drift			±2		ppm/°C
PSRR	Power-supply rejection ratio	4.75 V < AV _{DD} < 5.25 V		78		dB

(1) All typical values are at T_A = +25°C.

(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for CH x+ = –2 V to +2 V at 2.5 V, expressed either as the number of LSBs or as a percent of measured input range (4 V).

(3) Specified by design.

(4) Maximum values, including temperature drift, are specified over the full specified temperature range.

Electrical Characteristics (continued)

over recommended operating free-air temperature range at -40°C to $+105^{\circ}\text{C}$, $\text{AV}_{\text{DD}} = 5\text{ V}$, $\text{BV}_{\text{DD}} = 3\text{ V}$, $\text{CH x+} = 0.5\text{ V}$ to 4.5 V , $\text{CH x-} = 2.5\text{ V}$, $\text{REFIN} = \text{REFOUT} = \text{internal } 2.5\text{ V}$, $\text{CLKIN} = 20\text{ MHz}$, and 16-bit sinc³ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale differential range	(CH x+) – (CH x–); CH x– = 2.5 V			±2.5	V
	Specified differential range	(CH x+) – (CH x–); CH x– = 2.5 V			±2	V
	Maximum operating input range ⁽³⁾		0		AV_{DD}	V
	Input capacitance	Common-mode		1.5		pF
	Input leakage current	CLK turned off			±1	nA
	Differential input resistance			100		kΩ
	Differential input capacitance			2.5		pF
CMRR	Common-mode rejection ratio	At DC		100		dB
		$V_{\text{IN}} = \pm 1.25 V_{\text{PP}}$ at 40 kHz		110		
BW	Bandwidth	FS sine wave, –3 dB		50		MHz
SAMPLING DYNAMICS						
	Internal clock frequency	CLKSEL = 1	8	10	12	MHz
CLKIN	External clock frequency	CLKSEL = 0	1	20	32	MHz
AC ACCURACY						
THD	Total harmonic distortion	$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 5 kHz; $-40^{\circ}\text{C} \leq T_{\text{A}} \leq +85^{\circ}\text{C}$		–96	–88	dB
		$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 5 kHz; $-40^{\circ}\text{C} \leq T_{\text{A}} \leq +105^{\circ}\text{C}$		–96	–87	
SFDR	Spurious-free dynamic range	$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 5 kHz	92	100		dB
SNR	Signal-to-noise ratio	$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 5 kHz	86	89		dB
SINAD	Signal-to-noise + distortion	$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 5 kHz	85	89		dB
	Channel-to-channel isolation ⁽³⁾	$V_{\text{IN}} = \pm 2 V_{\text{PP}}$ at 50 kHz		85		dB
ENOB	Effective number of bits		14	14.5		Bits
VOLTAGE REFERENCE OUTPUT						
V_{OUT}	Reference voltage output		2.450	2.5	2.550	V
dV_{OUT}/dT	Output voltage temperature drift			±20		ppm/°C
	Output voltage noise	$f = 0.1\text{ Hz to } 10\text{ Hz}$, $C_{\text{L}} = 10\text{ }\mu\text{F}$		10		μVrms
		$f = 10\text{ Hz to } 10\text{ kHz}$, $C_{\text{L}} = 10\text{ }\mu\text{F}$		12		
PSRR	Power-supply rejection ratio			60		dB
I_{OUT}	Output current			10		μA
I_{SC}	Short-circuit current			0.5		mA
	Turn-on settling time	To 0.1% at $C_{\text{L}} = 0$		100		μs
VOLTAGE REFERENCE INPUT						
V_{IN}	Reference voltage input		0.5	2.5	2.6	V
	Reference input resistance			100		MΩ
	Reference input capacitance			5		pF
	Reference input current				1	μA
DIGITAL INPUTS⁽⁵⁾						
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	High-level input voltage		$0.7 \times \text{BV}_{\text{DD}}$		$\text{BV}_{\text{DD}} + 0.3$	V
V_{IL}	Low-level input voltage		–0.3		$0.3 \times \text{BV}_{\text{DD}}$	V
I_{IN}	Input current	$V_{\text{I}} = \text{BV}_{\text{DD}}$ or GND			±50	nA
C_{I}	Input capacitance			5		pF

(5) Applicable for 5.0-V nominal supply: BV_{DD} (min) = 4.5 V and BV_{DD} (max) = 5.5 V.

Electrical Characteristics (continued)

over recommended operating free-air temperature range at -40°C to $+105^{\circ}\text{C}$, $\text{AV}_{\text{DD}} = 5\text{ V}$, $\text{BV}_{\text{DD}} = 3\text{ V}$, $\text{CH}_{\text{x}+} = 0.5\text{ V}$ to 4.5 V , $\text{CH}_{\text{x}-} = 2.5\text{ V}$, $\text{REFIN} = \text{REFOUT} = \text{internal } 2.5\text{ V}$, $\text{CLKIN} = 20\text{ MHz}$, and 16-bit sinc³ filter with decimation by 256 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DIGITAL OUTPUTS⁽⁵⁾						
	Logic family		CMOS			
V_{OH}	High-level output voltage	$\text{BV}_{\text{DD}} = 4.5\text{ V}$, $I_{\text{OH}} = -100\text{ }\mu\text{A}$	4.44			V
V_{OL}	Low-level output voltage	$\text{BV}_{\text{DD}} = 4.5\text{ V}$, $I_{\text{OL}} = 100\text{ }\mu\text{A}$			0.5	V
C_{O}	Output capacitance			5		pF
C_{L}	Load capacitance				30	pF
	Data format		Bit stream			
DIGITAL INPUTS⁽⁶⁾						
	Logic family		LVCMOS			
V_{IH}	High-level input voltage	$\text{BV}_{\text{DD}} = 3.6\text{ V}$	2		$\text{BV}_{\text{DD}} + 0.3$	V
V_{IL}	Low-level input voltage	$\text{BV}_{\text{DD}} = 2.7\text{ V}$	-0.3		0.8	V
I_{IN}	Input current	$V_{\text{I}} = \text{BV}_{\text{DD}}$ or GND			± 50	nA
C_{I}	Input capacitance			5		pF
DIGITAL OUTPUTS⁽⁶⁾						
	Logic family		LVCMOS			
V_{OH}	High-level output voltage	$\text{BV}_{\text{DD}} = 2.7\text{ V}$, $I_{\text{OH}} = -100\text{ }\mu\text{A}$	$\text{BV}_{\text{DD}} - 0.2$			V
V_{OL}	Low-level output voltage	$\text{BV}_{\text{DD}} = 2.7\text{ V}$, $I_{\text{OL}} = 100\text{ }\mu\text{A}$			0.2	V
C_{O}	Output capacitance			5		pF
C_{L}	Load capacitance				30	pF
	Data format		Bit stream			
POWER SUPPLY						
AV_{DD}	Analog supply voltage		4.5		5.5	V
BV_{DD}	Buffer I/O supply voltage	Low-voltage levels	2.7		3.6	V
		5-V logic levels	4.5		5.5	
AI_{DD}	Analog operating supply current	$\text{CLKSEL} = 1$		22.5	30	mA
		$\text{CLKSEL} = 0$		22.4	29	
BI_{DD}	Buffer I/O operating supply current	$\text{BV}_{\text{DD}} = 3\text{ V}$, $\text{CLKOUT} = 10\text{ MHz}$			4	mA
		$\text{BV}_{\text{DD}} = 5\text{ V}$, $\text{CLKOUT} = 10\text{ MHz}$			4	
	Power dissipation	$\text{CLKSEL} = 0$		122	145	mW
		$\text{CLKSEL} = 1$		112.5	150	

(6) Applicable for 3.0-V nominal supply: BV_{DD} (min) = 2.7 V and BV_{DD} (max) = 3.6 V.

6.6 Timing Requirements: 5.0 V⁽¹⁾

over recommended operating free-air temperature range at -40°C to $+105^{\circ}\text{C}$, $\text{AV}_{\text{DD}} = 5\text{ V}$, and $\text{BV}_{\text{DD}} = 5\text{ V}$ (unless otherwise noted)

		MIN	MAX	UNIT
t_{C1}	CLKIN period	31.25	1000	ns
t_{W1}	CLKIN high time	10	$t_{\text{C1}} - 10$	ns
t_{C2}	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	$2 \times t_{\text{C1}}$		ns
t_{W2}	CLKOUT high time	$(t_{\text{C2}} / 2) - 5$	$(t_{\text{C2}} / 2) + 5$	ns
t_{D1}	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
t_{D2}	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	$(t_{\text{C2}} / 4) - 8$	$(t_{\text{C2}} / 4) + 8$	ns
t_{D4}	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	$t_{\text{W1}} - 3$	$t_{\text{W1}} + 7$	ns

(1) Applicable for 5.0-V nominal supply: $\text{BV}_{\text{DD}}(\text{min}) = 4.5\text{ V}$ and $\text{BV}_{\text{DD}}(\text{max}) = 5.5\text{ V}$. All input signals are specified with $t_{\text{R}} = t_{\text{F}} = 5\text{ ns}$ (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{\text{IL}} + V_{\text{IH}}) / 2$. See Figure 1.

6.7 Timing Requirements: 3.0 V⁽¹⁾

over recommended operating free-air temperature range at -40°C to $+105^{\circ}\text{C}$, $\text{AV}_{\text{DD}} = 5\text{ V}$, and $\text{BV}_{\text{DD}} = 3\text{ V}$ (unless otherwise noted)

		MIN	MAX	UNIT
t_{C1}	CLKIN period	31.25	1000	ns
t_{W1}	CLKIN high time	10	$t_{\text{C1}} - 10$	ns
t_{C2}	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	$2 \times t_{\text{C1}}$		ns
t_{W2}	CLKOUT high time	$(t_{\text{C2}} / 2) - 5$	$(t_{\text{C2}} / 2) + 5$	ns
t_{D1}	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
t_{D2}	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	$(t_{\text{C2}} / 4) - 8$	$(t_{\text{C2}} / 4) + 8$	ns
t_{D4}	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	$t_{\text{W1}} - 3$	$t_{\text{W1}} + 7$	ns

(1) Applicable for 3.0V nominal supply: $\text{BV}_{\text{DD}}(\text{min}) = 2.7\text{ V}$ and $\text{BV}_{\text{DD}}(\text{max}) = 3.6\text{ V}$. All input signals are specified with $t_{\text{R}} = t_{\text{F}} = 5\text{ ns}$ (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{\text{IL}} + V_{\text{IH}}) / 2$. See Figure 1.

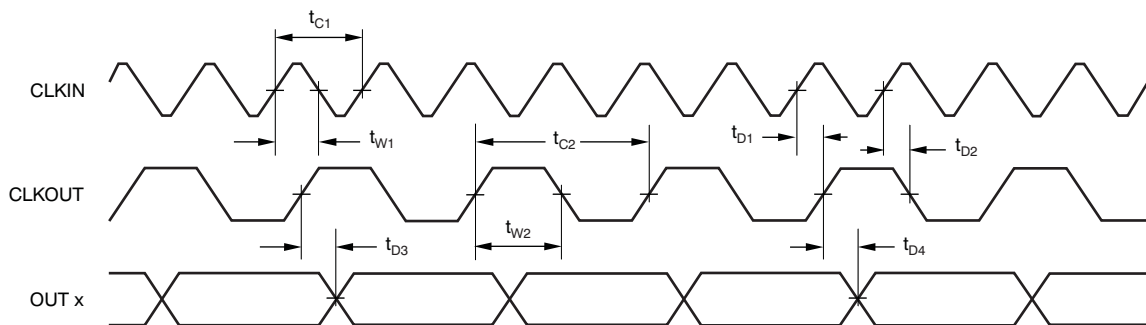


Figure 1. ADS1204 Timing Diagram

6.8 Typical Characteristics

$AV_{DD} = 5\text{ V}$, $BV_{DD} = 3\text{ V}$, $CH_{x+} = 0.5\text{ V to }4.5\text{ V}$, $CH_{x-} = 2.5\text{ V}$, $REFIN = \text{external}$, $CLKSEL = 0$, and 16-bit sinc³ filter, with $OSR = 256$ (unless otherwise noted)

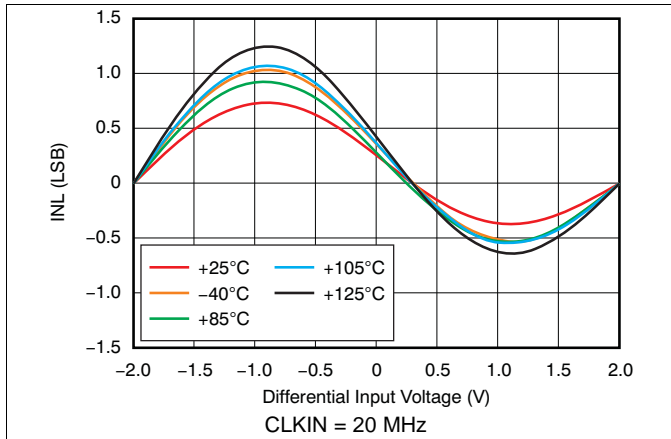


Figure 2. Integral Nonlinearity vs Input Signal

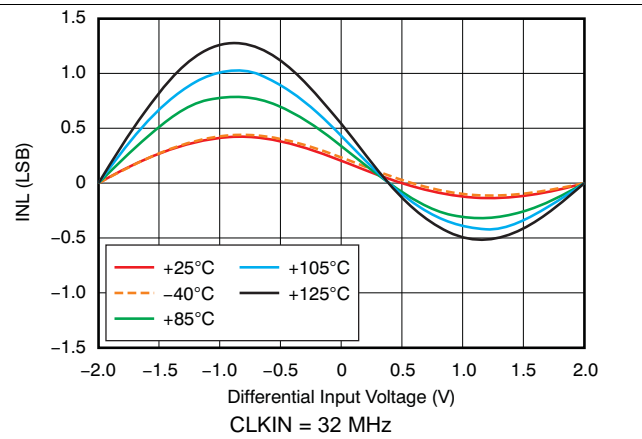


Figure 3. Integral Nonlinearity vs Input Signal

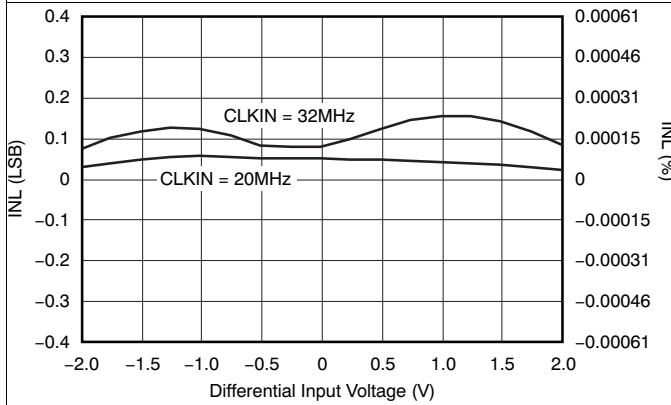


Figure 4. Integral Linearity Match of Channels vs Input Signal

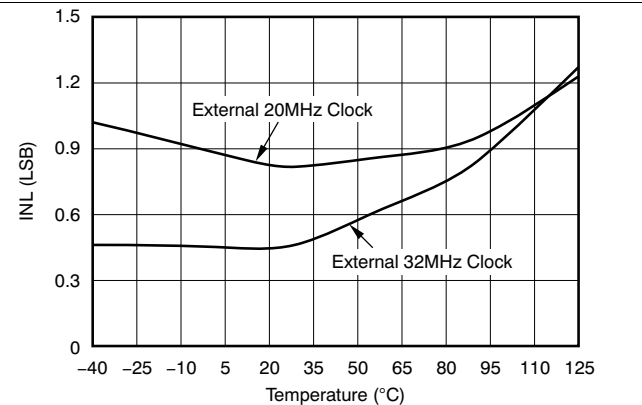


Figure 5. Maximum Integral Nonlinearity vs Temperature

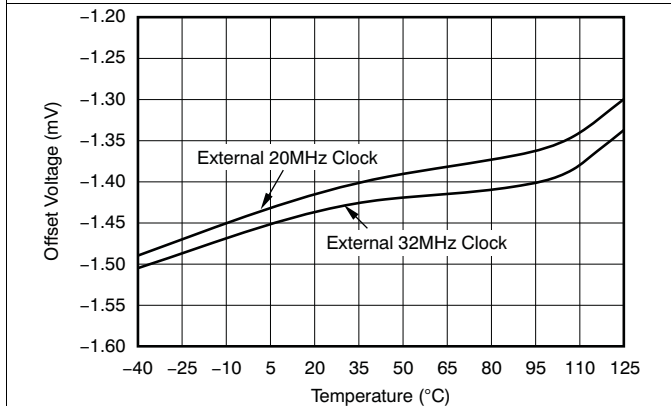


Figure 6. Offset vs Temperature

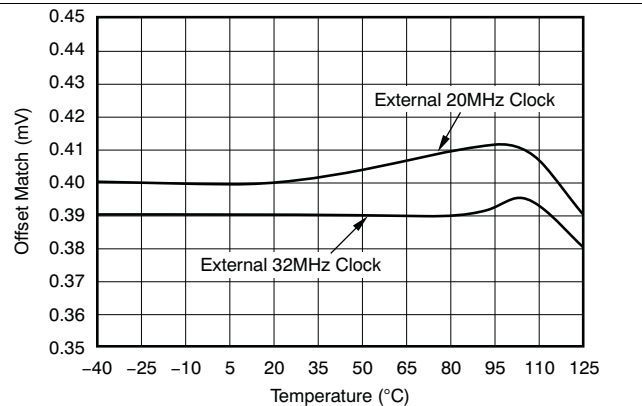


Figure 7. Offset Match vs Temperature

Typical Characteristics (continued)

$AV_{DD} = 5\text{ V}$, $BV_{DD} = 3\text{ V}$, $CH_{x+} = 0.5\text{ V}$ to 4.5 V , $CH_{x-} = 2.5\text{ V}$, $REFIN = \text{external}$, $CLKSEL = 0$, and 16-bit sinc³ filter, with $OSR = 256$ (unless otherwise noted)

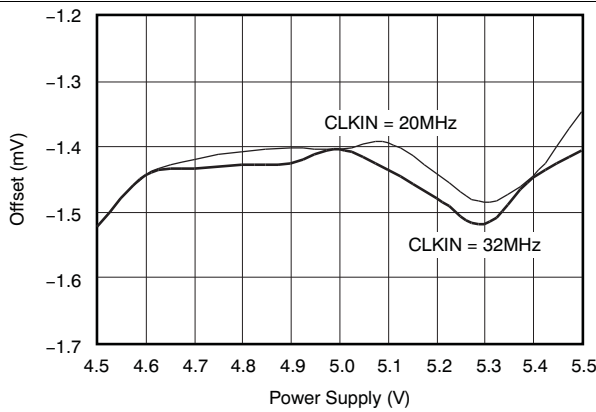


Figure 8. Offset vs Power Supply

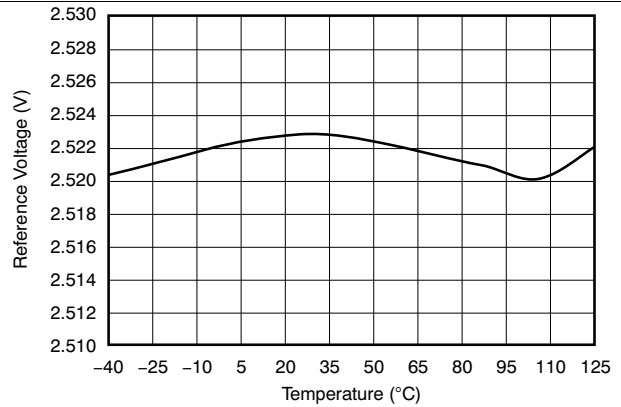


Figure 9. Internal Reference vs Temperature

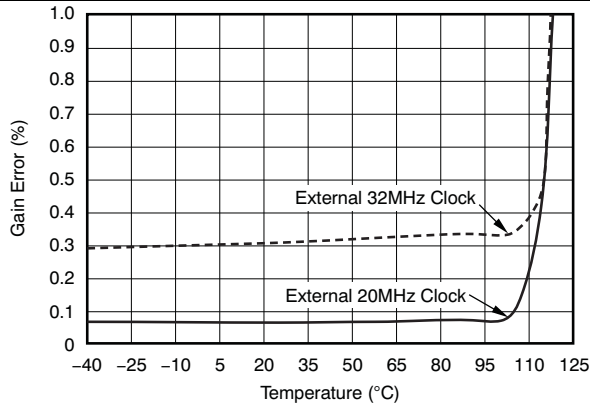


Figure 10. Gain Error vs Temperature

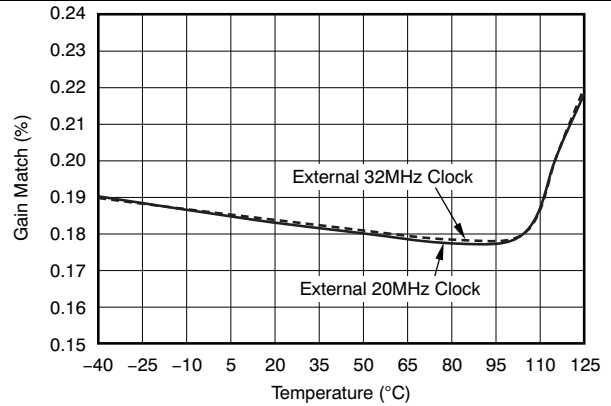


Figure 11. Gain Match vs Temperature

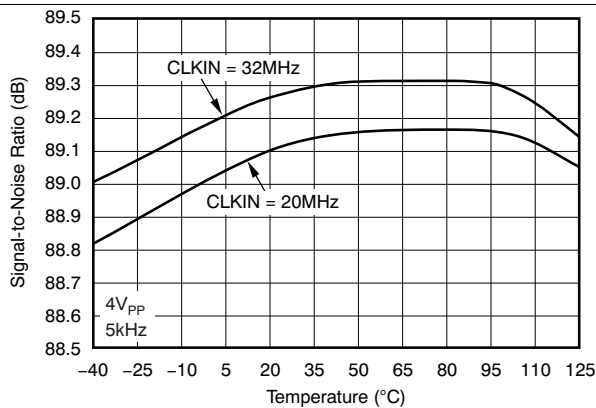


Figure 12. SNR vs Temperature

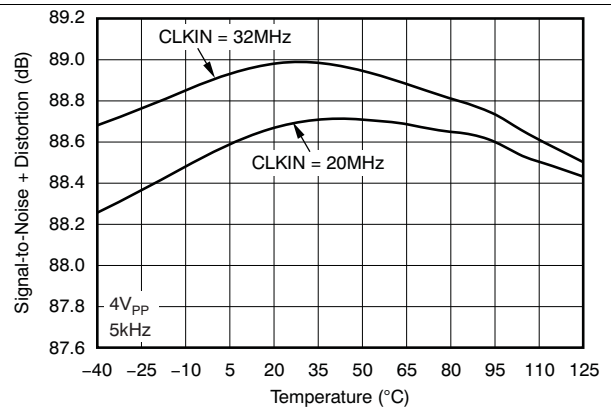


Figure 13. SINAD vs Temperature

Typical Characteristics (continued)

$AV_{DD} = 5\text{ V}$, $BV_{DD} = 3\text{ V}$, $CH_{x+} = 0.5\text{ V}$ to 4.5 V , $CH_{x-} = 2.5\text{ V}$, $REFIN = \text{external}$, $CLKSEL = 0$, and 16-bit sinc³ filter, with $OSR = 256$ (unless otherwise noted)

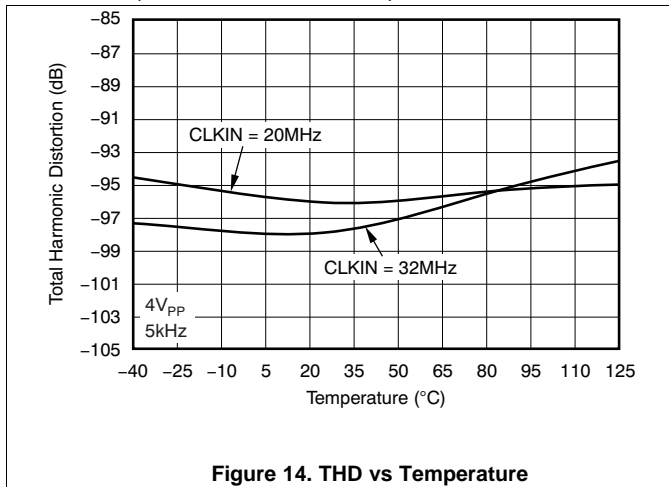


Figure 14. THD vs Temperature

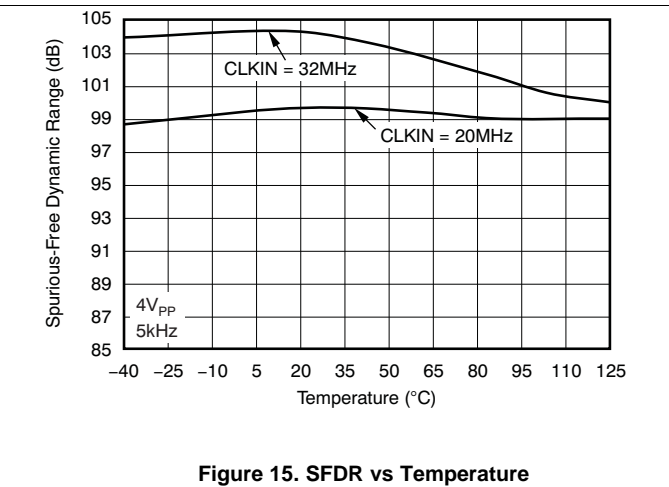


Figure 15. SFDR vs Temperature

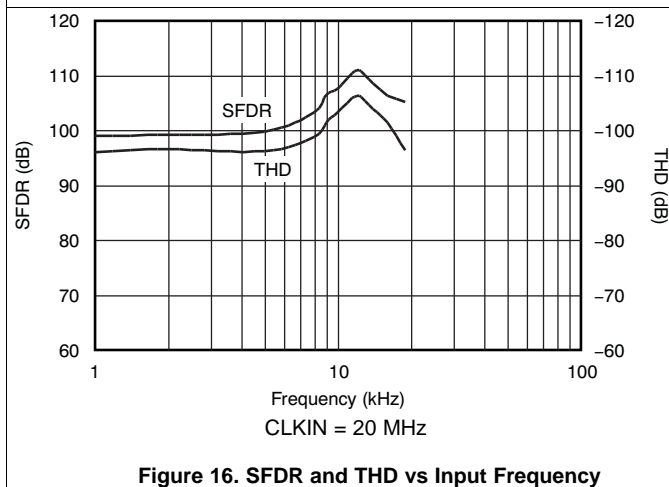


Figure 16. SFDR and THD vs Input Frequency

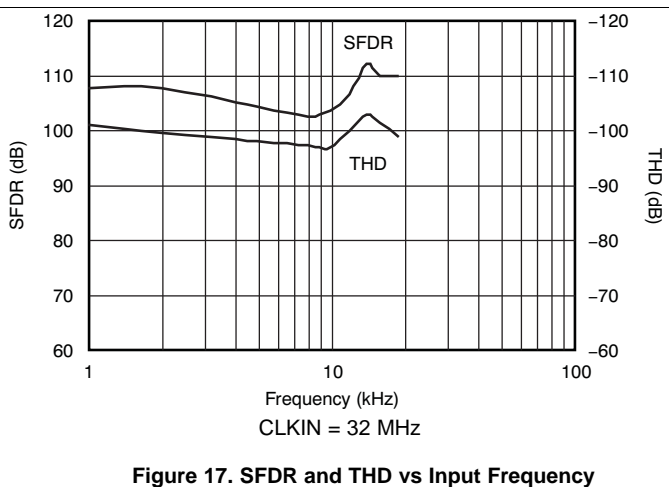


Figure 17. SFDR and THD vs Input Frequency

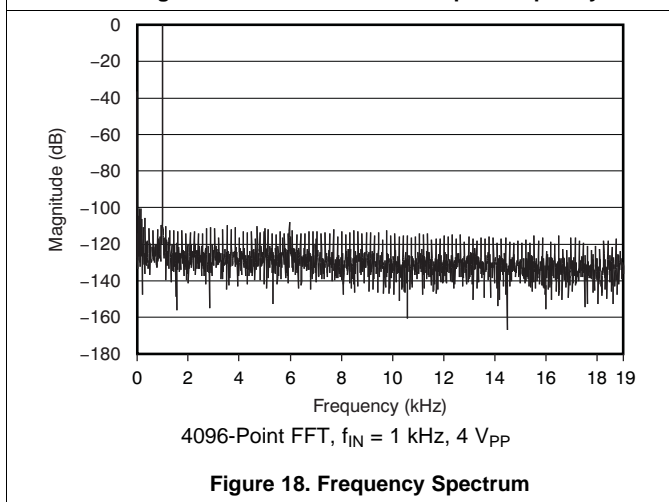


Figure 18. Frequency Spectrum

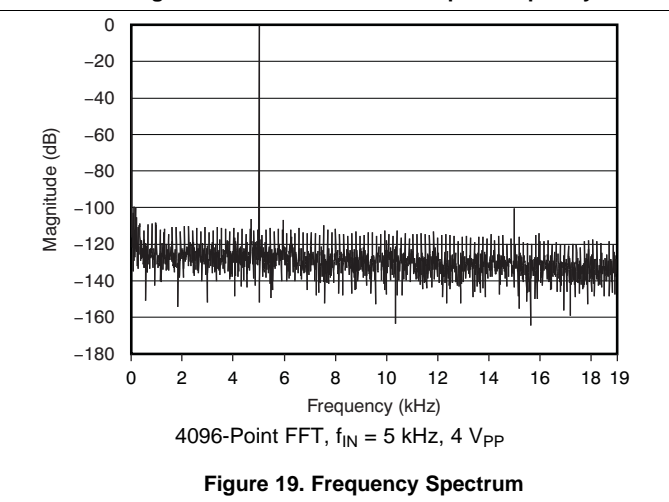
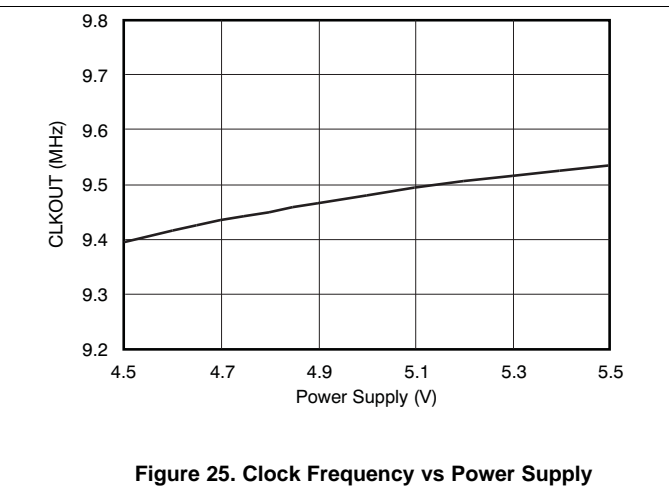
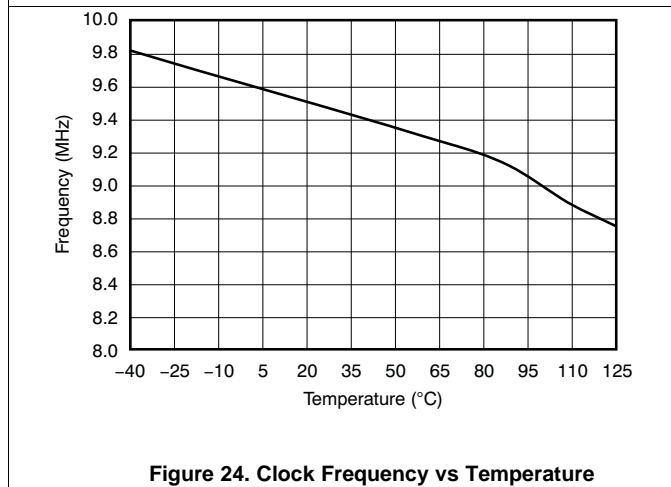
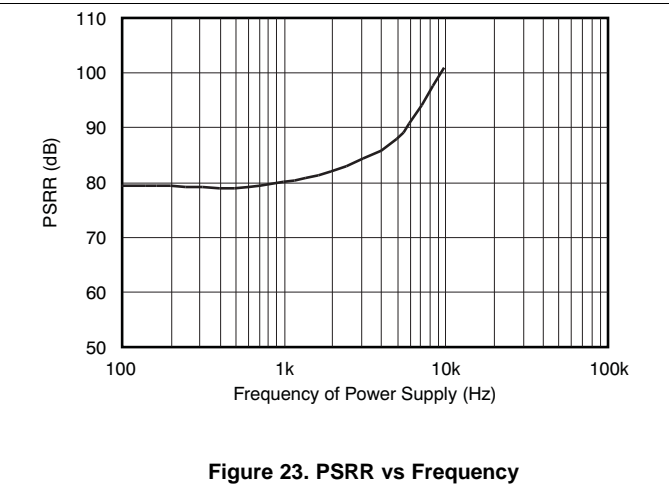
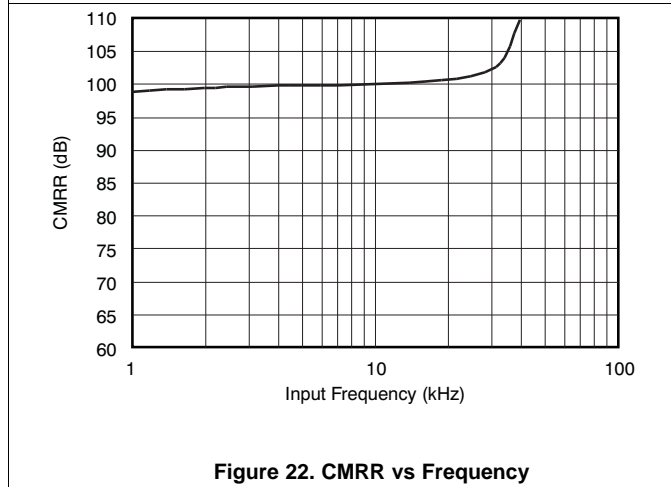
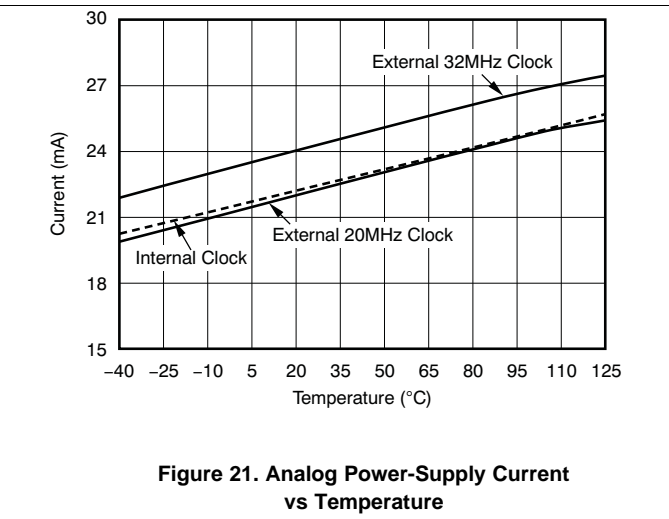
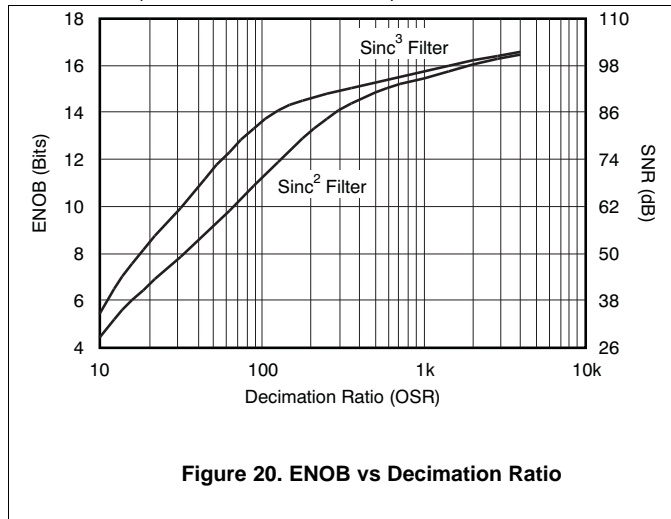


Figure 19. Frequency Spectrum

Typical Characteristics (continued)

$AV_{DD} = 5\text{ V}$, $BV_{DD} = 3\text{ V}$, $CH_{x+} = 0.5\text{ V to }4.5\text{ V}$, $CH_{x-} = 2.5\text{ V}$, $REFIN = \text{external}$, $CLKSEL = 0$, and 16-bit sinc³ filter, with $OSR = 256$ (unless otherwise noted)



7 Detailed Description

7.1 Overview

The ADS1204 is a four-channel, second-order, CMOS device with four delta-sigma ($\Delta\Sigma$) modulators, designed for medium- to high-resolution A/D signal conversions from dc to 39 kHz (filter response -3 dB) if an oversampling ratio (OSR) of 64 is chosen. The output of the converter (OUTX) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the $\Delta\Sigma$ modulator. The filter serves two functions. First, it filters out high-frequency noise. Second, the filter converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

An application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) could be used to implement the digital filter. Figure 26 and Figure 27 illustrate typical application circuits with the ADS1204 connected to an FPGA.

The overall performance (that is, speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 100 dB with an OSR equal to 256.

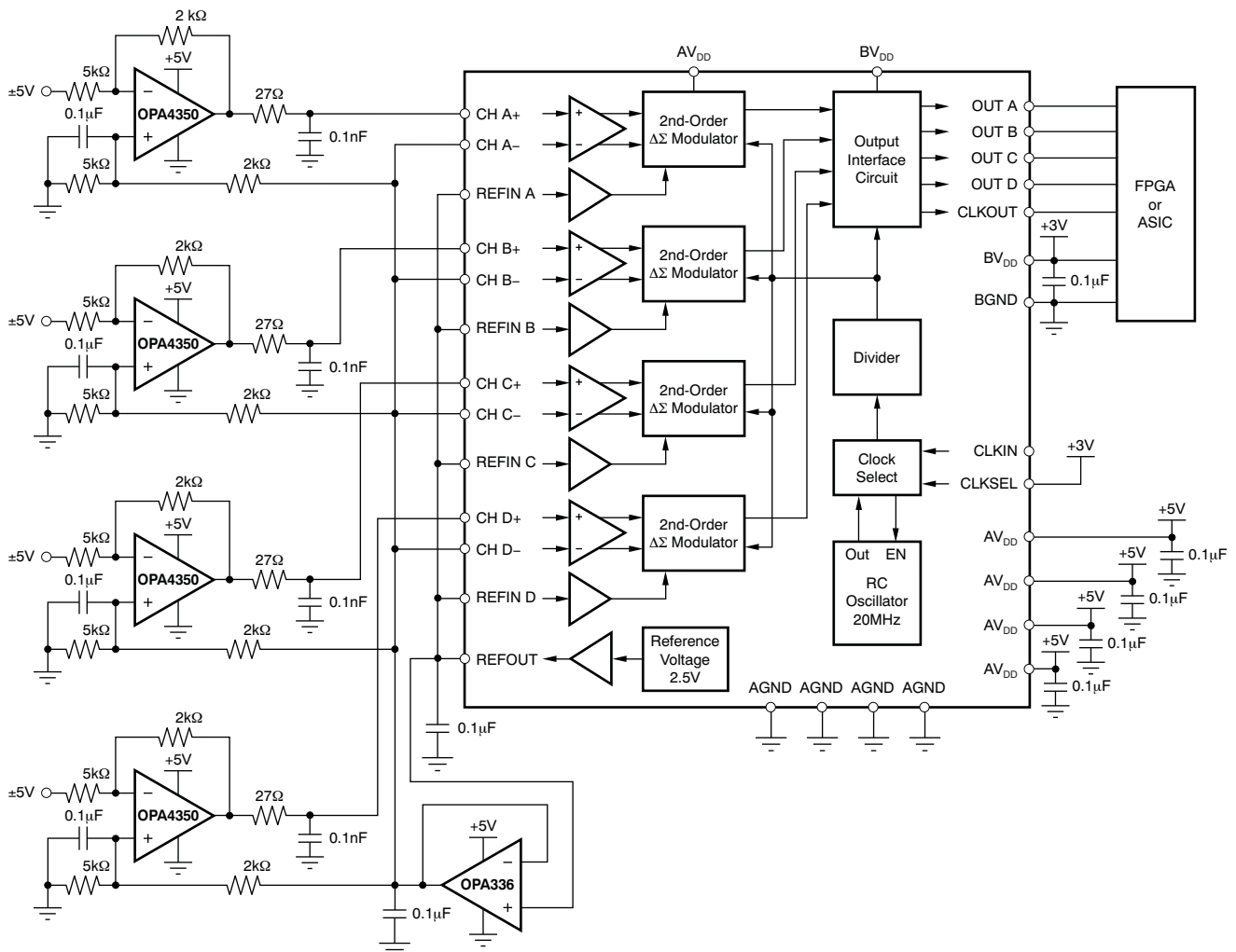


Figure 26. Single-Ended Connection Diagram for the ADS1204 $\Delta\Sigma$ Modulator

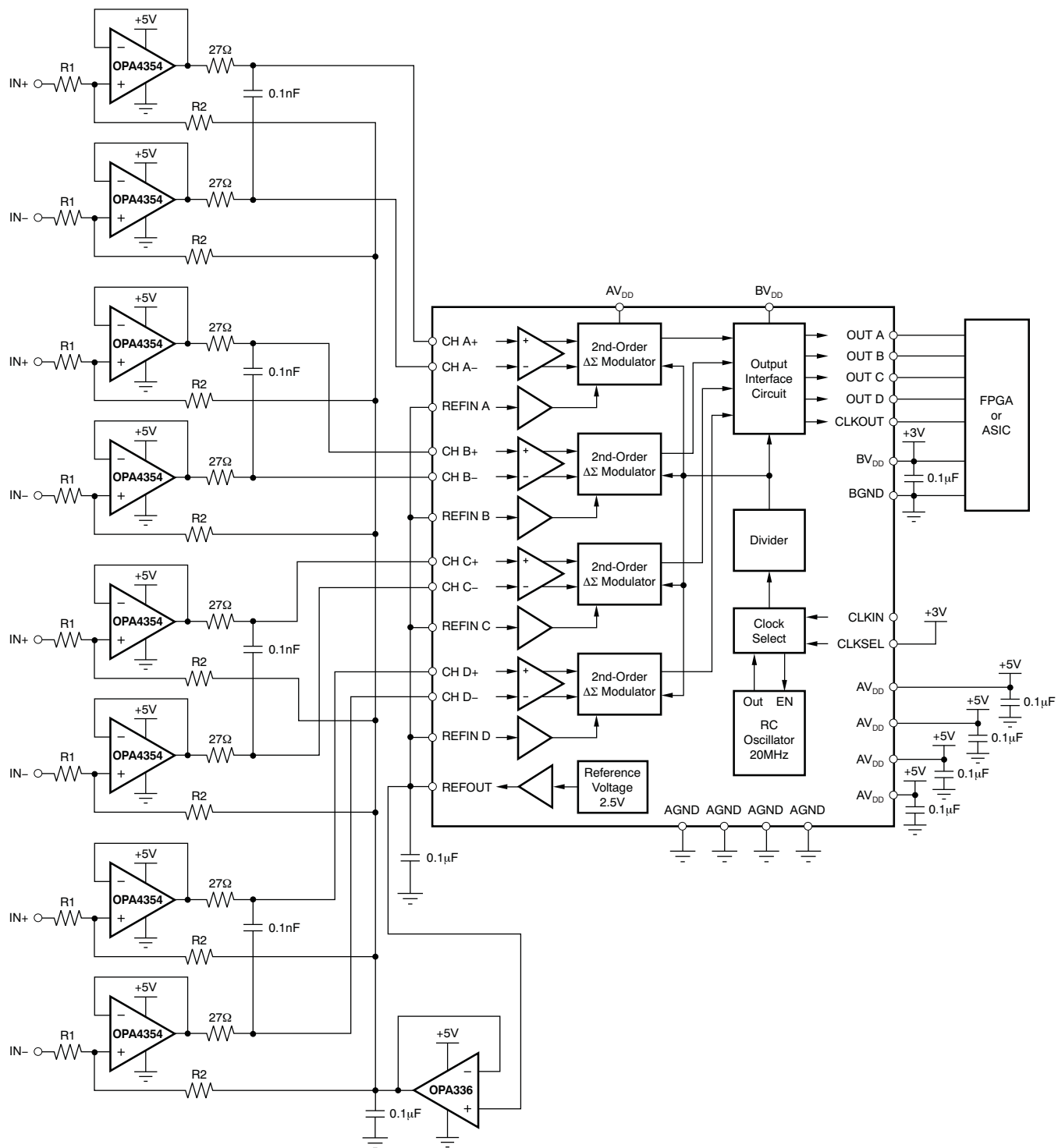
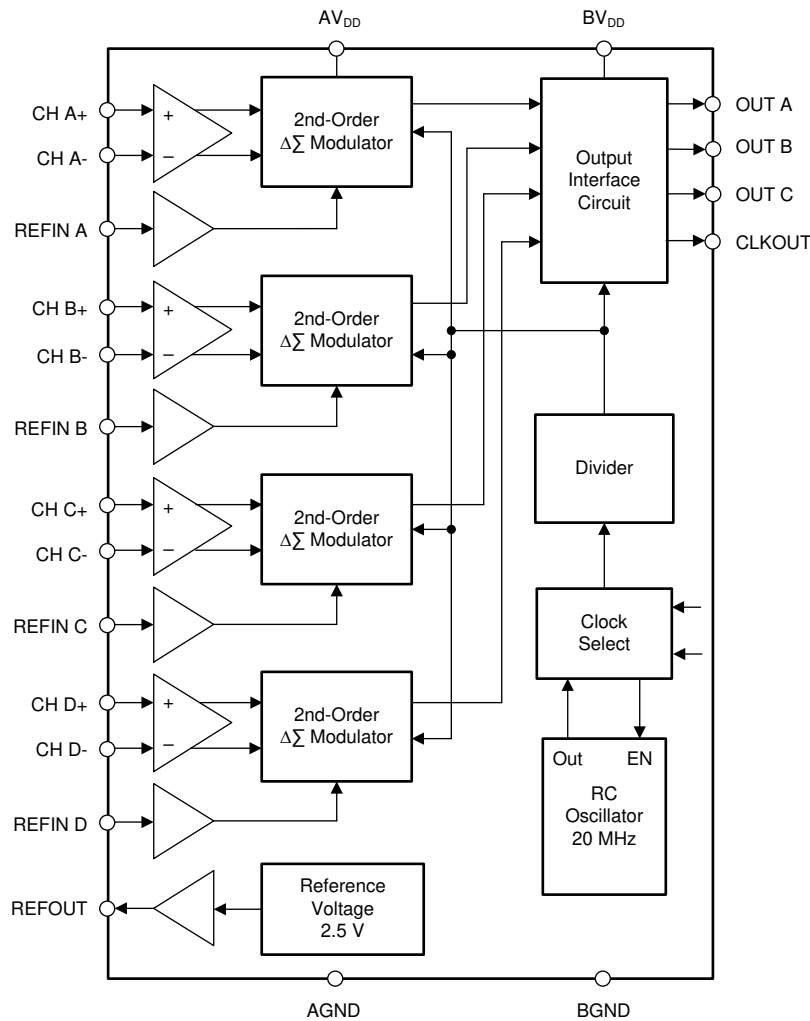


Figure 27. Differential Connection Diagram for the ADS1204 $\Delta\Sigma$ Modulator

7.2 Functional Block Diagram



7.3 Feature Description

The differential analog input of the ADS1204 is implemented with a switched-capacitor circuit. This circuit implements a second-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths. Every analog input signal is continuously sampled by the modulator and compared to a reference voltage that is applied to the REFINx pin. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the corresponding converter.

Feature Description (continued)

7.3.1 Analog Input Stage

7.3.1.1 Analog Input

The topology of the analog inputs of ADS1204 is based on fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (100 dB), and excellent power-supply rejection.

The input impedance of the analog input is dependent on the modulator clock frequency (f_{CLK}), which is also the sampling frequency of the modulator. Figure 28 shows the basic input structure of one channel of the ADS1204. The relationship between the input impedance of the ADS1204 and the modulator clock frequency is shown in Equation 1:

$$Z_{IN} = \frac{100k\Omega}{f_{MOD}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, CH x+ and CH x-. If the input voltage exceeds the range ($GND - 0.3 V$) to ($V_{DD} + 0.3 V$), the input current must be limited to 10 mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog voltage resides within $\pm 2 V$ (with V_{REF} as a midpoint); however, the FSR input voltage is $\pm 2.5 V$.

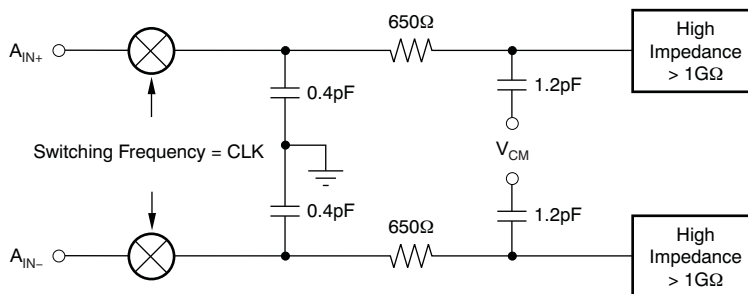


Figure 28. Input Impedance of the ADS1204

7.3.1.2 Modulator

The ADS1204 can be operated in two modes. When $CKLSEL = 1$, the four modulators operate using the internal clock, which is fixed at 20 MHz. When $CKLSEL = 0$, the modulators operate using an external clock. In both modes, the clock is divided by two internally and functions as the modulator clock. The frequency of the external clock can vary from 1 MHz to 32 MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a second-order, switched-capacitor, $\Delta\Sigma$ modulator, such as the one conceptualized in Figure 29. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X2 and X3. The voltages at X2 and X3 are presented to their individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

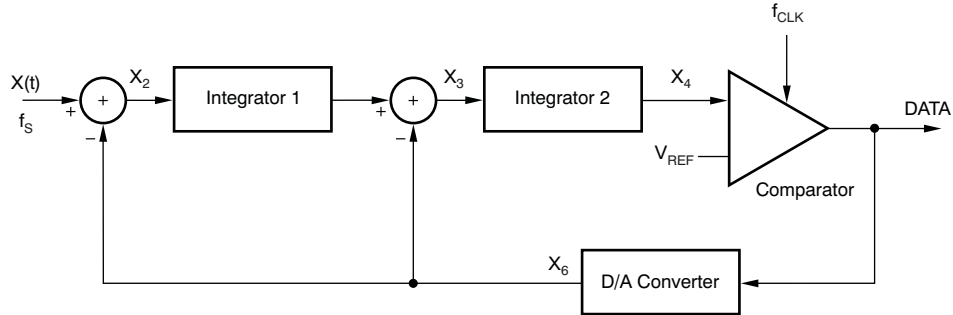


Figure 29. Block Diagram of the Second-Order Modulator

7.3.2 Digital Output

A differential input signal of 0 V will ideally produce a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 2 V produces a stream of ones and zeros that are high 80% of the time. A differential input of -2 V produces a stream of ones and zeros that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 30.

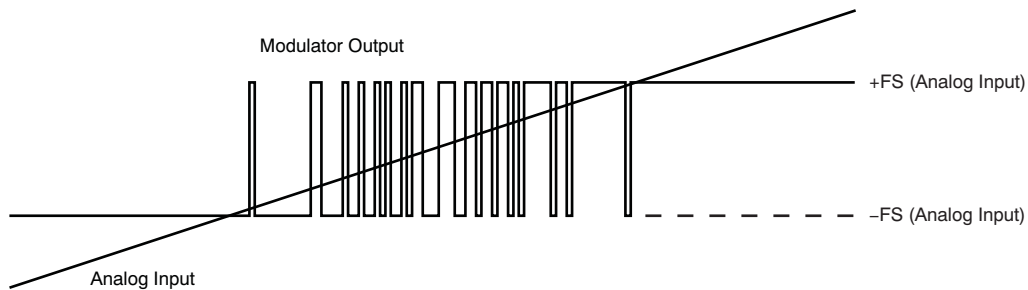
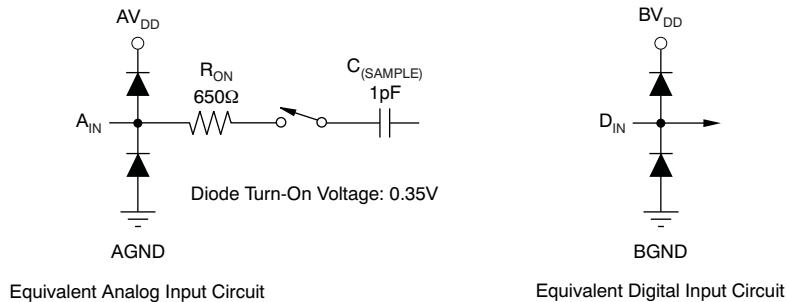


Figure 30. Analog Input versus Modulator Output of the ADS1204

7.3.3 Equivalent Input Circuits

Figure 31 shows equivalent circuits for the analog input and digital outputs.



NOTE: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

Figure 31. Equivalent Input Circuits

7.4 Device Functional Modes

The system clock of the ADS1204 is 20 MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the CLKIN pin is provided; it is controlled by the mode setting, CLKSEL.

The system clock is divided by two for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 32MHz, the modulator operates between 500 kHz and 16 MHz.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The analog signal connected to the input of the $\Delta\Sigma$ modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is generated and sent to the OUTx pin from the $\Delta\Sigma$ modulator. In most applications where a direct connection is realized between the $\Delta\Sigma$ modulator and an ASIC or FPGA (each with an implemented filter), the two standard signals per modulator (CLKOUT and OUTx) are provided from the modulator. The output clock signal is equal for all four modulators. If CLKSEL = 1, CLKIN must always be set either high or low.

8.1.1 Filter Usage

The modulator generates only a bitstream, which does not output a digital word like an A/D converter. In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

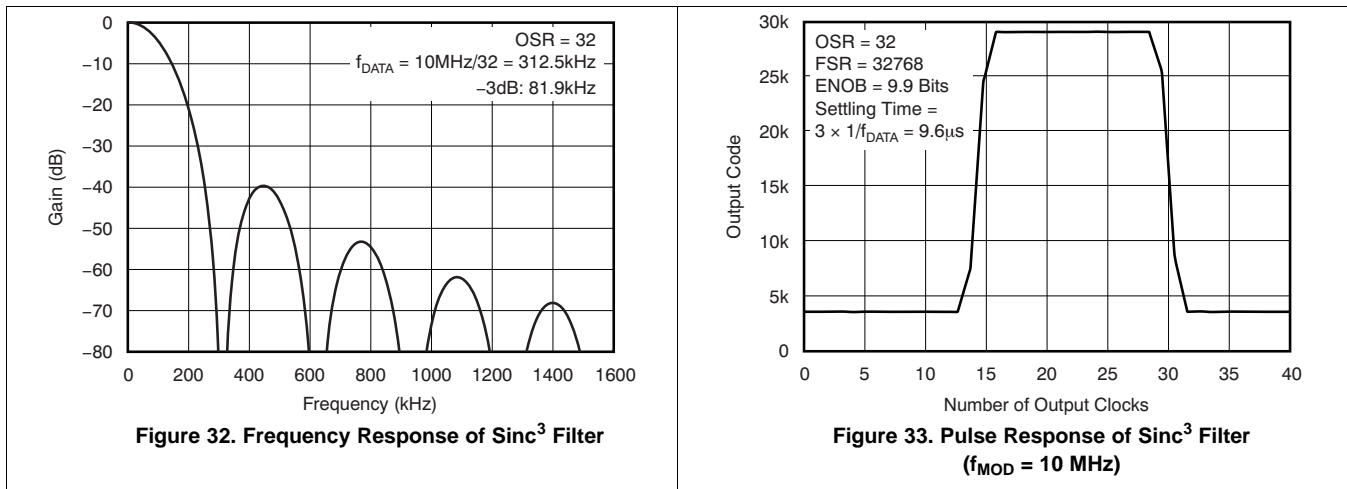
A very simple filter, built with minimal effort and hardware, is the sinc³ filter shown in [Equation 2](#):

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^2 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (for example, a count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a sinc³ filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a sinc³ filter response (see [Figure 32](#) and [Figure 33](#)), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK} / OSR$. The -3-dB point is located at half the Nyquist frequency or $f_{DATA} / 4$. For some applications, it may be necessary to use another filter type for better frequency response.

Application Information (continued)



This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a sinc³ filter with a low OSR and the second stage a high-order filter.

For more information, see the [Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications](#) application note, available for download at [www.ti.com](#).

The effective number of bits (ENOB) can be used to compare the performance of A/D converters and ΔΣ modulators. Figure 34 shows the ENOB of the ADS1204 with different filter types. In this data sheet, the ENOB is calculated from the SNR as shown in Equation 3:

$$SNR = 1.76dB + 6.02dB \times ENOB \tag{3}$$

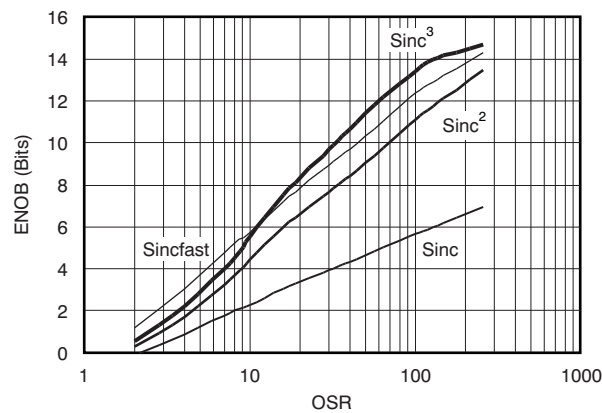


Figure 34. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1 μs and 5 μs with 3 bits to 7 bits resolution. The time for full settling is dependent on the filter order. Therefore, the full settling of the sinc³ filter needs three data clocks and the sinc² filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than sinc³ might be a better choice. A simple example is a sinc² filter. Figure 35 compares the settling time of different filter types. The Sincfast is a modified sinc² filter as Equation 4 shows:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^2 (1 + z^{-2 \times OSR}) \tag{4}$$

Application Information (continued)

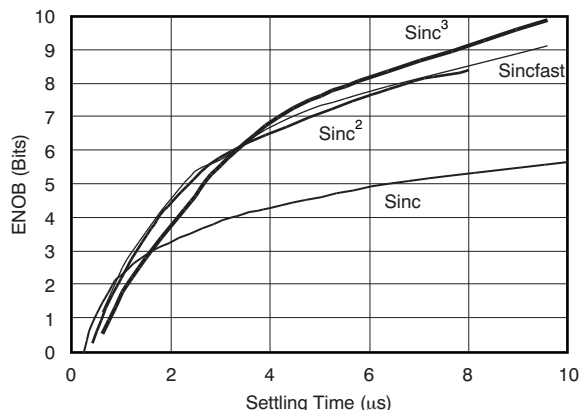


Figure 35. Measured ENOB versus Settling Time

For more information, see the [Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications](#) application note, available for download at www.ti.com.

9 Power Supply Recommendations

The ADS1204 requires two power supplies, AV_{DD} for analog, and BV_{DD} for digital. The analog supply is a fixed voltage of $5\text{ V} \pm 5\%$, whereas the digital supply can be set within a range of 2.7 V to 5.5 V. BV_{DD} determines the I/O voltage for the interface. If AV_{DD} equals BV_{DD} , the two supplies can be tied together.

9.1 Power-Supply Sequencing

The supplies can be sequenced in any order, but in no case must any analog or digital input exceed the respective analog or digital power-supply voltage and current limits. In particular, inputs to the ADS1204, such as CH x+, CH x–, and CLKIN, should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current to a maximum of 10 mA.

Wait approximately 600 μs after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

9.2 Power-Supply Decoupling

Good decoupling practices must be used for the ADS1204 and for all components in the design. All decoupling capacitors, specifically the 0.1- μF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1- μF and 10- μF capacitor, in parallel with the 0.1- μF ceramic capacitor, can be used to decouple AV_{DD} to AGND as well as BV_{DD} to BGND. At least one 0.1- μF ceramic capacitor must be used to decouple every AV_{DD} to AGND and BV_{DD} to BGND, as well as for the digital supply on each digital component.

In cases where both the analog and digital I/O supplies share the same supply source, an RC filter of 10 Ω and 0.1 μF can be used to help reduce the noise in the analog supply.

10 Layout

10.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. Figure 36 shows an example of good component placement. Although Figure 36 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

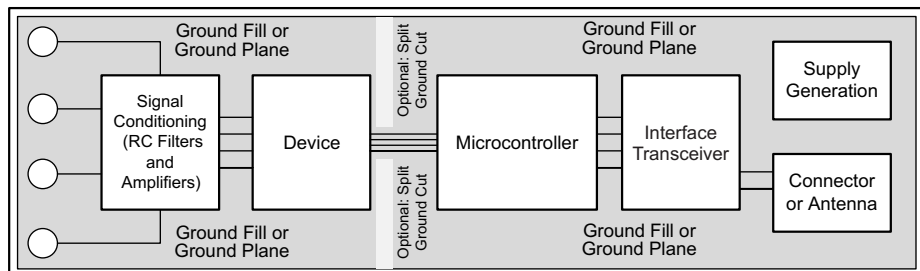


Figure 36. System Component Placement

The following basic recommendations for layout of the ADS1204 help achieve the best possible performance of the ADC.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Routing digital lines away from analog lines prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as CH A+, CH A– through CH D+ and CH D–). The differential capacitors must be of high quality. The best ceramic chip capacitors are COG (NPO) that have stable properties and low noise characteristics.

10.2 Layout Example

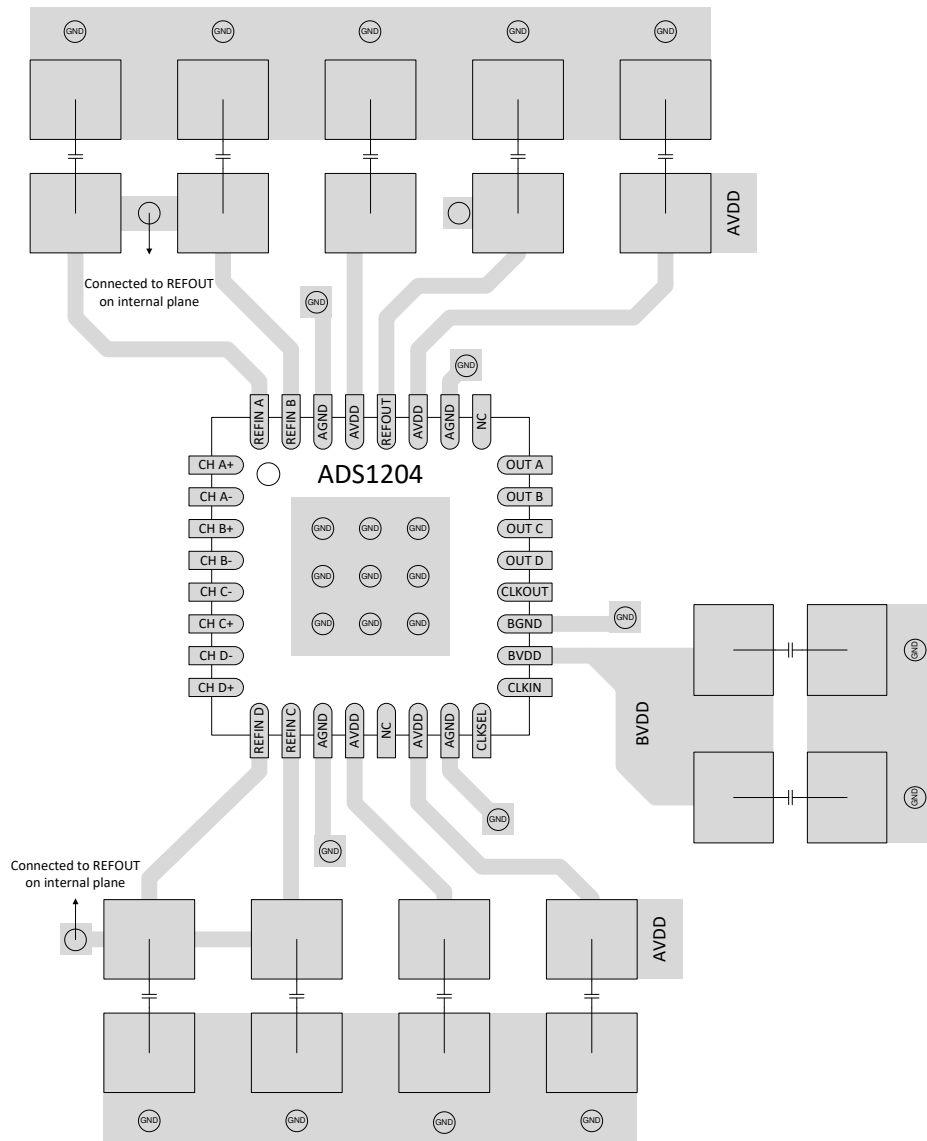


Figure 37. ADS1204 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary



[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1204IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I	
ADS1204IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1204I	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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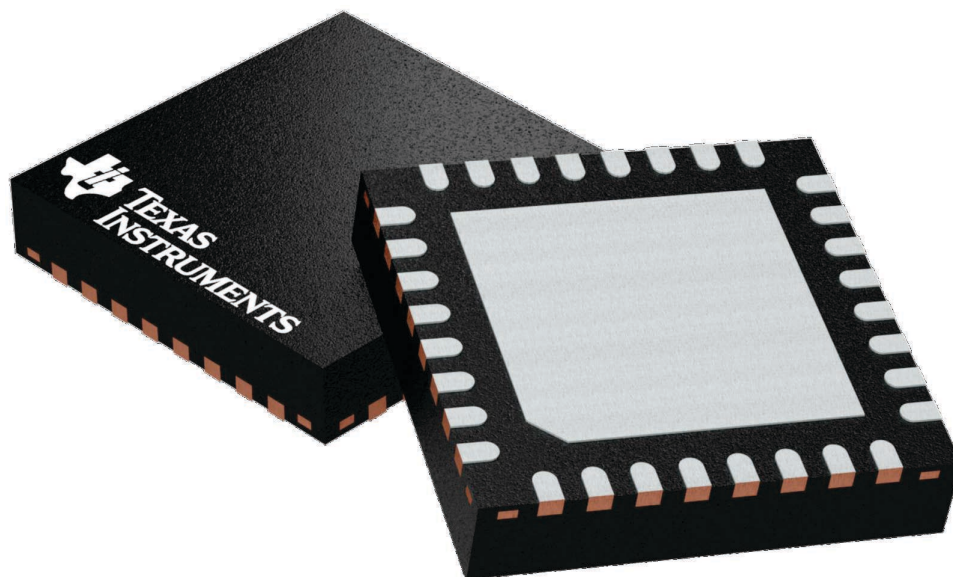
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



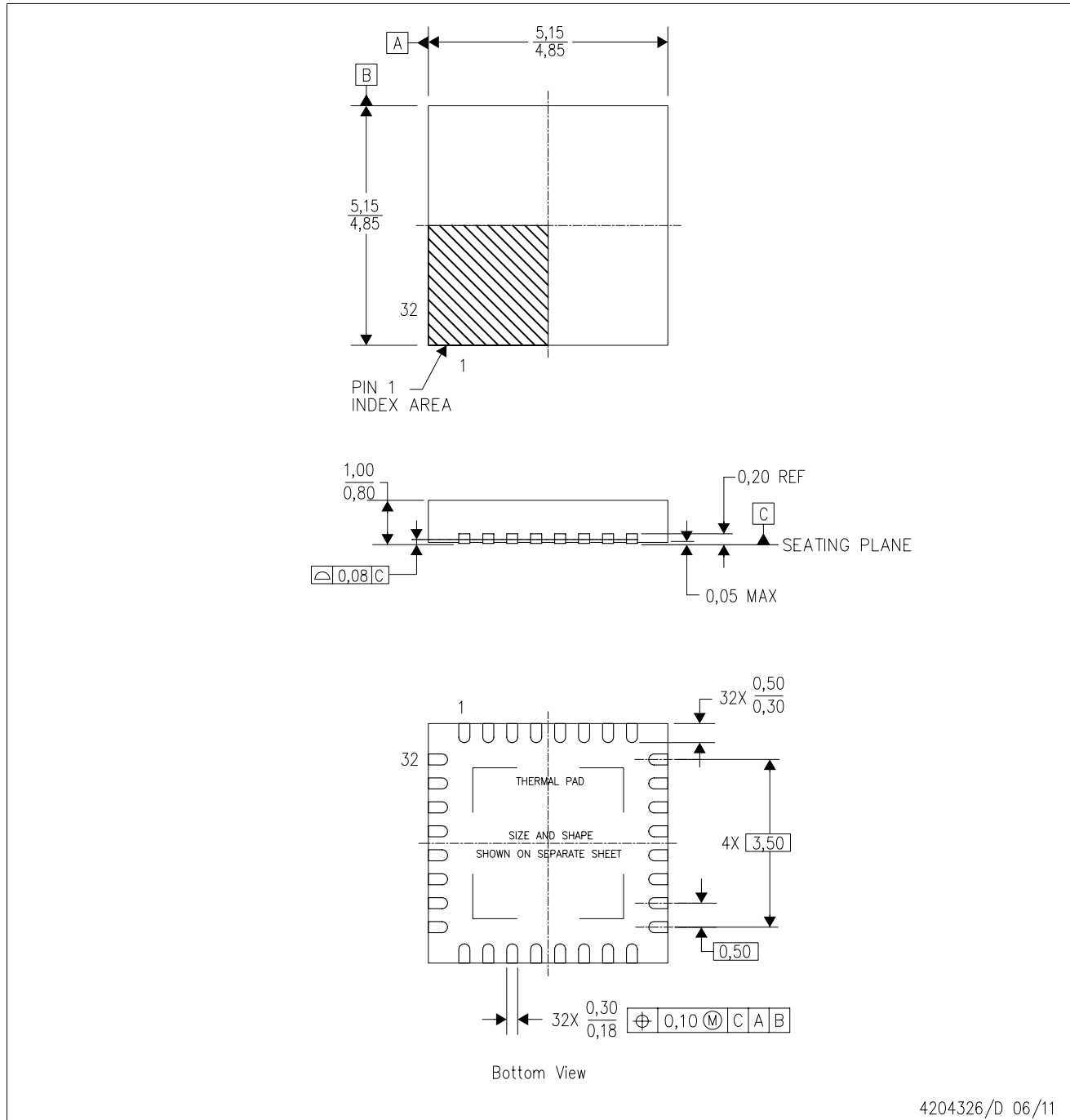
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

MECHANICAL DATA

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

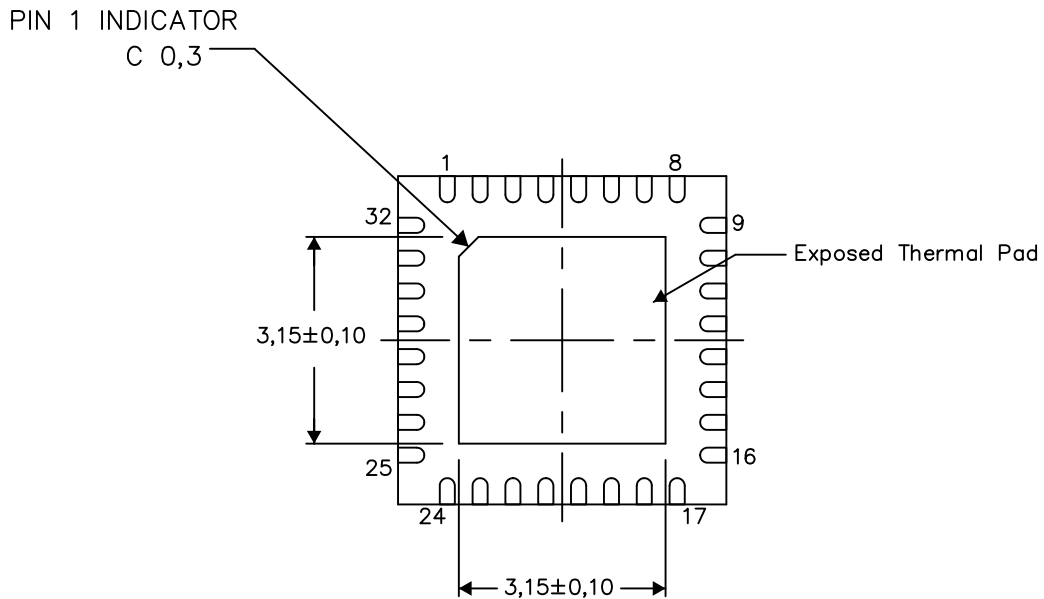
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

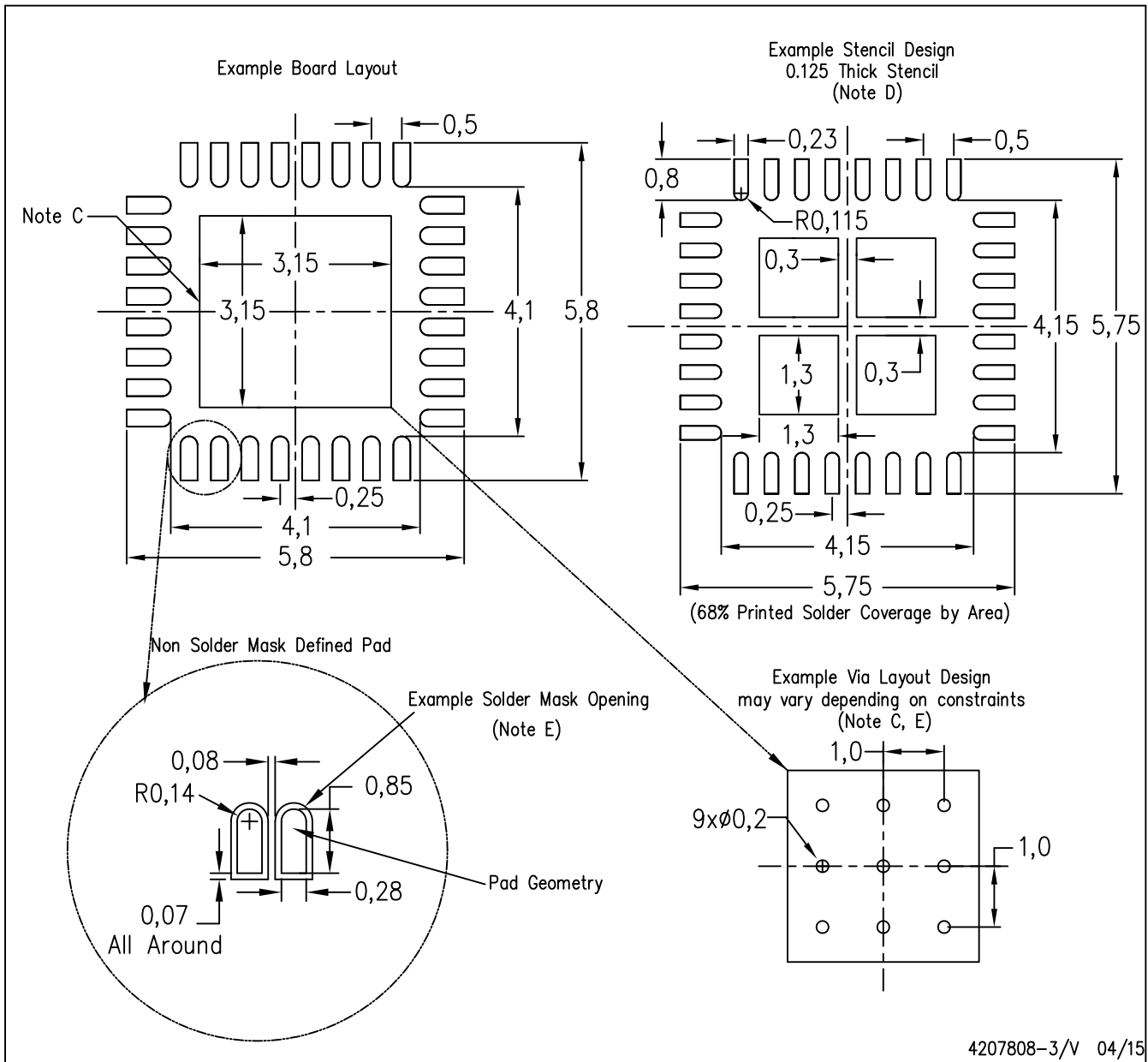
Exposed Thermal Pad Dimensions

4206356-3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

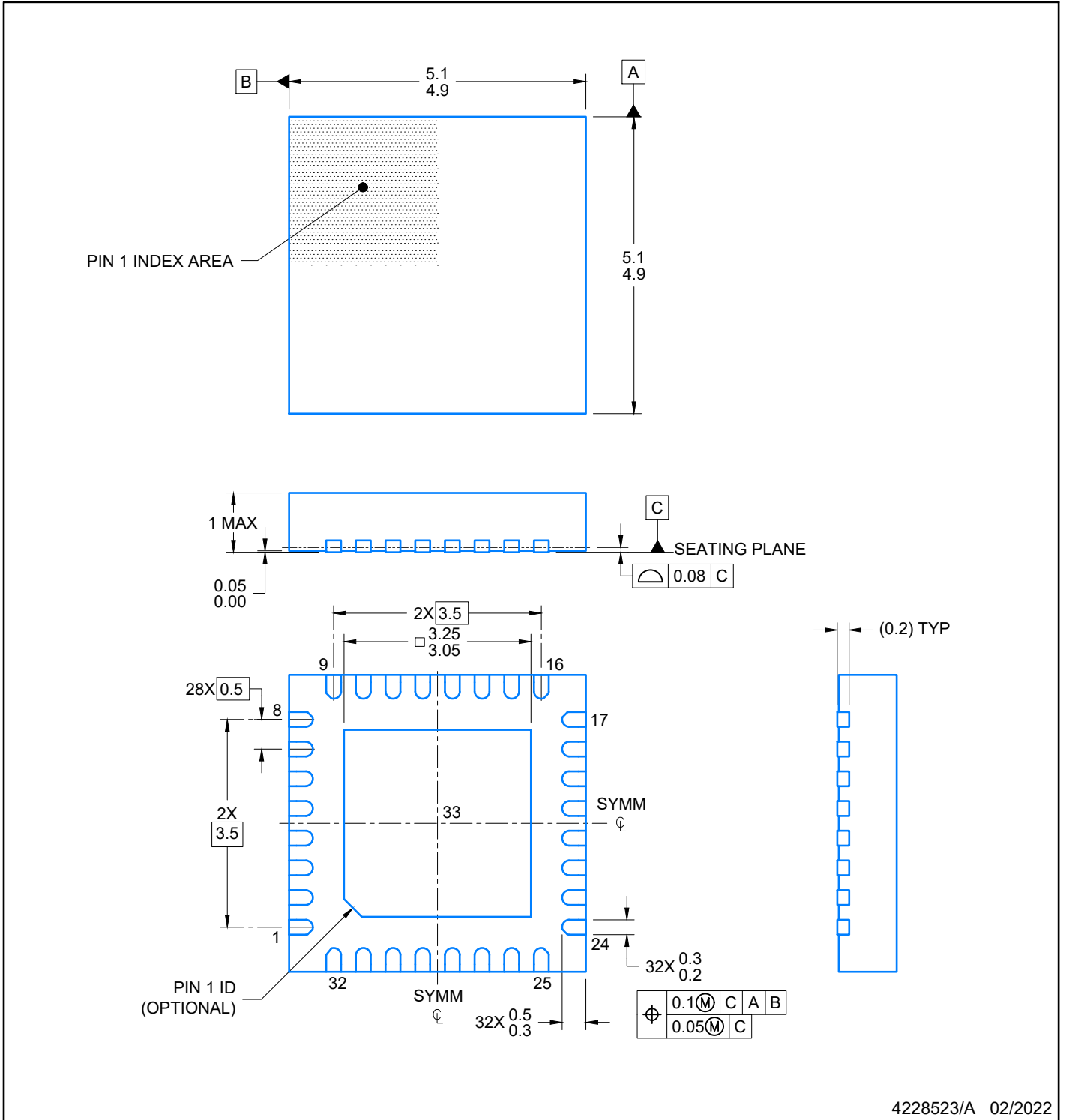
RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



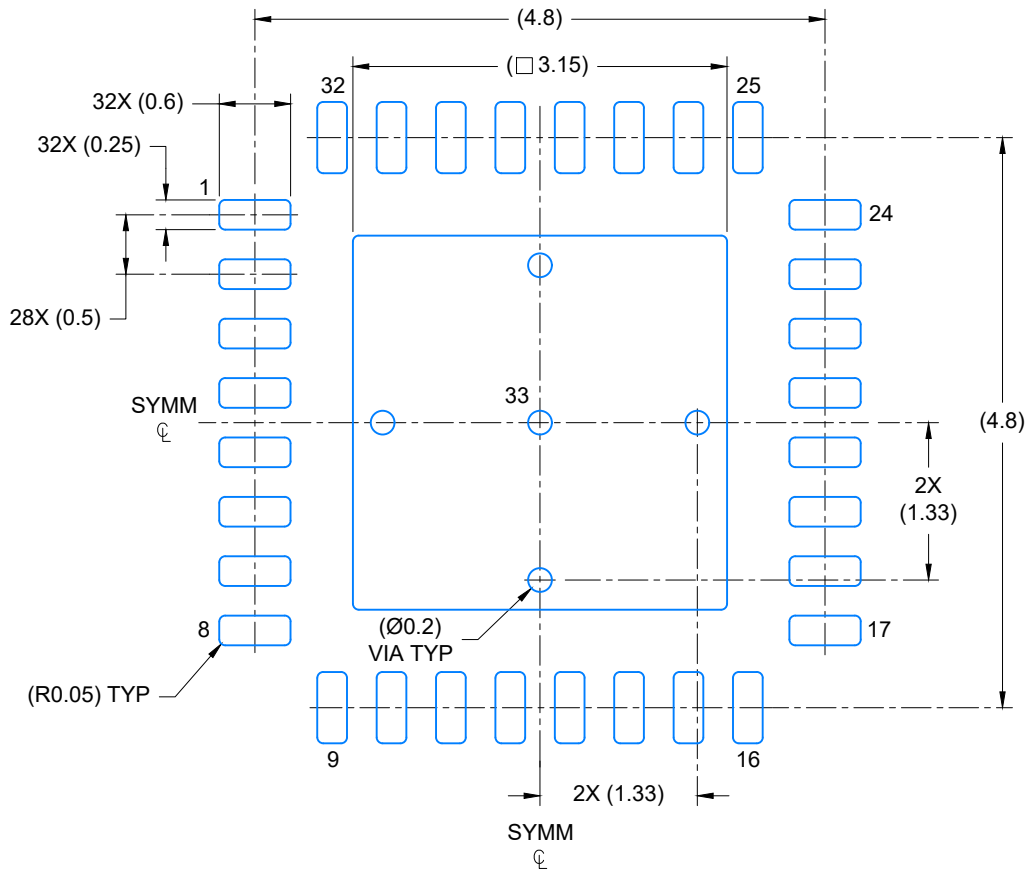
4207808-3/V 04/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

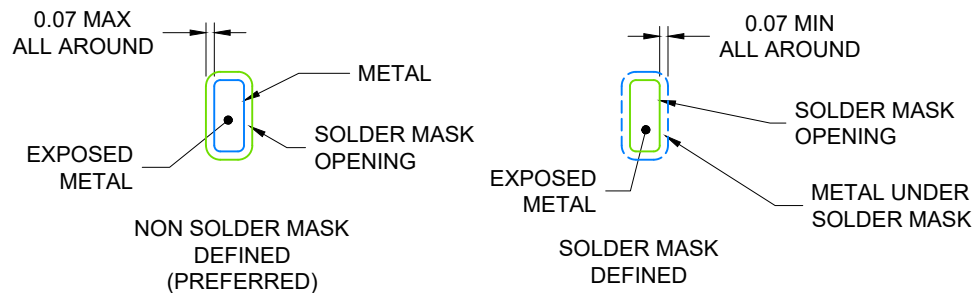


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4228523/A 02/2022

NOTES: (continued)

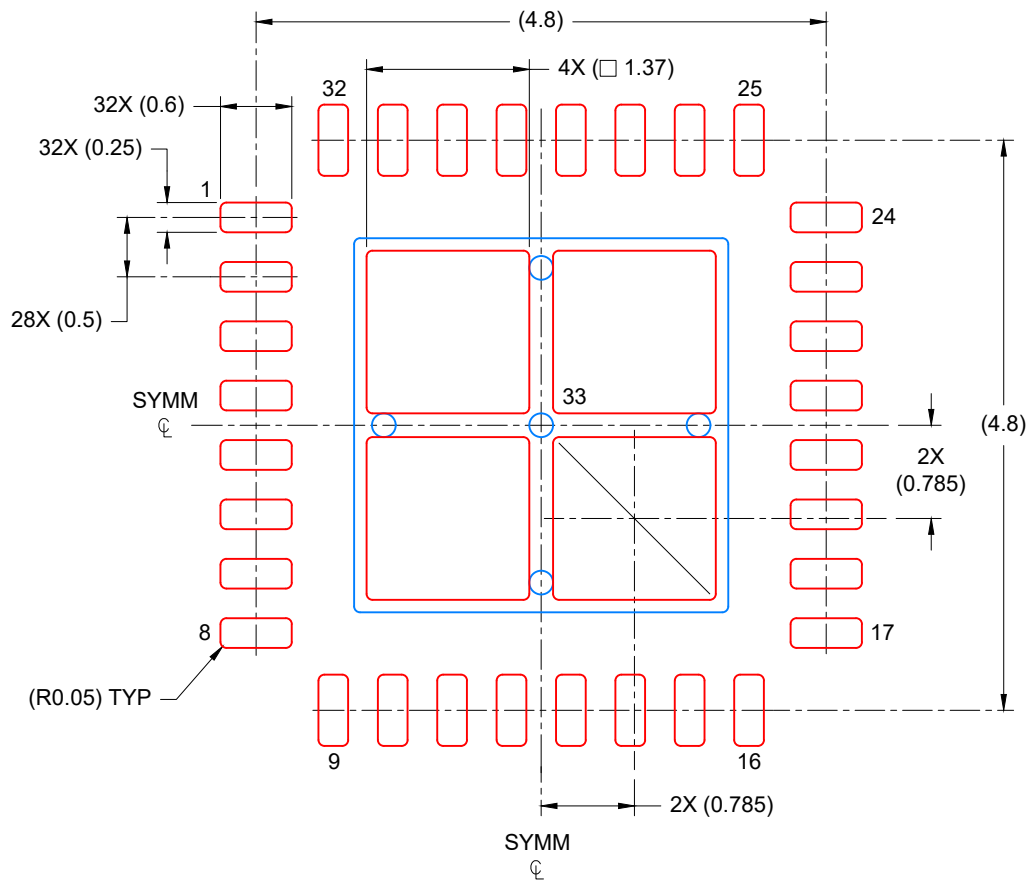
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RHB0032D

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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