

# ADS131B23-Q1 電圧、電流、温度センシング向け、 SPI と 3 チャンネルの ADC を搭載した車載用高電圧バッテリー・パック・モニタ

## 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$
- 機能安全準拠
  - 機能安全アプリケーション向けに開発
  - ASIL D までの ISO 26262 機能安全システム設計に役立つ資料を入手可能
  - ASIL D までの決定論的対応能力
  - ASIL D までのハードウェア機能
- 電流シャント測定用の 2 つの同時サンプリング 24 ビット ADC (ADC1A、ADC1B):
  - フルスケール・レンジをプログラム可能:
    - $\pm 39\text{mV} \sim \pm 312.5\text{mV}$
    - 幅広いシャント抵抗値と電流測定範囲をサポート
  - 以下を使用して、高精度の電流シャント測定を実現:
    - オフセット誤差:  $\pm 1.5\mu\text{V}$  (最大値)
    - ゲインのドリフト:  $20\text{ppm}/^{\circ}\text{C}$  (最大値)
  - データ・レートをプログラム可能:  $500\text{SPS} \sim 64\text{kSPS}$
  - 高速過電流検出用のプログラム可能なスレッシュホルドを備えた ADC ごとのデジタル過電流コンパレータ
- 電圧および温度測定用の 1 つの多重化 16 ビット ADC (ADC2A):
  - 8 つのアナログ入力
  - フルスケール・レンジをプログラム可能:  $\pm 312.5\text{mV} \sim \pm 1.25\text{V}$
  - チャンネル・シーケンサ

- ランダムなハードウェア障害を軽減および検出するための監視および診断機能
- 電源電圧範囲:  $2.9\text{V} \sim 16\text{V}$
- SPI 互換のインターフェイス
- PWM 機能を備えた 9 個の GPIO

## 2 アプリケーション

- 車載用バッテリー管理システム (BMS):
  - 電流シャント測定
  - 外付けの分圧抵抗を使用した電圧測定
  - サーミスタまたはアナログ出力温度センサを使用した温度測定

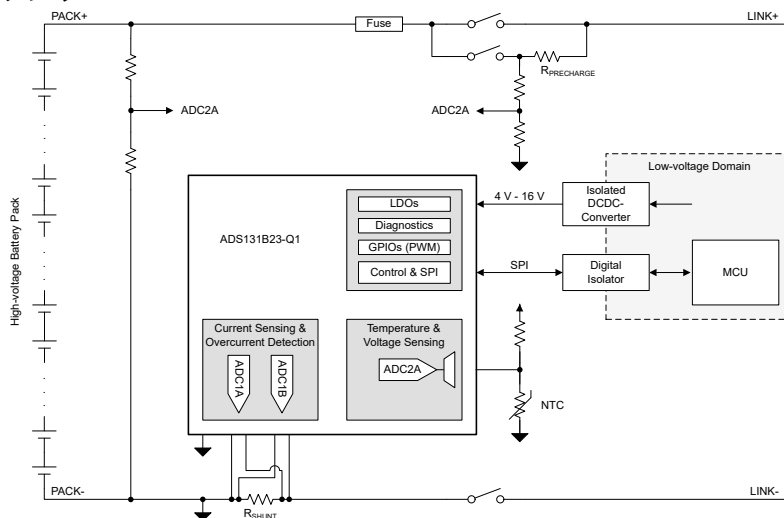
## 3 概要

ADS131B23-Q1 は、車載用電気自動車 (EV) バッテリー管理システム (BMS) 向けの完全統合型高電圧バッテリー・パック・モニタです。

### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージ・サイズ <sup>(2)</sup>
ADS131B23-Q1	PHP (HTQFP, 48)	9mm × 9mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



EV BMS 電流センス・モジュール (CSM) のシステム・ブロック図



## Table of Contents

<b>1 特長</b> .....	1	9.1 Overview.....	24
<b>2 アプリケーション</b> .....	1	9.2 Functional Block Diagram.....	25
<b>3 概要</b> .....	1	9.3 Feature Description.....	26
<b>4 Revision History</b> .....	2	9.4 Device Functional Modes.....	53
<b>5 概要 (続き)</b> .....	3	9.5 Programming.....	61
<b>6 Pin Configuration and Functions</b> .....	4	9.6 Register Map.....	74
<b>7 Specifications</b> .....	6	<b>10 Application and Implementation</b> .....	214
7.1 Absolute Maximum Ratings.....	6	10.1 Application Information.....	214
7.2 ESD Ratings.....	6	10.2 Typical Application.....	214
7.3 Recommended Operating Conditions.....	7	10.3 Power Supply Recommendations.....	217
7.4 Thermal Information.....	8	10.4 Layout.....	221
7.5 Electrical Characteristics.....	8	<b>11 Device and Documentation Support</b> .....	222
7.6 Timing Requirements.....	14	11.1 Documentation Support.....	222
7.7 Switching Characteristics.....	15	11.2 ドキュメントの更新通知を受け取る方法.....	222
7.8 Timing Diagram.....	15	11.3 サポート・リソース.....	222
7.9 Typical Characteristics.....	16	11.4 Trademarks.....	222
<b>8 Parameter Measurement Information</b> .....	22	11.5 静電気放電に関する注意事項.....	222
8.1 Offset Drift Measurement.....	22	11.6 用語集.....	222
8.2 Gain Drift Measurement.....	22	<b>12 Mechanical, Packaging, and Orderable              Information</b> .....	222
8.3 Noise Performance.....	23		
<b>9 Detailed Description</b> .....	24		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2023	*	Initial Release

## 5 概要 (続き)

ADS131B23-Q1 には 2 つの同時サンプリング、高精度、24 ビット ADC チャンネル (ADC1A、ADC1B) が内蔵されており、外付けのシャント抵抗を使用して高分解能かつ高精度でバッテリー電流を冗長測定できます。2 つの独立したデジタル・コンパレータにより、2 つの ADC と並列で高速な過電流検出が可能です。

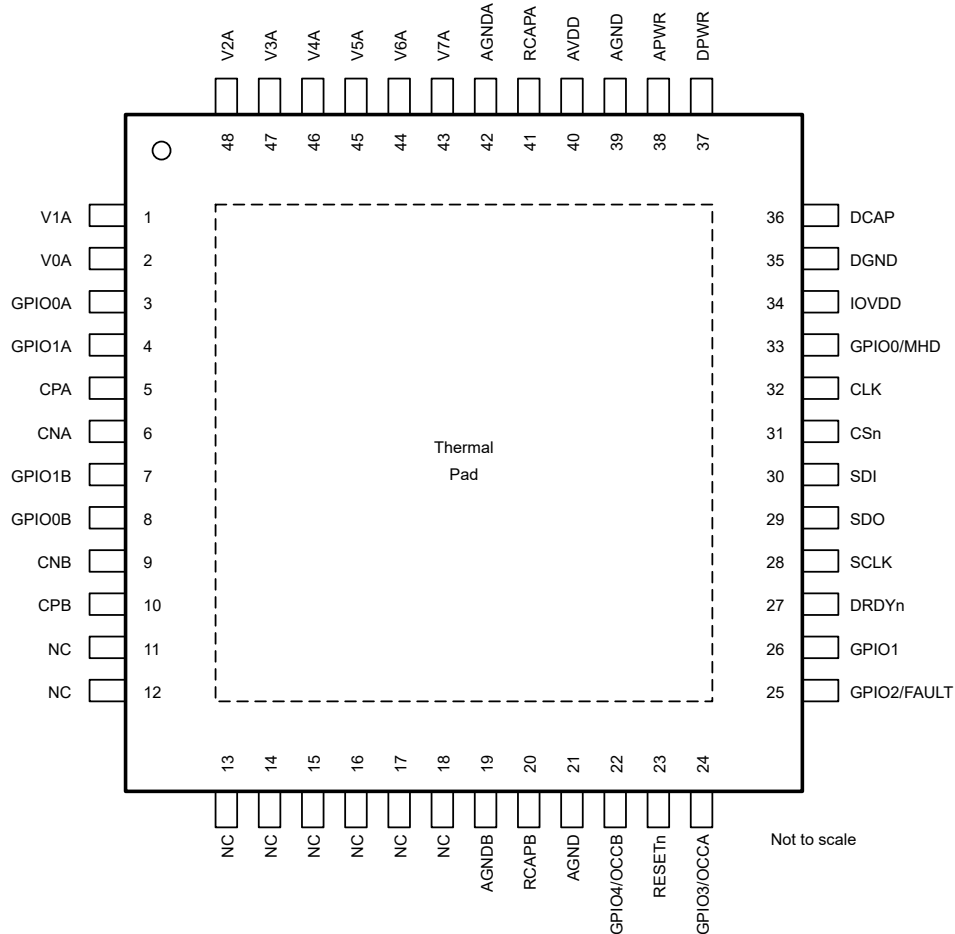
追加の多重化 16 ビット ADC (ADC2A) を利用すれば、外付けの高電圧抵抗分圧器を使用した、シャント温度やシステム内のその他の電圧の測定 (バッテリー・パック電圧など) が可能です。シャント温度は、サーミスタやアナログ出力温度センサなどの外付け温度センサを使用して測定します。ADC2A には、構成済みのマルチプレクサ入力を自動的に流して SPI 上の通信を低減する、チャンネル・シーケンサが搭載されています。

本デバイスは、ランダムなハードウェア障害を軽減および検出できる多数の監視 / 診断機能を内蔵しているため、機能安全 BMS の開発が容易になります。

最大 16V の入力範囲を持つ内部リニア・レギュレータは、非安定型 DC/DC コンバータを使用したデバイスへの電力供給をサポートしています。

ADS131B23-Q1 は、48 ピン HTQFP パッケージで供給され、車載用温度範囲の  $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$  で動作が規定されています。

## 6 Pin Configuration and Functions



**图 6-1. PHP Package, 48-Pin HTQFP (Top View)**

**表 6-1. Pin Functions**

PIN		TYPE	DESCRIPTION <sup>(1)</sup>
NAME	NO.		
AGND	39	Analog supply	Analog ground.
AGND	21	Analog supply	Analog ground.
AGNDA	42	Analog supply	Section A analog ground. Connect to AGND.
AGNDB	19	Analog supply	Section B analog ground. Connect to AGND.
APWR	38	Analog supply	Analog power supply. Connect a 1- $\mu$ F capacitor to AGND.
AVDD	40	Analog supply	Analog supply. Connect a 1- $\mu$ F capacitor to AGND. Sets the logic levels for GPIO0A, GPIO1A, GPIO0B, and GPIO1B.
CLK	32	Digital I/O	Main clock input. <sup>(4)</sup>
CNA	6	Analog input	ADC1A negative analog input.
CNB	9	Analog input	ADC1B negative analog input.
CPA	5	Analog input	ADC1A positive analog input.
CPB	10	Analog input	ADC1B positive analog input.

**表 6-1. Pin Functions (continued)**

PIN		TYPE	DESCRIPTION <sup>(1)</sup>
NAME	NO.		
CSn	31	Digital input	Chip-select input; active low. Internal pullup resistor to IOVDD. <sup>(4)</sup>
DCAP	36	Digital supply	DVDD LDO output. Connect a 220-nF capacitor to DGND.
DGND	35	Digital supply	Digital ground.
DPWR	37	Digital supply	Digital power supply. Connect a 1- $\mu$ F capacitor to DGND.
DRDYn	27	Digital output	Data-ready output; active low. <sup>(2) (4)</sup>
GPIO0A	3	Digital I/O	General-purpose digital input/output 0A. <sup>(2) (3)</sup>
GPIO0B	8	Digital I/O	General-purpose digital input/output 0B. <sup>(2) (3)</sup>
GPIO0/MHD	33	Digital I/O	General-purpose digital input/output 0. <sup>(2) (4)</sup> Missing host detect output. <sup>(2) (4)</sup>
GPIO1	26	Digital I/O	General-purpose digital input/output 1. <sup>(2) (4)</sup>
GPIO1A	4	Digital I/O	General-purpose digital input/output 1A. <sup>(2) (3)</sup>
GPIO1B	7	Digital I/O	General-purpose digital input/output 1B. <sup>(2) (3)</sup>
GPIO2/FAULT	25	Digital I/O	General-purpose digital input/output 2. <sup>(2) (4)</sup> Fault output. <sup>(2) (4)</sup>
GPIO3/OCCA	24	Digital I/O	General-purpose digital input/output 3. <sup>(2) (4)</sup> Overcurrent comparator A output. <sup>(2) (4)</sup>
GPIO4/OCCB	22	Digital I/O	General-purpose digital input/output 4. <sup>(2) (4)</sup> Overcurrent comparator B output. <sup>(2) (4)</sup>
IOVDD	34	Digital supply	Digital I/O supply. Connect a 1- $\mu$ F capacitor to DGND. Sets the logic levels for the digital I/Os, except for GPIO0A, GPIO1A, GPIO0B, and GPIO1B.
NC	11 to 18	NC	No connect. Leave these pins floating or connected to AGNDB.
RCAPA	41	Analog output	REFA voltage reference output. Connect a 1- $\mu$ F capacitor to AGNDA.
RCAPB	20	Analog output	REFB voltage reference output. Connect a 1- $\mu$ F capacitor to AGNDB.
RESETn	23	Digital input	Reset input; active low. Internal pulldown resistor to DGND.
SCLK	28	Digital input	Serial data clock input. <sup>(4)</sup>
SDI	30	Digital input	Serial data input. <sup>(4)</sup>
SDO	29	Digital output	Serial data output. <sup>(2) (4)</sup>
V0A	2	Analog input	ADC2A analog input 0A.
V1A	1	Analog input	ADC2A analog input 1A.
V2A	48	Analog input	ADC2A analog input 2A.
V3A	47	Analog input	ADC2A analog input 3A.
V4A	46	Analog input	ADC2A analog input 4A.
V5A	45	Analog input	ADC2A analog input 5A.
V6A	44	Analog input	ADC2A analog input 6A.
V7A	43	Analog input	ADC2A analog input 7A.
Thermal Pad	Pad	—	Thermal power pad. Connect to AGND.

- (1) See the [Unused Inputs and Outputs](#) section for details on how to connect unused pins.
- (2) Push-pull output.
- (3) Logic levels referenced to AVDD.
- (4) Logic levels referenced to IOVDD.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	APWR to AGND	-0.3	20	V
	DPWR to DGND	-0.3	20	
	AGND, AGNDy to DGND	-0.3	0.3	
	AVDD to AGND	-0.3	4	
	IOVDD to DGND	-0.3	7	
	DCAP to DGND	-0.3	2.2	
	RCAPy to AGND	-0.3	2.2	
Analog input voltage	CPy, CNy, Vxy	AGND - 1.6	AVDD + 0.3	V
Digital input voltage	CSn, SCLK, SDI, SDO, RESETn, DRDYn, CLK, GPIO0/MHD, GPIO1, GPIO2/FAULT, GPIO3/OCCA, GPIO4/OCCB	DGND - 0.3	IOVDD + 0.3	V
	GPIO0A, GPIO1A	AGNDA - 0.3	AVDD + 0.3	
	GPIO0B, GPIO1B	AGNDB - 0.3	AVDD + 0.3	
Input current	Continuous, all pins except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	-60	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000	V	
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins		±750
			All other non-corner pins		±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>						
	Power supply	APWR to AGND	4		16	V
		APWR = AVDD to AGND (APWR shorted to AVDD, AVDD LDO bypassed)	2.9	3.3	3.6	
		DPWR to DGND	4		16	
		DPWR = IOVDD to DGND (DPWR shorted to IOVDD, IOVDD LDO bypassed)	2.9	3.3	5.5	
		AGND, AGNDy to DGND	-0.2	0	0.2	
<b>ANALOG INPUTS ADC1A, ADC1B<sup>(1)</sup></b>						
$V_{CPy}, V_{CNy}$	Absolute input voltage	Gain = 4, 8, 16, 32	AGND - 0.3125		AVDD - 2.4	V
$V_{IN1y}$	Differential input voltage	$V_{IN1y} = V_{CPy} - V_{CNy}$	$-V_{REFy} / \text{Gain}$		$V_{REFy} / \text{Gain}$	V
<b>ANALOG INPUTS ADC2A<sup>(1)</sup></b>						
$V_{Vxy}$	Absolute input voltage	Gain = 1, 2	AGND - 0.1		AVDD - 1.2	V
		Gain = 4	AGND - 0.3125		AVDD - 2.4	
$V_{IN2y}$	Differential input voltage	$V_{IN2y} = V_{Vxy} - V_{AGNDy}$ or $V_{IN2y} = V_{Vxy} - V_{7y}$	$-V_{REFy} / \text{Gain}$		$V_{REFy} / \text{Gain}$	V
<b>EXTERNAL CLOCK SOURCE<sup>(2)</sup></b>						
$f_{CLK}$	External clock frequency		7.8	8.192	8.4	MHz
	Duty cycle		40%	50%	60%	
<b>DIGITAL INPUTS</b>						
	Input voltage	CSn, SCLK, SDI, SDO, RESETn, DRDYn, CLK, GPIO0/MHD, GPIO1, GPIO2/FAULT, GPIO3/OCCA, GPIO4/OCCB	DGND		IOVDD	V
		GPIO0A, GPIO1A	AGNDA		AVDD	
		GPIO0B, GPIO1B	AGNDB		AVDD	
<b>EXTERNAL CAPACITORS</b>						
	Capacitor value <sup>(3)</sup>	APWR, DPWR		1		μF
		AVDD, IOVDD	0.5	1	2	
		RCAPA, RCAPB	0.5	1	1.4	
		DCAP		220		
<b>TEMPERATURE RANGE</b>						
$T_A$	Specified ambient temperature		-40		105	°C
	Operating ambient temperature		-45		125	

- (1) The subscript y refers to section A or section B.  
The subscript x refers to analog input channel x on ADC2y.
- (2) An external clock is not required when the internal oscillator is used.
- (3) Capacitor values that need to be met over temperature and lifetime.  
See the [Power-Supply Decoupling](#) section for additional information.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TQFP (PHP)	UNIT
		48 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	23.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	15.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

minimum and maximum specifications apply from T<sub>A</sub> = –40°C to +105°C; typical specifications are at T<sub>A</sub> = 25°C; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock, f<sub>CLK</sub> = 8.192 MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT MEASUREMENT ADCS (ADC1A, ADC1B)</b>					
	Resolution	24			Bits
	Gain settings	4, 8, 16, 32			V/V
f <sub>DATA</sub>	Output data rate	f <sub>CLK</sub> = 8.192 MHz		64k	SPS
	Absolute input current	All data rates, all gains, global-chop enabled or disabled, V <sub>CPY</sub> = V <sub>CNY</sub> = 0 V		±0.5	nA
	Differential input current	All data rates, all gains, global-chop enabled or disabled, V <sub>CPY</sub> = V <sub>CNY</sub> = 0 V		–5      ±1      5	nA
	Differential input impedance	All data rates, all gains, global-chop enabled or disabled		1.8	MΩ
	Offset error (input referred)	Gain = 4, global-chop disabled		±1	μV
		Gain = 8 to 32, global-chop disabled		±15	
		All gains, global-chop enabled		–1.5      ±0.5      1.5	
	Offset drift	All gains, global-chop disabled		20      100	nV/°C
		All gains, global-chop enabled		1      7	
	Gain error	T <sub>A</sub> = 25°C, all gains, single-ended operation with CNY held at AGNDy, including initial accuracy of REFy		–0.15%      ±0.05%      0.15%	
	Gain drift	All gains, single-ended operation with CNY held at AGNDy, including drift of REFy		5      20	ppm/°C
	Gain long-term drift	1000 hours at 85°C, all gains, including long-term drift of REFy		±100	ppm
	Gain match	Between gain settings		–0.12%      ±0.03%      0.12%	
	Noise (input referred)	Gain = 8, f <sub>DATA</sub> = 1 kSPS		0.65	μV <sub>RMS</sub>
CMRR	Common-mode rejection ratio	At DC, global-chop disabled		110	dB
		At DC, global-chop enabled		113	
PSRR	Power-supply rejection ratio	APWR at DC, global-chop enabled or disabled		133	dB
		DPWR at DC, global-chop enabled or disabled		133	
		AVDD at DC, global-chop enabled or disabled		115	
		IOVDD at DC, global-chop enabled or disabled		131	



## 7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock,  $f_{\text{CLK}} = 8.192$  MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VOLTAGE AND TEMPERATURE MEASUREMENT ADC (ADC2A)</b>						
Resolution		16			Bits	
Gain settings			1, 2, 4		V/V	
Absolute input current	OSR2y = 64, all gains, $V_{\text{Vxy}} = 0$ V		$\pm 0.2$		nA	
Differential input current	OSR2y = 64, all gains, $V_{\text{Vxy}} = 0$ V		$\pm 0.4$		nA	
Differential input impedance	OSR2y = 64, all gains		15		M $\Omega$	
	OSR2y = 128, all gains		30			
	OSR2y = 256, all gains		60			
	OSR2y = 512, all gains		120			
Offset error (input referred)	Gain = 1	-350	$\pm 85$	350	$\mu\text{V}$	
	Gain = 2 and 4	-25	$\pm 5$	25		
Offset drift	Gain = 1		60	300	nV/ $^\circ\text{C}$	
	Gain = 2 and 4		30	150		
Gain error	$T_A = 25^\circ\text{C}$ , all gains, including initial accuracy of REFy	-0.3%	$\pm 0.1\%$	0.3%		
Gain drift	All gains, including drift of REFy		5	20	ppm/ $^\circ\text{C}$	
Gain long-term drift	1000 hours at $85^\circ\text{C}$ , all gains, including long-term drift of REFy		$\pm 100$		ppm	
Gain match	Between gain settings	-0.15%	$\pm 0.06\%$	0.15%		
CMRR	Common-mode rejection ratio	At DC	95		dB	
PSRR	Power-supply rejection ratio	APWR at DC	103		dB	
		DPWR at DC	103			
		AVDD at DC	91			
		IOVDD at DC	96			
Gain long-term drift	1000 hours at $85^\circ\text{C}$ , all gains, including long-term drift of REFy		$\pm 100$		ppm	
<b>PRECISION VOLTAGE REFERENCES (REFA, REFB)</b>						
$V_{\text{REFA}}$ , $V_{\text{REFB}}$	Reference voltage		1.25		V	
	Accuracy	$T_A = 25^\circ\text{C}$	-0.15%	$\pm 0.05\%$	0.15%	
	Temperature drift		3	15	ppm/ $^\circ\text{C}$	
	Output current	Source only, available for external loads on RCAPy pin		250	$\mu\text{A}$	
	Short-circuit current limit	Sink or source	-10	10	mA	
	Start-up time	1- $\mu\text{F}$ capacitor on RCAPy, 0.01% settling		8	ms	
<b>MAIN OSCILLATOR (OSCM)</b>						
$f_{\text{OSCM}}$	Frequency		8.192		MHz	
	Accuracy		-2.5%	2.5%		
<b>DIAGNOSTIC OSCILLATOR (OSCD)</b>						
$f_{\text{OSCD}}$	Frequency		8.192		MHz	
	Accuracy		-2.5%	2.5%		
<b>OVERCURRENT COMPARATORS (OCCA, OCCB)</b>						
	Offset error (input referred)	All gains	-500	$\pm 20$	500	$\mu\text{V}$
	Gain error	All gains, including error of REFy	-0.5%	$\pm 0.2\%$	0.5%	
<b>TEMPERATURE SENSOR (TSA)</b>						
$T_{\text{SOffset}}$	Output voltage	$T_A = 25^\circ\text{C}$		118.4	mV	
$T_{\text{STC}}$	Temperature coefficient			410	$\mu\text{V}/^\circ\text{C}$	

## 7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock,  $f_{\text{CLK}} = 8.192$  MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>COMMON-MODE OUTPUT BUFFERS (VCMA)</b>						
$V_{\text{CMA}}$	Common-mode output voltage		0.75	0.78	0.81	V
	Output current	Sink or source	-1		1	mA
	Short-circuit current limit	Sink or source	-5		5	mA
	Capacitive load				100	pF
<b>TEST DACS (TDACA, TDACB)</b>						
	Output voltage settings		$1 \times V_{\text{REFy}} / 40$ $2 \times V_{\text{REFy}} / 40$ $4 \times V_{\text{REFy}} / 40$ $9 \times V_{\text{REFy}} / 40$ $18 \times V_{\text{REFy}} / 40$ $36 \times V_{\text{REFy}} / 40$ $-4 \times V_{\text{REFy}} / 40$ $-9 \times V_{\text{REFy}} / 40$			V
	Accuracy		±0.3%			
	Drift	Positive output voltages	6			35
		Negative output voltages	12			80
<b>OPEN-WIRE DETECTION CURRENT SOURCES AND SINKS (OWD1A, OWD1B, OWD2A)</b>						
	Current source settings		4, 40, 240			μA
	Current sink settings		4, 40, 240			μA
	Current source accuracy		±8%			
	Current sink accuracy		±8%			
<b>DIGITAL INPUTS/OUTPUTS (GPIO0A, GPIO1A, GPIO0B, GPIO1B)</b>						
$V_{\text{IL}}$	Logic input level, low		AGNDy		0.3 AVDD	V
$V_{\text{IH}}$	Logic input level, high		0.7 AVDD		AVDD	V
$V_{\text{OL}}$	Logic output level, low	$I_{\text{OL}} = -100 \mu\text{A}$			0.2 AVDD	V
$V_{\text{OH}}$	Logic output level, high	$I_{\text{OH}} = 100 \mu\text{A}$	0.8 AVDD			V
$I_{\text{IN}}$	Input current	$\text{AGNDy} < V_{\text{Digital Input}} < \text{AVDD}$	-1		1	μA
	Short-circuit current limit	Sink or source	-8		8	mA
<b>DIGITAL INPUTS/OUTPUTS (CSn, SCLK, SDI, SDO, RESETn, DRDn, CLK, GPIO0/MHD, GPIO1, GPIO2/FAULT, GPIO3/OCCA, GPIO4/OCCB)</b>						
$V_{\text{IL}}$	Logic input level, low		DGND		0.3 IOVDD	V
$V_{\text{IH}}$	Logic input level, high		0.7 IOVDD		IOVDD	V
$V_{\text{OL}}$	Logic output level, low	$I_{\text{OL}} = -1 \text{ mA}$			0.2 IOVDD	V
$V_{\text{OH}}$	Logic output level, high	$I_{\text{OH}} = 1 \text{ mA}$	0.8 IOVDD			V
$I_{\text{IN}}$	Input current	$\text{DGND} < V_{\text{Digital Input}} < \text{IOVDD}$	-1		1	μA
	Short-circuit current limit	Sink or source	-80		80	mA

## 7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock,  $f_{\text{CLK}} = 8.192$  MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CLOCK MONITORS</b>						
$f_{\text{MCLK\_WD\_TH}}$	Main clock (MCLK) watchdog frequency threshold	Watchdog indicates a fault when MCLK frequency drops below frequency threshold			300	kHz
$f_{\text{OSCD\_WD\_TH}}$	Diagnostic oscillator (OSCD) watchdog frequency threshold	Watchdog indicates a fault when OSCD frequency drops below frequency threshold			300	kHz
MCLK_FAULT_TH	Main clock fault detection frequency threshold	Difference in clock frequencies between MCLK and OSCD to generate a fault		10%		
<b>POWER SUPPLY MONITORS</b>						
AVDD_UV_TH	AVDD undervoltage threshold		2.9	2.95	3.0	V
AVDD_OV_TH	AVDD overvoltage threshold		3.8	3.9	4.0	V
IOVDD_UV_TH	IOVDD undervoltage threshold	IOVDD_UV_TH = 1b	2.9	2.95	3.0	V
		IOVDD_UV_TH = 0b	4.2	4.3	4.4	
IOVDD_OV_TH	IOVDD overvoltage threshold	IOVDD_OV_TH = 1b	3.8	3.9	4.0	V
		IOVDD_OV_TH = 0b	5.6	5.75	5.9	
DVDD_UV_TH	DVDD undervoltage threshold		1.55	1.6	1.65	V
DVDD_OV_TH	DVDD overvoltage threshold		1.90	1.95	2.0	V
AVDD_OSC_MAG	AVDD oscillation detection magnitude	Amplitude required to generate fault	500			mV <sub>pp</sub>
AVDD_OSC_FREQ	AVDD oscillation detection input frequency	Oscillation frequency range to generate fault	2		500	kHz
IOVDD_OSC_MAG	IOVDD oscillation detection magnitude	Amplitude required to generate fault	500			mV <sub>pp</sub>
IOVDD_OSC_FREQ	IOVDD oscillation detection input frequency	Oscillation frequency range to generate fault	2		500	kHz
DVDD_OSC_MAG	DVDD oscillation detection magnitude	Amplitude required to generate fault	500			mV <sub>pp</sub>
DVDD_OSC_FREQ	DVDD oscillation detection input frequency	Oscillation frequency range to generate fault	2		500	kHz
AVDD_OTW_TH	AVDD overtemperature warning thresholds			-60 100 120 140		°C
		AVDD overtemperature warning threshold accuracy			±2	
IOVDD_OTW_TH	IOVDD overtemperature warning thresholds			-60 100 120 140		°C
		IOVDD overtemperature warning threshold accuracy			±2	
	ADC2y power-supply readback attenuation factor	APWR		103		
		DPWR		103		
		AVDD		4		
		IOVDD		4		
		DVDD		2		
	ADC2y power-supply readback accuracy	OSR2y = 128, MUX2y_DELAY ≥ 256 × t <sub>MCLK</sub>		±1%		
AVDD_POR_TH	AVDD POR release threshold		2.6	2.7	2.85	V
IOVDD_POR_TH	IOVDD POR release threshold		2.6	2.7	2.85	V
DVDD_POR_TH	DVDD POR release threshold		1.4	1.5	1.6	V

## 7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock,  $f_{\text{CLK}} = 8.192$  MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FAULT MONITOR RESPONSE TIMES</b>						
$t_{p(\text{AVDD\_OV})}$	AVDD overvoltage detection response time	Delay time from AVDD exceeding AVDD overvoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{IOVDD\_OV})}$	IOVDD overvoltage detection response time	Delay time from IOVDD exceeding IOVDD overvoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{DVDD\_OV})}$	DVDD overvoltage detection response time	Delay time from DVDD exceeding DVDD overvoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{AVDD\_UV})}$	AVDD undervoltage detection response time	Delay time from AVDD dropping below AVDD undervoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{IOVDD\_UV})}$	IOVDD undervoltage detection response time	Delay time from IOVDD dropping below IOVDD undervoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{DVDD\_UV})}$	DVDD undervoltage detection response time	Delay time from DVDD dropping below DVDD undervoltage threshold to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{AVDD\_OSC})}$	AVDD oscillation detection response time	Delay time from AVDD oscillations exceeding AVDD oscillation threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{IOVDD\_OSC})}$	IOVDD oscillation detection response time	Delay time from IOVDD oscillations exceeding IOVDD oscillation threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{DVDD\_OSC})}$	DVDD oscillation detection response time	Delay time from DVDD oscillations exceeding DVDD oscillation threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{AVDD\_CL})}$	AVDD current limit detection response time	Delay time from AVDD exceeding AVDD current limit threshold to FAULT pin active			40	$\mu\text{s}$
$t_{p(\text{IOVDD\_CL})}$	IOVDD current limit detection response time	Delay time from IOVDD exceeding IOVDD current limit threshold to FAULT pin active			40	$\mu\text{s}$
$t_{p(\text{AVDD\_OTW})}$	AVDD overtemperature warning response time	Delay time from AVDD exceeding AVDD overtemperature warning threshold to FAULT pin active			300	$\mu\text{s}$
$t_{p(\text{IOVDD\_OTW})}$	IOVDD overtemperature warning response time	Delay time from IOVDD exceeding IOVDD overtemperature warning threshold to FAULT pin active			300	$\mu\text{s}$
$t_{p(\text{AVDD\_POR})}$	AVDD POR detection response time	Delay time from AVDD dropping below AVDD POR threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{IOVDD\_POR})}$	IOVDD POR detection response time	Delay time from IOVDD dropping below IOVDD POR threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{DVDD\_POR})}$	DVDD POR detection response time	Delay time from DVDD dropping below DVDD POR threshold to FAULT pin active			30	$\mu\text{s}$
$t_{p(\text{DGND\_OPEN})}$	DGND open detection response time	Delay time from DGND pin disconnected to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{AGNDy\_OPEN})}$	AGNDy open detection response time	Delay time from AGNDy pin disconnected to FAULT pin active			4	$\mu\text{s}$
$t_{p(\text{MEM\_MAP\_CRC})}$	Memory map CRC fault detection response time	Delay time from bit flip occurrence in memory map to FAULT pin active		69	138	$t_{\text{OSCD}}$
$t_{p(\text{REG\_MAP\_CRC})}$	Register map CRC fault detection response time	Delay time from bit flip occurrence in register map to FAULT pin active		1024	2048	$t_{\text{OSCD}}$
$t_{p(\text{MCLK\_WD})}$	Main clock watchdog response time	Delay time from main clock watchdog timeout to FAULT pin active			2	$\mu\text{s}$
$t_{p(\text{OSCD\_WD})}$	Diagnostic oscillator watchdog response time	Delay time from diagnostic oscillator watchdog timeout to FAULT pin active			2	$\mu\text{s}$
$t_{p(\text{MCLK\_FAULT})}$	Main clock fault detection response time	Delay time from main clock fault detection to FAULT pin active			4096	$t_{\text{MCLK}}$

## 7.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ; all specifications are at APWR = 5 V, DPWR = 5 V, IOVDD = 3.3 V, external clock,  $f_{\text{CLK}} = 8.192$  MHz, global-chop mode disabled, ADC1y data rate = 1 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AVDD LDO</b>						
AVDD	Output voltage		3.1	3.3	3.5	V
	Load current	Available to external circuitry on the AVDD pin			20	mA
	Short-circuit current limit				60	mA
	Load regulation			1		mV/mA
<b>IOVDD LDO</b>						
IOVDD	Output voltage		3.1	3.3	3.5	V
	Load current	Available to external circuitry on the IOVDD pin			20	mA
	Short-circuit current limit				60	mA
	Load regulation			1		mV/mA
<b>SUPPLY CURRENTS</b>						
$I_{\text{APWR}}$	APWR supply current	Power-down mode		0.01		mA
		Standby mode		0.46		
		Active mode, all ADCs disabled		0.8		
		Active mode, all ADCs enabled and converting (all features enabled, no external load on AVDD LDO)		4.8	5.8	
	APWR supply current per individual ADC	ADC1y enabled and converting, all gains, all data rates		1.75		
		ADC2A enabled and converting, all gains, all data rates		0.5		
$I_{\text{DPWR}}$	DPWR supply current <sup>(1)</sup>	Power-down mode		0.01		mA
		Standby mode		0.4		
		Active mode, all ADCs disabled		0.8		
		Active mode, all ADCs enabled and converting (all features enabled, no external load on IOVDD LDO)		1.0	1.5	
	DPWR supply current per individual ADC <sup>(1)</sup>	ADC1y enabled and converting, all data rates		0.06		
		ADC2A enabled and converting, all data rates		0.06		
$I_{\text{AVDD}}$	AVDD supply current	APWR shorted to AVDD, AVDD LDO bypassed, active mode, all ADCs enabled and converting (all features enabled)		4.8		mA
$I_{\text{IOVDD}}$	IOVDD supply current <sup>(1)</sup>	DPWR shorted to IOVDD, IOVDD LDO bypassed, active mode, all ADCs enabled and converting (all features enabled)		1.0		mA
$P_D$	Power dissipation	Active mode, all ADCs enabled and converting (all features enabled, no external load on AVDD LDO)		29		mW

(1) Currents measured with SPI idle.

## 7.6 Timing Requirements

over operating ambient temperature range, SDO load: 20 pF || 100 kΩ (unless otherwise noted)

		MIN	MAX	UNIT
<b>3.0 V ≤ IOVDD ≤ 3.6 V</b>				
t <sub>w(CLH)</sub>	Pulse duration, CLK high	49		ns
t <sub>w(CLL)</sub>	Pulse duration, CLK low	49		ns
t <sub>c(SC)</sub>	SCLK period	64		ns
t <sub>w(SCL)</sub>	Pulse duration, SCLK low	32		ns
t <sub>w(SCH)</sub>	Pulse duration, SCLK high	32		ns
t <sub>d(CSSC)</sub>	Delay time, first SCLK rising edge after CSn falling edge	16		ns
t <sub>d(SCCS)</sub>	Delay time, CSn rising edge after final SCLK falling edge	10		ns
t <sub>w(CSH)</sub>	Pulse duration, CSn high	20		ns
t <sub>su(DI)</sub>	Setup time, SDI valid before SCLK falling edge	5		ns
t <sub>h(DI)</sub>	Hold time, SDI valid after SCLK falling edge	8		ns
t <sub>w(RSL)</sub>	Pulse duration, RESETh low to generate device reset	500		ns
<b>4.5 V ≤ IOVDD ≤ 5.5 V</b>				
t <sub>w(CLL)</sub>	Pulse duration, CLK low	49		ns
t <sub>w(CLH)</sub>	Pulse duration, CLK high	49		ns
t <sub>c(SC)</sub>	SCLK period	50		ns
t <sub>w(SCL)</sub>	Pulse duration, SCLK low	25		ns
t <sub>w(SCH)</sub>	Pulse duration, SCLK high	25		ns
t <sub>d(CSSC)</sub>	Delay time, first SCLK rising edge after CSn falling edge	16		ns
t <sub>d(SCCS)</sub>	Delay time, CSn rising edge after final SCLK falling edge	10		ns
t <sub>w(CSH)</sub>	Pulse duration, CSn high	15		ns
t <sub>su(DI)</sub>	Setup time, SDI valid before SCLK falling edge	5		ns
t <sub>h(DI)</sub>	Hold time, SDI valid after SCLK falling edge	8		ns
t <sub>w(RSL)</sub>	Pulse duration, RESETh low to generate device reset	500		ns

## 7.7 Switching Characteristics

over operating ambient temperature range, SDO load: 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>3.0 V ≤ IOVDD ≤ 3.6 V</b>						
$t_{p(CSDO)}$	Propagation delay time, CSn falling edge to SDO driven			50	ns	
$t_{p(CSDOZ)}$	Propagation delay time, CSn rising edge to SDO high impedance			75	ns	
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new SDO			32	ns	
$t_{w(DRH)}$	Pulse duration, DRDYn high		4		$t_{MCLK}$	
$t_{TIMEOUT}$	SPI timeout	16385			$t_{OSCD}$	
$t_{POR}$	Power-on-reset time	Measured from supplies crossing POR threshold to DRDYn rising edge		250	μs	
$t_{REGACQ}$	Register default value acquisition time	Measured from RESETn rising edge to DRDYn rising edge		44	114	μs
<b>4.5 V ≤ IOVDD ≤ 5.5 V</b>						
$t_{p(CSDO)}$	Propagation delay time, CSn falling edge to SDO driven			50	ns	
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new SDO			20	ns	
$t_{p(CSDOZ)}$	Propagation delay time, CSn rising edge to SDO high impedance			75	ns	
$t_{w(DRH)}$	Pulse duration, DRDYn high		4		$t_{MCLK}$	
$t_{TIMEOUT}$	SPI timeout	16385			$t_{OSCD}$	
$t_{POR}$	Power-on-reset time	Measured from supplies crossing POR threshold to DRDYn rising edge		250	μs	
$t_{REGACQ}$	Register default value acquisition time	Measured from RESETn rising edge to DRDYn rising edge		44	114	μs

## 7.8 Timing Diagram

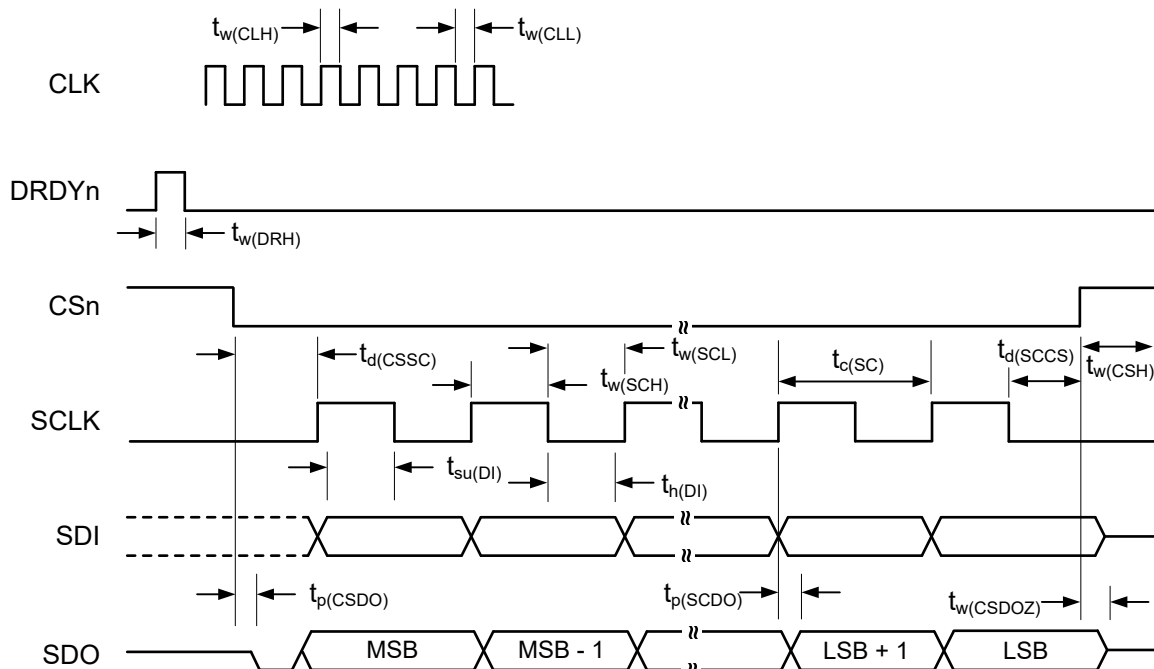
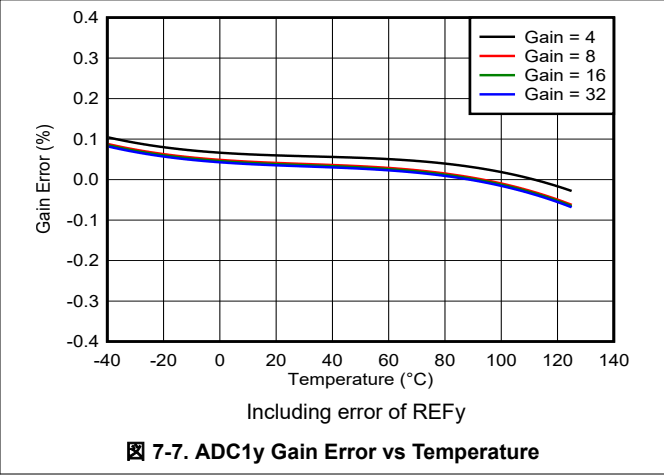
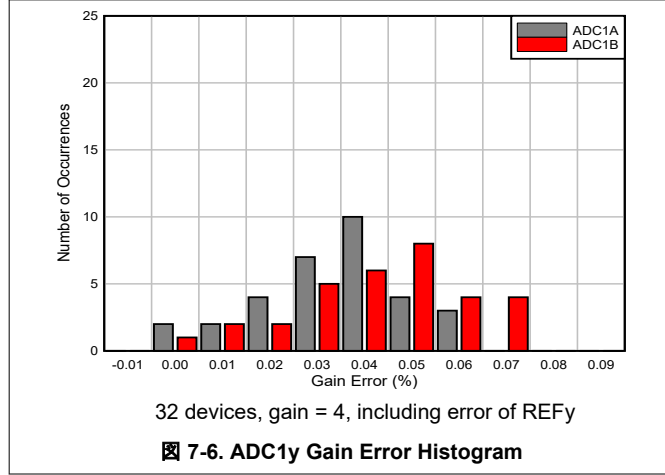
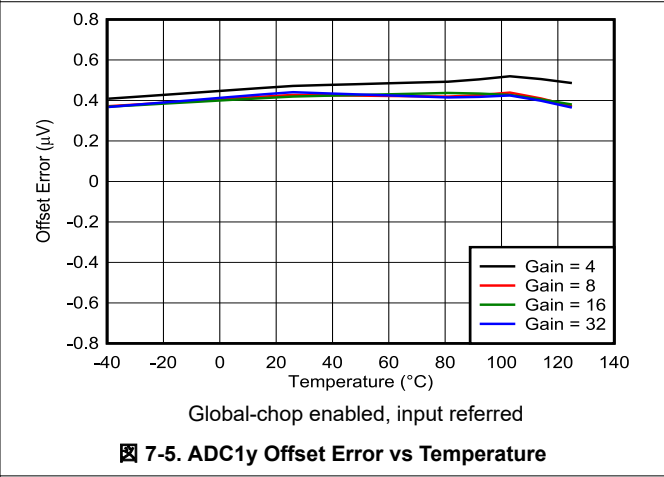
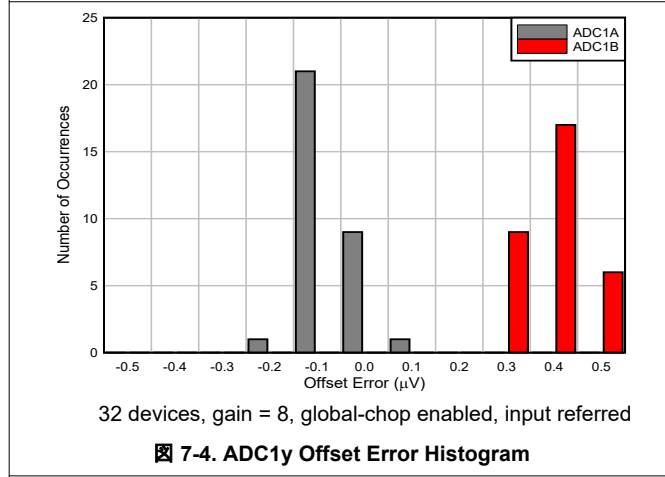
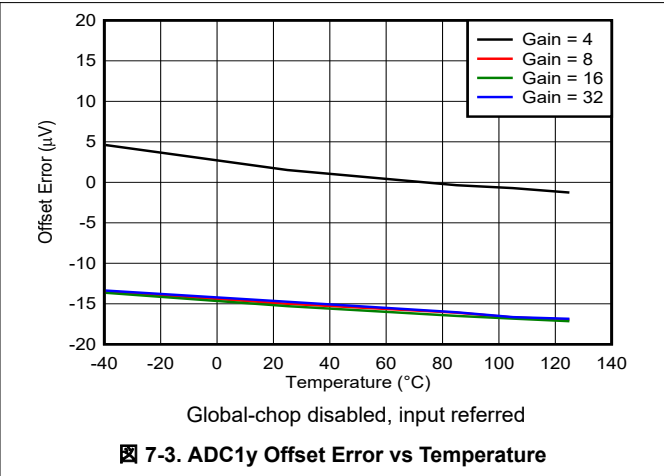
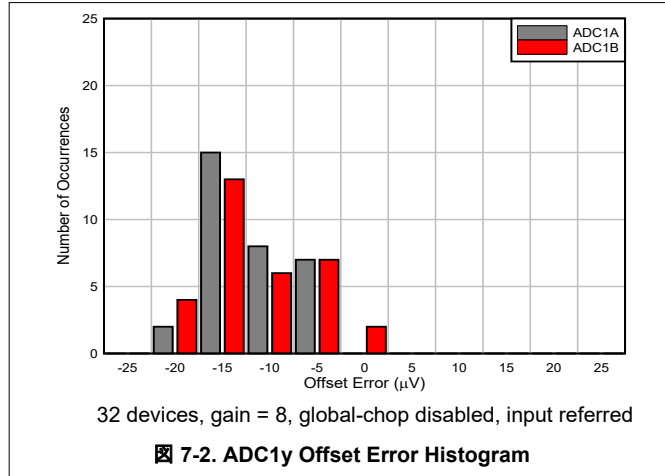


FIG 7-1. SPI Timing Requirements and Switching Characteristics

## 7.9 Typical Characteristics

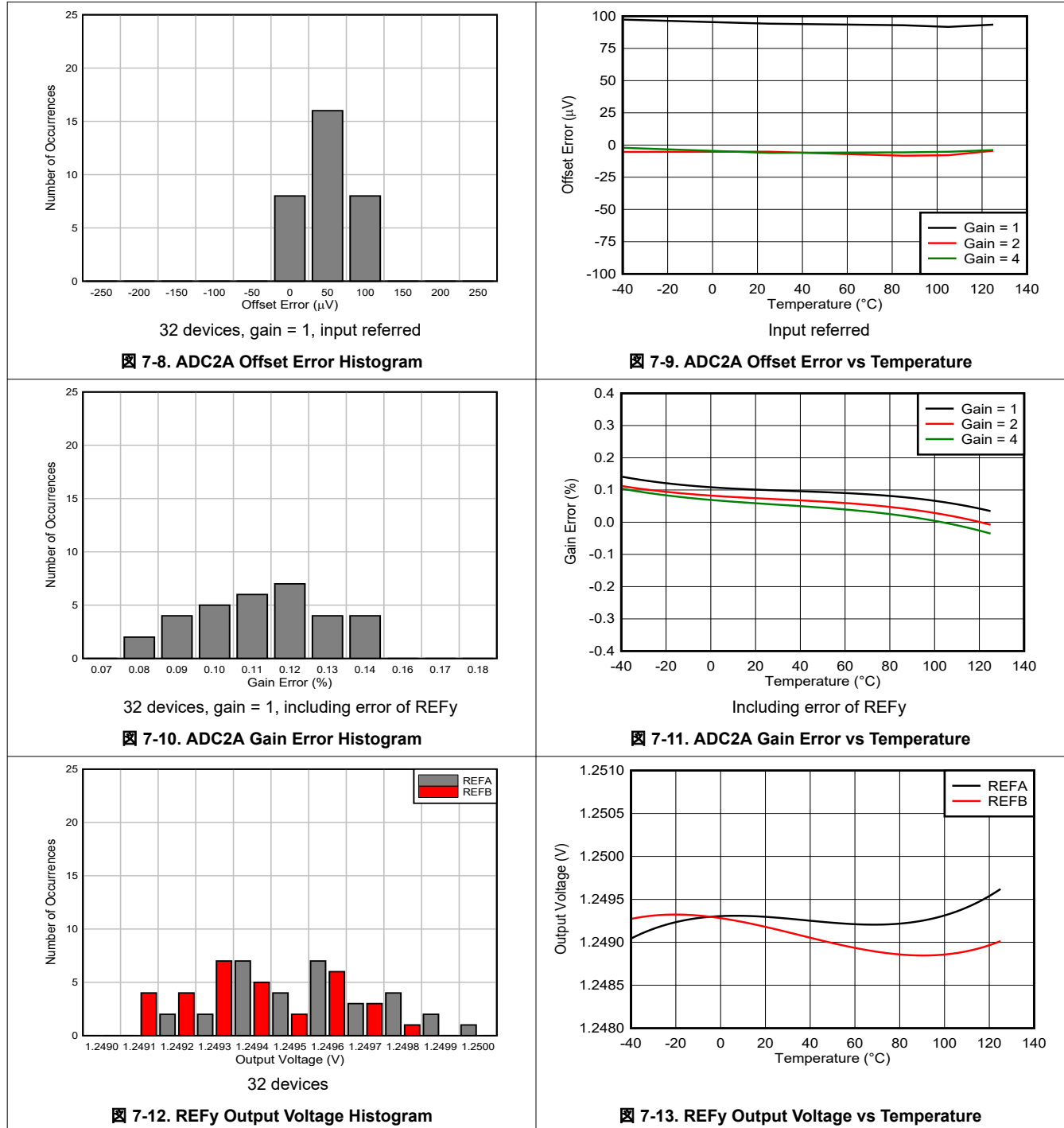
at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192\text{ MHz}$  (unless otherwise noted)





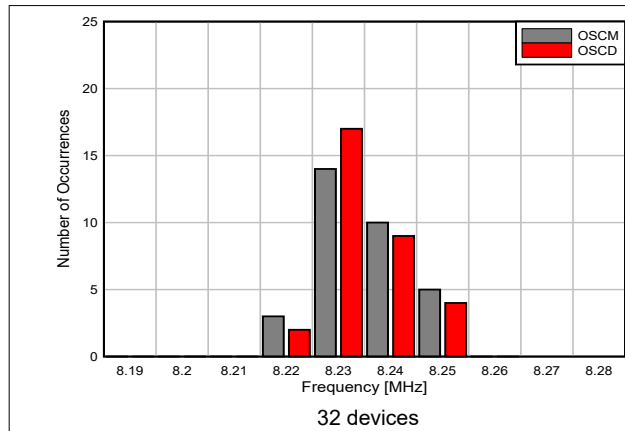
## 7.9 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192\text{ MHz}$  (unless otherwise noted)

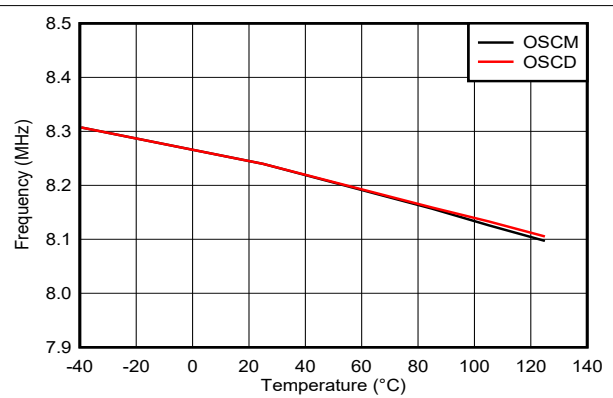


## 7.9 Typical Characteristics (continued)

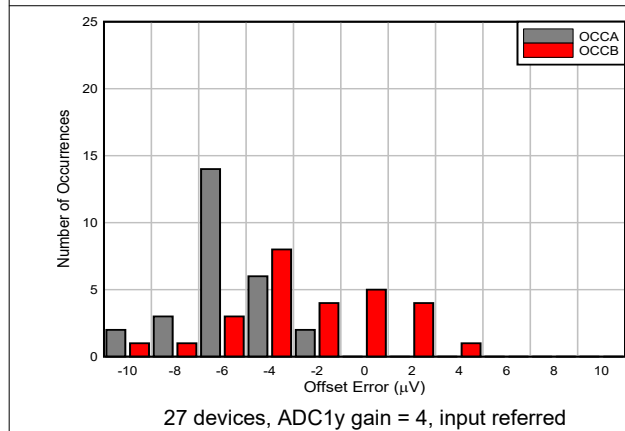
at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192$  MHz (unless otherwise noted)



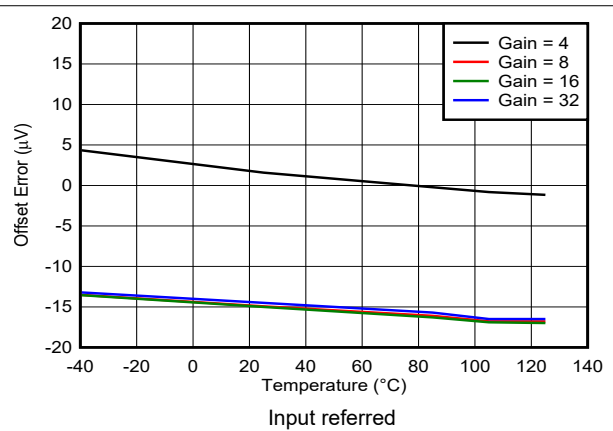
7-14. OSCM and OSCD Frequency Histogram



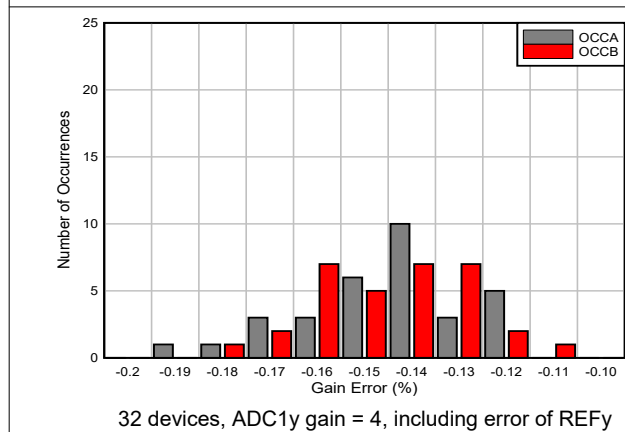
7-15. OSCM and OSCD Frequency vs Temperature



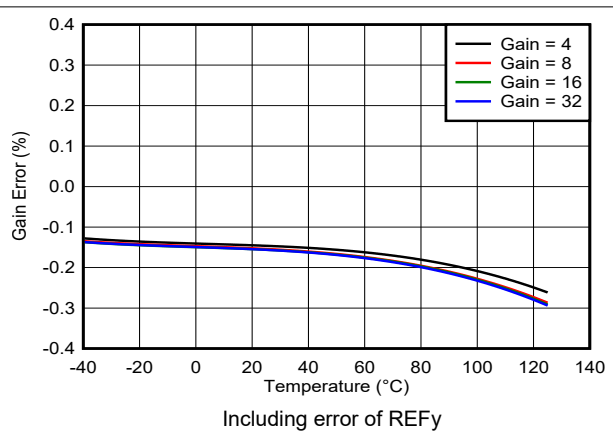
7-16. OCCy Offset Error Histogram



7-17. OCCy Offset Error vs Temperature



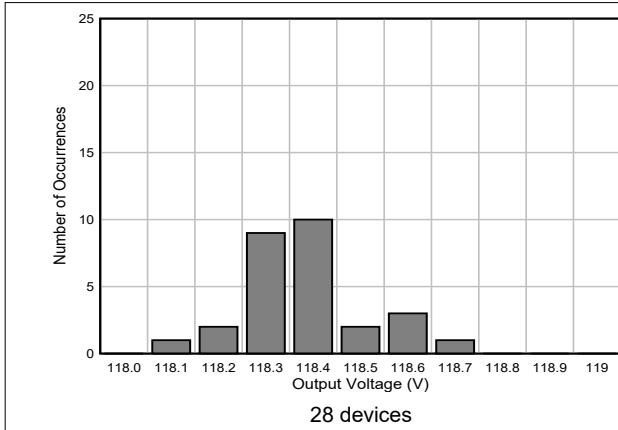
7-18. OCCy Gain Error Histogram



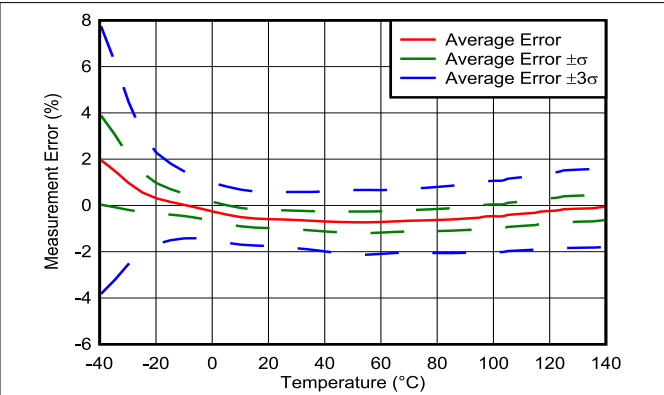
7-19. OCCy Gain Error vs Temperature

## 7.9 Typical Characteristics (continued)

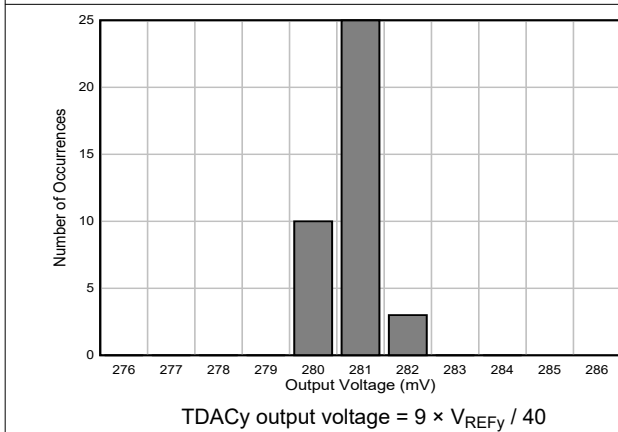
at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192\text{ MHz}$  (unless otherwise noted)



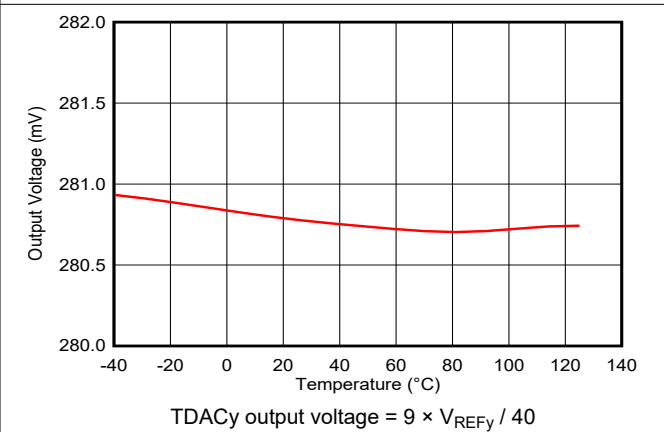
**7-20. Temperature Sensor Output Voltage Histogram**



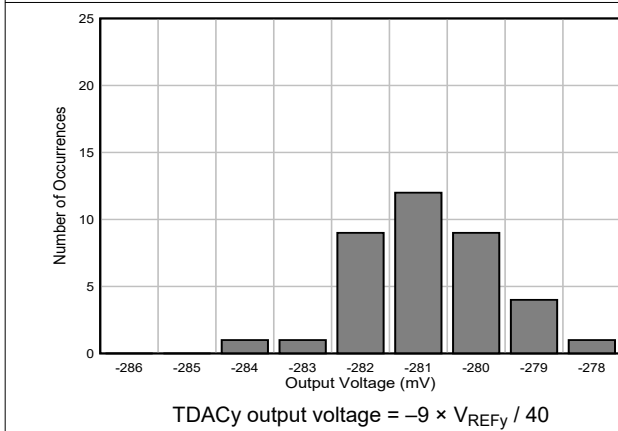
**7-21. Temperature Sensor Measurement Error vs Ambient Temperature**



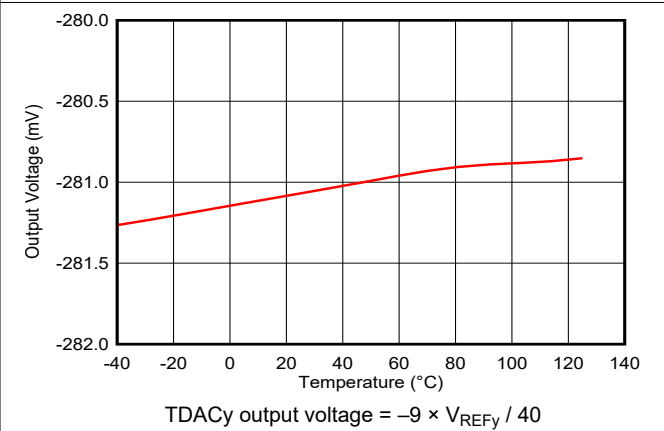
**7-22. Test DACy Output Voltage Histogram**



**7-23. Test DACy Output Voltage vs Temperature**



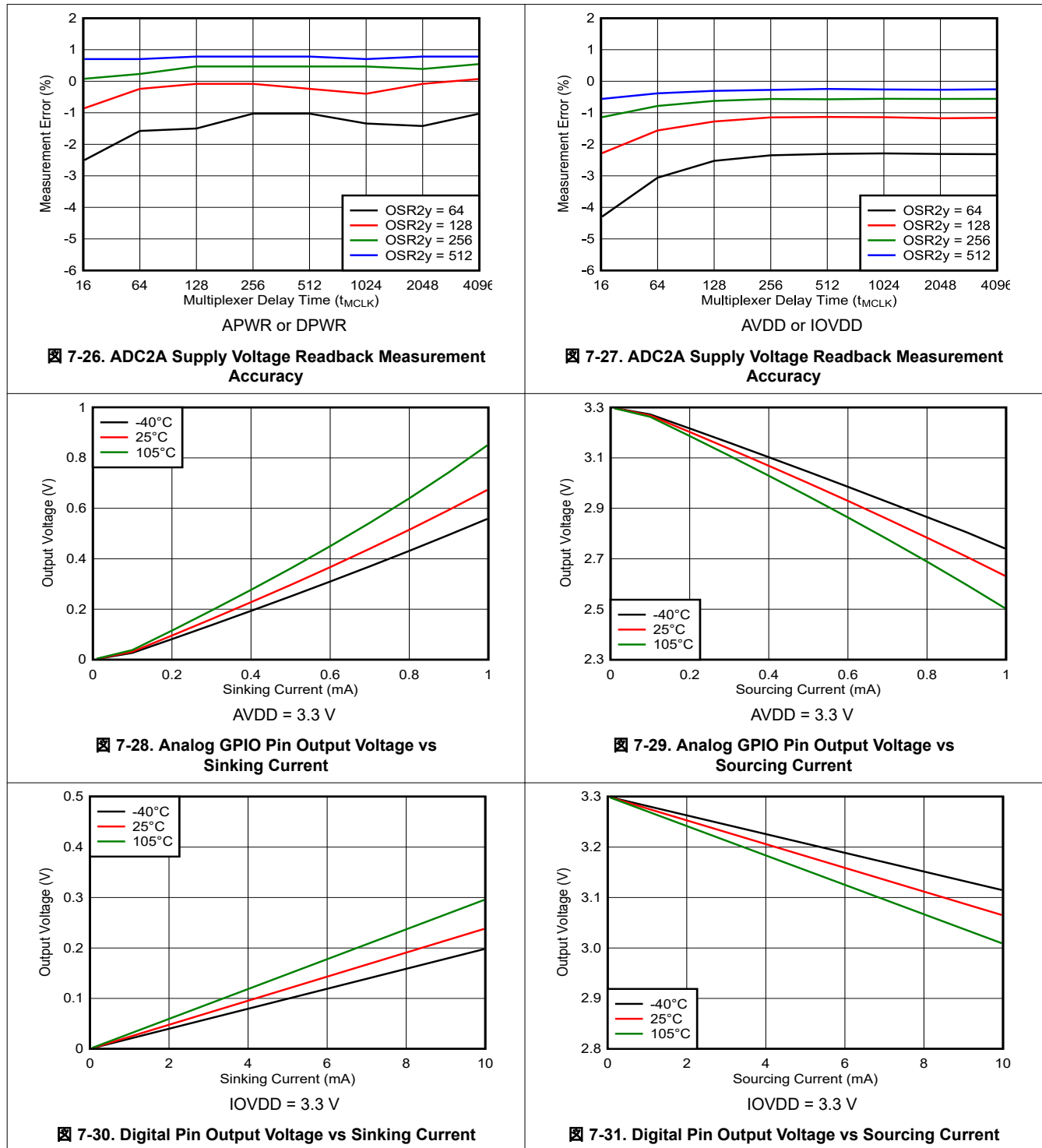
**7-24. Test DACy Output Voltage Histogram**



**7-25. Test DACy Output Voltage vs Temperature**

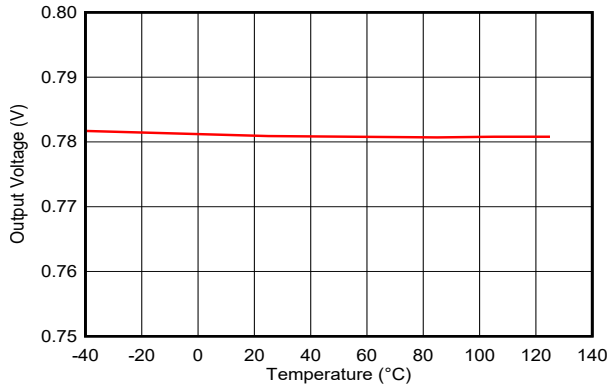
## 7.9 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192\text{ MHz}$  (unless otherwise noted)

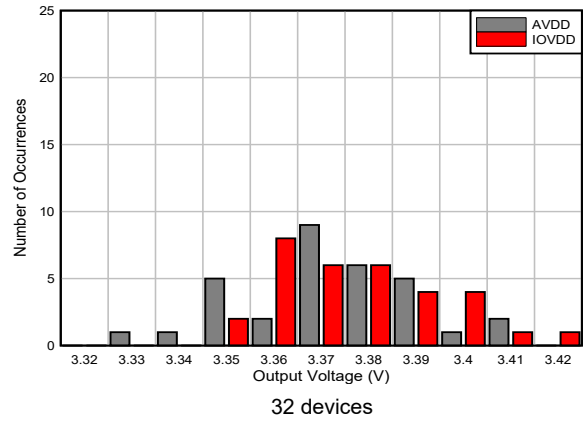


## 7.9 Typical Characteristics (continued)

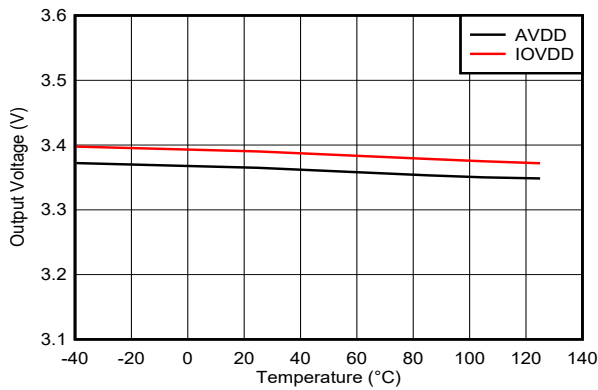
at  $T_A = 25^\circ\text{C}$ , APWR = 5 V, DPWR = 5 V, and external clock with  $f_{\text{CLK}} = 8.192 \text{ MHz}$  (unless otherwise noted)



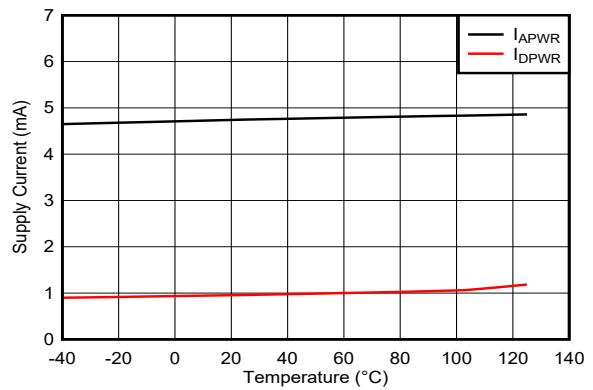
7-32. VCMA Output Voltage vs Temperature



7-33. AVDD and IOVDD LDO Output Voltage Histogram

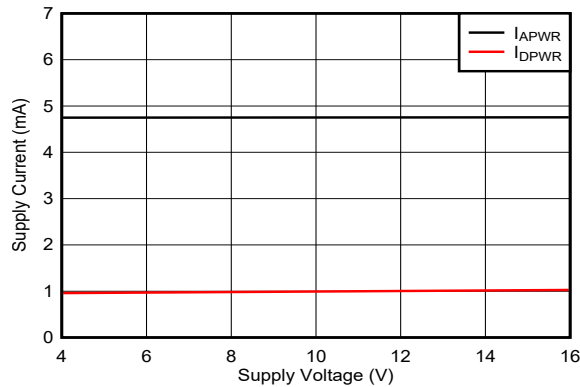


7-34. AVDD and IOVDD LDO Output Voltage vs Temperature



Active mode, all ADCs enabled and converting

7-35. Supply Current vs Temperature



Active mode, all ADCs enabled and converting

7-36. Supply Current vs Supply Voltage

## 8 Parameter Measurement Information

### 8.1 Offset Drift Measurement

Offset drift is defined as the change in offset voltage over the specified temperature range. Offset drift is calculated using the *box method* in which a box is formed over the maximum and minimum offset voltages and over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. For that reason, offset drift is specified as a positive number only, even though the drift can possibly be negative. 式 1 shows the offset drift calculation using the box method:

$$\text{Offset Drift (nV/}^{\circ}\text{C)} = 10^9 \times (V_{\text{OFSMAX}} - V_{\text{OFSMIN}}) / (T_{\text{MAX}} - T_{\text{MIN}}) \quad (1)$$

where:

- $V_{\text{OFSMIN}}$  and  $V_{\text{OFSMAX}}$  = Minimum and maximum offset voltages over the specified temperature range
- $T_{\text{MIN}}$  and  $T_{\text{MAX}}$  = Minimum and maximum temperatures

### 8.2 Gain Drift Measurement

Gain drift is defined as the change of gain error over the specified temperature range. Gain drift is calculated using the *box method* in which a box is formed over the maximum and minimum gain errors and over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. For that reason, gain drift is specified as a positive number only, even though the drift can possibly be negative. 式 2 describes the gain drift calculation using the box method.

$$\text{Gain Drift (ppm/}^{\circ}\text{C)} = (GE_{\text{MAX}} - GE_{\text{MIN}}) / (T_{\text{MAX}} - T_{\text{MIN}}) \quad (2)$$

where:

- $GE_{\text{MIN}}$  and  $GE_{\text{MAX}}$  = Minimum and maximum gain errors over the specified temperature range
- $T_{\text{MIN}}$  and  $T_{\text{MAX}}$  = Minimum and maximum temperatures

### 8.3 Noise Performance

Adjust the data rate and gain to optimize the noise performance of the individual ADCs. When reducing the data rate by increasing the oversampling ratio (OSR), averaging is increased and results in lower noise. 表 8-1 and 表 8-2 summarize the noise performance of ADC1y and ADC2y. The data are representative of typical noise performance at  $T_A = 25^\circ\text{C}$  using  $f_{\text{MCLK}} = 8.192\text{ MHz}$ . The data shown are typical input-referred noise results in units of  $\mu\text{V}_{\text{RMS}}$  with the analog inputs shorted together and averaging data across a 1-ms period. Use 式 3 to calculate effective resolution from the provided  $\mu\text{V}_{\text{RMS}}$  numbers.

$$\text{Effective Resolution} = \ln[(2 \times V_{\text{REFy}} / \text{Gain}) / V_{\text{RMS-Noise}}] / \ln(2) \quad (3)$$

The noise performance of ADC1y improves by a factor of  $\sqrt{2}$  in global-chop mode.

**表 8-1. ADC1y Noise Performance ( $\mu\text{V}_{\text{RMS}}$ ) at  $T_A = 25^\circ\text{C}$**

OSR1y	DATA RATE, $f_{\text{MCLK}} = 8.192\text{ MHz}$	GAIN			
		4	8	16	32
64	64 kSPS	20.7	10.8	10.8	10.8
128	32 kSPS	6.19	3.96	3.96	3.96
256	16 kSPS	3.70	2.51	2.51	2.51
512	8 kSPS	2.61	1.78	1.78	1.78
1024	4 kSPS	1.88	1.28	1.28	1.28
2048	2 kSPS	1.46	0.91	0.91	0.91
4096	1 kSPS	1.15	0.65	0.65	0.65
8192	0.5 kSPS	0.88	0.44	0.44	0.44

**表 8-2. ADC2y Noise Performance ( $\mu\text{V}_{\text{RMS}}$ ) at  $T_A = 25^\circ\text{C}$**

OSR2y	CONVERSION TIME, $f_{\text{MCLK}} = 8.192\text{ MHz}$	GAIN		
		1	2	4
64	46.87 $\mu\text{s}$	93.4	48.3	48.3
128	62.50 $\mu\text{s}$	48.4	26.5	26.5
256	93.75 $\mu\text{s}$	31.9	17.5	17.5
512	156.25 $\mu\text{s}$	22.4	12.1	12.1

## 9 Detailed Description

### 9.1 Overview

The ADS131B23-Q1 is a fully integrated, high-voltage battery pack monitor for automotive electrical vehicle (EV) battery management systems (BMS) that integrates two simultaneous-sampling, high-precision, 24-bit ADC channels (ADC1A, ADC1B) to redundantly measure battery current with high resolution and accuracy using an external shunt resistor. Two independent digital overcurrent detection comparators (OCCA, OCCB) work in parallel to the two ADCs for fast overcurrent detection.

Additionally, a multiplexed, 16-bit ADC (ADC2A) is available to measure shunt temperature using external temperature sensors, such as thermistors or analog output temperature sensors, and other voltages in the system. ADC2A is equipped with a channel sequencer that automatically steps through the configured multiplexer inputs, selects them for measurement, and starts ADC conversions.

The device is partitioned into two sections, A and B. The circuitry in section A is independent from the circuitry in section B. However, both sections are powered from the same supply, derive their respective clocks from the same main clock source, and share the same digital control and serial interface.

Besides the various ADC channels, each section provides:

- A precision, low-drift, 1.25-V voltage reference (REFA, REFB) that feeds the ADCs in each section
- A negative charge pump (NCPA, NCPB) that provides a negative supply voltage for the gain stages in front of each ADC to allow signal measurements below ground
- A Test DAC (Test DAC A, Test DAC B), which generates precision test voltages that can be routed for measurement to the ADCs in the other section
- Two GPIOs (GPIO0A, GPIO1A and GPIO0B, GPIO1B) with logic levels based on AVDD

In many BMS applications, the pack monitor is powered from an unregulated isolated DC/DC converter. For that reason, the ADS131B23-Q1 integrates linear regulators (AVDD and IOVDD LDOs) that accept voltages between 4 V and 16 V and provide regulated 3.3-V analog and digital supply rails for the internal circuitry. The two low-dropout regulators (LDOs) can also provide a limited amount of current to external circuitry. A common use case is to power the primary side of a digital isolator, which isolates the SPI communication to a host microcontroller, with the IOVDD LDO output; see the [ADS131B26Q1EVM-PDK Evaluation Module user guide](#).

The main clock for the ADS131B23-Q1 is either provided by the internal 8.192-MHz oscillator or by an external clock provided at the CLK pin.

A multitude of monitoring and diagnostic features are integrated in the device to mitigate and detect random hardware faults to aid in the development of functional safety BMS, such as:

- Supply undervoltage, overvoltage, overtemperature, and oscillation monitors
- Supply-voltage readback capability through ADC2A
- A set of open-wire detection current sources and sinks per ADC
- Clock monitors
- Cyclic redundancy check (CRC), timeout monitor, and SCLK counter on the SPI to achieve high data integrity for the communication
- Register and memory map CRC
- ADC conversion and sequence counters

The device offers five GPIOs (GPIO0 through GPIO4) with logic levels based on IOVDD and optional pulse-width modulation (PWM) input and output capability. GPIO2 can alternatively be configured as a FAULT output, and GPIO3 and GPIO4 can be configured as overcurrent comparator outputs.

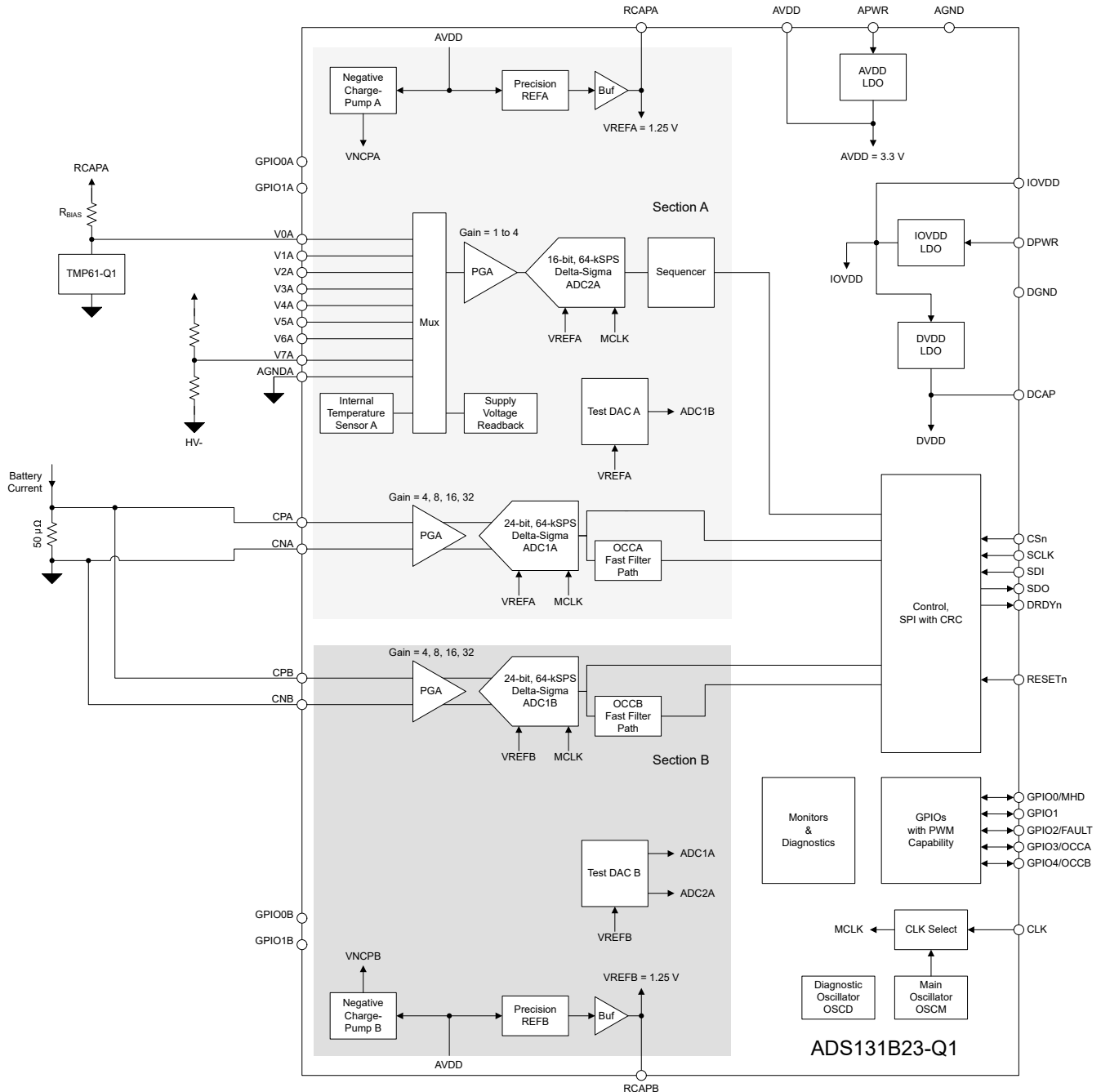


As shown in 表 9-1, the ADS131B2x-Q1 family consists of three devices that differ in the amount of integrated ADC channels.

**表 9-1. ADS131B2x-Q1 Device Family Comparison by Available ADC Channels**

DEVICE	ADC1A, ADC1B	ADC2A	ADC2B	ADC3A, ADC3B
ADS131B23-Q1	Yes	Yes	No	No
ADS131B24-Q1	Yes	Yes	Yes	No
ADS131B26-Q1	Yes	Yes	Yes	Yes

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Naming Conventions

Throughout this document, suffixes  $x$  and  $y$  refer to certain elements of the device:

- Suffix  $y$  refers to elements in both sections  $A$  and  $B$ .  
 For example, ADC $1y$  refers to ADC1A as well as to ADC1B.
- Suffix  $x$  either refers to all ADCs in one section or to all analog inputs of ADC $2y$ .  
 For example, ADC $x$ A refers to ADC1A and ADC2A, and V $x$ A refers to analog inputs V0A to V7A of ADC2A.

### 9.3.2 Precision Voltage References (REFA, REFB)

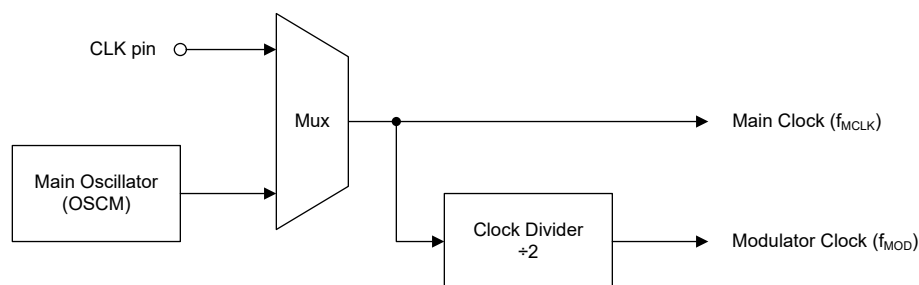
The ADS131B23-Q1 integrates two precision, low-drift, band-gap voltage references (REFA and REFB), one for each section of the device. The references have a nominal voltage of 1.25 V. No external voltage reference can be provided to the device. All ADCs in section A use REFA and, correspondingly, all ADCs in section B use REFB. The RCAPA and RCAPB pins are outputs of the voltage references. Decouple the RCAPA pin with a 1- $\mu$ F capacitor to AGNDA and the RCAPB pin with a 1- $\mu$ F capacitor to AGNDB. The voltage references are buffered and can source external circuitry with a limited amount of current out of the RCAP $y$  pins. The buffers cannot sink any current. See the [Electrical Characteristics](#) table for details.

### 9.3.3 Clocking (MCLK, OSCM, OSCD)

The ADS131B23-Q1 requires a main clock (MCLK) to operate. As shown in [Figure 9-1](#), the main clock to the ADS131B23-Q1 is provided in one of two ways:

- By the internal 8.192-MHz main oscillator (OSCM) or
- By an external clock on the CLK pin

The CLK\_SOURCE bit selects the according main clock source for the device. At device power-up or after device reset, the internal main oscillator is selected as the MCLK source by default.



**Figure 9-1. Main Clock Selection Diagram**

The modulator clock of the various delta-sigma ADCs is derived from the common main clock. A clock divider divides the main clock frequency ( $f_{MCLK}$ ) by a factor of two to create the modulator frequency ( $f_{MOD} = f_{MCLK} / 2$ ) with a duty cycle of 50%.

Before changing the clock source using the CLK\_SOURCE bit, disable all ADCs using the respective ADC enable bits or set the device in standby mode to prevent clock glitching during the clock switchover. When switching from an external clock source to the internal main oscillator, keep the external clock running until after the device switched over to the internal main oscillator.

The ADS131B23-Q1 integrates a second internal oscillator, called the *diagnostic oscillator (OSCD)*, which is used for various monitoring and diagnostic functions.

### 9.3.4 ADC1y

The primary purpose of the 24-bit ADC1A and ADC1B is to redundantly measure battery current across an external low-side, GND-referenced shunt resistor.

The ADC1y channel signal chain consists of two differential analog inputs (CPy, CNy), an input multiplexer followed by a programmable gain amplifier (PGA), a delta-sigma modulator and digital filter, and the global-chop and calibration logic.

#### 9.3.4.1 ADC1y Input Multiplexer

The input multiplexer controls which signals are routed to the PGA of the ADC1y channel. Configure the input multiplexer using the MUX1y[1:0] bits. The input multiplexer allows the following inputs to be connected to the PGA:

- The differential analog signal between the CPy and CNy inputs.
- The inverse differential analog signal between the CPy and CNy inputs.
- Internal short to AGNDy. The analog inputs CPy and CNy are disconnected from the PGA in this case. Use this setting for self-offset calibration of the ADC1y channel.
- DC test signal provided by the Test DAC of the other section.

Figure 9-2 shows a diagram of the ADC1A input multiplexer and Table 9-2 lists the according switch positions depending on the MUX1A[1:0] bit settings.

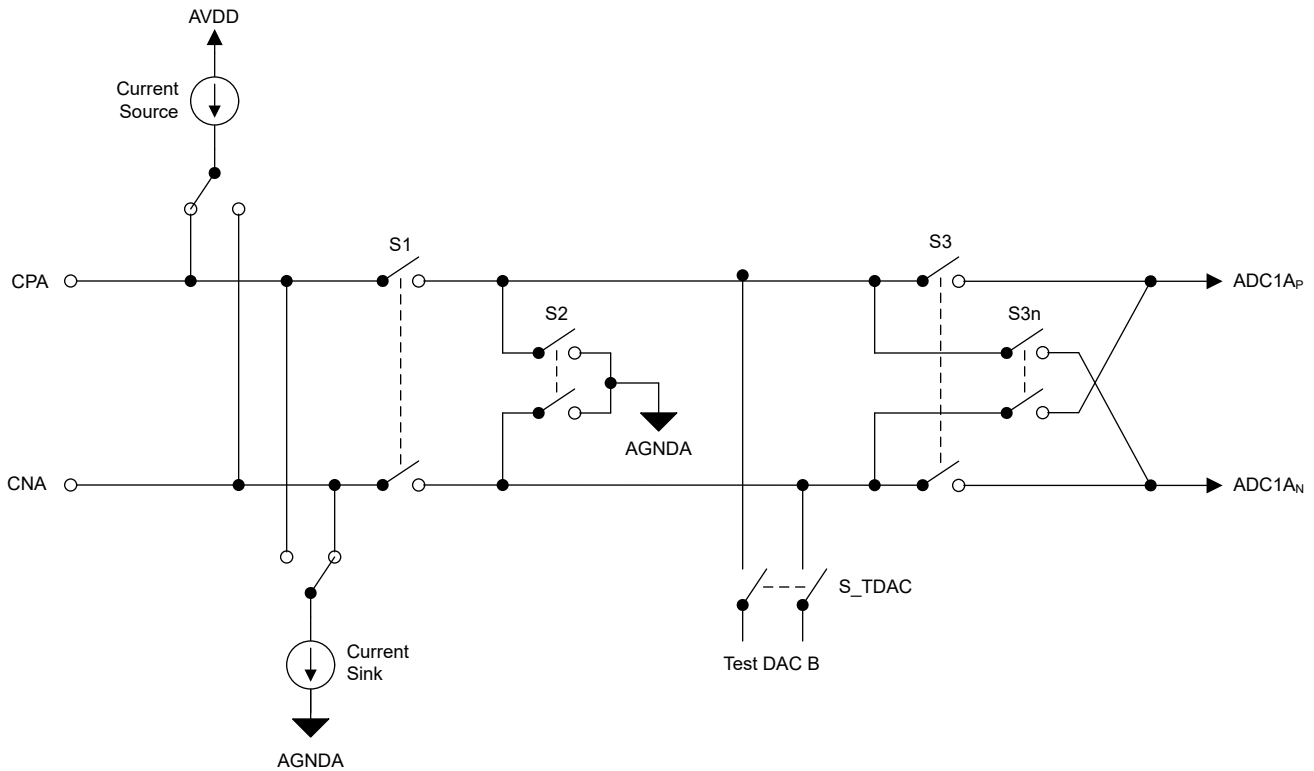


Figure 9-2. ADC1A Input Multiplexer

Table 9-2. ADC1A Multiplexer Switch Positions Based on MUX1A[1:0] Bit Settings

MUX1A[1:0] SETTING	S1	S2	S3	S3n	S_TDAC
00b	Closed	Open	Closed	Open	Open
01b	Closed	Open	Open	Closed	Open
10b	Open	Closed	Closed	Open	Open

**表 9-2. ADC1A Multiplexer Switch Positions Based on MUX1A[1:0] Bit Settings (continued)**

MUX1A[1:0] SETTING	S1	S2	S3	S3n	S_TDAC
11b	Open	Open	Closed	Open	Closed

### 9.3.4.2 ADC1y Programmable Gain Amplifier (PGA)

ADC1y features an integrated programmable gain amplifier (PGA) that provides gains of 4, 8, 16, and 32. Select the gain setting using the GAIN1y[1:0] bits.

Varying the PGA gain scales the differential full-scale input voltage range (FSR) of ADC1y. 式 4 describes the relationship between FSR and gain. 式 4 uses the internal reference voltage, 1.25 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$\text{FSR} = \pm 1.25 \text{ V} / \text{Gain} \quad (4)$$

表 9-3 shows the corresponding full-scale ranges for each gain setting.

**表 9-3. ADC1y Full-Scale Range**

GAIN SETTING	FSR
4	±312.5 mV
8	±156.25 mV
16	±78.125 mV
32	±39.063 mV

To measure bidirectional currents across a shunt resistor that is GND referenced, the PGA must accept voltages below GND. For that reason, the negative supply of the PGA is provided by an internal negative charge pump (NCPy). This provision allows the PGA to accept absolute input voltages on each input below GND.

The input impedance of the ADC1y channel is independent of the gain, OSR, and global-chop mode settings. The input impedance does, however, scale indirectly proportional with the MCLK frequency.

### 9.3.4.3 ADC1y $\Delta\Sigma$ Modulator

ADC1y uses a second-order delta-sigma ( $\Delta\Sigma$ ) modulator to convert the analog input signal to a 1's density modulated digital bit-stream. The  $\Delta\Sigma$  modulator oversamples the input signal at a frequency many times greater than the output data rate. The modulator frequency,  $f_{\text{MOD}}$ , of ADC1y is equal to half the main clock frequency (that is,  $f_{\text{MOD}} = f_{\text{MCLK}} / 2$ ).

### 9.3.4.4 ADC1y Digital Filter

The ADC1y  $\Delta\Sigma$  modulator bitstream feeds into a digital filter. The digital filter is a linear phase, finite impulse response (FIR), low-pass sinc3 filter that attenuates the out-of-band quantization noise of the  $\Delta\Sigma$  modulator. The low-resolution, high-speed modulator output is decimated and downsampled by the digital filter to produce high-resolution ADC data at an output data rate of  $f_{\text{DATA}}$ . The decimation factor, defined as per 式 5, is called the *oversampling ratio (OSR)*.

$$\text{OSR} = f_{\text{MOD}} / f_{\text{DATA}} \quad (5)$$

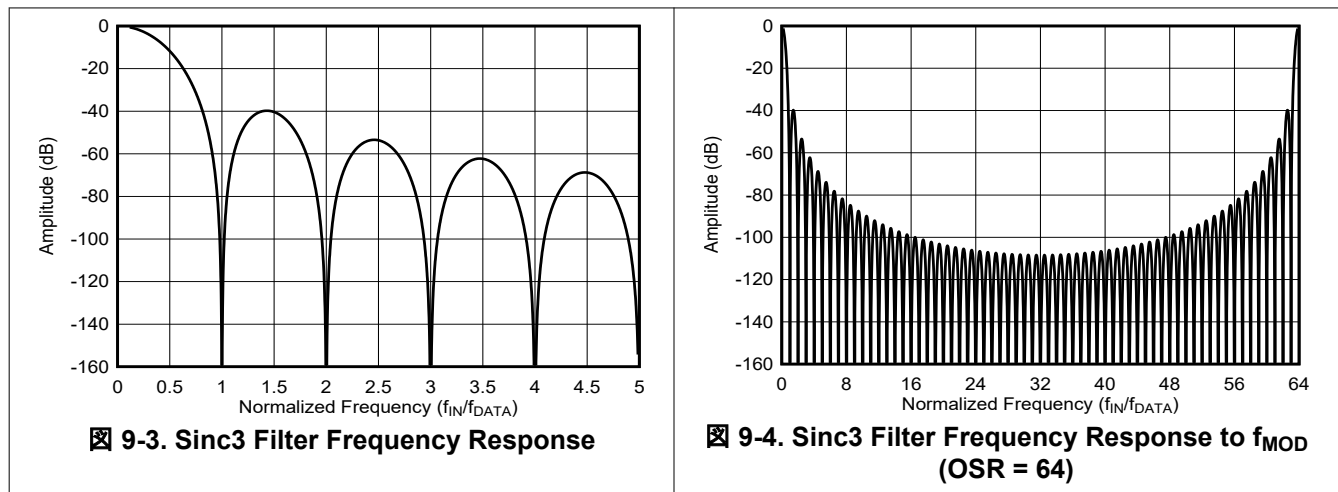
The OSR determines the amount of averaging that is applied to the modulator output in the digital filter and, therefore, the filter bandwidth and conversion noise. Higher OSRs lead to lower filter bandwidth and better noise performance.

The OSR is programmable within a range of 64 and 8192 using the OSR1y[2:0] bits. 表 9-4 lists the OSR settings for ADC1y together with the corresponding output data rates and –3-dB frequencies of the sinc3 filter for a nominal MCLK frequency of 8.192 MHz.

**表 9-4. ADC1y OSR Settings, Output Data Rates and –3-dB Frequencies for  $f_{MCLK} = 8.192$  MHz**

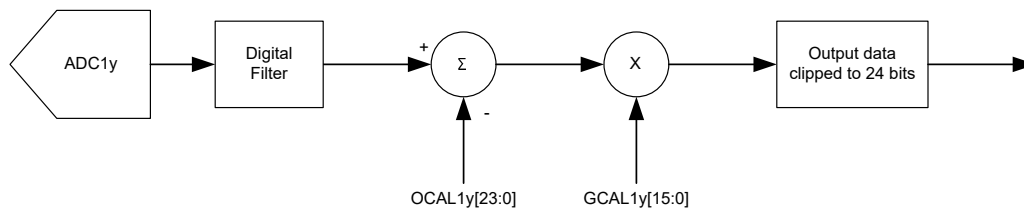
OSR	OUTPUT DATA RATE ( $f_{DATA}$ )	–3-dB FREQUENCY
64	64 kSPS	16.8 kHz
128	32 kSPS	8.4 kHz
256	16 kSPS	4.2 kHz
512	8 kSPS	2.1 kHz
1024	4 kSPS	1.0 kHz
2048	2 kSPS	524 Hz
4096	1 kSPS	262 Hz
8192	500 SPS	131 Hz

Figure 9-3 and Figure 9-4 show the filter frequency response of the sinc3 filter. The sinc3 filter has infinite attenuation at integer multiples of the output data rate except for integer multiples of  $f_{MOD}$ . As with all digital filters, the digital filter response repeats at integer multiples of the modulator frequency,  $f_{MOD}$ . The data rate and filter notch frequencies scale with  $f_{MOD}$ .



### 9.3.4.5 ADC1y Offset and Gain Calibration

ADC1y provides the ability to compute offset and gain corrected conversion data using user-programmable offset and gain correction registers. As shown in Figure 9-5, the 24-bit offset correction value (OCAL1y[23:0]) is subtracted from the conversion data before being multiplied by the 16-bit gain correction factor (GCAL1y[15:0]). Output data are rounded to the final resolution and clipped to +FS and –FS code values after the scaling operation. The offset and gain calibration coefficients must be stored in external nonvolatile memory and programmed into the offset and gain calibration registers each time the device powers up or resets because the ADS131B23-Q1 registers are volatile.



**Figure 9-5. Calibration Logic Block Diagram**

The 24-bit offset calibration value is provided in two's-complement format and programmed into the OCAL1y[23:0] bit field that spans across the ADC1y\_OCAL\_MSB and ADC1y\_OCAL\_LSB registers. 表 9-5 shows example offset calibration values. The LSB size of the offset calibration value is calculated using 式 6.

$$\text{LSB size} = (2 \times V_{\text{REFy}}) / (\text{GAIN1y} \times 2^{24}) \quad (6)$$

**表 9-5. Offset Calibration Value Examples**

OCAL1y[23:0] VALUE	APPLIED OFFSET CORRECTION
000010h	-16 LSB
000001h	-1 LSB
FFFFFFh	1 LSB
FFFFF0h	16 LSB

The 16-bit gain calibration value is provided in two's-complement format and programmed into the GCAL1y[15:0] bit field. One LSB of the gain calibration value equals a gain correction factor of  $1/2^{16} = 0.000015$ . 表 9-6 shows example gain calibration values.

**表 9-6. Gain Calibration Value Examples**

GCAL1y[15:0] VALUE	APPLIED GAIN CORRECTION
7FFFh	1.499985
0001h	1.000015
0000h	1
FFFFh	0.999985
8000h	0.5

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to OCAL1y[23:0] = 000000h and GCAL1y[15:0] = 0000h, respectively.
2. Perform an offset calibration by shorting the ADC1y inputs internally using the respective input multiplexer setting (MUX1y[1:0] = 10b), or short the inputs externally at the system level to include the offset error of the external filter stages. Acquire multiple conversion data and write the average value of the data into the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform a gain calibration by applying a precision calibration signal to the ADC1y inputs or at the system level to include the gain error of the external filter stages. Choose the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 150-mV calibration signal when using gain = 8. Acquire multiple conversion data and average the results. Use 式 7 to calculate the gain calibration value.

$$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \quad (7)$$

The expected output code for a 150-mV calibration voltage using gain = 8 is:  $(150 \text{ mV} / \text{LSB size}) = 7\text{AE}148\text{h}$ , where  $\text{LSB size} = (2 \times 1.25 \text{ V}) / (8 \times 2^{24})$ . If the actual measured output code is 6FB587h for example, then the gain calibration factor calculates to 1.1. The resulting gain calibration value to write into the GCAL1y[15:0] bit field is:  $(1.1 - 1) / (1 / 2^{16}) = 199\text{Ah}$ .

### 9.3.4.6 ADC1y Conversion Data

Conversion data for ADC1A and ADC1B are 24 bits and are automatically output on SDO as part of the SPI frame, unless register data are output following a register read command.

Data are provided in binary two's-complement format. Use 式 8 to calculate the size of one code (LSB).

$$1 \text{ LSB} = (2 \times V_{\text{REFy}} / \text{Gain}) / 2^{24} = +\text{FSR} / 2^{23} \quad (8)$$

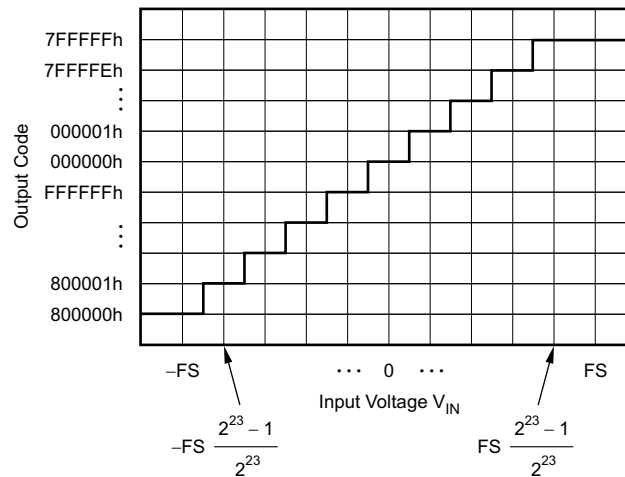
A positive full-scale input  $V_{\text{IN}} \geq +\text{FSR} - 1 \text{ LSB} = V_{\text{REFy}} / \text{Gain} - 1 \text{ LSB}$  produces an output code of 7FFFFFFh and a negative full-scale input ( $V_{\text{IN}} \leq -\text{FSR} = -V_{\text{REFy}} / \text{Gain}$ ) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

表 9-7 summarizes the ideal output codes for different input signals.

**表 9-7. Ideal Output Code versus Input Signal (24-Bit Conversion Data)**

INPUT SIGNAL ( $V_{\text{IN}} = V_{\text{AINP}} - V_{\text{AINN}}$ )	IDEAL OUTPUT CODE
$\geq \text{FSR} (2^{23} - 1) / 2^{23}$	7FFFFFFh
$\text{FSR} / 2^{23}$	000001h
0	000000h
$-\text{FSR} / 2^{23}$	FFFFFFh
$\leq -\text{FSR}$	800000h

图 9-6 shows the mapping of the analog input signal to the output codes.



**图 9-6. Code Transition Diagram (24-Bit Conversion Data)**



### 9.3.5 ADC2y

The purpose of the multiplexed, 16-bit ADC2A is to measure shunt temperature using external thermistors or analog output temperature sensors, and any other voltages that must be measured in the BMS.

The ADC2y channel signal chain consists of eight analog inputs (V0y to V7y), an input multiplexer followed by a programmable gain amplifier (PGA), a delta-sigma modulator and digital filter, calibration logic, and a channel sequencer.

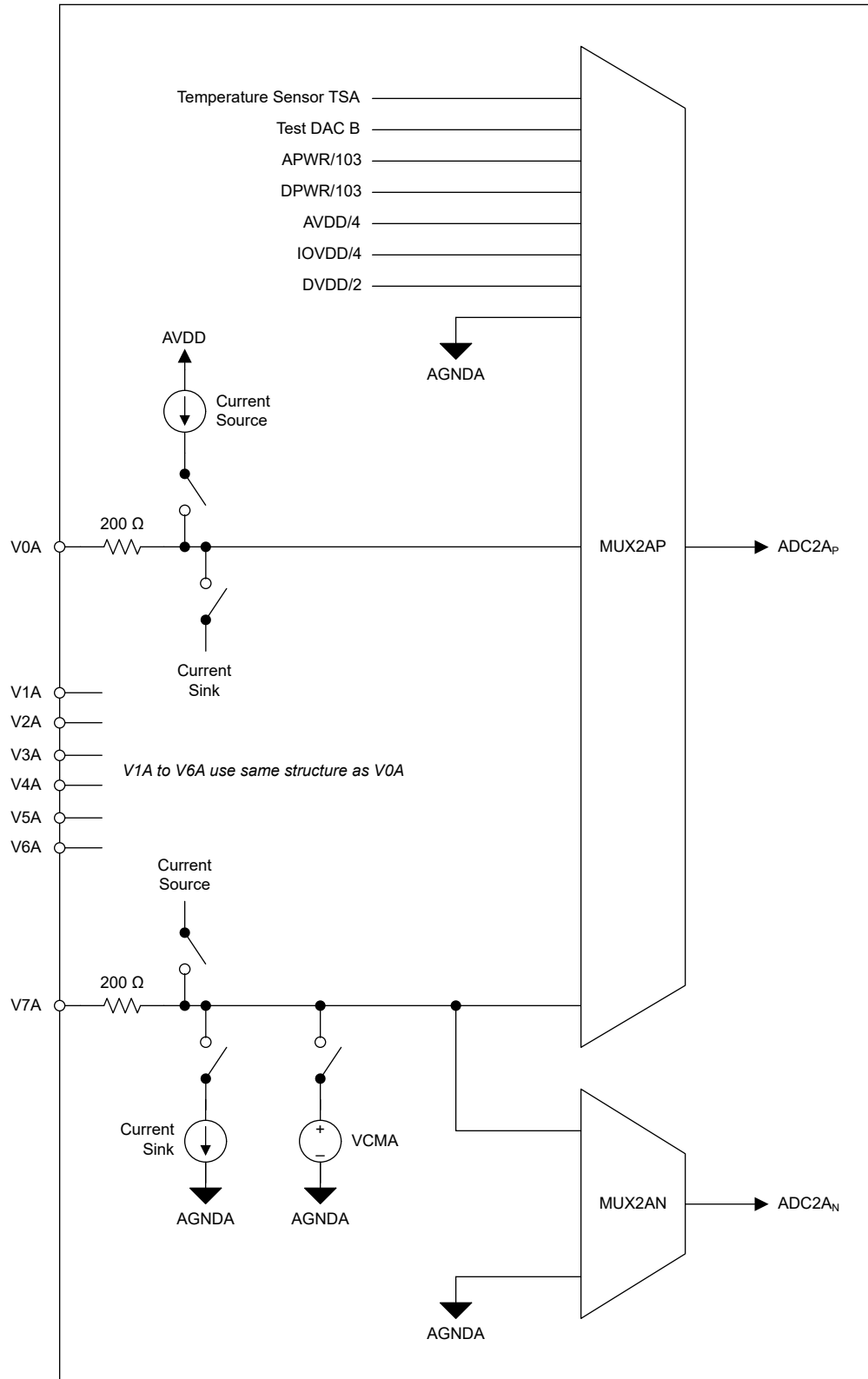
#### 9.3.5.1 ADC2y Input Multiplexer

The input multiplexer controls which signals are routed to the positive and negative PGA inputs of the ADC2y channel in each sequence step. Configure the input multiplexer using the SEQ2y\_STEPn\_CH\_P[3:0] and SEQ2y\_STEPn\_CH\_N bits.

The input multiplexer allows the following inputs to be connected to the PGA:

- Any of the eight analog inputs, V0y to V7y, in single-ended measurement configuration when AGNDy is selected as the negative multiplexer channel.
- Any of the seven analog inputs, V0y to V6y, in single-ended measurement configuration when V7y is selected as the negative multiplexer channel and connected to AGNDy externally.
- Any of the seven analog inputs, V0y to V6y, in pseudo-differential measurement configuration when V7y is selected as the negative multiplexer channel. Connect a positive bias voltage to V7y in this case, either using an external bias voltage or the internal common-mode voltage of the VCM<sub>y</sub> buffer.
- Internal temperature sensor, TS<sub>y</sub>.
- Internal short to AGNDy. Use this setting for self-offset calibration of the ADC2y channel.
- DC test signal provided by the Test DAC of the other section.
- Attenuated signals of the various supply voltages (APWR, DPWR, AVDD, IOVDD, and DVDD).

Whenever a signal other than an analog input is selected as the positive multiplexer input, the analog inputs are disconnected from the PGA and AGNDy is selected automatically as the negative multiplexer input. [☒ 9-7](#) illustrates a diagram of the ADC2A input multiplexer.



**图 9-7. ADC2A Input Multiplexer**

### 9.3.5.2 ADC2y Programmable Gain Amplifier (PGA)

ADC2y features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, and 4. Select the gain setting using the SEQ2y\_STEPn\_GAIN[1:0] bits.

Varying the PGA gain scales the differential full-scale input voltage range (FSR) of ADC2y. 式 9 describes the relationship between FSR and gain. 式 9 uses the internal reference voltage, 1.25 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$\text{FSR} = \pm 1.25 \text{ V} / \text{Gain} \quad (9)$$

表 9-8 shows the corresponding full-scale ranges for each gain setting.

**表 9-8. ADC2y Full-Scale Range**

GAIN SETTING	FSR
1	±1.25 V
2	±625 mV
4	±312.5 mV

When performing single-ended measurements (that is, AGNDy is selected as the negative multiplexer channel for ADC2y), gain settings of 1 and 2 only allow for unipolar measurements, whereas gain setting of 4 allows for both unipolar and bipolar input voltage measurements. See the absolute input voltage range specification of ADC2y in the [Recommended Operating Conditions](#) table for details and the [ADC2y Measurement Configurations](#) section for example input configurations. Unipolar measurements only use the positive code range from approximately 0000h to 7FFFh, which maps to an input voltage range from approximately 0 V to +FS.

The input impedance of the ADC2y channel depends on two factors: the main clock frequency ( $f_{\text{MCLK}}$ ) and the selected OSR setting. The [Electrical Characteristics](#) table lists typical input impedance values for  $f_{\text{MCLK}} = 8.192 \text{ MHz}$  at the various OSR settings. Increasing the OSR by twice the value effectively doubles the input impedance. The input impedance scales indirectly proportional with the MCLK frequency.

### 9.3.5.3 ADC2y $\Delta\Sigma$ Modulator

ADC2y uses a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator to convert the analog input signal to a 1's density modulated digital bitstream. The  $\Delta\Sigma$  modulator oversamples the input signal at a frequency many times greater than the output data rate. The modulator frequency,  $f_{\text{MOD}}$ , of ADC2y is equal to half the main clock frequency (that is,  $f_{\text{MOD}} = f_{\text{MCLK}} / 2$ ).

### 9.3.5.4 ADC2y Digital Filter

The ADC2y  $\Delta\Sigma$  modulator bitstream feeds into a digital filter. The digital filter is a linear phase, finite impulse response (FIR), low-pass sinc filter that attenuates the out-of-band quantization noise of the  $\Delta\Sigma$  modulator.

In contrast to ADC1y, ADC2y always operates in a single-shot conversion mode fashion. The ADC2y sequencer triggers the individual conversions. The digital filter resets at the start of every conversion and must completely settle for every conversion. ADC2y only outputs settled conversion results, assuming that the input signal settled before the conversion started.

Use the OSR2y[1:0] bits to select the conversion time for ADC2y. For an OSR = 64, the filter is comprised of a pure sinc3 filter. A sinc3 filter takes three cycles to settle. Therefore, the conversion time for an OSR = 64 equals ( $3 \times 64 / f_{\text{MOD}} = 192 t_{\text{MOD}} = 384 t_{\text{MCLK}}$ ). For higher OSR settings the sinc3 filter is followed by a sinc1 filter.

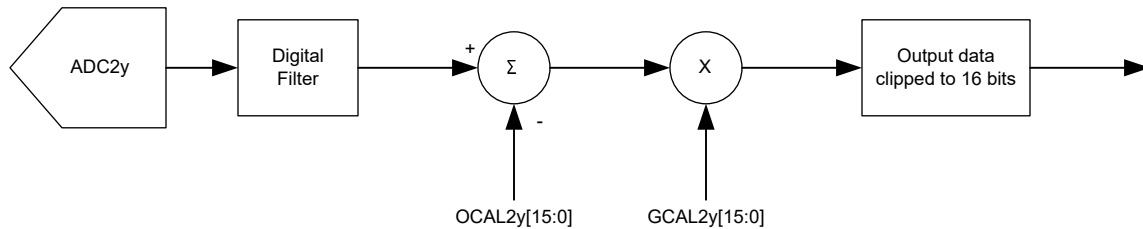
表 9-9 lists an overview of the OSR settings and the corresponding conversion times for ADC2y based on a nominal MCLK frequency of 8.192 MHz.

**表 9-9. ADC2y OSR Settings and Conversion Times for  $f_{MCLK} = 8.192 \text{ MHz}$**

OSR			CONVERSION TIME	
OVERALL	SINC3	SINC1	$t_{MCLK}$	$\mu\text{s}$
64	64	1	$384 t_{MCLK}$	46.87 $\mu\text{s}$
128	64	2	$512 t_{MCLK}$	62.50 $\mu\text{s}$
256	64	4	$768 t_{MCLK}$	93.75 $\mu\text{s}$
512	64	8	$1280 t_{MCLK}$	156.25 $\mu\text{s}$

**9.3.5.5 ADC2y Offset and Gain Calibration**

ADC2y provides the ability to compute offset and gain corrected conversion data using user-programmable offset and gain correction registers. The same calibration values are used for all sequence steps, however, the offset and gain correction factors are not applied when the internal temperature sensor is selected for measurement by MUX2y. As shown in [图 9-8](#), the 16-bit offset correction value (OCAL2y[15:0]) is subtracted from the conversion data before being multiplied by the 16-bit gain correction factor (GCAL2y[15:0]). Output data are rounded to the final resolution and clipped to +FS and -FS code values after the scaling operation. The offset and gain calibration coefficients must be stored in external nonvolatile memory and programmed into the offset and gain calibration registers each time the device powers up or resets because the ADS131B23-Q1 registers are volatile.



**图 9-8. Calibration Logic Block Diagram**

The 16-bit offset calibration value is provided in two's-complement format and programmed into the OCAL2y[15:0] bit field. [表 9-10](#) shows example offset calibration values. The LSB size of the offset calibration value is calculated using [式 10](#) and [式 11](#) depending on the selected gain setting.

$$\text{GAIN2y} = 1: \text{LSB size} = V_{REFy} / 2^{15} \tag{10}$$

$$\text{GAIN2y} = 2 \text{ or } 4: \text{LSB size} = V_{REFy} / (2 \times 2^{15}) \tag{11}$$

**表 9-10. Offset Calibration Value Examples**

OCAL2y[15:0] VALUE	APPLIED OFFSET CORRECTION
0010h	-16 LSB
0001h	-1 LSB
FFFFh	1 LSB
FFF0h	16 LSB

The 16-bit gain calibration value is provided in two's-complement format and programmed into the GCAL2y[15:0] bit field. One LSB of the gain calibration value equals a gain correction factor of  $1/2^{16} = 0.000015$ . [表 9-11](#) shows example gain calibration values.

**表 9-11. Gain Calibration Value Examples**

GCAL2y[15:0] VALUE	APPLIED GAIN CORRECTION
7FFFh	1.499985
0001h	1.000015
0000h	1
FFFFh	0.999985

表 9-11. Gain Calibration Value Examples  
(continued)

GCAL2y[15:0] VALUE	APPLIED GAIN CORRECTION
8000h	0.5

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to  $OCAL2y[15:0] = 0000h$  and  $GCAL2y[15:0] = 0000h$ , respectively.
2. Perform an offset calibration by shorting the ADC2y input in one or multiple sequence steps internally to AGNDy using the respective input multiplexer setting ( $SEQ2y\_STEPn\_CH\_P[3:0] = 1001b$ ), or short one of the ADC2y inputs externally at the system level to include the offset error of the external filter stages. Set the gain for the respective sequence step to 1 or 2. Acquire multiple conversion data and write the average value of the data into the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform a gain calibration by applying a precision calibration signal to one of the ADC2y inputs or at the system level to include the gain error of the external filter stages. Choose the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 1.2-V calibration signal when using gain = 1. Acquire multiple conversion data and average the results. Use 式 12 to calculate the gain calibration value.

$$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \quad (12)$$

The expected output code for a 1.2-V calibration voltage using gain = 1 is:  $(1.2 \text{ V} / \text{LSB size}) = 7AE1h$ , where  $\text{LSB size} = (1.25 \text{ V} / 2^{15})$ . If the actual measured output code is 6FB6h for example, then the gain calibration factor calculates to 1.1. The resulting gain calibration value to write into the GCAL2y[15:0] bit field is:  $(1.1 - 1) / (1 / 2^{16}) = 199Ah$ .

### 9.3.5.6 ADC2y Sequencer

See the [ADC2y Sequencer Operation and Sequence Modes](#) section for details.

### 9.3.5.7 VCM My Buffers

The ADC2y signal chain includes a bias voltage generator of typically 0.78 V followed by a common-mode buffer, VCM My. When the VCM My\_EN bit is set, the output of the VCM My buffer is internally connected to the V7y multiplexer channel to provide the bias voltage to V7y. Use the VCM My buffer to implement pseudo-differential measurements, where V7y is selected as the negative multiplexer channel of ADC2y.

When the VCM My buffer is enabled, the capacitive load from V7y to AGNDy must be limited to less than 100 pF.

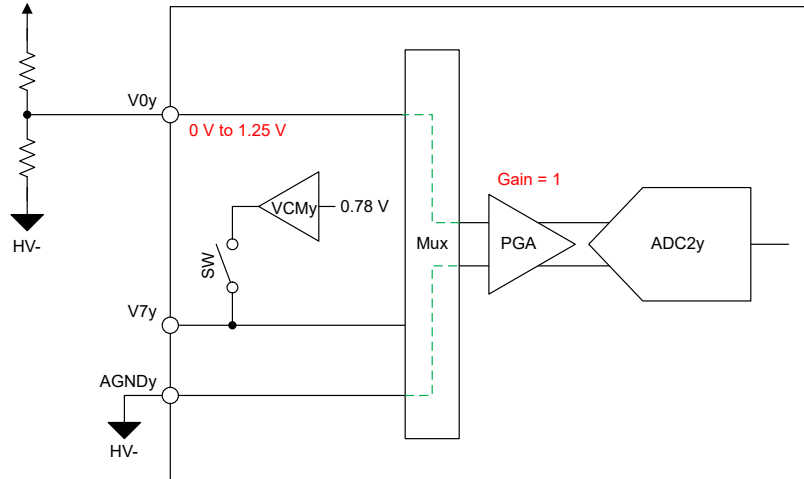
### 9.3.5.8 ADC2y Measurement Configurations

ADC2y allows measurements of input voltages in three different configurations, as summarized in [表 9-12](#), [图 9-9](#), [图 9-10](#), and [图 9-11](#).

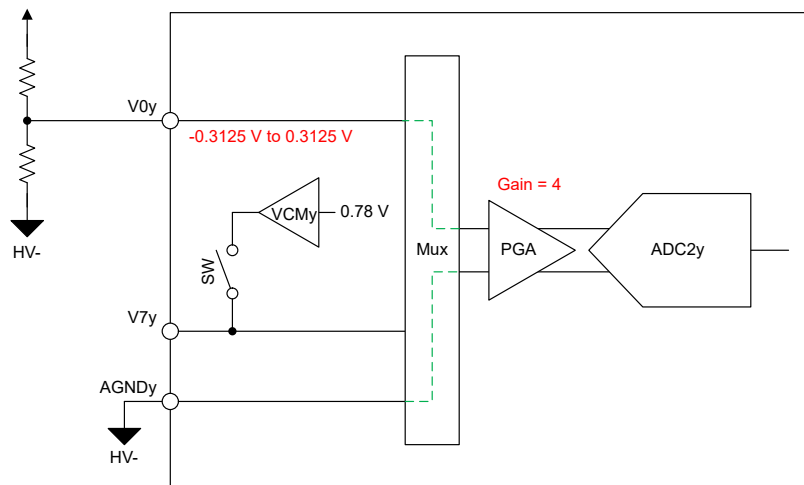
表 9-12. Overview of Possible Measurement Configurations for ADC2y

INPUT CONFIGURATION	POSITIVE MUX CHANNEL	NEGATIVE MUX CHANNEL	GAIN	INPUT RANGE	ABSOLUTE INPUT VOLTAGE	FIGURE
Single-ended	V0y to V7y	AGNDy	1, 2, or 4	Unipolar	0 V to +FS = $V_{REFy} / \text{Gain}$	<a href="#">图 9-9</a>
Single-ended	V0y to V7y	AGNDy	4	Bipolar	-0.3125 V to 0.3125 V	<a href="#">图 9-10</a>
Pseudo-differential	V0y to V6y	V7y	1, 2, or 4	Bipolar	$V_{V7y} \pm FS^{(1)}$	<a href="#">图 9-11</a>

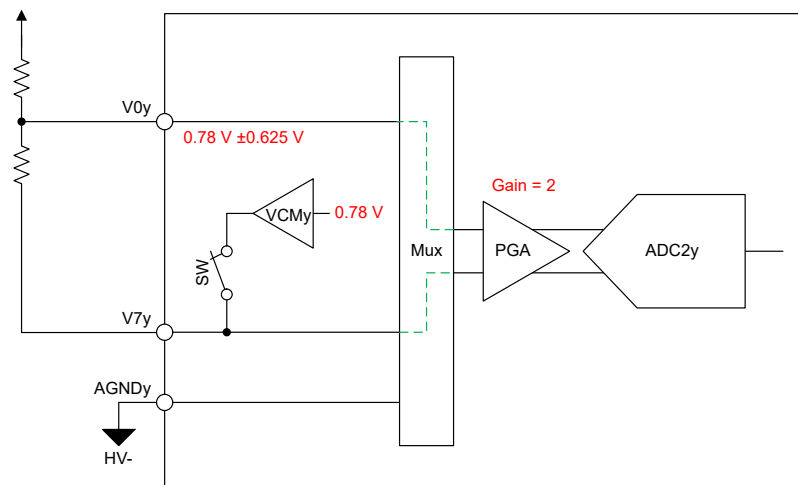
(1) Actual input range limited by absolute input voltage range specification in the [Recommended Operating Conditions](#) table.



☒ 9-9. Single-Ended Input, Unipolar Voltage Measurement (Gain = 1)



☒ 9-10. Single-Ended Input, Bipolar Voltage Measurement (Gain = 4)



☒ 9-11. Pseudo-Differential Input, Bipolar Voltage Measurement (Gain = 2, Using Internal Bias Voltage)

### 9.3.5.9 ADC2y Conversion Data

Conversion data for the sequence steps of ADC2y are 16 bits and (in contrast to ADC1y conversion data) stored in the user register space (register addresses 10h to 1Fh). Read ADC2y conversion data using the register read command.

Data are provided in binary two's-complement format. Use 式 13 to calculate the size of one code (LSB).

$$1 \text{ LSB} = (2 \times V_{\text{REFy}} / \text{Gain}) / 2^{16} = +\text{FSR} / 2^{15} \quad (13)$$

A positive full-scale input  $V_{\text{IN}} \geq +\text{FSR} - 1 \text{ LSB} = V_{\text{REFy}} / \text{Gain} - 1 \text{ LSB}$  produces an output code of 7FFFh and a negative full-scale input ( $V_{\text{IN}} \leq -\text{FSR} = -V_{\text{REFy}} / \text{Gain}$ ) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

表 9-13 summarizes the ideal output codes for different input signals.

表 9-13. Ideal Output Code versus Input Signal (16-Bit Conversion Data)

INPUT SIGNAL ( $V_{\text{IN}} = V_{\text{AINP}} - V_{\text{AINN}}$ )	IDEAL OUTPUT CODE
$\geq \text{FSR} (2^{15} - 1) / 2^{15}$	7FFFh
$\text{FSR} / 2^{15}$	0001h
0	0000h
$-\text{FSR} / 2^{15}$	FFFFh
$\leq -\text{FSR}$	8000h

图 9-12 shows the mapping of the analog input signal to the output codes.

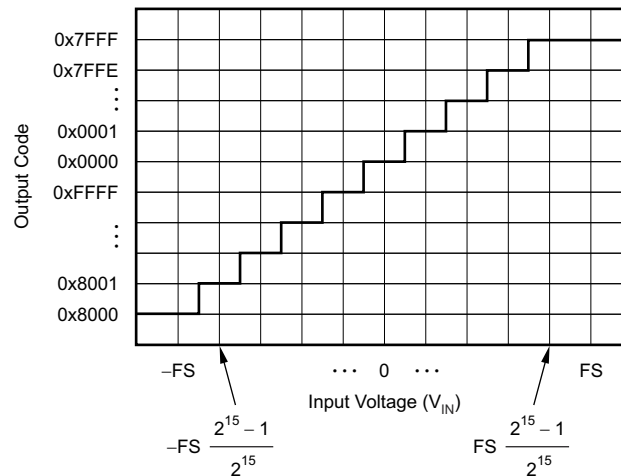


图 9-12. Code Transition Diagram (16-Bit Conversion Data)

### 9.3.6 General-Purpose Digital Inputs and Outputs (GPIO0 to GPIO4)

The ADS131B23-Q1 offers five GPIO pins (GPIO0 to GPIO4) that use logic levels based on the IOVDD supply. See the [Electrical Characteristics](#) table for details regarding the logic high and low levels. The GPIOs offer a multitude of configuration options:

- Configure the individual GPIOs as either digital inputs or digital outputs using the respective GPIOx\_DIR bits (x = 0, 1, 2, 3, or 4).
- Configure the input and output format of the individual GPIOs as either static logic levels or PWM using the respective GPIOx\_FMT bits. See the [GPIOx PWM Output Configuration](#) section for details on how to configure the PWM period and duty cycle for a specific GPIO.
- Four of the GPIO pins can be configured with a special output function (FAULT, MHD, OCCA, and OCCB) using the respective GPIOx\_SRC bits. Configure GPIOx as a digital output using the GPIOx\_DIR bit when selecting the special output function for GPIOx.

Use the GPOx\_DAT bit to drive a logic high or low level on the respective GPIO pin when GPIOx is configured as a digital output. The GPIO outputs are push-pull. GPIOx ignores the value written to the GPOx\_DAT bit when configured for a special output function.

The device always reads back the value of the GPIOs and provides the detected logic level in the GPIx\_DAT[1:0] bit fields, no matter if GPIOx is configured as digital input or output. See the GPIx\_DAT[1:0] bit field descriptions for details on how the device decodes PWM signals.

The GPIOs are configured as inputs when the device is held in reset.

#### 9.3.6.1 GPIOx PWM Output Configuration

When GPIOx is configured for PWM format using the GPIOx\_FMT bit, the PWM period and duty cycle can be independently configured for a logic high and low level with fine granularity. The GPIOx\_LL\_PWM\_LC[6:0] (GPIOx logic low level PWM low counter value) and GPIOx\_LL\_PWM\_HC[6:0] (GPIOx logic low level PWM high counter value) bits together with the GPIOx\_PWM\_TB[1:0] (GPIOx PWM time base) bits determine the PWM period and duty cycle when a logic low level is driven as per the GPOx\_DAT bit. Similarly, the GPIOx\_LH\_PWM\_LC[6:0] (GPIOx logic high level PWM low counter value) and GPIOx\_LH\_PWM\_HC[6:0] (GPIOx logic high level PWM high counter value) bits together with the GPIOx\_PWM\_TB[1:0] bits determine the PWM period and duty cycle when a logic high level is driven as per the GPOx\_DAT bit.


The following equations specify the PWM period and duty cycle:

$$\text{PWM period} = (\text{PWM high counter value} + \text{PWM low counter value}) \times \text{PWM time base} \quad (14)$$

$$\text{PWM low time} = (\text{PWM low counter value} \times \text{PWM time base}) \quad (15)$$

$$\text{PWM high time} = (\text{PWM high counter value} \times \text{PWM time base}) \quad (16)$$

$$\text{PWM duty cycle} = \text{PWM high time} / (\text{PWM high time} + \text{PWM low time}) \quad (17)$$

 **9-13** depicts a visual representation of how the various configuration values produce a certain PWM output. The PWM period always starts with the PWM low time. Changes to the PWM period and duty cycle based on the GPOx\_DAT bit only take effect at the start of a new PWM period.

**表 9-14** provides example configuration values for GPIO1 where the logic high level is configured for 75% duty cycle using a 1-ms period and the logic low level for a 25% duty cycle using the same 1-ms period. The PWM time base is chosen as  $8.192 \text{ MHz} / 1024 = 125 \mu\text{s}$ , assuming an  $f_{\text{MCLK}} = 8.192 \text{ MHz}$  is used. The sum of the high and low counter must be eight in this case to yield a PWM period of  $8 \times 125 \mu\text{s} = 1 \text{ ms}$ . Changing the GPIO1\_LL\_PWM\_LC[6:0] = 3Ch = 60 and the GPIO1\_LL\_PWM\_HC[6:0] = 14h = 20 (for example) results in the same 25% duty cycle, but at a PWM period of  $80 \times 125 \mu\text{s} = 10 \text{ ms}$ .



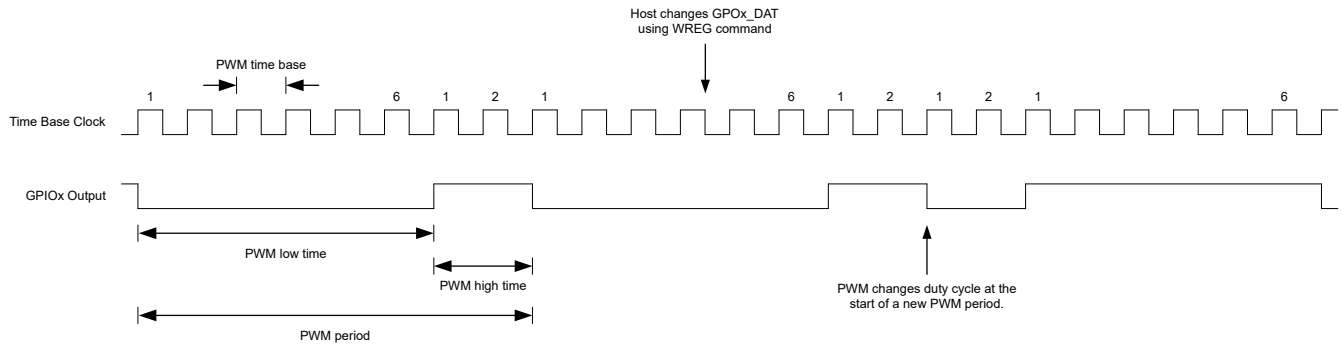


図 9-13. GPIOx PWM Output Timing Diagram

表 9-14. GPIO1 PWM Configuration Example

BIT FIELD	BIT FIELD SETTING	VALUE	CORRESPONDING TIME (BASED ON $f_{MCLK} = 8.192 \text{ MHz}$ )
GPIO1_PWM_TB[1:0]	3h	$1024 \times t_{MCLK}$	125 $\mu\text{s}$
GPIO1_LL_PWM_LC[6:0]	06h	6	750 $\mu\text{s}$
GPIO1_LL_PWM_HC[6:0]	02h	2	250 $\mu\text{s}$
GPIO1_LH_PWM_LC[6:0]	02h	2	250 $\mu\text{s}$
GPIO1_LH_PWM_HC[6:0]	06h	6	750 $\mu\text{s}$

### 9.3.6.2 GPIOx PWM Input Readback

For GPIOx to decode PWM input signals, configure the GPIOx\_FMT bit for PWM decoding. GPIOx uses the time base configured in the GPIOx\_PWM\_TB[1:0] bits for PWM decoding. The decoded input value is provided in the GPIx\_DAT[1:0] bit field. The GPIOs decode PWM signals with four different levels as specified in the GPI\_DAT[1:0] bit field description.

The GPIx\_DAT[1:0] bits need up to two PWM cycles to indicate the correct logic level after the PWM period or duty cycle applied to GPIOx changed.

### 9.3.7 General-Purpose Digital Inputs and Outputs (GPIO0A, GPIO1A, GPIO0B, GPIO1B)

The ADS131B23-Q1 offers four additional GPIO pins (GPIO0A, GPIO1A, GPIO0B, and GPIO1B) that use logic levels based on the AVDD supply. See the [Electrical Characteristics](#) table for details regarding the logic high and low levels. The GPIOs offer a multitude of configuration options:

- Configure the individual GPIOs as either digital inputs or digital outputs using the respective GPIOxy\_DIR bits ( $x = 0$  or  $1$ ,  $y = A$  or  $B$ ).
- Configure the input format of the individual GPIOs for either static logic level or PWM inputs using the respective GPIOxy\_FMT bits. In contrast to GPIO0 to GPIO4, the GPIOxy do not offer PWM output capability. Select the appropriate PWM timebase for each GPIO PWM decoder using the GPIOxy\_PWM\_TB[1:0] bits. The timebase of the source driving the GPIOxy input must be equal to or slower than the timebase of the GPIOxy input decoder, otherwise the logic levels are not correctly decoded. GPIOxy always uses static logic levels when configured as a digital output.

Use the GPOxy\_DAT bit to drive a logic high or low level on the respective GPIO pin when GPIOxy is configured as a digital output. The GPIO outputs are push-pull.

The device always reads back the value of the GPIOs and provides the detected logic level in the GPIxy\_DAT[1:0] bit fields, regardless if GPIOxy is configured as a digital input or output. See the GPIxy\_DAT[1:0] bit field descriptions for details on how the device decodes PWM signals.

### 9.3.8 Monitors and Diagnostics

The ADS131B23-Q1 integrates many monitor and diagnostic circuits to aid in the design of functional safety systems. *Monitors* detect faults in the device, such as a supply undervoltage condition, whereas *diagnostics* detect faults within the monitoring circuit to check if the monitor is still working as intended.

表 9-15 provides an overview of all available monitors and diagnostics. Most monitors can be enabled or disabled as required using a dedicated monitor enable bit. If a monitor detects a fault, the according low-active fault flag is set to 0b. Except for the communication-related monitor fault flags, the fault flags must be cleared to 1b by the host after the fault condition is removed. The communication-related monitor fault flags reset to 1b automatically in the SPI frame following a frame where no communication fault occurred.

The monitors that have a dedicated diagnostic circuit to check the integrity of the monitor show the respective diagnostic enable bit in 表 9-15. Monitors that do not show a dedicated diagnostic enable bit are diagnosed through other means, as explained in the Safety Manual.

The monitors have individual fault response times, which is the time from fault occurrence to fault flag indication, as specified in the [Electrical Characteristics](#) table.

**表 9-15. Monitor and Diagnostic Overview**

MONITOR NAME	MONITOR ENABLE BIT	MONITOR FAULT FLAG	DIAGNOSTIC ENABLE BIT	FAULT FLAG REGISTER LOCATION
<b>SUPPLY MONITORS AND DIAGNOSTICS</b>				
Reset	N/A	RESETn	See Safety Manual	STATUS_MSB
AVDD overvoltage	AVDD_OV_EN	AVDD_OVn	AVDD_OV_DIAG_EN	SUPPLY_STATUS
AVDD undervoltage	AVDD_UV_EN	AVDD_UVn	AVDD_UV_DIAG_EN	SUPPLY_STATUS
IOVDD overvoltage	IOVDD_OV_EN	IOVDD_OVn	IOVDD_OV_DIAG_EN	SUPPLY_STATUS
IOVDD undervoltage	IOVDD_UV_EN	IOVDD_UVn	IOVDD_UV_DIAG_EN	SUPPLY_STATUS
DVDD overvoltage	DVDD_OV_EN	DVDD_OVn	DVDD_OV_DIAG_EN	SUPPLY_STATUS
DVDD undervoltage	DVDD_UV_EN	DVDD_UVn	DVDD_UV_DIAG_EN	SUPPLY_STATUS
AVDD oscillation	AVDD_OSC_EN	AVDD_OSCn	AVDD_OSC_DIAG_EN	SUPPLY_STATUS
IOVDD oscillation	IOVDD_OSC_EN	IOVDD_OSCn	IOVDD_OSC_DIAG_EN	SUPPLY_STATUS
DVDD oscillation	DVDD_OSC_EN	DVDD_OSCn	DVDD_OSC_DIAG_EN	SUPPLY_STATUS
AVDD LDO overtemperature warning	AVDD_OTW_EN	AVDD_OTWn	See Safety Manual	SUPPLY_STATUS
IOVDD LDO overtemperature warning	IOVDD_OTW_EN	IOVDD_OTWn	See Safety Manual	SUPPLY_STATUS
AVDD LDO output current limit	AVDD_CL_EN	AVDD_CLn	N/A	SUPPLY_STATUS
IOVDD LDO output current limit	IOVDD_CL_EN	IOVDD_CLn	N/A	SUPPLY_STATUS
AGNDA pin disconnect	AGNDA_DISC_EN	AGNDA_DISCn	AGNDA_DISC_DIAG_EN	SUPPLY_STATUS
AGNDB pin disconnect	AGNDB_DISC_EN	AGNDB_DISCn	AGNDB_DISC_DIAG_EN	SUPPLY_STATUS
DGND pin disconnect	DGND_DISC_EN	DGND_DISCn	DGND_DISC_DIAG_EN	SUPPLY_STATUS
<b>CLOCK MONITORS AND DIAGNOSTICS</b>				
Main clock frequency	MCLK_MON_EN	MCLK_FAULTn	MCLK_HI_DIAG_EN, MCLK_LO_DIAG_EN	CLOCK_STATUS
Diagnostic oscillator watchdog	OSCD_WD_EN	OSCD_WDn	OSCD_WD_DIAG_EN	CLOCK_STATUS
Main clock watchdog	MCLK_WD_EN	MCLK_WDn	MCLK_WD_DIAG_EN	CLOCK_STATUS

**表 9-15. Monitor and Diagnostic Overview (continued)**

MONITOR NAME	MONITOR ENABLE BIT	MONITOR FAULT FLAG	DIAGNOSTIC ENABLE BIT	FAULT FLAG REGISTER LOCATION
<b>DIGITAL MONITORS AND DIAGNOSTICS</b>				
Register map section 1 CRC	REG_MAP1_CRC_EN	REG_MAP1_CRC_FAULT <sub>n</sub>	See Safety Manual	DIGITAL_STATUS
Register map section 2 CRC	REG_MAP2_CRC_EN	REG_MAP2_CRC_FAULT <sub>n</sub>	See Safety Manual	DIGITAL_STATUS
Register map section 3 CRC	REG_MAP3_CRC_EN	REG_MAP3_CRC_FAULT <sub>n</sub>	See Safety Manual	DIGITAL_STATUS
Memory map CRC	N/A	MEM_MAP_CRC_FAULT <sub>n</sub>	MEM_MAP_CRC_DIAG[1:0]	DIGITAL_STATUS
GPIOA readback	N/A	N/A	GPIOA_DIAG_EN	GPIA_GPIB_DATA
GPIOB readback	N/A	N/A	GPIOB_DIAG_EN	GPIA_GPIB_DATA
GPIO readback	N/A	N/A	GPIO_DIAG_EN	GPI_DATA
<b>COMMUNICATION MONITORS AND DIAGNOSTICS</b>				
SPI CRC	N/A	SPI_CRC_FAULT <sub>n</sub>	See Safety Manual	STATUS_MSB
SPI timeout	TIMEOUT_EN	SPI_TIMEOUT <sub>n</sub>	See Safety Manual	STATUS_MSB
SCLK counter	SCLK_COUNTER_EN	SCLK_COUNT_FAULT <sub>n</sub>	See Safety Manual	STATUS_MSB
Register access	N/A	REG_ACCESS_FAULT <sub>n</sub>	See Safety Manual	STATUS_MSB

In addition to the monitors that detect faults in the device, the ADS131B23-Q1 also provides the indicators shown in [表 9-16](#), which provide feedback about the device state or behavior.

**表 9-16. Indicator Overview**

INDICATOR NAME	INDICATOR STATUS BIT	STATUS BIT REGISTER LOCATION
Command response	COMMAND_RESPONSE[3:0]	STATUS_MSB
Lock state	LOCK	STATUS_MSB
Clock source	CLOCK	STATUS_MSB
Operating mode	MODE	STATUS_MSB
ADC2A sequence active	SEQ2A_ACTIVE	STATUS_LSB
OTP bank	OTB_BANK	DIGITAL_STATUS

Lastly, the device provides the conversion and sequence counters shown in [表 9-17](#) for the individual ADCs.

**表 9-17. Conversion and Sequence Counter Overview**

COUNTER NAME	COUNTER BITS	COUNTER BITS REGISTER LOCATION
ADC1A conversion counter	CONV1A_COUNT[1:0]	STATUS_LSB
ADC1B conversion counter	CONV1B_COUNT[1:0]	STATUS_LSB
ADC2A sequencer counter	SEQ2A_COUNT[1:0]	STATUS_LSB

Besides the monitors, indicators, and counters mentioned in the previous tables, the ADS131B23-Q1 offers additional means to check the integrity of the device, such as:

- Power-supply voltage readback using ADC2A
- A temperature sensor, TSA
- Two test DACs, TDACA and TDACB
- Open-wire detection current sources and sinks on every ADC

### 9.3.8.1 Supply Monitors

Individual power-on reset (POR) circuits are implemented on the AVDD, IOVDD, and DVDD supplies. If any of the three supplies drop below the respective POR threshold, the device is held in reset.

The ADS131B23-Q1 monitors the outputs of the three internal LDOs (AVDD, IOVDD, and DVDD) for overvoltage (OV), undervoltage (UV), and oscillations. See the [Electrical Characteristics](#) table for the according monitor detection thresholds. If an OV event occurs, the respective LDO shuts down to prevent damage to the internal circuitry. The LDO turns back on after the output voltage drops below the OV threshold. The device can potentially reset if the supply voltage drops below the POR threshold before the LDO is turned on again. The LDOs do not shut down when an OV diagnostic is performed.

AVDD or IOVDD can be supplied externally when shorting APWR to AVDD or DPWR to IOVDD, respectively, thus bypassing the internal LDOs. The monitors check the externally provided supply when bypassing the internal LDO. Configure the IOVDD OV and UV monitor thresholds using the IOVDD\_OV\_TH and IOVDD\_UV\_TH bits based on the used IOVDD supply.

The AVDD and IOVDD LDOs integrate individual temperature sensors to indicate potential overtemperature events. Configure the overtemperature warning thresholds using the AVDD\_OTW\_CFG[1:0] and IOVDD\_OTW\_CFG[1:0] bits.

The AGNDA, AGNDB, and DGND pins are monitored for pin disconnections. The AGND pin is implemented redundantly and therefore does not provide a pin disconnection monitor.

The AVDD and IOVDD LDOs are designed with an output current limit to prevent excessive current draw from the LDOs. When the LDOs operate in current limit, the according fault flags are set. If more current draw is demanded from the LDOs than the current limit, then the LDO output voltage typically drops below the POR threshold and causes a POR event.

### 9.3.8.2 Clock Monitors

The ADS131B23-Q1 integrates a diagnostic oscillator (OSCD) to monitor the frequency of the selected main clock (MCLK), which is either sourced from the internal main oscillator (OSCM) or from an external clock provided at the CLK pin. The MCLK\_FAULTn flag is set to 0b when the frequencies between the main clock and the diagnostic oscillator deviate by more than the main clock fault detection frequency threshold (MCLK\_FAULT\_TH).

Additionally, individual watchdogs (MCLK\_WD and OSCD\_WD) monitor the main clock and the diagnostic oscillator to detect a missing clock signal. The MCLK\_WDn flag is set to 0b when the MCLK frequency drops below  $f_{MCLK\_WD\_TH}$ , and the OSCD\_WDn flag is set to 0b when the OSCD frequency drops below  $f_{OSCD\_WD\_TH}$ .

### 9.3.8.3 Digital Monitors

The following sections explain the available digital monitors, such as register map CRC, memory map CRC, and GPIO readback functionality.

#### 9.3.8.3.1 Register Map CRC

Register map CRCs in the ADS131B23-Q1 detect unintended changes in the register map contents. The register map is divided into four sections.

Section 0 includes read-only bits that update the values based on the device state or ADC2y conversion data. Therefore, section 0 does not offer any register map CRC check.

Sections 1 to 3 include the device configuration bits and provide independent CRC checks. Enable the register map CRC for each section using the REG\_MAPx\_CRC\_EN ( $x = 1$  to 3) bits. When the register map CRC for a section is enabled, the device constantly calculates a 16-bit CRC value across that register map section and compares the internal calculation result against the CRC value provided by the user in the REG\_MAPx\_CRC\_VALUE[15:0] bit field. If the internal calculation result and the REG\_MAPx\_CRC\_VALUE[15:0] do not match, the REG\_MAPx\_CRC\_FAULTn is set to 0b. No other action is taken by the device in the event of a register map section CRC fault.

The CRC calculation begins with the MSB of the first register in the respective register section and ends with the LSB of the last *specified* register in the respective register section using the polynomial selected in the CRC\_TYPE bit. 表 9-18 shows the exact registers that are covered by the register map CRC in each section. Two types of CRC polynomials are available: CCITT CRC and ANSI CRC (CRC-16). See the [Communication Cyclic Redundancy Check \(CRC\)](#) section for details on the CRC polynomials. The CRC calculations are initialized with the seed value of FFFFh.

**表 9-18. Registers Covered by Register Map CRC**

REGISTER SECTION	REGISTERS COVERED BY REGISTER MAP CRC
0	N/A
1	40h to 59h
2	80h to A3h
3	C0h to E3h

The CRC calculation is implemented serially, one register map bit per OSCD period. Therefore, unintended bit changes are not indicated immediately in the REG\_MAPx\_CRC\_FAULTn fault flags, but can take up to  $t_{p(\text{REG\_MAP\_CRC})}$ .

Use the following procedure to change register bits in sections 1 to 3 without accidentally causing a REG\_MAPx\_CRC\_FAULTn indication:

- Disable the register map section x CRC by setting REG\_MAPx\_CRC\_EN = 0b
- Wait the fault response time  $t_{p(\text{REG\_MAP\_CRC})}$
- If the REG\_MAPx\_CRC\_FAULTn fault flag is set to 0b, clear the fault flag by writing 1b to the REG\_MAPx\_CRC\_FAULTn bit
- Optional: Verify the REG\_MAPx\_CRC\_FAULTn fault flag is cleared to 1b
- Optional: Clear the DIGITAL\_FAULTn fault flag by writing 1b to the DIGITAL\_FAULTn bit
- Change the section x register bits as needed
- Update the REG\_MAPx\_CRC\_VALUE[15:0] bits based on the new register map section x settings
- Enable the register map section x CRC by setting REG\_MAPx\_CRC\_EN = 1b

Register bits in section x can also be changed while the register map section x CRC is enabled, as discussed in the following procedure, but can cause unintended REG\_MAPx\_CRC\_FAULTn indications.

- Change the section x register bits as needed while the register map section x CRC is enabled
- Update the REG\_MAPx\_CRC\_VALUE[15:0] bits based on the new register map section x settings
- Wait the fault response time  $t_{p(\text{REG\_MAP\_CRC})}$
- If the the REG\_MAPx\_CRC\_FAULTn fault flag is set to 0b, clear the fault flag by writing 1b to the REG\_MAPx\_CRC\_FAULTn bit
- Optional: Verify the REG\_MAPx\_CRC\_FAULTn fault flag is cleared to 1b
- Optional: Clear the DIGITAL\_FAULTn fault flag by writing 1b to the DIGITAL\_FAULTn bit

### 9.3.8.3.2 Memory Map CRC

Similar to the register map CRC, the device uses a memory map CRC to check the internal memory for random bit changes. Changes to the internal memory bits can cause undetermined device behavior or degraded device performance.

The memory map CRC is always enabled and constantly calculates the CRC value across the internal memory map. The device compares the calculation result against a memory map CRC value that is stored in the memory map in production. If the internal calculation result and the stored memory map CRC value do not match, the MEM\_MAP\_CRC\_FAULTn is set to 0b. No other action is taken by the device in the event of a memory map CRC fault.

The CRC calculation is implemented serially, one memory map word per OSCD period. Therefore random bit changes are not indicated immediately in the MEM\_MAP\_CRC\_FAULTn fault flag, but can take up to  $t_{p(\text{MEM\_MAP\_CRC})}$ .

In case of a memory map CRC fault, write 1b to the MEM\_MAP\_CRC\_FAULTn bit to clear the fault flag to 1b. Reset the device if the fault flag continues to set to 0b.

### 9.3.8.3.3 GPIO Readback

All available GPIOs (GPIOx, GPIOxy) in ADS131B23-Q1 provide an independent readback path when the respective GPIO is configured as digital output. That means an input receiver circuit independent from the output driver circuit detects the voltage level driven on the GPIO pin. The result of the readback is displayed in the according GPIx\_DAT[1:0] and GPIxy\_DAT[1:0] bit fields.

### 9.3.8.4 Communication Monitors

The communication related monitors (SPI CRC, SPI timeout, and SCLK counter) are explained in detail in the [Serial Interface Communication Structure](#) section.

In addition, the register access monitor indicates if a read or write register access was attempted to register addresses FFh or beyond. Writing to or reading from not specified register addresses within the address range from 00h to FEh does not trigger a fault indication. The data and register address returned when reading from a non-existing register is all 0s.

### 9.3.8.5 Fault Flags and Fault Masking

Every monitor in the ADS131B23-Q1 has a corresponding fault flag (see [表 9-15](#)) that sets to 0b when the respective monitor detects a fault condition. As shown in [表 9-19](#), the RESETn and communication related fault flags are located in the STATUS\_MSB register, whereas the supply, clock, and digital related fault flags are grouped together in *detailed* status registers. The STATUS\_MSB register is transmitted as part of the STATUS word at the beginning of every SPI frame as described in the [STATUS Word](#) section. To allow immediate indication of any of the supply, clock, or digital related faults as part of the STATUS word, every detailed status register has a corresponding *combined* fault flag in the STATUS\_MSB register. That is, if any of the fault flags in the detailed status register set to 0b, then the combined fault flag sets to 0b as well.

**表 9-19. Detailed Status Registers and Corresponding Combined Fault Flags**

MONITOR FAULT FLAGS FOR:	DETAILED STATUS REGISTER LOCATION	COMBINED FAULT FLAG IN STATUS_MSB REGISTER
Supply	SUPPLY_STATUS	SUPPLY_FAULTn
Clock	CLOCK_STATUS	CLOCK_FAULTn
Digital	DIGITAL_STATUS	DIGITAL_FAULTn

To clear a set combined fault flag to 1b, the host must first clear all set fault flags in the corresponding detailed status register. Only after all fault flags in the detailed status register are cleared to 1b can the host clear the combined fault flag by writing 1b.

The ADS131B23-Q1 allows additional *masking* of individual fault flags located in the detailed status registers from triggering the combined fault flag in the STATUS\_MSB register. The masking bits are located in the SUPPLY\_FAULT\_MASK, CLOCK\_FAULT\_MASK, and DIGITAL\_FAULT\_MASK registers. If a fault flag in a detailed status register is masked, a fault indicated by this masked fault flag does not trigger a fault indication of the combined fault flag in the STATUS\_MSB register. However, the fault is still indicated by the fault flag in the detailed status register.

The following examples for the AVDD OV monitor explain the various configuration options:

- No AVDD OV fault indication required in either SUPPLY\_STATUS (AVDD\_OVn fault flag) or STATUS\_MSB (SUPPLY\_FAULTn fault flag) register: Disable the AVDD OV monitor by setting AVDD\_OV\_EN = 0b.
- AVDD OV fault indication in SUPPLY\_STATUS, but not in STATUS\_MSB register: Enable the AVDD OV monitor by setting AVDD\_OV\_EN = 1b. Mask the AVDD\_OVn fault flag from triggering the SUPPLY\_FAULTn fault flag by setting AVDD\_OV\_MASK = 1b.
- AVDD OV fault indication in both SUPPLY\_STATUS and STATUS\_MSB register: Enable the AVDD OV monitor by setting AVDD\_OV\_EN = 1b. Unmask the AVDD\_OVn fault flag by setting AVDD\_OV\_MASK = 0b.



### 9.3.8.6 FAULT Pin

The GPIO2/FAULT pin can be configured as a FAULT indication output by setting GPIO2\_DIR = 1b and GPIO2\_SRC = 0b. The FAULT pin is *active* when any of the STATUS\_MSB[14:7] fault flags set to 0b. The FAULT pin changes to *inactive* as soon as all STATUS\_MSB[14:7] fault flags are cleared to 1b.

The actual output signal of the FAULT pin when active or inactive depends on the GPIO2 format (GPIO2\_FMT bit) and FAULT pin polarity (FAULT\_POL bit) configuration. See the respective bit descriptions and the [General-Purpose Digital Inputs and Outputs \(GPIO0 to GPIO4\)](#) section for details. 表 9-20 shows an example where the FAULT pin is configured for a static low signal in an active state, and a static high signal in an inactive state. The pin can for example also be configured for a static low signal in an active state, and a PWM output signal with 50% duty cycle in an inactive state to act as some sort of heart beat to indicate there is no fault. The configuration options are endless.

**表 9-20. FAULT Pin Output Behavior Configuration Example**

REGISTER BIT	BIT SETTING	DESCRIPTION
GPIO2_DIR	1b	GPIO2/FAULT pin configured as digital output
GPIO2_SRC	0b	FAULT selected as data source for GPIO2/FAULT pin
GPIO2_FMT	0b	GPIO2/FAULT pin configured for static output levels
FAULT_POL	0b	FAULT output is active low

Additionally, the ADS131B23-Q1 allows *masking* of any of the eight STATUS\_MSB[14:7] fault flags from triggering the FAULT pin. Use the mask bits in the FAULT\_PIN\_MASK register to mask individual fault flags. If a fault flag is masked and the respective fault flag is set to 0b in the STATUS\_MSB register, then no fault is indicated on the FAULT pin.

### 9.3.8.7 Diagnostics and Diagnostic Procedure

Diagnostics detect faults within a monitoring circuit to check if the monitor is still working as intended. Enable a diagnostic using the respective enable bit in 表 9-15 to inject a fault condition into the monitoring circuit. When the according monitor fault flag sets to 0b within the specified monitor fault response time (see the [Electrical Characteristics](#) table), the diagnostic completed successfully, indicating a correctly working monitor.

Except for the main clock frequency monitor diagnostics (MCLK\_HI\_DIAG\_EN and MCLK\_LO\_DIAG\_EN), all diagnostics can be performed simultaneously to save execution time. The MCLK\_HI\_DIAG\_EN and MCLK\_LO\_DIAG\_EN diagnostics must be performed sequentially. However, either the MCLK\_HI\_DIAG\_EN or the MCLK\_LO\_DIAG\_EN can be executed together with all other diagnostics.

The following steps outline the general procedure for implementing a monitor diagnostic. An example for implementing the AVDD UV monitor diagnostic is shown in parentheses.

- Enable monitor (set AVDD\_UV\_EN = 1b)
- Wait the fault response time (wait  $t_{p(AVDD\_UV)}$ )
- Clear the detailed fault flag (write 1b to AVDD\_UVn)
- Optional: Verify that the detailed fault flag is cleared to 1b (read AVDD\_UVn)
- Optional: Clear the main fault flag (write 1b to SUPPLY\_FAULTn)
- Enable diagnostic (set AVDD\_UV\_DIAG\_EN = 1b)
- Wait the fault response time (wait  $t_{p(AVDD\_UV)}$ )
- Check if the detailed fault flag is set to 0b (read AVDD\_UVn)
- Disable monitor (set AVDD\_UV\_EN = 0b)
- Disable diagnostic (set AVDD\_UV\_DIAG\_EN = 0b)
- Clear the detailed fault flag (write 1b to AVDD\_UVn)
- Optional: Clear the main fault flag (write 1b to SUPPLY\_FAULTn)
- Enable monitor (set AVDD\_UV\_EN = 1b)

The memory map CRC diagnostic is a small exception. Instead of an enable bit, select any of the three bit patterns available in the MEM\_MAP\_CRC\_DIAG[1:0] bit field to inject into the memory map CRC calculation.

### 9.3.8.8 Indicators

The ADS131B23-Q1 provides a set of indicator bits inside the STATUS\_MSB and STATUS\_LSB registers that help to verify the state of the device:

- Command response: The COMMAND\_RESPONSE[3:0] bit field is transmitted in every SPI frame and provides feedback about the command that was received by the device in the previous frame. Information about which command was executed is also provided. See the COMMAND\_RESPONSE[3:0] register bit field description for details.
- Lock state: The LOCK bit indicates if the device is currently locked or unlocked. See the [Commands](#) section for details on how to lock and unlock the device.
- Clock source: The CLOCK bit indicates which clock source the device is using as the main clock, either the internal main oscillator (OSCM) or an external clock provided at the CLK pin.
- Operating mode: The MODE bit indicates which mode the device is currently operating in, either active, standby, or power-down mode.
- ADC2A sequence active: The SEQ2A\_ACTIVE bit indicates if a sequence on ADC2A is currently in progress.

An additional OTP\_BANK status bit is provided in the DIGITAL\_STATUS register. The device includes two one-time programmable (OTP) memory banks, bank 0 and bank 1. Device configuration and calibration data are stored during device production in those OTP banks. A corrupted OTP bank can cause undetermined device behavior or degraded device performance. The information in bank 0 is duplicated in bank 1 for redundancy. At device power-up or during reset, the device loads the content of OTP bank 0 into the internal memory. If the device fails to acquire the data from bank 0, then the device loads the content from OTP bank 1. The OTP\_BANK bit indicates which bank was acquired. The device performs normally even when running from OTP bank 1.

If the device fails to acquire data from OTP bank 1 as well, then the memory map CRC fault flag is set to 0b. If resetting the device does not clear the MEM\_MAP\_CRC\_FAULTn fault flag, consider the device damaged.

### 9.3.8.9 Conversion and Sequence Counters

The STATUS\_LSB register includes 2-bit conversion and sequence counters for the various ADCs (CONV1y\_COUNT[1:0], SEQ2y\_COUNT[1:0]).

The conversion counter, CONV1y\_COUNT[1:0], increments every time a new conversion on ADC1y completes. The counter rolls over from 11b to 00b. To reset the counter, disable ADC1y or place the device in standby or power-down mode. The device makes sure that the conversion counter value always matches to the ADC1y conversion result that is output in the same SPI frame.

The sequence counter, SEQ2y\_COUNT[1:0], increments every time a new sequence on ADC2y completes. The counter rolls over from 11b to 00b. To reset the counter, disable ADC2y or place the device in standby or power-down mode. The device makes sure that the sequence counter value always matches to the ADC2y conversion step results that are output in the same SPI frame. That means, if a new sequence completes while reading out conversion results from the ADC2y conversion step result registers (SEQxy\_STEPx\_DATA), the conversion results from the new sequence run are blocked from overwriting the conversion result registers, but are internally buffered. Only after the read command is complete do the buffered conversion results from the new sequence run update the conversion step result registers.



### 9.3.8.10 Supply Voltage Readback

In addition to the dedicated supply monitors, all supplies (APWR, DPWR, AVDD, IOVDD, and DVDD) can also be measured back internally through ADC2A. Resistor dividers are integrated in the device to attenuate the supply voltages to within the input voltage range of ADC2A. See the [Electrical Characteristics](#) table for the according attenuation factors. Use the SEQ2y\_STEPx\_CH\_P[3:0] bits to configure an ADC2y sequence step for any of the supply voltage measurements.

The supply voltage measurement accuracy depends on two factors:

- Multiplexer delay time (configured using the MUX2y\_DELAY[2:0] bits)
- ADC2y conversion time (configured using the OSR2y[1:0] bits)

The large resistor divider values used internally to divide the supply voltages down together with the internal filter capacitor lead to a large RC filter time constant. The input signal therefore needs considerable time to settle when the ADC2y multiplexer selects one of the supply voltage measurements. Increasing the multiplexer delay time provides more time for the input signal to settle after the multiplexer change before ADC2y starts converting. Setting the multiplexer delay time equal to or greater than  $256 \times t_{MCLK}$  provides sufficient time for the input signals to settle when measuring the supply voltages.

If increasing the multiplexer delay time is not possible, because the delay time affects all sequence steps equally, configure multiple consecutive sequence steps for the same supply voltage measurement. Then disregard the initial sequence step readings where the conversions are not settled yet.

The input impedance of ADC2y changes with the selected conversion time, see the [Electrical Characteristics](#) table. The impedance of the resistor divider interacts with the input impedance of ADC2y leading to a gain error. Increasing the ADC2y input impedance by increasing the ADC2y conversion time reduces the gain error for the supply voltage measurements.

See [Figure 7-26](#) for details on how the supply voltage measurement accuracy changes with the multiplexer delay time and the ADC2y conversion time.

### 9.3.8.11 Temperature Sensor (TSA)

The ADS131B23-Q1 integrates a temperature sensor (TSA) to measure the die temperature of the device. The temperature sensor outputs a linear voltage that is proportional to temperature. The output voltage characteristics ( $TS_{Offset}$ ,  $TS_{TC}$ ) of the temperature sensor are specified in the [Electrical Characteristics](#) table.

Use ADC2A to measure the output signal of TSA. To select TSA for measurement, configure any of the ADC2A sequence steps (SEQ2A\_STEPx\_CH\_P[3:0]) for TSA measurement. For best measurement performance, configure the respective sequence step for gain = 2 using the SEQ2A\_STEPx\_GAIN[1:0] bits.

[Equation 18](#) shows how to convert the measured temperature sensor output voltage to die temperature:

$$\text{Die temperature [}^\circ\text{C]} = 25^\circ\text{C} + (\text{Measured voltage} - TS_{Offset}) / TS_{TC} \quad (18)$$

### 9.3.8.12 Test DACs (TDACA, TDACB)

The ADS131B23-Q1 integrates two independent Test DACs, TDACA and TDACB, one in each section of the device. TDACA uses the voltage reference in section A (REFA), and TDACB uses the voltage reference in section B (REFB). Use the TDACy\_VALUE[2:0] bits to set the Test DAC output voltage to one of eight available settings. The output voltage of Test DAC A can be applied as an input signal to any of the ADCs in section B for measurement to check the accuracy and integrity of the ADCxB signal chains, including the voltage reference (REFB). Use the respective ADCxB multiplexer configuration bits to select Test DAC A as an input signal. Correspondingly, the output voltage of Test DAC B can be applied as an input signal to any of the ADCs in section A for measurement.

Selecting the Test DAC as an input signal for multiple ADCs at the same time can degrade the measurement accuracy because of loading of the Test DAC output.

### 9.3.8.13 Open-Wire Detection

To detect potential pin fault conditions (such as open, short-to-adjacent pin, short-to-GND, or short-to-supply) on the individual ADC analog input pins, every ADC integrates a dedicated open-wire detection (OWD) current source and sink. See [Figure 9-2](#) and [Figure 9-7](#) for how the current sources and sinks are connected to the ADC inputs. The input path of ADC2y includes a series impedance of approximately 200 Ω, see [Figure 9-7](#). Consider the additional voltage drop across this impedance when enabling the current source or sink on any of the ADC2y inputs.

As listed in [Table 9-21](#), every current source and sink offers individual configuration and control.

**表 9-21. Open-Wire Detection Current Source and Sink Configuration**

REGISTER BITS	FUNCTION
OWDxy_SOURCE_VALUE[1:0]	Enables current source and selects current source value from three available settings
OWDxy_SINK_VALUE[1:0]	Enables current sink and selects current sink value from three available settings
OWDxy_SOURCE_MUX	Selects the input channel that the current source is routed to
OWDxy_SINK_MUX	Selects the input channel that the current sink is routed to

### 9.3.8.14 Missing Host Detection and MHD Pin

The ADS131B23-Q1 offers a missing host detection (MHD) monitor that detects when the host is not communicating with the device anymore. A watchdog timer checks the time between two SPI frames with valid commands including valid CRCs. If a valid command with a valid CRC is not received within the watchdog time window, the host is considered missing. There is no monitor fault flag that indicates a missing host, only the MHD pin is used to detect this fault.

To use the missing host detection mode, configure the GPIO0/MHD pin as output (GPIO0\_DIR = 1b) and the GPIO0 source for missing host detection mode (GPIO0\_SRC = 0b). When the watchdog times out, the MHD pin is set *active*. Enable the missing host detection mode by setting the MHD\_CFG[1:0] bits to one of the three available watchdog timeout windows. To reset the MHD output after a missing host was detected, disable the missing host detection mode by setting MHD\_CFG = 00b.

The actual output signal of the MHD pin when active or inactive depends on the GPIO0 format (GPIO0\_FMT bit) and MHD pin polarity (MHD\_POL bit) configuration. See the respective bit descriptions and the [General-Purpose Digital Inputs and Outputs \(GPIO0 to GPIO4\)](#) section for details. [Table 9-22](#) shows an example where the MHD pin is configured for a static low signal in an active state, and a static high signal in an inactive state. The pin can for example also be configured for a static low signal in an active state, and a PWM output signal with 50% duty cycle in an inactive state to act as some sort of heart beat signal as long as the device detects a valid host.

**表 9-22. MHD Pin Output Behavior Configuration Example**

REGISTER BIT	BIT SETTING	DESCRIPTION
GPIO0_DIR	1b	GPIO0/MHD pin configured as digital output
GPIO0_SRC	0b	MHD selected as data source for GPIO0/MHD pin
GPIO0_FMT	0b	GPIO0/MHD pin configured for static output levels
MHD_POL	0b	MHD output is active low

### 9.3.8.15 Overcurrent Comparators (OCCA, OCCB)

The ADS131B23-Q1 integrates two *digital* overcurrent comparators (OCCA, OCCB), that provide a faster response to overcurrent conditions than ADC1y, especially when ADC1y is operating at low data rates. The comparators use the ADC1y  $\Delta\Sigma$  modulator (and therefore the same multiplexer and PGA settings as ADC1y) but with a separate digital fast filter that works in parallel to the main ADC1y digital filter. This fast filter is a sinc3 implementation with a fixed OSR of 64. The offset and gain calibration values (OCAL1y[23:0], GCAL1y[15:0]) for ADC1y do not affect the OCCy comparators, which means there is no user calibration of the overcurrent comparators possible.

Enable the overcurrent comparators using the OCCy\_EN bits. To use overcurrent comparator OCCy, ADC1y must be enabled (ADC1y\_EN = 1b) as well so that the ADC1y modulator is active. However, conversions on ADC1y do not need to be started to use the overcurrent comparator function. The sinc3 filter of the comparator starts operating as soon as the OCCy\_EN bit is set and runs independently of the conversion state of ADC1y.

The digital fast filter of the comparator outputs 16-bit conversion results that are internally compared against a high and low threshold, configured by the OCCy\_HIGH\_TH[15:0] and OCCy\_LOW\_TH[15:0] register bits, respectively. The comparator triggers when the conversion results exceed the high threshold or when the results fall below the low threshold. Set OCCy\_HIGH\_TH[15:0] = 7FFFh to disable the high threshold detection. Similarly, set OCCy\_LOW\_TH[15:0] = 8000h to disable the low threshold detection.

OCCy\_NUM[4:0] configures the number of conversions that the output of the digital fast filter must exceed the programmed high or low threshold before flagging an overcurrent condition in the OCCy\_HTn or OCCy\_LTn status bits, respectively. An internal counter keeps track of the number of conversions that exceed either the high or low threshold. The counter resets as soon as one conversion result drops below the threshold again or when the OCCy comparator is disabled (OCCy\_EN = 0b).

Disable the overcurrent comparator (OCCy\_EN = 0b) before changing any comparator settings in the OCCy\_CFG, OCCy\_HIGH\_THRESHOLD, or OCCy\_LOW\_THRESHOLD registers.

Similar to the detailed supply, clock, and digital status flags, the detailed status flags in the OCC\_STATUS register feed a combined OCC\_FAULTn flag in the STATUS\_MSB register. That is, if any of the fault flags in the OCC\_STATUS register set to 0b, then the OCC\_FAULTn flag sets to 0b as well.

To clear a set OCC\_FAULTn flag to 1b after the overcurrent condition is removed, the host must first clear all set fault flags in the OCC\_STATUS register. Only after all fault flags in the OCC\_STATUS register are cleared to 1b can the host clear the OCC\_FAULTn flag by writing 1b.

The ADS131B23-Q1 allows additional *masking* of the four fault flags located in the OCC\_STATUS register from triggering the combined OCC\_FAULTn flag in the STATUS\_MSB register. The masking bits are located in the OCC\_FAULT\_MASK register. If a fault flag in the OCC\_STATUS register is masked, then a fault indicated by this masked fault flag does not trigger the OCC\_FAULTn flag in the STATUS\_MSB register. However, the fault is still indicated by the fault flag in the OCC\_STATUS register.

#### 9.3.8.15.1 OCCA and OCCB Pins

Each comparator can be configured to drive a dedicated overcurrent comparator fault pin (OCCA and OCCB pins) for fast overcurrent indication without SPI communication. To configure GPIO3/OCCA for overcurrent comparator output, set GPIO3\_DIR = 1b for digital output function and GPIO3\_SRC = 0b for OCCA output. Equivalently, set GPIO4\_DIR = 1b and GPIO4\_SRC = 0b to configure GPIO4/OCCB for overcurrent comparator B output.

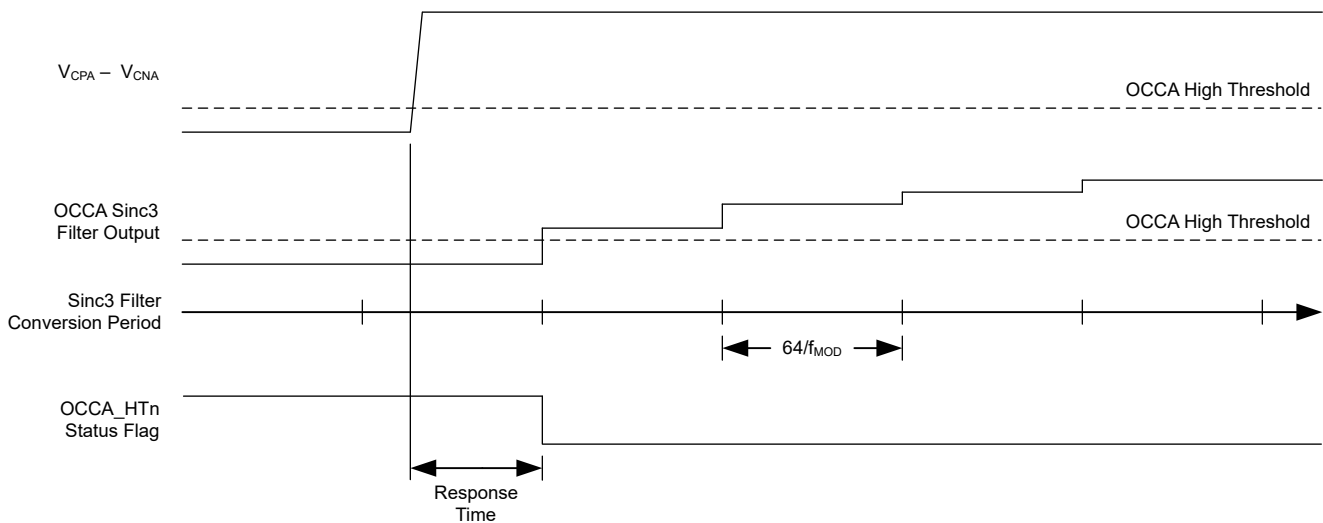
The OCCy pins indicate a fault when either the OCCy\_HTn or OCCy\_LTn bits, or both set to 0b. The mask bits in the OCC\_FAULT\_MASK register do not affect the output of the OCCy pins.

The actual output signal of the OCCy pins when active or inactive is configured in the same way as the FAULT pin. Use the GPIO3\_FMT and OCCA\_POL bits to configure the output behavior of the OCCA pin, and the GPIO4\_FMT and OCCB\_POL bits to configure the OCCB pin behavior.

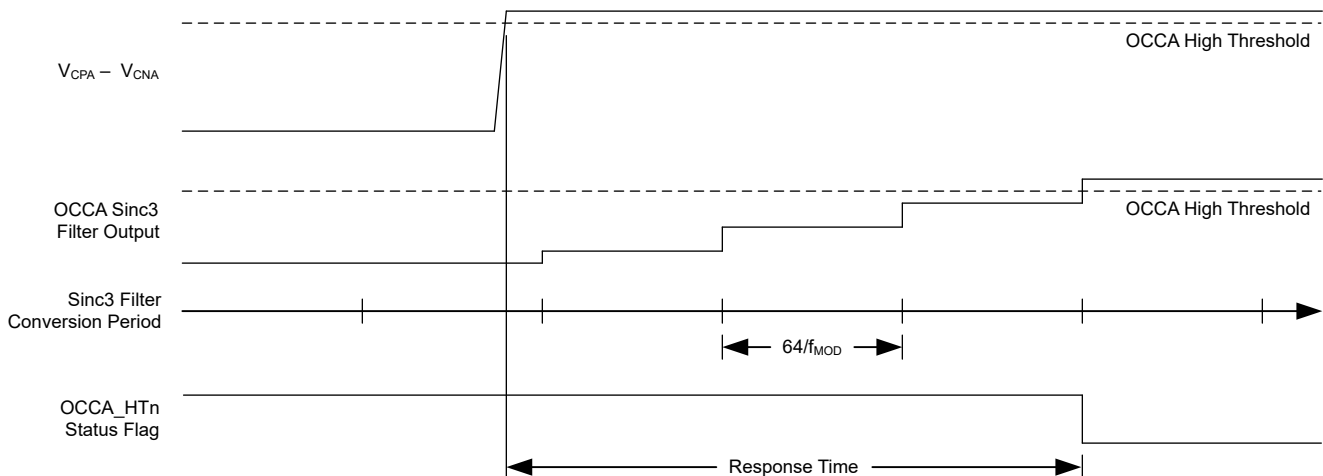
### 9.3.8.15.2 Overcurrent Indication Response Time

The fault indication response time to an overcurrent event depends on the amount of overshoot of the input signal beyond the comparator threshold. The reason for this dependency is the settling time of the sinc3 filter that is used for the digital comparator function.

☒ 9-14 and ☒ 9-15 show two examples for the OCCA fault indication behavior with  $OCCA\_NUM[4:0] = 00000b$ , that is only one conversion must exceed the threshold to trigger a fault. In ☒ 9-14 the comparator triggers in less than  $64/f_{MOD}$  ( $= 15.6 \mu s$  when using  $f_{MCLK} = 8.192 \text{ MHz}$ ) because the sinc3 filter already settles to a value above the set high threshold in one conversion due to the large overshoot beyond the high threshold on the input signal. ☒ 9-15 shows a worst case scenario where the sinc3 filter needs even four conversion periods to settle to a value above the set high threshold because the input signal barely exceeds the high threshold and the overcurrent event happens in the middle of a fast filter conversion cycle.



☒ 9-14. OCCA Behavior With Large Input Overshoot



☒ 9-15. OCCA Behavior With Small Input Overshoot

The response time changes when global-chop mode of ADC1y is enabled and ADC1y is converting. See the [Overcurrent Indication Response Time in Global-Chop Mode](#) section for details.

## 9.4 Device Functional Modes

### 9.4.1 Power-Up and Reset

The ADS131B23-Q1 is reset in one three ways:

- Power-on reset (POR)
- RESETn pin (hardware reset)
- RESET command (software reset)

After a reset occurs, the user registers reset to the respective default settings and the device is in active mode. All ADCs are enabled, but no conversions are started. With all three reset options, a low-to-high transition on the DRDYn pin indicates that the SPI interface is ready for communication. The device ignores any SPI communication before this point and SDO stays low.

#### 9.4.1.1 Power-On Reset (POR)

Power-on reset (POR) is the reset that occurs when valid supply voltages are first applied to the device. The POR process requires  $t_{POR}$  to complete from when all supply voltages exceed the respective POR thresholds (AVDD\_POR\_TH, IOVDD\_POR\_TH, and DVDD\_POR\_TH) to allow the internal circuitry to power up. The DRDYn pin transitions from low to high immediately after  $t_{POR}$ , indicating the SPI interface is ready for communication.

#### 9.4.1.2 RESETn Pin

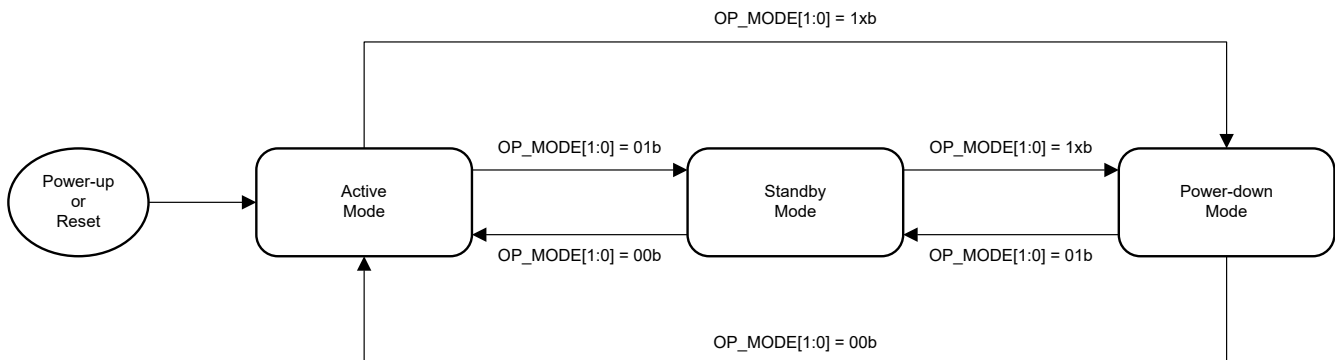
The RESETn pin is an active low pin with an internal pulldown resistor to DGND. The device resets if the pin is held low for longer than  $t_{w(RSL)}$  and maintains a reset state until the RESETn pin is returned high. The host must actively drive the pin high for the device to operate. Wait for at least  $t_{REGACQ}$  after the RESETn pin is brought high or for the DRDYn rising edge before communicating with the device.

#### 9.4.1.3 RESET Command

The ADS131B23-Q1 can be reset with the SPI RESET command. See the [RESET](#) section for details. A device reset occurs immediately after the RESET command is latched. The host must wait for at least  $t_{REGACQ}$  or for the DRDYn rising edge before communicating with the device.

### 9.4.2 Operating Modes

The ADS131B23-Q1 offers three operating modes: active, standby, and power-down mode. The mode is programmable using the OP\_MODE[1:0] bits. [Figure 9-16](#) shows how the device transitions between the different operating modes.



**Figure 9-16. Operating Mode State Diagram**

#### 9.4.2.1 Active Mode

Active mode is the default operating mode after power-up or reset. In active mode all internal circuitry is powered up. By default all ADCs are enabled, but no conversions are started. The individual ADCs can be enabled or

disabled using the respective ADCxy\_EN bits. ADC conversions can only be started in active mode and when the respective ADC is enabled.

#### 9.4.2.2 Standby Mode

In standby mode all internal circuitry is powered up, but all ADCs are disabled and ongoing conversions are stopped immediately irrespective of the ADCxy\_EN bit settings. No ADC conversions can be started in standby mode. Transition the device to standby mode before changing the main clock source using the CLK\_SOURCE bit to prevent clock glitching during the clock switchover.

#### 9.4.2.3 Power-Down Mode

In power-down mode, all nonessential internal circuitry (such as the ADCs, voltage references, and oscillators) is powered down. The LDOs and POR circuitry stay active. Register settings are retained in power-down mode. All ADCs are disabled and ongoing conversions are stopped immediately irrespective of the ADCxy\_EN bit settings. No conversions can be started in power-down mode. When transitioning to active mode, wait for the voltage reference start-up time before starting any conversions to allow the voltage references to power up.

### 9.4.3 ADC Conversion Modes

#### 9.4.3.1 ADC1y Conversion Modes

The ADS131B23-Q1 offers two conversion modes for ADCs ADC1y: continuous-conversion and single-shot conversion mode.

The CONV\_MODE1A bit selects the conversion mode for ADC1y.

Do not change the contents of the following registers while conversions on ADC1y are ongoing: ADC1y\_CFG, ADC1y\_OCAL\_MSB, ADC1y\_OCAL\_LSB, and ADC1y\_GCAL. Stop conversions or disable ADC1y before making changes to these registers.

##### 9.4.3.1.1 Continuous-Conversion Mode

In continuous-conversion mode, ADC1y converts indefinitely until stopped by the host. Set the respective STARTy bits in the CONVERSION\_CTRL register to start conversions of the enabled ADC, ADC1y. Conversions on ADC1A and ADC1B can be started at different times using the respective STARTA and STARTB bits. Setting the STARTy bit while conversions are ongoing on an ADC aborts the ongoing conversion and restarts conversions. Use the STOPy bits to stop conversions of the enabled ADC, ADC1y. The currently ongoing conversion is allowed to finish after the STOPy bit is set and the digital filter is held in reset thereafter. After setting the STOPy bits, the STOPy bits read back 1b until conversions are stopped.

The STARTy bits take priority over the STOPy bits. That means if both the STARTy and STOPy bits in the CONVERSION\_CTRL register are set at the same time, then conversions are started or ongoing conversions are aborted and new conversions are started.

The last conversion result of an ADC is still available for readout after conversions are stopped. The conversion results of an ADC are only cleared after a device reset, when the ADC is disabled, when the device is in standby or power-down mode, or are overwritten when a new conversion result becomes available.

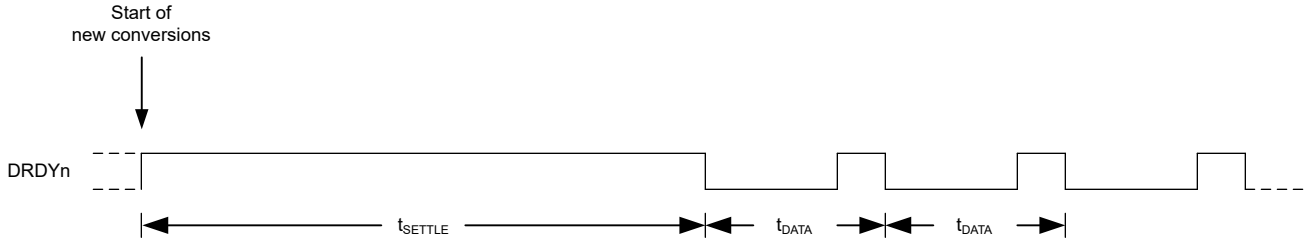
The STARTy bits take effect and conversions start at the last SCLK falling edge of the register data CRC word within the SPI frame where the CONVERSION\_CTRL register is written. See the [Serial Interface Communication Structure](#) section for details on the SPI frame of a register write command.

Setting the STARTy bit drives the DRDYn pin high if DRDYn was low, however the old conversion data can still be read until the new conversions become available.

ADC1y use a sinc3 digital filter that requires three conversion periods to settle. When conversions are started or restarted using the STARTy bits, the device hides the first two unsettled conversions and only provides a settled conversion result after the third conversion period. Use 式 19 to calculate the time until the first conversion after a conversion start is available. All subsequent conversions have a conversion period, as shown in 図 9-17, of  $t_{DATA} = 1 / f_{DATA} = OSR / f_{MOD}$ .

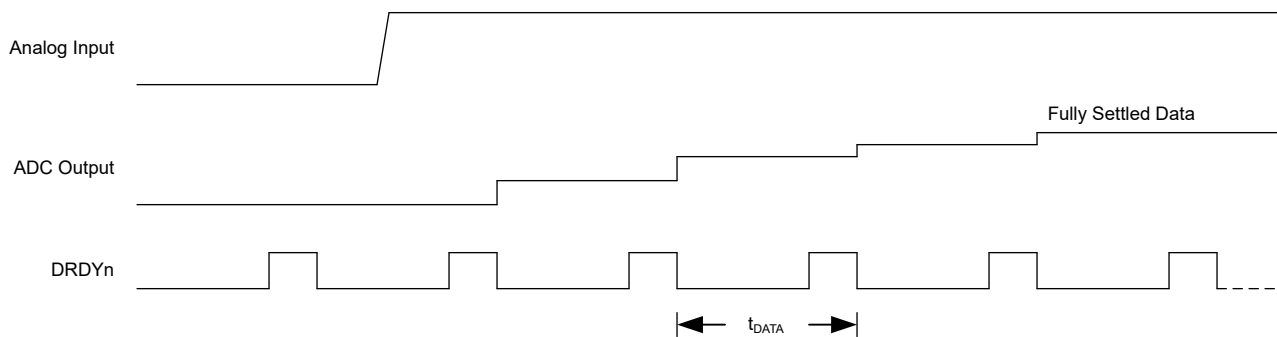
$$t_{SETTLE} = (3 \times OSR + 44) \times t_{MOD} \quad (19)$$





**图 9-17. Sinc3 Filter Settling Time and Conversion Period**

The ADC does not detect when a sudden step change on the analog input occurs while the ADC is continuously converting. Therefore, the ADC continues to output conversion data at the programmed output data rate. If the step change occurs concurrently with the start of a new conversion period, then settled data are output three conversion periods after the step change. However, the sinc3 filter takes four conversion periods to provide settled data, as shown in [图 9-18](#), if the step change occurs in the middle of a conversion period.



**图 9-18. SINC3 Filter Behavior During Input Step Change**

#### 9.4.3.1.2 Single-Shot Conversion Mode

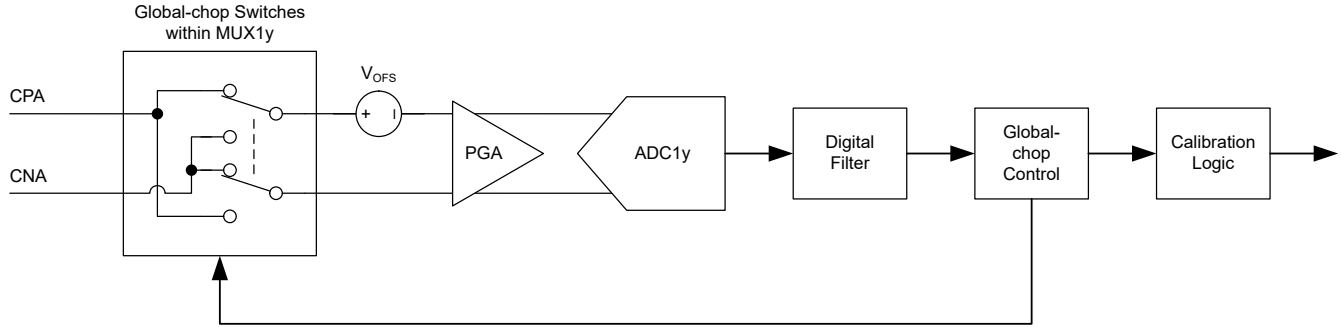
In single-shot conversion mode, ADC ADC1y performs one single conversion after the STARTy bit is set. Setting the STARTy bit while a conversion is ongoing on an ADC aborts the ongoing conversion and restarts a single new conversion. The STOPy bits have no effect in single-shot conversion mode.

Equivalent to continuous-conversion mode, the STARTy bits take effect and conversions start at the last SCLK falling edge of the register data CRC word within the SPI frame where the CONVERSION\_CTRL register is written.

Every conversion in single-shot conversion mode is available after the first-conversion settling time as calculated by [式 19](#). If an input step change occurs during the conversion process, the conversion result is not fully settled. Another subsequent single-shot conversion is required in that case to output a settled conversion result.

#### 9.4.3.1.3 Global-Chop Mode

The signal chain of ADC1y uses a very low-drift, chopper-stabilized PGA and  $\Sigma\Delta$ -modulator to provide very low offset error and offset drift. However, a small amount of offset drift remains in normal measurement. For that reason, the ADC1y signal chain incorporates an optional global-chop mode to reduce offset error and offset drift over both temperature and time to exceptionally low levels. When the global-chop mode is enabled by setting the GC1y\_EN bit, ADC1y performs two consecutive conversions with alternate input signal polarity to cancel offset error. The first conversion is taken with normal input polarity. The global-chop control logic inverts the input polarity and resets the digital filter for the second conversion. The average of the two conversions yields the final corrected result, removing the offset voltage. [图 9-19](#) illustrates a block diagram of the ADC1y global-chop implementation.  $V_{OFS}$  models the combined PGA and ADC1y internal offset voltage. Only this device-inherent offset voltage is reduced by global-chop mode. Offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.



**图 9-19. ADC1y Global-Chop Mode Control Diagram**

The operational sequence of global-chop mode is as follows:

- Conversion C1:  $V_{CPA} - V_{CNA} - V_{OFS} \rightarrow$  First conversion withheld after conversion start
- Conversion C2:  $V_{CNA} - V_{CPA} - V_{OFS} \rightarrow$  Output 1 =  $(V_{C1} - V_{C2}) / 2 = V_{CPA} - V_{CNA}$
- Conversion C3:  $V_{CPA} - V_{CNA} - V_{OFS} \rightarrow$  Output 2 =  $(V_{C3} - V_{C2}) / 2 = V_{CPA} - V_{CNA}$
- ...

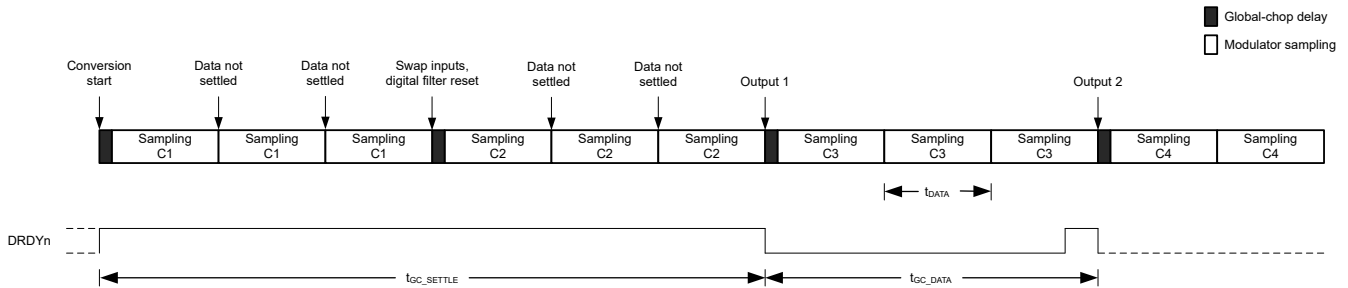
The first conversion result (Output 1) after a conversion start is available after ADC1y takes two settled conversions. Because of the sinc3 filter, data of one conversion settles in three conversions cycles. 式 20 calculates the time required to output the first conversion result after a conversion start.

In continuous-conversion mode with the global-chop mode enabled, subsequent conversions complete in  $t_{GC\_DATA}$ , as calculated by 式 21 and shown in 图 9-20. That means the data rate in global-chop mode is approximately  $1/3^{rd}$  the data rate in normal mode.

$$t_{GC\_SETTLE} = 2 \times (t_{GC1y\_DELAY} + 3 \times OSR \times t_{MOD}) + 44 t_{MOD} \quad (20)$$

$$t_{GC\_DATA} = t_{GC1y\_DELAY} + 3 \times OSR \times t_{MOD}, \quad (21)$$

Before starting conversions after the input polarity is inverted, ADC1y waits the global-chop delay time,  $GC1y\_DELAY[2:0]$ , to allow for the internal circuitry to settle. In some cases, the programmable global-chop delay time must be increased to allow for settling of external components.



**图 9-20. Sinc3 Filter Settling Time and Conversion Period in Global-Chop Mode**

Global-chop mode reduces the ADC1y noise by a factor of  $\sqrt{2}$  because two conversions are averaged. Divide the input-referred noise values in 表 8-1 by  $\sqrt{2}$  to derive the noise performance when global-chop mode is enabled.

The notches of the sinc3 filter in 图 9-3 do not change in global-chop mode. However, additional filter notches appear at multiples of  $f_{GC\_DATA} / 2$ .



#### 9.4.3.1.3.1 Overcurrent Indication Response Time in Global-Chop Mode

Enabling global-chop mode of ADC1y changes the overcurrent detection behavior of OCCy when ADC1y is converting. The OCCy digital fast filter resets each time ADC1y inverts the polarity of the analog inputs. After every fast filter reset, the device ignores the first two conversions of the OCCy filter because these conversions are unsettled. The device does not increment the OCCy\_NUM counter for these two conversions. Depending on the OCCy\_NUM and OSR1y settings, the overcurrent indication response time in global-chop mode can therefore be longer compared to when global-chop mode is disabled. The difference in response time is most noticeable when using large OCCy\_NUM and small OSR1y settings.

Figure 9-21 shows an example of the OCCy behavior with OSR1y = 128. The OCCy DRDYn signal indicates when conversions of the OCCy fast filter complete. This signal is internal only and is not accessible by the host. In this specific example, the OCCy\_NUM counter only manages to increment four times per ADC1y conversion period. If OCCy\_NUM = 8, up to two full ADC1y conversion periods are required before the OCCy\_NUM counter reaches 8. Which means that the overcurrent detection time increases from  $8 \times 64 / f_{MOD}$  (global-chop mode disabled) to  $12 \times 64 / f_{MOD}$  (global-chop mode enabled).

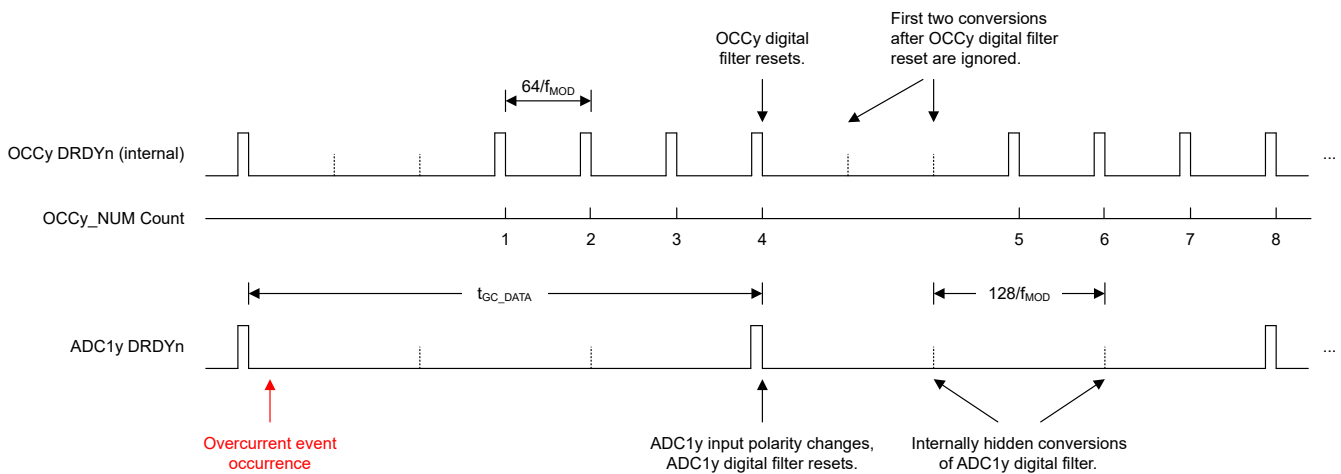


Figure 9-21. Overcurrent Detection Behavior With Global-Chop Mode Enabled (ADC1y OSR = 128)

### 9.4.3.2 ADC2y Sequencer Operation and Sequence Modes

In contrast to ADC1y, conversions on ADC2y are controlled by means of a channel sequencer. [Figure 9-22](#) depicts a flow chart of the sequencer operation. The ADC2y sequencer has up to 16 sequence steps that are individually enabled or disabled using the SEQ2y\_STEPn\_EN bits (n = 0 to 15). Each sequence step corresponds to one single conversion of ADC2y, which means up to 16 different measurements can be taken in one sequence run. The SEQ2y\_STEPn\_CFG registers configure the PGA gain, and the positive and negative input for the PGA for every sequence step. When a sequence is started, the sequencer steps through all enabled sequence steps, always starting with step 0. The sequencer ignores sequence steps that are disabled. One conversion is taken by ADC2y in each step before the sequencer configures ADC2y for the next step in the sequence. After the sequencer configures ADC2y for the next sequence step, the sequencer adds a programmable delay before starting the conversion to allow for settling of the input signal. The MUX2y\_DELAY[2:0] bits select the delay time globally for all sequence steps. The time required to complete a sequence is given by [Equation 22](#):

$$t_{\text{SEQ}} = N \times (t_{\text{MUX\_DELAY}} + t_{\text{CONVERSION}}) \quad (22)$$

where:

- N is the number of enabled steps
- $t_{\text{MUX\_DELAY}}$  is the multiplexer delay time
- $t_{\text{CONVERSION}}$  is the conversion time of ADC2y

While a sequence is ongoing, the SEQ2y\_ACTIVE bit is set in the STATUS register.

Do not make any changes to registers in the address range from 0x8C to 0x9F while ADC2A is enabled.

To avoid false sequencer starts, follow this procedure to configure and start the sequencer:

1. Disable ADC2y by setting ADC2y\_EN = 0b, or alternatively put the device into standby mode
2. Configure the ADC2y sequencer register bits
3. Enable ADC2y by setting ADC2y\_EN = 1b, or alternatively put the device back into active mode
4. Start the sequence by setting the SEQ2y\_START bit

Setting the SEQ2y\_START bit while ADC2y is disabled does not start a sequence.

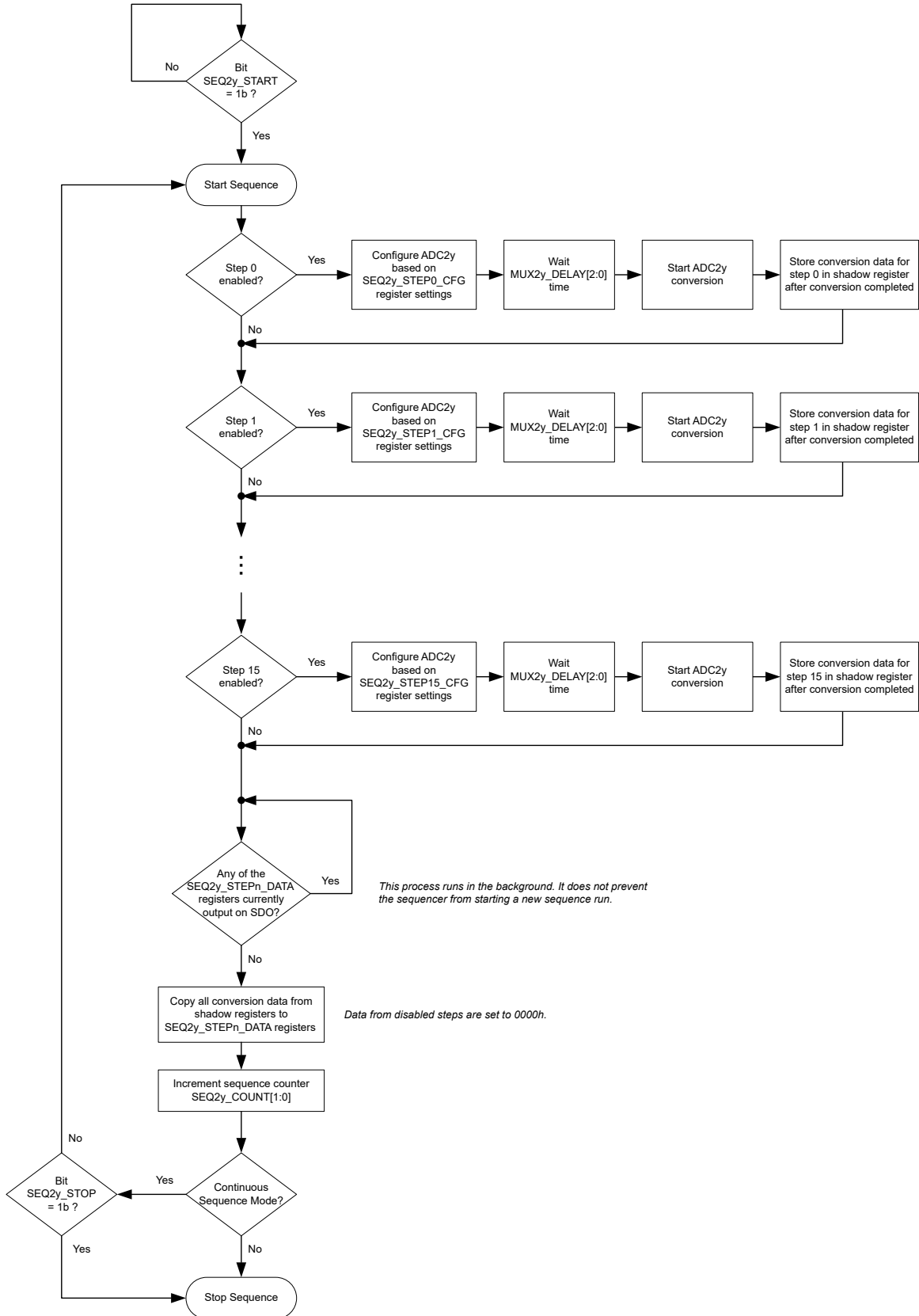
Conversion data for the sequence steps of ADC2y are 16 bits and (in contrast to ADC1y conversion data) are stored in the user register space (register addresses 10h to 1Fh). The conversion data for sequence step *n* are stored in the corresponding SEQ2y\_STEPn\_DATA register. Conversion data for a sequence step that is disabled are set to 0000h. Read ADC2y conversion data using the register read command.

The conversion data of all SEQ2y\_STEPn\_DATA registers only update when a sequence run of ADC2y completes. While a sequence run is ongoing, the conversion data of the previous sequence run are read from the SEQ2y\_STEPn\_DATA registers. There is no data corruption or mix of data from two different sequence runs, even when a sequence completes while the SEQ2y\_STEPn\_DATA registers are read.

The ADC2y sequencer offers three sequence modes:

- Continuous sequence mode
- Single-shot sequence mode
- Synchronized single-shot sequence mode based on ADC1y conversion starts

The SEQ2y\_MODE[1:0] bits select the sequence mode for ADC2y.



9-22. ADC2y Sequencer Flow Chart

#### 9.4.3.2.1 Continuous Sequence Mode

In continuous sequence mode, the ADC2y sequencer runs through the configured sequence over and over again until stopped by the host. Set the respective SEQ2y\_START bit in the CONVERSION\_CTRL register to start the sequencer of ADC2y. Setting the SEQ2y\_START bit while the sequencer is running aborts the ongoing sequence run and restarts a new sequence run from the beginning. Use the SEQ2y\_STOP bit to stop the sequencer of ADC2y. The currently ongoing sequence run is allowed to finish after the SEQ2y\_STOP bit is set. After setting the SEQ2y\_STOP bit, the SEQ2y\_STOP bit reads back 1b until the sequencer stopped. Disabling ADC2y or putting the device into standby or power-down mode aborts the sequence run immediately.

The SEQ2y\_START bits take priority over the SEQ2y\_STOP bits. That means if both the SEQ2y\_START and SEQ2y\_STOP bits in the CONVERSION\_CTRL register are set at the same time, then the sequencer starts a sequence run or aborts an ongoing sequence run and starts a new sequence run from the beginning.

The last conversion results of an ADC2y sequence run are still available for readout after the sequencer stopped. The conversion results of the sequencer are only cleared to 0000h after a device reset, when the ADC is disabled, when the device is in standby or power-down mode, or are overwritten when conversion results from a new sequence run become available.

#### 9.4.3.2.2 Single-Shot Sequence Mode



In single-shot sequence mode the ADC2y sequencer runs through the configured sequence one time after the SEQ2y\_START bit is set. Setting the SEQ2y\_START bit while a sequence is ongoing aborts the ongoing sequence and restarts a single new sequence run from the beginning. The SEQ2y\_STOP bit has no effect in single-shot sequence mode.

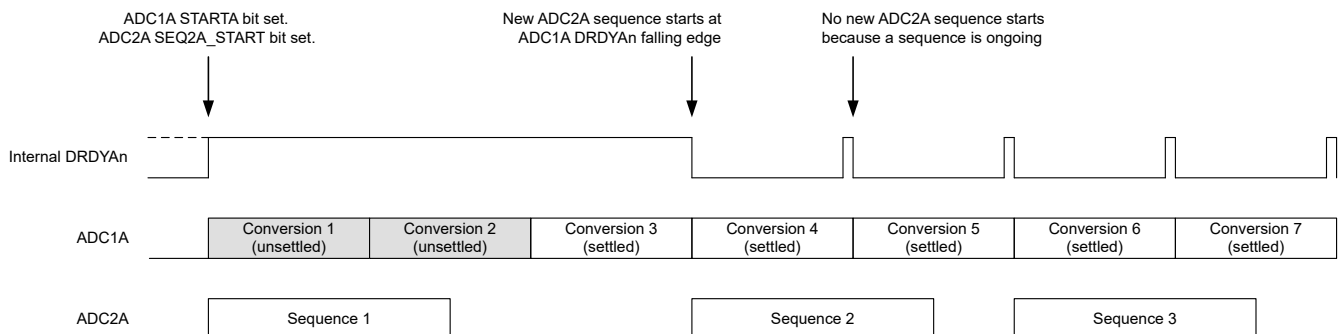
#### 9.4.3.2.3 Synchronized Single-Shot Sequence Mode Based on ADC1y Conversion Starts

The synchronized sequence mode allows the sequence starts of ADC2A to be synchronized with the conversion starts of ADC1A. In this mode a single sequence run is started on ADC2y whenever a new conversion on ADC1y starts. However, an *ongoing* sequence run on ADC2y does not abort and restart when a new conversion on ADC1y starts. This means a single new sequence run on ADC2y is only triggered by ADC1y when no sequence is currently ongoing.

Start the ADC2y sequencer initially by setting the SEQ2y\_START bit.

The synchronized single-shot sequence mode is only useful when ADC1y is configured for continuous-conversion mode. When ADC1y is configured for single-shot conversion mode, synchronize conversions of ADC1y and sequence starts of ADC2y by setting the STARTy and SEQy\_START bits at the same time.

 9-23 shows an example of how ADC1A conversions and ADC2A sequence starts are synchronized. The falling edge of the internally generated DRDYAn signal in  9-23 indicates when new ADC1A conversion results are available and a new ADC1A conversion starts.



 9-23. Synchronizing ADC1A Conversions and ADC2A Sequence Starts

## 9.5 Programming

### 9.5.1 Serial Interface

The ADS131B23-Q1 uses an SPI-compatible interface to configure the device and retrieve conversion data. The device always acts as an SPI peripheral; SCLK and CSn are inputs to the interface. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the controller and peripheral on SCLK falling edges. The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: CSn, SCLK, SDI, and SDO. In addition, the DRDYn pin serves as a flag to the host to indicate new conversion data are available.

#### 9.5.1.1 Serial Interface Signals

##### 9.5.1.1.1 Chip Select (CSn)

The CSn pin is an active low input signal that selects the device for communication. The device ignores any communication and SDO is high impedance when CSn is held high. Hold CSn low for the duration of a communication frame to ensure proper communication. The interface is reset each time CSn is taken high.

##### 9.5.1.1.2 Serial Data Clock (SCLK)

The SCLK pin is an input that serves as the serial clock for the interface. Output data on SDO transition on the rising edge of SCLK and input data on SDI are latched on the falling edge of SCLK.

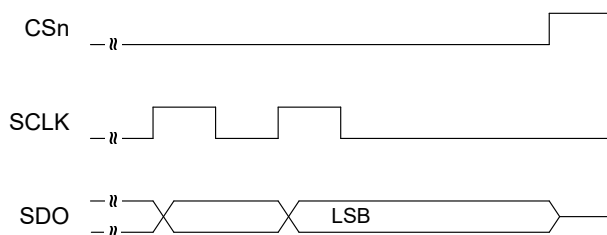
##### 9.5.1.1.3 Serial Data Input (SDI)

The SDI pin is the serial data input pin for the device. Serial commands are shifted in through the SDI pin by the device with each SCLK falling edge when the CSn pin is low.

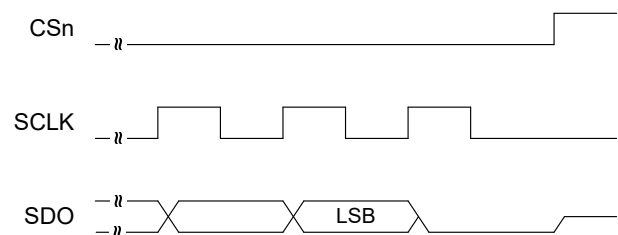
##### 9.5.1.1.4 Serial Data Output (SDO)

The SDO pin is the serial data output pin for the device. The device shifts out data serially with each rising SCLK edge when the CSn pin is low. This pin assumes a high-impedance state when CSn is high. When CSn transitions low, the SDO pin drives low.

SDO stays at the level of the last bit sent if the host does not send any extra SCLK pulses after the last data is shifted out on SDO. If the host sends additional SCLK pulses after the last data is shifted out, then SDO drives low. [Figure 9-24](#) and [Figure 9-25](#) show timing diagrams of the SDO behavior both without and with additional SCLK pulses, respectively.



**Figure 9-24. SDO Behavior Without Additional SCLK Pulses**

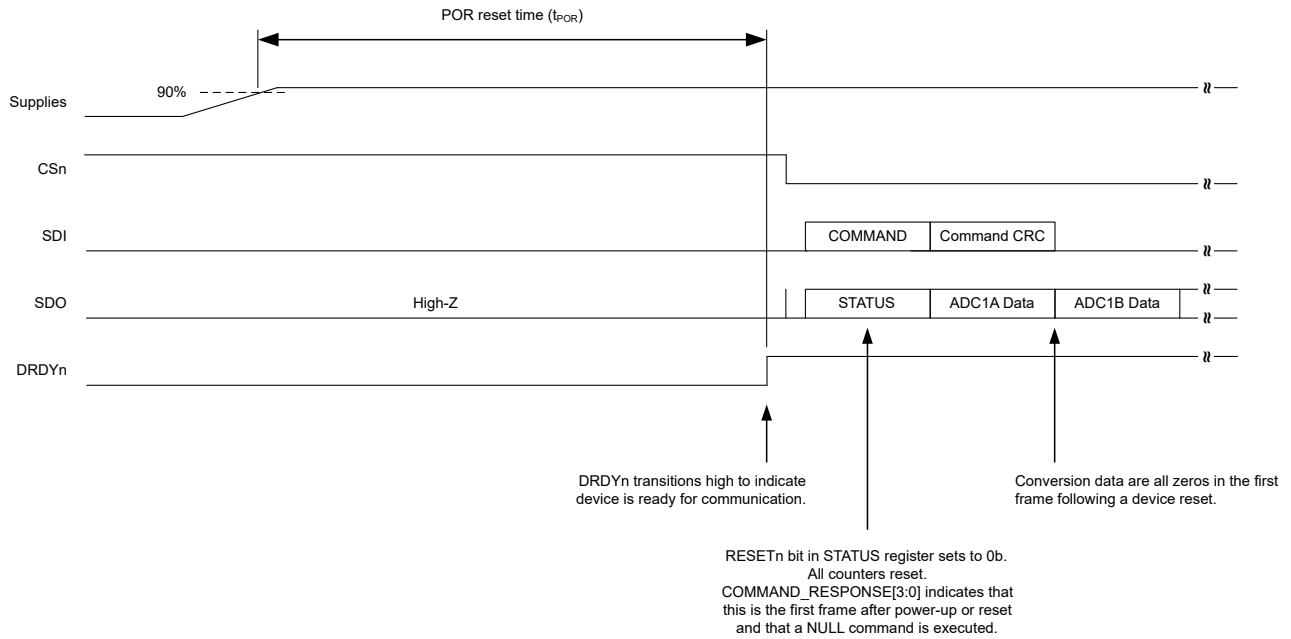


**Figure 9-25. SDO Behavior With Additional SCLK Pulses**

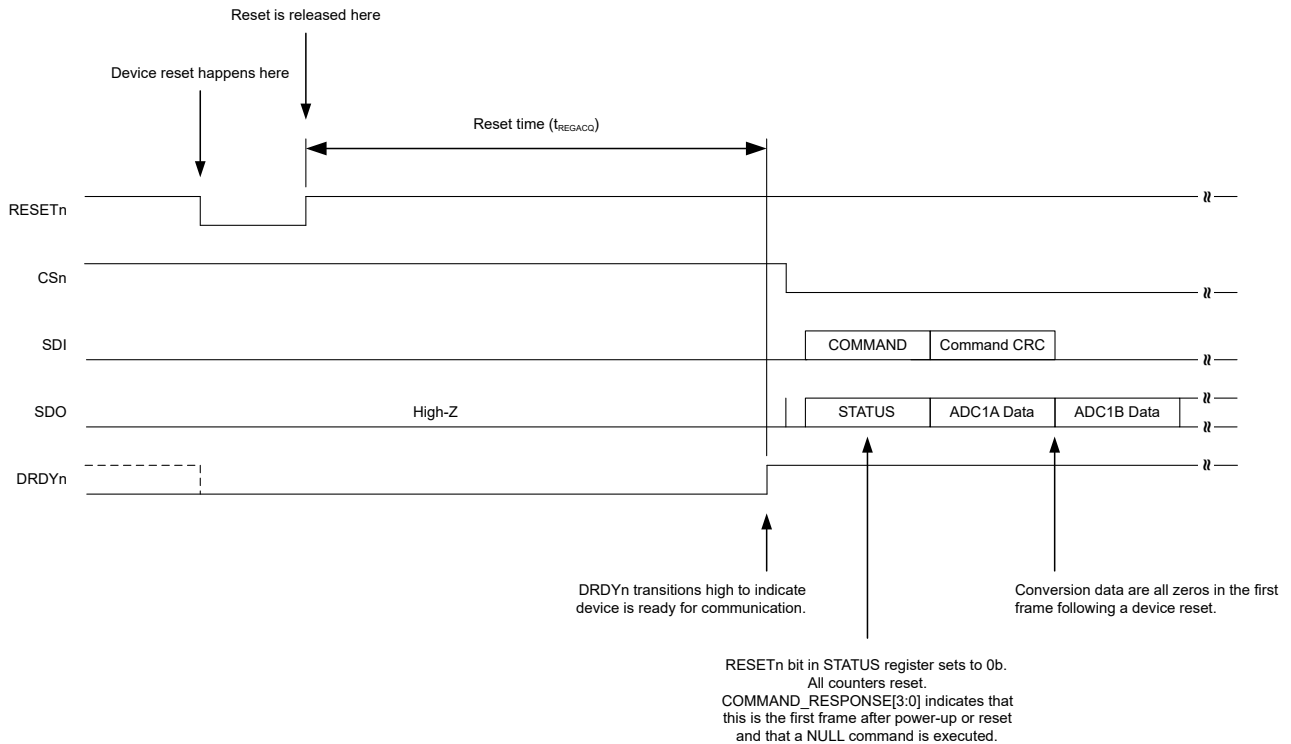
##### 9.5.1.1.5 Data Ready (DRDYn)

The DRDYn pin is an active-low, push-pull output. A DRDYn falling edge indicates when new conversion data of ADC1A or ADC1B are available for readout. The DRDY\_CTRL bit selects which ADC drives the DRDYn signal, either ADC1A or ADC1B. If the host starts ADC1A and ADC1B conversions at the same time by setting both the STARTA and STARTB bits during the same CONVERSION\_CTRL register write, conversions of both ADCs complete at the same time. The period between DRDYn falling edges is the data rate period of the ADC that controls the DRDYn pin.

During device power-up or while the device is held in reset, the DRDYn pin drives low. As shown in [9-26](#) and [9-27](#), the DRDYn pin drives high after the POR is released and the device is ready for communication.



**9-26. DRDYn Pin Behavior After POR**



**9-27. DRDYn Pin Behavior After Device Reset**

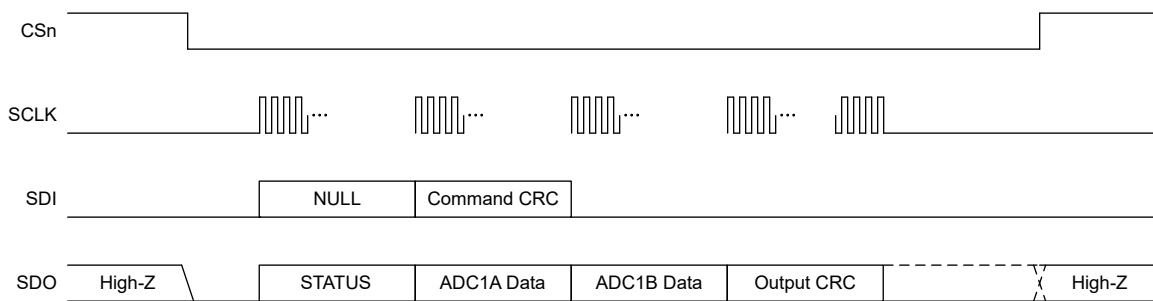
## 9.5.1.2 Serial Interface Communication Structure

### 9.5.1.2.1 SPI Communication Frames

SPI communication on the ADS131B23-Q1 is performed in frames. Each SPI communication frame starts with a CSn falling edge, consists of several words, and ends with a CSn rising edge. The interface is full duplex, meaning that the interface is capable of transmitting data on SDO while simultaneously receiving data on SDI. [Figure 9-28](#) provides an overview of the general SPI frame structure and frame length for the various commands.

The input frame that the host sends on SDI always begins with a command word followed by a command CRC word. The first word on the output frame that the device transmits on SDO always begins with the STATUS word. The number of words in a frame depends on the command provided. See the [Commands](#) section for a list of all valid commands on the ADS131B23-Q1.

For the NULL, RESET, LOCK, UNLOCK, and RREG commands there are four words in a frame. On SDI, the host provides the command, the command CRC, and two additional words of zeros. Simultaneously on SDO, the device outputs the STATUS word, two words of ADC data (representing the data from ADC1A and ADC1B), and an output CRC word. [Figure 9-28](#) shows a typical communication frame structure. In the remaining sections of this document the SCLK signal is omitted in the figures for clarity.



**Figure 9-28. Typical Communication Frame**

For a write register (WREG) command where more than one register is written, the frame extends to accommodate the additional data. See the [WREG](#) section for more details on the WREG command.

For a read register (RREG) command, the response to the command in the following frame contains the STATUS word followed by the register data requested, which can require a shorter or longer frame depending on how many registers are read. See the [RREG](#) section for more details on the RREG command.

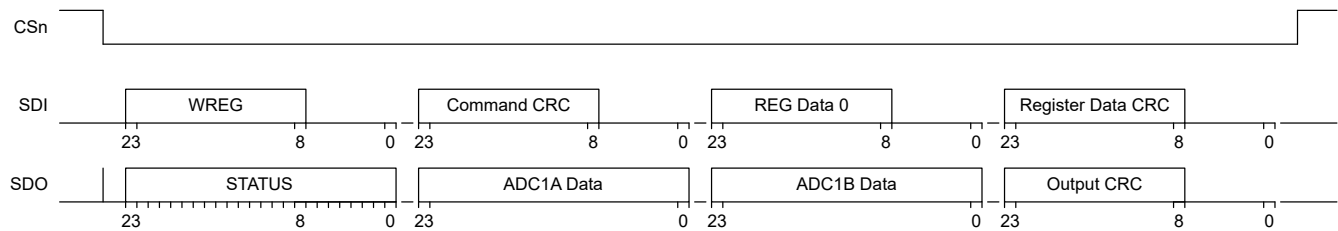
**9.5.1.2.2 SPI Communication Words**

An SPI communication frame of the ADS131B23-Q1 is made of multiple words. The word size is configurable as either 24 bits, or 32 bits using the WORD\_LENGTH bit in the DEVICE\_CFG register. The content within each word is always most significant bit (MSB) aligned and least significant bit (LSB) padded with zeros to accommodate 24-bit or 32-bit word sizes. 表 9-23 provides an overview of all available word types and the actual unpadding data length of the respective content.

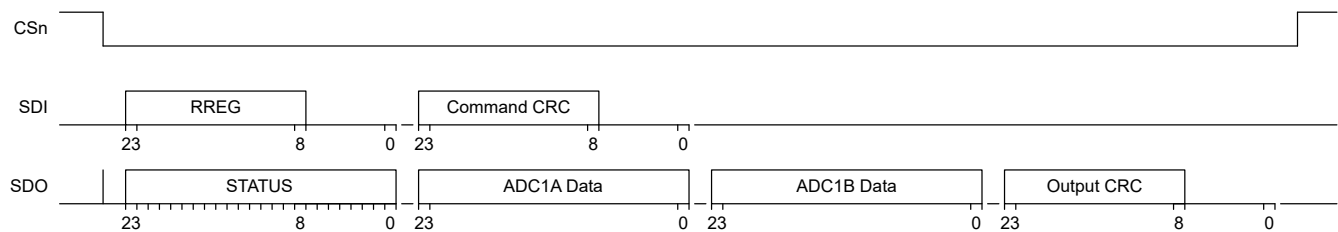
**表 9-23. Unpadding Data Length of Individual Word Types**

DIRECTION	WORD TYPE	UNPADDING DATA LENGTH
SDI	Command	16 bits
SDI	Command CRC	16 bits
SDI	Register data for WREG command	16 bits
SDI	Register data CRC for WREG command	16 bits
SDO	STATUS	24 bits
SDO	ADC1A and ADC1B conversion data	24 bits
SDO	Register data for RREG command	16 bits register data + 8 bits register address
SDO	Output CRC	16 bits

图 9-29 and 图 9-30 show the bit alignments and zero padding within the individual words for a WREG and RREG command, respectively.



**图 9-29. Bit Alignment, 24-Bit Word Size, WREG Command**



**图 9-30. Bit Alignment, 24-Bit Word Size, RREG Command**



### 9.5.1.2.3 STATUS Word

The ADS131B23-Q1 outputs a STATUS word as the first word in every frame on SDO. The 24-bit STATUS word is a concatenation of the STATUS\_MSB[15:0] and STATUS\_LSB[15:8] register bits. Fault flags, status flags, ADC1A and ADC1B conversion counters, ADC2A sequence counters, and the command response are all part of these bits. See the respective register bit descriptions in the [Register Map](#) section for details.

- Communication-related fault flags, such as the SPI\_CRC\_FAULTn, SPI\_TIMEOUTn, SCLK\_COUNT\_FAULTn, and REG\_ACCESS\_FAULTn flags, always indicate faults that occurred in the previous SPI frame. These fault flags clear automatically for the next SPI frame.
- All other device-related fault and status flags indicate the state of the device at the instance of the start of the current SPI frame.
- All fault flags, except for the communication related fault flags mentioned above, are latching. That means, these fault flags do not reset automatically to 1b when the fault condition is removed and must be cleared by the host.
- The command response indicates which command was received by the device in the previous SPI frame and was executed.
- The conversion and sequence counters indicate the count of the data which is output in the current SPI frame.

### 9.5.1.2.4 Communication Cyclic Redundancy Check (CRC)

The ADS131B23-Q1 features a cyclic redundancy check (CRC) engine on both input and output data to detect SPI communication errors. Overall there are three different CRCs that are all 16 bits wide:

- On SDI: Command CRC and, in case of a WREG command, a register data CRC
- On SDO: Output CRC

The command CRC covers the command word (that is, the first word on SDI in every frame). The WREG command is a special case that requires an additional register data CRC. The register data CRC covers the register data words transmitted after the command CRC word. The output CRC covers all words on SDO preceding the output CRC word. The CRCs also cover all zero-padded bits.

The device checks the provided command CRC, and (in case of a WREG command) the register data CRC against the internally calculated CRCs based on the received input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands if the command CRC or register data CRC checks fail. The device sets the SPI\_CRC\_FAULTn bit in the STATUS\_MSB register for all cases of a CRC error on the input data.

The response on the output in the SPI frame following a frame where a CRC error occurred is that of a NULL command, which means the STATUS word plus the conversion data for ADC1A and ADC1B are output in the following SPI frame. The SPI\_CRC\_FAULTn bit is output as part of the STATUS word to provide immediate indication that a CRC error occurred in the previous frame. The SPI\_CRC\_FAULTn bit clears automatically in the next SPI frame.

There are two types of CRC polynomials available: CCITT CRC and ANSI CRC (CRC-16). The CRC polynomial setting determines the algorithm for all three CRCs. The CRC type is programmed using the CRC\_TYPE bit. [表 9-24](#) lists the details of the two CRC types.

The CRC calculation is initialized with the seed value of FFFFh to detect errors in the event that SDI or SDO are stuck low.

**表 9-24. CRC Types**

CRC TYPE	POLYNOMIAL	BINARY POLYNOMIAL
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

**9.5.1.2.5 Commands**

表 9-25 contains a list of all valid commands, a short description of the command functionality, and the binary command word.

**表 9-25. Command Definitions**

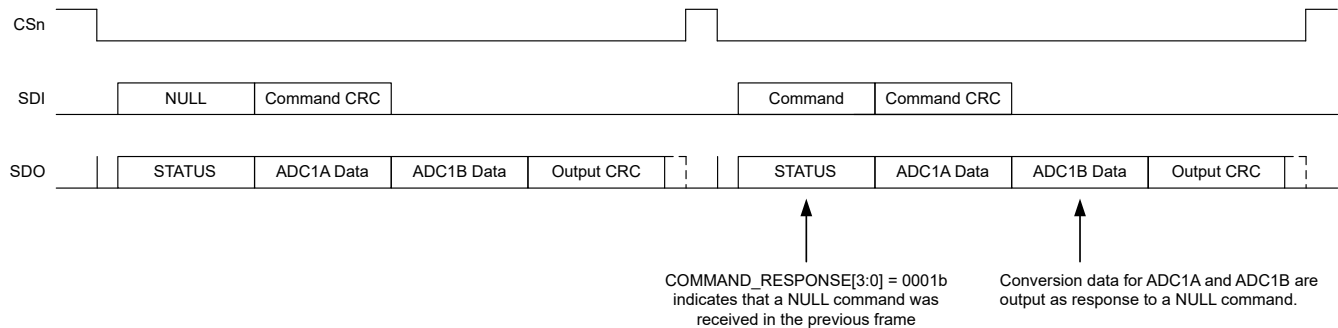
COMMAND	DESCRIPTION	COMMAND WORD
NULL	No operation	0000 0000 0000 0000b
RESET	Reset the device	0000 0000 0001 0001b
LOCK	Lock the interface such that only the NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101b
UNLOCK	Unlock the interface after the interface is locked	0000 0110 0101 0101b
WREG	Write <i>nnn</i> plus 1 registers beginning at address <i>a aaaa aaa</i>	011a aaaa aaa0 0nnnb
RREG	Read <i>n nnnn</i> plus 1 registers beginning at address <i>a aaaa aaa</i>	101a aaaa aaaa nnnnb

**9.5.1.2.5.1 NULL (0000 0000 0000 0000b)**

The NULL command is the *no-operation* command that results in no registers being read or written, and the state of the device remains unchanged. The intended use case for the NULL command is to read out conversion data for ADC1A and ADC1B.

The command response in the next frame indicates if an error occurred during the transmission of the NULL command frame. However, a NULL command is executed regardless if an error occurred or not.

图 9-31 shows a typical NULL command frame where no faults occurred during the communication.



**图 9-31. NULL Command Frame**

### 9.5.1.2.5.2 RESET (0000 0000 0001 0001b)

The RESET command resets the device and sets all user registers to the respective default values. The command is latched by the device at the last SCLK falling edge of the output CRC word. Terminating the frame before the output CRC word is shifted out on SDO causes the RESET command to be ignored. A reset occurs immediately after the command is latched. The DRDYn pin transitions low at the same instance. The host must wait for  $t_{REGACQ}$  after reset or for the DRDYn rising edge to make sure the device completes the reset process before communicating with the device.

The RESETn status bit and the command response in the next frame indicate if the RESET command executed successfully or if an error occurred that prevented the RESET command from executing. A NULL command is executed if the RESET command did not execute.

Figure 9-32 shows a RESET command frame where no faults occurred during the communication.

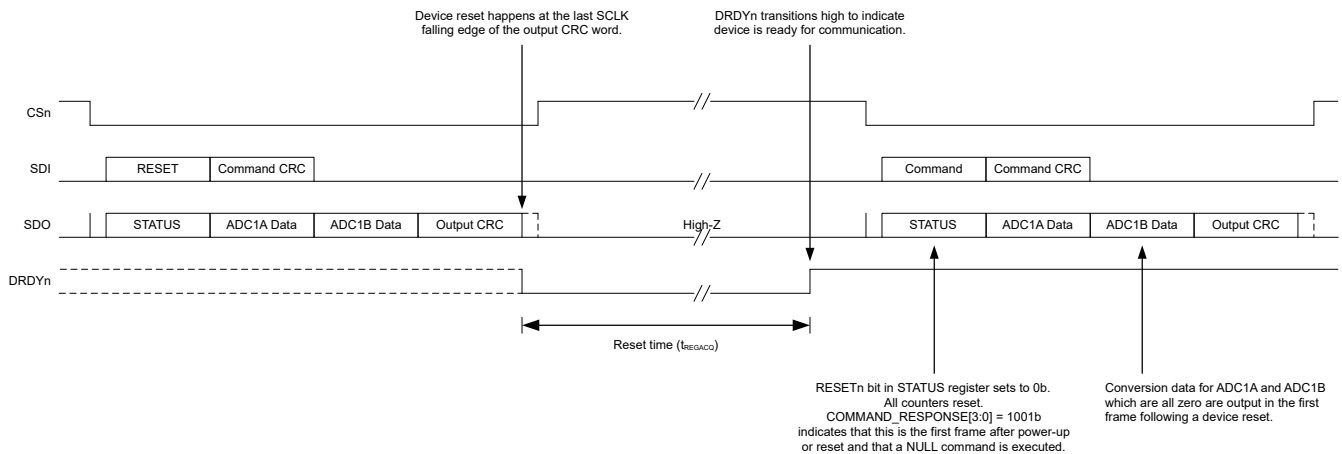


Figure 9-32. RESET Command Frame

### 9.5.1.2.5.3 LOCK (0000 0101 0101 0101b)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the NULL, RREG, and UNLOCK commands. The device continues to output conversion data even when locked.

The LOCK status bit and the command response in the next frame indicate if the LOCK command executed successfully or if an error occurred that prevented the LOCK command from executing. A NULL command is executed if the LOCK command did not execute.

Figure 9-33 shows a LOCK command frame where no faults occurred during the communication.

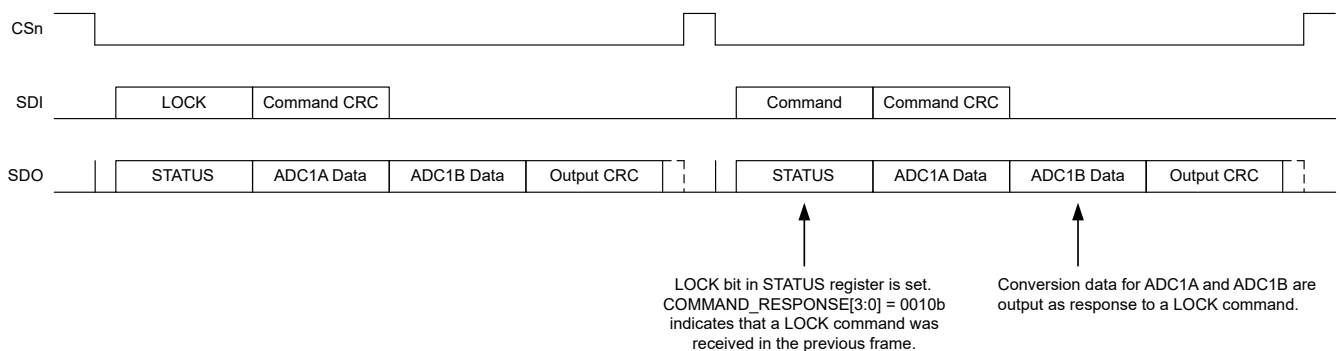


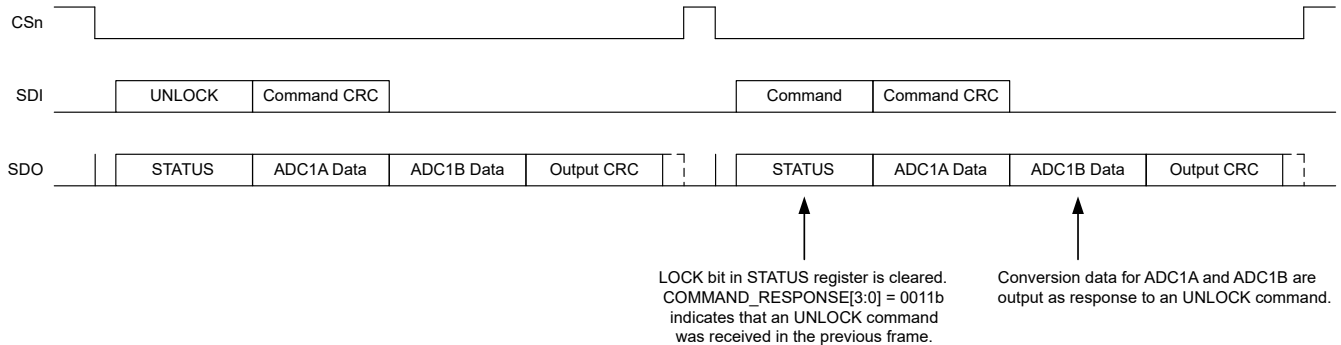
Figure 9-33. LOCK Command Frame

#### 9.5.1.2.5.4 UNLOCK (0000 0110 0101 0101b)

The UNLOCK command unlocks the interface if previously locked by the LOCK command.

The LOCK status bit and the command response in the next frame indicate if the UNLOCK command executed successfully or if an error occurred that prevented the UNLOCK command from executing. A NULL command is executed if the UNLOCK command did not execute.

 9-34 shows an UNLOCK command frame where no faults occurred during the communication.




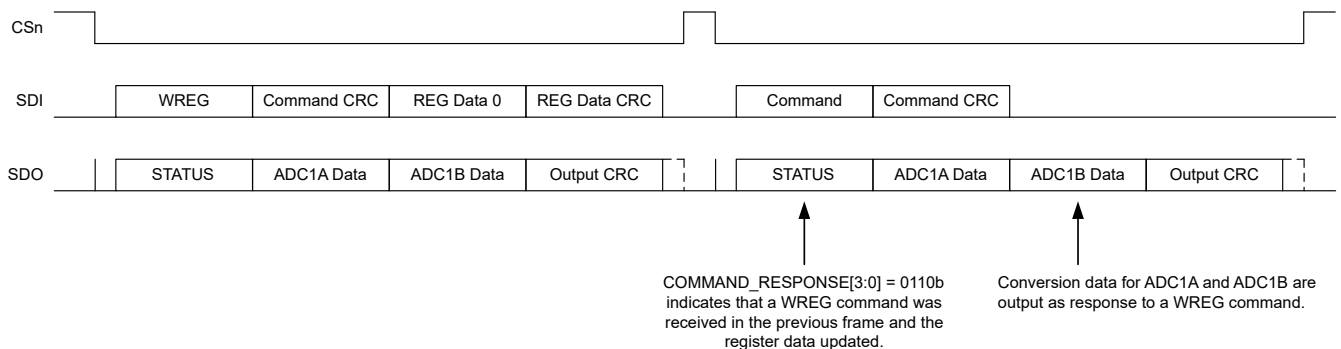
 9-34. UNLOCK Command Frame

#### 9.5.1.2.5.5 WREG (011a aaaa aaa0 0nnnb)

The WREG command is used to write the device registers. The binary format of the command word is 011a aaaa aaa0 0nnn, where a aaaa aaa is the binary address of the register to begin writing to and nnn is the unsigned binary number of consecutive registers to write minus one. Send the register data to be written immediately following the WREG command CRC word. Write the intended contents of each register into individual words, MSB aligned. Follow the register data words with the register data CRC word that covers the register data content.

The device prevents register data writes if the command CRC or register data CRC fail. The command response in the next frame indicates if the WREG command executed successfully or if an error occurred that prevented the WREG command from executing. A NULL command is executed if the WREG command did not execute.

 9-35 shows a WREG command frame for a single register write where no faults occurred during the communication.



 9-35. WREG Command Frame (Single Register)

Figure 9-36 shows a WREG command frame where the number of registers to write is larger than one and, therefore, the frame extends beyond the regular four words.

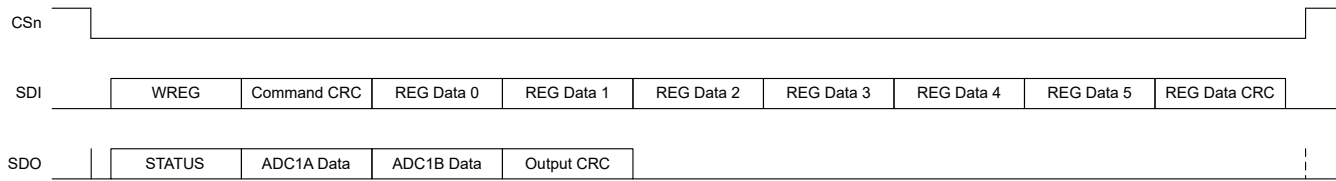


Figure 9-36. WREG Command Frame (Six Registers)

#### 9.5.1.2.5.6 RREG (101a aaaa aaan nnnnb)

RREG is used to read the device registers. The binary format of the command word is 101a aaaa aaan nnnn, where a aaaa aaa is the binary address of the register to begin reading from and n nnnn is the unsigned binary number of consecutive registers to read minus one. The device outputs the requested register data sequentially in order of addresses in the following frame instead of the conversion data of ADC1A and ADC1B. If more than two registers are read, the frame extends beyond the regular four words.

Send the NULL command in the frame following the RREG command frame to shift out the register data. No other command is accepted in the frame following the RREG command frame.

The 16-bit register data are MSB aligned within the individual words. As illustrated in Figure 9-30, the device outputs the respective 8-bit register address following the register data within each word for traceability. When reading from an invalid register address, the device responds with 0000h for the register data and 00h for the register address.

The command response in the frame following the RREG command frame indicates if the RREG command executed successfully or if an error occurred that prevented the RREG command from executing. A NULL command is executed if the RREG command did not execute.

Figure 9-37 shows a RREG command frame where no faults occurred during the communication.

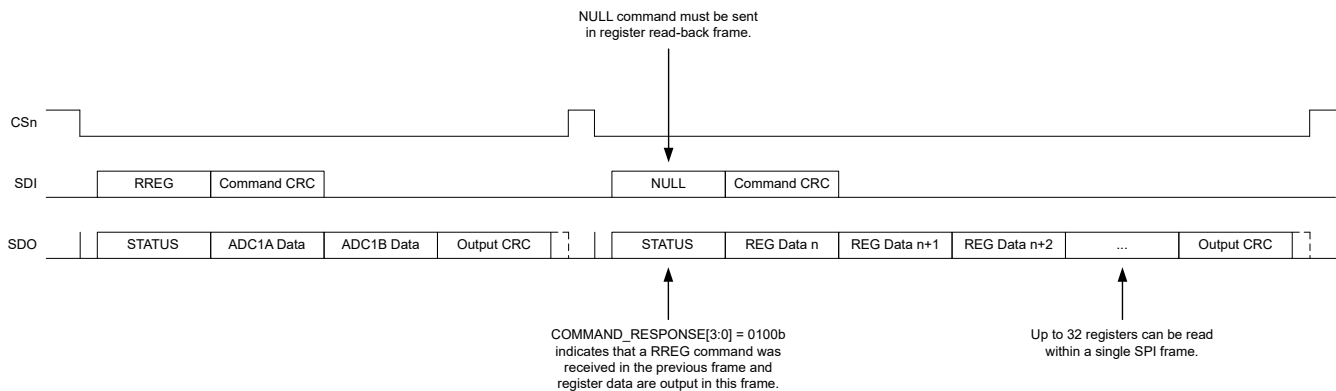


Figure 9-37. RREG Command Frame

#### 9.5.1.2.6 SCLK Counter

The ADS131B23-Q1 implements an SCLK counter that counts the received SCLK pulses within a frame. If the number of received SCLK pulses does not match the number of SCLKs to complete a specific frame, then the SCLK\_COUNT\_FAULTn flag is set in the following frame. Enable or disable the SCLK counter using the SCLK\_COUNTER\_EN bit.

The device determines the number of SCLKs expected for a specific SPI frame at the end of the command CRC word. Both the expected number of words to be received on SDI and the words to be transmitted on SDO are considered in the SCLK count calculation. The larger of the two values determines the SCLK count for the frame. For example, the SCLK count in the two frames in [Figure 9-35](#) is  $(4 \times N_{\text{WORD\_LENGTH}})$ , while in [Figure 9-36](#) the SCLK count for the frame is  $(9 \times N_{\text{WORD\_LENGTH}})$ . The data word length,  $N_{\text{WORD\_LENGTH}}$ , is either 24 or 32, as configured by the WORD\_LENGTH bit.

Sending more SCLK pulses than required to complete a frame does not impact the SPI communication, however the SCLK\_COUNT\_FAULTn does still set in that case to indicate that too many SCLKs were received.

Sending insufficient SCLK pulses to complete a frame does impact the SPI communication in certain situations:

- NULL command: No effect.
- RESET command: Does not execute until sufficient SCLK pulses are provided to clock out the complete output CRC word on SDO.
- LOCK, UNLOCK, RREG commands: Do execute if at least the command and command CRC words are received on SDI.
- WREG command: Does execute if at least the command, command CRC, register data, and register data CRC words are received on SDI.
- DRDYn pin: The DRDYn pin only transitions high after the conversion data word for ADC1B is clocked out on SDO. Otherwise, the device assumes the host did not receive the latest conversion data and the DRDYn pin stays low.

#### 9.5.1.2.7 SPI Timeout

The ADS131B23-Q1 implements an SPI timeout feature that measures the time between the CSn falling and CSn rising edge within a frame. If the CSn rising edge does not occur within the SPI timeout period ( $t_{\text{TIMEOUT}}$ ) after the CSn falling edge, then the SPI\_TIMEOUTn flag is set in the following frame. When a timeout occurs, the rest of the SPI frame on SDI is ignored before the rising edge of CSn. A new SPI transaction starts at the next CSn falling edge. Enable or disable the SPI timeout using the TIMEOUT\_EN bit.

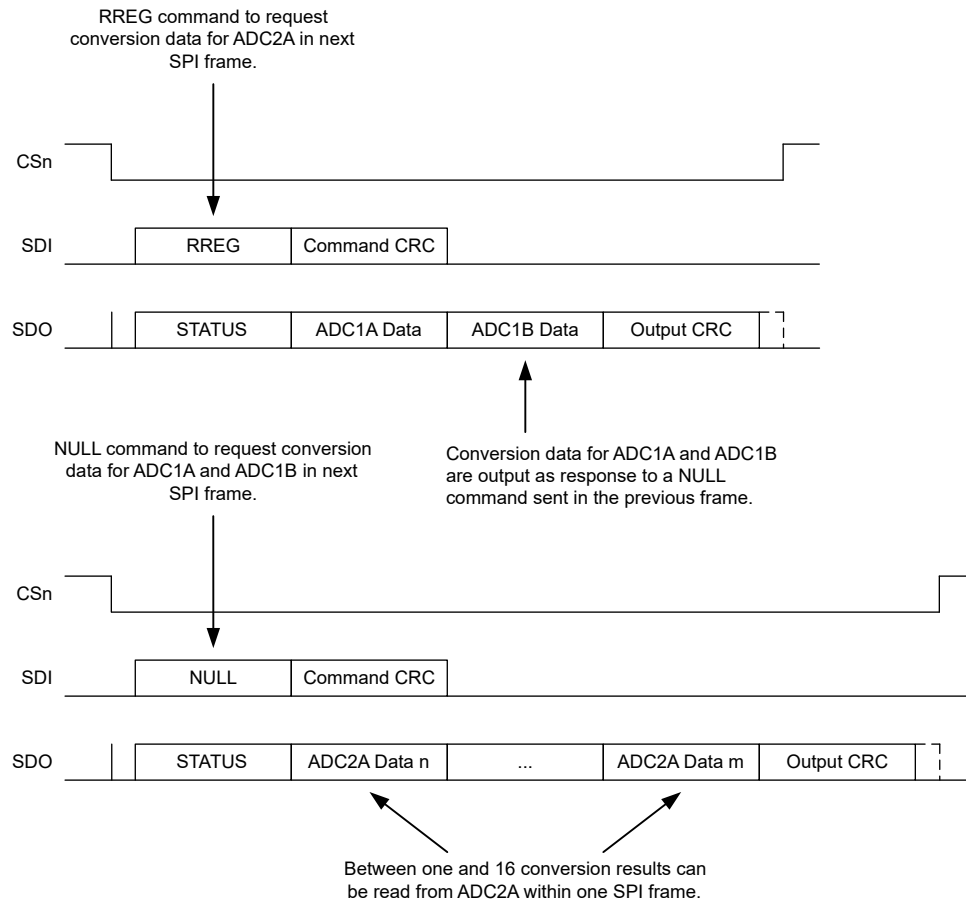
If the SPI times out after a complete frame was transmitted on SDI and SDO already, then there is no impact to the SPI communication, however the SPI\_TIMEOUTn flag does still set in that case to indicate that the CSn signal was held low for too long.

If the SPI times out before a complete frame is transmitted on SDI and SDO, then there is potential impact to the SPI communication in certain situations:

- NULL command: No effect.
- RESET command: Does not execute until the complete output CRC word is clocked out on SDO before the SPI times out.
- LOCK, UNLOCK, RREG commands: Do execute if at least the command and command CRC words are received on SDI before the SPI times out.
- WREG command: Does execute if at least the command, command CRC, register data, and register data CRC words are received on SDI before the SPI times out.
- DRDYn pin: The DRDYn pin only transitions high after the conversion data word for ADC1B is clocked out on SDO before the SPI times out. Otherwise, the device assumes the host did not receive the latest conversion data and the DRDYn pin stays low.

### 9.5.1.2.8 Reading ADC1A, ADC1B, and ADC2A Conversion Data

Conversion data from all three ADCs of the ADS131B23-Q1 can be read within two SPI frames. Conversion data for ADC1A and ADC1B are always output as the response to a NULL command in the following SPI frame. Conversion data for ADC2A must be read from the user registers using the RREG command. The conversion results for the various sequence steps of ADC2A are stored in consecutive register address locations starting at register address 10h. The RREG command allows to read up to 32 consecutive registers within one SPI frame, which is sufficient to read conversion data for all sequence steps of ADC2A. [Figure 9-38](#) shows an SPI frame sequence example of how to read all ADC conversion data.



**Figure 9-38. Reading Conversion Data From ADC1A, ADC1B, and ADC2A Within Two SPI Frames**

### 9.5.1.2.9 DRDYn Pin Behavior

This section provides details about the DRDYn pin behavior in various scenarios.

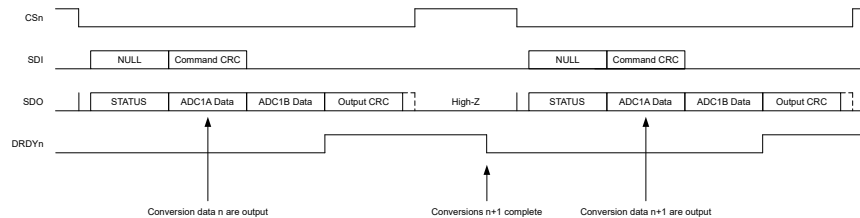
DRDYn transitions low whenever new conversion data complete on ADC1A or ADC1B, depending on which ADC drives the DRDYn signal as configured in the DRDY\_CTRL bit. If DRDYn is low when a new conversion completes on ADC1y, then DRDYn drives high  $t_{w(DRH)}$  before the DRDYn falling edge (see [9-40](#) and [9-42](#)).

DRDYn transitions high after the conversion data for ADC1B are retrieved on SDO ([9-39](#)). If CSn is driven high before the ADC1B conversion data are retrieved, then DRDYn stays low, indicating that not all conversion data were read ([9-40](#) and [9-41](#)).

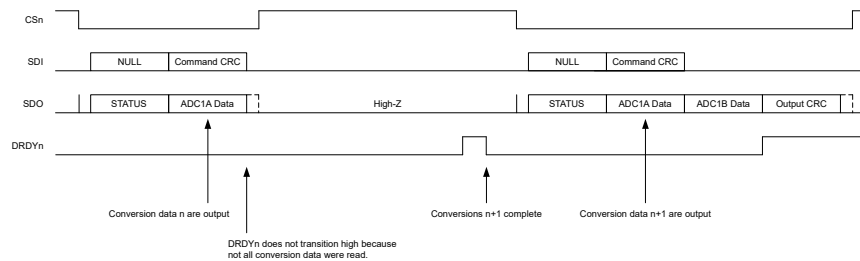
[9-41](#) shows that the same conversion data can be read multiple times until new conversions complete. The ADC1y conversion counters indicate if the same data were read again or if new data were read.

The device avoids data corruption if new conversions n+1 complete while conversion data n are being read. Conversion data n+1 are held in an internal buffer until the read of conversion data n is complete. In the following frame, conversion data n+1 are loaded into the SDO output buffer. DRDYn does not transition high after conversion data n have been read in this case to indicate that new conversion data n+1 are available for readout (see [9-42](#)).

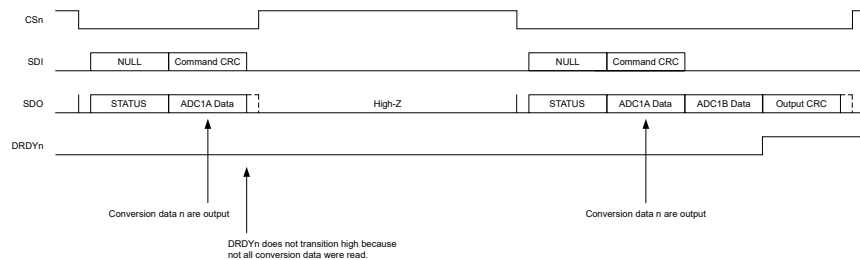
[9-43](#) illustrates that conversion data n+1 are lost when the host does not read the data before conversions n+2 complete. The ADC1y conversion counters are helpful in this situation to detect if the host missed reading the intermediate conversion results.



**9-39. DRDYn Pin Behavior: Reading All Conversion Data Before New Conversions Complete**

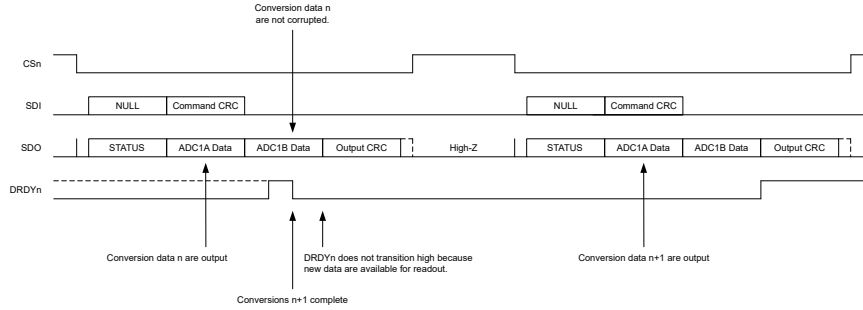


**9-40. DRDYn Pin Behavior: Incomplete Read of Conversion Data Before New Conversions Complete**

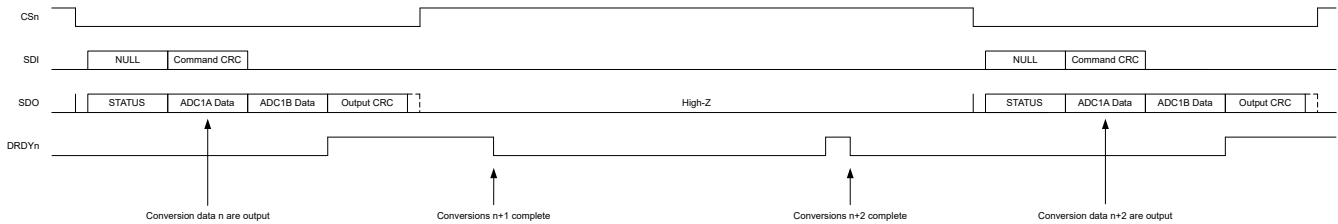


**9-41. DRDYn Pin Behavior: Incomplete Read of Conversion Data Followed by Complete Read of Same Conversion Data**



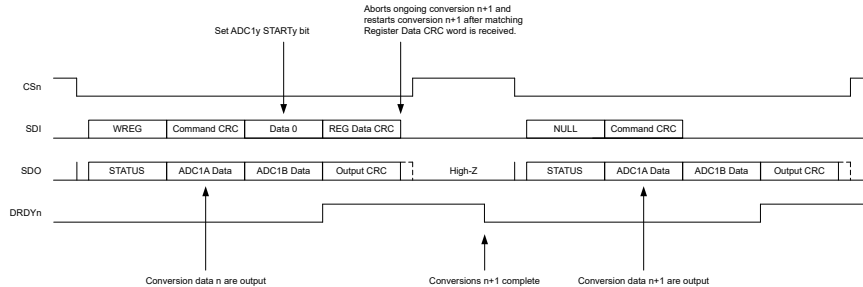


9-42. DRDYn Pin Behavior: Reading Conversion Data While New Conversions Complete

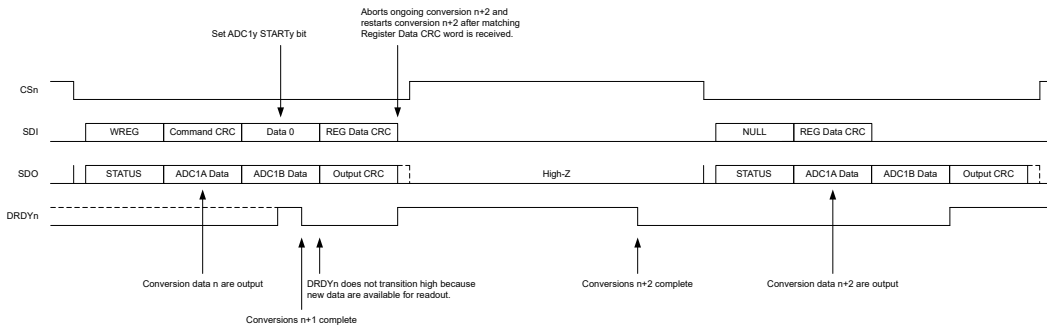


9-43. DRDYn Pin Behavior: Missed Reading Intermediate Conversion Results

Setting the STARTy bit drives the DRDYn pin high at the last SCLK falling edge of the register data CRC word within the SPI frame where the CONVERSION\_CTRL register is written. However, the old conversion data can still be read until the new conversions become available. 9-44 shows the device behavior when setting the STARTy bit to abort an ongoing conversion and to restart new conversions while reading out conversion data. 9-45 shows a scenario where new conversions complete while setting the STARTy bit and reading out conversion data.



9-44. DRDYn Pin Behavior: Setting the STARTy Bit While Reading Conversion Data



9-45. DRDYn Pin Behavior: Setting the STARTy Bit and Reading Conversion Data While New Conversions Complete

## 9.6 Register Map

The ADS131B23-Q1 register map spans across the address space from 00h to FEh and is divided into four general sections:

- Section 0 (address space: 00h to 1Fh): Only includes read-only bits (such as ID, status, GPIO input data, ADC2y conversion data, and the conversion and sequence control bits)
- Section 1 (address space: 40h to 7Eh): Includes global device configuration bits that are not specific to section A or B of the device
- Section 2 (address space: 80h to BEh): Includes device configuration bits that are specific to section A
- Section 3 (address space: C0h to FEh): Includes device configuration bits that are specific to section B

## 9.6.1 Registers

表 9-26 lists the memory-mapped registers for the Registers registers. All register offset addresses not listed in 表 9-26 should be considered as reserved locations and the register contents should not be modified.

**表 9-26. Register Map**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
<b>SECTION 0</b>											
00h	ID	X	REV[7:0]								
			ADC_COUNT[2:0]				DEVICE_ID[4:0]				
01h	STATUS_MSB	7FC8h	RESETn	SUPPLY_FAULTn	CLOCK_FAULTn	DIGITAL_FAULTn	OCC_FAULTn	SPI_CRC_FAULTn	SPI_TIMEOUTn	SCLK_COUNT_FAULTn	
			REG_ACCESS_FAULTn	COMMAND_RESPONSE[3:0]				LOCK	CLOCK	MODE	
02h	STATUS_LSB	0000h	SEQ2A_COUNT[1:0]		RESERVED		CONV1A_COUNT[1:0]		CONV1B_COUNT[1:0]		
			RESERVED							SEQ2A_ACTIVATE	RESERVED
03h	SUPPLY_STATUS	FFFFh	AVDD_OVn	AVDD_UVn	IOVDD_OVn	IOVDD_UVn	DVDD_OVn	DVDD_UVn	AVDD_OSCn	IOVDD_OSCn	
			DVDD_OSCn	AVDD_OTWn	IOVDD_OTWn	AVDD_CLn	IOVDD_CLn	AGNDA_DISCn	AGNDB_DISCn	DGND_DISCn	
04h	CLOCK_STATUS	FC07h	RESERVED								
			RESERVED						MCLK_FAULTn	OSCD_WDn	MCLK_WDn
05h	DIGITAL_STATUS	EC00h	REG_MAP1_CRC_FAULTn	REG_MAP2_CRC_FAULTn	REG_MAP3_CRC_FAULTn	RESERVED	MEM_MAP_CRC_FAULTn	OTP_BANK	RESERVED		
			RESERVED								
06h	OCC_STATUS	000Fh	RESERVED								
			RESERVED				OCCA_HTn	OCCA_LTn	OCCB_HTn	OCCB_LTn	
07h	GPI_DATA	0000h	RESERVED							GPI4_DAT[1:0]	
			GPI3_DAT[1:0]		GPI2_DAT[1:0]		GPI1_DAT[1:0]		GPI0_DAT[1:0]		
08h	GPIA_GPIB_DATA	0000h	RESERVED				GPI1A_DAT[1:0]		GPI0A_DAT[1:0]		
			RESERVED				GPI1B_DAT[1:0]		GPI0B_DAT[1:0]		
09h	CONVERSION_CTRL	0000h	RESERVED	STARTA	RESERVED	STARTB	RESERVED	STOPA	RESERVED	STOPB	
			RESERVED	SEQ2A_START	RESERVED				SEQ2A_STOP	RESERVED	
10h	SEQ2A_STEP0_DATA	0000h	SEQ2A_STEP0_DAT[15:0]								
11h	SEQ2A_STEP1_DATA	0000h	SEQ2A_STEP1_DAT[15:0]								
12h	SEQ2A_STEP2_DATA	0000h	SEQ2A_STEP2_DAT[15:0]								
13h	SEQ2A_STEP3_DATA	0000h	SEQ2A_STEP3_DAT[15:0]								
14h	SEQ2A_STEP4_DATA	0000h	SEQ2A_STEP4_DAT[15:0]								
15h	SEQ2A_STEP5_DATA	0000h	SEQ2A_STEP5_DAT[15:0]								
16h	SEQ2A_STEP6_DATA	0000h	SEQ2A_STEP6_DAT[15:0]								
17h	SEQ2A_STEP7_DATA	0000h	SEQ2A_STEP7_DAT[15:0]								
18h	SEQ2A_STEP8_DATA	0000h	SEQ2A_STEP8_DAT[15:0]								
19h	SEQ2A_STEP9_DATA	0000h	SEQ2A_STEP9_DAT[15:0]								
1Ah	SEQ2A_STEP10_DATA	0000h	SEQ2A_STEP10_DAT[15:0]								
1Bh	SEQ2A_STEP11_DATA	0000h	SEQ2A_STEP11_DAT[15:0]								
1Ch	SEQ2A_STEP12_DATA	0000h	SEQ2A_STEP12_DAT[15:0]								

**表 9-26. Register Map (continued)**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
1Dh	SEQ2A_STEP13_DATA	0000h	SEQ2A_STEP13_DAT[15:0]									
1Eh	SEQ2A_STEP14_DATA	0000h	SEQ2A_STEP14_DAT[15:0]									
1Fh	SEQ2A_STEP15_DATA	0000h	SEQ2A_STEP15_DAT[15:0]									
<b>SECTION 1</b>												
40h	DEVICE_MONITOR_CFG	0000h	REG_MAP1_CRC_EN	CRC_TYPE	SCLK_COUNT_ER_EN	TIMEOUT_EN	RESERVED			FAULT_POL		
41h	SUPPLY_MONITOR_CFG1	0000h	AVDD_OV_EN	AVDD_UV_EN	IOVDD_OV_EN	IOVDD_UV_EN	DVDD_OV_EN	DVDD_UV_EN	AVDD_OSC_EN	IOVDD_OSC_EN		
42h	SUPPLY_MONITOR_CFG2	10F0h	RESERVED		IOVDD_OTW_TH	IOVDD_UV_TH	RESERVED					
43h	CLOCK_MONITOR_CFG	0000h	RESERVED							MCLK_MON_EN	OSCD_WD_EN	MCLK_WD_EN
44h	SUPPLY_MONITOR_DIAGNOSTIC_CFG	0000h	AVDD_OV_DIAG_EN	AVDD_UV_DIAG_EN	IOVDD_OV_DIAG_EN	IOVDD_UV_DIAG_EN	DVDD_OV_DIAG_EN	DVDD_UV_DIAG_EN	AVDD_OSC_DIAG_EN	IOVDD_OSC_DIAG_EN		
45h	CLOCK_MONITOR_DIAGNOSTIC_CFG	0000h	SPARE[11:0]									
46h	DIGITAL_MONITOR_DIAGNOSTIC_CFG	0000h	RESERVED						MEM_MAP_CRC_DIAG[1:0]			
47h	SUPPLY_FAULT_MASK	0000h	AVDD_OV_MASK	AVDD_UV_MASK	IOVDD_OV_MASK	IOVDD_UV_MASK	DVDD_OV_MASK	DVDD_UV_MASK	AVDD_OSC_MASK	IOVDD_OSC_MASK		
48h	CLOCK_FAULT_MASK	0000h	RESERVED							MCLK_FAULT_MASK	OSCD_WD_MASK	MCLK_WD_MASK
49h	DIGITAL_FAULT_MASK	0000h	REG_MAP1_CRC_FAULT_MASK	REG_MAP2_CRC_FAULT_MASK	REG_MAP3_CRC_FAULT_MASK	RESERVED	MEM_MAP_CRC_FAULT_MASK	RESERVED				
4Ah	OCC_FAULT_MASK	0000h	RESERVED							OCCA_HT_MASK	OCCB_HT_MASK	OCCB_LT_MASK
4Bh	FAULT_PIN_MASK	0780h	RESERVED	SUPPLY_FAULT_MASK	CLOCK_FAULT_MASK	DIGITAL_FAULT_MASK	OCC_FAULT_MASK	SPI_CRC_FAULT_MASK	SPI_TIMEOUT_MASK	SCLK_COUNT_FAULT_MASK		
4Ch	DEVICE_CFG	0000h	RESERVED	DRDY_CTRL	RESERVED	CLK_SOURCE	WORD_LENGTH	RESERVED	OP_MODE[1:0]			
4Dh	GPIO_CFG	0000h	RESERVED	GPIO4_FMT	GPIO3_FMT	GPIO2_FMT	GPIO1_FMT	GPIO0_FMT	GPIO4_DIR	GPIO3_DIR		
4Eh	GPO_DATA	0000h	SPARE[10:0]									
4Fh	GPIO0_LL_PWM_CFG	007Fh	GPIO0_PWM_TB[1:0]			GPIO0_LL_PWM_HC[6:0]						
50h	GPIO0_LH_PWM_CFG	3F80h	RESERVED			GPIO0_LH_PWM_HC[6:0]						

**表 9-26. Register Map (continued)**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
51h	GPIO1_LL_PWM_CFG	007Fh	GPIO1_PWM_TB[1:0]		GPIO1_LL_PWM_HC[6:0]						
			GPIO1_LL_PWM_HC[6:0]		GPIO1_LL_PWM_LC[6:0]						
52h	GPIO1_LH_PWM_CFG	3F80h	RESERVED		GPIO1_LH_PWM_HC[6:0]						
			GPIO1_LH_PWM_HC[6:0]		GPIO1_LH_PWM_LC[6:0]						
53h	GPIO2_LL_PWM_CFG	007Fh	GPIO2_PWM_TB[1:0]		GPIO2_LL_PWM_HC[6:0]						
			GPIO2_LL_PWM_HC[6:0]		GPIO2_LL_PWM_LC[6:0]						
54h	GPIO2_LH_PWM_CFG	3F80h	RESERVED		GPIO2_LH_PWM_HC[6:0]						
			GPIO2_LH_PWM_HC[6:0]		GPIO2_LH_PWM_LC[6:0]						
55h	GPIO3_LL_PWM_CFG	007Fh	GPIO3_PWM_TB[1:0]		GPIO3_LL_PWM_HC[6:0]						
			GPIO3_LL_PWM_HC[6:0]		GPIO3_LL_PWM_LC[6:0]						
56h	GPIO3_LH_PWM_CFG	3F80h	RESERVED		GPIO3_LH_PWM_HC[6:0]						
			GPIO3_LH_PWM_HC[6:0]		GPIO3_LH_PWM_LC[6:0]						
57h	GPIO4_LL_PWM_CFG	007Fh	GPIO4_PWM_TB[1:0]		GPIO4_LL_PWM_HC[6:0]						
			GPIO4_LL_PWM_HC[6:0]		GPIO4_LL_PWM_LC[6:0]						
58h	GPIO4_LH_PWM_CFG	3F80h	RESERVED		GPIO4_LH_PWM_HC[6:0]						
			GPIO4_LH_PWM_HC[6:0]		GPIO4_LH_PWM_LC[6:0]						
59h	SPARE_59h	5555h	SPARE[15:0]								
			SPARE[15:0]								
7Eh	REGISTER_MAP1_CRC	0000h	REG_MAP1_CRC_VALUE[15:0]								
			REG_MAP1_CRC_VALUE[15:0]								
<b>SECTION 2</b>											
80h	REGMAP2_TDACA_CFG	0000h	REG_MAP2_CRC_EN	RESERVED							
			RESERVED				TDACA_VALUE[2:0]				
81h	GPIOA_CFG	8000h	RESERVED	SPARE[2:0]			GPIO1A_FMT	GPIO0A_FMT	GPIO1A_DIR	GPIO0A_DIR	
			GPIO1A_PWM_TB[1:0]		GPIO0A_PWM_TB[1:0]		SPARE[1:0]		GPO1A_DAT	GPO0A_DAT	
82h	ADC1A_CFG1	0400h	RESERVED				CONV_MODE1_A	OSR1A[2:0]			
			RESERVED				GC1A_EN	GC1A_DELAY[2:0]			
83h	ADC1A_CFG2	8010h	ADC1A_EN	RESERVED			GAIN1A[1:0]		MUX1A[1:0]		
			RESERVED		OWD1A_SOURCE_MUX	OWD1A_SINK_MUX	OWD1A_SOURCE_VALUE[1:0]		OWD1A_SINK_VALUE[1:0]		
84h	ADC1A_OCAL_MSB	0000h	OCAL1A[23:8]								
			OCAL1A[23:8]								
85h	ADC1A_OCAL_LSB	0000h	OCAL1A[7:0]								
			RESERVED								
86h	ADC1A_GCAL	0000h	GCAL1A[15:0]								
			GCAL1A[15:0]								
87h	OCCA_CFG	0000h	OCCA_EN	OCCA_POL	RESERVED	OCCA_NUM[4:0]					
			RESERVED								
88h	OCCA_HIGH_THRE_SHOLD	7FFFh	OCCA_HIGH_TH[15:0]								
			OCCA_HIGH_TH[15:0]								
89h	OCCA_LOW_THRE_SHOLD	8000h	OCCA_LOW_TH[15:0]								
			OCCA_LOW_TH[15:0]								
8Ah	SPARE_8Ah	5555h	SPARE[15:0]								
			SPARE[15:0]								
8Bh	ADC2A_CFG1	8010h	ADC2A_EN	RESERVED			VCMA_EN	OWD2A_SOURCE_MUX[2:0]			
			OWD2A_SOURCE_MUX[2:0]	OWD2A_SINK_MUX[2:0]			OWD2A_SOURCE_VALUE[1:0]		OWD2A_SINK_VALUE[1:0]		

**表 9-26. Register Map (continued)**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8Ch	ADC2A_CFG2	0000h	SEQ2A_MODE[1:0]		RESERVED			MUX2A_DELAY[2:0]		
			RESERVED						OSR2A[1:0]	
8Dh	SPARE_8Dh	0000h	RESERVED							
			SPARE[7:0]							
8Eh	ADC2A_OCAL	0000h	OCAL2A[15:0]							
			OCAL2A[15:0]							
8Fh	ADC2A_GCAL	0000h	GCAL2A[15:0]							
			GCAL2A[15:0]							
90h	SEQ2A_STEP0_CFG	0000h	SEQ2A_STEP0_EN	SEQ2A_STEP0_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP0_CH_N	SEQ2A_STEP0_CH_P[3:0]			
91h	SEQ2A_STEP1_CFG	0001h	SEQ2A_STEP1_EN	SEQ2A_STEP1_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP1_CH_N	SEQ2A_STEP1_CH_P[3:0]			
92h	SEQ2A_STEP2_CFG	0002h	SEQ2A_STEP2_EN	SEQ2A_STEP2_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP2_CH_N	SEQ2A_STEP2_CH_P[3:0]			
93h	SEQ2A_STEP3_CFG	0003h	SEQ2A_STEP3_EN	SEQ2A_STEP3_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP3_CH_N	SEQ2A_STEP3_CH_P[3:0]			
94h	SEQ2A_STEP4_CFG	0004h	SEQ2A_STEP4_EN	SEQ2A_STEP4_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP4_CH_N	SEQ2A_STEP4_CH_P[3:0]			
95h	SEQ2A_STEP5_CFG	0005h	SEQ2A_STEP5_EN	SEQ2A_STEP5_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP5_CH_N	SEQ2A_STEP5_CH_P[3:0]			
96h	SEQ2A_STEP6_CFG	0006h	SEQ2A_STEP6_EN	SEQ2A_STEP6_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP6_CH_N	SEQ2A_STEP6_CH_P[3:0]			
97h	SEQ2A_STEP7_CFG	0007h	SEQ2A_STEP7_EN	SEQ2A_STEP7_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP7_CH_N	SEQ2A_STEP7_CH_P[3:0]			
98h	SEQ2A_STEP8_CFG	0008h	SEQ2A_STEP8_EN	SEQ2A_STEP8_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP8_CH_N	SEQ2A_STEP8_CH_P[3:0]			
99h	SEQ2A_STEP9_CFG	0009h	SEQ2A_STEP9_EN	SEQ2A_STEP9_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP9_CH_N	SEQ2A_STEP9_CH_P[3:0]			
9Ah	SEQ2A_STEP10_CFG	000Ah	SEQ2A_STEP10_EN	SEQ2A_STEP10_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP10_CH_N	SEQ2A_STEP10_CH_P[3:0]			
9Bh	SEQ2A_STEP11_CFG	000Bh	SEQ2A_STEP11_EN	SEQ2A_STEP11_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP11_CH_N	SEQ2A_STEP11_CH_P[3:0]			
9Ch	SEQ2A_STEP12_CFG	000Ch	SEQ2A_STEP12_EN	SEQ2A_STEP12_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP12_CH_N	SEQ2A_STEP12_CH_P[3:0]			
9Dh	SEQ2A_STEP13_CFG	000Dh	SEQ2A_STEP13_EN	SEQ2A_STEP13_GAIN[1:0]		RESERVED				
			RESERVED			SEQ2A_STEP13_CH_N	SEQ2A_STEP13_CH_P[3:0]			

**表 9-26. Register Map (continued)**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
9Eh	SEQ2A_STEP14_CFG	000Eh	SEQ2A_STEP14_EN	SEQ2A_STEP14_GAIN[1:0]		RESERVED					
			RESERVED			SEQ2A_STEP14_CH_N	SEQ2A_STEP14_CH_P[3:0]				
9Fh	SEQ2A_STEP15_CFG	000Fh	SEQ2A_STEP15_EN	SEQ2A_STEP15_GAIN[1:0]		RESERVED					
			RESERVED			SEQ2A_STEP15_CH_N	SEQ2A_STEP15_CH_P[3:0]				
A0h	SPARE_A0h	0210h	RESERVED				SPARE[1:0]		RESERVED		
			RESERVED		SPARE[1:0]		RESERVED				
A1h	SPARE_A1h	0000h	SPARE[15:0]								
A2h	SPARE_A2h	0000h	SPARE[15:0]								
A3h	SPARE_A3h	0000h	SPARE[7:0]								
			RESERVED								
BEh	REGISTER_MAP2_CRC	0000h	SPARE[15:0]								
			SPARE[15:0]								
<b>SECTION 3</b>											
C0h	REGMAP3_TDACC_CFG	0000h	REG_MAP3_RC_EN	RESERVED							
			RESERVED					TDACB_VALUE[2:0]			
C1h	GPIOB_CFG	8000h	RESERVED	SPARE[2:0]			GPIO1B_FMT	GPIO0B_FMT	GPIO1B_DIR	GPIO0B_DIR	
			GPIO1B_PWM_TB[1:0]		GPIO0B_PWM_TB[1:0]		SPARE[1:0]		GPO1B_DAT	GPO0B_DAT	
C2h	ADC1B_CFG1	0400h	RESERVED				CONV_MODE1_B	OSR1B[2:0]			
			RESERVED				GC1B_EN	GC1B_DELAY[2:0]			
C3h	ADC1B_CFG2	8010h	ADC1B_EN	RESERVED			GAIN1B[1:0]		MUX1B[1:0]		
			RESERVED		OWD1B_SOURCE_MUX	OWD1B_SINK_MUX	OWD1B_SOURCE_VALUE[1:0]		OWD1B_SINK_VALUE[1:0]		
C4h	ADC1B_OCAL_MSB	0000h	OCAL1B[23:8]								
			OCAL1B[23:8]								
C5h	ADC1B_OCAL_LSB	0000h	OCAL1B[7:0]								
			RESERVED								
C6h	ADC1B_GCAL	0000h	GCAL1B[15:0]								
			GCAL1B[15:0]								
C7h	OCCB_CFG	0000h	OCCB_EN	OCCB_POL	RESERVED	OCCB_NUM[4:0]					
			RESERVED								
C8h	OCCB_HIGH_THRE_SHOLD	7FFFh	OCCB_HIGH_TH[15:0]								
			OCCB_HIGH_TH[15:0]								
C9h	OCCB_LOW_THRE_SHOLD	8000h	OCCB_LOW_TH[15:0]								
			OCCB_LOW_TH[15:0]								
CAh	SPARE_CAh	5555h	SPARE[15:0]								
			SPARE[15:0]								
CBh	SPARE_CBh	0010h	RESERVED						SPARE[6:0]		
			SPARE[6:0]			RESERVED			RESERVED		
CCh	SPARE_CCh	0000h	SPARE[1:0]		RESERVED				SPARE[2:0]		
			RESERVED						SPARE[1:0]		
CDh	SPARE_CDh	0000h	RESERVED								
			SPARE[7:0]								
CEh	SPARE_Ceh	0000h	SPARE[15:0]								
			SPARE[15:0]								
CFh	SPARE_CFh	0000h	SPARE[15:0]								
			SPARE[15:0]								
D0h	SPARE_D0h	0000h	SPARE[2:0]				RESERVED				
			RESERVED				SPARE[4:0]				

**表 9-26. Register Map (continued)**

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D1h	SPARE_D1h	0001h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D2h	SPARE_D2h	0002h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D3h	SPARE_D3h	0003h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D4h	SPARE_D4h	0004h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D5h	SPARE_D5h	0005h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D6h	SPARE_D6h	0006h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D7h	SPARE_D7h	0007h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D8h	SPARE_D8h	0008h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
D9h	SPARE_D9h	0009h	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DAh	SPARE_DAh	000Ah	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DBh	SPARE_DBh	000Bh	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DCh	SPARE_DCh	000Ch	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DDh	SPARE_DDh	000Dh	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DEh	SPARE_DEh	000Eh	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
DFh	SPARE_DFh	000Fh	SPARE[2:0]			RESERVED				
			RESERVED			SPARE[4:0]				
E0h	SPARE_E0h	0210h	RESERVED				SPARE[1:0]		RESERVED	
			RESERVED		SPARE[1:0]		RESERVED			
E1h	SPARE_E1h	0000h	SPARE[15:0]							
			SPARE[15:0]							
E2h	SPARE_E2h	0000h	SPARE[7:0]							
			RESERVED							
E3h	SPARE_E3h	0000h	SPARE[15:0]							
			SPARE[15:0]							
FEh	REGISTER_MAP3_CRC	0000h	REG_MAP3_CRC_VALUE[15:0]							
			REG_MAP3_CRC_VALUE[15:0]							



### 9.6.1.1 ID Register (Address = 00h) [Reset = X]

Return to the [Summary Table](#).

**图 9-46. ID Register**

15	14	13	12	11	10	9	8
REV[7:0]							
R-X							
7	6	5	4	3	2	1	0
ADC_COUNT[2:0]				DEVICE_ID[4:0]			
R-011b				R-X			

**表 9-27. ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	REV[7:0]	R	X	Revision ID Values are subject to change without notice
7:5	ADC_COUNT[2:0]	R	011b	ADC count 011b = 3 (ADC1A, ADC1B, ADC2A)
4:0	DEVICE_ID[4:0]	R	X	Device ID Values are subject to change without notice

### 9.6.1.2 STATUS\_MSB Register (Address = 01h) [Reset = 7FC8h]

Return to the [Summary Table](#).

**图 9-47. STATUS\_MSB Register**

15		14		13		12		11		10		9		8	
RESETh		SUPPLY_FAULTn		CLOCK_FAULTn		DIGITAL_FAULTn		OCC_FAULTn		SPI_CRC_FAULTn		SPI_TIMEOUTn		SCLK_COUNT_FAULTn	
R/W-0b		R/W-1b		R/W-1b		R/W-1b		R/W-1b		R-1b		R-1b		R-1b	
7		6		5		4		3		2		1		0	
REG_ACCESS_FAULTn		COMMAND_RESPONSE[3:0]								LOCK		CLOCK		MODE	
R-1b		R-1001b								R-0b		R-0b		R-0b	

**表 9-28. STATUS\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESETh	R/W	0b	RESET flag Indicates a device reset occurred. Write 1b to clear this bit to 1b. 0b = Reset occurred 1b = No reset occurred
14	SUPPLY_FAULTn	R/W	1b	Supply fault flag Indicates that one or more of the unmasked supply fault flags in the SUPPLY_STATUS register is set. Write 1b to clear this bit to 1b after all set unmasked supply fault flags are cleared. 0b = One or more of the unmasked supply fault flags is set 1b = None of the unmasked supply fault flags are set
13	CLOCK_FAULTn	R/W	1b	Clock fault flag Indicates that one or more of the unmasked clock fault flags in the CLOCK_STATUS register is set. Write 1b to clear this bit to 1b after all set unmasked clock fault flags are cleared. 0b = One or more of the unmasked clock fault flags is set 1b = None of the unmasked supply clock fault flags are set
12	DIGITAL_FAULTn	R/W	1b	Digital fault flag Indicates that one or more of the unmasked digital fault flags in the DIGITAL_STATUS register is set. Write 1b to clear this bit to 1b after all set unmasked digital fault flags are cleared. 0b = One or more of the unmasked digital fault flags is set 1b = None of the unmasked digital fault flags are set
11	OCC_FAULTn	R/W	1b	Overcurrent comparator fault flag Indicates that one or more of the unmasked overcurrent comparator fault flags in the OCC_STATUS register is set. Write 1b to clear this bit to 1b after all set unmasked overcurrent comparator fault flags are cleared. 0b = One or more of the unmasked overcurrent comparator fault flags is set 1b = None of the unmasked overcurrent comparator fault flags are set
10	SPI_CRC_FAULTn	R	1b	SPI CRC fault flag Indicates an SPI CRC fault occurred in the previous SPI frame. This bit clears automatically to 1b in each new SPI frame. 0b = SPI CRC fault occurred 1b = No SPI CRC fault occurred
9	SPI_TIMEOUTn	R	1b	SPI timeout fault flag Indicates an SPI timeout fault occurred in the previous SPI frame. This bit clears automatically to 1b in each new SPI frame. 0b = SPI timeout fault occurred 1b = No SPI timeout fault occurred
8	SCLK_COUNT_FAULTn	R	1b	SCLK counter fault flag Indicates an SCLK counter fault occurred in the previous SPI frame (that is, fewer or more SCLKs than required for the previous frame were sent). This bit clears automatically to 1b in each new SPI frame. 0b = SCLK counter fault occurred 1b = No SCLK counter fault occurred
7	REG_ACCESS_FAULTn	R	1b	Register access fault flag Indicates a read or write access to an invalid register address (register address FFh or beyond) occurred. This flag sets to 0b in the subsequent frame following the frame where a read or write operation to a register with an invalid register address was attempted. This bit clears automatically to 1b in each new SPI frame. 0b = Register access fault occurred 1b = No register access fault occurred

**表 9-28. STATUS\_MSB Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
6:3	COMMAND_RESPONSE[3:0]	R	1001b	<p>Command response indication Indicates which command was executed in the previous SPI frame.</p> <p>0000b = Invalid response that does not occur under normal circumstances. Can indicate a stuck-at SDO signal or that the device is held in reset.</p> <p>0001b = NULL command 0010b = LOCK command 0011b = UNLOCK command 0100b = RREG command 0101b = NULL command (because a NULL command was correctly sent as the second frame after a RREG command). This response serves as the frame counter for the two-frame RREG command. 0110b = WREG command 0111b = Invalid response that does not occur under normal circumstances. 1000b = Invalid response that does not occur under normal circumstances. 1001b = NULL command (first frame after power-up or reset). This response is only sent in the first frame after reset or power-up, the second frame has the response based on the command sent in the first frame. 1010b = NULL command (resulting from one of the following errors: a timeout occurred before a complete command CRC was received, insufficient SCLKs were sent to complete a command, a CRC mismatch between the command word and command CRC word, or a CRC mismatch between data words and the data CRC word in a WREG command). For the NULL, RREG, LOCK, and UNLOCK commands, the command and command CRC words must be sent to complete the command. For the RESET command, the STATUS word, all ADC data words, and the output CRC word must be read to complete the command. For the WREG command, the command and command CRC words, as well as the data and data CRC words must be sent to complete the command. 1011b = NULL command (resulting from an invalid command word with a matching CRC between the command word and command CRC word). 1100b = NULL command (resulting from a command other than the NULL command was sent in the second frame after the RREG command and ignored). This response serves as the frame counter for the two-frame RREG command. 1101b = NULL command (the RESET or WREG commands are ignored because the device is locked). 1110b = Invalid response that does not occur under normal circumstances. 1111b = Invalid response that does not occur under normal circumstances. Can indicate a stuck-at SDO signal.</p>
2	LOCK	R	0b	<p>Lock state indication Indicates if the device is locked or unlocked.</p> <p>0b = Device is unlocked 1b = Device is locked</p>
1	CLOCK	R	0b	<p>Clock source indication Indicates which clock source the device is currently using.</p> <p>0b = Internal oscillator 1b = External clock</p>
0	MODE	R	0b	<p>Operating mode indication Indicates which operating mode the device is currently in.</p> <p>0b = Active mode 1b = Standby or power-down mode</p>

### 9.6.1.3 STATUS\_LSB Register (Address = 02h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-48. STATUS\_LSB Register**

15	14	13	12	11	10	9	8
SEQ2A_COUNT[1:0]		RESERVED		CONV1A_COUNT[1:0]		CONV1B_COUNT[1:0]	
R-00b		R-00b		R-00b		R-00b	
7	6	5	4	3	2	1	0
RESERVED						SEQ2A_ACTIVE	RESERVED
R-000000b						R-0b	R-0b

**表 9-29. STATUS\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	SEQ2A_COUNT[1:0]	R	00b	ADC2A sequence counter Circular counter that increments each time a new sequence on ADC2A completes. This counter resets to 00b when ADC2A is disabled, when the device is put in standby or power-down mode, or after a device reset.
13:12	RESERVED	R	00b	Reserved Always reads 00b.
11:10	CONV1A_COUNT[1:0]	R	00b	ADC1A conversion counter Circular counter that increments each time a new conversion on ADC1A completes. This counter resets to 00b when ADC1A is disabled, when the device is put in standby or power-down mode, or after a device reset.
9:8	CONV1B_COUNT[1:0]	R	00b	ADC1B conversion counter Circular counter that increments each time a new conversion on ADC1B completes. This counter resets to 00b when ADC1B is disabled, when the device is put in standby or power-down mode, or after a device reset.
7:2	RESERVED	R	000000b	Reserved Always reads 000000b.
1	SEQ2A_ACTIVE	R	0b	ADC2A sequence in progress indication Indicates that a sequence on ADC2A is currently in progress. Changes to registers from address 8Ch to 9Fh of ADC2A must only be made when ADC2A is disabled. 0b = No sequence in progress 1b = Sequence in progress
0	RESERVED	R	0b	Reserved Always reads 0b.

### 9.6.1.4 SUPPLY\_STATUS Register (Address = 03h) [Reset = FFFFh]

Return to the [Summary Table](#).

**图 9-49. SUPPLY\_STATUS Register**

15	14	13	12	11	10	9	8
AVDD_OVn	AVDD_UVn	IOVDD_OVn	IOVDD_UVn	DVDD_OVn	DVDD_UVn	AVDD_OSCn	IOVDD_OSCn
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b
7	6	5	4	3	2	1	0
DVDD_OSCn	AVDD_OTWn	IOVDD_OTWn	AVDD_CLn	IOVDD_CLn	AGNDA_DISCn	AGNDB_DISCn	DGND_DISCn
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

**表 9-30. SUPPLY\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	AVDD_OVn	R/W	1b	AVDD overvoltage fault flag Indicates the AVDD supply voltage exceeded the AVDD overvoltage threshold. See the AVDD monitor description for details regarding the AVDD LDO shutdown during overvoltage. Write 1b to clear this bit to 1b. 0b = Overvoltage fault occurred 1b = No overvoltage fault occurred
14	AVDD_UVn	R/W	1b	AVDD undervoltage fault flag Indicates the AVDD supply voltage dropped below the AVDD undervoltage threshold. Write 1b to clear this bit to 1b. 0b = Undervoltage fault occurred 1b = No undervoltage fault occurred
13	IOVDD_OVn	R/W	1b	IOVDD overvoltage fault flag Indicates the IOVDD supply voltage exceeded the IOVDD overvoltage threshold. See the IOVDD monitor description for details regarding the IOVDD LDO shutdown during overvoltage. Write 1b to clear this bit to 1b. 0b = Overvoltage fault occurred 1b = No overvoltage fault occurred
12	IOVDD_UVn	R/W	1b	IOVDD undervoltage fault flag Indicates the IOVDD supply voltage dropped below the IOVDD undervoltage threshold. Write 1b to clear this bit to 1b. 0b = Undervoltage fault occurred 1b = No undervoltage fault occurred
11	DVDD_OVn	R/W	1b	DVDD overvoltage fault flag Indicates the DVDD supply voltage exceeded the DVDD overvoltage threshold. See the DVDD monitor description for details regarding the DVDD LDO shutdown during overvoltage. Write 1b to clear this bit to 1b. 0b = Overvoltage fault occurred 1b = No overvoltage fault occurred
10	DVDD_UVn	R/W	1b	DVDD undervoltage fault flag Indicates the DVDD supply voltage dropped below the DVDD undervoltage threshold. Write 1b to clear this bit to 1b. 0b = Undervoltage fault occurred 1b = No undervoltage fault occurred
9	AVDD_OSCn	R/W	1b	AVDD oscillation fault flag Indicates the AVDD supply voltage is oscillating. Write 1b to clear this bit to 1b. 0b = Oscillation fault occurred 1b = No oscillation fault occurred
8	IOVDD_OSCn	R/W	1b	IOVDD oscillation fault flag Indicates the IOVDD supply voltage is oscillating. Write 1b to clear this bit to 1b. 0b = Oscillation fault occurred 1b = No oscillation fault occurred
7	DVDD_OSCn	R/W	1b	DVDD oscillation fault flag Indicates the DVDD supply voltage is oscillating. Write 1b to clear this bit to 1b. 0b = Oscillation fault occurred 1b = No oscillation fault occurred
6	AVDD_OTWn	R/W	1b	AVDD overtemperature warning flag Indicates the AVDD LDO temperature exceeded the AVDD overtemperature warning threshold. Write 1b to clear this bit to 1b. 0b = Overtemperature warning 1b = No overtemperature warning
5	IOVDD_OTWn	R/W	1b	IOVDD overtemperature warning flag Indicates the IOVDD LDO temperature exceeded the IOVDD overtemperature warning threshold. Write 1b to clear this bit to 1b. 0b = Overtemperature warning 1b = No overtemperature warning
4	AVDD_CLn	R/W	1b	AVDD current limit flag Indicates the AVDD LDO current limit is active. Write 1b to clear this bit to 1b. 0b = Current limit 1b = No current limit

**表 9-30. SUPPLY\_STATUS Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	IOVDD_CLn	R/W	1b	IOVDD current limit flag Indicates the IOVDD LDO current limit is active. Write 1b to clear this bit to 1b. 0b = Current limit 1b = No current limit
2	AGNDA_DISCn	R/W	1b	AGNDA pin disconnect detection flag Indicates the AGNDA pin is disconnected. Write 1b to clear this bit to 1b. 0b = AGNDA pin disconnected 1b = AGNDA pin connected
1	AGNDB_DISCn	R/W	1b	AGNDB pin disconnect detection flag Indicates the AGNDB pin is disconnected. Write 1b to clear this bit to 1b. 0b = AGNDB pin disconnected 1b = AGNDB pin connected
0	DGND_DISCn	R/W	1b	DGND pin disconnect detection flag Indicates the DGND pin is disconnected. Write 1b to clear this bit to 1b. 0b = DGND pin disconnected 1b = DGND pin connected

### 9.6.1.5 CLOCK\_STATUS Register (Address = 04h) [Reset = FC07h]

Return to the [Summary Table](#).

**图 9-50. CLOCK\_STATUS Register**

15	14	13	12	11	10	9	8
RESERVED							
R-1111110000000b							
7	6	5	4	3	2	1	0
RESERVED				MCLK_FAULTn		OSCD_WDn	MCLK_WDn
R-1111110000000b				R/W-1b		R/W-1b	R/W-1b

**表 9-31. CLOCK\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	1111110000000b	Reserved Always reads 1111110000000b.
2	MCLK_FAULTn	R/W	1b	MCLK frequency too high or too low fault flag Indicates the main clock frequency of the selected clock source either exceeded the clock frequency high threshold or dropped below the clock frequency low threshold. Write 1b to clear this bit to 1b. 0b = MCLK frequency too high or too low fault occurred 1b = No MCLK frequency too high or too low fault occurred
1	OSCD_WDn	R/W	1b	Diagnostic oscillator watchdog fault flag Indicates a diagnostic oscillator watchdog fault occurred. Write 1b to clear this bit to 1b. 0b = Watchdog fault occurred 1b = No watchdog fault occurred
0	MCLK_WDn	R/W	1b	Main clock watchdog fault flag Indicates a main clock watchdog fault occurred. Write 1b to clear this bit to 1b. 0b = Watchdog fault occurred 1b = No watchdog fault occurred

**9.6.1.6 DIGITAL\_STATUS Register (Address = 05h) [Reset = EC00h]**

Return to the [Summary Table](#).

**图 9-51. DIGITAL\_STATUS Register**

15	14	13	12	11	10	9	8
REG_MAP1_CRC_F AULTn	REG_MAP2_CRC_F AULTn	REG_MAP3_CRC_F AULTn	RESERVED	MEM_MAP_CRC_FA ULTn	OTP_BANK	RESERVED	
R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-1b	R-1b	R-000000000b	
7	6	5	4	3	2	1	0
RESERVED							
R-000000000b							

**表 9-32. DIGITAL\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	REG_MAP1_CRC_FAULTn	R/W	1b	Register map section 1 CRC fault flag Indicates a register map CRC fault in section 1 (register address space from 40h to 59h) occurred. Write 1b to clear this bit to 1b. 0b = Register map CRC fault occurred 1b = No register map CRC fault occurred
14	REG_MAP2_CRC_FAULTn	R/W	1b	Register map section 2 CRC fault flag Indicates a register map CRC fault in section 2 (register address space from 80h to A3h) occurred. Write 1b to clear this bit to 1b. 0b = Register map CRC fault occurred 1b = No register map CRC fault occurred
13	REG_MAP3_CRC_FAULTn	R/W	1b	Register map section 3 CRC fault flag Indicates a register map CRC fault in section 3 (register address space from C0h to E3h) occurred. Write 1b to clear this bit to 1b. 0b = Register map CRC fault occurred 1b = No register map CRC fault occurred
12	RESERVED	R	0b	Reserved Always reads 0b.
11	MEM_MAP_CRC_FAULTn	R/W	1b	Memory map CRC fault flag Indicates a memory map CRC fault in the internal memory occurred. Write 1b to clear this bit to 1b. Reset the device in case the flag continues to set to 0b. 0b = Memory map CRC fault occurred 1b = No memory map CRC fault occurred
10	OTP_BANK	R	1b	OTP bank indication Indicates which OTP bank the device selected after reset. The OTP_BANK bit does not trigger the DIGITAL_FAULTn bit in the STATUS_MSB register. Reset the device in case the flag indicates that the backup OTP bank is used. 0b = Backup OTP bank (bank 1) 1b = Primary OTP bank (bank 0)
9:0	RESERVED	R	000000000b	Reserved Always reads 000000000b.



### 9.6.1.7 OCC\_STATUS Register (Address = 06h) [Reset = 000Fh]

Return to the [Summary Table](#).

**图 9-52. OCC\_STATUS Register**

15	14	13	12	11	10	9	8
RESERVED							
R-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				OCCA_HTn	OCCA_LTn	OCCB_HTn	OCCB_LTn
R-000000000000b				R/W-1b	R/W-1b	R/W-1b	R/W-1b

**表 9-33. OCC\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:4	RESERVED	R	000000000000b	Reserved Always reads 000000000000b.
3	OCCA_HTn	R/W	1b	ADC1A overcurrent comparator high threshold fault flag Indicates the ADC1A digital fast filter output exceeded the set high threshold for the set amount of conversions. Write 1b to clear this bit to 1b. 0b = High threshold fault occurred 1b = No high threshold fault occurred
2	OCCA_LTn	R/W	1b	ADC1A overcurrent comparator low threshold fault flag Indicates the ADC1A digital fast filter output dropped below the set low threshold for the set amount of conversions. Write 1b to clear this bit to 1b. 0b = Low threshold fault occurred 1b = No low threshold fault occurred
1	OCCB_HTn	R/W	1b	ADC1B overcurrent comparator high threshold fault flag Indicates the ADC1B digital fast filter output exceeded the set high threshold for the set amount of conversions. Write 1b to clear this bit to 1b. 0b = High threshold fault occurred 1b = No high threshold fault occurred
0	OCCB_LTn	R/W	1b	ADC1B overcurrent comparator low threshold fault flag Indicates the ADC1B digital fast filter output dropped below the set low threshold for the set amount of conversions. Write 1b to clear this bit to 1b. 0b = Low threshold fault occurred 1b = No low threshold fault occurred

### 9.6.1.8 GPI\_DATA Register (Address = 07h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-53. GPI\_DATA Register**

15	14	13	12	11	10	9	8
RESERVED						GPI4_DAT[1:0]	
R-000000b						R-00b	
7	6	5	4	3	2	1	0
GPI3_DAT[1:0]		GPI2_DAT[1:0]		GPI1_DAT[1:0]		GPI0_DAT[1:0]	
R-00b		R-00b		R-00b		R-00b	

**表 9-34. GPI\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	000000b	Reserved Always reads 000000b.
9:8	GPI4_DAT[1:0]	R	00b	GPI04 data readback Readback value of GPIO4 when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
7:6	GPI3_DAT[1:0]	R	00b	GPI03 data readback Readback value of GPIO3 when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
5:4	GPI2_DAT[1:0]	R	00b	GPI02 data readback Readback value of GPIO2 when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
3:2	GPI1_DAT[1:0]	R	00b	GPI01 data readback Readback value of GPIO1 when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
1:0	GPI0_DAT[1:0]	R	00b	GPI00 data readback Readback value of GPIO0 when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)

### 9.6.1.9 GPIA\_GPIB\_DATA Register (Address = 08h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-54. GPIA\_GPIB\_DATA Register**

15	14	13	12	11	10	9	8
RESERVED				GPI1A_DAT[1:0]		GPI0A_DAT[1:0]	
R-0000b				R-00b		R-00b	
7	6	5	4	3	2	1	0
RESERVED				GPI1B_DAT[1:0]		GPI0B_DAT[1:0]	
R-0000b				R-00b		R-00b	

**表 9-35. GPIA\_GPIB\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b.
11:10	GPI1A_DAT[1:0]	R	00b	GPI01A data readback Readback value of GPIO1A when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
9:8	GPI0A_DAT[1:0]	R	00b	GPI00A data readback Readback value of GPIO0A when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
7:4	RESERVED	R	0000b	Reserved Always reads 0000b.
3:2	GPI1B_DAT[1:0]	R	00b	GPI01B data readback Readback value of GPIO1B when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)
1:0	GPI0B_DAT[1:0]	R	00b	GPI00B data readback Readback value of GPIO0B when configured as a digital input or output. 00b = Low (static low or PWM with a low period >66.6%) 01b = Weak low (PWM with a low period ≥50% but ≤66.6%) 10b = Weak high (PWM with a high period >50% but ≤66.6%) 11b = High (static high or PWM with a high period >66.6%)

### 9.6.1.10 CONVERSION\_CTRL Register (Address = 09h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-55. CONVERSION\_CTRL Register**

15	14	13	12	11	10	9	8
RESERVED	STARTA	RESERVED	STARTB	RESERVED	STOPA	RESERVED	STOPB
R-0b	R/W-0b	R-0b	R/W-0b	R-0b	R/W-0b	R-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED	SEQ2A_START	RESERVED			SEQ2A_STOP	RESERVED	
R-0b	R/W-0b	R-000b			R/W-0b	R-00b	

**表 9-36. CONVERSION\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved Always reads 0b.
14	STARTA	R/W	0b	Start or re-start ADC1A conversions Write 1b to start or restart conversions of enabled ADC1A. Always reads back 0b.
13	RESERVED	R	0b	Reserved Always reads 0b.
12	STARTB	R/W	0b	Start or restart ADC1B conversions Write 1b to start or restart conversions of enabled ADC1B. Always reads back 0b.
11	RESERVED	R	0b	Reserved Always reads 0b.
10	STOPA	R/W	0b	Stop ADC1A conversions Write 1b to stop conversions of ADC1A in continuous-conversion mode. Ongoing conversions are allowed to complete. The STOPA bit has no effect in single-shot conversion mode. The STARTA bit takes priority over the STOPA bit if both bits are set during the same WREG command frame. The STOPA bit clears to 0b after the ongoing conversion finishes or when the STARTA bit is set before the ongoing conversion finishes, which aborts the ongoing conversion and restarts new conversions.
9	RESERVED	R	0b	Reserved Always reads 0b.
8	STOPB	R/W	0b	Stop ADC1B conversions Write 1b to stop conversions of ADC1B in continuous-conversion mode. Ongoing conversions are allowed to complete. The STOPB bit has no effect in single-shot conversion mode. The STARTB bit takes priority over the STOPB bit if both bits are set during the same WREG command frame. The STOPB bit clears to 0b after the ongoing conversion finishes or when the STARTB bit is set before the ongoing conversion finishes, which aborts the ongoing conversion and restarts new conversions.
7	RESERVED	R	0b	Reserved Always reads 0b.
6	SEQ2A_START	R/W	0b	Start ADC2A sequence Write 1b to start or restart sequence of ADC2A. Always reads back 0b.
5:3	RESERVED	R	000b	Reserved Always reads 000b.
2	SEQ2A_STOP	R/W	0b	Stop ADC2A sequence Write 1b to stop ADC2A sequence. A sequence in progress is allowed to finish. The SEQ2A_START bit takes priority over the SEQ2A_STOP bit if both bits are set during the same WREG command frame. The SEQ2A_STOP bit clears to 0b after the ongoing sequence finishes or when the SEQ2A_START bit is set before the ongoing sequence finishes, which aborts the ongoing sequence and restarts a new sequence.
1:0	RESERVED	R	00b	Reserved Always reads 00b.

**9.6.1.11 SEQ2A\_STEP0\_DATA Register (Address = 10h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-56. SEQ2A\_STEP0\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP0_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP0_DAT[15:0]							
R-0000000000000000b							

**表 9-37. SEQ2A\_STEP0\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP0_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 0 conversion data Value provided in two's complement format.

**9.6.1.12 SEQ2A\_STEP1\_DATA Register (Address = 11h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-57. SEQ2A\_STEP1\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP1_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP1_DAT[15:0]							
R-0000000000000000b							

**表 9-38. SEQ2A\_STEP1\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP1_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 1 conversion data Value provided in two's complement format.

**9.6.1.13 SEQ2A\_STEP2\_DATA Register (Address = 12h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-58. SEQ2A\_STEP2\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP2_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP2_DAT[15:0]							
R-0000000000000000b							

**表 9-39. SEQ2A\_STEP2\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP2_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 2 conversion data Value provided in two's complement format.

**9.6.1.14 SEQ2A\_STEP3\_DATA Register (Address = 13h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-59. SEQ2A\_STEP3\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP3_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP3_DAT[15:0]							
R-0000000000000000b							

**表 9-40. SEQ2A\_STEP3\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP3_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 3 conversion data Value provided in two's complement format.



**9.6.1.15 SEQ2A\_STEP4\_DATA Register (Address = 14h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-60. SEQ2A\_STEP4\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP4_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP4_DAT[15:0]							
R-0000000000000000b							

**表 9-41. SEQ2A\_STEP4\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP4_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 4 conversion data Value provided in two's complement format.

**9.6.1.16 SEQ2A\_STEP5\_DATA Register (Address = 15h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-61. SEQ2A\_STEP5\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP5_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP5_DAT[15:0]							
R-0000000000000000b							

**表 9-42. SEQ2A\_STEP5\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP5_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 5 conversion data Value provided in two's complement format.

**9.6.1.17 SEQ2A\_STEP6\_DATA Register (Address = 16h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-62. SEQ2A\_STEP6\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP6_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP6_DAT[15:0]							
R-0000000000000000b							

**表 9-43. SEQ2A\_STEP6\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP6_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 6 conversion data Value provided in two's complement format.

**9.6.1.18 SEQ2A\_STEP7\_DATA Register (Address = 17h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-63. SEQ2A\_STEP7\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP7_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP7_DAT[15:0]							
R-0000000000000000b							

**表 9-44. SEQ2A\_STEP7\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP7_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 7 conversion data Value provided in two's complement format.

**9.6.1.19 SEQ2A\_STEP8\_DATA Register (Address = 18h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-64. SEQ2A\_STEP8\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP8_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP8_DAT[15:0]							
R-0000000000000000b							

**表 9-45. SEQ2A\_STEP8\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP8_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 8 conversion data Value provided in two's complement format.

**9.6.1.20 SEQ2A\_STEP9\_DATA Register (Address = 19h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-65. SEQ2A\_STEP9\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP9_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP9_DAT[15:0]							
R-0000000000000000b							

**表 9-46. SEQ2A\_STEP9\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP9_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 9 conversion data Value provided in two's complement format.

**9.6.1.21 SEQ2A\_STEP10\_DATA Register (Address = 1Ah) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-66. SEQ2A\_STEP10\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP10_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP10_DAT[15:0]							
R-0000000000000000b							

**表 9-47. SEQ2A\_STEP10\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP10_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 10 conversion data Value provided in two's complement format.

**9.6.1.22 SEQ2A\_STEP11\_DATA Register (Address = 1Bh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-67. SEQ2A\_STEP11\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP11_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP11_DAT[15:0]							
R-0000000000000000b							

**表 9-48. SEQ2A\_STEP11\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP11_DAT[15:0]	R	0000000000000000b	ADC2A sequence step 11 conversion data Value provided in two's complement format.



**9.6.1.23 SEQ2A\_STEP12\_DATA Register (Address = 1Ch) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-68. SEQ2A\_STEP12\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP12_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP12_DAT[15:0]							
R-0000000000000000b							

**表 9-49. SEQ2A\_STEP12\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP12_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 12 conversion data Value provided in two's complement format.

**9.6.1.24 SEQ2A\_STEP13\_DATA Register (Address = 1Dh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-69. SEQ2A\_STEP13\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP13_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP13_DAT[15:0]							
R-0000000000000000b							

**表 9-50. SEQ2A\_STEP13\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP13_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 13 conversion data Value provided in two's complement format.

**9.6.1.25 SEQ2A\_STEP14\_DATA Register (Address = 1Eh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-70. SEQ2A\_STEP14\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP14_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP14_DAT[15:0]							
R-0000000000000000b							

**表 9-51. SEQ2A\_STEP14\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP14_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 14 conversion data Value provided in two's complement format.

**9.6.1.26 SEQ2A\_STEP15\_DATA Register (Address = 1Fh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-71. SEQ2A\_STEP15\_DATA Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP15_DAT[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
SEQ2A_STEP15_DAT[15:0]							
R-0000000000000000b							

**表 9-52. SEQ2A\_STEP15\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SEQ2A_STEP15_DAT[15:0]	R	0000000000000000 000b	ADC2A sequence step 15 conversion data Value provided in two's complement format.

### 9.6.1.27 DEVICE\_MONITOR\_CFG Register (Address = 40h) [Reset = 0000h]

Return to the [Summary Table](#).

**図 9-72. DEVICE\_MONITOR\_CFG Register**

15		14		13		12		11		10		9		8	
REG_MAP1_CRC_EN		CRC_TYPE		SCLK_COUNTER_EN		TIMEOUT_EN		RESERVED				FAULT_POL			
R/W-0b		R/W-0b		R/W-0b		R/W-0b		R-000b				R/W-0b			
7		6		5		4		3		2		1		0	
RESERVED								MHD_POL		MHD_CFG[1:0]					
R-00000b								R/W-0b		R/W-00b					

**表 9-53. DEVICE\_MONITOR\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	REG_MAP1_CRC_EN	R/W	0b	Register map section 1 CRC enable Enables the register map CRC for section 1 (register address space from 40h to 59h). 0b = Disabled 1b = Enabled
14	CRC_TYPE	R/W	0b	CRC type selection Selects the CRC polynomial that is used for the SPI and register map CRC calculation. 0b = 16-bit CCITT 1b = 16-bit ANSI
13	SCLK_COUNTER_EN	R/W	0b	SCLK counter enable Enables the SCLK counter. 0b = Disabled 1b = Enabled
12	TIMEOUT_EN	R/W	0b	SPI timeout enable Enables the SPI timeout. When enabled the timeout checks that a rising edge of CSn happens within $2^{14} t_{OSCD}$ cycles after a CSn falling edge. When a timeout occurs, the remainder of the SPI frame on SDI is ignored before the rising edge of CSn. A new SPI transaction starts at the next CSn falling edge. 0b = Disabled 1b = Enabled
11:9	RESERVED	R	000b	Reserved Always reads back 000b.
8	FAULT_POL	R/W	0b	FAULT pin polarity selection Selects the polarity of the FAULT pin. The actual output behavior of the GPIO2/FAULT pin, when configured as a FAULT output in the GPIO2_SRC bit, depends on the GPIO2_FMT setting. A FAULT is active when any of the non-masked STATUS_MSB[14:7] bits are active. 0b = Active low. In case of a fault a logic low level is driven. 1b = Active high. In case of a fault a logic high level is driven.
7:3	RESERVED	R	00000b	Reserved Always reads back 00000b.
2	MHD_POL	R/W	0b	Missing host detection fault pin polarity selection Selects the polarity of the MHD pin. The actual output behavior of the GPIO0/MHD pin, when configured as an MHD output in the GPIO0_SRC bit, depends on the GPIO0_FMT setting. 0b = Active low. In case of a fault a logic low level is driven. 1b = Active high. In case of a fault a logic high level is driven.
1:0	MHD_CFG[1:0]	R/W	00b	Missing host detection configuration Detects when the host is not communicating with the device anymore. A watchdog timer checks the time between two valid commands with a valid CRC. If a valid command with a valid CRC is not received within the watchdog time window, the host is considered missing. When the watchdog times out, the GPIO0/MHD pin is set to active. To use the missing host detection mode, configure the GPIO0/MHD pin as an output using the GPIO0_DIR bit and the source for missing host detection mode using the GPIO0_SRC bit. To reset the GPIO0/MHD output after a missing host was detected, disable the missing host detection mode by setting MHD_CFG = 00b. 00b = Disabled 01b = $5120 \times t_{OSCD}$ (= 0.625 ms for $f_{OSCD} = 8.192$ MHz) 10b = $10240 \times t_{OSCD}$ (= 1.25 ms for $f_{OSCD} = 8.192$ MHz) 11b = $20480 \times t_{OSCD}$ (= 2.5 ms for $f_{OSCD} = 8.192$ MHz)

### 9.6.1.28 SUPPLY\_MONITOR\_CFG1 Register (Address = 41h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-73. SUPPLY\_MONITOR\_CFG1 Register**

15	14	13	12	11	10	9	8
AVDD_OV_EN	AVDD_UV_EN	IOVDD_OV_EN	IOVDD_UV_EN	DVDD_OV_EN	DVDD_UV_EN	AVDD_OSC_EN	IOVDD_OSC_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
DVDD_OSC_EN	AVDD_OTW_EN	IOVDD_OTW_EN	AVDD_CL_EN	IOVDD_CL_EN	AGNDA_DISC_EN	AGNDB_DISC_EN	DGND_DISC_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**表 9-54. SUPPLY\_MONITOR\_CFG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	AVDD_OV_EN	R/W	0b	AVDD LDO overvoltage monitor enable Enables the AVDD LDO output overvoltage monitor. 0b = Disabled 1b = Enabled
14	AVDD_UV_EN	R/W	0b	AVDD LDO undervoltage monitor enable Enables the AVDD LDO output undervoltage monitor. 0b = Disabled 1b = Enabled
13	IOVDD_OV_EN	R/W	0b	IOVDD LDO overvoltage monitor enable Enables the IOVDD LDO output overvoltage monitor. 0b = Disabled 1b = Enabled
12	IOVDD_UV_EN	R/W	0b	IOVDD LDO undervoltage monitor enable Enables the IOVDD LDO output undervoltage monitor. 0b = Disabled 1b = Enabled
11	DVDD_OV_EN	R/W	0b	DVDD LDO overvoltage monitor enable Enables the DVDD LDO output overvoltage monitor. 0b = Disabled 1b = Enabled
10	DVDD_UV_EN	R/W	0b	DVDD LDO undervoltage monitor enable Enables the DVDD LDO output undervoltage monitor. 0b = Disabled 1b = Enabled
9	AVDD_OSC_EN	R/W	0b	AVDD LDO oscillation monitor enable Enables the AVDD LDO output oscillation monitor. 0b = Disabled 1b = Enabled
8	IOVDD_OSC_EN	R/W	0b	IOVDD LDO oscillation monitor enable Enables the IOVDD LDO output oscillation monitor. 0b = Disabled 1b = Enabled
7	DVDD_OSC_EN	R/W	0b	DVDD LDO oscillation monitor enable Enables the DVDD LDO output oscillation monitor. 0b = Disabled 1b = Enabled
6	AVDD_OTW_EN	R/W	0b	AVDD LDO overtemperature warning monitor enable Enables the AVDD LDO overtemperature warning monitor. 0b = Disabled 1b = Enabled
5	IOVDD_OTW_EN	R/W	0b	IOVDD LDO overtemperature warning monitor enable Enables the IOVDD LDO overtemperature warning monitor. 0b = Disabled 1b = Enabled
4	AVDD_CL_EN	R/W	0b	AVDD LDO current limit enable Enables the AVDD LDO current limit. 0b = Disabled 1b = Enabled
3	IOVDD_CL_EN	R/W	0b	IOVDD LDO current limit enable Enables the IOVDD LDO current limit. 0b = Disabled 1b = Enabled
2	AGNDA_DISC_EN	R/W	0b	AGNDA disconnect monitor enable Enables the AGNDA disconnect monitor. 0b = Disabled 1b = Enabled
1	AGNDB_DISC_EN	R/W	0b	AGNDB disconnect monitor enable Enables the AGNDB disconnect monitor. 0b = Disabled 1b = Enabled

**表 9-54. SUPPLY\_MONITOR\_CFG1 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	DGND_DISC_EN	R/W	0b	DGND disconnect monitor enable Enables the DGND disconnect monitor. 0b = Disabled 1b = Enabled

### 9.6.1.29 SUPPLY\_MONITOR\_CFG2 Register (Address = 42h) [Reset = 10F0h]

Return to the [Summary Table](#).

**图 9-74. SUPPLY\_MONITOR\_CFG2 Register**

15	14	13	12	11	10	9	8
RESERVED		IOVDD_OV_TH	IOVDD_UV_TH	RESERVED			
R-00b		R/W-0b	R/W-1b	R-0000b			
7	6	5	4	3	2	1	0
AVDD_OTW_CFG[1:0]		IOVDD_OTW_CFG[1:0]		RESERVED			
R/W-11b		R/W-11b		R-0000b			

**表 9-55. SUPPLY\_MONITOR\_CFG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads back 00b.
13	IOVDD_OV_TH	R/W	0b	IOVDD overvoltage threshold selection Selects the threshold for the IOVDD LDO output overvoltage monitor. 0b = 5.7 V 1b = 3.9 V
12	IOVDD_UV_TH	R/W	1b	IOVDD undervoltage threshold selection Selects the threshold for the IOVDD LDO output undervoltage monitor. 0b = 4.3 V 1b = 2.95 V
11:8	RESERVED	R	0000b	Reserved Always reads back 0000b.
7:6	AVDD_OTW_CFG[1:0]	R/W	11b	AVDD LDO overtemperature warning threshold selection Selects the threshold for AVDD LDO overtemperature warning. 00b = #dash<deg#C 01b = 100°C 10b = 120°C 11b = 140°C
5:4	IOVDD_OTW_CFG[1:0]	R/W	11b	IOVDD LDO overtemperature warning threshold selection Selects the threshold for IOVDD LDO overtemperature warning. 00b = #dash<deg#C 01b = 100°C 10b = 120°C 11b = 140°C
3:0	RESERVED	R	0000b	Reserved Always reads back 0000b.



### 9.6.1.30 CLOCK\_MONITOR\_CFG Register (Address = 43h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-75. CLOCK\_MONITOR\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED						RESERVED	
R/W-000000b						R-0000000b	
7	6	5	4	3	2	1	0
RESERVED					MCLK_MON_EN	OSCD_WD_EN	MCLK_WD_EN
R-0000000b					R/W-0b	R/W-0b	R/W-0b

**表 9-56. CLOCK\_MONITOR\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved Always write 000000b.
9:3	RESERVED	R	0000000b	Reserved Always reads back 0000000b.
2	MCLK_MON_EN	R/W	0b	MCLK monitor enable Enables the main clock frequency monitor. 0b = Disabled 1b = Enabled
1	OSCD_WD_EN	R/W	0b	Diagnostic oscillator watchdog enable Enables the diagnostic oscillator watchdog. 0b = Disabled 1b = Enabled
0	MCLK_WD_EN	R/W	0b	Main clock watchdog enable Enables the main clock watchdog. 0b = Disabled 1b = Enabled

### 9.6.1.31 SUPPLY\_MONITOR\_DIAGNOSTIC\_CFG Register (Address = 44h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-76. SUPPLY\_MONITOR\_DIAGNOSTIC\_CFG Register**

15		14		13		12		11		10		9		8	
AVDD_OV_DIAG_EN	AVDD_UV_DIAG_EN	IOVDD_OV_DIAG_EN	IOVDD_UV_DIAG_EN	DVDD_OV_DIAG_EN	DVDD_UV_DIAG_EN	AVDD_OSC_DIAG_EN	IOVDD_OSC_DIAG_EN								
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b								
7		6		5		4		3		2		1		0	
DVDD_OSC_DIAG_EN	RESERVED						AGNDA_DISC_DIAG_EN	AGNDB_DISC_DIAG_EN	DGND_DISC_DIAG_EN						
R/W-0b	R-0000b						R/W-0b	R/W-0b	R/W-0b						

**表 9-57. SUPPLY\_MONITOR\_DIAGNOSTIC\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	AVDD_OV_DIAG_EN	R/W	0b	AVDD LDO overvoltage monitor diagnostic enable Enables the AVDD LDO output overvoltage monitor diagnostic. AVDD_OV_EN must be set for the diagnostic to work. The AVDD_OVn fault flag sets within $t_{p(AVDD\_OV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
14	AVDD_UV_DIAG_EN	R/W	0b	AVDD LDO undervoltage monitor diagnostic enable Enables the AVDD LDO output undervoltage monitor diagnostic. AVDD_UV_EN must be set for the diagnostic to work. The AVDD_UVn fault flag sets within $t_{p(AVDD\_UV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
13	IOVDD_OV_DIAG_EN	R/W	0b	IOVDD LDO overvoltage monitor diagnostic enable Enables the IOVDD LDO output overvoltage monitor diagnostic. IOVDD_OV_EN must be set for the diagnostic to work. The IOVDD_OVn fault flag sets within $t_{p(IOVDD\_OV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
12	IOVDD_UV_DIAG_EN	R/W	0b	IOVDD LDO undervoltage monitor diagnostic enable Enables the IOVDD LDO output undervoltage monitor diagnostic. IOVDD_UV_EN must be set for the diagnostic to work. The IOVDD_UVn fault flag sets within $t_{p(IOVDD\_UV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
11	DVDD_OV_DIAG_EN	R/W	0b	DVDD LDO overvoltage monitor diagnostic enable Enables the DVDD LDO output overvoltage monitor diagnostic. DVDD_OV_EN must be set for the diagnostic to work. The DVDD_OVn fault flag sets within $t_{p(DVDD\_OV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
10	DVDD_UV_DIAG_EN	R/W	0b	DVDD LDO undervoltage monitor diagnostic enable Enables the DVDD LDO output undervoltage monitor diagnostic. DVDD_UV_EN must be set for the diagnostic to work. The DVDD_UVn fault flag sets within $t_{p(DVDD\_UV)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
9	AVDD_OSC_DIAG_EN	R/W	0b	AVDD LDO oscillation monitor diagnostic enable Enables the AVDD LDO output oscillation monitor diagnostic. AVDD_OSC_EN must be set for the diagnostic to work. The AVDD_OSCn fault flag sets within $t_{p(AVDD\_OSC)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
8	IOVDD_OSC_DIAG_EN	R/W	0b	IOVDD LDO oscillation monitor diagnostic enable Enables the IOVDD LDO output oscillation monitor diagnostic. IOVDD_OSC_EN must be set for the diagnostic to work. The IOVDD_OSCn fault flag sets within $t_{p(IOVDD\_OSC)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
7	DVDD_OSC_DIAG_EN	R/W	0b	DVDD LDO oscillation monitor diagnostic enable Enables the DVDD LDO output oscillation monitor diagnostic. DVDD_OSC_EN must be set for the diagnostic to work. The DVDD_OSCn fault flag sets within $t_{p(DVDD\_OSC)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
6:3	RESERVED	R	0000b	Reserved Always reads back 0000b.

**表 9-57. SUPPLY\_MONITOR\_DIAGNOSTIC\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
2	AGNDA_DISC_DIAG_EN	R/W	0b	AGNDA disconnect monitor diagnostic enable Enables the AGNDA disconnect monitor diagnostic. AGNDA_DISC_EN must be set for the diagnostic to work. The AGNDA_DISCn fault flag sets within $t_{p(AGNDA\_OPEN)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
1	AGNDB_DISC_DIAG_EN	R/W	0b	AGNDB disconnect monitor diagnostic enable Enables the AGNDB disconnect monitor diagnostic. AGNDB_DISC_EN must be set for the diagnostic to work. The AGNDB_DISCn fault flag sets within $t_{p(AGNDB\_OPEN)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
0	DGND_DISC_DIAG_EN	R/W	0b	DGND disconnect monitor diagnostic enable Enables the DGND disconnect monitor diagnostic. DGND_DISC_EN must be set for the diagnostic to work. The DGND_DISCn fault flag sets within $t_{p(DGND\_OPEN)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled

### 9.6.1.32 CLOCK\_MONITOR\_DIAGNOSTIC\_CFG Register (Address = 45h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-77. CLOCK\_MONITOR\_DIAGNOSTIC\_CFG Register**

15	14	13	12	11	10	9	8
SPARE[11:0]							
R/W-000000000000b							
7	6	5	4	3	2	1	0
SPARE[11:0]				MCLK_HI_DIAG_EN	MCLK_LO_DIAG_EN	OSCD_WD_DIAG_EN	MCLK_WD_DIAG_EN
R/W-000000000000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

**表 9-58. CLOCK\_MONITOR\_DIAGNOSTIC\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:4	SPARE[11:0]	R/W	000000000000b	Spare bits Provided as R/W bits as a means to check the register map section 1 CRC. Bit settings have no effect.
3	MCLK_HI_DIAG_EN	R/W	0b	MCLK frequency too high monitor diagnostic enable Enables the main clock frequency too high monitor diagnostic. MCLK_MON_EN must be set for the diagnostic to work. The MCLK_FAULTn fault flag sets within $t_{p(MCLK\_FAULT)}$ when the diagnostic completed successfully. Do not enable the MCLK_LO_DIAG_EN at the same time. Execute the MCLK_HI_DIAG_EN and MCLK_LO_DIAG_EN sequentially. 0b = Disabled 1b = Enabled
2	MCLK_LO_DIAG_EN	R/W	0b	MCLK frequency too low monitor diagnostic enable Enables the main clock frequency too low monitor diagnostic. MCLK_MON_EN must be set for the diagnostic to work. The MCLK_FAULTn fault flag sets within $t_{p(MCLK\_FAULT)}$ when the diagnostic completed successfully. Do not enable the MCLK_HI_DIAG_EN at the same time. Execute the MCLK_HI_DIAG_EN and MCLK_LO_DIAG_EN sequentially. 0b = Disabled 1b = Enabled
1	OSCD_WD_DIAG_EN	R/W	0b	Diagnostic oscillator watchdog diagnostic enable Enables the diagnostic oscillator watchdog diagnostic. OSCD_WD_EN must be set for the diagnostic to work. The OSCD_WDn fault flag sets within $t_{p(OSCD\_WD)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled
0	MCLK_WD_DIAG_EN	R/W	0b	Main clock watchdog diagnostic enable Enables the main clock watchdog diagnostic. MCLK_WD_EN must be set for the diagnostic to work. The MCLK_WDn fault flag sets within $t_{p(MCLK\_WD)}$ when the diagnostic completed successfully. 0b = Disabled 1b = Enabled

### 9.6.1.33 DIGITAL\_MONITOR\_DIAGNOSTIC\_CFG Register (Address = 46h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-78. DIGITAL\_MONITOR\_DIAGNOSTIC\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED						MEM_MAP_CRC_DIAG[1:0]	
R-000000b						R/W-00b	
7	6	5	4	3	2	1	0
RESERVED				GPIOA_DIAG_EN	GPIOB_DIAG_EN	GPIO_DIAG_EN	
R-000000b				R/W-0b	R/W-0b	R/W-0b	

**表 9-59. DIGITAL\_MONITOR\_DIAGNOSTIC\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	000000b	Reserved Always reads back 000000b.
9:8	MEM_MAP_CRC_DIAG[1:0]	R/W	00b	Memory map CRC diagnostic bit pattern selection Selects the bit pattern to use for the memory map CRC diagnostic. The MEM_MAP_CRC_FAULTn fault flag sets within t <sub>DIAG</sub> (MEM_MAP_CRC) when the diagnostic completed successfully. Any of the three available bit patterns can be used for the diagnostic. 00b = Disabled 01b = Pattern 1 10b = Pattern 2 11b = Pattern 3
7:3	RESERVED	R	00000b	Reserved Always reads back 00000b.
2	GPIOA_DIAG_EN	R/W	0b	GPIOA readback diagnostic enable Inverts the readback value of the GPIOA_DAT[1:0] bits if GPIOA_DIR is configured as a digital output. 0b = Disabled 1b = Enabled
1	GPIOB_DIAG_EN	R/W	0b	GPIOB readback diagnostic enable Inverts the readback value of the GPIOB_DAT[1:0] bits if GPIOB_DIR is configured as a digital output. 0b = Disabled 1b = Enabled
0	GPIO_DIAG_EN	R/W	0b	GPIO readback diagnostic enable Inverts the readback value of the GPIO_DAT[1:0] bits if GPIO_DIR is configured as a digital output. 0b = Disabled 1b = Enabled

### 9.6.1.34 SUPPLY\_FAULT\_MASK Register (Address = 47h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-79. SUPPLY\_FAULT\_MASK Register**

15		14		13		12		11		10		9		8	
AVDD_OV_MASK	AVDD_UV_MASK	IOVDD_OV_MASK	IOVDD_UV_MASK	DVDD_OV_MASK	DVDD_UV_MASK	AVDD_OSC_MASK	IOVDD_OSC_MASK								
R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b	
7		6		5		4		3		2		1		0	
DVDD_OSC_MASK	AVDD_OTW_MASK	IOVDD_OTW_MASK	AVDD_CL_MASK	IOVDD_CL_MASK	AGNDA_DISC_MASK	AGNDB_DISC_MASK	DGND_DISC_MASK								
R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b		R/W-0b	

**表 9-60. SUPPLY\_FAULT\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	AVDD_OV_MASK	R/W	0b	AVDD overvoltage fault flag mask Masks the AVDD overvoltage fault flag (AVDD_OVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
14	AVDD_UV_MASK	R/W	0b	AVDD undervoltage fault flag mask Masks the AVDD undervoltage fault flag (AVDD_UVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
13	IOVDD_OV_MASK	R/W	0b	IOVDD overvoltage fault flag mask Masks the IOVDD overvoltage fault flag (IOVDD_OVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
12	IOVDD_UV_MASK	R/W	0b	IOVDD undervoltage fault flag mask Masks the IOVDD undervoltage fault flag (IOVDD_UVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
11	DVDD_OV_MASK	R/W	0b	DVDD overvoltage fault flag mask Masks the DVDD overvoltage fault flag (DVDD_OVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
10	DVDD_UV_MASK	R/W	0b	DVDD undervoltage fault flag mask Masks the DVDD undervoltage fault flag (DVDD_UVn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
9	AVDD_OSC_MASK	R/W	0b	AVDD oscillation fault flag mask Masks the AVDD oscillation fault flag (AVDD_OSCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
8	IOVDD_OSC_MASK	R/W	0b	IOVDD oscillation fault flag mask Masks the IOVDD oscillation fault flag (IOVDD_OSCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
7	DVDD_OSC_MASK	R/W	0b	DVDD oscillation fault flag mask Masks the DVDD oscillation fault flag (DVDD_OSCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
6	AVDD_OTW_MASK	R/W	0b	AVDD overtemperature warning flag mask Masks the AVDD LDO overtemperature warning flag (AVDD_OTWn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
5	IOVDD_OTW_MASK	R/W	0b	IOVDD overtemperature warning flag mask Masks the IOVDD LDO overtemperature warning flag (IOVDD_OTWn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
4	AVDD_CL_MASK	R/W	0b	AVDD current limit flag mask Masks the AVDD LDO current limit flag (AVDD_CLn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked

**表 9-60. SUPPLY\_FAULT\_MASK Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	IOVDD_CL_MASK	R/W	0b	IOVDD current limit flag mask Masks the IOVDD LDO current limit flag (IOVDD_CLn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
2	AGNDA_DISC_MASK	R/W	0b	AGNDA pin disconnect detection flag mask Masks the AGNDA pin disconnect detection flag (AGNDA_DISCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
1	AGNDB_DISC_MASK	R/W	0b	AGNDB pin disconnect detection flag mask Masks the AGNDB pin disconnect detection flag (AGNDB_DISCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
0	DGND_DISC_MASK	R/W	0b	DGND pin disconnect detection flag mask Masks the DGND pin disconnect detection flag (DGND_DISCn) from triggering the SUPPLY_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked

### 9.6.1.35 CLOCK\_FAULT\_MASK Register (Address = 48h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-80. CLOCK\_FAULT\_MASK Register**

15	14	13	12	11	10	9	8
RESERVED						RESERVED	
R/W-000000b						R-0000000b	
7	6	5	4	3	2	1	0
RESERVED					MCLK_FAULT_MAS K	OSCD_WD_MASK	MCLK_WD_MASK
R-0000000b					R/W-0b	R/W-0b	R/W-0b

**表 9-61. CLOCK\_FAULT\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved Always write 000000b.
9:3	RESERVED	R	0000000b	Reserved Always reads back 0000000b.
2	MCLK_FAULT_MASK	R/W	0b	MCLK frequency too high or too low fault flag mask Masks the MCLK frequency too high or too low fault flag (MCLK_FAULTn) from triggering the CLOCK_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
1	OSCD_WD_MASK	R/W	0b	Diagnostic oscillator watchdog fault flag mask Masks the diagnostic oscillator watchdog fault flag (OSCD_WDn) from triggering the CLOCK_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
0	MCLK_WD_MASK	R/W	0b	Main clock watchdog fault flag mask Masks the main clock watchdog fault flag (MCLK_WDn) from triggering the CLOCK_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked



### 9.6.1.36 DIGITAL\_FAULT\_MASK Register (Address = 49h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-81. DIGITAL\_FAULT\_MASK Register**

15	14	13	12	11	10	9	8
REG_MAP1_CRC_FAULT_MASK	REG_MAP2_CRC_FAULT_MASK	REG_MAP3_CRC_FAULT_MASK	RESERVED	MEM_MAP_CRC_FAULT_MASK	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R-00000000000b		
7	6	5	4	3	2	1	0
RESERVED							
R-00000000000b							

**表 9-62. DIGITAL\_FAULT\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	REG_MAP1_CRC_FAULT_MASK	R/W	0b	Register map section 1 CRC fault flag mask Masks the register map section 1 CRC fault flag (REG_MAP1_CRC_FAULTn) from triggering the DIGITAL_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
14	REG_MAP2_CRC_FAULT_MASK	R/W	0b	Register map section 2 CRC fault flag mask Masks the register map section 2 CRC fault flag (REG_MAP2_CRC_FAULTn) from triggering the DIGITAL_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
13	REG_MAP3_CRC_FAULT_MASK	R/W	0b	Register map section 3 CRC fault flag mask Masks the register map section 3 CRC fault flag (REG_MAP3_CRC_FAULTn) from triggering the DIGITAL_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
12	RESERVED	R	0b	Reserved Always reads back 0b.
11	MEM_MAP_CRC_FAULT_MASK	R/W	0b	Memory map CRC fault flag mask Masks the memory map CRC fault flag (MEM_MAP_CRC_FAULTn) from triggering the DIGITAL_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
10:0	RESERVED	R	00000000000b	Reserved Always reads back 00000000000b.

### 9.6.1.37 OCC\_FAULT\_MASK Register (Address = 4Ah) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-82. OCC\_FAULT\_MASK Register**

15	14	13	12	11	10	9	8
RESERVED							
R-0000000000000b							
7	6	5	4	3	2	1	0
RESERVED				OCCA_HT_MASK	OCCA_LT_MASK	OCCB_HT_MASK	OCCB_LT_MASK
R-0000000000000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

**表 9-63. OCC\_FAULT\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:4	RESERVED	R	0000000000000b	Reserved Always reads back 0000000000000b.
3	OCCA_HT_MASK	R/W	0b	ADC1A overcurrent comparator high threshold fault flag mask Masks the ADC1A overcurrent comparator high threshold fault flag (OCCA_HTN) from triggering the OCC_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
2	OCCA_LT_MASK	R/W	0b	ADC1A overcurrent comparator low threshold fault flag mask Masks the ADC1A overcurrent comparator low threshold fault flag (OCCA_LTN) from triggering the OCC_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
1	OCCB_HT_MASK	R/W	0b	ADC1B overcurrent comparator high threshold fault flag mask Masks the ADC1B overcurrent comparator high threshold fault flag (OCCB_HTN) from triggering the OCC_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked
0	OCCB_LT_MASK	R/W	0b	ADC1B overcurrent comparator low threshold fault flag mask Masks the ADC1B overcurrent comparator low threshold fault flag (OCCB_LTN) from triggering the OCC_FAULTn flag in the STATUS_MSB register. 0b = Unmasked 1b = Masked

### 9.6.1.38 FAULT\_PIN\_MASK Register (Address = 4Bh) [Reset = 0780h]

Return to the [Summary Table](#).

**图 9-83. FAULT\_PIN\_MASK Register**

15	14	13	12	11	10	9	8
RESERVED	SUPPLY_FAULT_MASK	CLOCK_FAULT_MASK	DIGITAL_FAULT_MASK	OCC_FAULT_MASK	SPI_CRC_FAULT_MASK	SPI_TIMEOUT_MASK	SCLK_COUNT_FAULT_MASK
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-1b
7	6	5	4	3	2	1	0
REG_ACCESS_FAULT_MASK	RESERVED						
R/W-1b	R-0000000b						

**表 9-64. FAULT\_PIN\_MASK Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved Always reads back 0b.
14	SUPPLY_FAULT_MASK	R/W	0b	Supply fault flag mask Masks the supply fault flag (SUPPLY_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
13	CLOCK_FAULT_MASK	R/W	0b	Clock fault flag mask Masks the clock fault flag (CLOCK_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
12	DIGITAL_FAULT_MASK	R/W	0b	Digital fault flag mask Masks the digital fault flag (DIGITAL_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
11	OCC_FAULT_MASK	R/W	0b	Overcurrent comparator fault flag mask Masks the overcurrent comparator fault flag (OCC_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
10	SPI_CRC_FAULT_MASK	R/W	1b	SPI CRC fault flag mask Masks the SPI CRC fault flag (SPI_CRC_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
9	SPI_TIMEOUT_MASK	R/W	1b	SPI timeout fault flag mask Masks the SPI timeout fault flag (SPI_TIMEOUTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
8	SCLK_COUNT_FAULT_MASK	R/W	1b	SCLK counter fault flag mask Masks the SCLK counter fault flag (SCLK_COUNT_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
7	REG_ACCESS_FAULT_MASK	R/W	1b	Register access fault flag mask Masks the register access fault flag (REG_ACCESS_FAULTn) in the STATUS_MSB register from triggering the FAULT pin when the GPIO2/FAULT pin is configured as a FAULT output. 0b = Unmasked 1b = Masked
6:0	RESERVED	R	0000000b	Reserved Always reads back 0000000b.

### 9.6.1.39 DEVICE\_CFG Register (Address = 4Ch) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-84. DEVICE\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED	DRDY_CTRL	RESERVED	CLK_SOURCE	WORD_LENGTH	RESERVED	OP_MODE[1:0]	
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-00b	
7	6	5	4	3	2	1	0
RESERVED							
R-0000000b							

**表 9-65. DEVICE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved Always reads back 0b.
14	DRDY_CTRL	R/W	0b	DRDYn pin control selection Selects which ADC controls the DRDYn pin indication. 0b = ADC1A 1b = ADC1B
13	RESERVED	R/W	0b	Reserved Always write 0b.
12	CLK_SOURCE	R/W	0b	MCLK clock source selection Selects the main clock source of the device. Before changing this bit, all ADCs must be disabled or the device placed in standby or power-down mode. When switching from an external clock to the internal oscillator, the external clock must be provided until after the switch-over is complete. 0b = Internal oscillator 1b = External clock
11	WORD_LENGTH	R/W	0b	Data word length selection Selects the length of every word in the SPI frame. 0b = 24 bits 1b = 32 bits; LSB zero padding
10	RESERVED	R	0b	Reserved Always reads back 0b.
9:8	OP_MODE[1:0]	R/W	00b	Operating mode selection Selects the operating mode for the device. 00b = Active mode 01b = Standby mode (Disables all ADCs) 10b = Power-down mode 11b = Power-down mode
7:0	RESERVED	R	0000000b	Reserved Always reads back 0000000b.

### 9.6.1.40 GPIO\_CFG Register (Address = 4Dh) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-85. GPIO\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED	GPIO4_FMT	GPIO3_FMT	GPIO2_FMT	GPIO1_FMT	GPIO0_FMT	GPIO4_DIR	GPIO3_DIR
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
GPIO2_DIR	GPIO1_DIR	GPIO0_DIR	GPIO4_SRC	GPIO3_SRC	GPIO2_SRC	RESERVED	GPIO0_SRC
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b

**表 9-66. GPIO\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0b	Reserved Always reads back 0b.
14	GPIO4_FMT	R/W	0b	GPIO4 format Configures GPIO4 for static input and output levels or for PWM input and output levels 0b = When GPIO4 is configured as a digital input: Logic levels are based on static input levels. When GPIO4 is configured as a digital output: Output with static output levels. (GPIO4_LL_PWM_CFG and GPIO4_LH_PWM_CFG registers are ignored in this case). For parallel GPO readback purposes the readback path is configured for logic levels based on static input levels in this case. 1b = When GPIO4 is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO4 is configured as a digital output: Output with PWM output defined by the GPIO4_LL_PWM_CFG and GPIO4_LH_PWM_CFG registers. For parallel GPO readback purposes the readback path is configured for logic levels based on PWM decoding using the time base configured in GPIO4_PWM_TB in this case.
13	GPIO3_FMT	R/W	0b	GPIO3 format Configures GPIO3 for static input and output levels or for PWM input and output levels 0b = When GPIO3 is configured as a digital input: Logic levels are based on static input levels. When GPIO3 is configured as a digital output: Output with static output levels. (GPIO3_LL_PWM_CFG and GPIO3_LH_PWM_CFG registers are ignored in this case). For parallel GPO readback purposes the readback path is configured for logic levels based on static input levels in this case. 1b = When GPIO3 is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO3 is configured as a digital output: Output with PWM output defined by the GPIO3_LL_PWM_CFG and GPIO3_LH_PWM_CFG registers. For parallel GPO readback purposes the readback path is configured for logic levels based on PWM decoding using the time base configured in GPIO3_PWM_TB in this case.
12	GPIO2_FMT	R/W	0b	GPIO2 format Configures GPIO2 for static input and output levels or for PWM input and output levels 0b = When GPIO2 is configured as a digital input: Logic levels are based on static input levels. When GPIO2 is configured as a digital output: Output with static output levels. (GPIO2_LL_PWM_CFG and GPIO2_LH_PWM_CFG registers are ignored in this case). For parallel GPO readback purposes the readback path is configured for logic levels based on static input levels in this case. 1b = When GPIO2 is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO2 is configured as a digital output: Output with PWM output defined by the GPIO2_LL_PWM_CFG and GPIO2_LH_PWM_CFG registers. For parallel GPO readback purposes the readback path is configured for logic levels based on PWM decoding using the time base configured in GPIO2_PWM_TB in this case.
11	GPIO1_FMT	R/W	0b	GPIO1 format Configures GPIO1 for static input and output levels or for PWM input and output levels 0b = When GPIO1 is configured as a digital input: Logic levels are based on static input levels. When GPIO1 is configured as a digital output: Output with static output levels. (GPIO1_LL_PWM_CFG and GPIO1_LH_PWM_CFG registers are ignored in this case). For parallel GPO readback purposes the readback path is configured for logic levels based on static input levels in this case. 1b = When GPIO1 is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO1 is configured as a digital output: Output with PWM output defined by the GPIO1_LL_PWM_CFG and GPIO1_LH_PWM_CFG registers. For parallel GPO readback purposes the readback path is configured for logic levels based on PWM decoding using the time base configured in GPIO1_PWM_TB in this case.
10	GPIO0_FMT	R/W	0b	GPIO0 format Configures GPIO0 for static input and output levels or for PWM input and output levels 0b = When GPIO0 is configured as a digital input: Logic levels are based on static input levels. When GPIO0 is configured as a digital output: Output with static output levels. (GPIO0_LL_PWM_CFG and GPIO0_LH_PWM_CFG registers are ignored in this case). For parallel GPO readback purposes the readback path is configured for logic levels based on static input levels in this case. 1b = When GPIO0 is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO0 is configured as a digital output: Output with PWM output defined by the GPIO0_LL_PWM_CFG and GPIO0_LH_PWM_CFG registers. For parallel GPO readback purposes the readback path is configured for logic levels based on PWM decoding using the time base configured in GPIO0_PWM_TB in this case.

**表 9-66. GPIO\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
9	GPIO4_DIR	R/W	0b	GPIO4 direction Configures GPIO4 as a digital input or output. Configure as a digital output when used as OCCB output. 0b = Digital input 1b = Digital output
8	GPIO3_DIR	R/W	0b	GPIO3 direction Configures GPIO3 as a digital input or output. Configure as a digital output when used as OCCA output. 0b = Digital input 1b = Digital output
7	GPIO2_DIR	R/W	0b	GPIO2 direction Configures GPIO2 as a digital input or output. Configure as a digital output when used as FAULT output. 0b = Digital input 1b = Digital output
6	GPIO1_DIR	R/W	0b	GPIO1 direction Configures GPIO1 as a digital input or output. 0b = Digital input 1b = Digital output
5	GPIO0_DIR	R/W	0b	GPIO0 direction Configures GPIO0 as a digital input or output. Configure as a digital output when used as MHD output. 0b = Digital input 1b = Digital output
4	GPIO4_SRC	R/W	0b	GPIO4 data source selection Selects the data source of the GPIO4/OCCB pin when GPIO4 is configured as an output. 0b = OCCB 1b = GPIO
3	GPIO3_SRC	R/W	0b	GPIO3 data source selection Selects the data source of the GPIO3/OCCA pin when GPIO3 is configured as an output. 0b = OCCA 1b = GPIO
2	GPIO2_SRC	R/W	0b	GPIO2 data source selection Selects the data source of the GPIO2/FAULT pin when GPIO2 is configured as an output. 0b = FAULT 1b = GPIO
1	RESERVED	R	0b	Reserved Always reads back 0b.
0	GPIO0_SRC	R/W	0b	GPIO0 data source selection Selects the data source of the GPIO0/MHD pin when GPIO0 is configured as an output. 0b = Missing host detection (MHD) 1b = GPIO

### 9.6.1.41 GPO\_DATA Register (Address = 4Eh) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-86. GPO\_DATA Register**

15	14	13	12	11	10	9	8
SPARE[10:0]							
R/W-00000000000b							
7	6	5	4	3	2	1	0
SPARE[10:0]			GPO4_DAT	GPO3_DAT	GPO2_DAT	GPO1_DAT	GPO0_DAT
R/W-00000000000b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

**表 9-67. GPO\_DATA Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:5	SPARE[10:0]	R/W	00000000000b	Spare bits Provided as R/W bits as a means to check the register map section 1 CRC. Bit settings have no effect.
4	GPO4_DAT	R/W	0b	GPIO4 output data Output value of GPIO4 when configured as a digital output. Bit setting has not effect when GPIO4 is configured as an input or as OCCB output. 0b = Low 1b = High
3	GPO3_DAT	R/W	0b	GPIO3 output data Output value of GPIO3 when configured as a digital output. Bit setting has not effect when GPIO3 is configured as an input or as OCCA output. 0b = Low 1b = High
2	GPO2_DAT	R/W	0b	GPIO2 output data Output value of GPIO2 when configured as a digital output. Bit setting has not effect when GPIO2 is configured as an input or as FAULT output. 0b = Low 1b = High
1	GPO1_DAT	R/W	0b	GPIO1 output data Output value of GPIO1 when configured as a digital output. Bit setting has not effect when GPIO1 is configured as an input. 0b = Low 1b = High
0	GPO0_DAT	R/W	0b	GPIO0 output data Output value of GPIO0 when configured as a digital output. Bit setting has not effect when GPIO0 is configured as an input or as MHD output. 0b = Low 1b = High

### 9.6.1.42 GPIO0\_LL\_PWM\_CFG Register (Address = 4Fh) [Reset = 007Fh]

Return to the [Summary Table](#).

**图 9-87. GPIO0\_LL\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
GPIO0_PWM_TB[1:0]			GPIO0_LL_PWM_HC[6:0]				
R/W-00b			R/W-0000000b				
7	6	5	4	3	2	1	0
GPIO0_LL_PWM_HC[6:0]		GPIO0_LL_PWM_LC[6:0]					
R/W-0000000b		R/W-1111111b					

**表 9-68. GPIO0\_LL\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPIO0_PWM_TB[1:0]	R/W	00b	GPIO0/MHD PWM time base selection Selects the time base used for the GPIO0/MHD PWM generation when the GPIO0/MHD pin is configured as an output as well as the time base used for the PWM encoder. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
13:7	GPIO0_LL_PWM_HC[6:0]	R/W	0000000b	GPIO0/MHD logic low level PWM high counter Sets the high period of the PWM for a logic low level of GPIO0/MHD. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO0/MHD logic low level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO0/MHD logic low level as static low.
6:0	GPIO0_LL_PWM_LC[6:0]	R/W	1111111b	GPIO0/MHD logic low level PWM low counter Sets the low period of the PWM for a logic low level of GPIO0/MHD. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO0/MHD logic low level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO0/MHD logic low level as static low.



### 9.6.1.43 GPIO0\_LH\_PWM\_CFG Register (Address = 50h) [Reset = 3F80h]

Return to the [Summary Table](#).

**图 9-88. GPIO0\_LH\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED			GPIO0_LH_PWM_HC[6:0]				
R-00b			R/W-1111111b				
7	6	5	4	3	2	1	0
GPIO0_LH_PWM_H C[6:0]		GPIO0_LH_PWM_LC[6:0]					
R/W-1111111b		R/W-0000000b					

**表 9-69. GPIO0\_LH\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads 00b.
13:7	GPIO0_LH_PWM_HC[6:0]	R/W	1111111b	GPIO0/MHD logic high level PWM high counter Sets the high period of the PWM for a logic high level of GPIO0/MHD. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO0/MHD logic high level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO0/MHD logic high level as static low.
6:0	GPIO0_LH_PWM_LC[6:0]	R/W	0000000b	GPIO0/MHD logic high level PWM low counter Sets the low period of the PWM for a logic high level of GPIO0/MHD. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO0/MHD logic high level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO0/MHD logic high level as static low.

### 9.6.1.44 GPIO1\_LL\_PWM\_CFG Register (Address = 51h) [Reset = 007Fh]

Return to the [Summary Table](#).

**图 9-89. GPIO1\_LL\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
GPIO1_PWM_TB[1:0]		GPIO1_LL_PWM_HC[6:0]					
R/W-00b		R/W-0000000b					
7	6	5	4	3	2	1	0
GPIO1_LL_PWM_HC[6:0]		GPIO1_LL_PWM_LC[6:0]					
R/W-0000000b		R/W-1111111b					

**表 9-70. GPIO1\_LL\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPIO1_PWM_TB[1:0]	R/W	00b	GPIO1 PWM time base selection Selects the time base used for the GPIO1 PWM generation when the GPIO1 pin is configured as an output as well as the time base used for the PWM encoder. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
13:7	GPIO1_LL_PWM_HC[6:0]	R/W	0000000b	GPIO1 logic low level PWM high counter Sets the high period of the PWM for a logic low level of GPIO1. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO1 logic low level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO1 logic low level as static low.
6:0	GPIO1_LL_PWM_LC[6:0]	R/W	1111111b	GPIO1 logic low level PWM low counter Sets the low period of the PWM for a logic low level of GPIO1. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO1 logic low level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO1 logic low level as static low.

### 9.6.1.45 GPIO1\_LH\_PWM\_CFG Register (Address = 52h) [Reset = 3F80h]

Return to the [Summary Table](#).

**图 9-90. GPIO1\_LH\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED			GPIO1_LH_PWM_HC[6:0]				
R-00b			R/W-1111111b				
7	6	5	4	3	2	1	0
GPIO1_LH_PWM_H C[6:0]		GPIO1_LH_PWM_LC[6:0]					
R/W-1111111b		R/W-0000000b					

**表 9-71. GPIO1\_LH\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads 00b.
13:7	GPIO1_LH_PWM_HC[6:0]	R/W	1111111b	GPIO1 logic high level PWM high counter Sets the high period of the PWM for a logic high level of GPIO1. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO1 logic high level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO1 logic high level as static low.
6:0	GPIO1_LH_PWM_LC[6:0]	R/W	0000000b	GPIO1 logic high level PWM low counter Sets the low period of the PWM for a logic high level of GPIO1. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO1 logic high level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO1 logic high level as static low.

### 9.6.1.46 GPIO2\_LL\_PWM\_CFG Register (Address = 53h) [Reset = 007Fh]

Return to the [Summary Table](#).

**图 9-91. GPIO2\_LL\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
GPIO2_PWM_TB[1:0]		GPIO2_LL_PWM_HC[6:0]					
R/W-00b		R/W-0000000b					
7	6	5	4	3	2	1	0
GPIO2_LL_PWM_HC[6:0]		GPIO2_LL_PWM_LC[6:0]					
R/W-0000000b		R/W-1111111b					

**表 9-72. GPIO2\_LL\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPIO2_PWM_TB[1:0]	R/W	00b	GPIO2/FAULT PWM time base selection Selects the time base used for the GPIO2/FAULT PWM generation when the GPIO2/FAULT pin is configured as an output as well as the time base used for the PWM encoder. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
13:7	GPIO2_LL_PWM_HC[6:0]	R/W	0000000b	GPIO2/FAULT logic low level PWM high counter Sets the high period of the PWM for a logic low level of GPIO2/FAULT. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO2/FAULT logic low level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/FAULT logic low level as static low.
6:0	GPIO2_LL_PWM_LC[6:0]	R/W	1111111b	GPIO2/FAULT logic low level PWM low counter Sets the low period of the PWM for a logic low level of GPIO2/FAULT. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO2/FAULT logic low level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/FAULT logic low level as static low.

### 9.6.1.47 GPIO2\_LH\_PWM\_CFG Register (Address = 54h) [Reset = 3F80h]

Return to the [Summary Table](#).

**图 9-92. GPIO2\_LH\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED			GPIO2_LH_PWM_HC[6:0]				
R-00b			R/W-1111111b				
7	6	5	4	3	2	1	0
GPIO2_LH_PWM_H C[6:0]		GPIO2_LH_PWM_LC[6:0]					
R/W-1111111b		R/W-0000000b					

**表 9-73. GPIO2\_LH\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads 00b.
13:7	GPIO2_LH_PWM_HC[6:0]	R/W	1111111b	GPIO2/FAULT logic high level PWM high counter Sets the high period of the PWM for a logic high level of GPIO2/FAULT. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO2/FAULT logic high level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/FAULT logic high level as static low.
6:0	GPIO2_LH_PWM_LC[6:0]	R/W	0000000b	GPIO2/FAULT logic high level PWM low counter Sets the low period of the PWM for a logic high level of GPIO2/FAULT. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO2/FAULT logic high level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/FAULT logic high level as static low.

### 9.6.1.48 GPIO3\_LL\_PWM\_CFG Register (Address = 55h) [Reset = 007Fh]

Return to the [Summary Table](#).

**图 9-93. GPIO3\_LL\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
GPIO3_PWM_TB[1:0]		GPIO3_LL_PWM_HC[6:0]					
R/W-00b		R/W-0000000b					
7	6	5	4	3	2	1	0
GPIO3_LL_PWM_HC[6:0]		GPIO3_LL_PWM_LC[6:0]					
R/W-0000000b		R/W-1111111b					

**表 9-74. GPIO3\_LL\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPIO3_PWM_TB[1:0]	R/W	00b	GPIO3/OCCA PWM time base selection Selects the time base used for the GPIO3/OCCA PWM generation when the GPIO3/OCCA pin is configured as an output as well as the time base used for the PWM encoder. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
13:7	GPIO3_LL_PWM_HC[6:0]	R/W	0000000b	GPIO3/OCCA logic low level PWM high counter Sets the high period of the PWM for a logic low level of GPIO3/OCCA. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO3/OCCA logic low level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO3/OCCA logic low level as static low.
6:0	GPIO3_LL_PWM_LC[6:0]	R/W	1111111b	GPIO3/OCCA logic low level PWM low counter Sets the low period of the PWM for a logic low level of GPIO3/OCCA. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO3/OCCA logic low level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO3/OCCA logic low level as static low.

### 9.6.1.49 GPIO3\_LH\_PWM\_CFG Register (Address = 56h) [Reset = 3F80h]

Return to the [Summary Table](#).

**图 9-94. GPIO3\_LH\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED			GPIO3_LH_PWM_HC[6:0]				
R-00b			R/W-1111111b				
7	6	5	4	3	2	1	0
GPIO3_LH_PWM_H C[6:0]		GPIO3_LH_PWM_LC[6:0]					
R/W-1111111b		R/W-0000000b					

**表 9-75. GPIO3\_LH\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads 00b.
13:7	GPIO3_LH_PWM_HC[6:0]	R/W	1111111b	GPIO3/OCCA logic high level PWM high counter Sets the high period of the PWM for a logic high level of GPIO3/OCCA. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO3/OCCA logic high level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/OCCA logic high level as static low.
6:0	GPIO3_LH_PWM_LC[6:0]	R/W	0000000b	GPIO3/OCCA logic high level PWM low counter Sets the low period of the PWM for a logic high level of GPIO3/OCCA. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO3/OCCA logic high level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO2/OCCA logic high level as static low.

### 9.6.1.50 GPIO4\_LL\_PWM\_CFG Register (Address = 57h) [Reset = 007Fh]

Return to the [Summary Table](#).

**图 9-95. GPIO4\_LL\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
GPIO4_PWM_TB[1:0]		GPIO4_LL_PWM_HC[6:0]					
R/W-00b		R/W-0000000b					
7	6	5	4	3	2	1	0
GPIO4_LL_PWM_HC[6:0]		GPIO4_LL_PWM_LC[6:0]					
R/W-0000000b		R/W-1111111b					

**表 9-76. GPIO4\_LL\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	GPIO4_PWM_TB[1:0]	R/W	00b	GPIO4/OCCB PWM time base selection Selects the time base used for the GPIO4/OCCB PWM generation when the GPIO4/OCCB pin is configured as an output as well as the time base used for the PWM encoder 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
13:7	GPIO4_LL_PWM_HC[6:0]	R/W	0000000b	GPIO4/OCCB logic low level PWM high counter Sets the high period of the PWM for a logic low level of GPIO4/OCCB. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO4/OCCB logic low level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO4/OCCB logic low level as static low.
6:0	GPIO4_LL_PWM_LC[6:0]	R/W	1111111b	GPIO4/OCCB logic low level PWM low counter Sets the low period of the PWM for a logic low level of GPIO4/OCCB. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO4/OCCB logic low level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO4/OCCB logic low level as static low.



### 9.6.1.51 GPIO4\_LH\_PWM\_CFG Register (Address = 58h) [Reset = 3F80h]

Return to the [Summary Table](#).

**图 9-96. GPIO4\_LH\_PWM\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED			GPIO4_LH_PWM_HC[6:0]				
R-00b			R/W-1111111b				
7	6	5	4	3	2	1	0
GPIO4_LH_PWM_H C[6:0]		GPIO4_LH_PWM_LC[6:0]					
R/W-1111111b		R/W-0000000b					

**表 9-77. GPIO4\_LH\_PWM\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	00b	Reserved Always reads 00b.
13:7	GPIO4_LH_PWM_HC[6:0]	R/W	1111111b	GPIO4BOCCB logic high level PWM high counter Sets the high period of the PWM for a logic high level of GPIO4. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM high time = (PWM high counter value x PWM time base) Setting the PWM high counter value to 0000000b configures the GPIO4 logic high level as static low. Setting both the PWM high and low counter values to 0000000b configures the GPIO4/OCCB logic high level as static low.
6:0	GPIO4_LH_PWM_LC[6:0]	R/W	0000000b	GPIO4/OCCB logic high level PWM low counter Sets the low period of the PWM for a logic high level of GPIO4/OCCB. PWM period = (PWM high counter value + PWM low counter value) x PWM time base PWM low time = (PWM low counter value x PWM time base) Setting the PWM low counter value to 0000000b configures the GPIO4/OCCB logic high level as static high. Setting both the PWM high and low counter values to 0000000b configures the GPIO4/OCCB logic high level as static low.

**9.6.1.52 SPARE\_59h Register (Address = 59h) [Reset = 5555h]**

Return to the [Summary Table](#).

**图 9-97. SPARE\_59h Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0101010101010101b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0101010101010101b							

**表 9-78. SPARE\_59h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0101010101010101b	Spare bits Provided as R/W bits as a means to check the register map section 1 CRC. Bit settings have no effect.

### 9.6.1.53 REGISTER\_MAP1\_CRC Register (Address = 7Eh) [Reset = 0000h]

Return to the [Summary Table](#).

**図 9-98. REGISTER\_MAP1\_CRC Register**

15	14	13	12	11	10	9	8
REG_MAP1_CRC_VALUE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_MAP1_CRC_VALUE[15:0]							
R/W-0000000000000000b							

**表 9-79. REGISTER\_MAP1\_CRC Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	REG_MAP1_CRC_VALUE[15:0]	R/W	0000000000000000 000b	Register map CRC value for section 1 Register map CRC value for section 1.

### 9.6.1.54 REGMAP2\_TDACA\_CFG Register (Address = 80h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-99. REGMAP2\_TDACA\_CFG Register**

15	14	13	12	11	10	9	8
REG_MAP2_CRC_EN		RESERVED					
R/W-0b		R-0000000000000b					
7	6	5	4	3	2	1	0
RESERVED					TDACA_VALUE[2:0]		
R-0000000000000b					R/W-000b		

**表 9-80. REGMAP2\_TDACA\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	REG_MAP2_CRC_EN	R/W	0b	Register map section 2 CRC enable Enables the register map CRC for section 2 (register address space from 80h to A3h). 0b = Disabled 1b = Enabled
14:3	RESERVED	R	0000000000000b	Reserved Always reads 0000000000000b.
2:0	TDACA_VALUE[2:0]	R/W	000b	Test DAC A output value Selects the output value of Test DAC A. 000b = 1 x VREFA/40 001b = 2 x VREFA/40 010b = 4 x VREFA/40 011b = 9 x VREFA/40 100b = 18 x VREFA/40 101b = 36 x VREFA/40 110b = -4 x VREFA/40 111b = -9 x VREFA/40

### 9.6.1.55 GPIOA\_CFG Register (Address = 81h) [Reset = 8000h]

Return to the [Summary Table](#).

**图 9-100. GPIOA\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED	SPARE[2:0]		GPIO1A_FMT		GPIO0A_FMT	GPIO1A_DIR	GPIO0A_DIR
R-1b	R/W-000b		R/W-0b		R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
GPIO1A_PWM_TB[1:0]		GPIO0A_PWM_TB[1:0]		SPARE[1:0]		GPO1A_DAT	GPO0A_DAT
R/W-00b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

**表 9-81. GPIOA\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b	Reserved Always reads 1b.
14:12	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
11	GPIO1A_FMT	R/W	0b	GPIO1A format Configures GPIO1A for static input and output levels or for PWM input levels. 0b = When GPIO1A is configured as a digital input: Logic levels are based on static input levels. When GPIO1A is configured as a digital output: Output with static output levels. 1b = When GPIO1A is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO1A is configured as a digital output: Output with static output levels. GPIO1A does not have PWM output capability.
10	GPIO0A_FMT	R/W	0b	GPIO0A format Configures GPIO0A for static input and output levels or for PWM input levels. 0b = When GPIO0A is configured as a digital input: Logic levels are based on static input levels. When GPIO0A is configured as a digital output: Output with static output levels. 1b = When GPIO0A is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO0A is configured as a digital output: Output with static output levels. GPIO0A does not have PWM output capability.
9	GPIO1A_DIR	R/W	0b	GPIO1A direction Configures GPIO1A as a digital input or digital output. 0b = Digital input 1b = Digital output
8	GPIO0A_DIR	R/W	0b	GPIO0A direction Configures GPIO0A as a digital input or digital output. 0b = Digital input 1b = Digital output
7:6	GPIO1A_PWM_TB[1:0]	R/W	00b	GPIO1A PWM time base selection Selects the time base used for the PWM encoder when GPIO1A is configured as a digital input. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
5:4	GPIO0A_PWM_TB[1:0]	R/W	00b	GPIO0A PWM time base selection Selects the time base used for the PWM encoder when GPIO0A is configured as a digital input. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
3:2	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
1	GPO1A_DAT	R/W	0b	GPIO1A output data Output value of GPIO1A when configured as a digital output. Bit setting has not effect when GPIO1A is configured as a digital input. 0b = Low 1b = High
0	GPO0A_DAT	R/W	0b	GPIO0A output data Output value of GPIO0A when configured as a digital output. Bit setting has not effect when GPIO0A is configured as a digital input. 0b = Low 1b = High

### 9.6.1.56 ADC1A\_CFG1 Register (Address = 82h) [Reset = 0400h]

Return to the [Summary Table](#).

**图 9-101. ADC1A\_CFG1 Register**

15	14	13	12	11	10	9	8
RESERVED				CONV_MODE1A	OSR1A[2:0]		
R-0000b				R/W-0b	R/W-100b		
7	6	5	4	3	2	1	0
RESERVED				GC1A_EN	GC1A_DELAY[2:0]		
R-0000b				R/W-0b	R/W-000b		

**表 9-82. ADC1A\_CFG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b.
11	CONV_MODE1A	R/W	0b	Conversion mode selection Selects the conversion mode for ADC1A. 0b = Continuous-conversion mode 1b = Single-shot conversion mode
10:8	OSR1A[2:0]	R/W	100b	Oversampling ratio selection Selects the oversampling ratio for ADC1A. The data rate calculates to $f_{MOD} / OSR$ . 000b = 64 001b = 128 010b = 256 011b = 512 100b = 1024 101b = 2048 110b = 4096 111b = 8192
7:4	RESERVED	R	0000b	Reserved Always reads 0000b.
3	GC1A_EN	R/W	0b	Global-chop mode enable Enables the global-chop mode for ADC1A. 0b = Disabled 1b = Enabled
2:0	GC1A_DELAY[2:0]	R/W	000b	Global-chop mode delay time selection Selects the delay time in global-chop mode for ADC1A. 000b = $2 \times t_{MOD}$ 001b = $4 \times t_{MOD}$ 010b = $8 \times t_{MOD}$ 011b = $16 \times t_{MOD}$ 100b = $32 \times t_{MOD}$ 101b = $64 \times t_{MOD}$ 110b = $128 \times t_{MOD}$ 111b = $256 \times t_{MOD}$

### 9.6.1.57 ADC1A\_CFG2 Register (Address = 83h) [Reset = 8010h]

Return to the [Summary Table](#).

**图 9-102. ADC1A\_CFG2 Register**

15	14	13	12	11	10	9	8
ADC1A_EN	RESERVED			GAIN1A[1:0]		MUX1A[1:0]	
R/W-1b	R-000b			R/W-00b		R/W-00b	
7	6	5	4	3	2	1	0
RESERVED		OWD1A_SOURCE_MUX	OWD1A_SINK_MUX	OWD1A_SOURCE_VALUE[1:0]		OWD1A_SINK_VALUE[1:0]	
R-00b		R/W-0b	R/W-1b	R/W-00b		R/W-00b	

**表 9-83. ADC1A\_CFG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ADC1A_EN	R/W	1b	ADC1A enable Enables ADC1A. The conversion data of ADC1A reset to 000000h and the conversion counter CONV1A_COUNT[1:0] resets to 00b when ADC1A is disabled or when the device is put in standby or power-down mode. 0b = Disabled 1b = Enabled
14:12	RESERVED	R	000b	Reserved Always reads 000b.
11:10	GAIN1A[1:0]	R/W	00b	ADC1A gain selection Selects the gain (FSR = full scale range) of ADC1A. Gains 16 and 32 are digital gains using analog gain = 8. 00b = 4 01b = 8 10b = 16 11b = 32
9:8	MUX1A[1:0]	R/W	00b	ADC1A multiplexer channel selection Selects the multiplexer channel for ADC1A. 00b = AINp = CPA, AINn = CNA 01b = AINp = CNA, AINn = CPA 10b = Internal short to AGNDA. Analog inputs CPA, CNA disconnected from ADC1A. 11b = Test DAC B output
7:6	RESERVED	R	00b	Reserved Always reads 00b.
5	OWD1A_SOURCE_MUX	R/W	0b	ADC1A current source multiplexer selection Selects the multiplexer channel for the ADC1A current source. 0b = CPA 1b = CNA
4	OWD1A_SINK_MUX	R/W	1b	ADC1A current sink multiplexer selection Selects the multiplexer channel for the ADC1A current sink. 0b = CPA 1b = CNA
3:2	OWD1A_SOURCE_VALUE[1:0]	R/W	00b	ADC1A current source value selection Selects the current value for the ADC1A current source. 00b = Off 01b = 4 µA 10b = 40 µA 11b = 240 µA
1:0	OWD1A_SINK_VALUE[1:0]	R/W	00b	ADC1A current sink value selection Selects the current value for the ADC1A current sink. 00b = Off 01b = 4 µA 10b = 40 µA 11b = 240 µA

**9.6.1.58 ADC1A\_OCAL\_MSB Register (Address = 84h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-103. ADC1A\_OCAL\_MSB Register**

15	14	13	12	11	10	9	8
OCAL1A[23:8]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
OCAL1A[23:8]							
R/W-0000000000000000b							

**表 9-84. ADC1A\_OCAL\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCAL1A[23:8]	R/W	0000000000000000 000b	ADC1A offset calibration bits [23:8] Value provided in two's complement format. LSB size = (2 x VREFA) / (GAIN1A x 2 <sup>24</sup> )



**9.6.1.59 ADC1A\_OCAL\_LSB Register (Address = 85h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-104. ADC1A\_OCAL\_LSB Register**

15	14	13	12	11	10	9	8
OCAL1A[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

**表 9-85. ADC1A\_OCAL\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	OCAL1A[7:0]	R/W	00000000b	ADC1A offset calibration bits [7:0] Value provided in two's complement format. LSB size = $(2 \times VREFA) / (GAIN1A \times 2^{24})$
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b.

**9.6.1.60 ADC1A\_GCAL Register (Address = 86h) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-105. ADC1A\_GCAL Register**

15	14	13	12	11	10	9	8
GCAL1A[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
GCAL1A[15:0]							
R/W-0000000000000000b							

**表 9-86. ADC1A\_GCAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	GCAL1A[15:0]	R/W	0000000000000000b	ADC1A gain calibration bits [15:0] Value provided in two's complement format. LSB size = $1/2^{16} = 0.000015$ Mapping: 0111111111111111b = 1.499985 0000000000000001b = 1.000015 0000000000000000b = 1 1111111111111111b = 0.999985 1000000000000000b = 0.5

### 9.6.1.61 OCCA\_CFG Register (Address = 87h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-106. OCCA\_CFG Register**

15	14	13	12	11	10	9	8	
OCCA_EN	OCCA_POL	RESERVED	OCCA_NUM[4:0]					
R/W-0b	R/W-0b	R/W-0b	R/W-00000b					
7	6	5	4	3	2	1	0	
RESERVED								
R-00000000b								

**表 9-87. OCCA\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	OCCA_EN	R/W	0b	ADC1A overcurrent comparator enable Enables the digital fast filter and digital comparator on ADC1A. ADC1A must be enabled to use the overcurrent comparator. The fast filter is not affected by the STARTA and STOPA bits. 0b = Disabled 1b = Enabled
14	OCCA_POL	R/W	0b	OCCA pin polarity selection Selects the polarity of the OCCA pin. The actual output behavior of the GPIO3/OCCA pin, when configured as OCCA output in the GPIO3_SRC bit, depends on the GPIO3_FMT setting. An OCCA fault is active when any of the OCCA_HTn or OCCA_LTn bits are active. 0b = Active low. In case of a fault a logic low level is driven. 1b = Active high. In case of a fault a logic high level is driven.
13	RESERVED	R/W	0b	Reserved Always write 0b.
12:8	OCCA_NUM[4:0]	R/W	00000b	ADC1A overcurrent comparator deglitch filter selection Selects the number of conversions the output of the ADC1A digital fast filter must exceed the set high or low thresholds to trip the OCCA_HTn or OCCA_LTn comparator output. The fast filter path uses a SINC3 filter with a fixed OSR = 64. The counter starts again whenever the digital fast filter output falls below the threshold, means there is no hysteresis. 00000b = 1 00001b = 2 00010b = 3 00011b = 4 00100b = 5 00101b = 6 00110b = 7 00111b = 8 01000b = 9 01001b = 10 01010b = 12 01011b = 14 01100b = 16 01101b = 18 01110b = 20 01111b = 22 10000b = 24 10001b = 26 10010b = 28 10011b = 32 10100b = 40 10101b = 48 10110b = 56 10111b = 64 11000b = 72 11001b = 80 11010b = 88 11011b = 96 11100b = 104 11101b = 112 11110b = 120 11111b = 128
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

**9.6.1.62 OCCA\_HIGH\_THRESHOLD Register (Address = 88h) [Reset = 7FFFh]**

Return to the [Summary Table](#).

**图 9-107. OCCA\_HIGH\_THRESHOLD Register**

15	14	13	12	11	10	9	8
OCCA_HIGH_TH[15:0]							
R/W-0111111111111111b							
7	6	5	4	3	2	1	0
OCCA_HIGH_TH[15:0]							
R/W-0111111111111111b							

**表 9-88. OCCA\_HIGH\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCCA_HIGH_TH[15:0]	R/W	0111111111111111 1b	ADC1A overcurrent comparator high threshold bits [15:0] Value provided in two's complement format. LSB size = $(2 \times VREFA) / (GAIN1A \times 2^{16})$ Values larger than the high threshold trigger an OCCA_HTN event. Setting the value to +FS (= 7FFFh) disables the high threshold detection.

**9.6.1.63 OCCA\_LOW\_THRESHOLD Register (Address = 89h) [Reset = 8000h]**

Return to the [Summary Table](#).

**图 9-108. OCCA\_LOW\_THRESHOLD Register**

15	14	13	12	11	10	9	8
OCCA_LOW_TH[15:0]							
R/W-1000000000000000b							
7	6	5	4	3	2	1	0
OCCA_LOW_TH[15:0]							
R/W-1000000000000000b							

**表 9-89. OCCA\_LOW\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCCA_LOW_TH[15:0]	R/W	1000000000000000000b	ADC1A overcurrent comparator low threshold bits [15:0] Value provided in two's complement format. LSB size = $(2 \times VREFA) / (GAIN1A \times 2^{16})$ Values smaller than the low threshold trigger an OCCA_LTn event. Setting the value to -FS (= 8000h) disables the low threshold detection.

**9.6.1.64 SPARE\_8Ah Register (Address = 8Ah) [Reset = 5555h]**

Return to the [Summary Table](#).

**图 9-109. SPARE\_8Ah Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0101010101010101b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0101010101010101b							

**表 9-90. SPARE\_8Ah Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0101010101010101b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.

### 9.6.1.65 ADC2A\_CFG1 Register (Address = 8Bh) [Reset = 8010h]

Return to the [Summary Table](#).

**图 9-110. ADC2A\_CFG1 Register**

15	14	13	12	11	10	9	8
ADC2A_EN	RESERVED				VCMA_EN	OWD2A_SOURCE_MUX[2:0]	
R/W-1b	R-0000b				R/W-0b	R/W-000b	
7	6	5	4	3	2	1	0
OWD2A_SOURCE_MUX[2:0]	OWD2A_SINK_MUX[2:0]			OWD2A_SOURCE_VALUE[1:0]		OWD2A_SINK_VALUE[1:0]	
R/W-000b	R/W-001b			R/W-00b		R/W-00b	

**表 9-91. ADC2A\_CFG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ADC2A_EN	R/W	1b	ADC2A enable Enables ADC2A. Only change settings of registers from address 8Ch to 9Fh of ADC2A when ADC2A is disabled. The conversion data of ADC2A reset to 0000h and the sequence counter SEQ2A_COUNT[1:0] resets to 00b when ADC2A is disabled or when the device is put in standby or power-down mode. 0b = Disabled 1b = Enabled
14:11	RESERVED	R	0000b	Reserved Always reads 0000b.
10	VCMA_EN	R/W	0b	Common-mode output buffer VCMA enable Enables the common-mode output buffer VCMA on analog input V7A. 0b = Disabled 1b = Enabled
9:7	OWD2A_SOURCE_MUX[2:0]	R/W	000b	ADC2A current source multiplexer selection Selects the multiplexer channel for the ADC2A current source. 000b = V0A 001b = V1A 010b = V2A 011b = V3A 100b = V4A 101b = V5A 110b = V6A 111b = V7A
6:4	OWD2A_SINK_MUX[2:0]	R/W	001b	ADC2A current sink multiplexer selection Selects the multiplexer channel for the ADC2A current sink. 000b = V0A 001b = V1A 010b = V2A 011b = V3A 100b = V4A 101b = V5A 110b = V6A 111b = V7A
3:2	OWD2A_SOURCE_VALUE[1:0]	R/W	00b	ADC2A current source value selection Selects the current value for the ADC2A current source. 00b = Off 01b = 4 $\mu$ A 10b = 40 $\mu$ A 11b = 240 $\mu$ A
1:0	OWD2A_SINK_VALUE[1:0]	R/W	00b	ADC2A current sink value selection Selects the current value for the ADC2A current sink. 00b = Off 01b = 4 $\mu$ A 10b = 40 $\mu$ A 11b = 240 $\mu$ A

### 9.6.1.66 ADC2A\_CFG2 Register (Address = 8Ch) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-111. ADC2A\_CFG2 Register**

15	14	13	12	11	10	9	8
SEQ2A_MODE[1:0]		RESERVED			MUX2A_DELAY[2:0]		
R/W-00b		R-000b			R/W-000b		
7	6	5	4	3	2	1	0
RESERVED						OSR2A[1:0]	
R-000000b						R/W-00b	

**表 9-92. ADC2A\_CFG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	SEQ2A_MODE[1:0]	R/W	00b	ADC2A sequencer mode selection Selects the way the ADC2A sequencer starts a new sequence. Setting the SEQ2A_START bit always aborts and restarts an ongoing sequence in all modes. 00b = Single-shot sequence mode based on SEQ2A_START bit (ADC2A runs one time through the sequence after the SEQ2A_START bit is set) 01b = Single-shot sequence mode based on ADC1A conversion starts or SEQ2A_START bit. This setting is only useful when ADC1A is configured for continuous-conversion mode. Sequences are started at the falling edge of DRDYAn or when the SEQ2A_START bit is set. Conversion starts triggered by the DRDYAn signal are ignored, that is do not abort and restart a sequence, while a sequence is ongoing. 10b = Continuous sequence mode based on SEQ2A_START bit 11b = Continuous sequence mode based on SEQ2A_START bit
13:11	RESERVED	R	000b	Reserved Always reads 00b.
10:8	MUX2A_DELAY[2:0]	R/W	000b	ADC2A multiplexer delay time selection Selects the delay time before starting conversion on the next sequence step. 000b = $16 \times t_{MCLK}$ (= 2 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 001b = $64 \times t_{MCLK}$ (= 7.8 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 010b = $128 \times t_{MCLK}$ (= 15.6 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 011b = $256 \times t_{MCLK}$ (= 31.2 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 100b = $512 \times t_{MCLK}$ (= 62.5 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 101b = $1024 \times t_{MCLK}$ (= 124.9 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 110b = $2048 \times t_{MCLK}$ (= 249.9 $\mu$ s for $f_{MCLK} = 8.192$ MHz) 111b = $4096 \times t_{MCLK}$ (= 499.7 $\mu$ s for $f_{MCLK} = 8.192$ MHz)
7:2	RESERVED	R	000000b	Reserved Always reads 000000b.
1:0	OSR2A[1:0]	R/W	00b	ADC2A oversampling ratio selection Selects the oversampling ratio for ADC2A. 00b = 64 (SINC3 OSR = 64, conversion time = $384 \times t_{MCLK}$ ) 01b = 128 (SINC3 OSR = 64, SINC1 OSR = 2, conversion time = $512 \times t_{MCLK}$ ) 10b = 256 (SINC3 OSR = 64, SINC1 OSR = 4, conversion time = $768 \times t_{MCLK}$ ) 11b = 512 (SINC3 OSR = 64, SINC1 OSR = 8, conversion time = $1280 \times t_{MCLK}$ )



**9.6.1.67 SPARE\_8Dh Register (Address = 8Dh) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-112. SPARE\_8Dh Register**

15	14	13	12	11	10	9	8
RESERVED							
R-00000000b							
7	6	5	4	3	2	1	0
SPARE[7:0]							
R/W-00000000b							

**表 9-93. SPARE\_8Dh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	00000000b	Reserved Always reads 00000000b.
7:0	SPARE[7:0]	R/W	00000000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.

**9.6.1.68 ADC2A\_OCAL Register (Address = 8Eh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-113. ADC2A\_OCAL Register**

15	14	13	12	11	10	9	8
OCAL2A[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
OCAL2A[15:0]							
R/W-0000000000000000b							

**表 9-94. ADC2A\_OCAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCAL2A[15:0]	R/W	0000000000000000 000b	ADC2A offset calibration bits [15:0] Value provided in two's complement format. GAIN2A = 1: LSB size = $(2 \times VREFA) / 2^{16}$ GAIN2A = 2, 4: LSB size = $(2 \times VREFA) / (2 \times 2^{16})$

**9.6.1.69 ADC2A\_GCAL Register (Address = 8Fh) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-114. ADC2A\_GCAL Register**

15	14	13	12	11	10	9	8
GCAL2A[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
GCAL2A[15:0]							
R/W-0000000000000000b							

**表 9-95. ADC2A\_GCAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	GCAL2A[15:0]	R/W	0000000000000000b	ADC2A gain calibration bits [15:0] Value provided in two's complement format. LSB size = $1/2^{16} = 0.000015$ Mapping: 0111111111111111b = 1.499985 0000000000000001b = 1.000015 0000000000000000b = 1 1111111111111111b = 0.999985 1000000000000000b = 0.5

### 9.6.1.70 SEQ2A\_STEP0\_CFG Register (Address = 90h) [Reset = 0000h]

Return to the [Summary Table](#).

**9-115. SEQ2A\_STEP0\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP0_EN		SEQ2A_STEP0_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP0_CH_N	SEQ2A_STEP0_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0000b			

**表 9-96. SEQ2A\_STEP0\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP0_EN	R/W	0b	ADC2A sequence step 0 enable Enables sequence step 0 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP0_GAIN[1:0]	R/W	00b	ADC2A sequence step 0 gain selection Selects the gain of ADC2A for sequence step 0. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP0_CH_N	R/W	0b	ADC2A sequence step 0 negative input channel selection Selects the negative ADC2A analog input for sequence step 0. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP0_CH_P[3:0]	R/W	0000b	ADC2A sequence step 0 positive input channel selection Selects the positive ADC2A analog input for sequence step 0. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP0_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.71 SEQ2A\_STEP1\_CFG Register (Address = 91h) [Reset = 0001h]

Return to the [Summary Table](#).

**9-116. SEQ2A\_STEP1\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP1_EN		SEQ2A_STEP1_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP1_CH_N	SEQ2A_STEP1_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0001b			

**表 9-97. SEQ2A\_STEP1\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP1_EN	R/W	0b	ADC2A sequence step 1 enable Enables sequence step 1 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP1_GAIN[1:0]	R/W	00b	ADC2A sequence step 1 gain selection Selects the gain of ADC2A for sequence step 1. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP1_CH_N	R/W	0b	ADC2A sequence step 1 negative input channel selection Selects the negative ADC2A analog input for sequence step 1. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP1_CH_P[3:0]	R/W	0001b	ADC2A sequence step 1 positive input channel selection Selects the positive ADC2A analog input for sequence step 1. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP1_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.72 SEQ2A\_STEP2\_CFG Register (Address = 92h) [Reset = 0002h]

Return to the [Summary Table](#).

**9-117. SEQ2A\_STEP2\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP2_EN		SEQ2A_STEP2_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP2_CH_N	SEQ2A_STEP2_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0010b			

**表 9-98. SEQ2A\_STEP2\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP2_EN	R/W	0b	ADC2A sequence step 2 enable Enables sequence step 2 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP2_GAIN[1:0]	R/W	00b	ADC2A sequence step 2 gain selection Selects the gain of ADC2A for sequence step 2. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP2_CH_N	R/W	0b	ADC2A sequence step 2 negative input channel selection Selects the negative ADC2A analog input for sequence step 2. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP2_CH_P[3:0]	R/W	0010b	ADC2A sequence step 2 positive input channel selection Selects the positive ADC2A analog input for sequence step 2. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP2_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.73 SEQ2A\_STEP3\_CFG Register (Address = 93h) [Reset = 0003h]

Return to the [Summary Table](#).

**☒ 9-118. SEQ2A\_STEP3\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP3_EN		SEQ2A_STEP3_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP3_CH_N	SEQ2A_STEP3_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0011b			

**表 9-99. SEQ2A\_STEP3\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP3_EN	R/W	0b	ADC2A sequence step 3 enable Enables sequence step 3 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP3_GAIN[1:0]	R/W	00b	ADC2A sequence step 3 gain selection Selects the gain of ADC2A for sequence step 3. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP3_CH_N	R/W	0b	ADC2A sequence step 3 negative input channel selection Selects the negative ADC2A analog input for sequence step 3. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP3_CH_P[3:0]	R/W	0011b	ADC2A sequence step 3 positive input channel selection Selects the positive ADC2A analog input for sequence step 3. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP3_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.74 SEQ2A\_STEP4\_CFG Register (Address = 94h) [Reset = 0004h]

Return to the [Summary Table](#).

**图 9-119. SEQ2A\_STEP4\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP4_EN		SEQ2A_STEP4_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP4_CH_N	SEQ2A_STEP4_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0100b			

**表 9-100. SEQ2A\_STEP4\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP4_EN	R/W	0b	ADC2A sequence step 4 enable Enables sequence step 4 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP4_GAIN[1:0]	R/W	00b	ADC2A sequence step 4 gain selection Selects the gain of ADC2A for sequence step 4. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP4_CH_N	R/W	0b	ADC2A sequence step 4 negative input channel selection Selects the negative ADC2A analog input for sequence step 4. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP4_CH_P[3:0]	R/W	0100b	ADC2A sequence step 4 positive input channel selection Selects the positive ADC2A analog input for sequence step 4. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP4_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)



### 9.6.1.75 SEQ2A\_STEP5\_CFG Register (Address = 95h) [Reset = 0005h]

Return to the [Summary Table](#).

**图 9-120. SEQ2A\_STEP5\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP5_EN		SEQ2A_STEP5_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP5_CH_N	SEQ2A_STEP5_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0101b			

**表 9-101. SEQ2A\_STEP5\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP5_EN	R/W	0b	ADC2A sequence step 5 enable Enables sequence step 5 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP5_GAIN[1:0]	R/W	00b	ADC2A sequence step 5 gain selection Selects the gain of ADC2A for sequence step 5. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP5_CH_N	R/W	0b	ADC2A sequence step 5 negative input channel selection Selects the negative ADC2A analog input for sequence step 5. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP5_CH_P[3:0]	R/W	0101b	ADC2A sequence step 5 positive input channel selection Selects the positive ADC2A analog input for sequence step 5. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP5_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.76 SEQ2A\_STEP6\_CFG Register (Address = 96h) [Reset = 0006h]

Return to the [Summary Table](#).

**图 9-121. SEQ2A\_STEP6\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP6_EN		SEQ2A_STEP6_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP6_CH_N	SEQ2A_STEP6_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0110b			

**表 9-102. SEQ2A\_STEP6\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP6_EN	R/W	0b	ADC2A sequence step 6 enable Enables sequence step 6 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP6_GAIN[1:0]	R/W	00b	ADC2A sequence step 6 gain selection Selects the gain of ADC2A for sequence step 6. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP6_CH_N	R/W	0b	ADC2A sequence step 6 negative input channel selection Selects the negative ADC2A analog input for sequence step 6. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP6_CH_P[3:0]	R/W	0110b	ADC2A sequence step 6 positive input channel selection Selects the positive ADC2A analog input for sequence step 6. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP6_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.77 SEQ2A\_STEP7\_CFG Register (Address = 97h) [Reset = 0007h]

Return to the [Summary Table](#).

**图 9-122. SEQ2A\_STEP7\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP7_EN		SEQ2A_STEP7_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP7_CH_N	SEQ2A_STEP7_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-0111b			

**表 9-103. SEQ2A\_STEP7\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP7_EN	R/W	0b	ADC2A sequence step 7 enable Enables sequence step 7 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP7_GAIN[1:0]	R/W	00b	ADC2A sequence step 7 gain selection Selects the gain of ADC2A for sequence step 7. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP7_CH_N	R/W	0b	ADC2A sequence step 7 negative input channel selection Selects the negative ADC2A analog input for sequence step 7. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP7_CH_P[3:0]	R/W	0111b	ADC2A sequence step 7 positive input channel selection Selects the positive ADC2A analog input for sequence step 7. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP7_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.78 SEQ2A\_STEP8\_CFG Register (Address = 98h) [Reset = 0008h]

Return to the [Summary Table](#).

**图 9-123. SEQ2A\_STEP8\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP8_EN		SEQ2A_STEP8_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP8_CH_N	SEQ2A_STEP8_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1000b			

**表 9-104. SEQ2A\_STEP8\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP8_EN	R/W	0b	ADC2A sequence step 8 enable Enables sequence step 8 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP8_GAIN[1:0]	R/W	00b	ADC2A sequence step 8 gain selection Selects the gain of ADC2A for sequence step 8. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP8_CH_N	R/W	0b	ADC2A sequence step 8 negative input channel selection Selects the negative ADC2A analog input for sequence step 8. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP8_CH_P[3:0]	R/W	1000b	ADC2A sequence step 8 positive input channel selection Selects the positive ADC2A analog input for sequence step 8. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP8_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.79 SEQ2A\_STEP9\_CFG Register (Address = 99h) [Reset = 0009h]

Return to the [Summary Table](#).

**图 9-124. SEQ2A\_STEP9\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP9_EN		SEQ2A_STEP9_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP9_CH_N	SEQ2A_STEP9_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1001b			

**表 9-105. SEQ2A\_STEP9\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP9_EN	R/W	0b	ADC2A sequence step 9 enable Enables sequence step 9 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP9_GAIN[1:0]	R/W	00b	ADC2A sequence step 9 gain selection Selects the gain of ADC2A for sequence step 9. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP9_CH_N	R/W	0b	ADC2A sequence step 9 negative input channel selection Selects the negative ADC2A analog input for sequence step 9. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP9_CH_P[3:0]	R/W	1001b	ADC2A sequence step 9 positive input channel selection Selects the positive ADC2A analog input for sequence step 9. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP9_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.80 SEQ2A\_STEP10\_CFG Register (Address = 9Ah) [Reset = 000Ah]

Return to the [Summary Table](#).

**图 9-125. SEQ2A\_STEP10\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP10_EN		SEQ2A_STEP10_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP10_CH_N	SEQ2A_STEP10_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1010b			

**表 9-106. SEQ2A\_STEP10\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP10_EN	R/W	0b	ADC2A sequence step 10 enable Enables sequence step 10 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP10_GAIN[1:0]	R/W	00b	ADC2A sequence step 10 gain selection Selects the gain of ADC2A for sequence step 10. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP10_CH_N	R/W	0b	ADC2A sequence step 10 negative input channel selection Selects the negative ADC2A analog input for sequence step 10. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP10_CH_P[3:0]	R/W	1010b	ADC2A sequence step 10 positive input channel selection Selects the positive ADC2A analog input for sequence step 10. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP10_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.81 SEQ2A\_STEP11\_CFG Register (Address = 9Bh) [Reset = 000Bh]

Return to the [Summary Table](#).

**图 9-126. SEQ2A\_STEP11\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP11_EN		SEQ2A_STEP11_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP11_CH_N	SEQ2A_STEP11_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1011b			

**表 9-107. SEQ2A\_STEP11\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP11_EN	R/W	0b	ADC2A sequence step 11 enable Enables sequence step 11 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP11_GAIN[1:0]	R/W	00b	ADC2A sequence step 11 gain selection Selects the gain of ADC2A for sequence step 11. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP11_CH_N	R/W	0b	ADC2A sequence step 11 negative input channel selection Selects the negative ADC2A analog input for sequence step 11. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP11_CH_P[3:0]	R/W	1011b	ADC2A sequence step 11 positive input channel selection Selects the positive ADC2A analog input for sequence step 11. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP11_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.82 SEQ2A\_STEP12\_CFG Register (Address = 9Ch) [Reset = 000Ch]

Return to the [Summary Table](#).

**图 9-127. SEQ2A\_STEP12\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP12_EN		SEQ2A_STEP12_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP12_CH_N	SEQ2A_STEP12_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1100b			

**表 9-108. SEQ2A\_STEP12\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP12_EN	R/W	0b	ADC2A sequence step 12 enable Enables sequence step 12 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP12_GAIN[1:0]	R/W	00b	ADC2A sequence step 12 gain selection Selects the gain of ADC2A for sequence step 12. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP12_CH_N	R/W	0b	ADC2A sequence step 12 negative input channel selection Selects the negative ADC2A analog input for sequence step 12. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP12_CH_P[3:0]	R/W	1100b	ADC2A sequence step 12 positive input channel selection Selects the positive ADC2A analog input for sequence step 12. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP12_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)



### 9.6.1.83 SEQ2A\_STEP13\_CFG Register (Address = 9Dh) [Reset = 000Dh]

Return to the [Summary Table](#).

**图 9-128. SEQ2A\_STEP13\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP13_EN		SEQ2A_STEP13_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP13_CH_N	SEQ2A_STEP13_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1101b			

**表 9-109. SEQ2A\_STEP13\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP13_EN	R/W	0b	ADC2A sequence step 13 enable Enables sequence step 13 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP13_GAIN[1:0]	R/W	00b	ADC2A sequence step 13 gain selection Selects the gain of ADC2A for sequence step 13. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP13_CH_N	R/W	0b	ADC2A sequence step 13 negative input channel selection Selects the negative ADC2A analog input for sequence step 13. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP13_CH_P[3:0]	R/W	1101b	ADC2A sequence step 13 positive input channel selection Selects the positive ADC2A analog input for sequence step 13. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP13_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.84 SEQ2A\_STEP14\_CFG Register (Address = 9Eh) [Reset = 000Eh]

Return to the [Summary Table](#).

**图 9-129. SEQ2A\_STEP14\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP14_EN		SEQ2A_STEP14_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP14_CH_N	SEQ2A_STEP14_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1110b			

**表 9-110. SEQ2A\_STEP14\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP14_EN	R/W	0b	ADC2A sequence step 14 enable Enables sequence step 14 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP14_GAIN[1:0]	R/W	00b	ADC2A sequence step 14 gain selection Selects the gain of ADC2A for sequence step 14. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP14_CH_N	R/W	0b	ADC2A sequence step 14 negative input channel selection Selects the negative ADC2A analog input for sequence step 14. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP14_CH_P[3:0]	R/W	1110b	ADC2A sequence step 14 positive input channel selection Selects the positive ADC2A analog input for sequence step 14. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP14_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

### 9.6.1.85 SEQ2A\_STEP15\_CFG Register (Address = 9Fh) [Reset = 000Fh]

Return to the [Summary Table](#).

**图 9-130. SEQ2A\_STEP15\_CFG Register**

15	14	13	12	11	10	9	8
SEQ2A_STEP15_EN		SEQ2A_STEP15_GAIN[1:0]		RESERVED			
R/W-0b		R/W-00b		R-00000000b			
7	6	5	4	3	2	1	0
RESERVED			SEQ2A_STEP15_CH_N	SEQ2A_STEP15_CH_P[3:0]			
R-00000000b			R/W-0b	R/W-1111b			

**表 9-111. SEQ2A\_STEP15\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	SEQ2A_STEP15_EN	R/W	0b	ADC2A sequence step 15 enable Enables sequence step 15 of the ADC2A sequencer. 0b = Disabled 1b = Enabled
14:13	SEQ2A_STEP15_GAIN[1:0]	R/W	00b	ADC2A sequence step 15 gain selection Selects the gain of ADC2A for sequence step 15. 00b = 1 01b = 2 10b = 4 11b = 4
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4	SEQ2A_STEP15_CH_N	R/W	0b	ADC2A sequence step 15 negative input channel selection Selects the negative ADC2A analog input for sequence step 15. 0b = AGNDA 1b = V7A
3:0	SEQ2A_STEP15_CH_P[3:0]	R/W	1111b	ADC2A sequence step 15 positive input channel selection Selects the positive ADC2A analog input for sequence step 15. For settings where the negative ADC input is automatically selected, the SEQ2A_STEP15_CH_N bit has no effect. 0000b = V0A 0001b = V1A 0010b = V2A 0011b = V3A 0100b = V4A 0101b = V5A 0110b = V6A 0111b = V7A 1000b = Temperature sensor A (negative ADC input is automatically selected) 1001b = Internal short to AGNDA, disconnected from inputs (negative ADC input is automatically selected) 1010b = Test DAC B (negative ADC input is automatically selected) 1011b = AVDD/4 (negative ADC input is automatically selected) 1100b = IOVDD/4 (negative ADC input is automatically selected) 1101b = DVDD/2 (negative ADC input is automatically selected) 1110b = APWR/103 (negative ADC input is automatically selected) 1111b = DPWR/103 (negative ADC input is automatically selected)

**9.6.1.86 SPARE\_A0h Register (Address = A0h) [Reset = 0210h]**

Return to the [Summary Table](#).

**图 9-131. SPARE\_A0h Register**

15	14	13	12	11	10	9	8
RESERVED				SPARE[1:0]		RESERVED	
R-0000b				R/W-00b		R-1000b	
7	6	5	4	3	2	1	0
RESERVED		SPARE[1:0]			RESERVED		
R-1000b		R/W-01b			R-0000b		

**表 9-112. SPARE\_A0h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b.
11:10	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
9:6	RESERVED	R	1000b	Reserved Always reads 1000b.
5:4	SPARE[1:0]	R/W	01b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
3:0	RESERVED	R	0000b	Reserved Always reads 0000b.

**9.6.1.87 SPARE\_A1h Register (Address = A1h) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-132. SPARE\_A1h Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-113. SPARE\_A1h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000 000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.

**9.6.1.88 SPARE\_A2h Register (Address = A2h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-133. SPARE\_A2h Register**

15	14	13	12	11	10	9	8
SPARE[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

**表 9-114. SPARE\_A2h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	SPARE[7:0]	R/W	00000000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b.

**9.6.1.89 SPARE\_A3h Register (Address = A3h) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-134. SPARE\_A3h Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-115. SPARE\_A3h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.

**9.6.1.90 REGISTER\_MAP2\_CRC Register (Address = BEh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-135. REGISTER\_MAP2\_CRC Register**

15	14	13	12	11	10	9	8
REG_MAP2_CRC_VALUE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_MAP2_CRC_VALUE[15:0]							
R/W-0000000000000000b							

**表 9-116. REGISTER\_MAP2\_CRC Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	REG_MAP2_CRC_VALUE[15:0]	R/W	0000000000000000 000b	Register map CRC value for section 2 Register map CRC value for section 2.



### 9.6.1.91 REGMAP3\_TDACB\_CFG Register (Address = C0h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-136. REGMAP3\_TDACB\_CFG Register**

15	14	13	12	11	10	9	8
REG_MAP3_CRC_EN		RESERVED					
R/W-0b		R-000000000000b					
7	6	5	4	3	2	1	0
RESERVED					TDACB_VALUE[2:0]		
R-000000000000b					R/W-000b		

**表 9-117. REGMAP3\_TDACB\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	REG_MAP3_CRC_EN	R/W	0b	Register map section 3 CRC enable Enables the register map CRC for section 3 (register address space from C0h to E3h). 0b = Disabled 1b = Enabled
14:3	RESERVED	R	000000000000b	Reserved Always reads 000000000000b.
2:0	TDACB_VALUE[2:0]	R/W	000b	Test DAC B output value Selects the output value of Test DAC B. 000b = 1 x VREFB/40 001b = 2 x VREFB/40 010b = 4 x VREFB/40 011b = 9 x VREFB/40 100b = 18 x VREFB/40 101b = 36 x VREFB/40 110b = -4 x VREFB/40 111b = -9 x VREFB/40

### 9.6.1.92 GPIOB\_CFG Register (Address = C1h) [Reset = 8000h]

Return to the [Summary Table](#).

**图 9-137. GPIOB\_CFG Register**

15	14	13	12	11	10	9	8
RESERVED	SPARE[2:0]		GPIO1B_FMT		GPIO0B_FMT	GPIO1B_DIR	GPIO0B_DIR
R-1b	R/W-000b		R/W-0b		R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
GPIO1B_PWM_TB[1:0]		GPIO0B_PWM_TB[1:0]		SPARE[1:0]		GPO1B_DAT	GPO0B_DAT
R/W-00b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

**表 9-118. GPIOB\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	1b	Reserved Always reads 1b.
14:12	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
11	GPIO1B_FMT	R/W	0b	GPIO1B format Configures GPIO1B for static input and output levels or for PWM input levels. 0b = When GPIO1B is configured as a digital input: Logic levels are based on static input levels. When GPIO1B is configured as a digital output: Output with static output levels. 1b = When GPIO1B is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO1B is configured as a digital output: Output with static output levels. GPIO1B does not have PWM output capability.
10	GPIO0B_FMT	R/W	0b	GPIO0B format Configures GPIO0B for static input and output levels or for PWM input levels. 0b = When GPIO0B is configured as a digital input: Logic levels are based on static input levels. When GPIO0B is configured as a digital output: Output with static output levels. 1b = When GPIO0B is configured as a digital input: Logic levels are based on PWM input decoding. When GPIO0B is configured as a digital output: Output with static output levels. GPIO0B does not have PWM output capability.
9	GPIO1B_DIR	R/W	0b	GPIO1B direction Configures GPIO1B as a digital input or digital output. 0b = Digital input 1b = Digital output
8	GPIO0B_DIR	R/W	0b	GPIO0B direction Configures GPIO0B as a digital input or digital output. 0b = Digital input 1b = Digital output
7:6	GPIO1B_PWM_TB[1:0]	R/W	00b	GPIO1B PWM time base selection Selects the time base used for the PWM encoder when GPIO1B is configured as a digital input. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
5:4	GPIO0B_PWM_TB[1:0]	R/W	00b	GPIO0B PWM time base selection Selects the time base used for the PWM encoder when GPIO0B is configured as a digital input. 00b = $16 \times t_{MCLK}$ (= 1/512 kHz for $f_{MCLK} = 8.192$ MHz) 01b = $64 \times t_{MCLK}$ (= 1/128 kHz for $f_{MCLK} = 8.192$ MHz) 10b = $256 \times t_{MCLK}$ (= 1/32 kHz for $f_{MCLK} = 8.192$ MHz) 11b = $1024 \times t_{MCLK}$ (= 1/8 kHz for $f_{MCLK} = 8.192$ MHz)
3:2	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 2 CRC. Bit settings have no effect.
1	GPO1B_DAT	R/W	0b	GPIO1B output data Output value of GPIO1B when configured as an output. Bit setting has not effect when GPIO1B is configured as a digital input. 0b = Low 1b = High
0	GPO0B_DAT	R/W	0b	GPIO0B output data Output value of GPIO0B when configured as an output. Bit setting has not effect when GPIO0B is configured as a digital input. 0b = Low 1b = High

### 9.6.1.93 ADC1B\_CFG1 Register (Address = C2h) [Reset = 0400h]

Return to the [Summary Table](#).

**图 9-138. ADC1B\_CFG1 Register**

15	14	13	12	11	10	9	8
RESERVED				CONV_MODE1B	OSR1B[2:0]		
R-0000b				R/W-0b	R/W-100b		
7	6	5	4	3	2	1	0
RESERVED				GC1B_EN	GC1B_DELAY[2:0]		
R-0000b				R/W-0b	R/W-000b		

**表 9-119. ADC1B\_CFG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b.
11	CONV_MODE1B	R/W	0b	Conversion mode selection Selects the conversion mode for ADC1B. 0b = Continuous-conversion mode 1b = Single-shot conversion mode
10:8	OSR1B[2:0]	R/W	100b	Oversampling ratio selection Selects the oversampling ratio for ADC1B. The data rate calculates to $f_{MOD} / OSR$ . 000b = 64 001b = 128 010b = 256 011b = 512 100b = 1024 101b = 2048 110b = 4096 111b = 8192
7:4	RESERVED	R	0000b	Reserved Always reads 0000b.
3	GC1B_EN	R/W	0b	Global-chop mode enable Enables the global-chop mode for ADC1B. 0b = Disabled 1b = Enabled
2:0	GC1B_DELAY[2:0]	R/W	000b	Global-chop mode delay time selection Selects the delay time in global-chop mode for ADC1B. 000b = $2 \times t_{MOD}$ 001b = $4 \times t_{MOD}$ 010b = $8 \times t_{MOD}$ 011b = $16 \times t_{MOD}$ 100b = $32 \times t_{MOD}$ 101b = $64 \times t_{MOD}$ 110b = $128 \times t_{MOD}$ 111b = $256 \times t_{MOD}$

### 9.6.1.94 ADC1B\_CFG2 Register (Address = C3h) [Reset = 8010h]

Return to the [Summary Table](#).

**图 9-139. ADC1B\_CFG2 Register**

15	14	13	12	11	10	9	8
ADC1B_EN	RESERVED			GAIN1B[1:0]	MUX1B[1:0]		
R/W-1b	R-000b			R/W-00b	R/W-00b		
7	6	5	4	3	2	1	0
RESERVED		OWD1B_SOURCE_MUX	OWD1B_SINK_MUX	OWD1B_SOURCE_VALUE[1:0]		OWD1B_SINK_VALUE[1:0]	
R-00b		R/W-0b	R/W-1b	R/W-00b		R/W-00b	

**表 9-120. ADC1B\_CFG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ADC1B_EN	R/W	1b	ADC1B enable Enables ADC1B. The conversion data of ADC1B reset to 000000h and the conversion counter CONV1B_COUNT[1:0] resets to 00b when ADC1B is disabled or when the device is put in standby or power-down mode.. 0b = Disabled 1b = Enabled
14:12	RESERVED	R	000b	Reserved Always reads 000b.
11:10	GAIN1B[1:0]	R/W	00b	ADC1B gain selection Selects the gain (FSR = full scale range) of ADC1B. Gains 16 and 32 are digital gains using analog gain = 8. 00b = 4 01b = 8 10b = 16 11b = 32
9:8	MUX1B[1:0]	R/W	00b	ADC1B multiplexer channel selection Selects the multiplexer channel for ADC1B. 00b = AINp = CPB, AINn = CNB 01b = AINp = CNB, AINn = CPB 10b = Internal short to AGNDB. Analog inputs CPB, CNB disconnected from ADC1B. 11b = Test DAC A output
7:6	RESERVED	R	00b	Reserved Always reads 00b.
5	OWD1B_SOURCE_MUX	R/W	0b	ADC1B current source multiplexer selection Selects the multiplexer channel for the ADC1B current source. 0b = CPB 1b = CNB
4	OWD1B_SINK_MUX	R/W	1b	ADC1B current sink multiplexer selection Selects the multiplexer channel for the ADC1B current sink. 0b = CPB 1b = CNB
3:2	OWD1B_SOURCE_VALUE[1:0]	R/W	00b	ADC1B current source value selection Selects the current value for the ADC1B current source. 00b = Off 01b = 4 µA 10b = 40 µA 11b = 240 µA
1:0	OWD1B_SINK_VALUE[1:0]	R/W	00b	ADC1B current sink value selection Selects the current value for the ADC1B current sink. 00b = Off 01b = 4 µA 10b = 40 µA 11b = 240 µA

**9.6.1.95 ADC1B\_OCAL\_MSB Register (Address = C4h) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-140. ADC1B\_OCAL\_MSB Register**

15	14	13	12	11	10	9	8
OCAL1B[23:8]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
OCAL1B[23:8]							
R/W-0000000000000000b							

**表 9-121. ADC1B\_OCAL\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCAL1B[23:8]	R/W	0000000000000000 000b	ADC1B offset calibration bits [23:8] Value provided in two's complement format. LSB size = $(2 \times VREFB) / (GAIN1B \times 2^{24})$

**9.6.1.96 ADC1B\_OCAL\_LSB Register (Address = C5h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-141. ADC1B\_OCAL\_LSB Register**

15	14	13	12	11	10	9	8
OCAL1B[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

**表 9-122. ADC1B\_OCAL\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	OCAL1B[7:0]	R/W	00000000b	ADC1B offset calibration bits [7:0] Value provided in two's complement format. LSB size = $(2 \times VREFB) / (GAIN1B \times 2^{24})$
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b.

**9.6.1.97 ADC1B\_GCAL Register (Address = C6h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-142. ADC1B\_GCAL Register**

15	14	13	12	11	10	9	8
GCAL1B[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
GCAL1B[15:0]							
R/W-0000000000000000b							

**表 9-123. ADC1B\_GCAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	GCAL1B[15:0]	R/W	0000000000000000b	ADC1B gain calibration bits [15:0] Value provided in two's complement format. LSB size = $1/2^{16} = 0.000015$ Mapping: 0111111111111111b = 1.499985 0000000000000001b = 1.000015 0000000000000000b = 1 1111111111111111b = 0.999985 1000000000000000b = 0.5

**9.6.1.98 OCCB\_CFG Register (Address = C7h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-143. OCCB\_CFG Register**

15	14	13	12	11	10	9	8	
OCCB_EN	OCCB_POL	RESERVED	OCCB_NUM[4:0]					
R/W-0b	R/W-0b	R/W-0b	R/W-00000b					
7	6	5	4	3	2	1	0	
RESERVED								
R-00000000b								

**表 9-124. OCCB\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	OCCB_EN	R/W	0b	ADC1B overcurrent comparator enable Enables the digital fast filter and digital comparator on ADC1B. ADC1B must be enabled to use the overcurrent comparator. The fast filter is not affected by the STARTB and STOPB bits. 0b = Disabled 1b = Enabled
14	OCCB_POL	R/W	0b	OCCB pin polarity selection Selects the polarity of the OCCB pin. The actual output behavior of the GPIO4/OCCB pin, when configured as OCCB output in the GPIO4_SRC bit, depends on the GPIO4_FMT setting. An OCCB fault is active when any of the OCCB_HTn or OCCB_LTn bits are active. 0b = Active low. In case of a fault a logic low level is driven. 1b = Active high. In case of a fault a logic high level is driven.
13	RESERVED	R/W	0b	Reserved Always write 0b.
12:8	OCCB_NUM[4:0]	R/W	00000b	ADC1B overcurrent comparator deglitch filter selection Selects the number of conversions the output of the ADC1B digital fast filter must exceed the set high or low thresholds to trip the OCCB_HTn or OCCB_LTn comparator output. The fast filter path uses a SINC3 filter with a fixed OSR = 64. The counter starts again whenever the digital fast filter output falls below the threshold, means there is no hysteresis. 00000b = 1 00001b = 2 00010b = 3 00011b = 4 00100b = 5 00101b = 6 00110b = 7 00111b = 8 01000b = 9 01001b = 10 01010b = 12 01011b = 14 01100b = 16 01101b = 18 01110b = 20 01111b = 22 10000b = 24 10001b = 26 10010b = 28 10011b = 32 10100b = 40 10101b = 48 10110b = 56 10111b = 64 11000b = 72 11001b = 80 11010b = 88 11011b = 96 11100b = 104 11101b = 112 11110b = 120 11111b = 128
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b.



**9.6.1.99 OCCB\_HIGH\_THRESHOLD Register (Address = C8h) [Reset = 7FFFh]**

Return to the [Summary Table](#).

**図 9-144. OCCB\_HIGH\_THRESHOLD Register**

15	14	13	12	11	10	9	8
OCCB_HIGH_TH[15:0]							
R/W-0111111111111111b							
7	6	5	4	3	2	1	0
OCCB_HIGH_TH[15:0]							
R/W-0111111111111111b							

**表 9-125. OCCB\_HIGH\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCCB_HIGH_TH[15:0]	R/W	0111111111111111 1b	ADC1B overcurrent comparator high threshold bits [15:0] Value provided in two's complement format. LSB size = $(2 \times VREFB) / (GAIN1B \times 2^{16})$ Values larger than the high threshold trigger an OCCB_HTN event. Setting the value to +FS (= 7FFFh) disables the high threshold detection.

**9.6.1.100 OCCB\_LOW\_THRESHOLD Register (Address = C9h) [Reset = 8000h]**

Return to the [Summary Table](#).

**图 9-145. OCCB\_LOW\_THRESHOLD Register**

15	14	13	12	11	10	9	8
OCCB_LOW_TH[15:0]							
R/W-1000000000000000b							
7	6	5	4	3	2	1	0
OCCB_LOW_TH[15:0]							
R/W-1000000000000000b							

**表 9-126. OCCB\_LOW\_THRESHOLD Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	OCCB_LOW_TH[15:0]	R/W	1000000000000000b	ADC1B overcurrent comparator low threshold bits [15:0] Value provided in two's complement format. LSB size = $(2 \times VREFB) / (GAIN1B \times 2^{16})$ Values smaller than the low threshold trigger an OCCB_LTn event. Setting the value to -FS (= 8000h) disables the low threshold detection.

### 9.6.1.101 SPARE\_CAh Register (Address = CAh) [Reset = 5555h]

Return to the [Summary Table](#).

**図 9-146. SPARE\_CAh Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0101010101010101b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0101010101010101b							

**表 9-127. SPARE\_CAh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0101010101010101b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.102 SPARE\_CBh Register (Address = CBh) [Reset = 0010h]**

Return to the [Summary Table](#).

**图 9-147. SPARE\_CBh Register**

15	14	13	12	11	10	9	8
RESERVED					SPARE[6:0]		
R-00000b					R/W-0000001b		
7	6	5	4	3	2	1	0
SPARE[6:0]				RESERVED			
R/W-0000001b				R-0000b			

**表 9-128. SPARE\_CBh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	00000b	Reserved Always reads 00000b.
10:4	SPARE[6:0]	R/W	0000001b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
3:0	RESERVED	R	0000b	Reserved Always reads 0000b.

### 9.6.1.103 SPARE\_CCh Register (Address = CCh) [Reset = 0000h]

Return to the [Summary Table](#).

**図 9-148. SPARE\_CCh Register**

15	14	13	12	11	10	9	8
SPARE[1:0]		RESERVED			SPARE[2:0]		
R/W-00b		R-000b			R/W-000b		
7	6	5	4	3	2	1	0
RESERVED						SPARE[1:0]	
R-000000b						R/W-00b	

**表 9-129. SPARE\_CCh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:14	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
13:11	RESERVED	R	000b	Reserved Always reads 00b.
10:8	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
7:2	RESERVED	R	000000b	Reserved Always reads 000000b.
1:0	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.104 SPARE\_CDh Register (Address = CDh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-149. SPARE\_CDh Register**

15	14	13	12	11	10	9	8
RESERVED							
R-00000000b							
7	6	5	4	3	2	1	0
SPARE[7:0]							
R/W-00000000b							

**表 9-130. SPARE\_CDh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	00000000b	Reserved Always reads 00000000b.
7:0	SPARE[7:0]	R/W	00000000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.105 SPARE\_CEH Register (Address = CEh) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-150. SPARE\_CEH Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-131. SPARE\_CEH Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000 000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.106 SPARE\_CFh Register (Address = CFh) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-151. SPARE\_CFh Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-132. SPARE\_CFh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000 000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.



### 9.6.1.107 SPARE\_D0h Register (Address = D0h) [Reset = 0000h]

Return to the [Summary Table](#).

**图 9-152. SPARE\_D0h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00000b				

**表 9-133. SPARE\_D0h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.108 SPARE\_D1h Register (Address = D1h) [Reset = 0001h]**

Return to the [Summary Table](#).

**图 9-153. SPARE\_D1h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00001b				

**表 9-134. SPARE\_D1h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00001b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.109 SPARE\_D2h Register (Address = D2h) [Reset = 0002h]

Return to the [Summary Table](#).

**图 9-154. SPARE\_D2h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00010b				

**表 9-135. SPARE\_D2h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00010b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.110 SPARE\_D3h Register (Address = D3h) [Reset = 0003h]**

Return to the [Summary Table](#).

**图 9-155. SPARE\_D3h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00011b				

**表 9-136. SPARE\_D3h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00011b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.111 SPARE\_D4h Register (Address = D4h) [Reset = 0004h]**

Return to the [Summary Table](#).

**图 9-156. SPARE\_D4h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00100b				

**表 9-137. SPARE\_D4h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00100b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.112 SPARE\_D5h Register (Address = D5h) [Reset = 0005h]**

Return to the [Summary Table](#).

**图 9-157. SPARE\_D5h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00101b				

**表 9-138. SPARE\_D5h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00101b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.113 SPARE\_D6h Register (Address = D6h) [Reset = 0006h]

Return to the [Summary Table](#).

**图 9-158. SPARE\_D6h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00110b				

**表 9-139. SPARE\_D6h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00110b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.114 SPARE\_D7h Register (Address = D7h) [Reset = 0007h]**

Return to the [Summary Table](#).

**图 9-159. SPARE\_D7h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-00111b				

**表 9-140. SPARE\_D7h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	00111b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.



### 9.6.1.115 SPARE\_D8h Register (Address = D8h) [Reset = 0008h]

Return to the [Summary Table](#).

**图 9-160. SPARE\_D8h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01000b				

**表 9-141. SPARE\_D8h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.116 SPARE\_D9h Register (Address = D9h) [Reset = 0009h]**

Return to the [Summary Table](#).

**图 9-161. SPARE\_D9h Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01001b				

**表 9-142. SPARE\_D9h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01001b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.117 SPARE\_DAh Register (Address = DAh) [Reset = 000Ah]

Return to the [Summary Table](#).

**图 9-162. SPARE\_DAh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01010b				

**表 9-143. SPARE\_DAh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01010b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.118 SPARE\_DBh Register (Address = DBh) [Reset = 000Bh]**

Return to the [Summary Table](#).

**图 9-163. SPARE\_DBh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01011b				

**表 9-144. SPARE\_DBh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01011b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.119 SPARE\_DCh Register (Address = DCh) [Reset = 000Ch]

Return to the [Summary Table](#).

**図 9-164. SPARE\_DCh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01100b				

**表 9-145. SPARE\_DCh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01100b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.120 SPARE\_DDh Register (Address = DDh) [Reset = 000Dh]**

Return to the [Summary Table](#).

**图 9-165. SPARE\_DDh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01101b				

**表 9-146. SPARE\_DDh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01101b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.121 SPARE\_DEh Register (Address = DEh) [Reset = 000Eh]

Return to the [Summary Table](#).

**图 9-166. SPARE\_DEh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]				RESERVED			
R/W-000b				R-00000000b			
7	6	5	4	3	2	1	0
RESERVED				SPARE[4:0]			
R-00000000b				R/W-01110b			

**表 9-147. SPARE\_DEh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01110b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.122 SPARE\_DFh Register (Address = DFh) [Reset = 000Fh]**

Return to the [Summary Table](#).

**图 9-167. SPARE\_DFh Register**

15	14	13	12	11	10	9	8
SPARE[2:0]			RESERVED				
R/W-000b			R-00000000b				
7	6	5	4	3	2	1	0
RESERVED			SPARE[4:0]				
R-00000000b			R/W-01111b				

**表 9-148. SPARE\_DFh Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:13	SPARE[2:0]	R/W	000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
12:5	RESERVED	R	00000000b	Reserved Always reads 00000000b.
4:0	SPARE[4:0]	R/W	01111b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.



### 9.6.1.123 SPARE\_E0h Register (Address = E0h) [Reset = 0210h]

Return to the [Summary Table](#).

**图 9-168. SPARE\_E0h Register**

15	14	13	12	11	10	9	8
RESERVED				SPARE[1:0]		RESERVED	
R-0000b				R/W-00b		R-1000b	
7	6	5	4	3	2	1	0
RESERVED		SPARE[1:0]			RESERVED		
R-1000b		R/W-01b			R-0000b		

**表 9-149. SPARE\_E0h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0000b	Reserved Always reads 0000b.
11:10	SPARE[1:0]	R/W	00b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
9:6	RESERVED	R	1000b	Reserved Always reads 1000b.
5:4	SPARE[1:0]	R/W	01b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
3:0	RESERVED	R	0000b	Reserved Always reads 0000b.

**9.6.1.124 SPARE\_E1h Register (Address = E1h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-169. SPARE\_E1h Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-150. SPARE\_E1h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000 000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

### 9.6.1.125 SPARE\_E2h Register (Address = E2h) [Reset = 0000h]

Return to the [Summary Table](#).

**図 9-170. SPARE\_E2h Register**

15	14	13	12	11	10	9	8
SPARE[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

**表 9-151. SPARE\_E2h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:8	SPARE[7:0]	R/W	00000000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.
7:0	RESERVED	R	00000000b	Reserved Always reads 0x00.

**9.6.1.126 SPARE\_E3h Register (Address = E3h) [Reset = 0000h]**

Return to the [Summary Table](#).

**图 9-171. SPARE\_E3h Register**

15	14	13	12	11	10	9	8
SPARE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
SPARE[15:0]							
R/W-0000000000000000b							

**表 9-152. SPARE\_E3h Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	SPARE[15:0]	R/W	0000000000000000 000b	Spare bits Provided as R/W bits as a means to check the register map section 3 CRC. Bit settings have no effect.

**9.6.1.127 REGISTER\_MAP3\_CRC Register (Address = FEh) [Reset = 0000h]**

Return to the [Summary Table](#).

**図 9-172. REGISTER\_MAP3\_CRC Register**

15	14	13	12	11	10	9	8
REG_MAP3_CRC_VALUE[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
REG_MAP3_CRC_VALUE[15:0]							
R/W-0000000000000000b							

**表 9-153. REGISTER\_MAP3\_CRC Register Field Descriptions**

Bit	Field	Type	Reset	Description
15:0	REG_MAP3_CRC_VALUE[15:0]	R/W	0000000000000000 000b	Register map CRC value for section 3 Register map CRC value for section 3.

## 10 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 10.1 Application Information

#### 10.1.1 Unused Inputs and Outputs

Follow these guidelines for unused device pin connections:

- Leave any unused ADCxy analog inputs floating or connect the unused analog inputs to AGNDy.
- Tie unused GPIO pins (GPIO0 to GPIO4, GPIO0A, GPIO1A, GPIO0B, and GPIO1B) to DGND when configured as digital inputs because excessive power-supply current can result when digital inputs are left floating.
- Tie the CLK pin to DGND if the internal main oscillator is used.
- Tie the RESETn pin to IOVDD if the host does not drive the RESETn pin. The RESETn pin has an internal pulldown resistor to DGND.
- Leave the DRDYn pin unconnected if unused or connect the pin to IOVDD with a weak pullup resistor.

#### 10.1.2 Minimum Interface Connections

The ADS131B23-Q1 requires at a minimum four pins for communication with a host microcontroller: CSn, SCLK, SDI, and SDO. CSn cannot be tied low permanently.

The following pins are optional, but connecting these pins to the host helps with device operation:

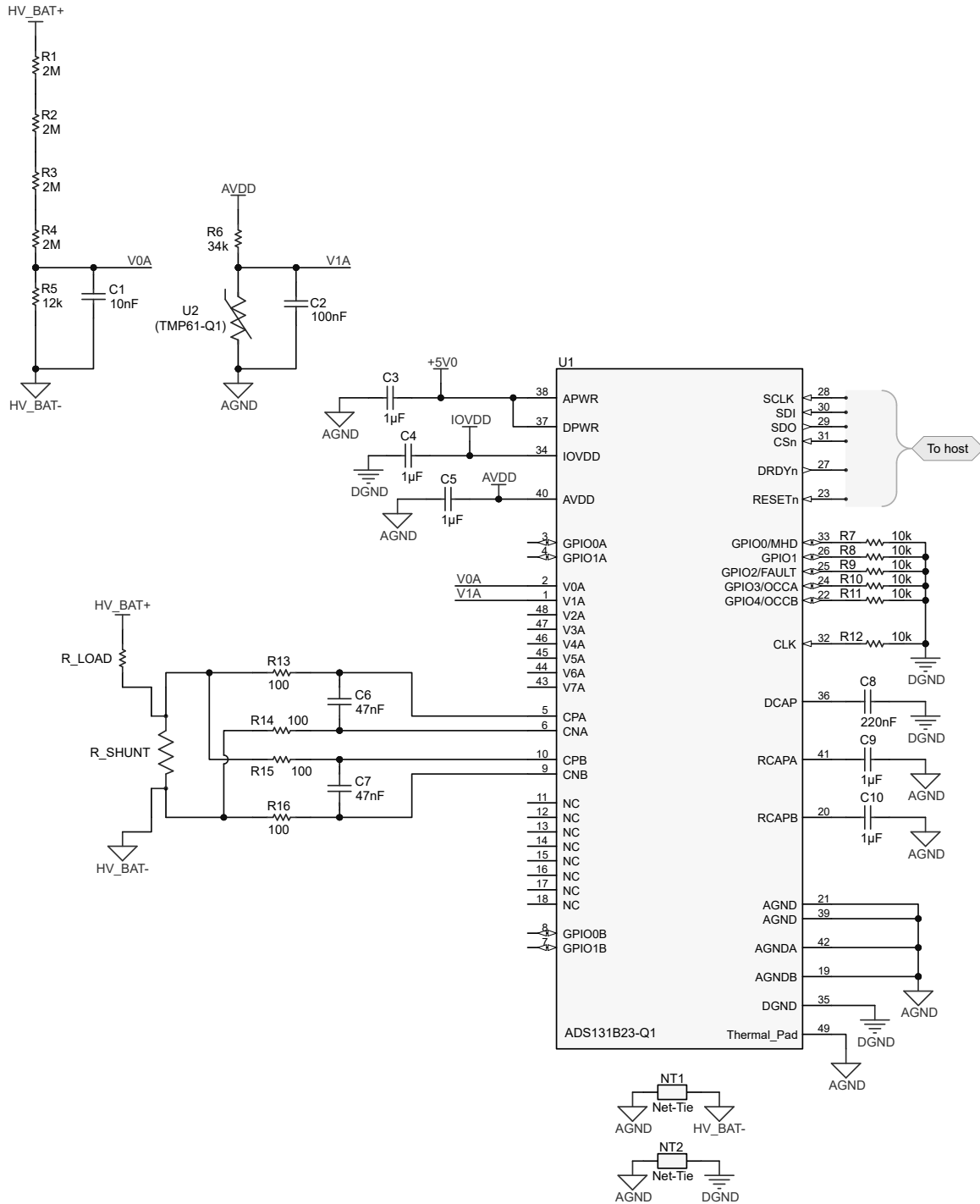
- DRDYn: Helps determine exactly when new conversion data on ADC1A or ADC1B are available.
- RESETn: If the SPI communication is corrupted (that is, if the RESET command cannot be sent), a *hardware* reset is required to recover the device. Without controlling the RESETn pin, the only way to perform a hardware reset on the device is through cycling the power supplies.
- GPIOs: The different special functions available on the various GPIO pins, such as FAULT, MHD, OCCA, and OCCB, help alert the host of device or system faults.

### 10.2 Typical Application

This section describes a typical battery management system (BMS) application circuit using the ADS131B23-Q1. The device serves the following primary functions in this BMS:

- Measure battery current redundantly through ADC1A and ADC1B with high resolution and accuracy using a low-side current shunt sensor
- Measure peak battery currents and detect overcurrent or short-circuit conditions
- Measure battery-pack voltage through ADC2A using a high-voltage resistor divider
- Measure shunt temperature through ADC2A using a linear positive temperature coefficient (PTC) thermistor, the TMP61-Q1

☒ 10-1 illustrates the front-end for the battery management system circuit design.



**10-1. The ADS131B23-Q1 in a Typical Battery Management System Application**

## 10.2.1 Design Requirements

表 10-1. Design Parameters

DESIGN PARAMETER	VALUE
<b>Current Measurement</b>	
Current measurement range	±3 kA
Current shunt value	50 μΩ
Update rate	1 ms
<b>Battery-Pack Voltage Measurement</b>	
Voltage measurement range	0 V to 800 V
<b>Shunt Temperature Measurement</b>	
Temperature measurement range	–40°C to +125°C
Thermistor type	TMP61-Q1 (10-kΩ PTC)

## 10.2.2 Detailed Design Procedure

The following sections provide guidelines for selecting the external components and the configuration of the ADS131B23-Q1 for the various measurements in this application example.

### 10.2.2.1 Current Shunt Measurement

In a typical BMS application, the current through the shunt resistor must be measured in both directions for charging and discharging the battery pack. In an overcurrent or short-circuit condition, the current can be as high as  $I_{BAT\_MAX} = \pm 3$  kA in this example application. Therefore, the maximum voltage drop across the shunt is up to  $V_{SHUNT} = R_{SHUNT} \times I_{BAT\_MAX} = 50 \mu\Omega \times \pm 3$  kA = ±150 mV.

To measure this shunt voltage, ADC1A is configured for gain = 8, which allows differential voltage measurements of  $V_{IN1A} = V_{CPA} - V_{CNA} = \pm V_{REFA} / 8 = \pm 1.25$  V / 8 = ±156 mV. The integrated charge pump in the device allows voltage measurements 312.5 mV below AGNDA while using a unipolar analog power supply. This bipolar voltage measurement capability is important because one side of the shunt is connected to the same GND potential as the AGNDA pin of the ADS131B23-Q1, which means that the absolute voltage that the device must measure is up to 150 mV below AGNDA.

To enable fast overcurrent detection within 1 ms while providing high accuracy and resolution, the ADS131B23-Q1 is configured to operate at 4 kSPS (OSR = 1024) using global-chop mode. Global-chop mode enables measurements with minimal offset error over temperature and time. The conversion time using these settings is 0.75 ms according to 式 21. The input-referred noise is approximately  $1.28 \mu V_{RMS} / \sqrt{2} = 0.91 \mu V_{RMS}$  following the explanations in the [Global-Chop Mode](#) section. Thus, currents as small as  $0.91 \mu V_{RMS} / 50 \mu\Omega = 18$  mA can be resolved. The resolution can be further improved by averaging the conversion results over a longer period of time in the microcontroller that interfaces with the ADS131B23-Q1.

The –3-dB corner frequency of the differential antialiasing filter on the analog inputs (R13, R14, and C6) is set to  $1 / (2 \times \pi \times 2 \times 100 \Omega \times 47$  nF) = 16.9 kHz to provide more than 40-dB attenuation at the ADC1A modulator frequency. Keep the series resistor values (R13 and R14) small to avoid additional offset errors created by the voltage drop across the resistors because of the ADC1A input currents.

ADC1B is configured identical to ADC1A to allow for simultaneous sampling of the shunt voltage with the same digital filter response.

### 10.2.2.2 Battery Pack Voltage Measurement

The 800-V battery-pack voltage is divided down to the voltage range of ADC2A using a high-voltage resistor divider, consisting of R1, R2, R3, R4, and R5. Gain = 1 is used for ADC2A in this case to allow differential voltage measurements of  $V_{IN2A} = V_{V0A} - V_{AGNDA} = \pm 1.25$  V. The battery-pack voltage measurement is a unipolar, single-ended measurement with the negative multiplexer channel of ADC2A internally connected to AGNDA. Thus, only the voltage range from 0 V to 1.25 V of ADC2A is used. 式 23 calculates the resistor divider ratio.



$$V_{V0A} / V_{BAT\_MAX} = 1.25 \text{ V} / 800 \text{ V} = R_5 / (R_1 + R_2 + R_3 + R_4 + R_5) \quad (23)$$

The leakage current drawn by the resistor divider should be less than 100  $\mu\text{A}$  in this example to avoid unnecessarily draining the battery. The resistance of the divider must therefore be larger than  $R_{TOTAL} \geq V_{BAT\_MAX} / I_{LEAKAGE} = 800 \text{ V} / 100 \mu\text{A} = 8 \text{ M}\Omega$ . The resistor values are chosen as  $R_1 = R_2 = R_3 = R_4 = 2 \text{ M}\Omega$  and  $R_5 = 12 \text{ k}\Omega$ . Thus, the maximum voltage across  $R_5$  is 1.2 V at  $V_{BAT\_MAX} = 800 \text{ V}$ , leaving some headroom to the maximum input voltage of 1.25 V of ADC2A.

The maximum resistance of a single resistor that can be used in an automotive circuit design is often limited to a certain value. Also, the maximum voltage a single resistor can withstand is limited. These reasons are why the high-side resistor of the divider is split into multiple resistors ( $R_1, R_2, R_3,$  and  $R_4$ ). Another reason is that in case a single resistor has a short-circuit fault, the remaining resistors still limit the current into the ADC2A analog input pin, V0A, to safe levels.

### 10.2.2.3 Shunt Temperature Measurement

The shunt temperature in this example is measured using the TMP61-Q1, a linear 10-k $\Omega$  PTC, in a typical voltage divider configuration using the analog supply (AVDD) as excitation. The PTC resistance is calculated using 式 25, which is derived from 式 24:

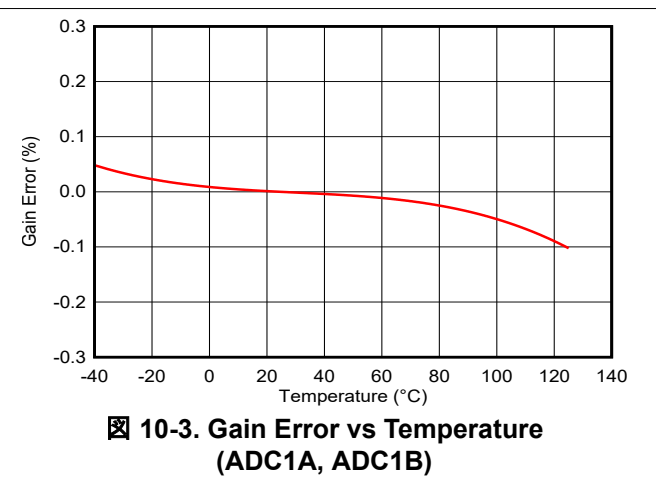
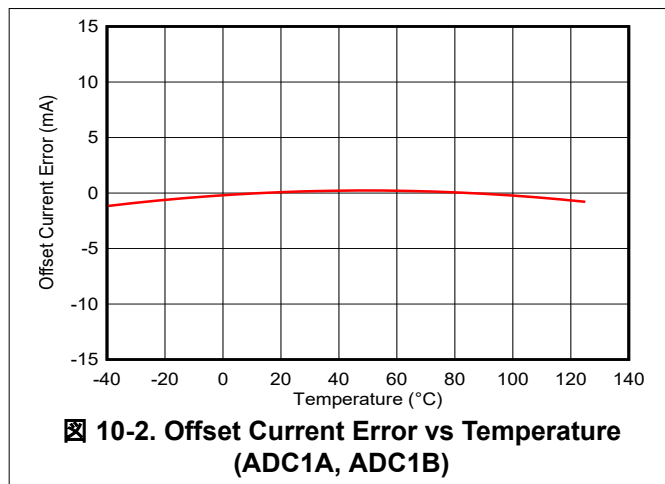
$$V_{PTC} = V_{V1A} - V_{AGNDA} = AVDD \times R_{PTC} / (R_6 + R_{PTC}) \quad (24)$$

$$R_{PTC} = R_6 \times V_{PTC} / (AVDD - V_{PTC}) \quad (25)$$

The maximum input voltage on V1A is limited to 1.25 V when using gain = 1 for ADC2A with the negative multiplexer channel of ADC2A internally connected to AGNDA. Therefore, the value of the precision resistor,  $R_6$ , must be chosen so that the voltage on V1A stays below 1.25 V for the value range of the PTC across the temperature range to be measured. The TMP61-Q1 has the largest resistance at the most positive temperature, approximately 18 k $\Omega$  at +125°C. Following 式 25, that means  $R_6 \geq 29.5 \text{ k}\Omega$ . A value of 34 k $\Omega$  is chosen for  $R_6$  to allow variation in the AVDD supply voltage up to 3.6 V without exceeding the maximum V1A voltage of 1.25 V.

### 10.2.3 Application Curves

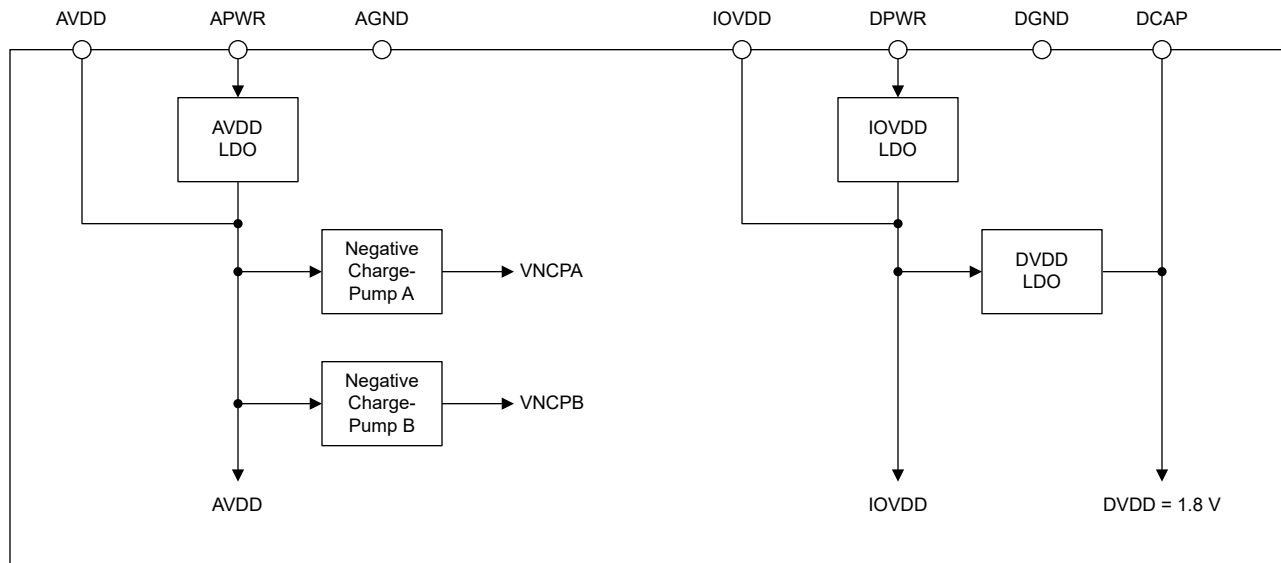
Figure 10-2 depicts the measurement accuracy of the current measurement (ADC1A, ADC1B) over temperature for a 0-A current through the shunt. Figure 10-3 illustrates the gain error of the current measurement (ADC1A, ADC1B) over temperature excluding the error of the shunt. The offset and gain error are calibrated at 25°C.



## 10.3 Power Supply Recommendations

### 10.3.1 Power-Supply Options

The ADS131B23-Q1 power-supply architecture shown in Figure 10-4 allows multiple ways to power the device to support different application requirements.



**10-4. Power-Supply Architecture**

The AVDD LDO accepts unregulated voltages between 4 V and 16 V on the APWR pin and outputs a regulated 3.3-V AVDD supply that is available at the AVDD pin to power external circuitry. The AVDD supply powers all analog circuitry in the device. If a regulated 3.3-V supply is available in the application, the AVDD LDO can be bypassed by shorting the APWR and AVDD pins.

The negative charge pumps in section A and section B provide a negative supply voltage for the various gain stages of every ADC to allow input voltage measurements below GND.

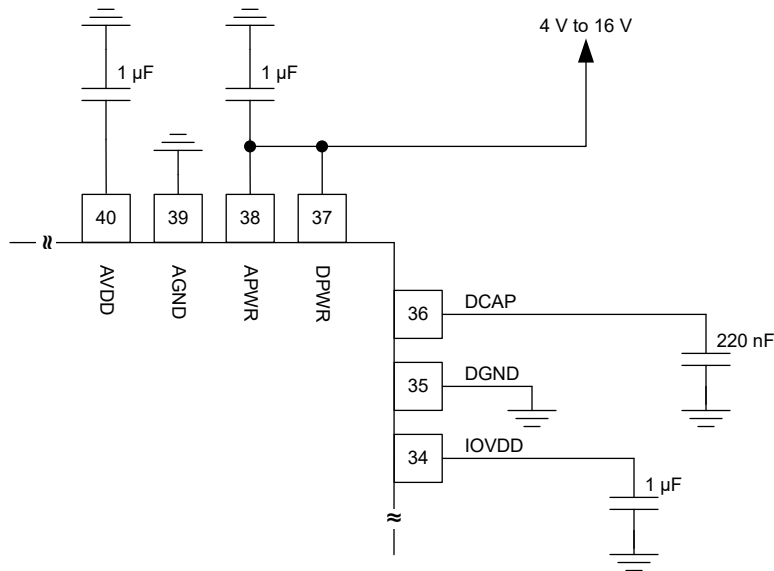
The IOVDD LDO accepts unregulated voltages between 4 V and 16 V on the DPWR pin and outputs a regulated 3.3-V IOVDD supply that is available at the IOVDD pin to power external circuitry. The IOVDD supply sets the voltage for the digital I/Os of the device. If a regulated 3.3-V or 5-V supply is available in the application, the IOVDD LDO can be bypassed by shorting the DPWR and IOVDD pins.

The DVDD LDO creates the 1.8-V supply for the digital core of the device.

The following sections show the three most commonly used external power-supply options, however other combinations are possible as well.

### 10.3.1.1 Single Unregulated External 4-V to 16-V Supply (3.3-V Digital I/O Levels)

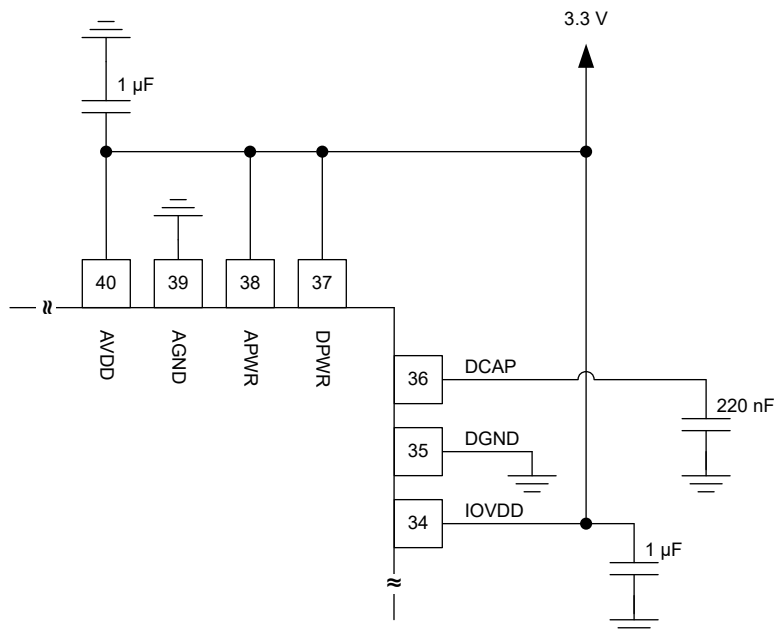
A single unregulated 4-V to 16-V supply (as shown in [Figure 10-5](#)) connected to both the APWR and DPWR pins can be used to power the device. No external supply is provided at the AVDD and IOVDD pins in this case. The AVDD LDO creates the internal 3.3-V AVDD supply, and the IOVDD LDO creates the 3.3-V I/O supply.



**Figure 10-5. Single Unregulated External 4-V to 16-V Supply**

### 10.3.1.2 Single Regulated External 3.3-V Supply (3.3-V Digital IO Levels)

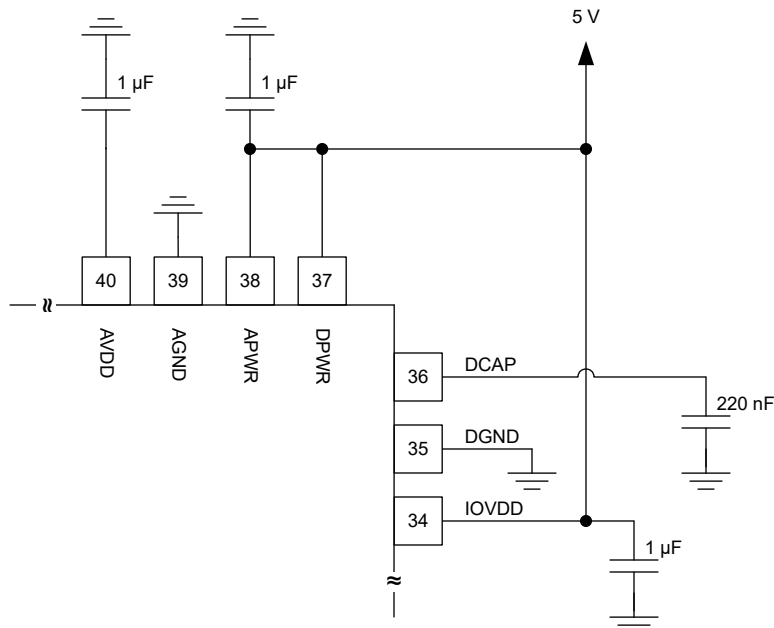
A single regulated 3.3-V supply connected to both the APWR and DPWR pins (as shown in [Figure 10-6](#)) can be used to power the device. In this case the APWR and AVDD pins must be shorted externally, as well as the DPWR and IOVDD pins. That way the AVDD and IOVDD LDOs are bypassed. The external 3.3-V supply is directly used as the AVDD and IOVDD supplies.



**Figure 10-6. Single Regulated External 3.3-V Supply**

### 10.3.1.3 Single Regulated External 5-V Supply (5-V Digital I/O Levels)

To allow operation of the digital I/Os with 5-V levels, a single regulated 5-V supply (shown in [Figure 10-7](#)) connected to both the APWR and DPWR pins can be used to power the device. No external supply is provided at the AVDD pin in this case. The AVDD LDO creates the internal 3.3-V AVDD supply. The DPWR and IOVDD pins must be shorted externally. That way the IOVDD LDO is bypassed. The external 5-V supply is directly used as the IOVDD supply.



**Figure 10-7. Single Regulated External 5-V Supply**

### 10.3.2 Power-Supply Sequencing

The power supplies can be sequenced in any order but the analog and digital inputs must never exceed the respective analog or digital power-supply voltage limits.

### 10.3.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance.

- APWR and AVDD must each be decoupled with a 1- $\mu$ F capacitor to AGND.  
 If APWR and AVDD are shorted together, a single 1- $\mu$ F decoupling capacitor placed close to the AVDD pin is sufficient.
- DPWR and IOVDD must each be decoupled with a 1- $\mu$ F capacitor to DGND.  
 If DPWR and IOVDD are shorted together, a single 1- $\mu$ F decoupling capacitor placed close to the IOVDD pin is sufficient.
- If APWR and DPWR are shorted together, a single 1- $\mu$ F decoupling capacitor for the two supplies is sufficient.
- The DVDD LDO output at the DCAP pin must be decoupled with a 220-nF capacitor to DGND.

Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

## 10.4 Layout

### 10.4.1 Layout Guidelines



For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the device. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

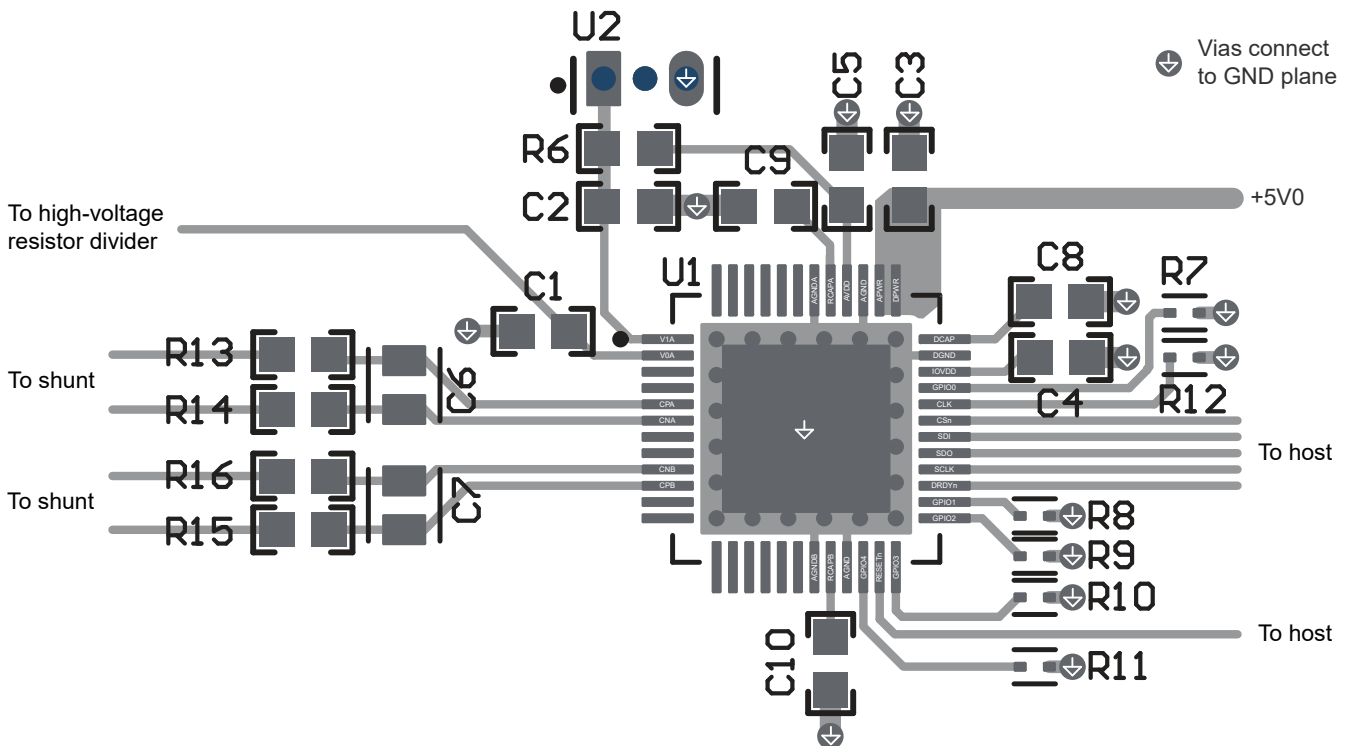
Route digital traces away from all analog inputs and associated components in order to minimize interference.

Use C0G capacitors on the analog inputs. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

### 10.4.2 Layout Example

 10-8 shows an example layout for the ADS131B23-Q1, referencing the components of the circuit in  10-1. In general, analog signals are partitioned to the left and digital signals to the right.



 10-8. Layout Example

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TMP61-Q1 Automotive Grade, ±1% 10-kΩ Linear Thermistor data sheet](#)

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
すべての商標は、それぞれの所有者に帰属します。

### 11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS131B23QPHPRQ1	ACTIVE	HTQFP	PHP	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	131B23Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ADS131B23-Q1 :**

- Catalog : [ADS131B23](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



## GENERIC PACKAGE VIEW

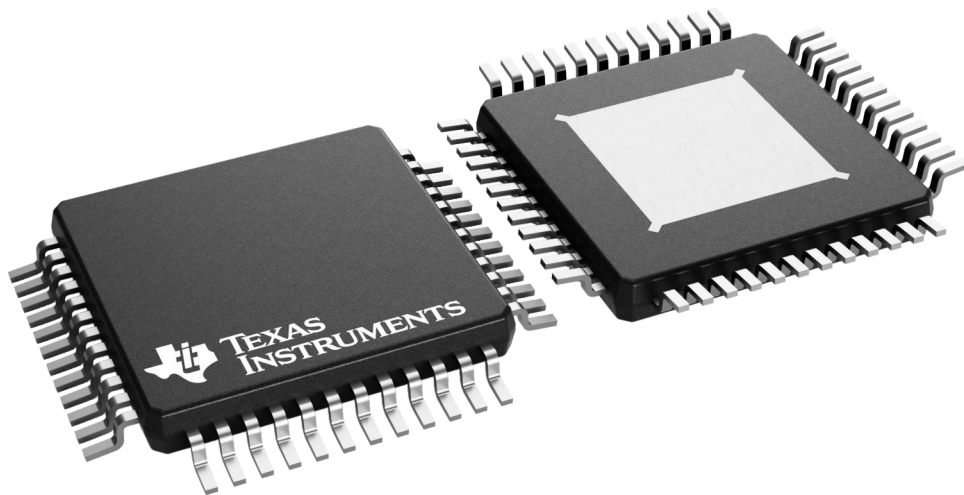
**PHP 48**

**TQFP - 1.2 mm max height**

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



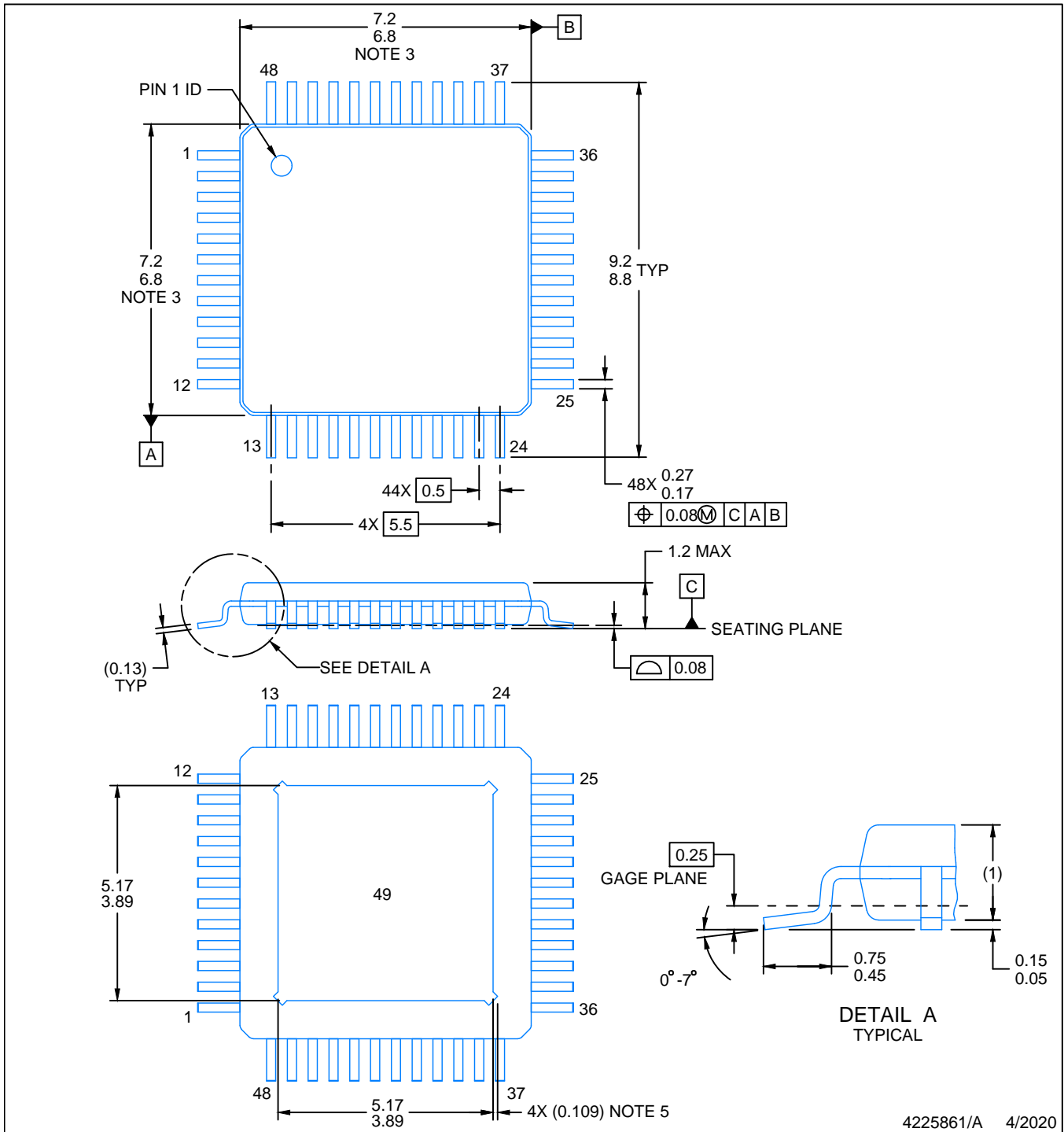
4226443/A

# PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4225861/A 4/2020

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

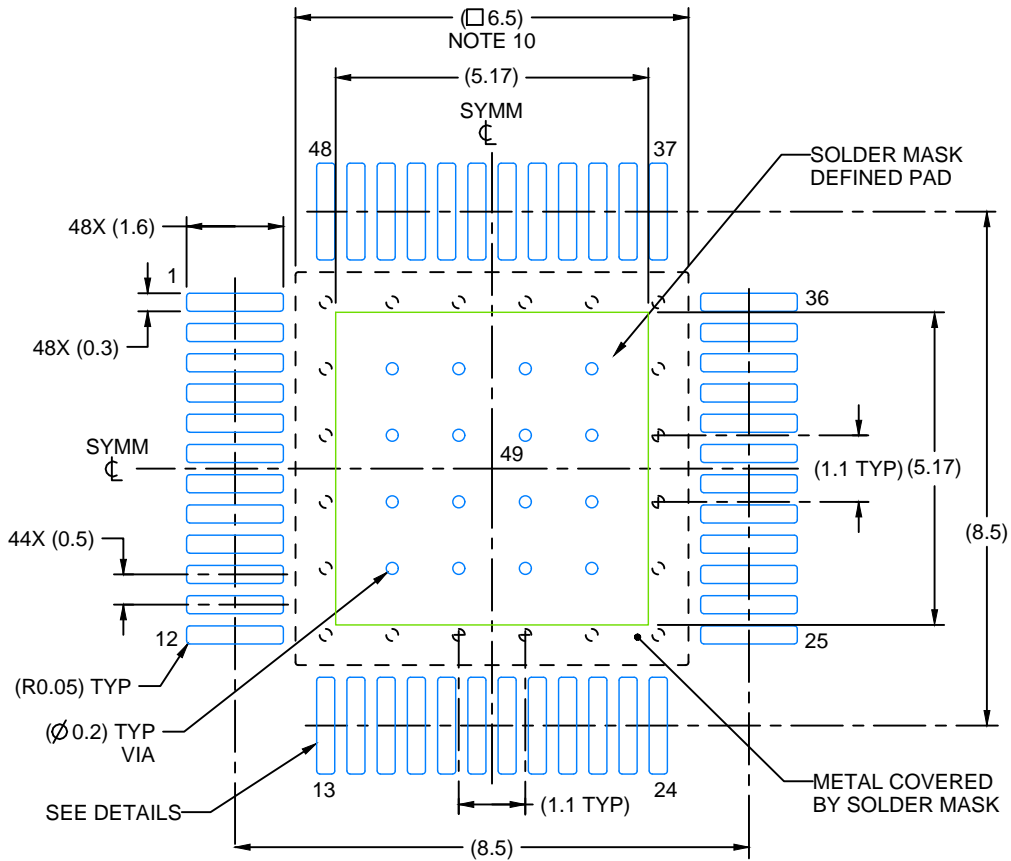
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

# EXAMPLE BOARD LAYOUT

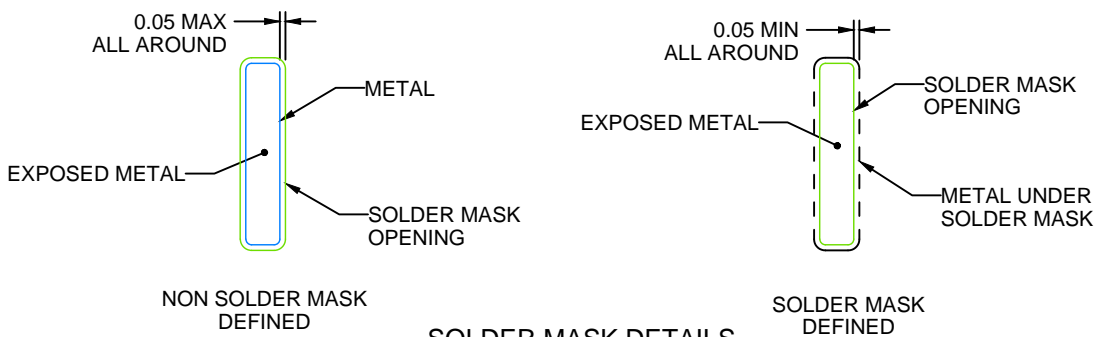
PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4225861/A 4/2020

NOTES: (continued)

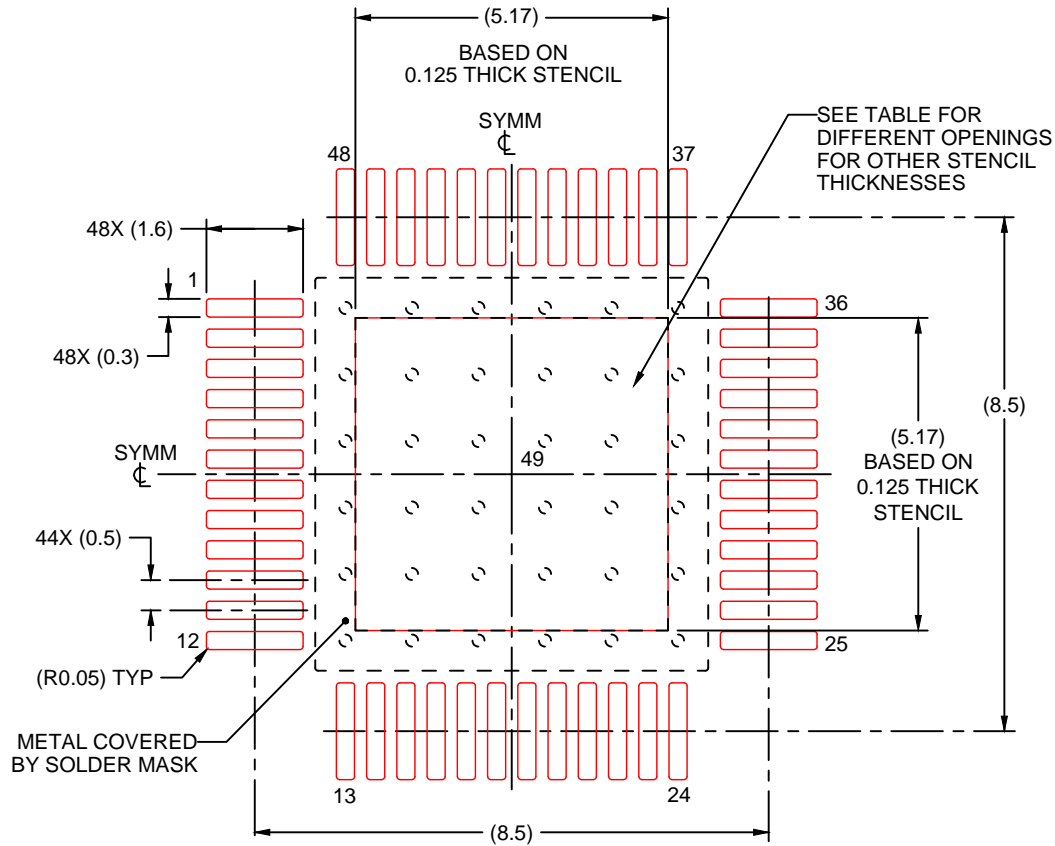
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](https://www.ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated