ADS42B49 Dual-Channel, 14-Bit, 250-MSPS Ultralow-Power ADC with Analog Input Buffer

1 Features

- Maximum Sample Rate: 250 MSPS
- Ultralow Power:
  - 850-mW Total Power at 250 MSPS
- Integrated Analog Input Buffer:
  - Input Capacitance: 2.2 pF at 170 MHz
  - Input Resistance: 1.1 kΩ at 170 MHz
- High Dynamic Performance:
  - 85-dBc SFDR at 170 MHz
  - 70.7-dBFS SNR at 170 MHz
- Crosstalk: > 85 dB at 185 MHz
- Programmable Gain Up to 6 dB for SNR and SFDR Trade-off
- DC Offset Correction
- Output Interface Options:
  - 1.8-V Parallel CMOS Interface
  - Double Data Rate (DDR) LVDS with Programmable Swing:
    - Standard Swing: 350 mV
    - Low Swing: 200 mV
- Supports Low Input Clock Amplitude Down to 200 mV_{PP}
- Package: 9.00 mm × 9.00 mm, 64-Pin Quad Flat No-Lead (VQFN) Package

2 Applications

- Wireless Communications Infrastructure
- Software-Defined Radio
- Power Amplifier Linearization

3 Description

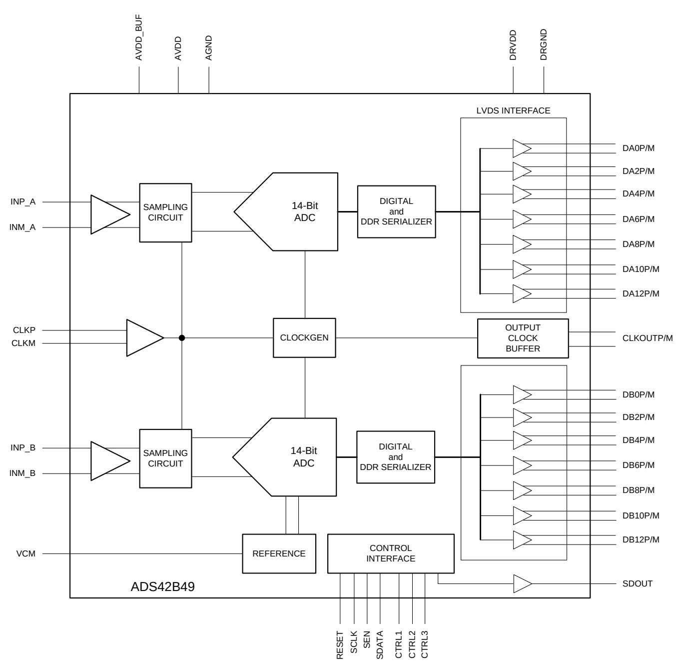
The ADS42B49 is an ultralow-power dual-channel, 14-bit analog-to-digital converter (ADC) featuring integrated analog input buffers. It uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power. The presence of analog input buffers makes this device easy to drive and helps achieve high performance over a wide frequency range. The ADS42B49 is well-suited for multi-carrier, wide bandwidth communications applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS42B49	VQFN(64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Revision A (December 2012) to Revision B — **Page**

- Changed footnote for CMOS Timings at Lower Sampling Frequencies 14
- Changed first two sentences in Description of High-Performance Modes table 27
- Changed D2 and D1 bit names in address 03h of Table 10 36
- Changed Register Address 03h 38

Changes from Original (December 2012) to Revision A — **Page**

- Changed product status from Product Preview to Production Data 1
- Changed Analog Inputs, V_{ID} parameter nominal specification in Recommended Operating Conditions table 9
- Changed Analog Inputs, *Maximum analog input frequency* parameter rows in Recommended Operating conditions table 9
- Changed footnote 1 in Recommended Operating Conditions table 9
- Changed *PSRR* parameter test conditions in Electrical Characteristics: ADS42B49 table 11
- Deleted DNL and INL rows from Electrical Characteristics: ADS42B49 table 11
- Changed Analog Inputs, V_{ID} parameter typical specification in Electrical Characteristics: General table 11
- Deleted Analog Inputs, *Analog input common-mode current* row from Electrical Characteristics: General table 11

- Changed DC Accuracy, *Offset error* parameter typical specification in Electrical Characteristics: General table 11
- Changed Power Supply, *IDRVDD* parameter CMOS interface row in Electrical Characteristics: General table................. 11
- Changed Power Supply, *Digital power, CMOS interface* parameter typical specification in Electrical Characteristics: General table 11
- Changed t_J parameter typical specification in Timing Requirements table 13
- Deleted Wakeup time maximum specifications in Timing Requirements table 13
- Changed footnote 1 in Timing Requirements table 13
- Changed ADC latency, default after reset typical specification in Timing Requirements table.......... 13
- Changed *ADC latency* parameter typical specification in Timing Requirements table 13
- Added t_{PDI} specifications to Timing Requirements table 13
- Updated Figure 40 22
- Updated Figure 41 23
- Filled in TBD in *Theory of Operation* section.......... 24
- Changed description of *Multiplexed Mode of Operation* section 32
- Changed first column of (5 / 8) AVDD row in Table 7 33
- Changed sixth row in Table 8 33
- Changed CTRL1, CTRL2, and CTRL3 control mode description in Table 9 34
- Changed third paragraph in the *Serial Register Readout* section 36
- Added *Analog Input* section.......... 49
- Changed description of *Driving Circuit* section.......... 49
- Added Figure 54 to *Drive Circuit Requirements* section 50

5 Description (continued)

The ADS42B49 has gain options that can be used to improve SFDR performance at lower full-scale input ranges. This device also includes a dc offset correction loop that can be used to cancel the ADC offset. Both DDR LVDS and parallel CMOS digital output interfaces are available in a compact VQFN-64 PowerPAD™ package.

The device includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The ADS42B49 is specified over the industrial temperature range (–40°C to 85°C).

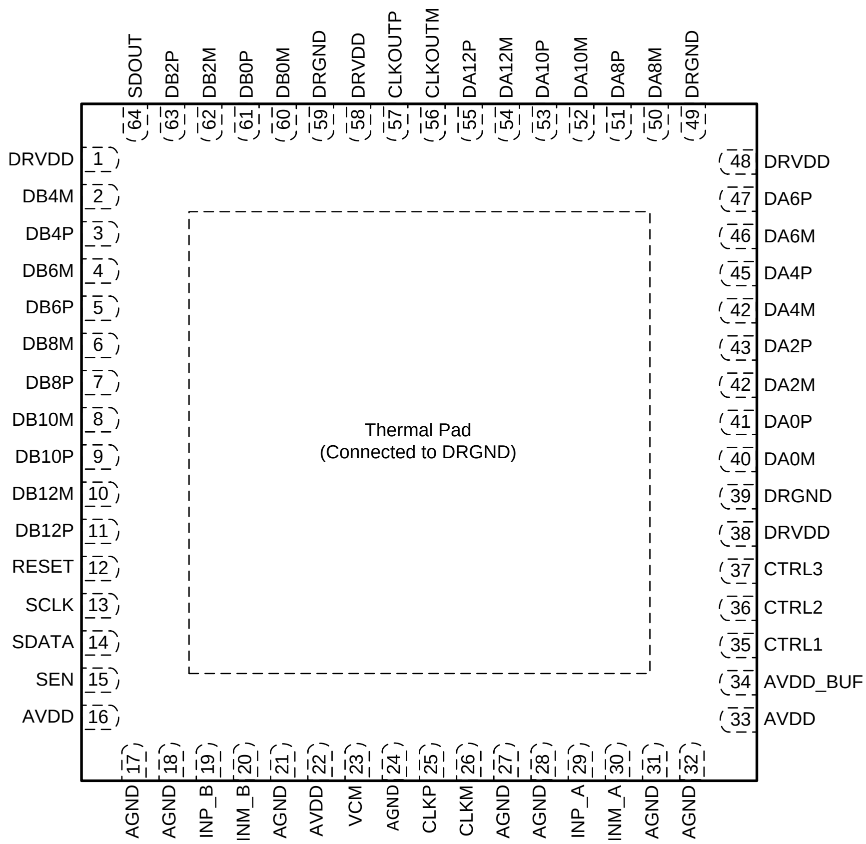
6 ADS424x and ADS422x Family Comparison(1)

	65 MSPS	125 MSPS	160 MSPS	250 MSPS
ADS422x 12-bit family	ADS4222	ADS4225	ADS4226	ADS4229
ADS424x 14-bit family	ADS4242	ADS4245	ADS4246	ADS4249, ADS42B49 (with analog input buffers)

(1) See *Migrating from the ADS62P49 and ADS4249* for details on migrating from the ADS62P49 family.

7 Pin Configuration and Functions

RGC Package[1]
64-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



(1) The thermal pad is connected to DRGND.

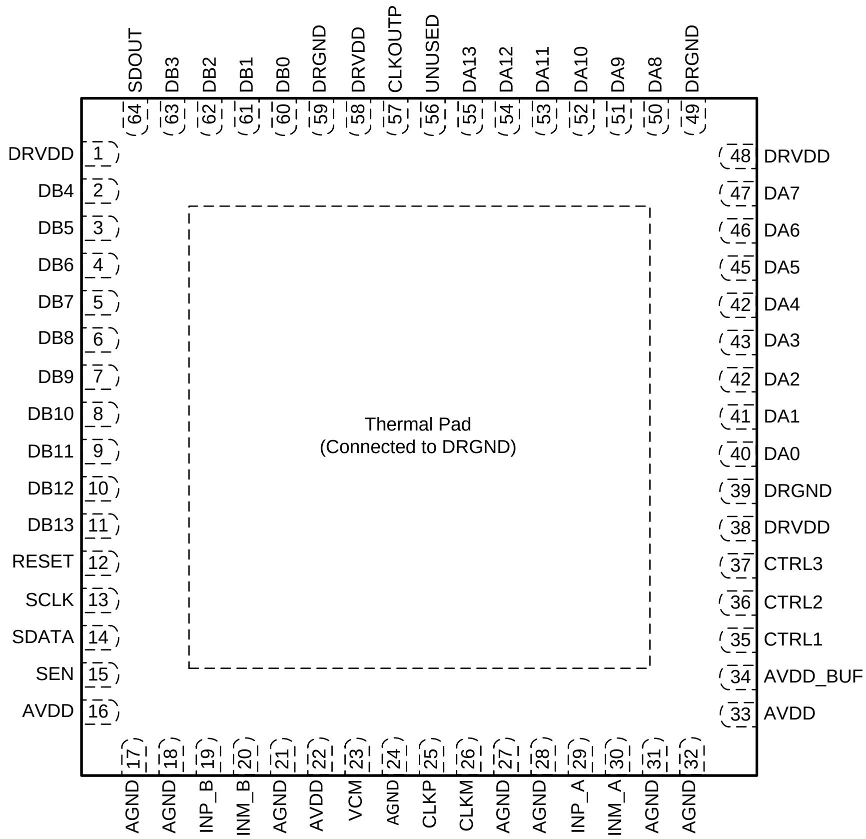
Pin Functions - LVDS Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	17, 18, 21, 24, 27, 28, 31, 32	Input	Analog ground
AVDD	16, 22, 33	Input	Analog power supply
AVDD_BUF	34	Input	Analog buffer supply
CLKM	26	Input	Differential clock negative input
CLKP	25	Input	Differential clock positive input
CLKOUTM	56	Output	Differential output clock, complement
CLKOUTP	57	Output	Differential output clock, true
CTRL1	35	Input	Digital control input pins. Together, these pins control the various power-down modes.
CTRL2	36	Input	Digital control input pins. Together, these pins control the various power-down modes.
CTRL3	37	Input	Digital control input pins. Together, these pins control the various power-down modes.
DA0P, DA0M	41, 40	Output	Channel A differential output data pair, D0 and D1 multiplexed
DA2P, DA2M	43, 42	Output	Channel A differential output data D2 and D3 multiplexed
DA4P, DA4M	45, 44	Output	Channel A differential output data D4 and D5 multiplexed
DA6P, DA6M	47, 46	Output	Channel A differential output data D6 and D7 multiplexed
DA8P, DA8M	51, 50	Output	Channel A differential output data D8 and D9 multiplexed

Pin Functions - LVDS Mode (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA10P, DA10M	53, 52	Output	Channel A differential output data D10 and D11 multiplexed
DA12P, DA12M	55, 54	Output	Channel A differential output data D12 and D13 multiplexed
DB0P, DB0M	61, 60	Output	Channel B differential output data pair, D0 and D1 multiplexed
DB2P, DB2M	63, 62	Output	Channel B differential output data D2 and D3 multiplexed
DB4P, DB4M	3, 2	Output	Channel B differential output data D4 and D5 multiplexed
DB6P, DB6M	5, 4	Output	Channel B differential output data D6 and D7 multiplexed
DB8P, DB8M	7, 6	Output	Channel B differential output data D8 and D9 multiplexed
DB10P, DB10M	9, 8	Output	Channel B differential output data D10 and D11 multiplexed
DB12P, DB12M	11, 10	Output	Channel B differential output data D12 and D13 multiplexed
DRGND	39, 49, 59, PAD	Input	Output buffer ground, should be shorted on-board to analog ground.
DRVDD	1, 38, 48, 58	Input	Output buffer supply
INM_A	30	Input	Differential analog negative input, channel A
INP_A	29	Input	Differential analog positive input, channel A
INM_B	20	Input	Differential analog negative input, channel B
INP_B	19	Input	Differential analog positive input, channel B
RESET	12	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
SCLK	13	Input	This pin functions as a serial interface clock input when RESET is low. SCLK controls the low-speed mode selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
SDOUT	64	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
SEN	15	Input	This pin functions as a serial interface enable input when RESET is low. SEN controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.
VCM	23	Output	This pin outputs the common-mode voltage (1.9 V) that can be used externally to bias the analog input pins

RGC Package(2)
64-Pin VQFN With Exposed Thermal Pad
CMOS Mode - Top View



(1) The thermal pad is connected to DRGND.

Pin Functions - CMOS Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	17, 18, 21, 24, 27, 28, 31, 32	Input	Analog ground
AVDD	16, 22, 33	Input	Analog power supply
AVDD_BUF	34	Input	Analog buffer supply
CLKM	26	Input	Differential clock negative input
CLKP	25	Input	Differential clock positive input
CLKOUT	57	Output	CMOS output clock
CTRL1	35	Input	Digital control input pins. Together, these pins control various power-down modes.
CTRL2	36	Input	Digital control input pins. Together, these pins control various power-down modes.
CTRL3	37	Input	Digital control input pins. Together, these pins control various power-down modes.
DA0 to DA13	40, 41, 42, 43, 44, 45, 46, 47, 50, 51, 52, 53, 54 ,55	Output	Channel A ADC output data bits, CMOS levels
DB0 to DB13	60, 61, 62, 63, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	Output	Channel B ADC output data bits, CMOS levels
DRGND	39, 49, 59, PAD	Input	Output buffer ground, should be shorted on-board to analog ground.
DRVDD	1, 38, 48, 58	Input	Output buffer supply
INM_A	30	Input	Differential analog negative input, channel A
INP_A	29	Input	Differential analog positive input, channel A
INM_B	20	Input	Differential analog negative input, channel B

Pin Functions - CMOS Mode (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
INP_B	19	Input	Differential analog positive input, channel B
RESET	12	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
SCLK	13	Input	This pin functions as a serial interface clock input when RESET is low. SCLK controls the low-speed mode when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
SDOUT	64	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
SEN	15	Input	This pin functions as a serial interface enable input when RESET is low. SEN controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.
UNUSED	56	—	This pin is not used in the CMOS interface
VCM	23	Output	This pin outputs the common-mode voltage (1.9 V) that can be used externally to bias the analog input pins

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	2.1	V
	AVDD_BUF	–0.3	3.6	V
	DRVDD	–0.3	2.1	V
Voltage between:	AGND and DRGND	–0.3	0.3	V
	AVDD to DRVDD (when AVDD leads DRVDD)	–2.4	2.4	V
	DRVDD to AVDD (when DRVDD leads AVDD)	–2.4	2.4	V
	AVDD_BUF to DRVDD and AVDD	–3.9	3.9	V
Voltage applied to	INP, INM	–0.3	Minimum (3, AVDD_BUF + 0.3)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3	3.9	V
Temperature	Operating free-air, T_A	–40	85	°C
	Operating junction, T_J		125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range, unless otherwise noted.

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.8	1.9	2	V
AVDD_BUF	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	2	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range			2		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.05		V
	Maximum analog input frequency with 2-V_{PP} input amplitude[(1)]			400		MHz
	Maximum analog input frequency with 1.6-V_{PP} input amplitude[(1)]			500		MHz
CLOCK INPUT						
Input clock sample rate	Low-speed mode enabled[(2)]		1		80	MSPS
	Low-speed mode disabled[(2)] (by default after reset)		80		250	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
Input clock duty cycle	Low-speed mode disabled		45%	50%	55%	
	Low-speed mode enabled		40%	50%	60%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the *Analog Input* section in the *Application Information*.
(2) See the *Serial Interface Configuration* section for details on programming the low-speed mode.

8.4 Thermal Information

THERMAL METRIC[(1)]		ADS42B49 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics: ADS42B49 (250 MSPS)

Typical values are at 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				14	Bits
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		71.3		dBFS
		f_{IN} = 70 MHz		71.2		
		f_{IN} = 100 MHz		71.1		
		f_{IN} = 170 MHz, 0-dB gain	68	70.7		
		f_{IN} = 170 MHz, 3-dB gain		67.8		
		f_{IN} = 300 MHz		69.5		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		71		dBFS
		f_{IN} = 70 MHz		71		
		f_{IN} = 100 MHz		70.9		
		f_{IN} = 170 MHz, 0-dB gain	67	70.4		
		f_{IN} = 170 MHz, 3-dB gain		67.7		
		f_{IN} = 300 MHz		67.7		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		87		
		f_{IN} = 100 MHz		86		
		f_{IN} = 170 MHz, 0-dB gain	73	85		
		f_{IN} = 170 MHz, 3-dB gain		89		
		f_{IN} = 300 MHz		73		
THD	Total harmonic distortion	f_{IN} = 10 MHz		82		dBc
		f_{IN} = 70 MHz		84		
		f_{IN} = 100 MHz		85		
		f_{IN} = 170 MHz, 0-dB gain	70	83		
		f_{IN} = 170 MHz, 3-dB gain		86		
		f_{IN} = 300 MHz		72		
HD2	Second-harmonic distortion	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 70 MHz		93		
		f_{IN} = 100 MHz		98		
		f_{IN} = 170 MHz, 0-dB gain	73	89		
		f_{IN} = 170 MHz, 3-dB gain		94		
		f_{IN} = 300 MHz		80		
HD3	Third-harmonic distortion	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		87		
		f_{IN} = 100 MHz		86		
		f_{IN} = 170 MHz, 0-dB gain	73	85		
		f_{IN} = 170 MHz, 3-dB gain		89		
		f_{IN} = 300 MHz		73		
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		100		dBc
		f_{IN} = 70 MHz		100		
		f_{IN} = 100 MHz		100		
		f_{IN} = 170 MHz, 0-dB gain	84	95		
		f_{IN} = 170 MHz, 3-dB gain		97		
		f_{IN} = 300 MHz		94		
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		88		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		83		

Electrical Characteristics: ADS42B49 (250 MSPS) (continued)

Typical values are at 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crosstalk	10-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel		> 85		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply		30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.4		LSBs

8.6 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER			MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range			2		V_{PP}
	Differential input resistance (at 170 MHz)			1.2		kΩ
	Differential input capacitance (at 170 MHz)			2.2		pF
	Analog input bandwidth (with 50-Ω source impedance, and 50-Ω termination)			700		MHz
VCM	Common-mode output voltage			1.9(1)		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20	3	20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.005		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			186	225	mA
IAVDD_BUF	Analog buffer supply current			67	90	mA
IDRVDD	Output buffer supply current	LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz		151	180	mA
		CMOS interface, 8-pF external load capacitance, f_{IN} = 2.5 MHz(2)		128		mA
	Analog power			353		mW
	Analog buffer power			224		mW
	Digital power, LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			272		mW
	Digital power, CMOS interface, 8-pF external load capacitance,(2) f_{IN} = 2.5 MHz			230		mW
	Total power, LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			850	925	mW
	Global power-down				20	mW

(1) After the HIGH PERF MODE[10:0] bits are set.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

8.7 Digital Characteristics

At AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level 0 or 1.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)(1)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	SDATA, SCLK(2)	V_{HIGH} = 1.8 V		10		µA
		SEN(3)	V_{HIGH} = 1.8 V		0		
I_{IL}	Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		
DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)							
V_{OH}	High-level output voltage			DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
C_O	Output capacitance (internal to device)						pF
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	275	350	425	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–425	–350	–275	mV
V_{OCM}	Output common-mode voltage			0.9	1.05	1.25	V

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA and SCLK have an internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

8.8 Timing Requirements: LVDS and CMOS Modes

Typical values are at 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.7 V to 2 V.

			MIN	NOM	MAX	UNIT
t_A	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
t_J	Aperture jitter			120		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50		µs
		Time to valid data after coming out of GLOBAL power-down mode		100		µs
	ADC latency(1)	Default latency after reset		11		Clock cycles
		Digital functions enabled (EN DIGITAL = 1)		19		Clock cycles
DDR LVDS MODE(2)(3)						
t_{SU_RISE}	Data setup time on rising edge of CLKOUTP	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(4)	0.32	0.68		ns
t_{HO_RISE}	Data hold time on rising edge of CLKOUTP	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(4)	0.5	0.82		ns
t_{SU_FALL}	Data setup time on falling edge of CLKOUTP	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(4)	0.63	1.04		ns
t_{HO_FALL}	Data hold time on falling edge of CLKOUTP	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(4)	0.18	0.58		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock (CLKOUTP – CLKOUTM) rising edge cross-over	7.6	8.9	10.2	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock (CLKOUTP – CLKOUTM)		57%		
t_{FALL}, t_{RISE}	Data fall time, Data rise time	Rise time measured from –100 mV to 100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to 100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD 1 MSPS ≤ Sampling frequency ≤ 250 MSPS		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD 1 MSPS ≤ Sampling frequency ≤ 250 MSPS		0.13		ns
PARALLEL CMOS MODE						
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	5.9	8.3	10.6	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		50%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns

(1) Overall latency = ADC latency + t_{PDI}. At 250 MSPS, t_{PDI} is greater than two clock periods. Therefore, overall latency at 250 MSPS = ADC latency + 2 clock cycles.
(2) Setup and hold values in DDR LVDS mode are taken with a delayed output clock by writing register 42h, value 30h.
(3) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(4) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.

8.9 Serial Interface Timing Characteristics

Typical values at 25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted.

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

8.10 Reset Timing (Only When Serial Interface is Used)

Typical values at 25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

			MIN	NOM	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

8.11 LVDS Timings at Lower Sampling Frequencies(1)

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)						HOLD TIME (ns)						CLOCK PROPAGATION DELAY (ns)		
	t_{SU_RISE}			t_{SU_FALL}			t_{HO_RISE}			t_{HO_FALL}			t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
100	0.36	0.72		0.67	1.10		3.37	3.80		3.02	3.48		10.4	11.8	13.1
125	0.35	0.72		0.66	1.08		2.43	2.82		2.09	2.51		9.4	10.8	12.1
150	0.35	0.70		0.66	1.07		1.77	2.15		1.47	1.86		8.8	10.1	11.5
175	0.35	0.70		0.63	1.07		1.32	1.67		1.00	1.40		8.3	9.7	11.0
200	0.38	0.70		0.68	1.08		0.93	1.29		0.66	1.04		8.0	9.4	10.8
230	0.33	0.69		0.67	1.06		0.63	0.97		0.35	0.74		7.7	9.1	10.5

(1) Setup and hold values in DDR LVDS mode belong to delayed output clock by writing register 42h, value 30h.

8.12 CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME(1) (t_{SU}, ns)			HOLD TIME(1) (t_{HO}, ns)			CLOCK PROPAGATION DELAY (t_{PDI}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
100	3.91	4.40		3.68	4.18		9.5	11.5	13.3
125	2.81	3.40		2.73	3.14		8.5	10.5	12.3
150	2.00	2.64		2.09	2.52		7.9	9.9	11.7
175	1.43	2.14		1.67	2.06		7.6	9.4	11.4
200	1.01	1.76		1.25	1.68		6.4	8.9	11.1

(1) In CMOS mode, setup time is measured from the beginning of data valid to the mid-point of the CLKOUT rising edge, whereas hold time is measured from the mid-point of the CLKOUT rising edge to data becoming invalid.

8.13 Typical Characteristics

8.13.1 ADS42B49

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

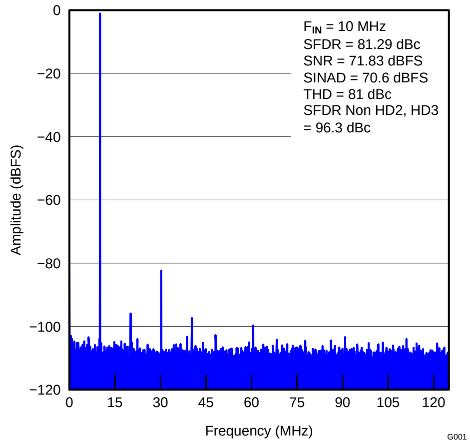


Figure 1. Input Signal (10 MHz)

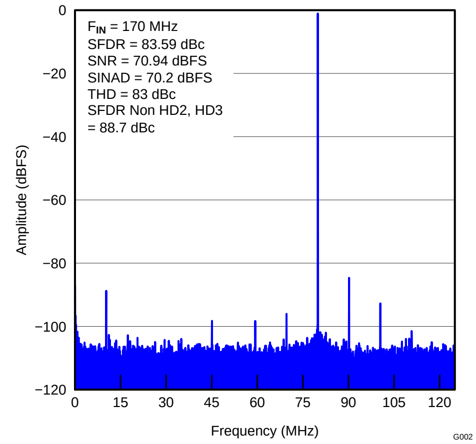


Figure 2. Input Signal (170 MHz)

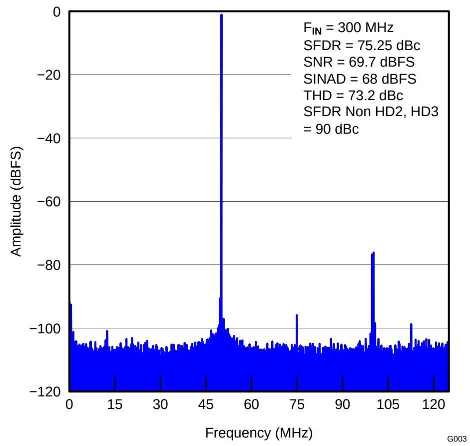


Figure 3. Input Signal (300 MHz)

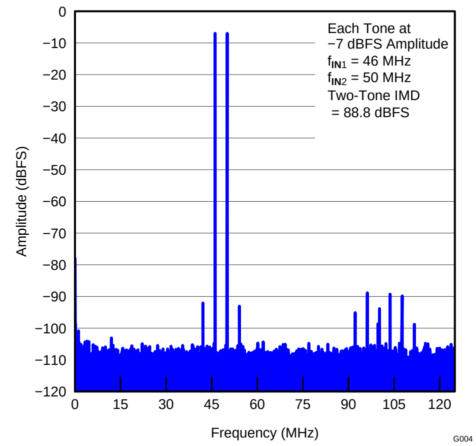


Figure 4. Two-Tone Input Signal

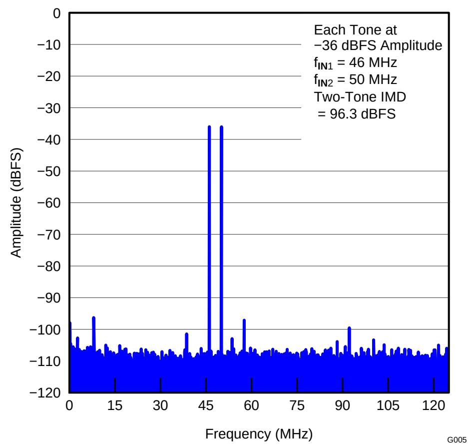


Figure 5. Two-Tone Input Signal

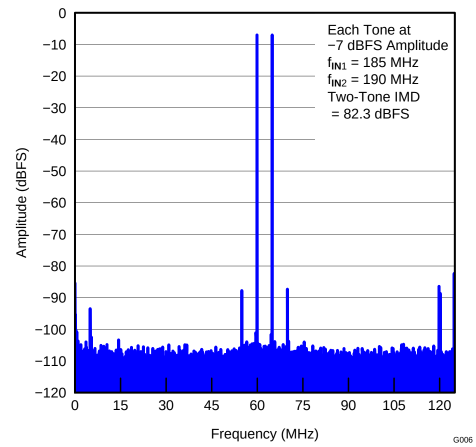


Figure 6. Two-Tone Input Signal

ADS42B49 (continued)

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

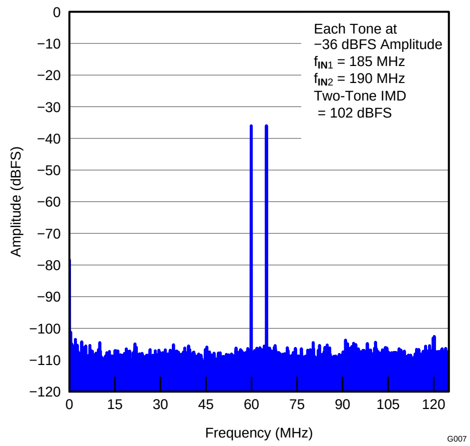


Figure 7. Two-Tone Input Signal

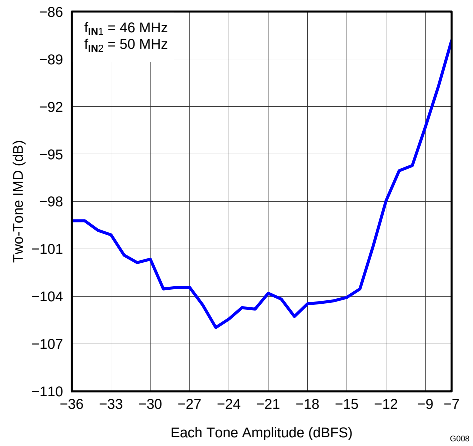


Figure 8. Two-Tone IMD3 vs Input Amplitude

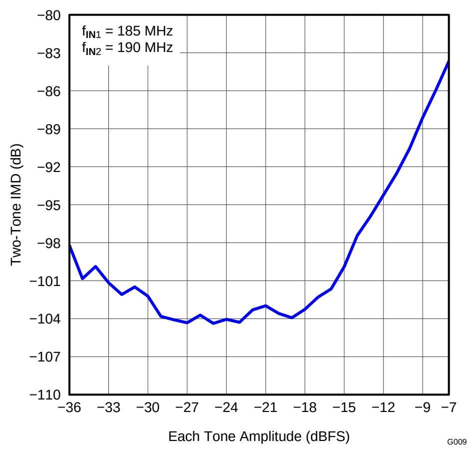


Figure 9. Two-Tone IMD3 vs Input Amplitude

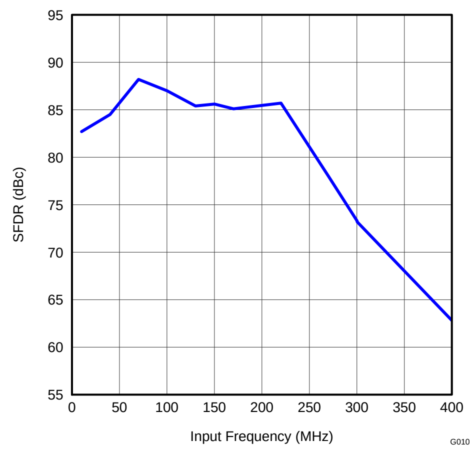


Figure 10. Spurious-Free Dynamic Range vs Input Frequency

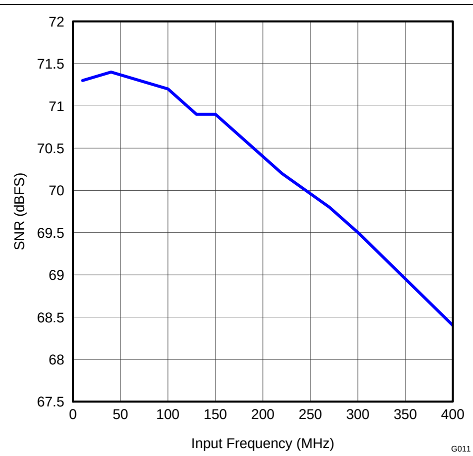


Figure 11. Signal-to-Noise Ratio vs Input Frequency

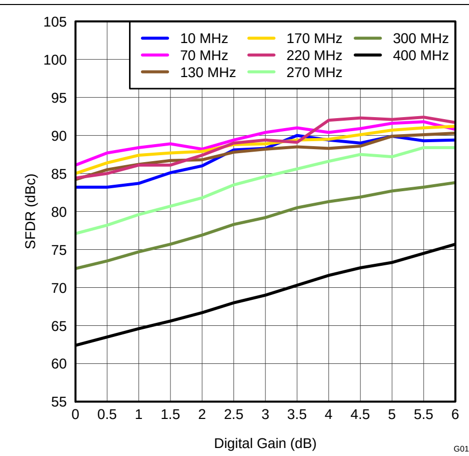


Figure 12. Spurious-Free Dynamic Range vs Gain and Input Frequency

ADS42B49 (continued)

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

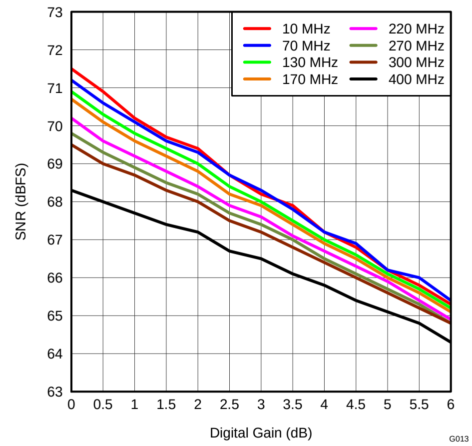


Figure 13. Signal-to-Noise Ratio vs Gain and Input Frequency

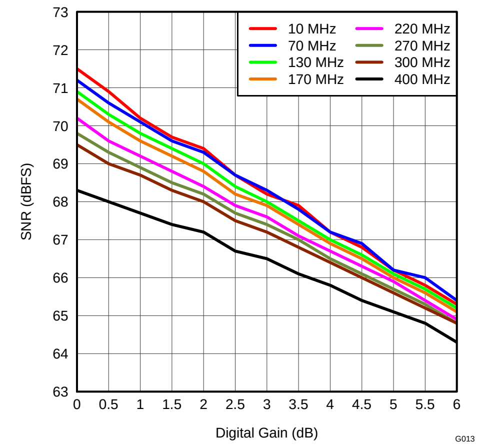


Figure 14. Performance vs Input Amplitude

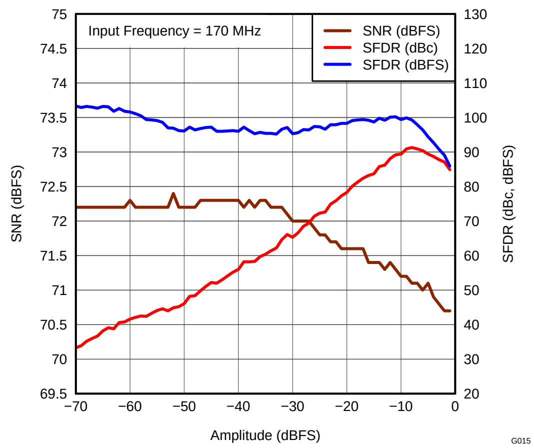


Figure 15. Performance vs Input Amplitude

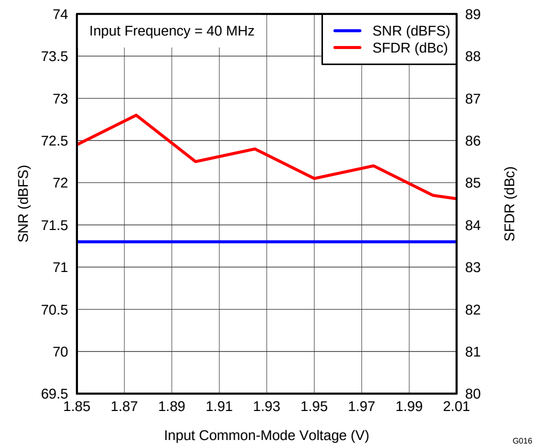


Figure 16. Performance vs Input Common-Mode Voltage

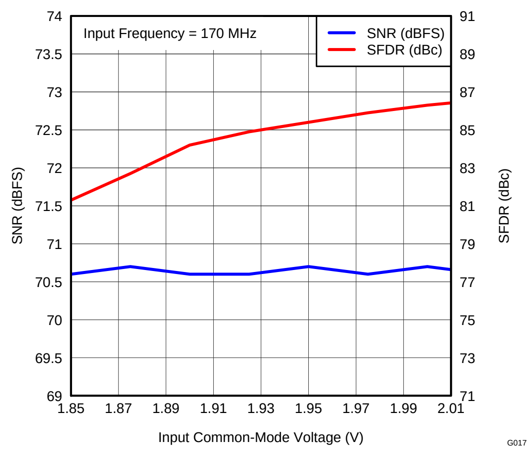


Figure 17. Performance vs Input Common-Mode Voltage

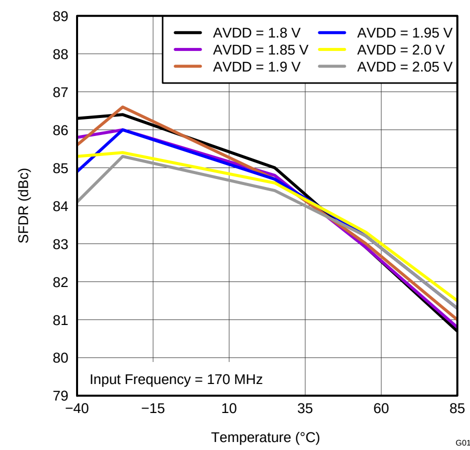


Figure 18. Spurious-Free Dynamic Range vs Temperature and AVDD Supply

ADS42B49 (continued)

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

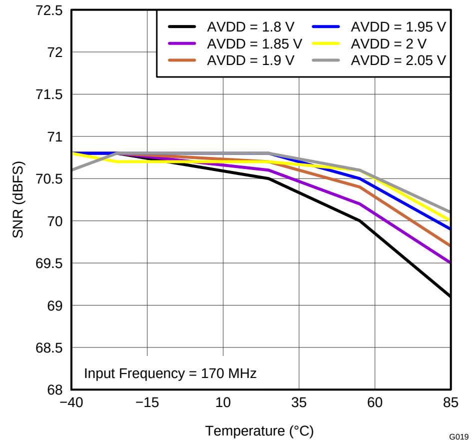


Figure 19. Signal-to-Noise Ratio vs Temperature and AVDD Supply

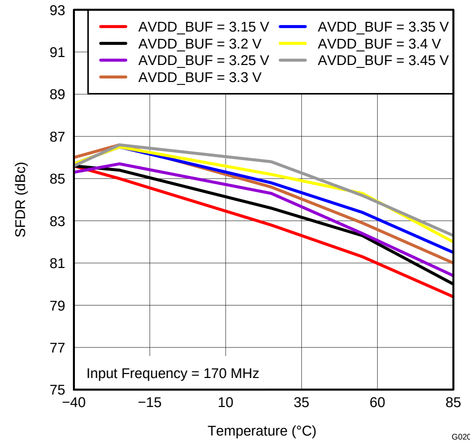


Figure 20. Spurious-Free Dynamic Range vs Temperature and AVDD_BUF Supply

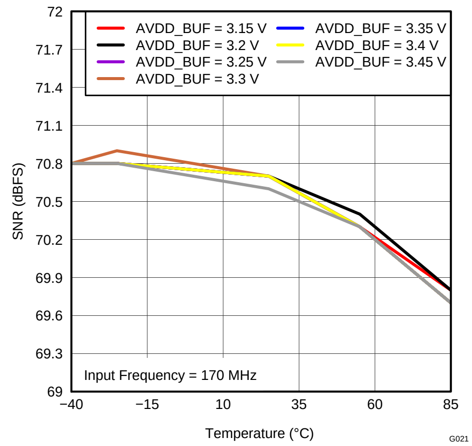


Figure 21. Signal-to-Noise Ratio vs Temperature and AVDD_BUF Supply

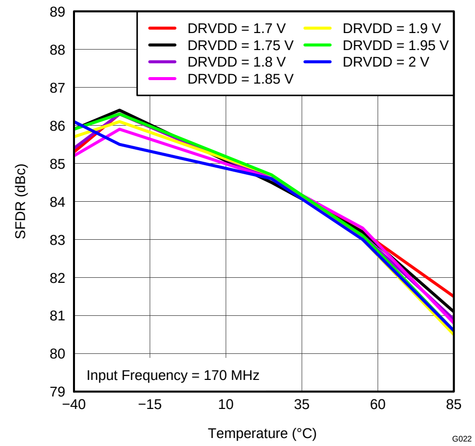


Figure 22. Spurious-Free Dynamic Range vs Temperature and DRVDD Supply Voltage

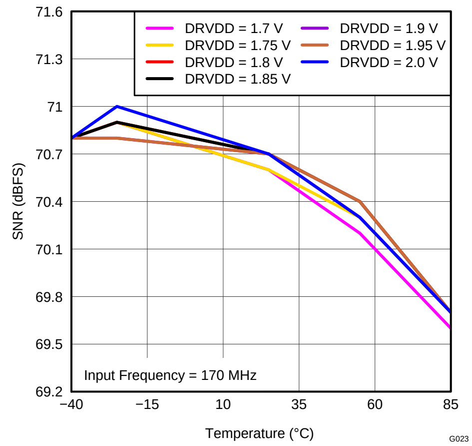


Figure 23. Signal-to-Noise Ratio vs Temperature and DRVDD Supply Voltage

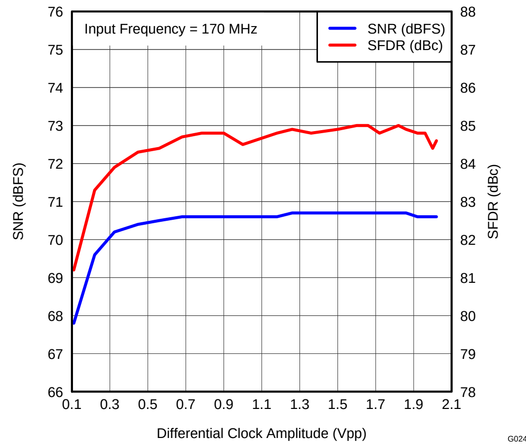


Figure 24. Performance vs Input Clock Amplitude

ADS42B49 (continued)

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

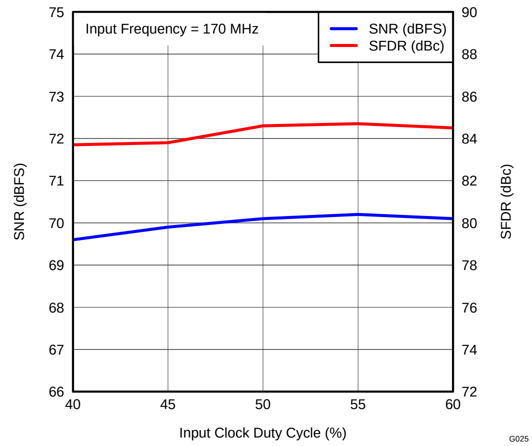


Figure 25. Performance vs Input Clock Duty Cycle

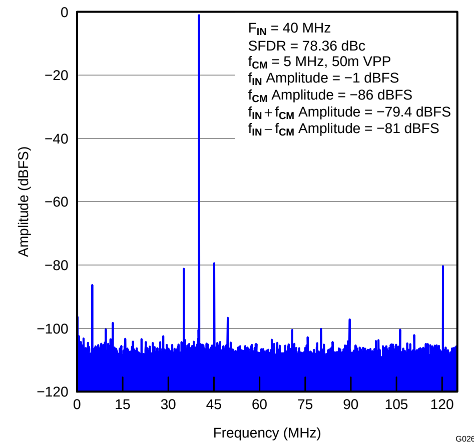


Figure 26. Common-Mode Rejection Ratio Plot

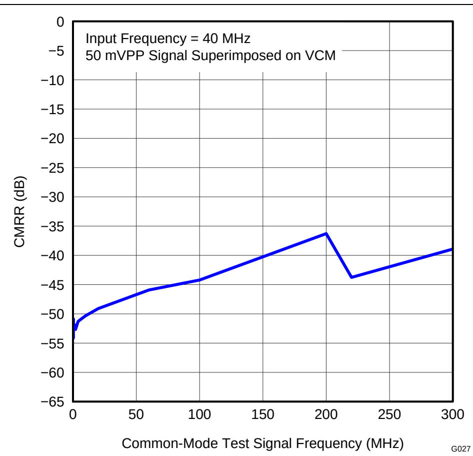


Figure 27. Common-Mode Rejection Ratio vs Test Signal Frequency

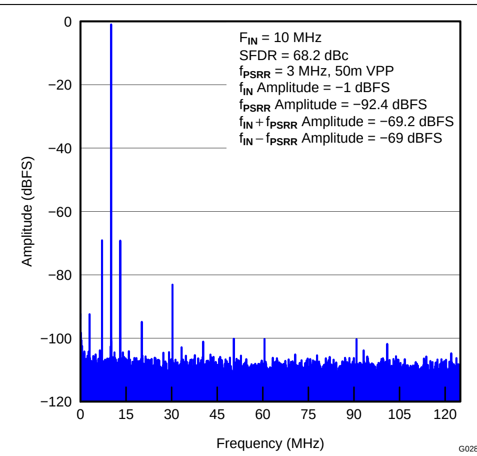


Figure 28. Power-Supply Rejection Ratio Plot

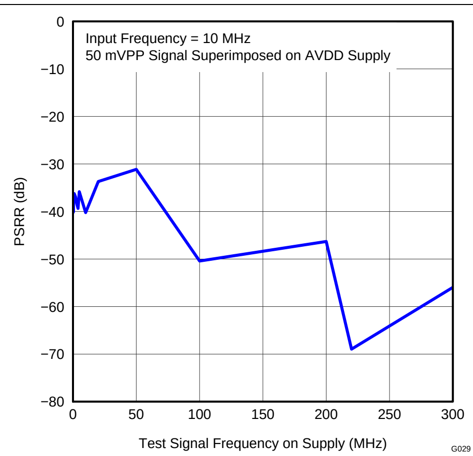


Figure 29. Power-Supply Rejection Ratio vs Test Signal Frequency

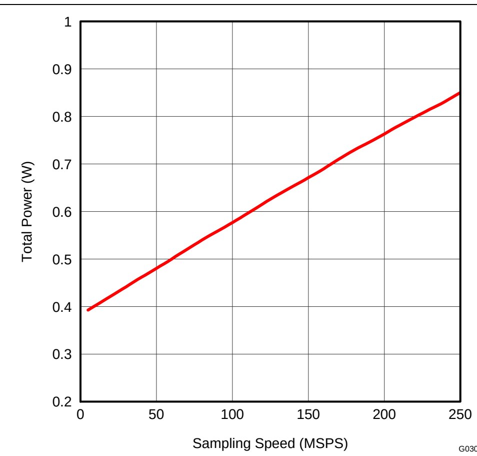


Figure 30. Total Power vs Sampling Frequency

ADS42B49 (continued)

At T_A = 25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

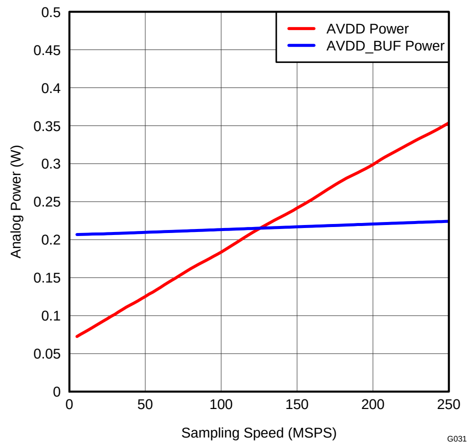


Figure 31. Analog Power vs Sampling Frequency

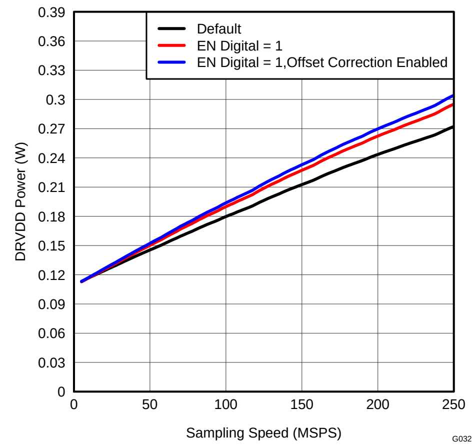


Figure 32. Digital Power vs Sampling Frequency

8.13.2 Contour

All graphs are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

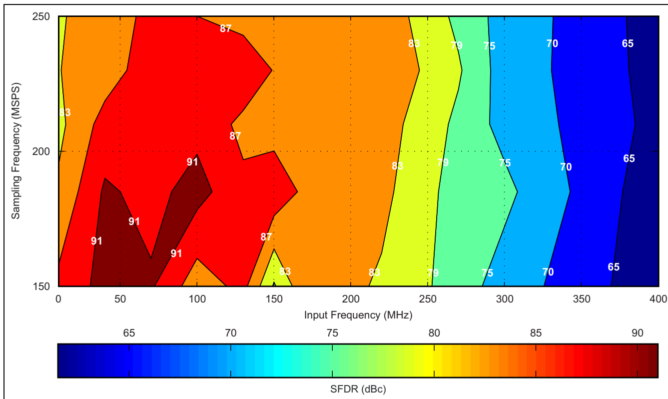


Figure 33. Spurious-Free Dynamic Range (0-dB Gain)

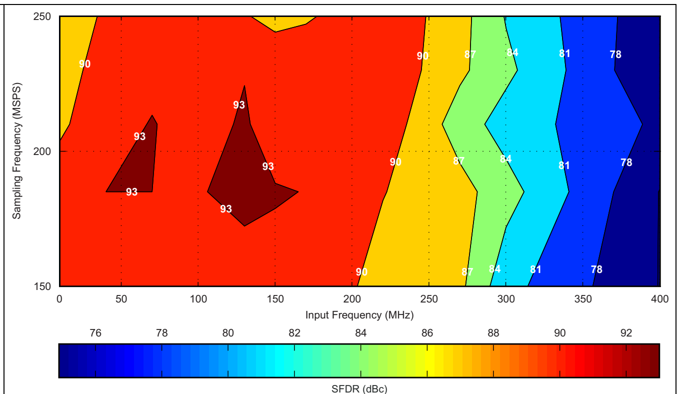


Figure 34. Spurious-Free Dynamic Range (6-dB Gain)

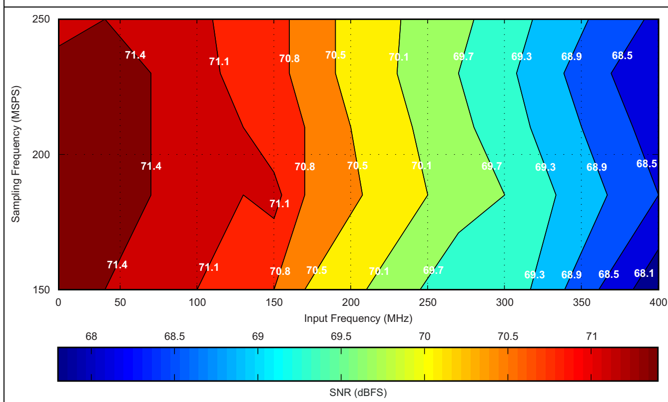


Figure 35. Signal-to-Noise Ratio (0-dB Gain)

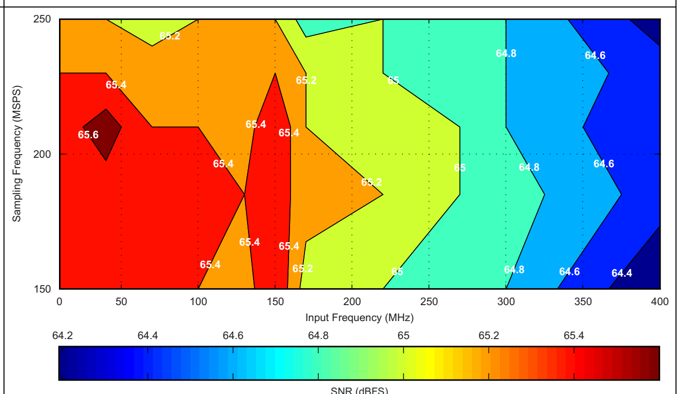
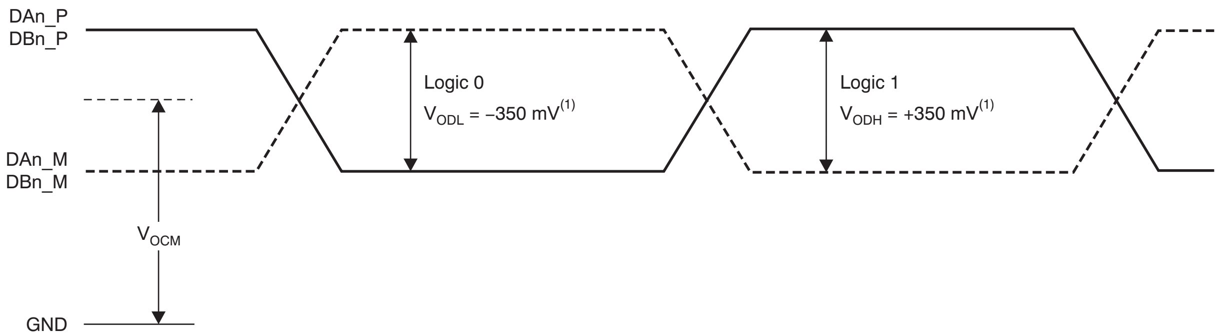


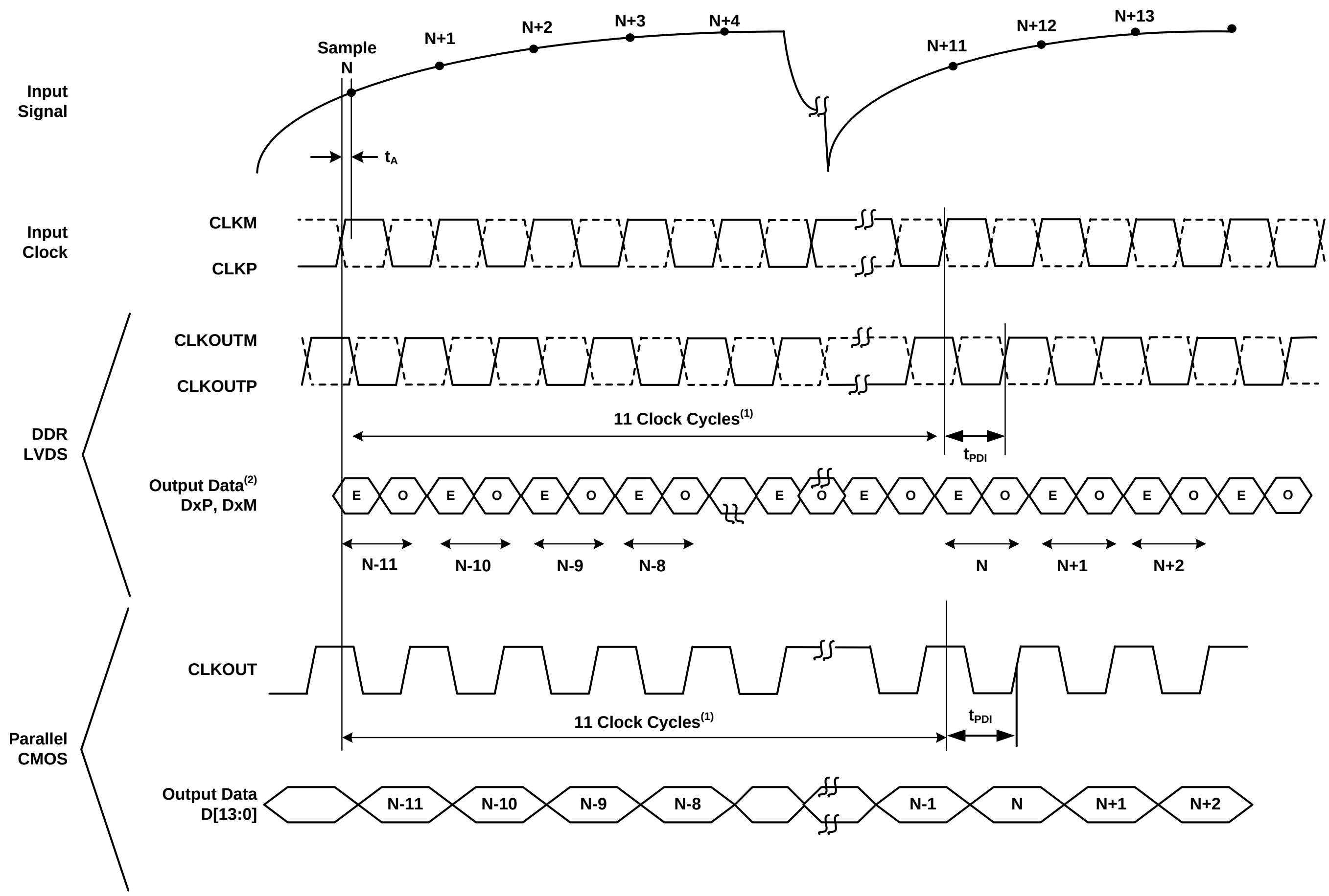
Figure 36. Signal-to-Noise Ratio (6-dB Gain)

9 Parameter Measurement Information



(1) With an external 100-Ω termination.

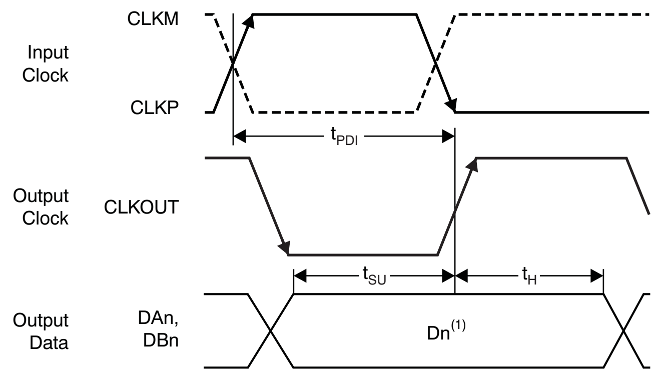
Figure 37. LVDS Output Voltage Levels



(1) The ADC latency after reset is 11 clock cycles. Overall latency = ADC latency + t_{PDI}.
(2) E = even bits (D0, D2, D4, and so forth); O = odd bits (D1, D3, D5, and so forth).

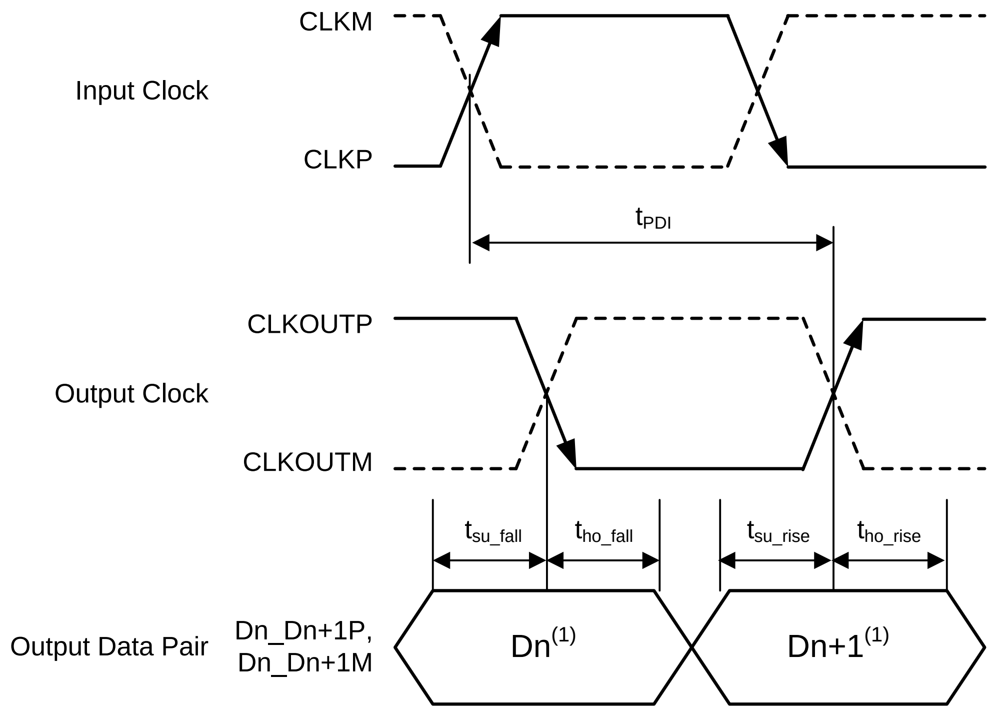
Figure 38. Latency Timing Diagram

Parameter Measurement Information (continued)



(1) D*n* = bits D0, D1, D2, and so forth of channels A and B.

Figure 39. CMOS Interface Timing Diagram



(1) D*n* = D0, D2, D4, and so forth. D*n*+1 = D1, D3, D5, and so forth.

Figure 40. LVDS Interface Timing Diagram

Parameter Measurement Information (continued)

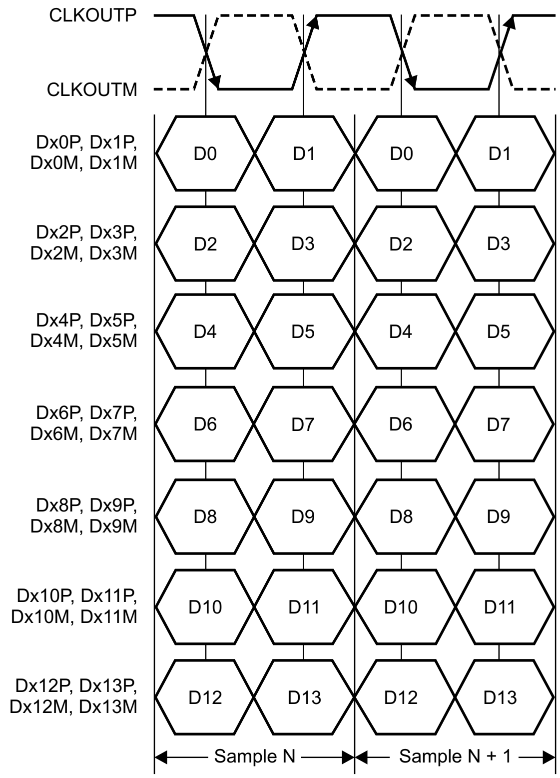


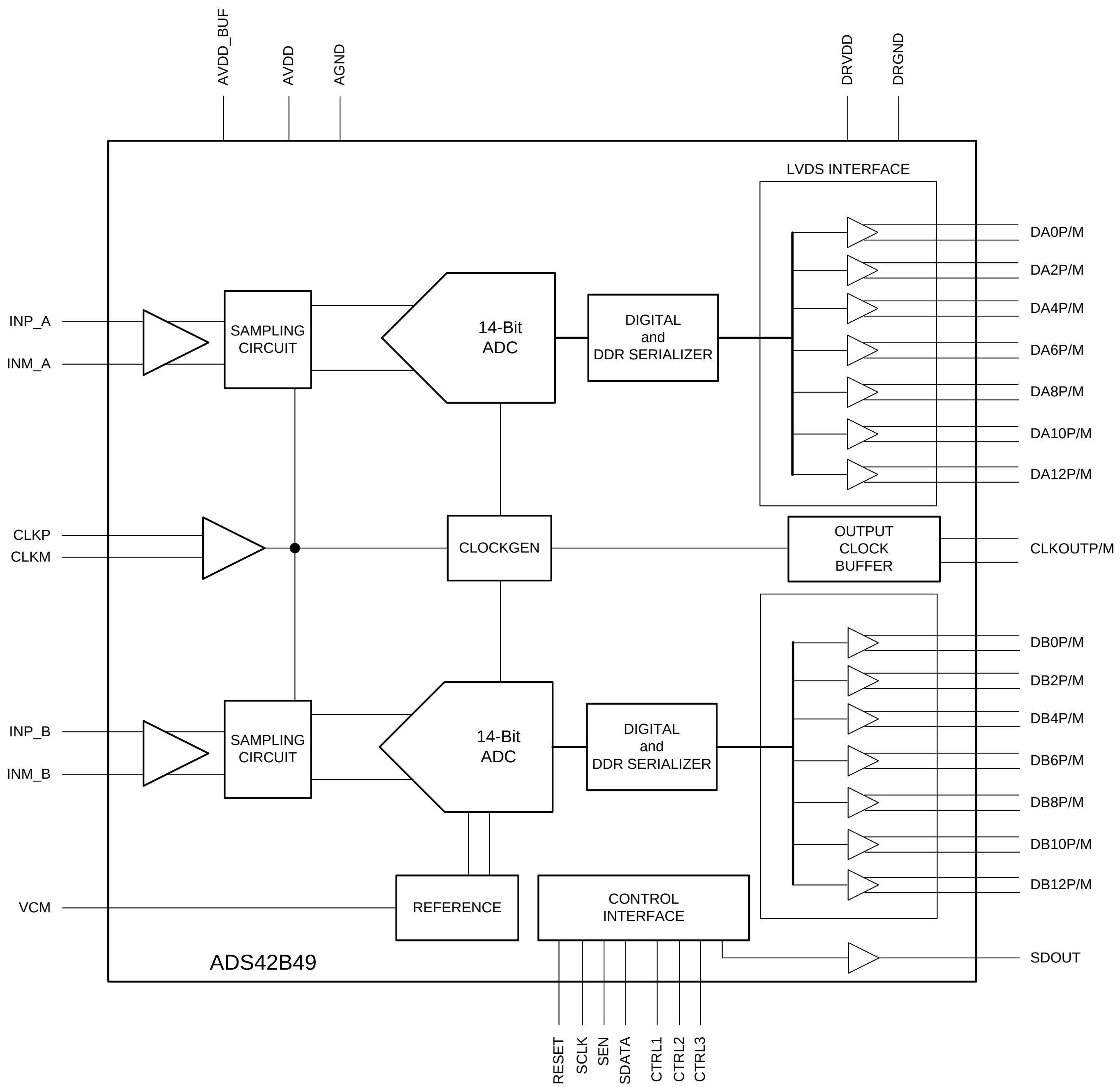
Figure 41. LVDS Bit Order

10 Detailed Description

10.1 Overview

The ADS42B49 belongs to a family of buffered analog input and ultralow-power analog-to-digital converters (ADCs) with maximum sampling rates up to 250 MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 11 clock cycles. The output is available as 14-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Migrating from the ADS62P49 and ADS4249

The ADS42B49 is pin-compatible with the previous generation ADS62P49 data converter; this similar architecture enables easy migration. However, there are some important differences between the two device generations, summarized in Table 1.

Table 1. Migrating from the ADS62P49 and ADS4249

ADS62P49	ADS4249	ADS42B49
PINS		
Pin 22 is NC (not connected). Must float.	Pin 22 is AVDD (1.8 V)	Pin 22 is AVDD (1.9 V)
Pin 34 is AVDD (3.3 V)	Pin 34 is AVDD (1.8 V)	Pin 34 is AVDD_BUF (3.3 V)
Pin 38 is DRVDD (1.8 V)	Pin 38 is NC. Must float.	Pin 38 is DRVDD (1.8 V)
Pin 39 is DRGND	Pin 39 is NC. Must float.	Pin 39 is DRGND
Pin 58 is DRVDD (1.8 V)	Pin 58 is NC. Must float.	Pin 58 is DRVDD (1.8 V)
Pin 59 is DRGND	Pin 59 is NC. Must float.	Pin 59 is DRGND
SUPPLY		
AVDD is 3.3 V	AVDD is 1.8 V	AVDD is 1.9 V
DRVDD is 1.8 V	DRVDD is 1.8 V	DRVDD is 1.8 V
		AVDD_BUF is 3.3 V
INPUT COMMON-MODE VOLTAGE		
CM is 1.5 V	CM is 0.95 V	CM is 1.9 V
BIASING FOR INPUT PINS (INP, INM)		
INP and INM must be externally biased at 1.5 V	NP and INM must be externally biased at 0.95 V	INP and INM do not require external biasing. Device internally biases these pins to 1.9 V.
EXTERNAL REFERENCE		
Supported	Not supported	Not supported
PARALLEL CONFIGURATION		
SCLK pin controls internal and external reference mode	SCLK pin enables low-speed mode	SCLK pin enables low-speed mode

10.3.2 Digital Functions

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. Figure 42 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to 1. After this, the respective register bits must be programmed as described in the following sections and in the *Register Maps* section.

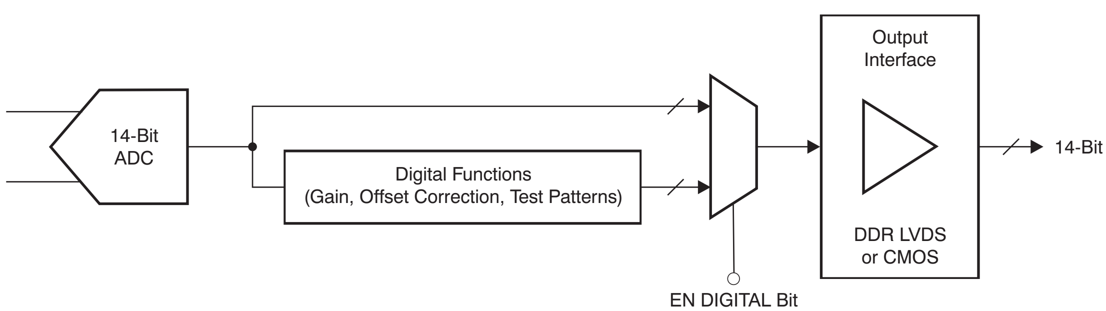


Figure 42. Digital Processing Block

10.3.3 Gain for SFDR and SNR Trade-Off

The ADS42B49 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 2.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 2. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	1.9
1	Fine, programmable	1.69
2	Fine, programmable	1.51
3	Fine, programmable	1.35
4	Fine, programmable	1.2
5	Fine, programmable	1.07
6	Fine, programmable	0.95

10.3.4 Offset Correction

The ADS42B49 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 3.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

Table 3. Time Constant of Offset Correction Algorithm

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1 / f_S$ (ms)[1]
0000	1 M	4
0001	2 M	8
0010	4 M	16.7
0011	8 M	33.5
0100	16 M	67
0101	32 M	134
0110	64 M	268
0111	128 M	537
1000	256 M	1010
1001	512 M	2150
1010	1 G	4300
1011	2 G	8600
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250 MSPS.

10.4 Device Functional Modes

Table 4. High-Performance Modes(1)(2)

PARAMETER	DESCRIPTION
High-performance modes	Set the HIGH PERF MODE[0] to improve SNR in CMOS mode by approximately 0.5 dB at 170 MHz. Register Address = 03h, data = 02h Set the HIGH PERF MODE[1:11] bits to obtain best performance across input signal frequencies. Register Address = 06h, data = 06h Register Address = BAh, data = 08h Register Address = D5h, data = 20h Register Address = D9h, data = 22h Register Address = DBh, data = E0h Register Address = DCh, data = 22h

(1) TI recommends using these modes to obtain best performance.
(2) See the *Serial Interface Configuration* section for details on register programming.

10.4.1 Power-Down

The ADS42B49 has two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in Table 5).

Table 5. Power-Down Settings

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Default
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Partial power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] pins

10.4.1.1 Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of typically less than 10 mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100 µs.

10.4.1.2 Channel Standby

In this mode, each ADC channel is powered down. The internal references are active, resulting in a quick wake-up time of 50 µs. The total power dissipation in standby is approximately 240 mW at 250 MSPS.

10.4.1.3 Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 190 mW.

10.4.2 Digital Output Information

The ADS42B49 provides 14-bit digital data for each channel and an output clock synchronized with the data.

10.4.2.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

10.4.2.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 43.

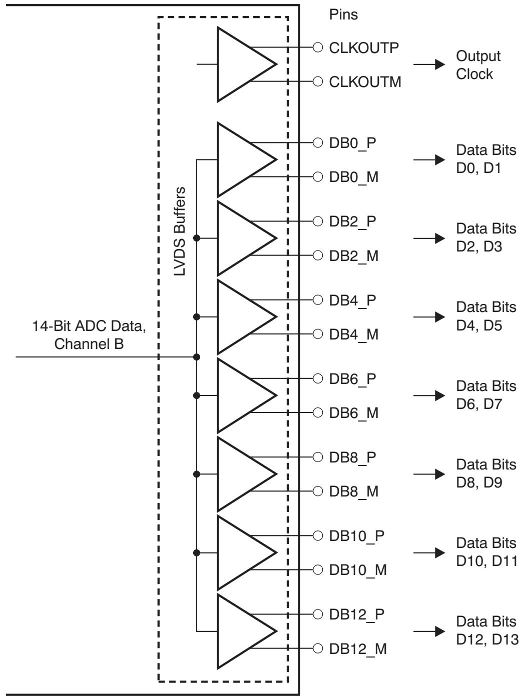


Figure 43. LVDS Interface

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 44.

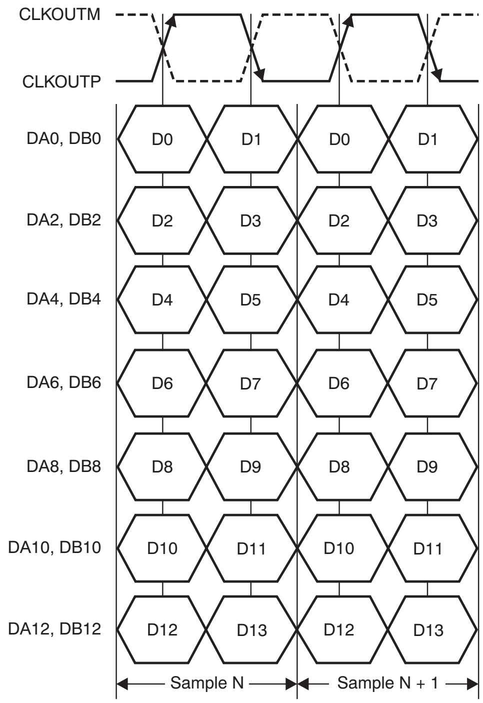
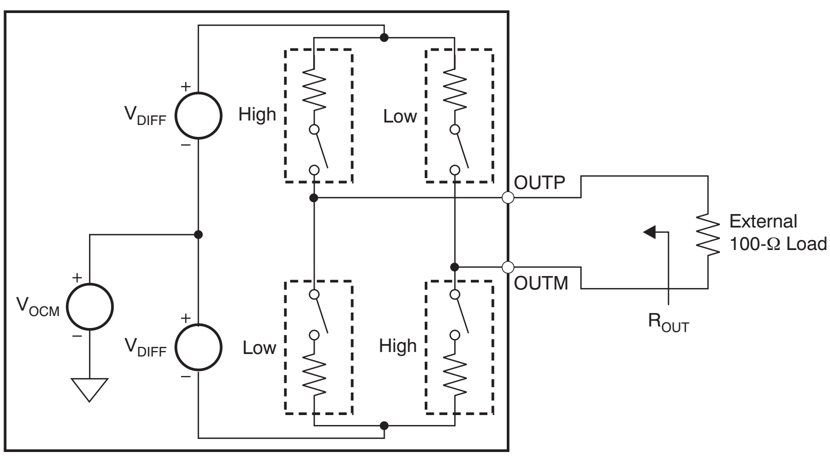


Figure 44. DDR LVDS Interface Timing

10.4.2.3 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 45. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.



NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

Figure 45. LVDS Buffer Equivalent Circuit

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 46. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

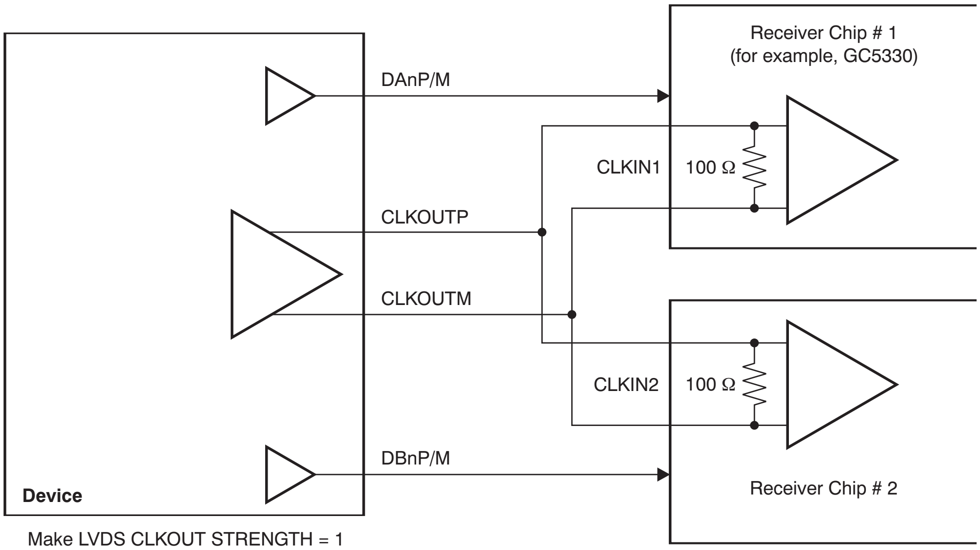


Figure 46. LVDS Buffer Differential Termination

10.4.2.4 Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as Figure 47 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. TI recommends minimizing the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

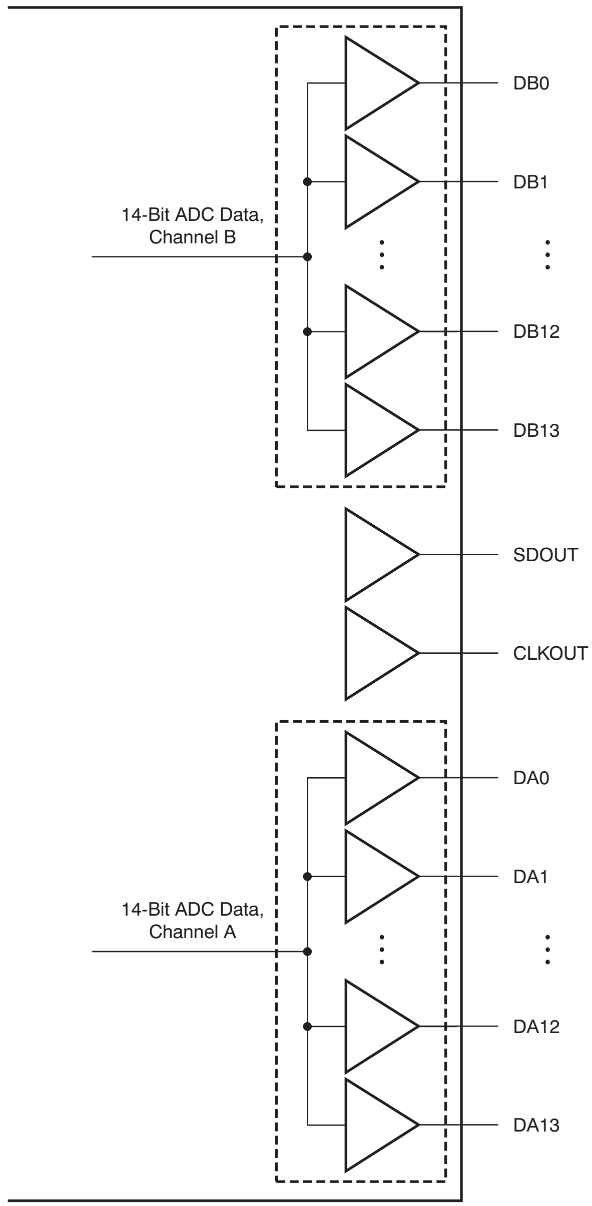


Figure 47. CMOS Outputs

10.4.2.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

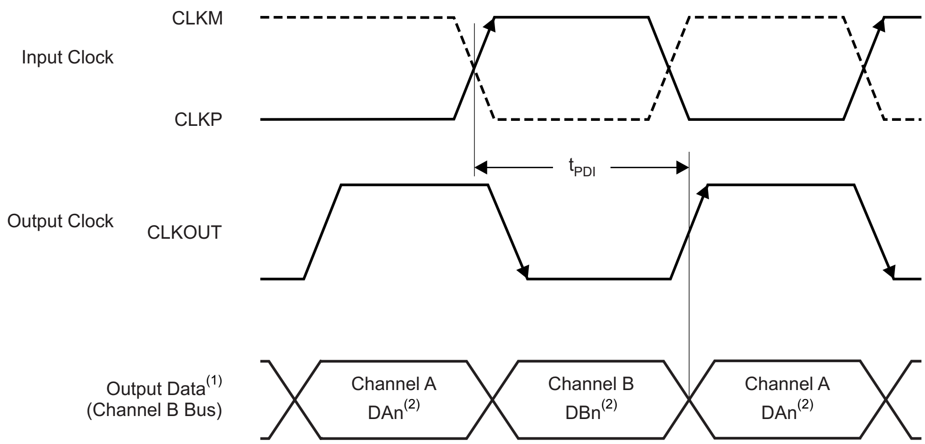
$$\text{Digital current as a result of CMOS output switching} = C_L \times DRVDD \times (N \times F_{AVG}) \quad (1)$$

where

- C_L = load capacitance
- $N \times F_{AVG}$ = average number of output bits switching

10.4.2.6 Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[11:0] pins), as shown in Figure 48. The channel A output pins (DA[11:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 125 MSPS). This mode can be enabled by the CTRL[3:1] parallel pins.



(1) In multiplexed mode, the output of both channels comes on the channel B output pins.

(2) Dn = bits D0, D1, D2, and so forth

Figure 48. Multiplexed Mode Timing Diagram

10.4.2.7 Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFFh for the ADS42B49 in offset binary output format; the output code is 1FFFh for the ADS42B49 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 2000h for the ADS42B49 in twos complement output format.

10.4.3 Parallel Configuration Details

The functions controlled by each parallel pin are described in Table 6, Table 7, and Table 8. A simple way of configuring the parallel pins is shown in Figure 49.

Table 6. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
Low	Low-speed mode is disabled
High	Low-speed mode is enabled

Table 7. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (50 mV / 0 mV)	Twos complement and parallel CMOS output
(3 / 8) AVDD (±50 mV)	Offset binary and parallel CMOS output
(5 / 8) AVDD (±50 mV)	Offset binary and DDR LVDS output
AVDD (0 mV / –50 mV)	Twos complement and DDR LVDS output

Table 8. CTRL1, CTRL2, and CTRL3 Pins

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Partial power-down
High	Low	High	Channel A is powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] pins.

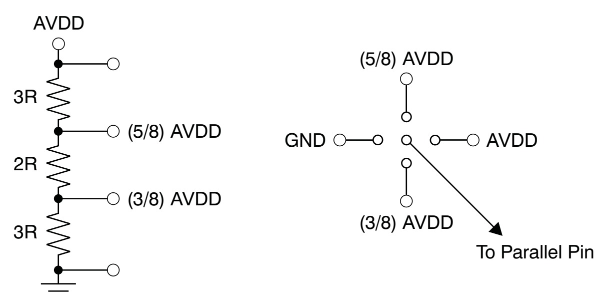


Figure 49. Simple Scheme to Configure the Parallel Pins

10.5 Programming

The ADS42B49 can be configured independently using either parallel interface control or serial interface programming.

10.5.1 Parallel Configuration Only

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 9 to Table 8). There is no need to apply a reset and SDATA can be connected to ground.

Programming (continued)

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 9 describes the modes controlled by the parallel pins.

Table 9. Parallel Pin Definition

PIN	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	Together, these pins control the power-down modes and multiplexed-mode selection (in CMOS interface)
CTRL2	
CTRL3	

10.5.2 Serial Interface Configuration Only

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Register Maps* section describes the register programming and the register reset process in more detail.

10.5.3 Using Both Serial Interface and Parallel Controls

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 8). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to 1. After reset, the RESET pin must be kept low. The *Register Maps* section describes register programming and the register reset process in more detail.

10.5.4 Serial Interface Details

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

10.5.4.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Through a hardware reset by applying a high pulse on the RESET pin (of width greater than 10 ns), as shown in Figure 50 and Serial Interface Timing Characteristics; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low. See Figure 51 and Reset Timing (Only When Serial Interface is Used) for reset timing.

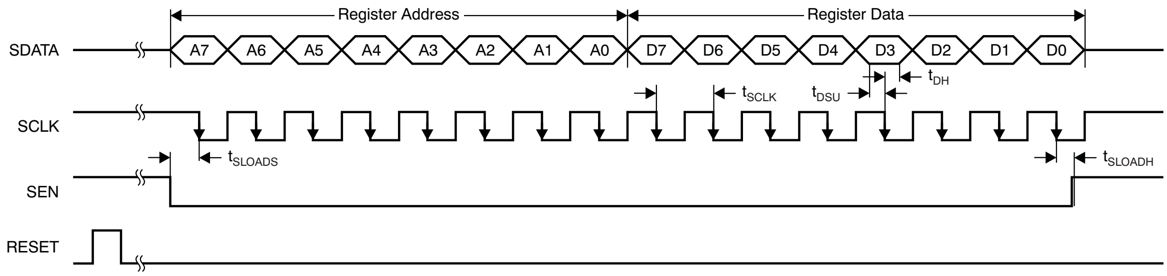
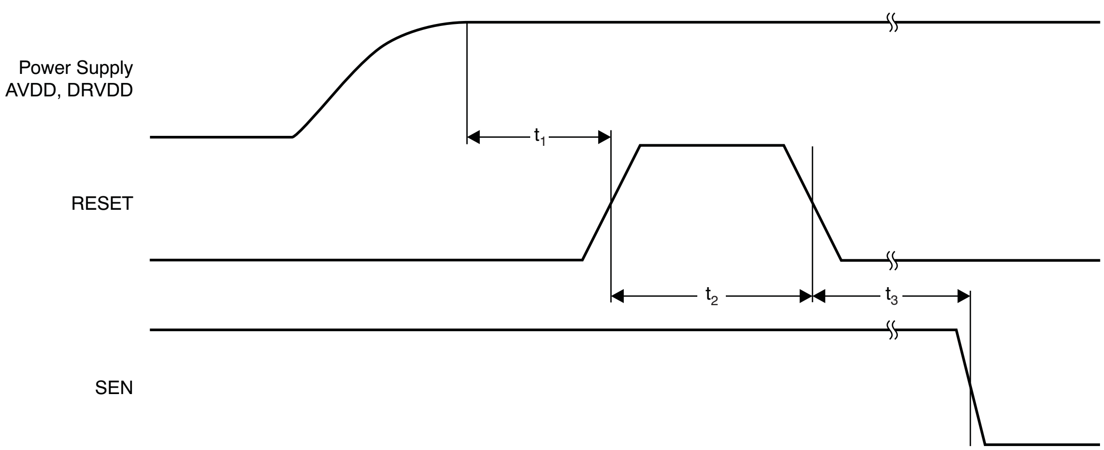


Figure 50. Serial Interface Timing



NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 51. Reset Timing Diagram

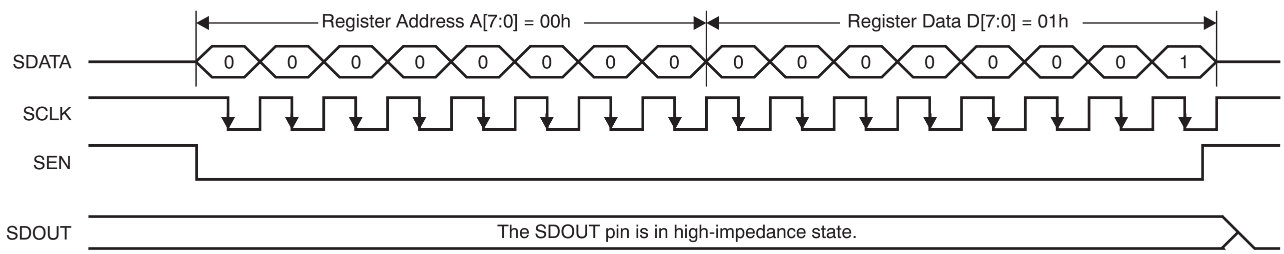
10.5.4.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

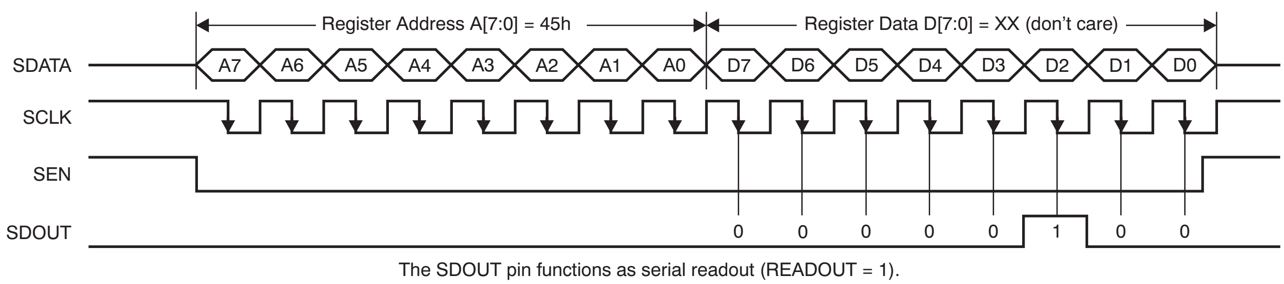
1. Set the READOUT register bit to 1. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to 0.

The serial register readout works with both CMOS and LVDS interfaces on pin 64. A serial readout timing diagram is shown in Figure 52.

Note that the contents of register 00h cannot be read back because the register contains RESET and READOUT bits. When READOUT is disabled, the SDOUT pin is in a high-impedance state.



a) Enable serial readout (READOUT = 1)



b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

Figure 52. Serial Readout Timing Diagram

10.6 Register Maps

Table 10 summarizes the functions supported by the serial interface.

Table 10. Serial Interface Register Map(1)

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	RESET	READOUT
01	LVDS SWING						0	0
03	0	0	0	0	0	0	HP[0]	0
06	0	0	0	0	0	HP[2]	HP[1]	0
25	CH A GAIN				0	CH A TEST PATTERNS		
29	0	0	0	DATA FORMAT		0	0	0

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to 0 after reset.

Register Maps (continued)

Table 10. Serial Interface Register Map(1) (continued)

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2B	CH B GAIN				0	CH B TEST PATTERNS		
3D	0	0	ENABLE OFFSET CORR	0	0	0	0	0
3F	0	0	CUSTOM PATTERN D[13:8]					
40	CUSTOM PATTERN D[7:0]							
41	LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	
42	CLKOUT DELAY PROG				0	0	0	0
44	0	0	0	0	0	0	0	EN DIGITAL
45	STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0
BA	0	0	0	0	HP[3]	0	0	0
BF	CH A OFFSET PEDESTAL				0	0	0	0
C1	CH B OFFSET PEDESTAL				0	0	0	0
CF	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
D5	0	0	HP[4}	0	0	0	0	0
D9	0	0	HP[6]	0	0	0	HP[5]	0
DB	HP[9]	HP[8]	HP[7]	0	0	0	0	LOW SPEED MODE CH B
DC	0	0	HP[11]	0	0	0	HP[10]	0
EF	0	0	0	EN LOW SPEED MODE	0	0	0	0
F1	0	0	0	0	0	0	EN LVDS SWING	
F2	0	0	0	0	LOW SPEED MODE CH A	0	0	0

10.6.1 Register Description

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits 7-2 **Always write 0**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits 7-2 **LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to 1 before programming swing.
000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing ±410 mV
110010 = LVDS swing ±465 mV
010100 = LVDS swing ±570 mV
111110 = LVDS swing ±200 mV
001111 = LVDS swing ±125 mV

Bits 1-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HP[0]	0

Bits 7-2 **Always write 0**

Bit 1 **HP[0]**

This bit improves SNR in CMOS mode, increases AVDD supply current by approximately 3 mA.

0 = Default after reset

1 = HP[0] is enabled

Bit 0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	0	0	HP[2]	HP[1]	0

Bits 7-3 **Always write 0**

Bits 2-1 **HP[2:1]**

Set bits HP[11:1] for best performance.

00 = Default after reset

11 = HP[2:1] are enabled

Bit 0 **Always write 0**

7	6	5	4	3	2	1	0
CH A GAIN				0	CH A TEST PATTERNS		

Bits 7-4 **CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel A.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit 3 **Always write 0**

Bits 2-0 **CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

7	6	5	4	3	2	1	0
0	0	0	DATA FORMAT		0	0	0

Bits 7-5 **Always write 0**

Bits 4-3 **DATA FORMAT: Data format selection**

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

Bits 2-0 **Always write 0**

7	6	5	4	3	2	1	0
CH B GAIN				0	CH B TEST PATTERNS		

Bits 7-4 **CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel B.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit 3 **Always write 0**

Bits 2-0 **CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[11:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

7	6	5	4	3	2	1	0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

Bits 7-6 **Always write 0**

Bit 5 **ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits 4-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits 7-6 **Always write 0**

Bits 5-0 **CUSTOM PATTERN D[13:8]**

These are the six upper bits of the custom pattern available at the output instead of ADC data.
The ADS42B49 custom pattern is 14-bit.

7	6	5	4	3	2	1	0
CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0

Bits 7-0 **CUSTOM PATTERN D[7:0]**

These are the eight lower bits of the custom pattern available at the output instead of ADC data.
The ADS42B49 custom pattern is 14-bit; use the CUSTOM PATTERN D[13:0] register bits.

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	

Bits 7-6 **LVDS CMOS: Interface selection**

These bits select the interface.
00 = DDR LVDS interface
01 = DDR LVDS interface
10 = DDR LVDS interface
11 = Parallel CMOS interface

Bits 5-4 **CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bits 3-2 **Always write 0**

Bits 1-0 **DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.
00 = Default
01 = Power-down data output buffers for channel B
10 = Power-down data output buffers for channel A
11 = Power-down data output buffers for both channels as well as the clock output buffer

7	6	5	4	3	2	1	0
CLKOUT DELAY PROG				0	0	0	0

Bits 7-4 **CLKOUT DELAY PROG**

These bits are useful to delay output clock in LVDS mode to optimize setup and hold time. Typical delay in output clock obtained by these bits in LVDS mode is given below:
0000 = Default
0001 = 190 ps
0010 = 350 ps
0011 = 700 ps
0111 = 1000 ps
1011 = 1250 ps
1111 = 1450 ps
Others = Do not use

Bits 3-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN DIGITAL

Bits 7-1 **Always write 0**

Bit 0 **EN DIGITAL: Digital function enable**

0 = Default

1 = Digital functions including test pattern are enabled

7	6	5	4	3	2	1	0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

Bit 7 **STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wake-up time from this mode is fast (typically 50 µs).

Bit 6 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100-Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50-Ω external termination

Bit 5 **LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100-Ω external termination
1 = All LVDS data buffers have double strength to be used with 50-Ω external termination

Bits 4-3 **Always write 0**

Bit 2 **PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wake-up time from this mode is slow (typically 100 µs).

Bits 1-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	0	HP[3]	0	0	0

Bits 7-4 **Always write 0**

Bit 3 **HP[3]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[3] is enabled

Bits 2-0 **Always write 0**

7	6	5	4	3	2	1	0
CH A OFFSET PEDESTAL						0	0

Bits 7-4 **CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D[7:2].

Program bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits 3-0 **Always write 0**

7	6	5	4	3	2	1	0
CH B OFFSET PEDESTAL						0	0

Bits 7-4 **CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D7-D2.

Program Bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits 3-0 **Always write 0**

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

Bit 6 **Always write 0**

Bits 5-2 **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

Bits 1-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	HP[4]	0	0	0	0	0

Bits 7-6 **Always write 0**

Bit 5 **HP[4]**

Set bits HP[11:1] for best performance.

0 = Default after Reset

1 = HP[4] is enabled

Bits 4-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	HP[6]	0	0	0	HP[5]	0

Bits 7-6 **Always write 0**

Bit 5 **HP[6]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[6] is enabled

Bits 4-2 **Always write 0**

Bit 1 **HP[5]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[5] is enabled

Bit 0 **Always write 0**

7	6	5	4	3	2	1	0
HP[9]	HP[8]	HP[7]	0	0	0	0	LOW SPEED MODE CH B

Bits 7-5 **HP[9:7]**

Bit 5 **HP[6]**

Set bits HP[11:1] for best performance.

000 = Default after reset

111 = HP[9:7] are enabled

Bits 4-1 **Always write 0**

Bit 0 **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to 1 before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

7	6	5	4	3	2	1	0
0	0	HP[11]	0	0	0	HP[10]	0

Bits 7-6 **Always write 0**

Bit 5 **HP[11]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[11] is enabled

Bits 4-2 **Always write 0**

Bit 1 **HP[10]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[10] is enabled

Bit 0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	EN LOW SPEED MODE	0	0	0	0

Bits 7-5 **Always write 0**

Bit 4 **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.
0 = Low-speed mode is disabled
1 = Low-speed mode is controlled by serial register bits

Bits 3-0 **Always write 0**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN LVDS SWING	

Bits 7-2 **Always write 0**

Bits 1-0 **EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

7	6	5	4	3	2	1	0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

Bits 7-4 **Always write 0**

Bit 3 **LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to 1 before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

Bits 2-0 **Always write 0**

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The analog input pins have analog buffers (running off the AVDD_BUF supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 2.5-pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 700 MHz (measured with 50-Ω source driving 50-Ω termination between INP and INM).

The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 400 MHz (with 2-V_{PP} amplitude) and to approximately 500 MHz (with 1.6-V_{PP} amplitude) before the performance degrades. This offset is separate from the full-power analog bandwidth of 700 MHz, which is only an indicator of signal amplitude versus frequency.

11.1.1 Driving Circuit

Example driving circuit configuration is shown in Figure 53. Notice that the board circuitry is simplified compared to the non-buffered ADS4249.

To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 53. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

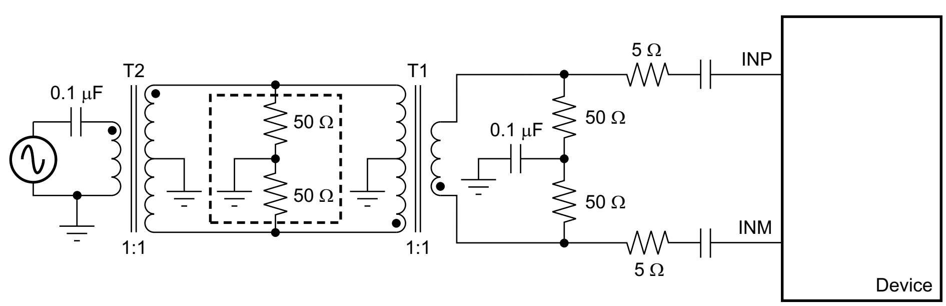


Figure 53. Drive Circuit for High Input Frequencies

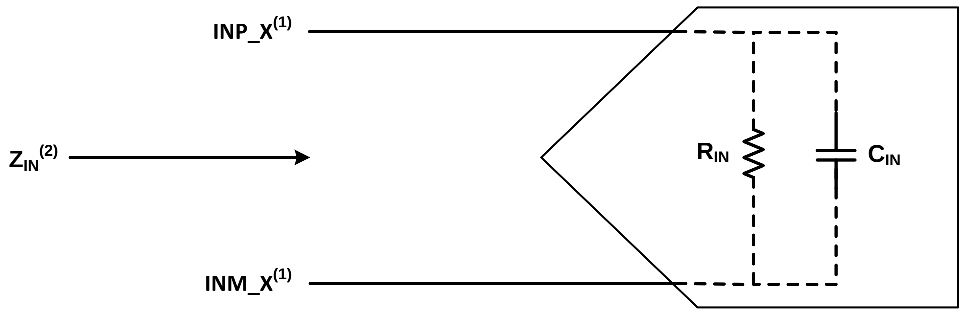
The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 53. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance).

Application Information (continued)

11.1.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 54, Figure 55, and Figure 56 show the differential impedance ($Z_{IN} = R_{IN}$ || C_{IN}) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.
(2) $Z_{IN} = R_{IN}$ || ($1/j\omega C_{IN}$).

Figure 54. ADC Equivalent Input Impedance

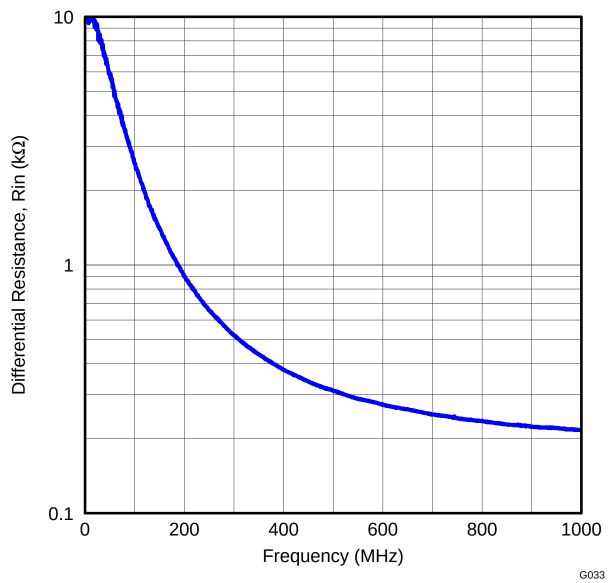


Figure 55. ADC Analog Input Resistance (R_{IN}) Across Frequency

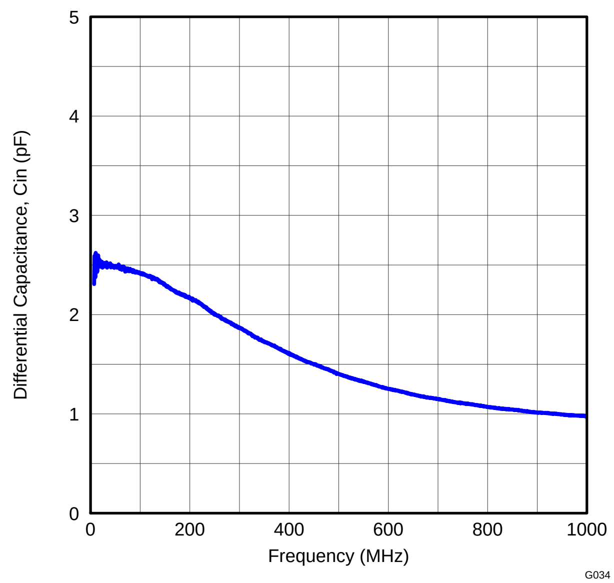
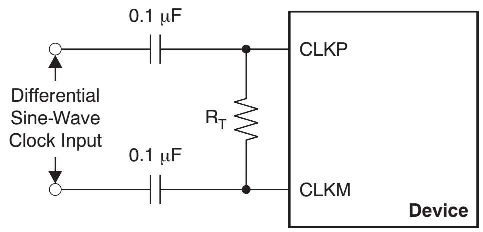


Figure 56. ADC Analog Input Capacitance (C_{IN}) Across Frequency

11.1.2 Clock Input

The ADS42B49 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in Figure 57, Figure 58 and Figure 59. See Figure 60 details the internal clock buffer.



Note: R_T = termination resistor, if necessary.

Figure 57. Differential Sine-Wave Clock Driving Circuit

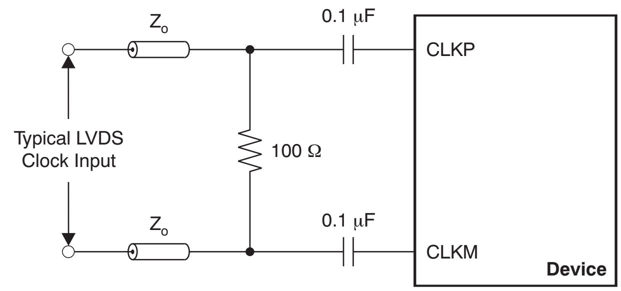


Figure 58. LVDS Clock Driving Circuit

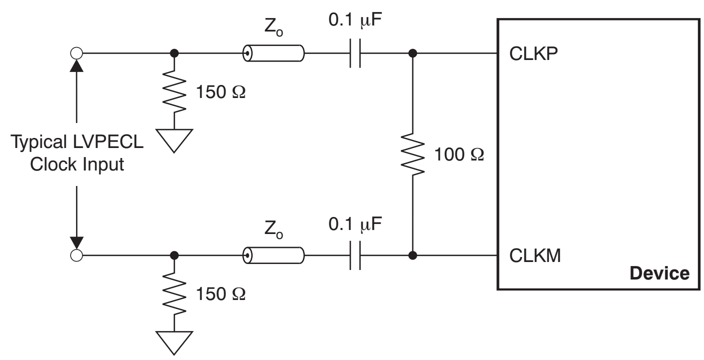
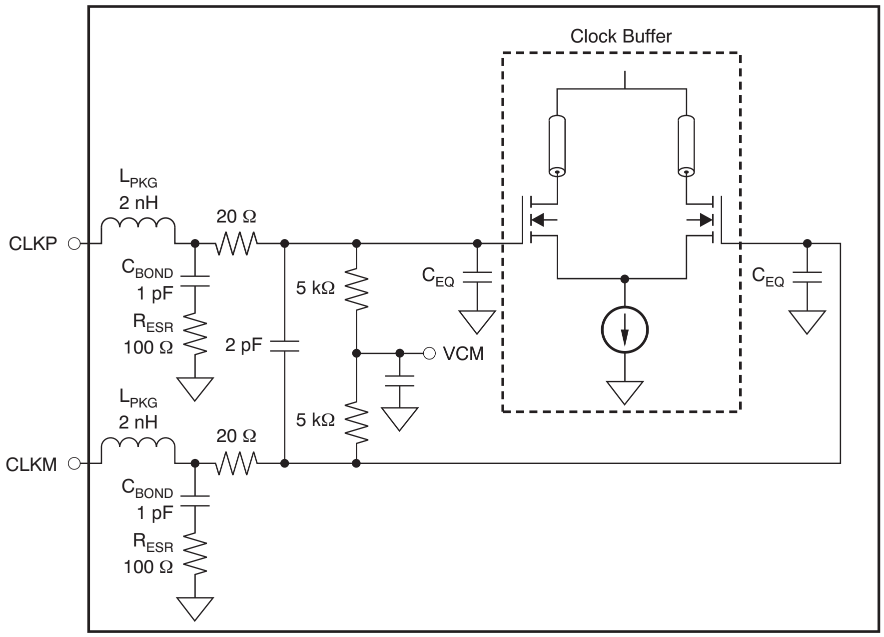


Figure 59. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 60. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 61. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

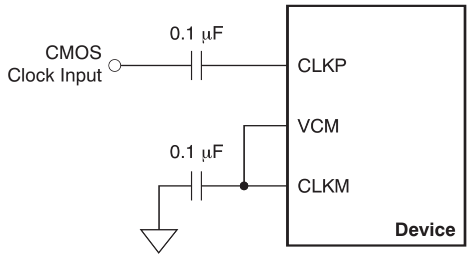


Figure 61. Single-Ended Clock Driving Circuit

11.2 Typical Application

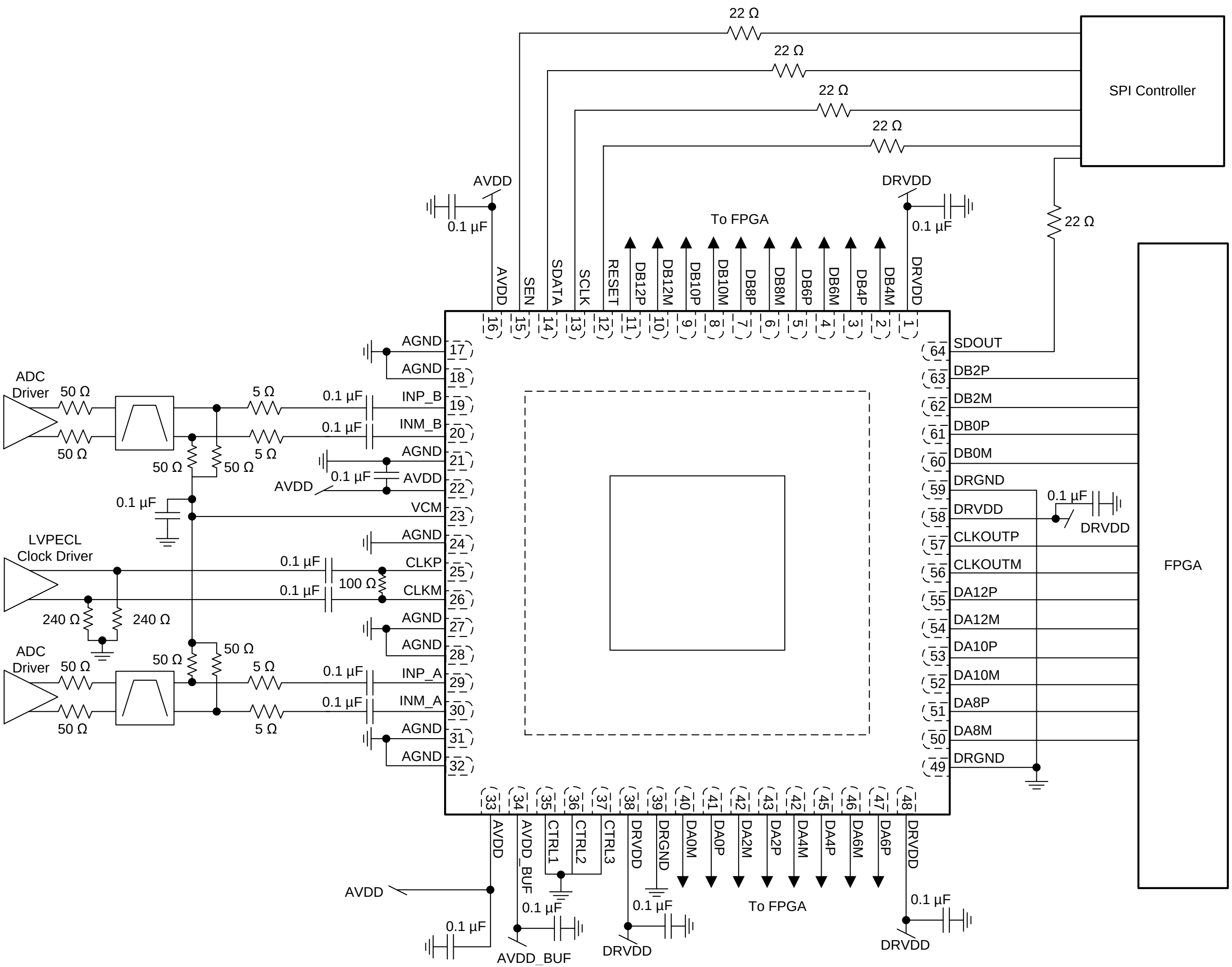


Figure 62. Example Schematic for ADS42B49

11.2.1 Design Requirements

Example design requirements are listed in Table 11 for the ADC portion of the signal chain. These do not necessary reflect the requirements of an actual system, but rather demonstrate why the ADS42B49 may be chosen for a system based on a set of requirements.

Typical Application (continued)

Table 11. Design Requirements for ADS42B49

DESIGN PARAMETER	EXAMPLE DESIGN REQUIREMENT	ADS42B49 CAPABILITY
Sampling rate	≥ 200 Msps to allow 125 MHz of unaliased bandwidth	Max sampling rate: 250 Msps
Input frequency	> 200 MHz to accommodate full 2nd nyquist zone	Large signal –3-dB bandwidth: 400-MHz operation
SNR	> 68 dBFS at –1 dFBS, 170 MHz	70.7 dBFS at –1 dBFS, 170 MHz (0-dB gain)
SFDR	> 80 dBc at –1 dFBS, 170 MHz	85 dBc at –1 dBFS, 170 MHz (0-dB gain)
Input full scale voltage	1.5 Vpp	1.5 Vpp
Overload recovery time	< 3 clock cycles	1 clock cycle
Digital interface	DDR LVDS	DDR LVDS
Power consumption	< 500 mW per channel	425 mW per channel

11.2.2 Detailed Design Procedure

11.2.2.1 Analog Input

The analog input of the ADS42B49 is typically driven by a fully-differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier affects the combined performance of the ADC and amplifier. The amplifier is often AC coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common-mode voltages. The user can DC couple the amplifier to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

11.2.2.2 Clock Driver

The ADS42B49 should be driven by a high performance clock driver, such as a clock jitter cleaner. The clock must have low noise to maintain optimal performance. LVPECL is the most common clocking interface, but LVDS and LVCMOS can also be used. Do not drive the clock input from an FPGA, unless the noise degradation can be tolerated, such as for input signals near DC where the clock noise impact is minimal.

11.2.2.3 Digital Interface

The ADS42B49 supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs, resistors should be placed in series with the outputs to reduce the output current spikes and limit the performance degradation. The resistors should be large enough to limit current spikes, but not so large as to significantly distort the digital output waveform. An external CMOS buffer should be used when driving distances greater than a few inches, to reduce ground bounce within the ADC.

11.2.3 Application Curves

Figure 63 and Figure 64 show performance obtained at 100-MHz and 280-Mhz input frequencies, respectively, using appropriate driving circuit.

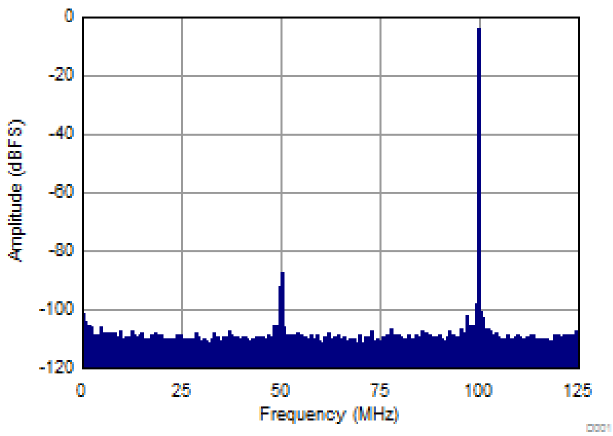


Figure 63. 100-MHz Input Frequency

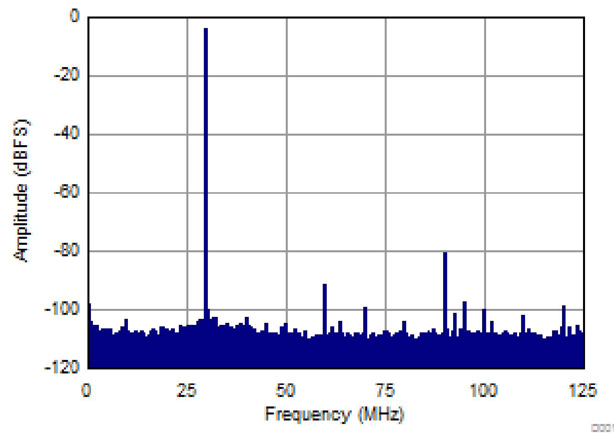


Figure 64. 280-MHz Input Frequency

12 Power Supply Recommendations

The ADS42B49 has three power supplies: two analog (AVDD and AVDD_BUF) and one digital (DRVDD) supply. The AVDD supply has a nominal voltage of 1.9 V. The AVDD_BUF supply has a nominal voltage of 3.3 V. DRVDD supply has a nominal voltage of 1.8 V. Both AVDD supplies are noise sensitive and the digital supply is not.

12.1 Using DC/DC Power Supplies

DC/DC switching power supplies can be used to power DRVDD without issue. Both AVDD supplies can be powered from a switching regulator. Noise and spurs on the AVDD power supply affect the SNR and SFDR of the ADC, and appear near DC and as a modulated component around the input frequency. If a switching regulator is used, it should be designed to have minimal voltage ripple. Supply filtering should be used to limit the amount of spurious noise at the AVDD supply pins. Extra placeholders should be placed on the schematic for additional filtering. Optimize filtering in the final system to achieve the desired performance. The choice of power supply ultimately depends on the system requirements. For instance, if very low phase noise is required, do not use a switching regulator.

12.2 Power Supply Bypassing

Because the ADS42B49 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. A 0.1-uF capacitor is recommended near each supply pin. The decoupling capacitors should be placed very close to the converter supply pins.

13 Layout

13.1 Layout Guidelines

13.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. Download the ADS42xx_58C28EVM DesignPkg file from the ADS42B49EVM product folder on the TI website for details on layout and grounding.

13.1.2 Supply Decoupling

Because the ADS42B49 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

13.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Thus, the exposed pad must be soldered to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

13.1.4 Routing Analog Inputs

TI advises routing differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock; see the *ADS42Bx EVM User's Guide* (SLAU477) for reference routing. Figure 65 shows a snapshot of the PCB layout from the ADS42xxEVM.

13.2 Layout Example

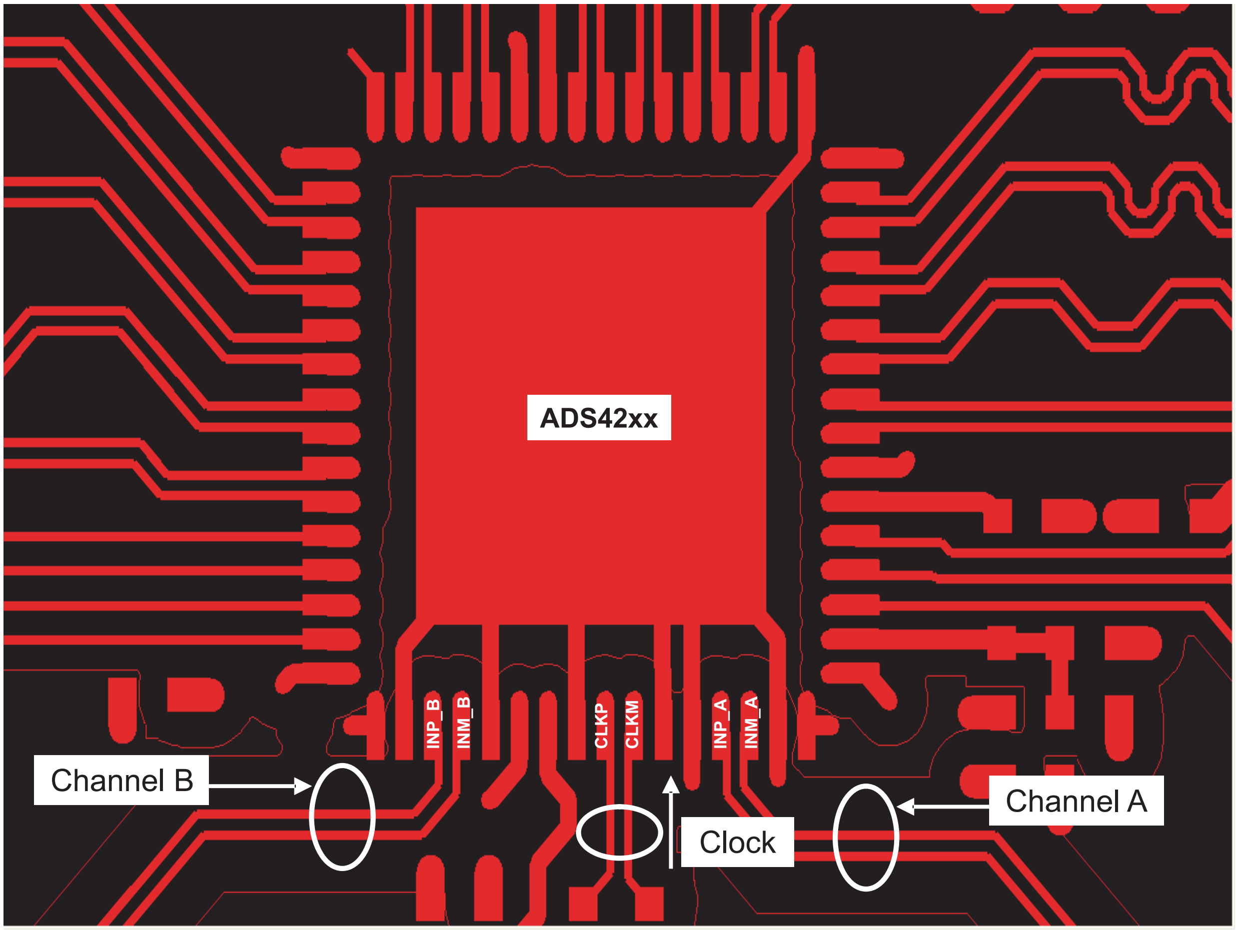


Figure 65. ADS42xxEVM PCB Layout

14 Device and Documentation Support

14.1 Device Support

14.1.1 Device Nomenclature

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle: The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy (E_{GREF}) and error as a result of the channel (E_{GCHAN}). Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 – 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error: The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (2)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (3)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Device Support (continued)

Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (5)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR): The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR): DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (6)$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (7)$$

Crosstalk (only for multichannel ADCs): Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

14.2 Documentation Support

14.2.1 Related Documentation

For related documentation, see the following:

- QFN Layout Guidelines (SLOA122)
- QFN/SON PCB Attachment (SLUA271)
- ADS42XX_58C28EVM DesignPkg (SLAC459)
- ADS42B4X User's Guide (SLAU477)

14.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS42B49IRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ42B49I	Samples
ADS42B49IRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ42B49I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

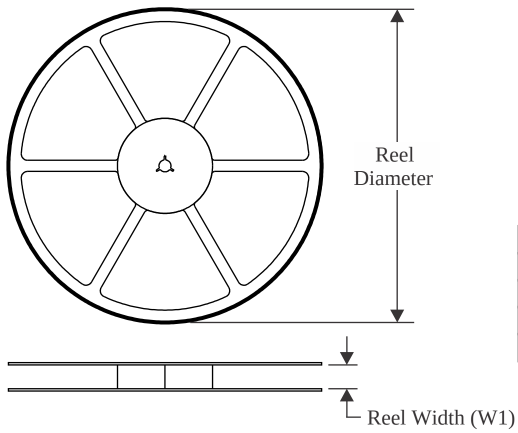
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

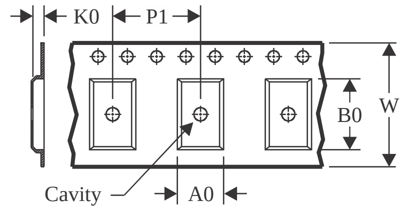
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

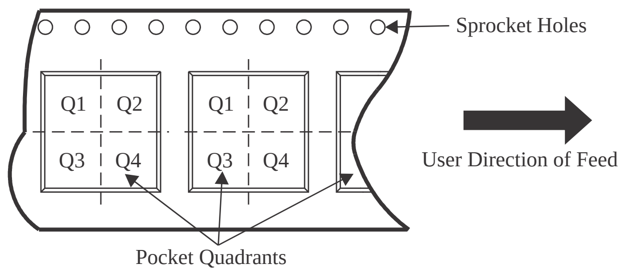


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

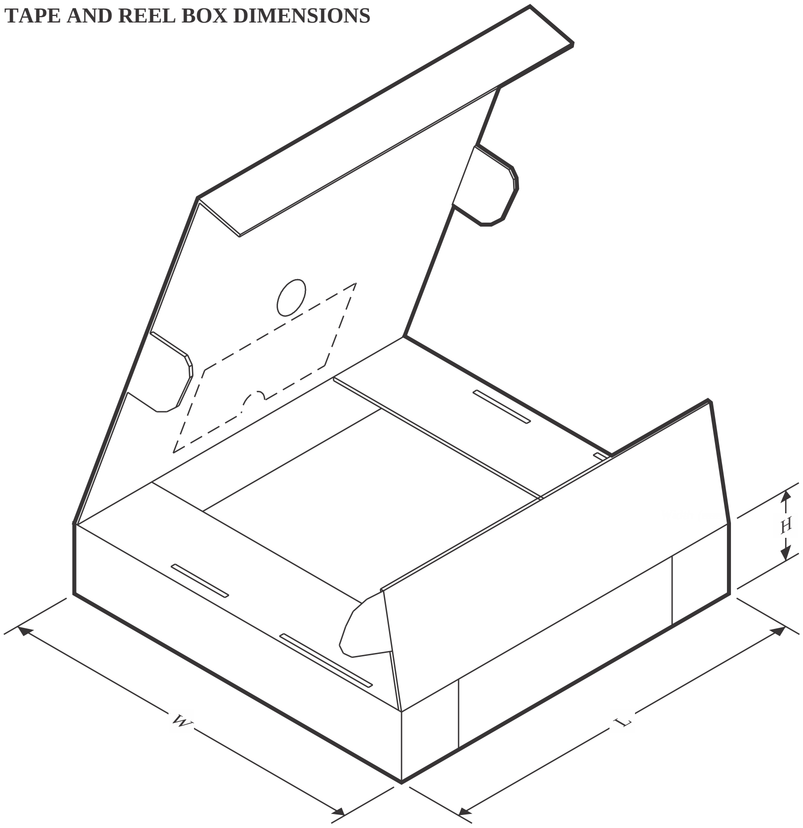
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS42B49IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

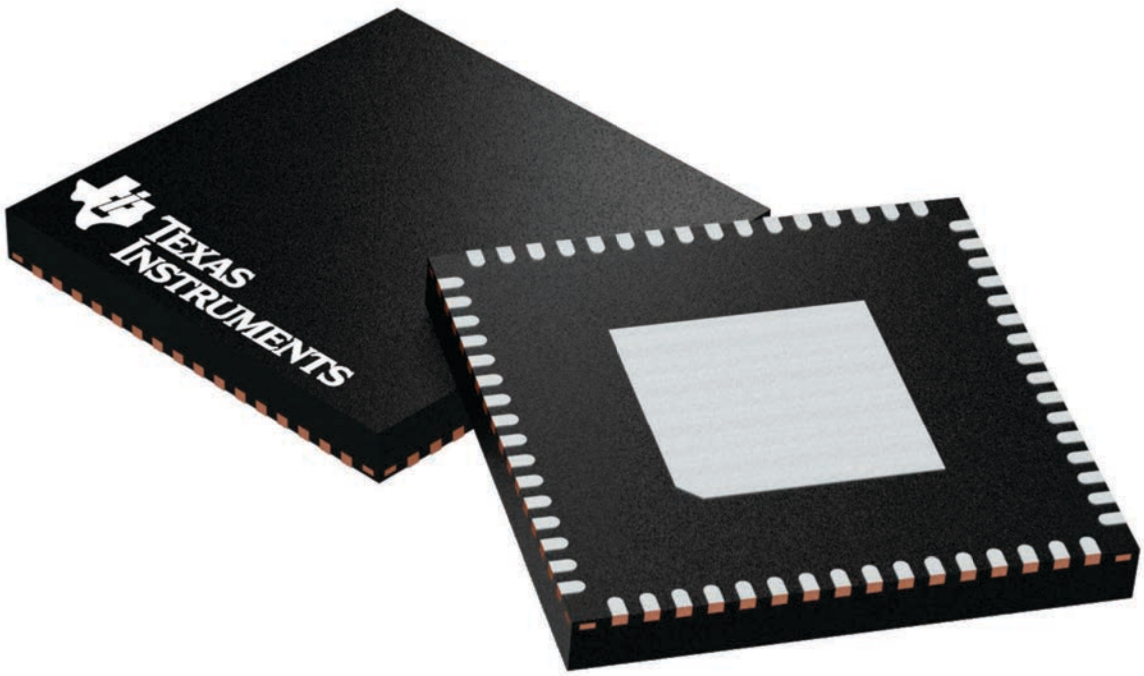
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS42B49IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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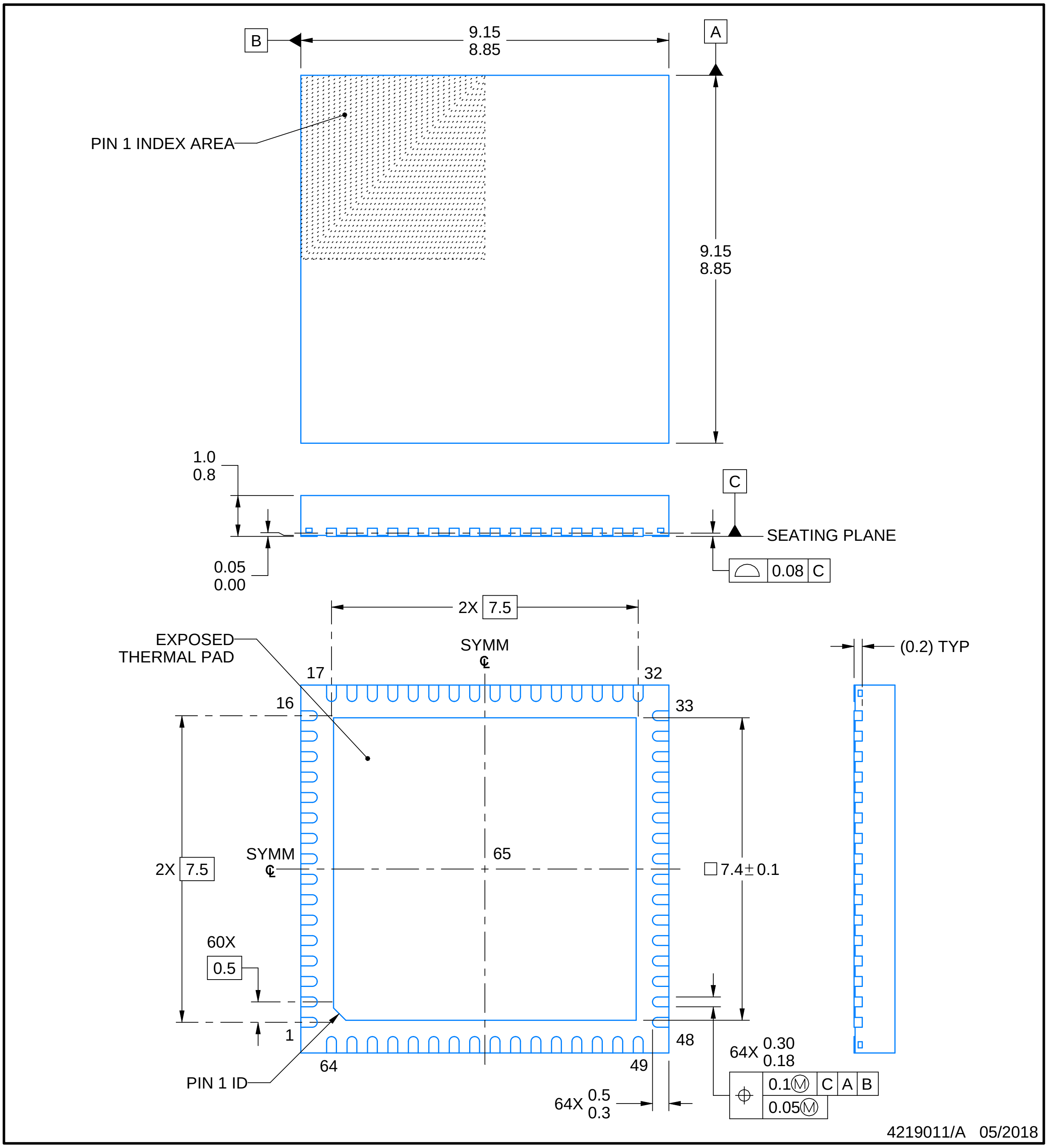
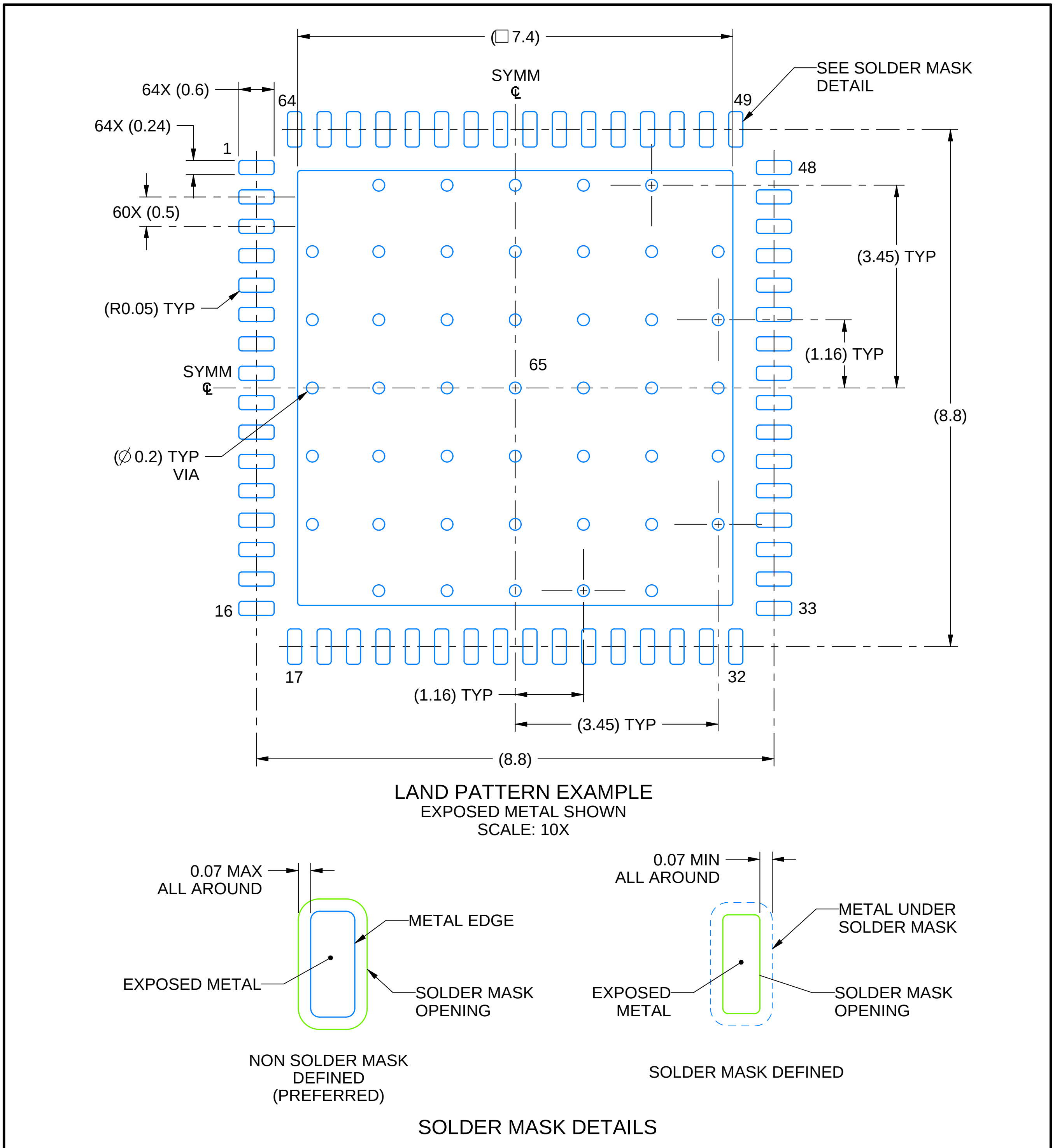


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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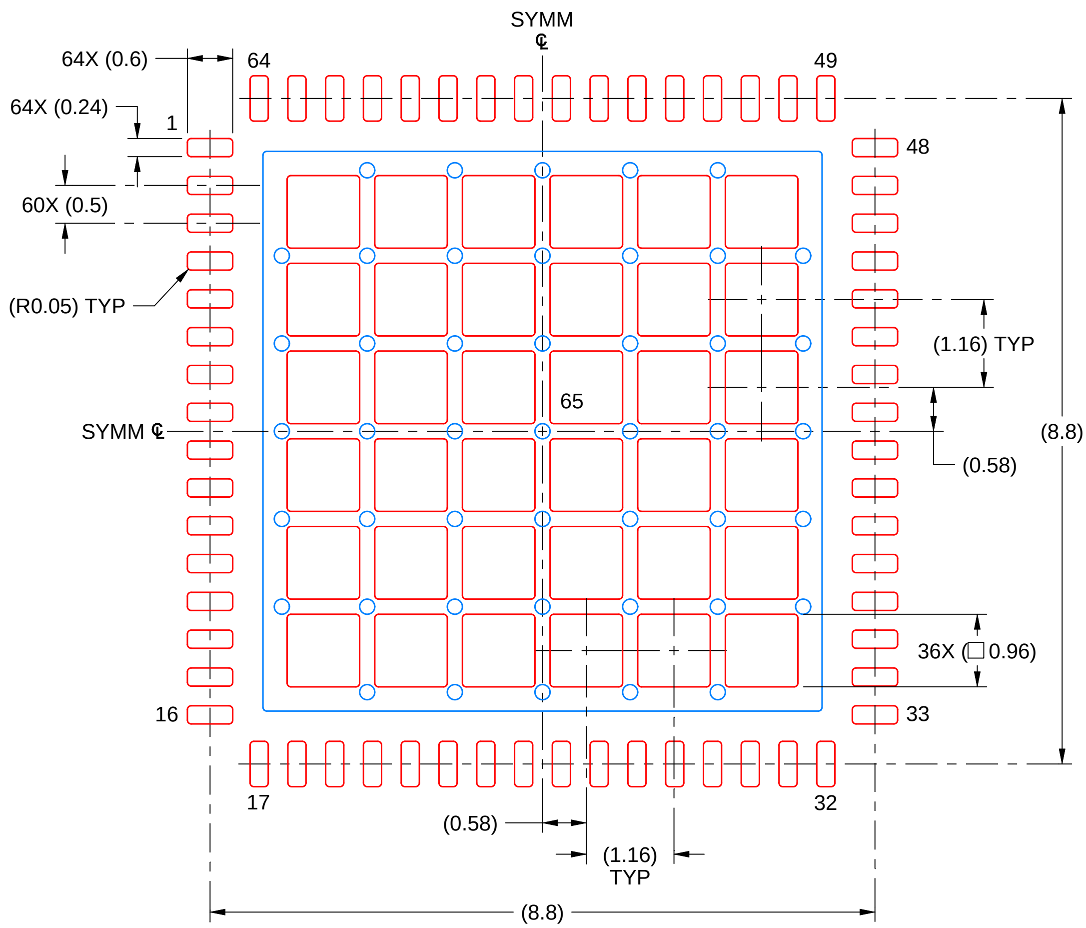
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.