ADS8353-Q1 車載用、16 ビット、2 チャネル 同時サンプリング、600kSPS のアナログ/デジタル・コンバータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 16 ビット分解能
- 2 チャネルの同時サンプリング
- シングルエンドおよび擬似差動入力をサポート
- 2 つのユニポーラ入力範囲をソフトウェアで選択可能
  - (0V～V_{REF}) または (0V～2×V_{REF})
- 最高 600kSPS のサンプリング速度
- 非常に優れた DC 性能
  - DNL:±0.6LSB
  - INL:±1LSB
  - ゲイン誤差:±0.05%
- 非常に優れた AC 性能
  - SNR:89dB
  - THD:-100dB
- デュアル、低ドリフト (10ppm/℃)、プログラム可能な 2.5V の内部基準電圧

2 アプリケーション

- バッテリ管理システム (BMS)
- DC/DC コンバータ
- エネルギー・ストレージ電力変換システム (PCS)
- ソーラー・アーク保護

3 概要

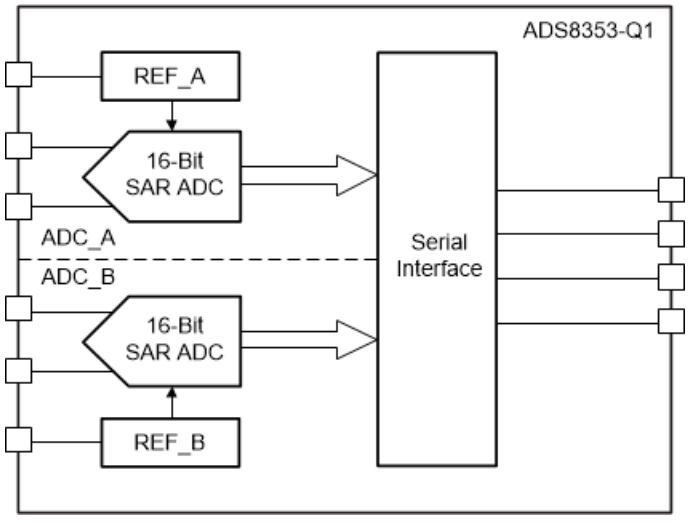
ADS8353-Q1 は 16 ビット、デュアル・チャネル、高速、同時サンプリングのアナログ/デジタル・コンバータ (ADC) で、シングル・エンドと擬似差動のアナログ入力に対応しています。

ADS8353-Q1 には 2 つの基準電圧源があり、独立してプログラム可能で、システム・レベルのゲイン較正に使用できます。また、広い電源電圧範囲で動作可能な、柔軟性の高いシリアル・インターフェイスにより、多くの種類のホスト・コントローラと簡単に通信できます。デバイスが 2 つの低消費電力モードをサポートしているため、与えられたスループットについて消費電力を最適化できます。ADS8353-Q1 は、-40℃～+125℃の温度範囲で完全に動作が規定されており、16 ピンの TSSOP パッケージで供給されます。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
ADS8353-Q1	TSSOP (16)	5.00mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーションの図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2019) to Revision B (July 2022)	Page
• *文書全体にわたって表、図、相互参照の採番方法を更新*	1
• 「特長」の車載特有の箇条書き項目を変更	1
• 「特長」セクションに機能安全対応の箇条書きを追加	1
• 「非常に優れた DC 性能」の副項目を変更:「DNL:±1LSB (標準値)」を「DNL:±0.6LSB」に変更し、「INL:±1LSB (標準値)」を「INL:±1LSB」に変更	1
• 「アプリケーション」セクションを変更	1

Changes from Revision * (January 2019) to Revision A (March 2019)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

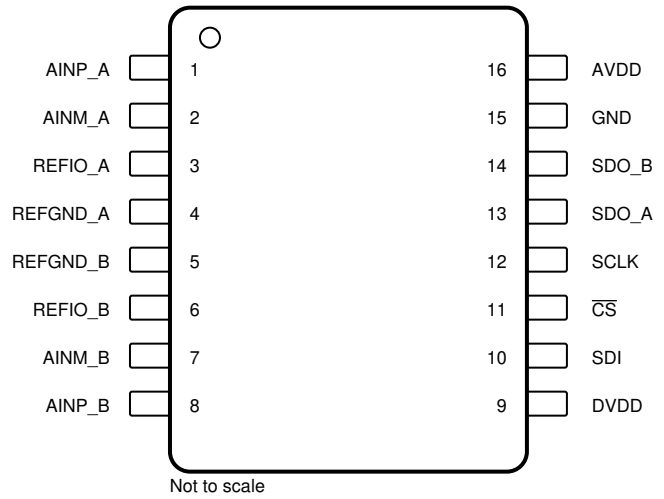


図 5-1. PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	TSSOP		
AINM_A	2	Analog input	Negative analog input, channel A
AINM_B	7	Analog input	Negative analog input, channel B
AINP_A	1	Analog input	Positive analog input, channel A
AINP_B	8	Analog input	Positive analog input, channel B
AVDD	16	Supply	Supply voltage for ADC operation
$\overline{CS}$	11	Digital input	Chip-select signal; active low
DVDD	9	Digital I/O supply	Digital I/O supply
GND	15	Supply	Digital ground
REFGND_A	4	Supply	Reference ground potential A
REFGND_B	5	Supply	Reference ground potential B
REFIO_A	3	Analog input/output	Reference voltage input/output, channel A
REFIO_B	6	Analog input/output	Reference voltage input/output, channel B
SCLK	12	Digital input	Clock for serial communication
SDI	10	Digital input	Data input for serial communication
SDO_A	13	Digital output	Data output for serial communication, channel A and channel B
SDO_B	14	Digital output	Data output for serial communication, channel B

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to REFGND_x(2) or GND	–0.3	6	V
DVDD to GND	–0.3	6	V
Analog (AINP_x and AINM_x)(3) and reference input (REFIO_x) voltage with respect to REFGND_x	REFGND_x – 0.3	AVDD + 0.3	V
Digital input voltage with respect to GND	DVDD + 0.3	DVDD + 0.3	V
REFGND_x	GND – 0.3	GND + 0.3	V
Input current to any pin except supply pins	-10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) REFGND_x refers to REFGND_A and REFGND_B. REFIO_x refers to REFIO_A and REFIO_B.
(3) AINP_x refers AINP_A and AINP_B. AINM_x refers to AINM_A and AINM_B.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-001, level C4B	Corner pins (1,8,9 and 16)	±750	
			All other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		ADS8353-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	44.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage (AVDD to AGND)	V_{REF} range, internal reference	4.5	5	5.5	V
		V_{REF} range, external reference V_{EXT_REF} < 4.5 V	4.5	5	5.5	
		V_{REF} range, external reference V_{EXT_REF} > 4.5 V	V_{EXT_REF}	5	5.5	
		2x V_{REF} range, internal reference	5	5	5.5	
		2x V_{REF} range, external reference	2 x V_{EXT_REF}	5	5.5	
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS (Single-Ended Configuration)						
FSR	Full-scale input range (AINP_x to AINM_x)(1)	V_{REF} range, single-ended input, AINM_x = GND	0		V_{REF}	V
		2x V_{REF} range, single-ended input, AINM_x = GND	0		2 x V_{REF}	
V_{INP}	Absolute input voltage (AINP_x to REFGND_x)(2)	V_{REF} range	0		V_{REF}	V
		2x V_{REF} range, AVDD ≥ 2x V_{REF}	0		2 x V_{REF}	
V_{INM}	Absolute input voltage (AINM_x to REFGND_x)	V_{REF} range, single-ended input	–0.1		0.1	V
		2x V_{REF} range, single-ended input, AVDD ≥ 2 x V_{REF}	–0.1		0.1	
ANALOG INPUTS (Pseudo-Differential Configuration)						
FSR	Full-scale input range (AINP_x-AINM_x)	V_{REF} range, pseudo-differential input, AINM_x = V_{REF}/2	$-V_{REF\,/\,2}$		$V_{REF\,/\,2}$	V
		2x V_{REF} range, pseudo-differential input, AINM_x = V_{REF}, AVDD ≥ 2x V_{REF}	$-V_{REF}$		V_{REF}	
V_{INP}	Absolute input voltage (AINP_x to REFGND_x)	V_{REF} range	0		V_{REF}	V
	Absolute input voltage (AINP_x to REFGND_x)(2)	2x V_{REF} range, AVDD ≥ 2x V_{REF}	0		2 x V_{REF}	
V_{INM}	Absolute input voltage (AINM_x -REFGND_x)	V_{REF} range, pseudo-differential input	$V_{REF\,/\,2}$ –0.1		$V_{REF\,/\,2}$+0.1	V
	Absolute input voltage (AINM_x -REFGND_x)	2x V_{REF} range, single-ended input, AVDD ≥ 2x V_{REF}	V_{REF}–0.1		V_{REF}+0.1	
EXTERNAL REFERENCE INPUT						
V_{REFIO}	REFIO_x(3) input voltage	V_{REF} range	2.4	2.5	AVDD	V
		2x V_{REF} range	2.4	2.5	AVDD / 2	
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINP_x refers to analog input pins AINP_A and AINP_B. AINM_x refers to analog input pins AINM_A and AINM_B.
(2) REFGND_x refers to reference ground pins REFGND_A and REFGND_B.
(3) REFIO_x refers to voltage reference inputs REFIO_A and REFIO_B.

6.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, V_{REF_A} = V_{REF_B} = V_{REF} = 2.5 V (internal), and f_{DATA} = 600 kSPS (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_i	Input capacitance	In sample mode		40		pF
		In hold mode		4		
I_{lkg}	Input leakage current			0.1		µA
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
NMC	No missing codes			16		Bits
INL	Integral nonlinearity		–4	±1	4	LSB
DNL	Differential nonlinearity			±0.6		LSB
E_{IO}	Input offset error		–1	±0.5	1	mV
	E_{IO} match	ADC_A to ADC_B	–1	±0.5	1	mV
dE_{IO}/dT	Input offset thermal drift			1		µV/°C
E_G	Gain error	Referenced to the voltage at REFIO_x	–0.1	±0.05	0.1	%FS
	E_G match	ADC_A to ADC_B	–0.1	±0.05	0.1	%FS
dE_G/dT	Gain error thermal drift	Referenced to the voltage at REFIO_x		1		ppm/°C
AC ACCURACY						
SINAD	Signal-to-noise + distortion	V_{REF} = 2.5 V, V_{REF} input range	80.2	83		dB
		V_{REF} = 2.5 V, 2x V_{REF} input range		83.9		
		V_{REF} = 5 V, V_{REF} input range		88.7		
SNR	Signal-to-noise ratio	V_{REF} = 2.5 V, V_{REF} input range	80.5	83		dB
		V_{REF} = 2.5 V, 2x V_{REF} input range		84		
		V_{REF} = 5 V, V_{REF} input range		89		
THD	Total harmonic distortion	V_{REF} = 2.5 V, V_{REF} input range		–100		dB
		V_{REF} = 2.5 V, 2x V_{REF} input range		–100		
		V_{REF} = 5 V, V_{REF} input range		–100		
SFDR	Spurious-free dynamic range	V_{REF} = 2.5 V, V_{REF} input range		105		dB
		V_{REF} = 2.5 V, 2 x V_{REF} input range		105		
		V_{REF} = 5 V, V_{REF} input range		105		
INTERNAL VOLTAGE REFERENCE						
V_{REFOUT}	Reference output voltage	REFDAC_x = 1FFh (default) at 25°C	2.495	2.5	2.505	V
$V_{REF\text{-}match}$	VREF_A to VREF_B matching	REFDAC_x = 1FFh (default) at 25°C		±1		mV
REFDAC_x resolution[(1)]				1.1		mV
dV_{REFOUT}/dT	Reference voltage temperature drift	REFDAC_x = 1FFh (default) at 25°C		±10		ppm/°C
dV_{REFOUT}/dt	Long-term stability	1000 hours		150		ppm
R_O	Internal reference output impedance			1		Ω
I_{REFOUT}	Reference output dc current			2		mA
C_{REFOUT}	Reference output capacitor			10		µF
t_{REFON}	Reference output settling time			8		ms
VOLTAGE REFERENCE INPUT						
I_{REF}	Average reference input current	Per ADC		300		µA

6.5 Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, $V_{REF\_A} = V_{REF\_B} = V_{REF}$ = 2.5 V (internal), and f_{DATA} = 600 kSPS (unless otherwise noted); minimum and maximum values at T_A = –40°C to 125°C; typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{REF}	External ceramic reference capacitor			10		µF
$I_{lkg(dc)}$	DC leakage current			±0.1		µA
SAMPLING DYNAMICS						
t_A	Aperture delay			8		ns
	t_A match	ADC_A to ADC_B		40		ps
t_{AJIT}	Aperture jitter			50		ps
DIGITAL INPUTS						
V_{IH}	High-level input voltage	DVDD > 2.3 V	0.7 DVDD		DVDD + 0.3	V
		DVDD ≤ 2.3 V	0.8 DVDD		DVDD + 0.3	
V_{IL}	Low-level input voltage	DVDD > 2.3 V	–0.3		0.3 DVDD	V
		DVDD ≤ 2.3 V	–0.3		0.2 DVDD	
	Input current			±10		nA
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = 500-µA source	0.8 DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 500-µA sink	0		0.2 DVDD	V
POWER SUPPLY						
AIDD	Analog supply current	AVDD = 5 V, fastest throughput internal reference		8.5	10	mA
		AVDD = 5 V, fastest throughput external reference(2)		7.5	3.6	
		AVDD = 5V, no conversion internal reference		5.5	7	
		AVDD = 5 V, no conversion external reference(2)		4.5		
		AVDD = 5 V, STANDBY mode internal reference		2.5		
		AVDD = 5 V, STANDBY mode external reference(2)		1		
		Power-down mode		10	50	µA
DIDD	Digital supply current	DVDD = 3.3 V, C_{load} = 10 pF, fastest throughput		0.5		mA
		DVDD = 5 V, C_{load} = 10 pF, fastest throughput		1		
P_D	Power dissipation (normal operation)	AVDD = 5 V, fastest throughput, internal reference		42.5	50	mW

(1) Refer to the Reference section for more details.
(2) With internal reference powered down, CFR.B6 = 0.

6.6 Timing Requirements

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{PH_CK}	CLOCK high time		0.4		0.6	t_{CLK}
t_{PL_CK}	CLOCK low time		0.4		0.6	t_{CLK}
f_{CLK}	CLOCK frequency				20	MHz
t_{ACQ}	Acquisition time	32-clock, dual SDO mode			33 x t_{CLK} - t_{CONV}	ns
		32-clock, single SDO mode			49 x t_{CLK} - t_{CONV}	
t_{CONV}	Conversion time				730	ns
t_{PH_CS}	$\overline{CS}$ high time		40			ns
$t_{PH\_CS\_SHRT}$	$\overline{CS}$ high time after frame abort		150			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling edge to SCLK falling edge		15			ns
t_{D_CKCS}	Delay time: Last SCLK falling edge to $\overline{CS}$ rising edge		15			ns
t_{SU_CKDI}	Setup time: DIN data valid to SCLK falling edge		5			ns
t_{HT_CKDI}	Hold time: SCLK falling edge to (previous) data valid on DIN		5			ns
t_{PU_STDBY}	Power-up time from STANDBY mode		1			µs
t_{PU_SPD}	Power-up time from SPD mode	With internal reference	3			ms
		With external reference	1			

6.7 Switching Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{THROUGHPUT}$	Throughput time		1.666			µs
$f_{THROUGHPUT}$	Throughput				600	kSPS
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling edge to data enable				12	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising edge to data going to 3-state				12	ns
t_{D_CKDO}	Delay time: SCLK falling edge to next data valid				20	ns

6.8 Timing Diagram

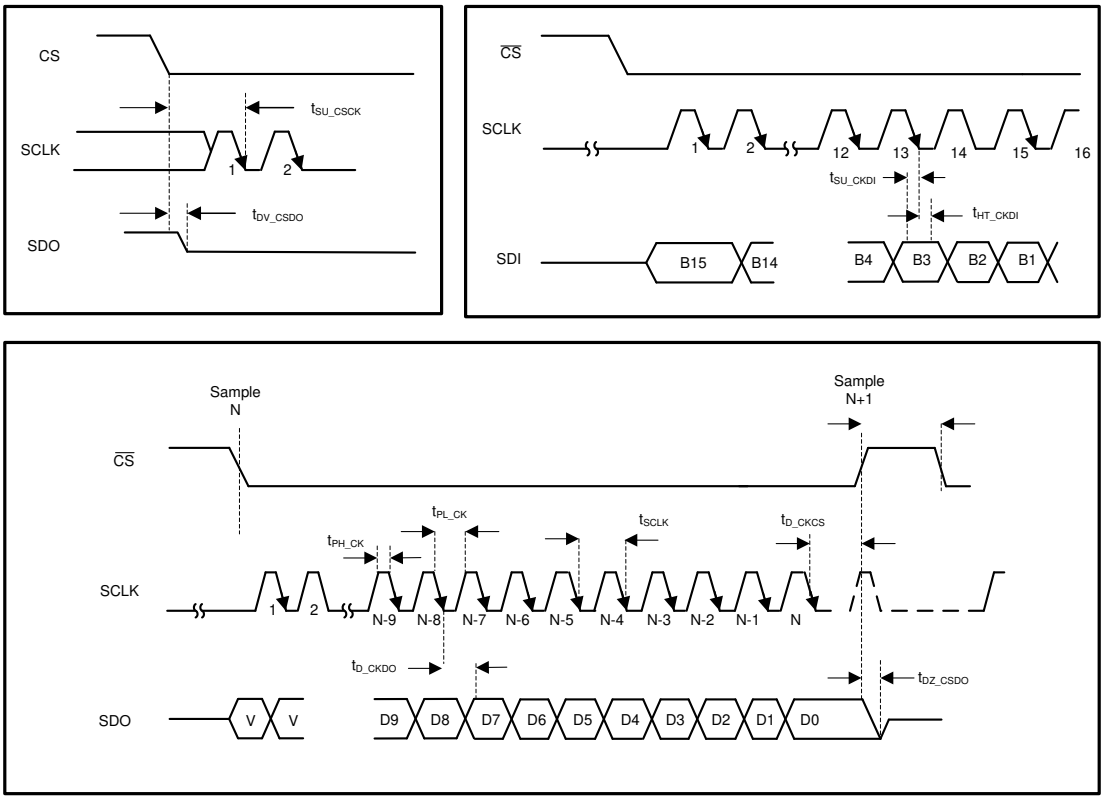
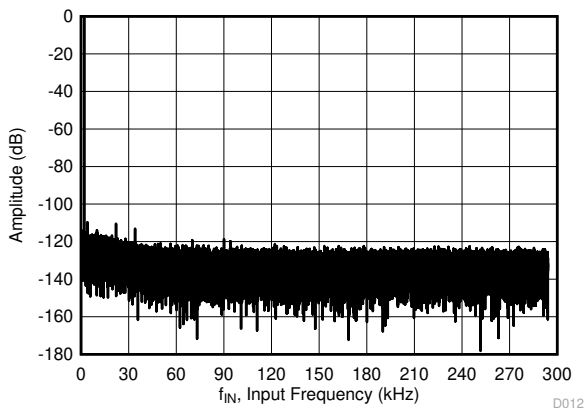


図 6-1. Serial Interface Timing Diagram

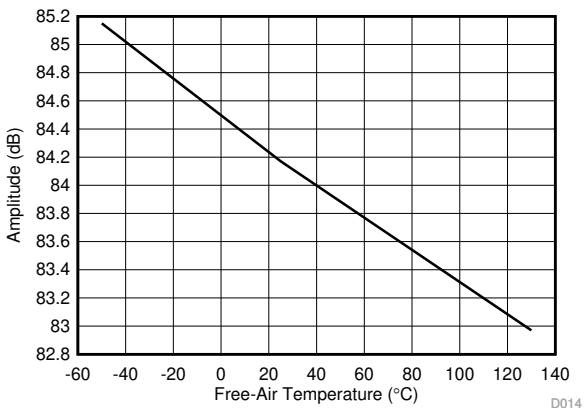
6.9 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 600 kSPS (unless otherwise noted)



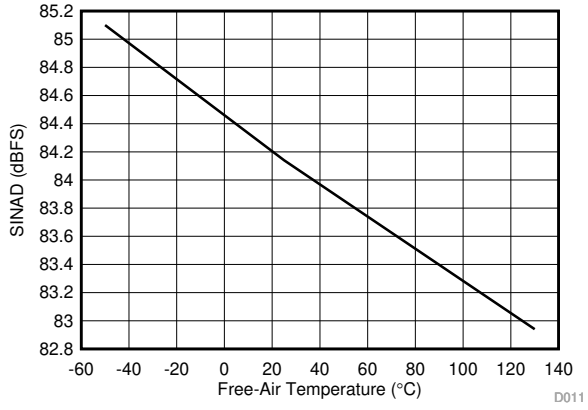
f_{IN} = 2 kHz, SNR = 84.6 dB, THD = –107.6 dB

図 6-2. Typical FFT



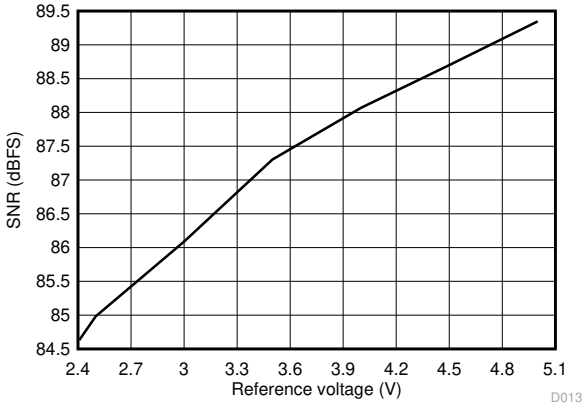
f_{IN} = 2 kHz

図 6-3. SNR vs Temperature



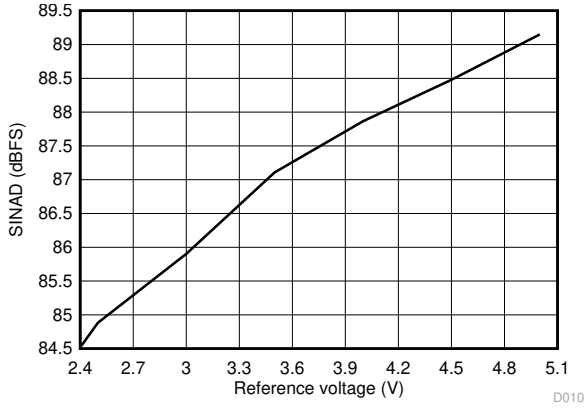
f_{IN} = 2 kHz

図 6-4. SINAD vs Temperature



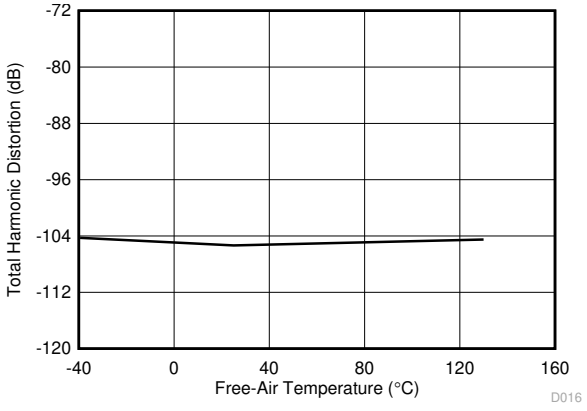
f_{IN} = 2 kHz

図 6-5. SNR vs Reference Voltage



f_{IN} = 2 kHz

図 6-6. SINAD vs Reference Voltage

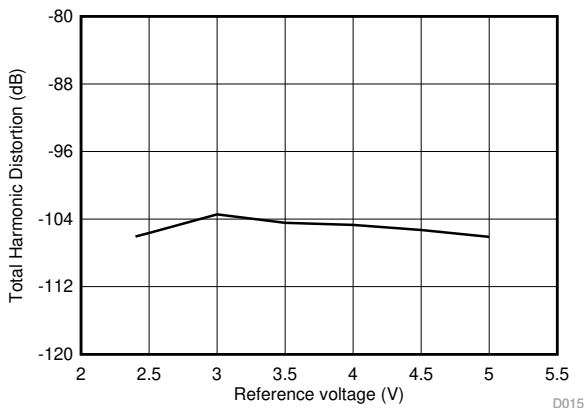


f_{IN} = 2 kHz

図 6-7. THD vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 600 kSPS (unless otherwise noted)



f_{IN} = 2 kHz

図 6-8. THD vs Reference Voltage

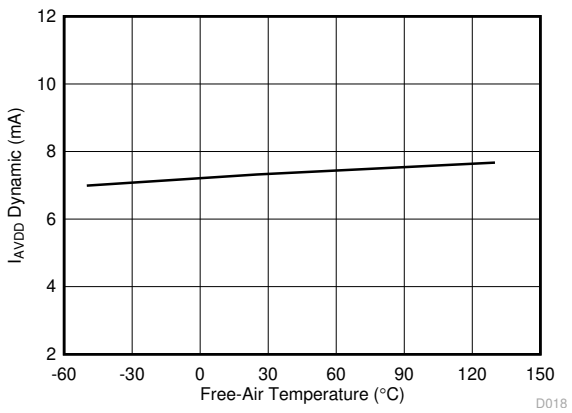


図 6-9. Analog Supply Current vs Temperature

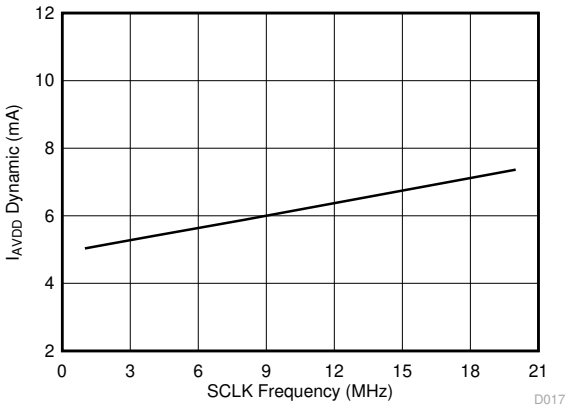
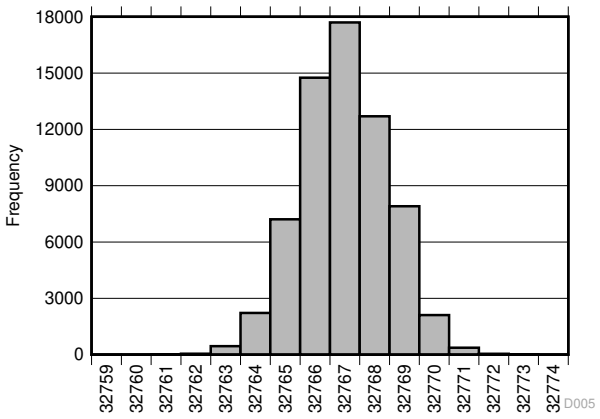


図 6-10. Analog Supply Current vs SCLK Frequency



65536 data points, $V_{IN-DIFF}$ = 0 V

図 6-11. DC Histogram

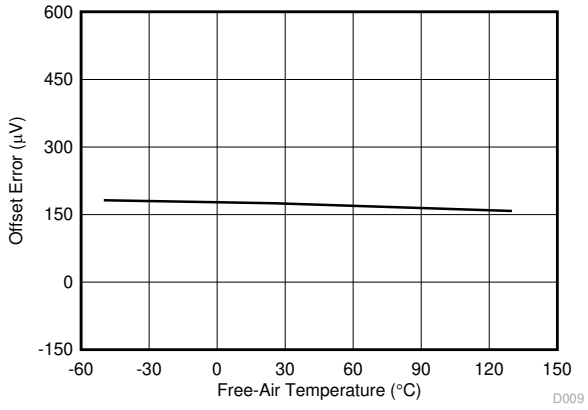


図 6-12. Offset Error vs Temperature

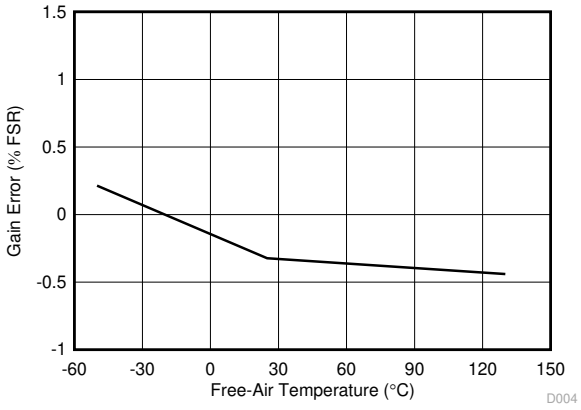


図 6-13. Gain Error vs Temperature

6.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V (internal), and f_{DATA} = 600 kSPS (unless otherwise noted)

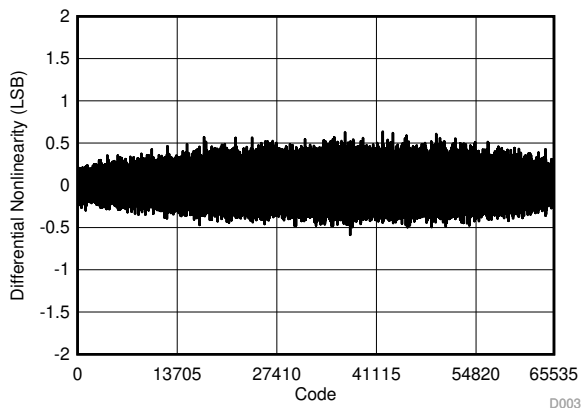


図 6-14. Typical DNL

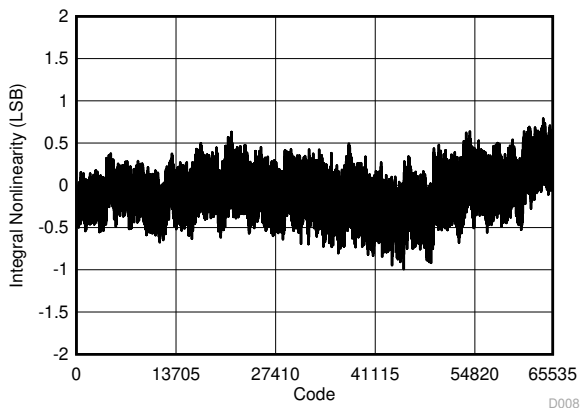


図 6-15. Typical INL

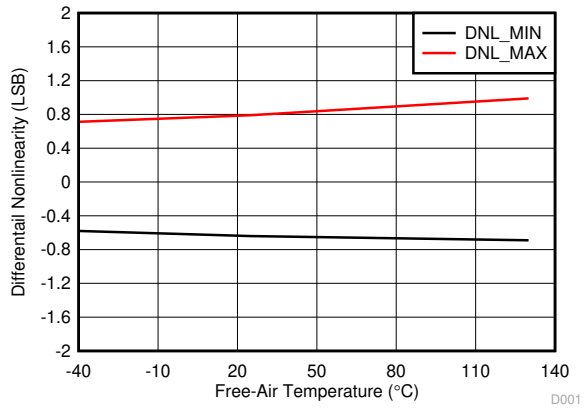


図 6-16. DNL vs Temperature

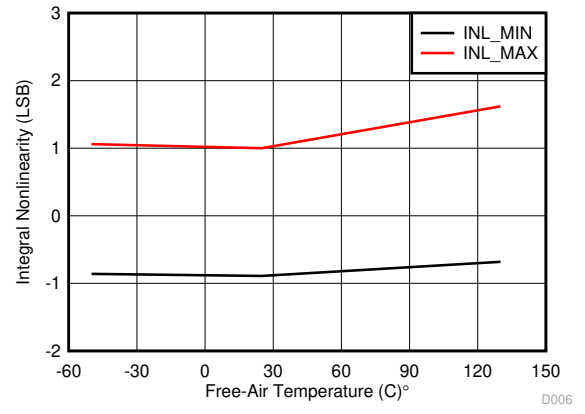


図 6-17. INL vs Temperature

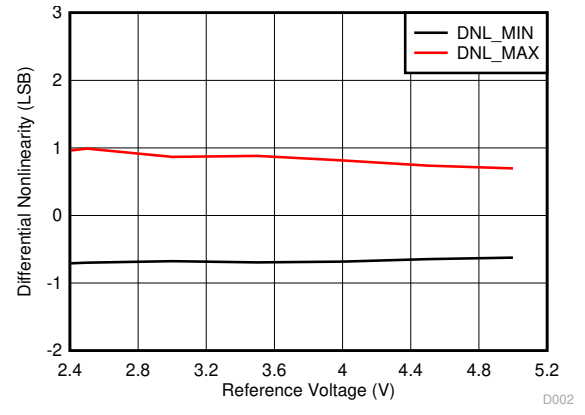


図 6-18. DNL vs Reference Voltage

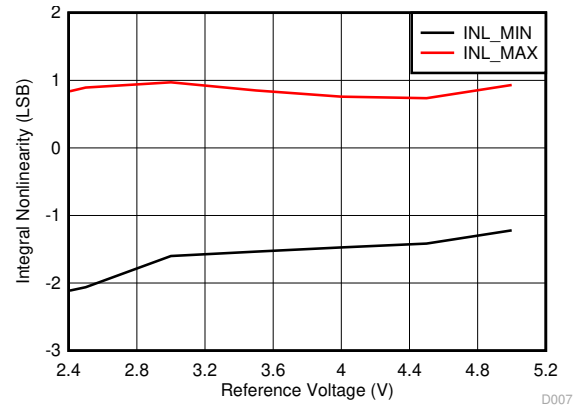


図 6-19. INL vs Reference Voltage

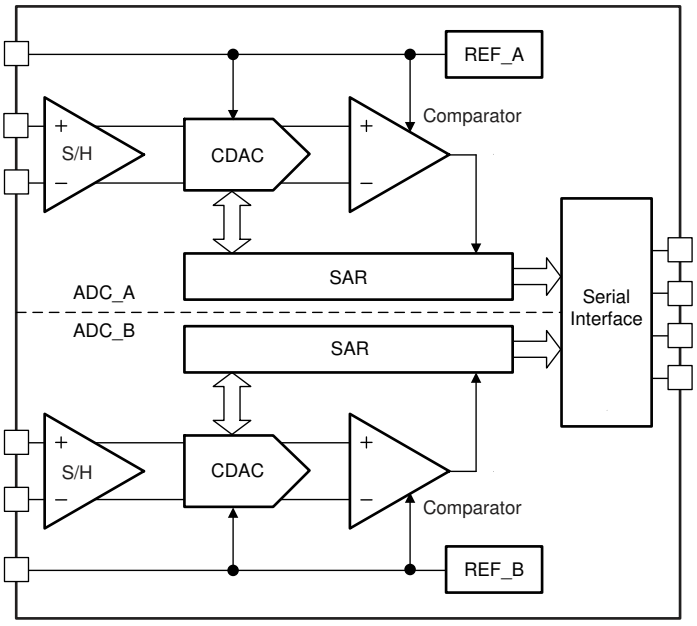
7 Detailed Description

7.1 Overview

The ADS8353-Q1 is a 16-bit, dual-channel, high-speed, simultaneous-sampling, analog-to-digital converter (ADC). The ADS8353-Q1 supports single-ended and pseudo-differential input signals. The device provides a simple, serial interface to the host controller and operates over a wide range of analog and digital power supplies.

The device has two independently programmable internal references to achieve system-level gain error correction. The *Functional Block Diagram* section provides a functional block diagram of the device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

The device has two simultaneous sampling ADCs (ADC_A and ADC_B). ADC_A and ADC_B operate with reference voltages present on the REFIO_A and REFIO_B pins, respectively. Decouple the REFIO_A and REFIO_B pins with the REFGND_A and REFGND_B pins, respectively, with 10-µF decoupling capacitors.

図 7-1 shows that the device supports operation either with an internal or external reference source. The reference voltage source is determined by setting bit 6 of the configuration register (CFR.B6). This bit is common to ADC_A and ADC_B.

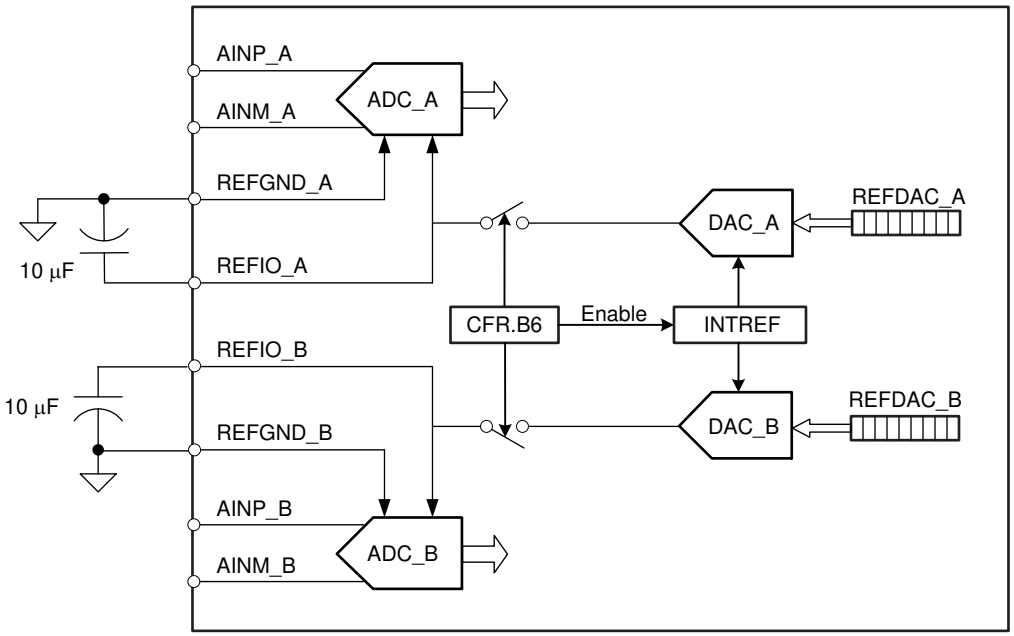


図 7-1. Reference Configurations and Connections

When CFR.B6 is 0, the device shuts down the internal reference source (INTREF) and ADC_A and ADC_B operate on external reference voltages provided by the user on the REFIO_A and REFIO_B pins, respectively.

When CFR.B6 is 1, the device operates with the internal reference source (INTREF) connected to REFIO_A and REFIO_B via DAC_A and DAC_B, respectively. In this configuration, V_{REF_A} and V_{REF_B} can be changed independently by writing to the respective user-programmable registers, REFDAC_A and REFDAC_B, respectively. See the *Register Maps* section for more details.

7.3.2 Analog Inputs

The ADS8353-Q1 supports single-ended or pseudo-differential analog inputs on both ADC channels. These inputs are sampled and converted simultaneously by the two ADCs, ADC_A and ADC_B. ADC_A samples and converts ($V_{AINP\_A} – V_{AINM\_A}$), and ADC_B samples and converts ($V_{AINP\_B} – V_{AINM\_B}$).

図 7-2a and 図 7-2b show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively. Series resistance, R_S, represents the on-state sampling switch resistance (typically 50 Ω) and C_{SAMPLE} is the device sampling capacitor (typically 40 pF).

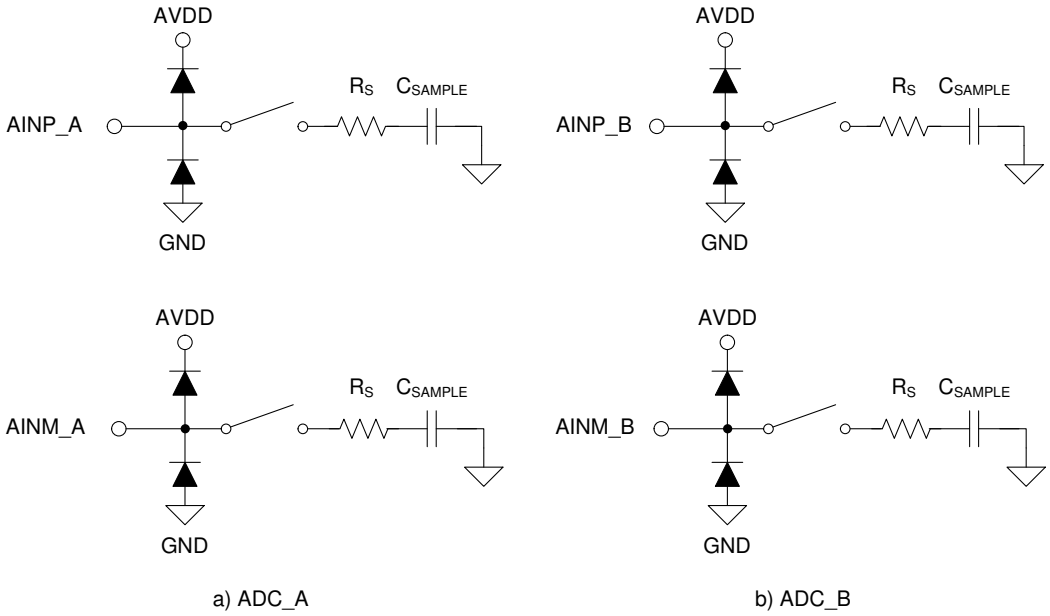


図 7-2. Equivalent Circuit for the Analog Input Pins

7.3.2.1 Analog Input: Full-Scale Range Selection

The full-scale range (FSR) supported at the analog inputs of the device is programmable with bit B9 of the configuration register (CFR.B9). This bit is common for both ADCs (ADC_A and ADC_B). 式 1 and 式 2 give the FSR:

For CFR.B9 = 0, FSR_ADC_A = 0 to V_{REF_A} and FSR_ADC_B = 0 to V_{REF_B} (1)

For CFR.B9 = 1, FSR_ADC_A = 0 to 2 × V_{REF_A} and FSR_ADC_B = 0 to 2 × V_{REF_B} (2)

where:

- V_{REF_A} and V_{REF_B} are the reference voltages going to ADC_A and ADC_B, respectively (as described in the *Reference* section).

Therefore, with appropriate settings of the REFDAC_A and REFDAC_B registers, CFR.B7, and CFR.B9, the maximum dynamic range of the ADC can be used.

Make sure that the ADC analog supply (AVDD) is as in 式 3 and 式 4 when CFR.B9 is set to 1:

$2 \times V_{REF\_A} \le AVDD \le AVDD(max)$ (3)

$2 \times V_{REF\_B} \le AVDD \le AVDD(max)$ (4)

7.3.2.2 Analog Input: Single-Ended and Pseudo-Differential Configurations

The ADS8353-Q1 can support single-ended or pseudo-differential input configurations.

For supporting single-ended inputs, B7 in the configuration register (CFR.B7) must be set to 0 (CFR.B7 = 0) and AINM_A and AINM_B must be externally connected to GND.

For supporting pseudo-differential inputs, CFR.B7 must be set to 1 (CFR.B7 = 1) and AINM_A and AINM_B must be externally connected to FSR_ADC_A / 2 and FSR_ADC_B / 2, respectively. CFR.B7 is common to both ADCs.

The CFR.B9 and CFR.B7 settings can be combined as shown in 表 7-1 to select the desired input configuration.

表 7-1. Input Configurations

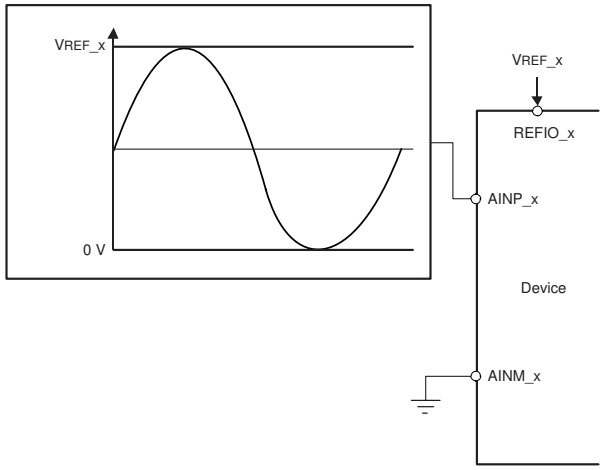
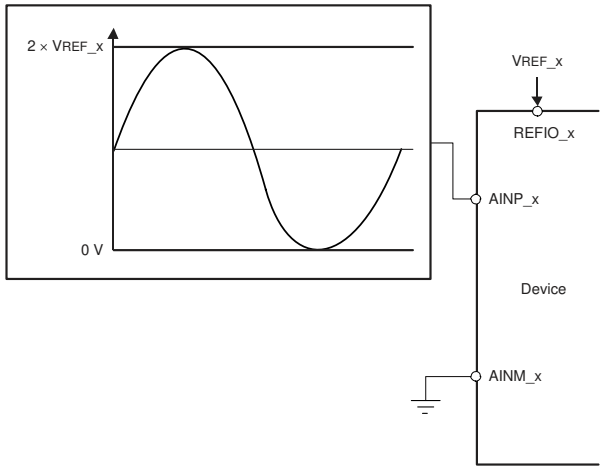
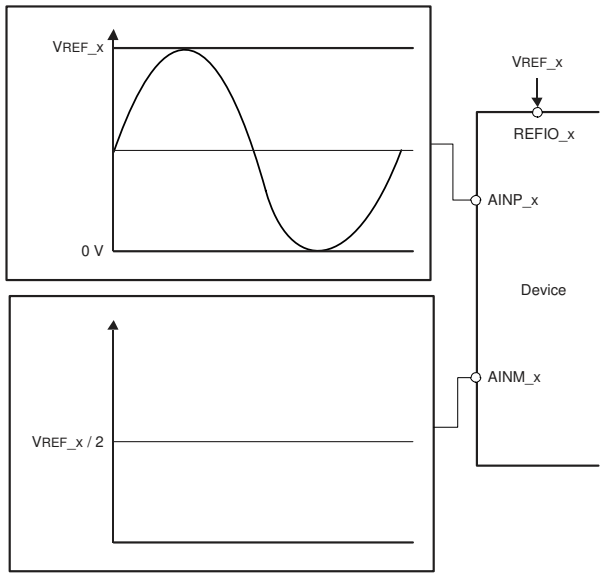
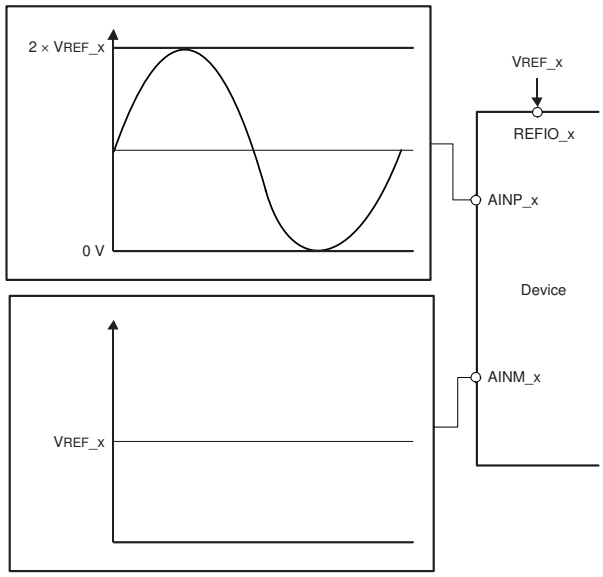
INPUT RANGE SELECTION	AINM SELECTION	CONNECTION DIAGRAM
CFR.B9 = 0 (FSR_ADC_A = 0 to V_{REF_A}) (FSR_ADC_B = 0 to V_{REF_B})	CFR.B7 = 0 (AINM_A = GND) (AINM_B = GND)	
CFR.B9 = 1 (FSR_ADC_A = 0 to 2 x V_{REF_A}) (FSR_ADC_B = 0 to 2 x V_{REF_B})	CFR.B7 = 0 (AINM_A = GND) (AINM_B = GND)	

表 7-1. Input Configurations (continued)

INPUT RANGE SELECTION	AINM SELECTION	CONNECTION DIAGRAM
CFR.B9 = 0 (FSR_ADC_A = V_{REF_A}) (FSR_ADC_B = V_{REF_B})	CFR.B7 = 1 (AINM_A = V_{REF_A}/2) (AINM_B = V_{REF_B}/2)	
CFR.B9 = 1 (FSR_ADC_A = 2 x V_{REF_A}) (FSR_ADC_B = 2 x V_{REF_B})	CFR.B7 = 1 (AINM_A = V_{REF_A}) (AINM_B = V_{REF_B})	

7.3.3 Transfer Function

The device supports two input configurations:

1. Single-ended inputs, CFR.B7 = 0 (default), or
2. Pseudo-differential inputs, CFR.B7 = 1

The device also supports two output data formats:

1. Straight binary output, CFR.B4 = 0 (default), or
2. Two's compliment output, CFR.B4 = 1

式 5 calculates the device resolution:

$$1\ LSB = (FSR\_ADC\_x) / (2^N) \quad (5)$$

where:

- N = 16
- FSR_ADC_x = the full-scale input range of the ADC (see the *Analog Inputs* section for more details)

表 7-2 and 表 7-3 show the different input voltages and the corresponding output codes from the device.

表 7-2. Transfer Characteristics for Straight Binary Output (CFR.B4 = 0, Default)

INPUT CONFIGURATION	INPUT VOLTAGE			OUTPUT CODE (Hex)	
				STRAIGHT BINARY (CFR.B4 = 0, Default)	
	AINP_x	AINM_x	AINP_x - AINM_x	CODE	ADS8353-Q1
Single-ended (CFR.B7 = 0, default)	≤ 1 LSB	0	≤ 1 LSB	ZC	0000
	FSR_ADC_x / 2		FSR_ADC_x / 2	MC	7FFF
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x – 1 LSB	FSC	FFFF
Pseudo-differential (CFR.B7 = 1)	≤ 1 LSB	FSR_ADC_x / 2	≤ –FSR_ADC_x / 2 + 1 LSB	ZC	0000
	FSR_ADC_x / 2		0	MC	7FFF
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x / 2 – 1 LSB	FSC	FFFF

表 7-3. Transfer Characteristics for Two's Compliment Output (CFR.B4 = 1)

INPUT CONFIGURATION	INPUT VOLTAGE			OUTPUT CODE (Hex)	
				TWO'S COMPLIMENT (CFR.B4 = 1, Default)	
	AINP_x	AINM_x	AINP_x - AINM_x	CODE	ADS8353-Q1
Single-ended (CFR.B7 = 0, default)	≤ 1 LSB	0	≤ 1 LSB	NFSC	8000
	FSR_ADC_x / 2		FSR_ADC_x / 2	MC	0000
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x – 1 LSB	PFSC	7FFF
Pseudo-differential (CFR.B7 = 1)	≤ 1 LSB	FSR_ADC_x / 2	≤ –FSR_ADC_x / 2 + 1 LSB	NFSC	8000
	FSR_ADC_x / 2		0	MC	0000
	≥ FSR_ADC_x – 1 LSB		≥ FSR_ADC_x / 2 – 1 LSB	PFSC	7FFF

図 7-3 shows the ideal device transfer characteristics for the single-ended analog input.

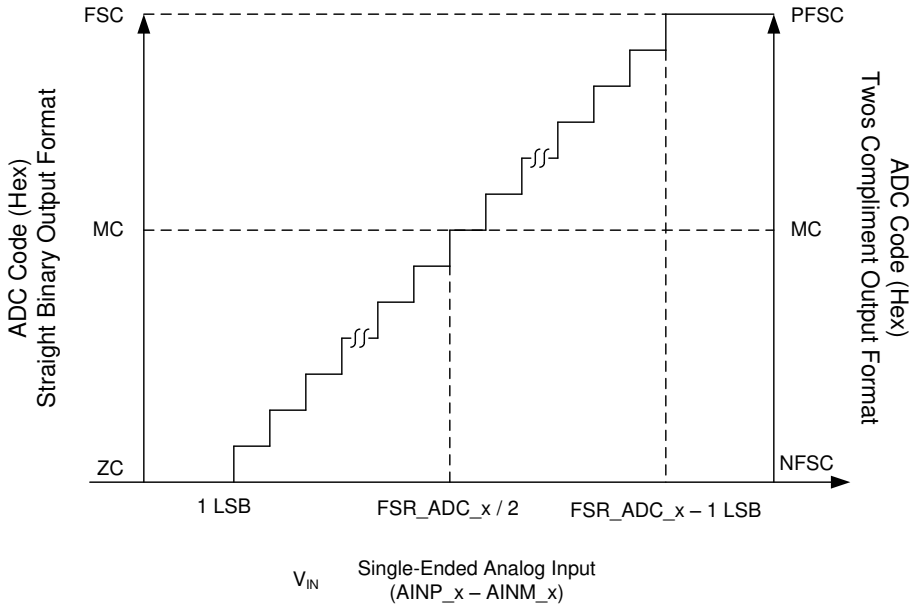


図 7-3. Ideal Transfer Characteristics for a Single-Ended Analog Input

図 7-4 shows the ideal device transfer characteristics for the pseudo-differential analog input.

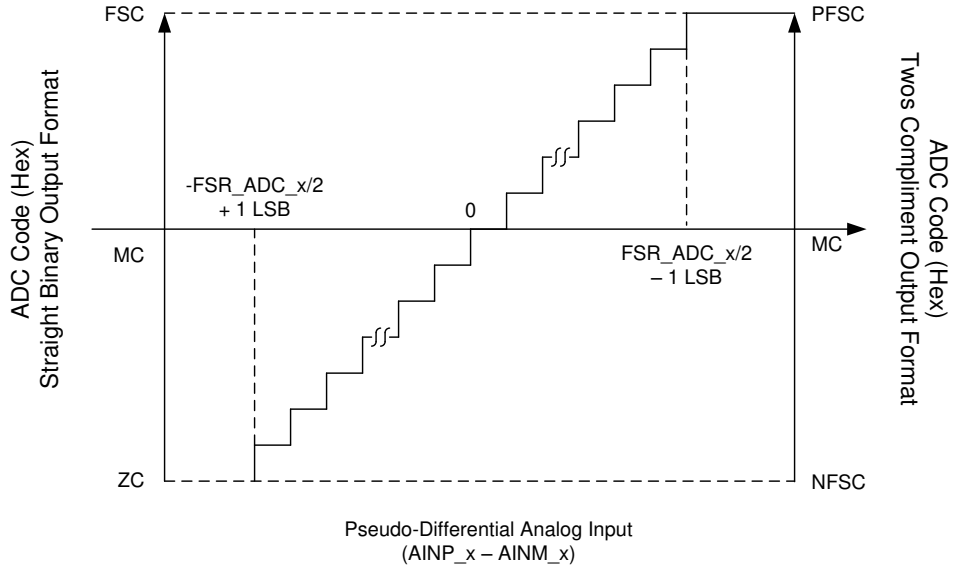


図 7-4. Ideal Transfer Characteristics for a Pseudo-Differential Analog Input

7.4 Device Functional Modes

The device provides three user-programmable registers: the configuration register (CFR), the REFDAC_A register, and the REFDAC_B register. These registers support write (see the *Write to User-Programmable Registers* section) and readback (see the *Reading User-Programmable Registers* section) operations and allow the ADC behavior to be customized for specific application requirements.

The device supports two interface modes (see the *Conversion Data Read* section), two low-power modes (see the *Low-Power Modes* section), and a short-cycling or reconversion feature (see the *Frame Abort, Reconversion, or Short-Cycling* section).

7.5 Programming

7.5.1 Serial Interface

The device uses the serial clock (SCLK) for synchronizing data transfers in and out of the device.

The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. Between the start and end of the frame, a minimum of *N* SCLK falling edges must be provided to validate the read or write operation. As shown in 表 7-4, *N* depends upon the interface mode used to read the conversion result. When *N* SCLK falling edges are provided, the write operation attempted in the frame is validated and the internal user-programmable registers are updated on the subsequent $\overline{CS}$ rising edge. This $\overline{CS}$ rising edge also ends the frame.

表 7-4. SCLK Falling Edges for a Valid Write Operation

INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION *N*
32-CLK, dual-SDO mode (default); see the *32-CLK, Dual-SDO Mode (CFR.B11 = 0, CFR.B10 = 0, Default)* section	32
32-CLK, single-SDO mode; see the *32-CLK, Single-SDO Mode (CFR.B11 = 0, CFR.B10 = 1)* section	48

If $\overline{CS}$ is brought high before providing *N* SCLK falling edges, the write operation attempted in the frame is not valid. See the *Frame Abort, Reconversion, or Short-Cycling* section for more details.

7.5.2 Write to User-Programmable Registers

The device features three user-programmable registers: the configuration register (CFR), the REFDAC_A register, and the REFDAC_B register. These registers can be written with the device SDI pin. The first 16 bits of data on SDI are latched into the device on the first 16 SCLK falling edges. However, the new configuration takes effect only when the read or write operation is validated. If these registers are not required to update, SDI must remain low during the respective frames.

The first four SDI data bits (B[15:12]) determine what operation is performed (that is, either a read or write operation or no operation), which register address the operation uses, and the function of the next 12 SDI data bits (B[11:0]). 表 7-5 lists the various combinations supported for B[15:12].

表 7-5. Data Write Operation

B15	B14	B13	B12	OPERATION	FUNCTION OF BITS B[11:0]
0	0	0	0	No operation is performed	These bits are ignored
0	0	0	1	REFDAC_A read	000h; see the *Reading User-Programmable Registers* section
0	0	1	0	REFDAC_B read	000h; see the *Reading User-Programmable Registers* section
0	0	1	1	CFR read	000h; see the *Reading User-Programmable Registers* section
1	0	0	0	CFR write	See the CFR register
1	0	0	1	REFDAC_A write	See the REFDAC register
1	0	1	0	REFDAC_B write	See the REFDAC register
1	0	1	1	No operation is performed	These bits are ignored

表 7-5. Data Write Operation (continued)

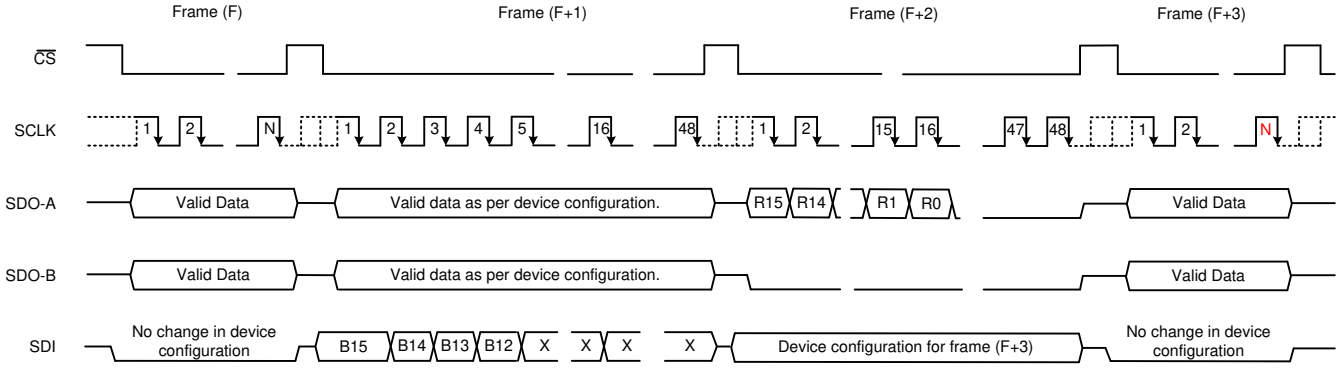
B15	B14	B13	B12	OPERATION	FUNCTION OF BITS B[11:0]
X	1	X	X	No operation is performed	These bits are ignored

7.5.3 Data Read Operation

The device supports two types of read operations: reading user-programmable registers and reading conversion results.

7.5.3.1 Reading User-Programmable Registers

The device supports a readback option for all user-programmable registers: CFR, REFDAC_A, and REFDAC_B. 図 7-5 shows a detailed timing diagram for this operation.



N is a function of the device configuration, as described in 表 7-4.

図 7-5. Register Readback Timing

To readback the user-programmable register settings, transmit the appropriate control word, as shown in 表 7-6, to the device during frame (F+1). Frame (F+1) must have at least 48 SCLK falling edges.

表 7-6. Control Word to Readback User-Programmable Registers

USER-PROGRAMMABLE REGISTER	CONTROL WORD TO BE PROGRAMMED IN FRAME (F+1)	
	B[15:12] (Binary)	B[11:0] (Hex)
CFR	0011b	000h
REFDAC_A	0001b	000h
REFDAC_B	0010b	000h

Frame (F+2) must have at least 48 SCLK falling edges. During frame (F+2), SDO_A outputs the contents of the selected user-programmable register on the first 16 SCLK falling edges (as shown in 表 7-7) and then outputs 0's for any subsequent SCLK falling edges. The SDO_B pin outputs 0's for all SCLK falling edges.

表 7-7. Register Data Read Back

USER-PROGRAMMABLE REGISTER	DATA READ ON SDO-A IN FRAME (F+2)									
	R15	R14	R13	R12	R11	—	R3	R2	R1	R0
CFR	0	0	1	1	CFG.B11	—	CFG.B3	CFG.B2	CFG.B1	CFG.B0
REFDAC_A	0	0	0	1	REFDAC_A.D8	—	REFDAC_A.D0	0	0	0
REFDAC_B	0	0	1	0	REFDAC_B.D8	—	REFDAC_B.D0	0	0	0

Register settings programmed during frame (F+2) determine the device configuration in frame (F+3).

7.5.3.2 Conversion Data Read

The device provides two different interface modes for reading the conversion result. These modes offer flexible hardware connections and firmware programming. 表 7-8 shows how to select one of the two interface modes.

表 7-8. Interface Mode Selection

CFR.B11	CFR.B10	INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION *N*
0	0	32-CLK, dual-SDO mode (default)	32
0	1	32-CLK, single-SDO mode	48

In the 32-CLK interface modes, the device uses an internal clock to convert the sampled analog signal. The conversion is completed during the first 16 periods of SCLK and the conversion result can be read on the subsequent SCLK falling edges.

The following sections detail the various interface modes supported by the device.

7.5.3.2.1 32-CLK, Dual-SDO Mode (CFR.B11 = 0, CFR.B10 = 0, Default)

The 32-CLK, dual-SDO mode is the default mode supported by the device. This mode can also be selected by writing CFR.B11 = 0 and CFR.B10 = 0.

In this mode, the SDO_A pin outputs the ADC_A conversion result and the SDO_B pin outputs the ADC_B conversion result. 図 7-6 shows a detailed timing diagram for this mode.

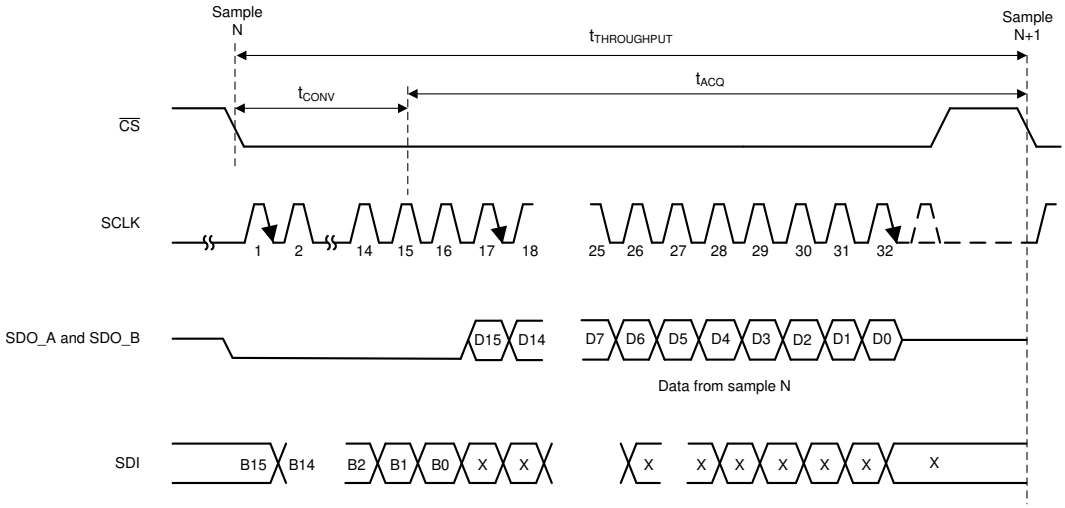


図 7-6. 32-CLK, Dual-SDO Mode Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A and SDO_B pins. The device converts the sampled analog input during the conversion time (t_{CONV}). SDO_A and SDO_B read 0 during this period. After completing the conversion process, the sample-and-hold circuit returns to sample mode. The device outputs the MSBs of ADC_A and ADC_B on the SDO_A and SDO_B pins, respectively, on the 16th SCLK falling edge. As shown in 表 7-9, the subsequent SCLK falling edges are used to shift out the rest of the bits of the conversion result.

表 7-9. Data Launch Edge

DEVICE	PINS	LAUNCH EDGE												
		$\overline{CS}$	SCLK											$\overline{CS}$
		↓	↓1	—	↓15	↓16	—	↓27	↓28	↓29	↓30	↓31	↓32 ...	↑
ADS8353-Q1	SDO-A	0	0	—	0	D15_A	—	D4_A	D3_A	D2_A	D1_A	D0_A	0 ...	Hi-Z
	SDO-B	0	0	—	0	D15_B	—	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z

In this mode, at least 32 SCLK falling edges must be given to validate the read or write frame. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

See the *Timing Requirements* table for timing specifications specific to this serial interface mode.

7.5.3.2.2 32-CLK, Single-SDO Mode (CFR.B11 = 0, CFR.B10 = 1)

The 32-CLK, single-SDO mode provides the option of using only one SDO pin (SDO_A) to read conversion results from both ADCs (ADC_A and ADC_B). SDO_B remains in 3-state and can be treated as a no connect (NC) pin.

This mode can be selected by writing CFR.B11 = 0 and CFR.B10 = 1. 図 7-7 shows a detailed timing diagram for this mode.

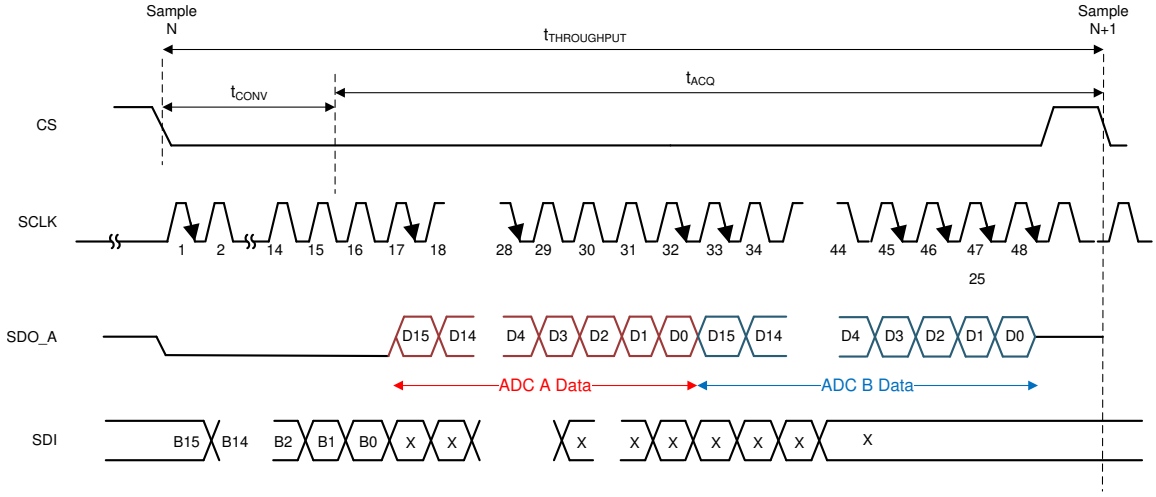


図 7-7. 32-CLK, Single-SDO Mode Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A pin. The device converts the sampled analog input during the conversion time (t_{CONV}). SDO_A reads 0 during this period. After competing the conversion process, the sample-and-hold circuit goes back into sample mode. The device outputs the MSB of ADC_A on the SDO_A pin on the 16th SCLK falling edge. As shown in 表 7-10, the subsequent SCLK falling edges are used to shift out the conversion result of ADC_A followed by the conversion result of ADC_B on the SDO_A pin.

表 7-10. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE																			
		$\overline{CS}$	SCLK																		$\overline{CS}$
		↓	↓1	—	↓15	↓16	—	↓27	↓28	↓29	↓30	↓31	↓32	—	↓43	↓44	↓45	↓46	↓47	↓ 48 ...	↑
ADS8353-Q1	SDO-A	0	0	—	0	D15_A	—	D4_A	D3_A	D2_A	D1_A	D0_A	D15_B	—	D4_B	D3_B	D2_B	D1_B	D0_B	0 ...	Hi-Z

In this mode, at least 48 SCLK falling edges must be given to validate the read or write frame. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

See the *Timing Requirements* table for timing specifications specific to this serial interface mode.

7.5.4 Low-Power Modes

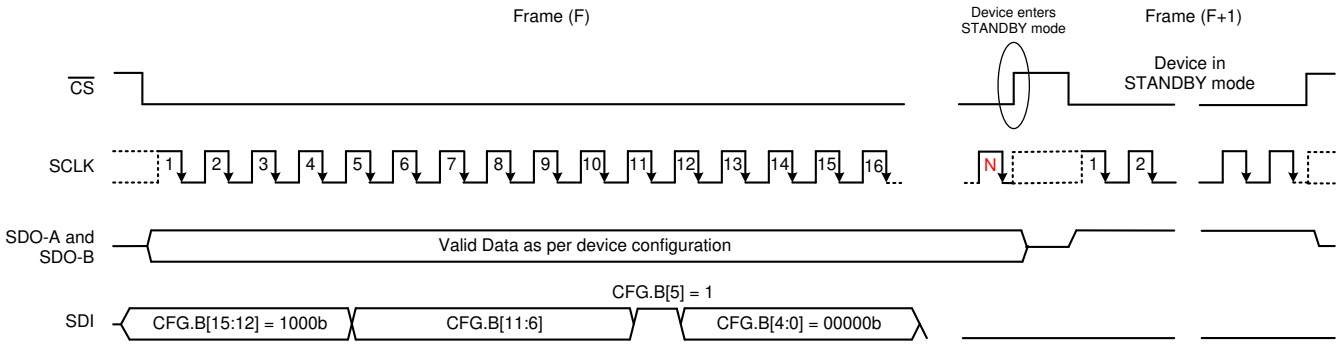
In normal mode of operation, all internal circuits of the device are always powered up and the device is always ready to commence a new conversion. This mode enables the device to support the rated throughput. The device also supports two low-power modes to optimize the power consumption at lower throughputs: STANDBY mode and software power-down (SPD) mode.

7.5.4.1 STANDBY Mode

The device supports a STANDBY mode of operation where some of the internal circuits of the device are powered down. However, if bit 6 in configuration register is set to 1 (CFR.B6 = 1), then the internal reference is not powered down and the contents of the REFDAC_A and REFDAC_B registers are retained to enable faster power-up to a normal mode of operation.

As shown in 図 7-8, a valid write operation in frame (F) programs the configuration register with B5 set to 1 (CFR.B5 = 1) and places the device into a STANDBY mode of operation on the following $\overline{CS}$ rising edge. While in STANDBY mode, SDO_A and SDO_B output all 1s when $\overline{CS}$ is low and remain in 3-state when $\overline{CS}$ is high.

To remain in STANDBY mode, SDI must remain low in the subsequent frames.

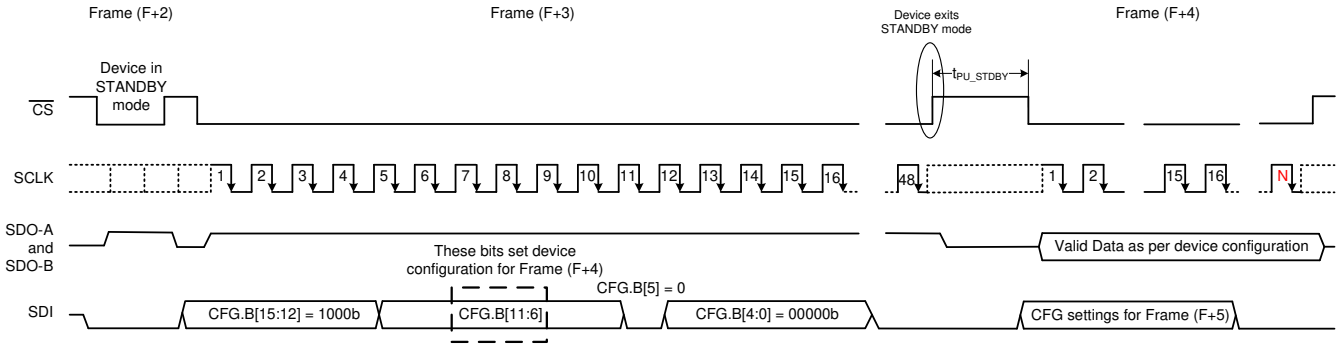


N is a function of the device configuration, as described in 表 7-4.

図 7-8. Enter STANDBY Mode

As shown in 図 7-9, a valid write operation in frame (F+3) writes the configuration register with B5 set to 0 (CFR.B5 = 0) and brings the device out of STANDBY mode on the following $\overline{CS}$ rising edge. Frame (F+3) must have at least 48 SCLK falling edges.

After exiting the STANDBY mode, a delay of t_{PU_STDBY} must elapse for the internal circuits to fully power-up and resume normal operation in frame (F+4). Device configuration for frame (F+4) is determined by the status of the CFR.B[11:6] bits programmed during frame (F+3).



N is a function of the device configuration, as described in 表 7-4.

図 7-9. Exit STANDBY Mode

See the *Timing Requirements* table for timing specifications for this operating mode.

7.5.4.2 Software Power-Down (SPD) Mode

In software power-down (SPD) mode, all internal circuits (including the internal references) are powered down. However, the contents of the REFDAC_A and REFDAC_B registers are retained.

As shown in 図 7-10, to enter SPD mode, the device must be selected (by bringing $\overline{CS}$ low) and SDI must be kept high for a minimum of 48 SCLK cycles during frame (F). The device goes to SPD on the $\overline{CS}$ rising edge following frame (F). While in SPD mode, SDO_A and SDO_B go to 3-state irrespective of the status of the $\overline{CS}$ signal.

To remain in SPD mode, SDI must remain high in all subsequent frames.

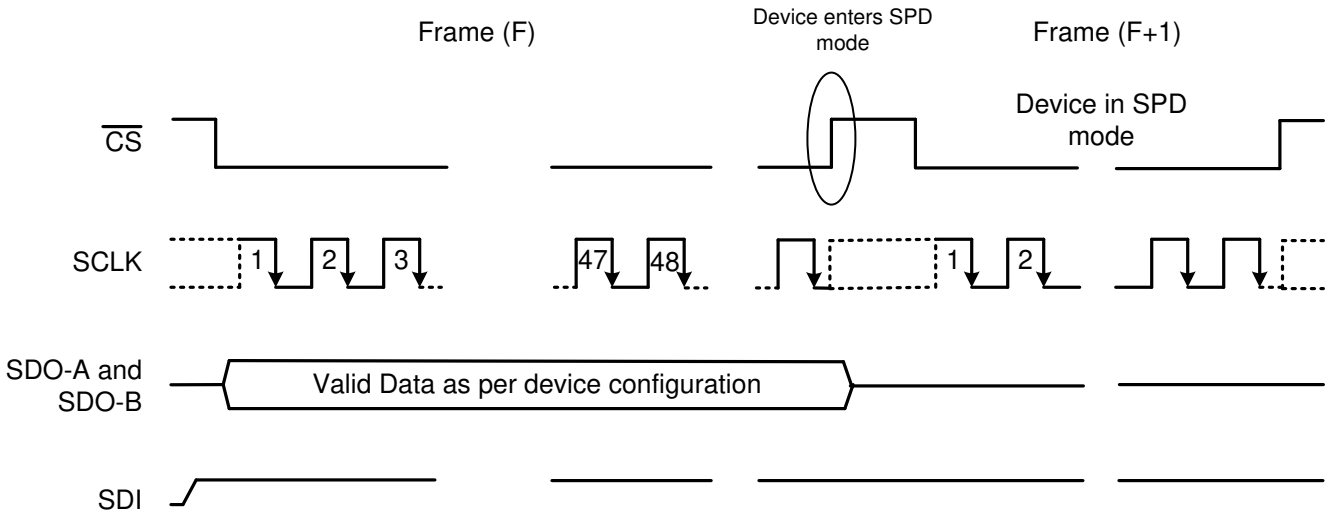
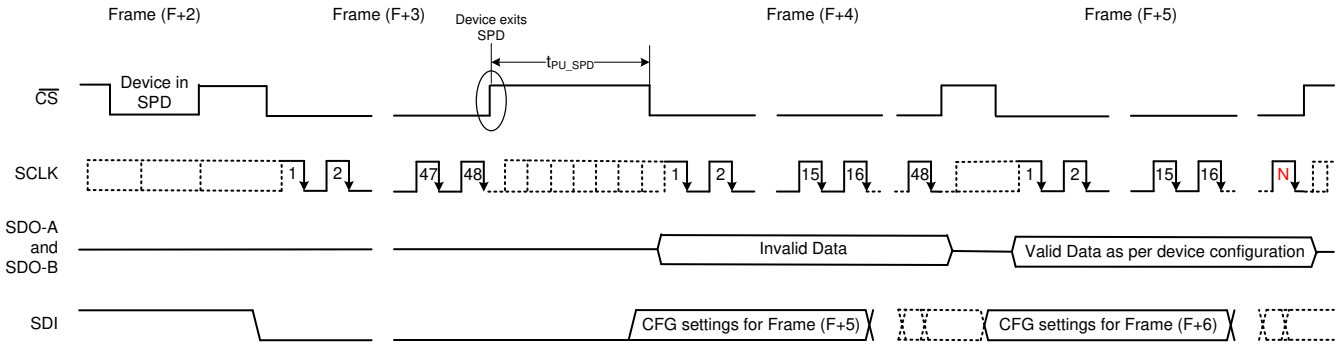


図 7-10. Enter SPD Mode

As shown in 図 7-11, to exit SPD mode, the device must be selected (by bringing $\overline{CS}$ low) and SDI must be kept low for a minimum of 48 SCLK cycles during frame (F+3). The device starts powering-up on a $\overline{CS}$ rising edge following frame (F+3). After frame (F+3), a delay of t_{PU_SPD} must elapse before programming the configuration register.

A valid write operation in frame (F+4) sets the device configuration for frame (F+5). Frame (F+4) must have at least 48 SCLK falling edges. Discard the output data in frame (F+4).



N is a function of the device configuration, as described in 表 7-4.

図 7-11. Exit SPD Mode

See the *Timing Requirements* table for timing specifications for this operating mode.

7.5.5 Frame Abort, Reconversion, or Short-Cycling

As shown in 図 7-12, the minimum number of SCLK falling edges (*N*) that must be provided between the beginning and end of the frame depends on the serial interface mode. The SCLK falling edges (*N*) program the device and retrieve the conversion result. If $\overline{CS}$ is brought high before the expected number of SCLK falling edges are provided, the current frame is aborted and the device starts sampling the new analog input signal.

If frame (F) is aborted, then the register write operation attempted in frame (F) is considered invalid and the internal registers are not updated. The device continues to have the same configuration in frame (F+1) from frame (F).

The output data bits latched before the $\overline{CS}$ rising edge are still valid data that correspond to sample N.

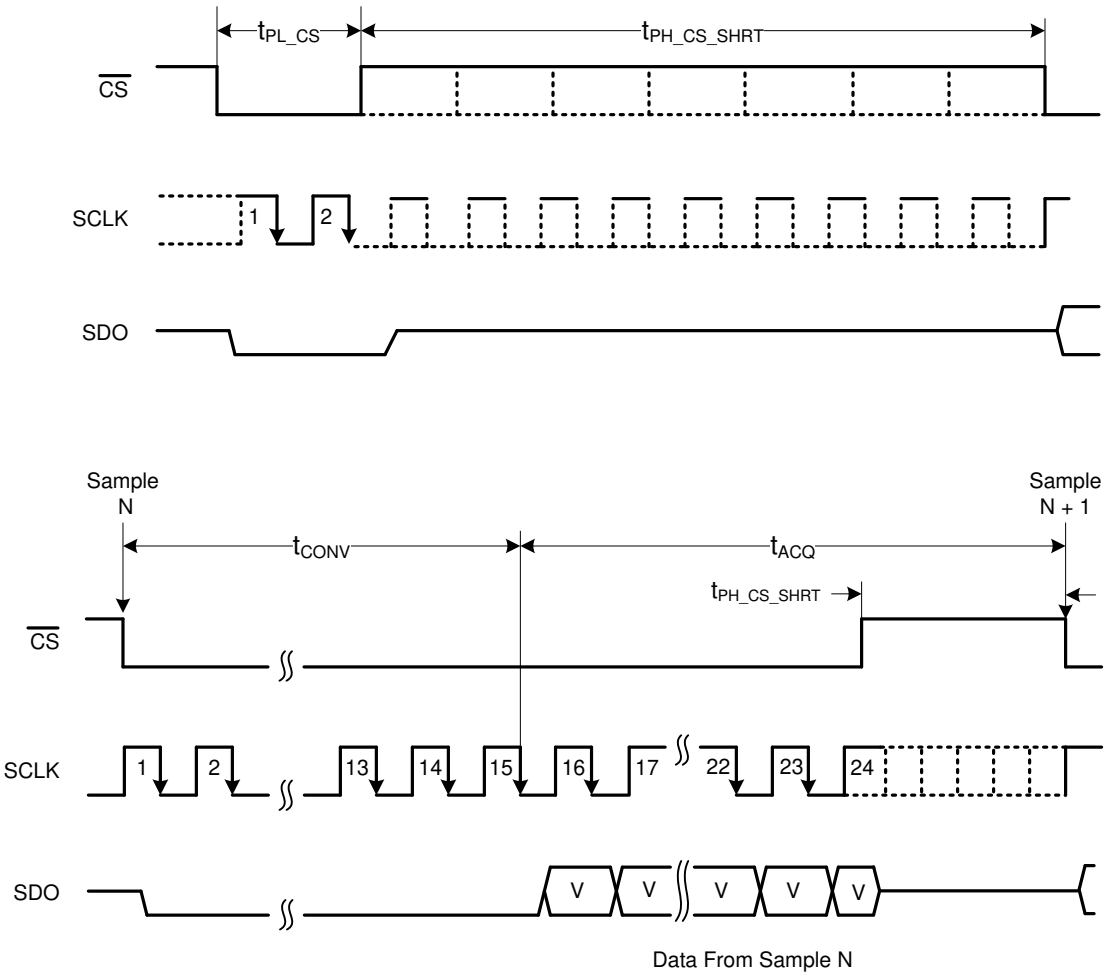


図 7-12. Frame Abort, Reconversion, or Short-Cycling Feature

See the *Timing Requirements* table for timing specifications for this operating mode.

7.6 Register Maps

7.6.1 ADS8353-Q1 Registers

表 7-11 lists the memory-mapped registers for the ADS8353-Q1 registers. Consider any register offset addresses not listed in 表 7-11 as reserved locations and, therefore, do not modify the register contents.

表 7-11. ADS8353-Q1 Registers

Offset	Acronym	Register Name	Section
0h	CFR	CFR register	セクション 7.6.1.2
2h	REFDAC	REFDAC register	セクション 7.6.1.3

Complex bit access types are encoded to fit into small table cells. 表 7-12 shows the codes that are used for access types in this section.

表 7-12. ADS8353-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 CFR Register (Offset = 0h) [reset = 0h]

CFR is shown in 図 7-9 and described in 表 7-13.

Return to 表 7-11.

図 7-13. CFR Register

15	14	13	12	11	10	9	8
WRITE_READ_CFR[3:0]				RD_CLK_MODE	RD_DATA_LINES	INPUT_RANGE	RESERVED
R/W-0000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
INM_SEL	REF_SEL	STANDBY	RD_DATA_FORMAT	0[3:0]			
R/W-0b	R/W-0b	W-0b	R/W-0b	R/W-0000b			

表 7-13. CFR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	WRITE_READ_CFR[3:0]	R/W	0000b	These bits select the user-programmable register. 0011b = Select this combination to read the CFR register 1000b = Select this combination to write to CFR register and enable bits 11:0
11	RD_CLK_MODE	R/W	0b	This bit must be set to 0 (default).
10	RD_DATA_LINES	R/W	0b	This bit provides data line selection for the serial interface. 0b = Use SDO_A to output ADC_A data and SDO_B to output of ADC_B data (default) 1b = Use only SDO_A to output of ADC_A data followed by ADC_B data
9	INPUT_RANGE	R/W	0b	This bit selects the maximum input range for the ADC as a function of the reference voltage provided to the ADC. See the *Analog Inputs* section for more details. 0b = FSR equals V_{REF} 1b = FSR equals 2 × V_{REF}
8	RESERVED	R/W	0b	This bit must be set to 0 (default).
7	INM_SEL	R/W	0b	This bit selects the voltage to be externally connected to the INM pin. 0b = INM must be externally connected to the GND potential (default) 1b = INM must be externally connected to the FSR_ADC_x / 2
6	REF_SEL	R/W	0b	This bit selects the ADC reference voltage source. See the *Reference* section for more details. 0b = Use external reference (default) 1b = Use internal reference
5	STANDBY	W	0b	This bit is used by the device to enter or exit STANDBY mode. See the *STANDBY Mode* section for more details.

表 7-13. CFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RD_DATA_FORMAT	R/W	0b	This bit selects the output data format. 0b = Output is in straight binary format (default) 1b = Output is in two's complement format
3-0	0[3:0]	R/W	0000b	These bits must be set to 0 (default).

7.6.1.2 REFDAC Register (Offset = 2h) [reset = 0h]

REFDAC is shown in 図 7-10 and described in 表 7-14.

Return to 表 7-11.

図 7-14. REFDAC Register

15	14	13	12	11	10	9	8
WRITE_READ_REFDAC[3:0]				D[8:0]			
R/W-0000b				R/W-000000000b			
7	6	5	4	3	2	1	0
D[8:0]					RESERVED		
R/W-000000000b					R/W-000b		

表 7-14. REFDAC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	WRITE_READ_REFDAC[3:0]	R/W	0000b	These bits select the configurable register address. 1001 = Select this combination to write to the REFDAC_A register 1010 = Select this combination to write to the REFDAC_B register
11-3	D[8:0]	R/W	000000000b	Data to program the individual DAC output voltage. These bits are valid only for bits 15:12 = 1001 or bits 15:12 = 1010. 表 7-15 shows the relationship between the REFDAC_x programmed value and the DAC_x output voltage.
2-0	RESERVED	R/W	000b	This bit must be set to 0 (default).

表 7-15. REFDAC Settings

REFDAC_x VALUE (Bits 11:3 in Hex)	B[2:0]	Typical DAC_x OUPTUT VOLTAGE (V)(1)
1FF (default)	000	2.5000
1FE	000	2.4989
1FD	000	2.4978
—	—	—
1D7	000	2.45
—	—	—
1AE	000	2.40
—	—	—
186	000	2.35
—	—	—
15D	000	2.30
—	—	—
134	000	2.25
—	—	—
10C	000	2.20
—	—	—

表 7-15. REFDAC Settings (continued)

REFDAC_x VALUE (Bits 11:3 in Hex)	B[2:0]	Typical DAC_x OUPTUT VOLTAGE (V)(1)
0E3	000	2.15
—	—	—
0BA	000	2.10
—	—	—
091	000	2.05
—	—	—
069	000	2.00
—	—	—
064 to 000	000	Do not use

(1) Actual output voltage may vary by a few millivolts from the specified value. To obtain the desired output voltage, TI recommends starting with the specified register setting and then experimenting with five codes on either side of the specified register setting.

8 Application and Implementation

注

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8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, and some application circuits designed using these devices.

The device supports operation either with an internal or external reference source. See the *Reference* section for details about the decoupling requirements.

The reference source to the ADC must provide low-drift and very accurate dc voltage and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise (typically in the order of a few 100 μV_{RMS}) of the reference source must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred hertz. After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive the reference input pin must be stable while driving this large capacitor and must have low output impedance, low offset, and temperature drift specifications. To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an charge kickback filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

8.1.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. Select the amplifier bandwidth as described in 式 6 to maintain the overall stability of the input driver circuit:

$$Unity-Gain\ Bandwidth \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (6)$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. 式 7 calculates noise from the input driver circuit. This noise is band-limited by designing a low cutoff frequency RC filter:

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (7)$$

where:

- V_{1/f_AMP_PP} = the peak-to-peak flicker noise in µV
- e_{n_RMS} = the amplifier broadband noise density in nV/√Hz
- f_{-3dB} = the 3-dB bandwidth of the RC filter
- N_G = the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC, as shown in 式 8, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \quad (8)$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver with TINA™-SPICE simulations before selecting the amplifier.

8.1.2 Charge Kickback Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, charge kickback filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. A charge kickback filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, keep the filter bandwidth low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

A filter capacitor, C_{FLT}, connected across the ADC inputs (see 図 8-1), filters the noise from the front-end drive circuitry, reduces the sampling charge injection, and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor must be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} must be greater than 400 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

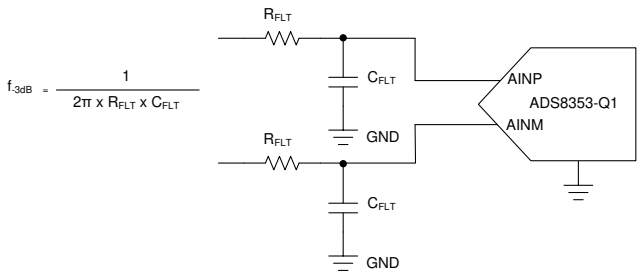
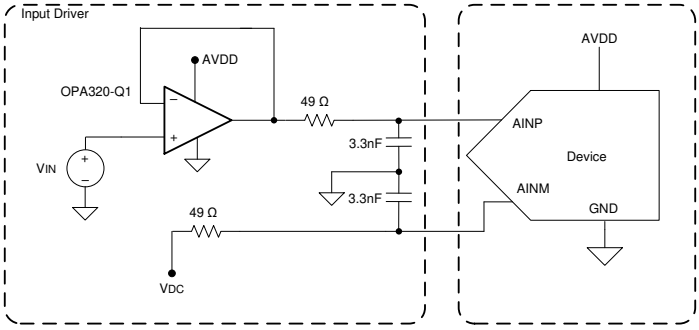


図 8-1. Charge Kickback Filter

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of

the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For more information on ADC input R-C filter component selection, see the TI Precision Labs on ti.com.

8.2 Typical Application



Only one ADC channel is shown in this diagram. Replicate the same circuit for other ADC channels.

図 8-2. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at Full Throughput, 32-CLK Interface

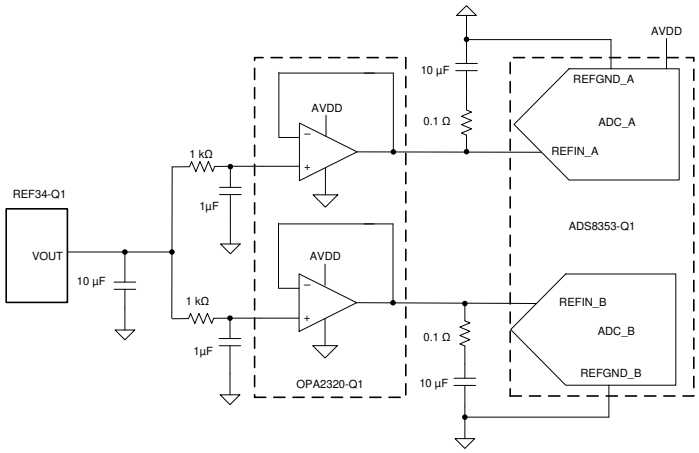


図 8-3. Reference Drive Circuit

8.2.1 Design Requirements

表 8-1 lists the target specifications for this application.

表 8-1. Target Specifications

TARGET SPECIFICATIONS		TEST CONDITIONS			
SNR	THD	DEVICE	INPUT SIGNAL FREQUENCY	THROUGHPUT	INTERFACE MODE
> 83 dB	< –100 dB	ADS8353-Q1	10 kHz	Maximum supported	32-CLK, dual-SDO

8.2.2 Detailed Design Procedure

Best practice is for the distortion from the input driver to be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of rail-to-rail swing at the amplifier input. The low-power OPA320-Q1, used as an input driver, provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

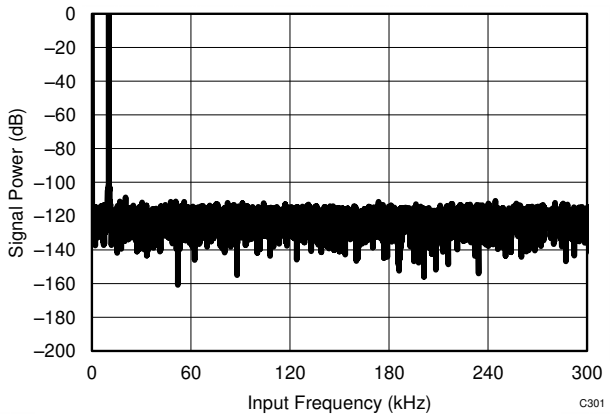
The application circuit illustrated in 図 8-2 is optimized to achieve the lowest distortion and lowest noise for a 10-kHz input signal fed to the ADS8353-Q1 operating at full throughput with the default 32-CLK, dual-SDO interface mode. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the device.

図 8-3 illustrates the reference driver circuit when operation with an external reference is desired. The reference voltage is generated by the high-precision, low-noise REF34-Q1 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10 µF. The low output impedance, low noise, and fast settling time make the OPA2320-Q1 a good choice for driving this high capacitive load.

8.2.3 Application Curve

To minimize external components and to maximize the dynamic range of the ADC, the device is configured to operate with internal reference (CFR.B6 = 1) and 2x V_{REF_x} input full-scale range (CFR.B9 = 1).

図 8-4 shows the FFT plot and test result obtained with the ADS8353-Q1 operating at full throughput with a 32-CLK interface and the circuit configuration of 図 8-2.



SNR = 83.5 dB, THD = –101.2 dB, f_{IN} = 10.1 kHz

図 8-4. ADS8353-Q1 in 32-CLK Interface Mode

8.3 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges.

When using the device with the 2× V_{REF} input range (CFR.B9 = 1), the AVDD supply voltage value defines the permissible voltage swing on the analog input pins. AVDD must be set as shown in 式 9, 式 10, and 式 11 to avoid saturation of output codes and to use the full dynamic range on the analog input pins:

$$AVDD \geq 2 \times V_{REF\_A} \quad (9)$$

$$AVDD \geq 2 \times V_{REF\_B} \quad (10)$$

$$4.75\ V \leq AVDD \leq 5.25\ V \quad (11)$$

Decouple the AVDD and DVDD pins, as shown in 図 8-5, with the GND pin using individual 10-µF decoupling capacitors.

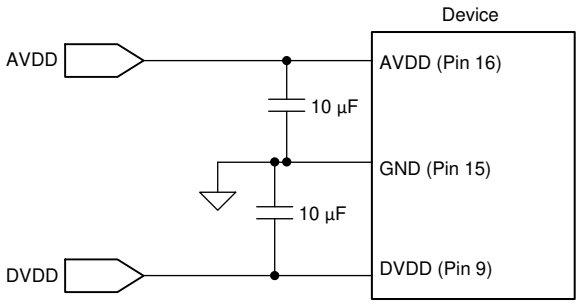


図 8-5. Power-Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

図 8-6 shows a board layout example for the ADS8353-Q1 TSSOP package. Partition the printed circuit board (PCB) into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in 図 8-6, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the device must be clean and well-bypassed. Use 10-µF, ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low impedance paths.

The REFIO-A and REFIO-B reference inputs and outputs are bypassed with 10-µF, X7R-grade, 0805-size, 16-V rated ceramic capacitors (C_{REF-x}). Place the reference bypass capacitors as close as possible to the reference REFIO-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIO-x pins and the bypass capacitors. Small 0.1-Ω to 0.2-Ω resistors (R_{REF-x}) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. 図 8-6 shows C_{IN-A} and C_{IN-B} filter capacitors placed across the analog input pins of the device.

8.4.2 Layout Example

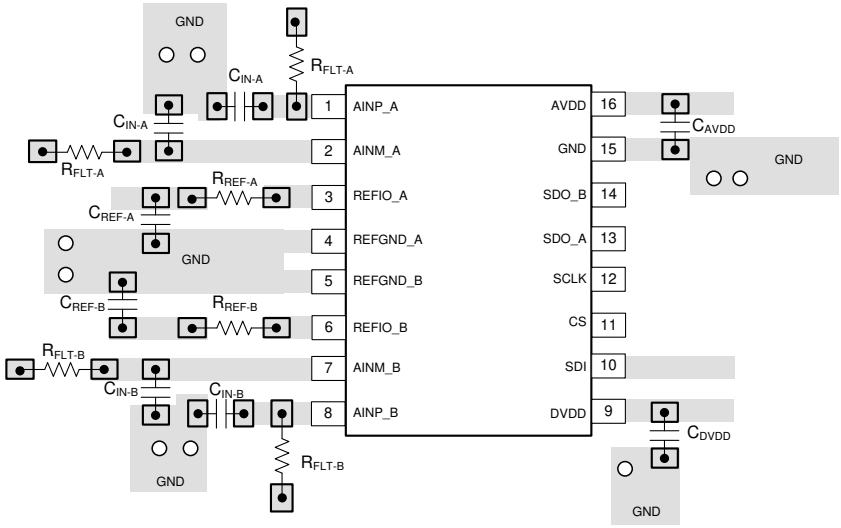


図 8-6. Recommended Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

Texas Instruments, *TI Precision Labs* TI training and videos site

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPAx320-Q1 Precision, 20-MHz, 0.9-pA, low-noise, RRIO, CMOS operational amplifier* data sheet
- Texas Instruments, *REF34-Q1 Low-drift, low-power, small-footprint series voltage references* data sheet

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8353QPWQ1	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A8353Q	Samples
ADS8353QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A8353Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS8353-Q1 :

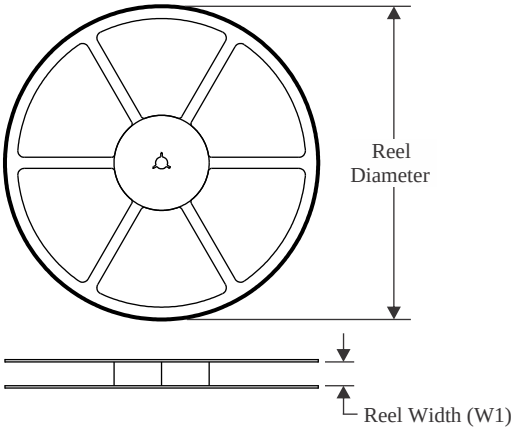
- Catalog : ADS8353

NOTE: Qualified Version Definitions:

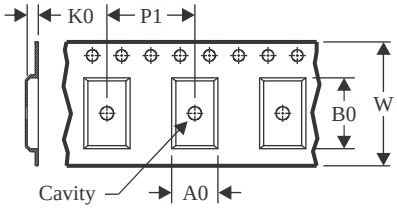
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

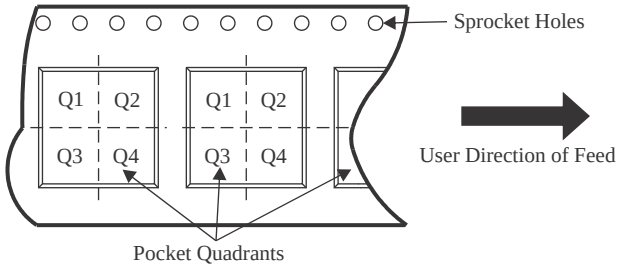


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

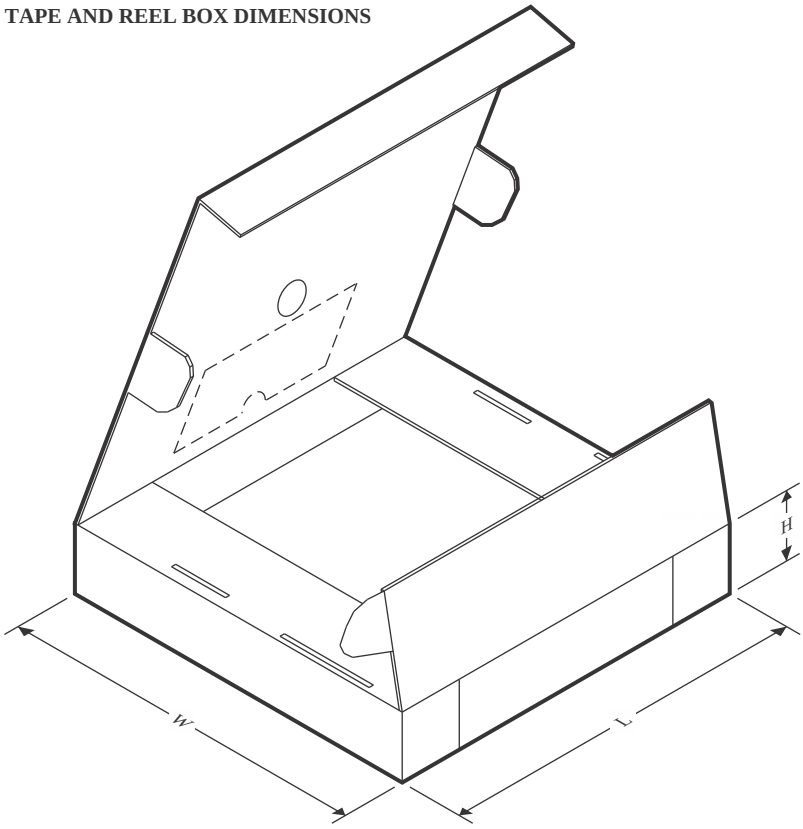
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8353QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

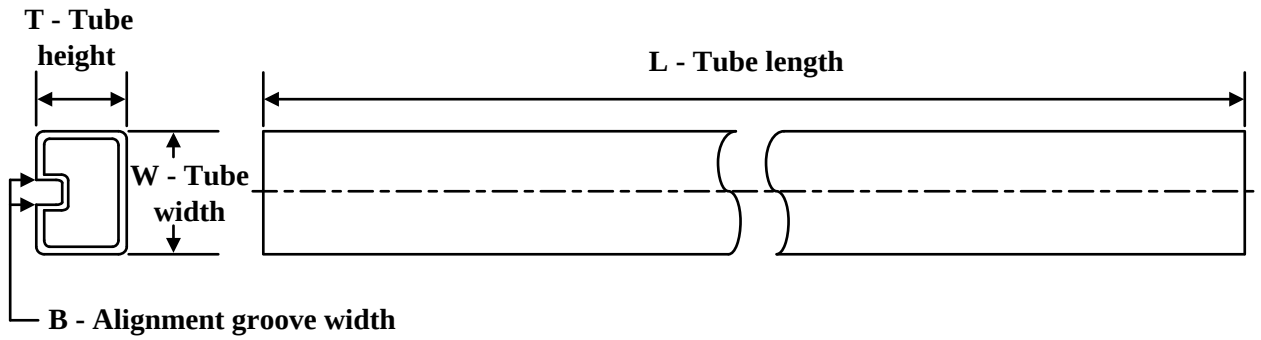
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8353QPWRQ1	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

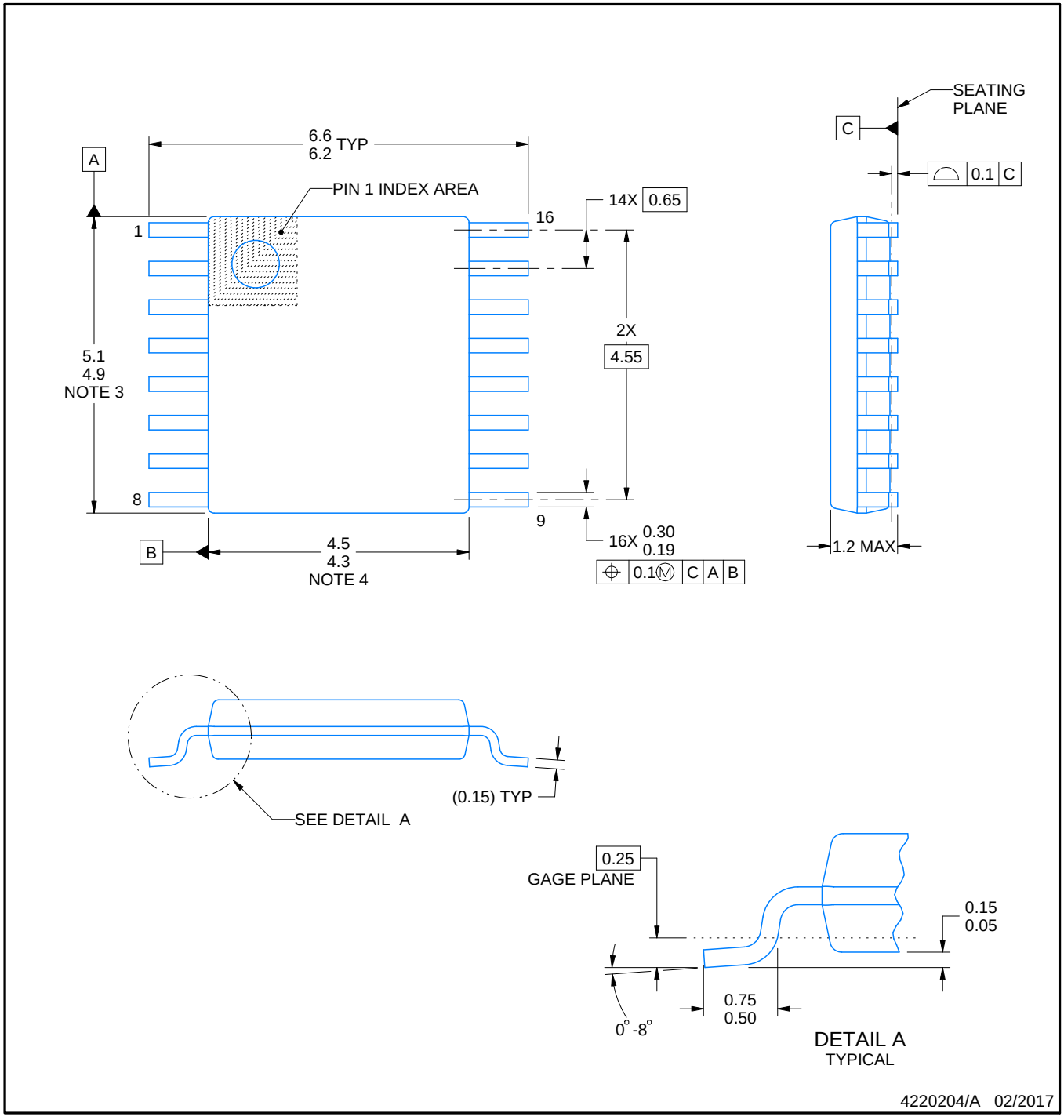
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8353QPWQ1	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

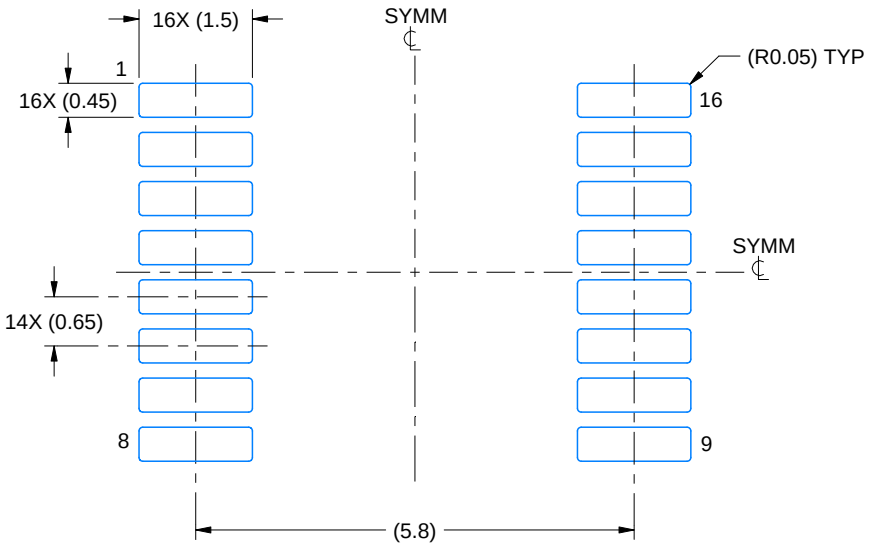
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

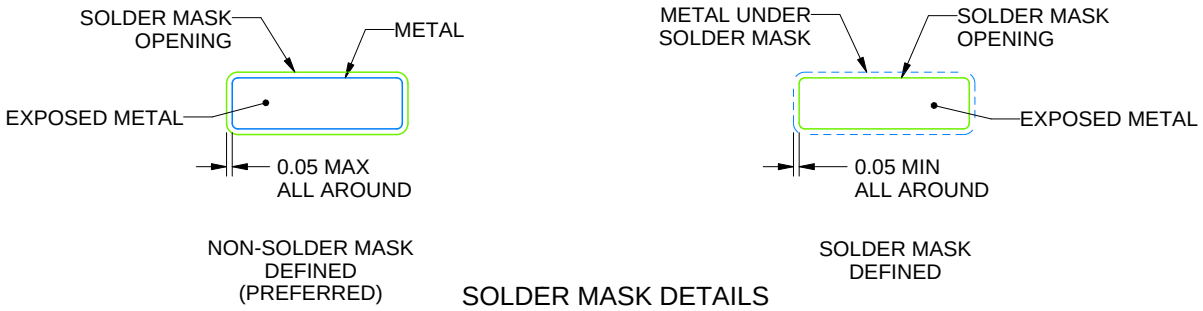


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

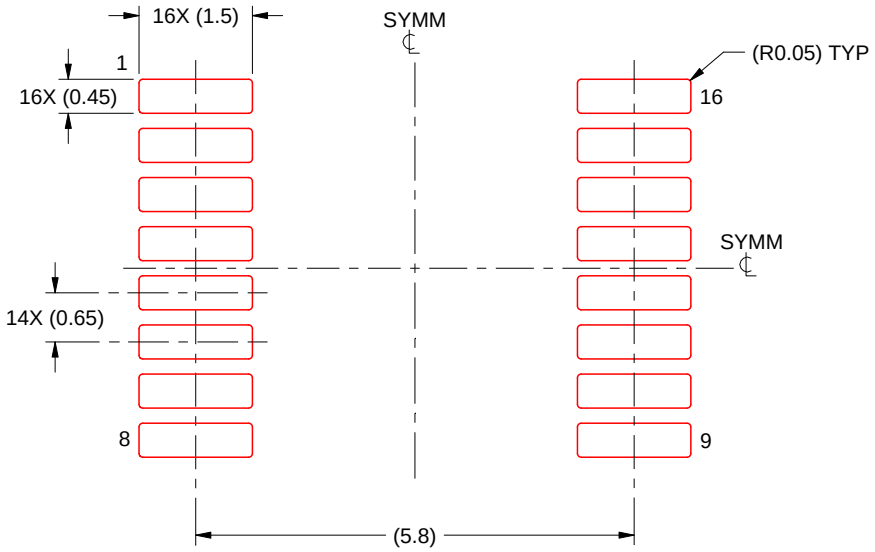


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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