TEXAS INSTRUMENTS

ADS8688AT

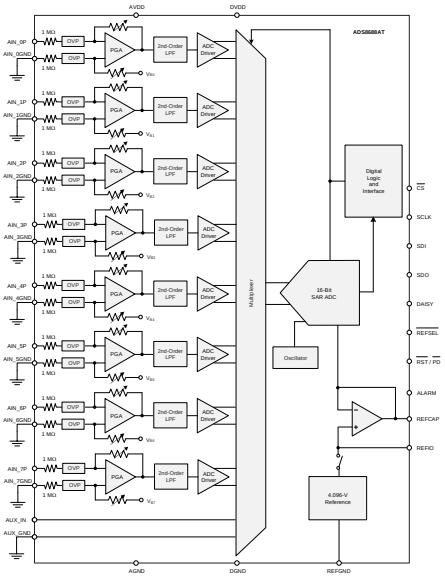
JAJSFM5 – JUNE 2018

ADS8688AT 16ビット、500kSPS、8チャネル、シングル電源、バイポーラ入力範囲のSAR ADC

1 特長

- アナログ・フロントエンド内蔵の16ビットADC
- 自動および手動スキャン機能付きの8チャネルMUX
- チャネルと独立のプログラム可能入力
  - ±10.24V、±5.12V、±2.56V、±1.28V、±0.64V
  - 10.24V、5.12V、2.56V、1.28V
- 5Vアナログ電源: 1.65V～5VのI/O電源
- 一定の抵抗性入力インピーダンス: 1MΩ
- 入力過電圧保護: 最高±20V
- 4.096Vでドリフト係数6ppm/℃の基準電圧を内蔵
- 優れた性能
  - 500kSPSの合計スループット
  - DNL: ±0.5LSB、INL: ±0.75LSB
  - ゲイン誤差およびオフセットのドリフト係数: 1ppm/℃
  - SNR: 92dB、THD: -102dB
  - 低消費電力: 65mW
- AUX入力 → ADC入力への直接接続
- ALARM → チャネルごとの高/低スレッショルド
- SPI™互換のインターフェイス、デイジー・チェーン接続
- 温度範囲: -55℃～+125℃
- TSSOP-38パッケージ(9.7mm×4.4mm)

ブロック図



2 アプリケーション

- パワー・オートメーション
- 保護リレー
- PLCアナログ入力モジュール

3 概要

ADS8688ATは8チャネルの統合データ収集システムで、16ビットの逐次比較(SAR)アナログ/デジタル・コンバータ(ADC)を基礎とし、最高500kSPSのスループットで動作します。このデバイスでは、各入力チャネルにアナログ・フロントエンド回路が搭載されており、最高±20Vの過電圧保護、自動および手動スキャン・モードを持つ8チャネルのマルチプレクサ、および温度ドリフト係数の低い4.096Vの基準電圧が内蔵されています。

単一の5Vアナログ電源で動作し、各チャネル入力は複数の真のバイポーラおよびユニポーラ入力範囲に対応します。各入力範囲はソフトウェアによりプログラム可能で、チャネルごとに独立しているため、システムを最大限に柔軟に活用できます。すべての入力範囲に対して高いDC精度を保証するよう、アナログ・フロントエンドのゲインは正確にトリムされています。このデバイスは、選択されたあらゆる入力範囲について1MΩの一定の抵抗性入力インピーダンスを持つため、デバイスにセンサを直接接続できます。

ADS8688ATには、デジタル・ホストと接続するための単純なSPI互換のシリアル・インターフェイスがあり、複数のデバイスをデイジー・チェーン接続できます。デジタル電源は1.65V～5.25Vで動作し、広範なホスト・コントローラと直接接続できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS8688AT	TSSOP (38)	9.70mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

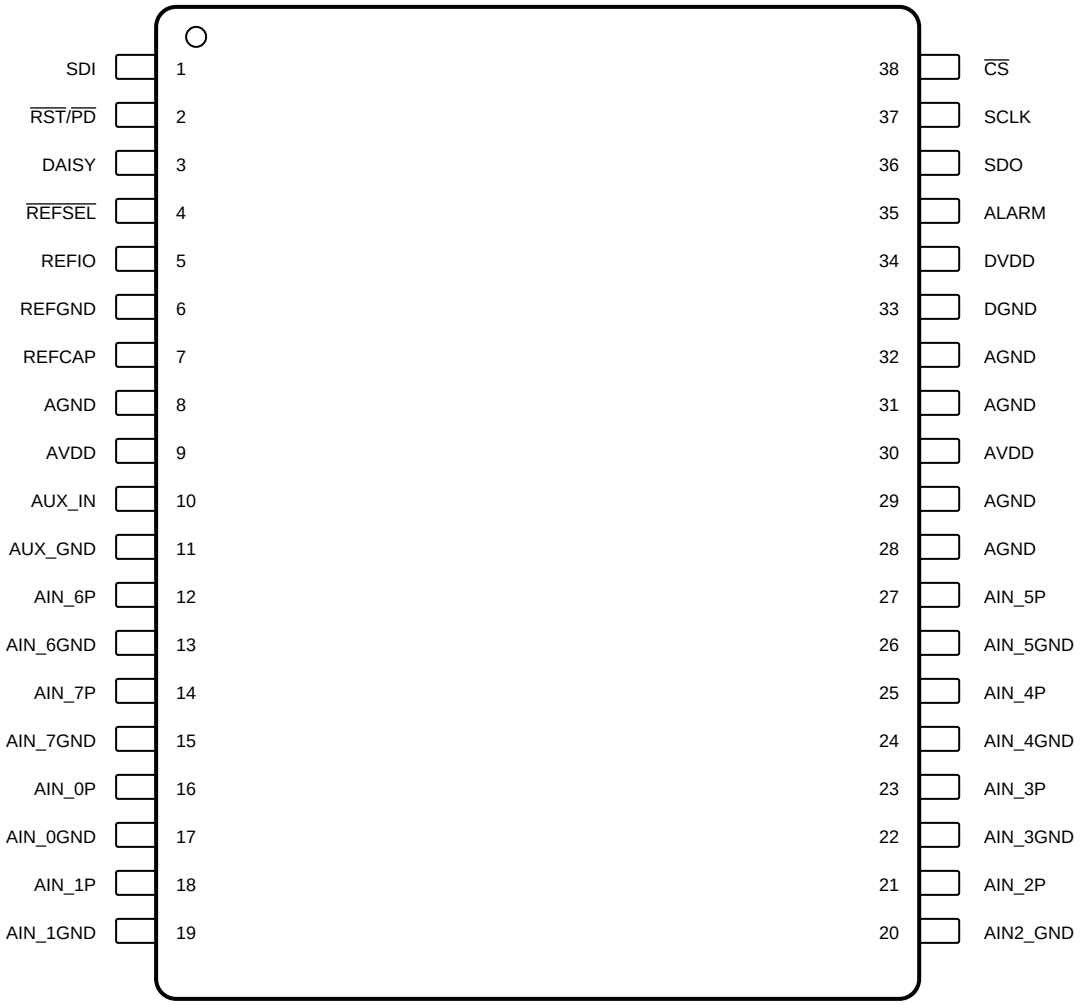
目次

4 改訂履歴

日付	リビジョン	注
2018年6月	*	初版

5 Pin Configuration and Functions

DBT Package
38-Pin TSSOP
Top View



Not to scale

Pin Functions

NO.	NAME	I/O	DESCRIPTION
1	SDI	Digital input	Data input for serial communication.
2	$\overline{\text{RST}}/\overline{\text{PD}}$	Digital input	Active low logic input. Dual functionality to reset or power-down the device.
3	DAISY	Digital input	Chain the data input during serial communication in daisy-chain mode.
4	$\overline{\text{REFSEL}}$	Digital input	Active low logic input to enable the internal reference. When low, the internal reference is enabled; REFIO becomes an output that includes the V_{REF} voltage. When high, the internal reference is disabled; REFIO becomes an input to apply the external V_{REF} voltage.
5	REFIO	Analog input, output	Internal reference output and external reference input pin. Decouple with REFGND on pin 6.
6	REFGND	Power supply	Reference GND pin; short to the analog GND plane. Decouple with REFIO on pin 5 and REFCAP on pin 7.
7	REFCAP	Analog output	ADC reference decoupling capacitor pin. Decouple with REFGND on pin 6.
8	AGND	Power supply	Analog ground pin. Decouple with AVDD on pin 9.
9	AVDD	Power supply	Analog supply pin. Decouple with AGND on pin 8.
10	AUX_IN	Analog input	Auxiliary input channel: positive input. Decouple with AUX_GND on pin 11.
11	AUX_GND	Analog input	Auxiliary input channel: negative input. Decouple with AUX_IN on pin 10.
12	AIN_6P	Analog input	Analog input channel 6, positive input. Decouple with AIN_6GND on pin 13.
13	AIN_6GND	Analog input	Analog input channel 6, negative input. Decouple with AIN_6P on pin 12.
14	AIN_7P	Analog input	Analog input channel 7, positive input. Decouple with AIN_7GND on pin 15.
15	AIN_7GND	Analog input	Analog input channel 7, negative input. Decouple with AIN_7P on pin 14.
16	AIN_0P	Analog input	Analog input channel 0, positive input. Decouple with AIN_0GND on pin 17.
17	AIN_0GND	Analog input	Analog input channel 0, negative input. Decouple with AIN_0P on pin 16.
18	AIN_1P	Analog input	Analog input channel 1, positive input. Decouple with AIN_1GND on pin 19.
19	AIN_1GND	Analog input	Analog input channel 1, negative input. Decouple with AIN_1P on pin 18.
20	AIN2_GND	Analog input	Analog input channel 2, negative input. Decouple with AIN_2P on pin 21.
21	AIN_2P	Analog input	Analog input channel 2, positive input. Decouple with AIN_2GND on pin 20.
22	AIN_3GND	Analog input	Analog input channel 3, negative input. Decouple with AIN_3P on pin 23.
23	AIN_3P	Analog input	Analog input channel 3, positive input. Decouple with AIN_3GND on pin 22.
24	AIN_4GND	Analog input	Analog input channel 4, negative input. Decouple with AIN_4P on pin 25.
25	AIN_4P	Analog input	Analog input channel 4, positive input. Decouple with AIN_4GND on pin 24.
26	AIN_5GND	Analog input	Analog input channel 5, negative input. Decouple with AIN_5P on pin 27.
27	AIN_5P	Analog input	Analog input channel 5, positive input. Decouple with AIN_5GND on pin 26.
28	AGND	Power supply	Analog ground pin
29	AGND	Power supply	Analog ground pin
30	AVDD	Power supply	Analog supply pin. Decouple with AGND on pin 31.
31	AGND	Power supply	Analog ground pin. Decouple with AVDD on pin 30.
32	AGND	Power supply	Analog ground pin
33	DGND	Power supply	Digital ground pin. Decouple with DVDD on pin 34.
34	DVDD	Power supply	Digital supply pin. Decouple with DGND on pin 33.
35	ALARM	Digital output	Active high alarm output
36	SDO	Digital output	Data output for serial communication
37	SCLK	Digital input	Clock input for serial communication
38	$\overline{\text{CS}}$	Digital input	Active low logic input; chip-select signal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AIN_*n*P, AIN_*n*GND to GND(2)	–20	20	V
AIN_*n*P, AIN_*n*GND to GND(3)	–11	11	V
AUX_GND to GND	–0.3	0.3	V
AUX_IN to GND	–0.3	AVDD + 0.3	V
AVDD to GND or DVDD to GND	–0.3	7	V
REFCAP to REFGND or REFIO to REFGND	–0.3	5.7	V
GND to REFGND	–0.3	0.3	V
Digital input pins to GND	–0.3	DVDD + 0.3	V
Digital output pins to GND	–0.3	DVDD + 0.3	V
Operating temperature, T_A	–55	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AVDD = 5 V.
(3) AVDD = floating.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Analog input pins (AIN_*n*P; AIN_*n*GND)	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	4.75	5	5.25	V
DVDD	Digital supply voltage	1.65	3.3	AVDD	V

6.4 Thermal Information

THERMAL METRIC(1)		ADS8688AT DBT (TSSOP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
ANALOG INPUTS							
	Full-scale input span(2) (AIN_*n*P to AIN_*n*GND)	Input range = ±2.5 × V_{REF}	–2.5 × V_{REF}		2.5 × V_{REF}	V	A
		Input range = ±1.25 × V_{REF}	–1.25 × V_{REF}		1.25 × V_{REF}		A
		Input range = ±0.625 × V_{REF}	–0.625 × V_{REF}		0.625 × V_{REF}		A
		Input range = ±0.3125 × V_{REF}	–0.3125 × V_{REF}		0.3125 × V_{REF}		A
		Input range = ±0.15625 × V_{REF}	–0.15625 × V_{REF}		0.15625 × V_{REF}		A
		Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}		A
		Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}		A
		Input range = 0.625 × V_{REF}	0		0.625 × V_{REF}		A
		Input range = 0.3125 × V_{REF}	0		0.3125 × V_{REF}		A
AIN_*n*P	Operating input range, positive input	Input range = ±2.5 × V_{REF}	–2.5 × V_{REF}		2.5 × V_{REF}	V	A
		Input range = ±1.25 × V_{REF}	–1.25 × V_{REF}		1.25 × V_{REF}		A
		Input range = ±0.625 × V_{REF}	–0.625 × V_{REF}		0.625 × V_{REF}		A
		Input range = ±0.3125 × V_{REF}	–0.3125 × V_{REF}		0.3125 × V_{REF}		A
		Input range = ±0.15625 × V_{REF}	–0.15625 × V_{REF}		0.15625 × V_{REF}		A
		Input range = 2.5 × V_{REF}	0		2.5 × V_{REF}		A
		Input range = 1.25 × V_{REF}	0		1.25 × V_{REF}		A
		Input range = 0.625 × V_{REF}	0		0.625 × V_{REF}		A
		Input range = 0.3125 × V_{REF}	0		0.3125 × V_{REF}		A
AIN_*n*GND	Operating input range, negative input	All input ranges	–0.1	0	0.1	V	B
z_i	Input impedance	At T_A = 25°C, all input ranges	0.85	1	1.15	MΩ	B
	Input impedance drift	All input ranges		7	32	ppm/°C	B
$I_{lkg(in)}$	Input leakage current	With voltage at AIN_*n*P pin = V_{IN}, input range = ±2.5 × V_{REF}	$\frac{V_{IN} - 2.25}{R_{IN}}$			µA	A
		With voltage at AIN_*n*P pin = V_{IN}, input range = ±1.25 × V_{REF}	$\frac{V_{IN} - 2.00}{R_{IN}}$				A
		With voltage at AIN_*n*P pin = V_{IN}, input ranges = ±0.625 × V_{REF}; ±0.3125 × V_{REF}; ±0.15625 × V_{REF}	$\frac{V_{IN} - 1.60}{R_{IN}}$				A
		With voltage at AIN_*n*P pin = V_{IN}, input range = 2.5 × V_{REF}	$\frac{V_{IN} - 2.50}{R_{IN}}$				A
		With voltage at AIN_*n*P pin = V_{IN}, input range = 1.25 × V_{REF}; 0.625 × V_{REF}; 0.3125 × V_{REF}	$\frac{V_{IN} - 2.50}{R_{IN}}$				A
INPUT OVERVOLTAGE PROTECTION							
V_{OVP}	Overvoltage protection voltage	AVDD = 5 V	–20		20	V	B
		AVDD = floating	–11		11		B

(1) Test Levels: **(A)** Tested at final test. Overtemperature limits are set by characterization and simulation. **(B)** Limits set by characterization and simulation, across temperature range. **(C)** Typical value only for information, provided by design simulation.
(2) Ideal input span, does not include gain or offset error.

Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
SYSTEM PERFORMANCE							
	Resolution		16			Bits	A
NMC	No missing codes		16			Bits	A
DNL	Differential nonlinearity		–0.99	±0.5	1.5	LSB(3)	A
INL	Integral nonlinearity(4)		–2	±0.75	2	LSB	A
E_G	Gain error	At T_A = 25°C, all input ranges		±0.02	±0.05	%FSR(5)	A
	Gain error matching (channel-to-channel)	At T_A = 25°C, all input ranges		±0.02	±0.05	%FSR	A
	Gain error temperature drift	All input ranges		1	6	ppm/°C	B
E_O	Offset error	At T_A = 25°C, input range = ±2.5 × V_{REF}(6)		±0.5	±1	mV	A
		At T_A = 25°C, input range = ±1.25 × V_{REF}		±0.5	±1		A
		At T_A = 25°C, input range = ±0.625 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, input range = ±0.3125 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, input range = ±0.15625 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, all unipolar input ranges		±0.5	±2		A
	Offset error matching (channel-to-channel)	At T_A = 25°C, input range = ±2.5 × V_{REF}(6)		±0.5	±1	mV	A
		At T_A = 25°C, input range = ±1.25 × V_{REF}		±0.5	±1		A
		At T_A = 25°C, input range = ±0.625 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, input range = ±0.3125 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, input range = ±0.15625 × V_{REF}		±0.5	±1.5		A
		At T_A = 25°C, all unipolar input ranges		±0.5	±2		A
	Offset error temperature drift	Input range = ±2.5 × V_{REF}		1	15	ppm/°C	B
		Input range = ±1.25 × V_{REF}		1	4		B
		Input range = ±0.625 × V_{REF}		1	4		B
		Input range = ±0.3125 × V_{REF}		2	15		B
		Input range = ±0.15625 × V_{REF}		4	26		B
		Input range = 0 to 2.5 × V_{REF}		1	12		B
		Input range = 0 to 1.25 × V_{REF}		1	6		B
		Input range = 0 to 0.625 × V_{REF}		2	15		B
		Input range = 0 to 0.3125 × V_{REF}		4	26		B
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				850	ns	A
t_{ACQ}	Acquisition time		1150			ns	A
f_S	Maximum throughput rate without latency				500	kSPS	A

(3) LSB = least significant bit.
(4) This parameter is the endpoint INL, not best-fit INL.
(5) FSR = full-scale range.
(6) Does not include the shift in offset over time.

Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
DYNAMIC CHARACTERISTICS							
SNR	Signal-to-noise ratio (V_{IN} – 0.5 dBFS at 1 kHz)	Input range = ±2.5 × V_{REF}	90	92		dB	A
		Input range = ±1.25 × V_{REF}	89	91			A
		Input range = ±0.625 × V_{REF}	87.5	89			A
		Input range = ±0.3125 × V_{REF}	81.5	83			A
		Input range = ±0.15625 × V_{REF}	75.5	77			A
		Input range = 2.5 × V_{REF}	88.5	90.5			A
		Input range = 1.25 × V_{REF}	87.5	89			A
		Input range = 0.625 × V_{REF}	81.5	83			A
		Input range = 0.3125 × V_{REF}	75.5	77			A
THD	Total harmonic distortion(7) (V_{IN} – 0.5 dBFS at 1 kHz)	Input ranges = ±2.5 × V_{REF}, ±1.25 × V_{REF}, ±0.625 × V_{REF}, 2.5 × V_{REF}, 1.25 × V_{REF}		–102		dB	B
		Input ranges = ±0.3125 × V_{REF}, ±0.15625 × V_{REF}, 0.625 × V_{REF}, 0.3125 × V_{REF}		–100			
SINAD	Signal-to-noise ratio (V_{IN} – 0.5 dBFS at 1 kHz)	Input range = ±2.5 × V_{REF}	89	91.5		dB	A
		Input range = ±1.25 × V_{REF}	88.5	91			A
		Input range = ±0.625 × V_{REF}	87	89			A
		Input range = ±0.3125 × V_{REF}	81	83			A
		Input range = ±0.15625 × V_{REF}	75	77			A
		Input range = 2.5 × V_{REF}	87.5	90.5			A
		Input range = 1.25 × V_{REF}	87	89			A
		Input range = 0.625 × V_{REF}	81	83			A
		Input range = 0.3125 × V_{REF}	75	77			A
SFDR	Spurious-free dynamic range (V_{IN} – 0.5 dBFS at 1 kHz)	Input ranges = ±2.5 × V_{REF}, ±1.25 × V_{REF}, ±0.625 × V_{REF}, 2.5 × V_{REF}, 1.25 × V_{REF}		103		dB	B
		Input ranges = ±0.3125 × V_{REF}, ±0.15625 × V_{REF}, 0.625 × V_{REF}, 0.3125 × V_{REF}		101			
	Crosstalk isolation(8)	Aggressor channel input overdriven to 2 × maximum input voltage		110		dB	B
	Crosstalk memory(9)	Aggressor channel input overdriven to 2 × maximum input voltage		90		dB	B
$BW_{(–3\ dB)}$	Small-signal bandwidth, –3 dB	At T_A = 25°C, all input ranges		15		kHz	B
$BW_{(–0.1\ dB)}$	Small-signal bandwidth, –0.1 dB	At T_A = 25°C, all input ranges		2.5		kHz	B

(7) Calculated on the first nine harmonics of the input frequency.
(8) Isolation crosstalk is measured by applying a full-scale sinusoidal signal up to 10 kHz to a channel, not selected in the multiplexing sequence, and measuring its effect on the output of any selected channel.
(9) Memory crosstalk is measured by applying a full-scale sinusoidal signal up to 10 kHz to a channel that is selected in the multiplexing sequence, and measuring its effect on the output of the next selected channel for all combinations of input channels.

Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AUXILIARY CHANNEL							
	Resolution		16			Bits	A
$V_{(AUX\_IN)}$	AUX_IN voltage range	(AUX_IN – AUX_GND)	0		V_{REF}	V	A
	Operating input range	AUX_IN	0		V_{REF}	V	A
		AUX_GND		0		V	A
C_i	Input capacitance	During sampling		75		pF	C
		During conversion		5		pF	C
$I_{lkg(in)}$	Input leakage current			100		nA	A
DNL	Differential nonlinearity		–0.99	±0.6	2	LSB	A
INL	Integral nonlinearity		–4	±1.5	4	LSB	A
$E_{G(AUX)}$	Gain error	At T_A = 25°C		±0.02	±0.2	%FSR	A
$E_{O(AUX)}$	Offset error	At T_A = 25°C	–5		5	mV	A
SNR	Signal-to-noise ratio	$V_{(AUX\_IN)}$ = –0.5 dBFS at 1 kHz	87	89		dB	A
THD	Total harmonic distortion(7)	$V_{(AUX\_IN)}$ = –0.5 dBFS at 1 kHz		–102		dB	B
SINAD	Signal-to-noise + distortion	$V_{(AUX\_IN)}$ = –0.5 dBFS at 1 kHz	86	88.5		dB	A
SFDR	Spurious-free dynamic range	$V_{(AUX\_IN)}$ = –0.5 dBFS at 1 kHz		103		dB	B
INTERNAL REFERENCE OUTPUT							
$V_{(REFIO\_INT)}$(10)	Voltage on REFIO pin (configured as output)	At T_A = 25°C	4.095	4.096	4.097	V	A
	Internal reference temperature drift			6	17	ppm/°C	B
$C_{(OUT\_REFIO)}$	Decoupling capacitor on REFIO		10	22		µF	B
$V_{(REFCAP)}$	Reference voltage to ADC (on REFCAP pin)	At T_A = 25°C	4.095	4.096	4.097	V	A
	Reference buffer output impedance			0.5	1	Ω	B
	Reference buffer temperature drift			0.6	4.5	ppm/°C	B
$C_{(OUT\_REFCAP)}$	Decoupling capacitor on REFCAP		10	22		µF	B
	Turn-on time	$C_{(OUT\_REFCAP)}$ = 22 µF, $C_{(OUT\_REFIO)}$ = 22 µF		15		ms	B
EXTERNAL REFERENCE INPUT							
V_{REFIO_EXT}	External reference voltage on REFIO (configured as input)		4.046	4.096	4.146	V	C

(10) Does not include the variation in voltage resulting from solder-shift and long-term effects.

Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
POWER-SUPPLY REQUIREMENTS								
AVDD	Analog power-supply voltage		Analog supply	4.75	5	5.25	V	B
DVDD	Digital power-supply voltage		Digital supply range	1.65	3.3	AVDD	V	B
			Digital supply range for specified performance	2.7	3.3	5.25		B
I_{AVDD_DYN}	Analog supply current	Dynamic, AVDD	AVDD = 5 V, f_S = maximum and internal reference		13	16	mA	A
I_{AVDD_STC}		Static	AVDD = 5 V, device not converting and internal reference		10	12	mA	A
I_{STDBY}		Standby	At AVDD = 5 V, device in STDBY mode and internal reference		3	4.5	mA	A
I_{PWR_DN}		Power-down	At AVDD = 5 V, device in PWR_DN		3	20	µA	B
I_{DVDD_DYN}	Digital supply current		At DVDD = 3.3 V, output = 0000h		0.5		mA	A
DIGITAL INPUTS (CMOS)								
V_{IH}	Digital input high logic levels		DVDD > 2.1 V	0.7 × DVDD		DVDD + 0.3	V	A
			DVDD ≤ 2.1 V	0.8 × DVDD		DVDD + 0.3		A
V_{IL}	Digital input low logic levels		DVDD > 2.1 V	–0.3		0.3 × DVDD	V	A
			DVDD ≤ 2.1 V	–0.3		0.2 × DVDD		A
	Input leakage current				100		nA	A
	Input pin capacitance				5		pF	C
DIGITAL OUTPUTS (CMOS)								
V_{OH}	Digital output logic levels		I_O = 500-µA source	0.8 × DVDD		DVDD	V	A
V_{OL}			I_O = 500-µA sink	0		0.2 × DVDD		A
	Floating state leakage current		Only for SDO		1		µA	A
	Internal pin capacitance				5		pF	C

6.6 Timing Requirements: Serial Interface

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), SDO load = 20 pF, and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

		MIN	NOM	MAX	UNIT
t_{ACQ}	Acquisition time	1150			ns
t_{PH_CK}	Clock high time	0.4		0.6	t_{SCLK}
t_{PL_CK}	Clock low time	0.4		0.6	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time	30			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	30			ns
t_{HT_CKDO}	Hold time: SCLK falling to (previous) data valid on SDO	10			ns
t_{SU_DOCK}	Setup time: SDO data valid to SCLK falling	25			ns
t_{SU_DICK}	Setup time: SDI data valid to SCLK falling	5			ns
t_{HT_CKDI}	Hold time: SCLK falling to (previous) data valid on SDI	5			ns
t_{SU_DSYCK}	Setup time: DAISY data valid to SCLK falling	5			ns
t_{HT_CKDSY}	Hold time: SCLK falling to (previous) data valid on DAISY	5			ns

6.7 Switching Characteristics: Serial Interface

minimum and maximum specifications are at T_A = –55°C to +125°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), SDO load = 20 pF, and f_{SAMPLE} = 500 kSPS (unless otherwise noted); typical specifications are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_S	Sampling frequency (f_{CLK} = max)				500	kSPS
t_S	ADC cycle time period (f_{CLK} = max)		2			µs
f_{SCLK}	Serial clock frequency (f_S = max)				17	MHz
t_{SCLK}	Serial clock time period (f_S = max)		59			ns
t_{CONV}	Conversion time				850	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ falling to data enable				10	ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		10			ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to 3-state		10			ns

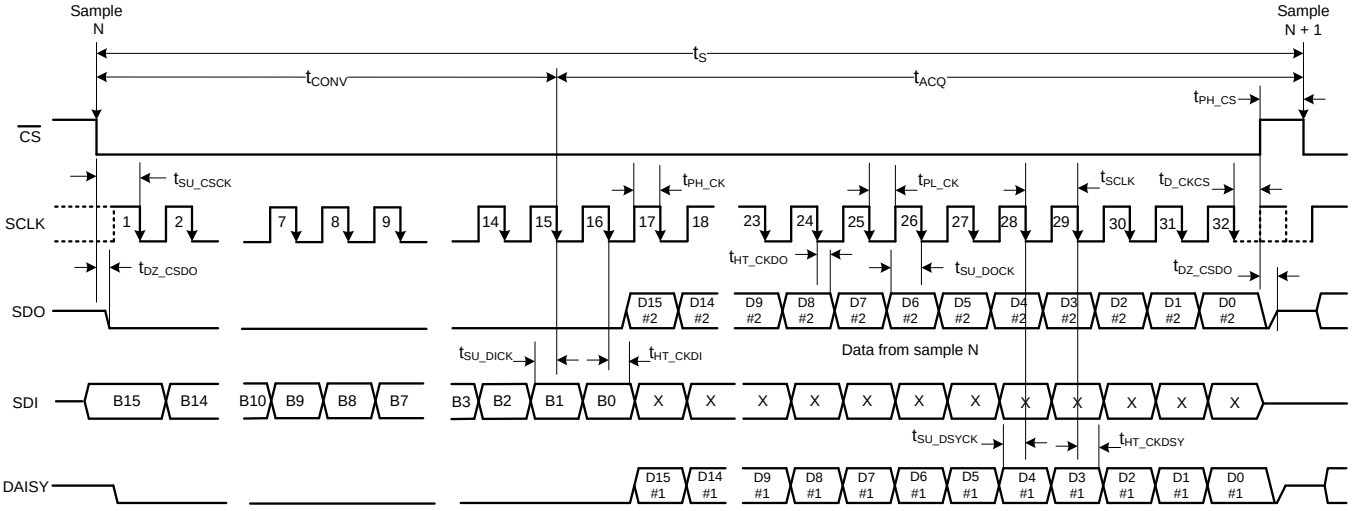


図 1. Serial Interface Timing Diagram

6.8 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

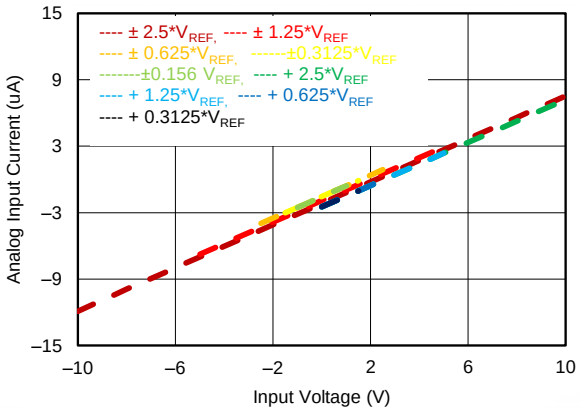
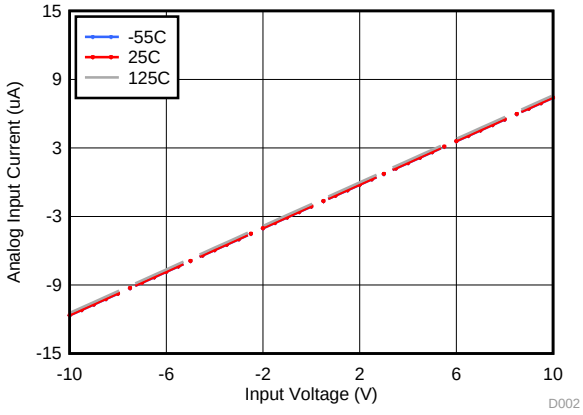
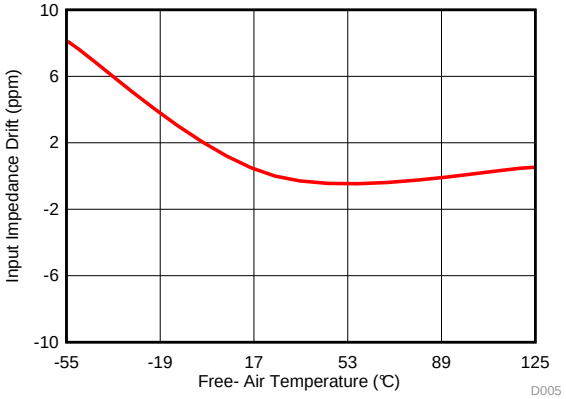


図 2. Input I-V Characteristic



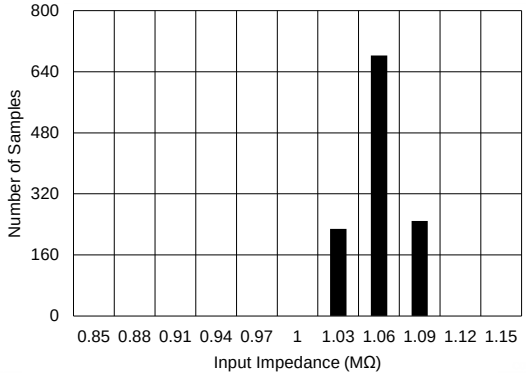
Input range = ±2.5 × V_{REF}

図 3. Input Current vs Temperature



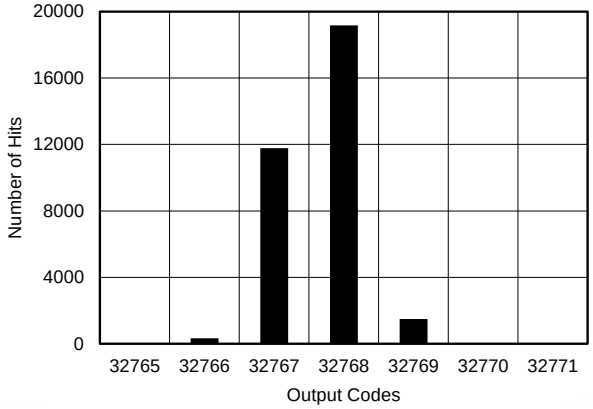
All input ranges

図 4. Input Impedance Variation vs Temperature



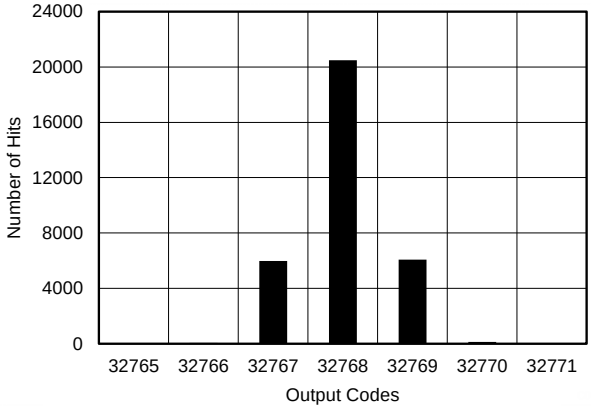
Number of samples = 1160

図 5. Typical Distribution of Input Impedance



Mean = 32768.67, sigma = 0.58, input = 0 V,
range = ±2.5 × V_{REF}

図 6. DC Histogram for Mid-Scale Inputs (±2.5 × V_{REF})

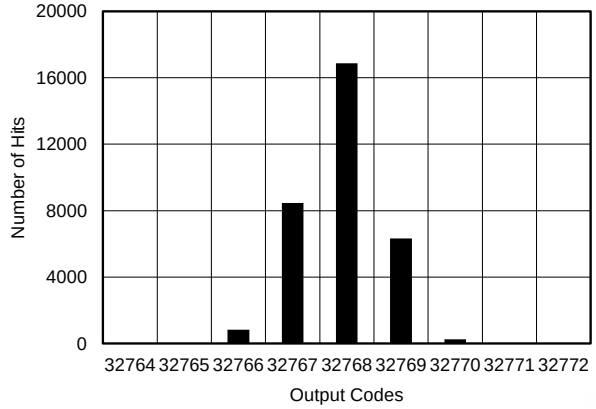


Mean = 32768.60, sigma = 0.63, input = 0 V,
range = ±1.25 × V_{REF}

図 7. DC Histogram for Mid-Scale Inputs (±1.25 × V_{REF})

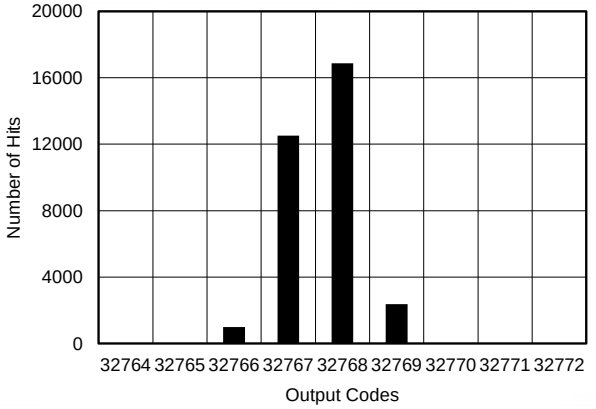
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



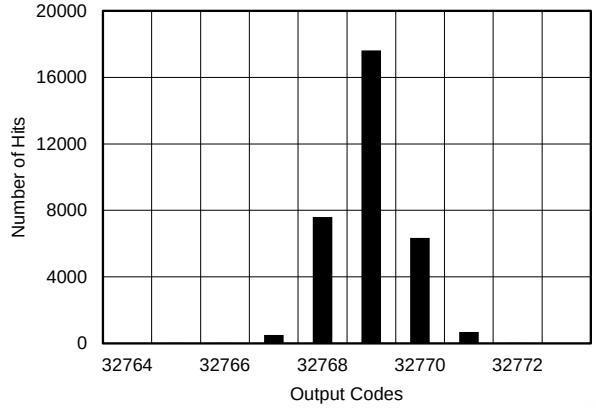
Mean = 32768.8, sigma = 0.76, input = 0 V,
range = ±0.625 × V_{REF}

図 8. DC Histogram for Mid-Scale Inputs (±0.625 × V_{REF})



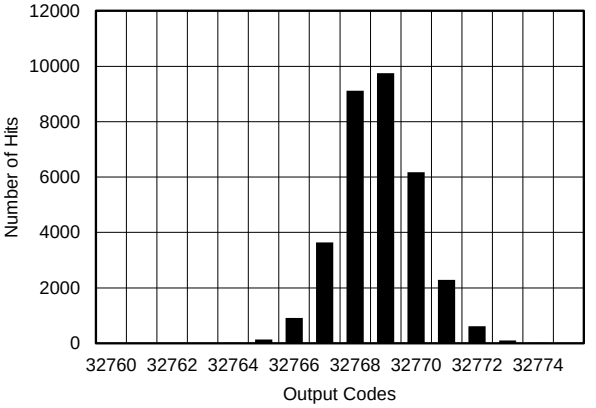
Mean = 32767.75, sigma = 0.65, input = 1.25 × V_{REF},
range = 2.5 × V_{REF}

図 9. DC Histogram for Mid-Scale Inputs (2.5 × V_{REF})



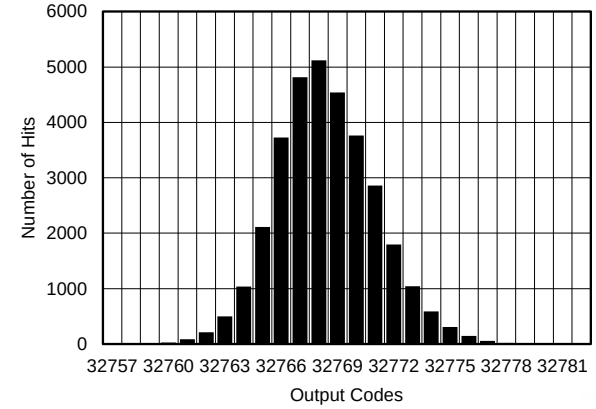
Mean = 32768.2, sigma = 0.75, input = 0.625 × V_{REF},
range = 1.25 × V_{REF}

図 10. DC Histogram for Mid-Scale Inputs (1.25 × V_{REF})



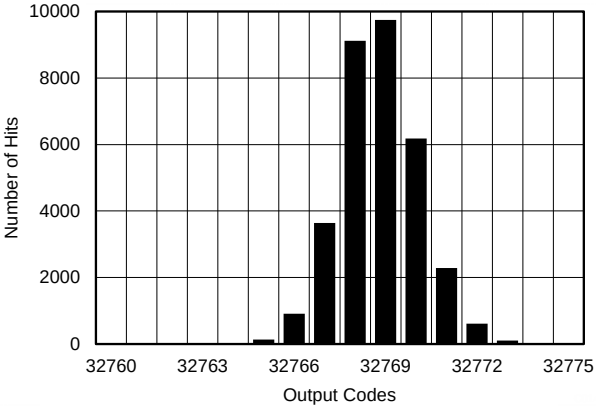
Mean = 32768.5, sigma = 1.30, input = 0 V,
range = ±0.3125 × V_{REF}

図 11. DC Histogram for Mid-Scale Inputs (±0.3125 × V_{REF})



Mean = 32768.5, sigma = 2.68, input = 0 V,
range = ±0.15625 × V_{REF}

図 12. DC Histogram for Mid-Scale Inputs (±0.15625 × V_{REF})

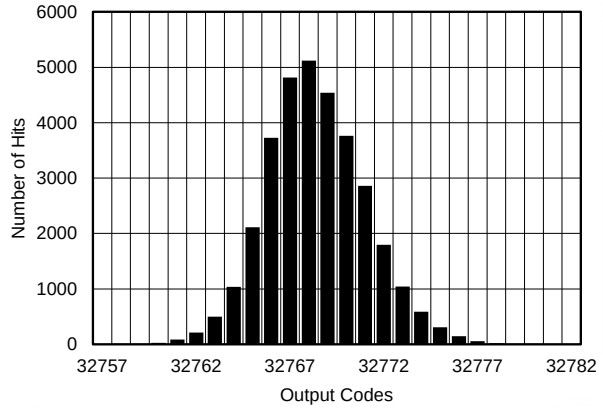


Mean = 32768.5, sigma = 1.30, input = 0.3125 × V_{REF},
range = 0.625 × V_{REF}

図 13. DC Histogram for Mid-Scale Inputs (0.625 × V_{REF})

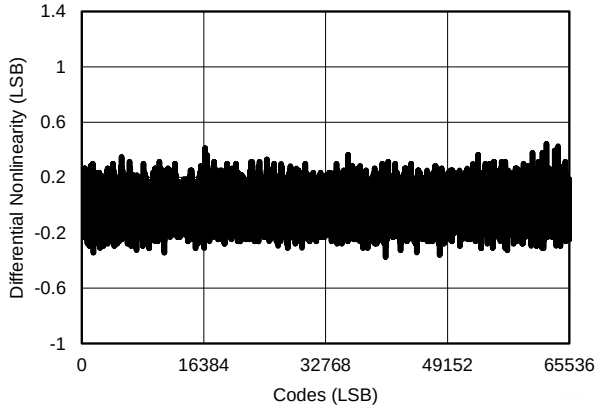
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



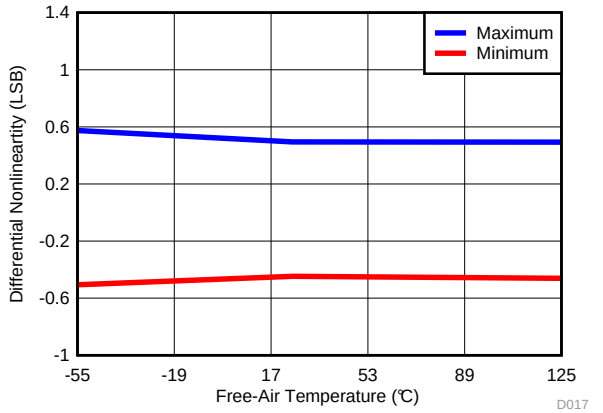
Mean = 32768.5, sigma = 2.68, input = 0.15625 × V_{REF}, range = 0.3125 × V_{REF}

図 14. DC Histogram for Mid-Scale Inputs (0.3125 × V_{REF})



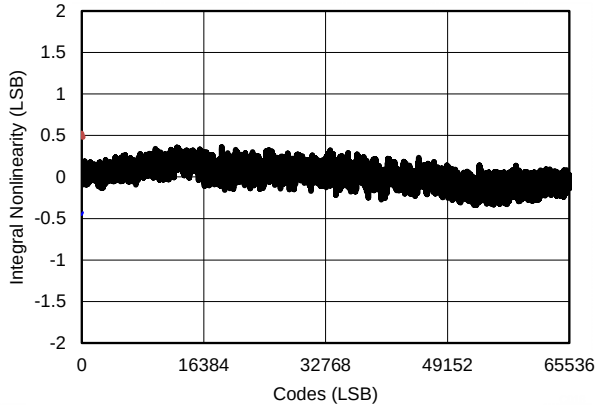
All input ranges

図 15. Typical DNL for All Codes



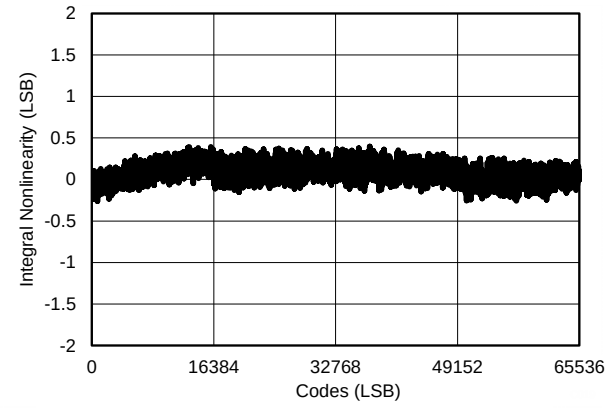
All input ranges

図 16. DNL vs Temperature



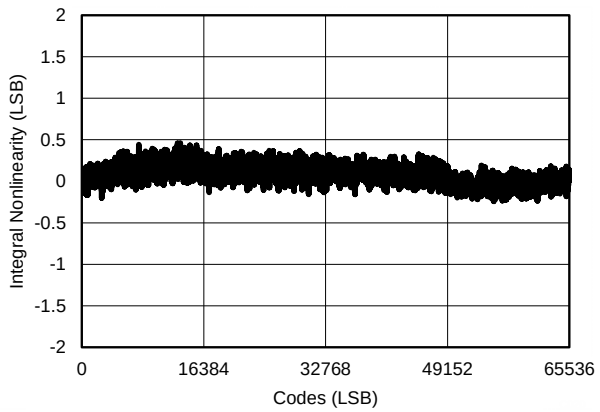
Range = ±2.5 × V_{REF}

図 17. Typical INL for All Codes



Range = ±1.25 × V_{REF}

図 18. Typical INL for All Codes

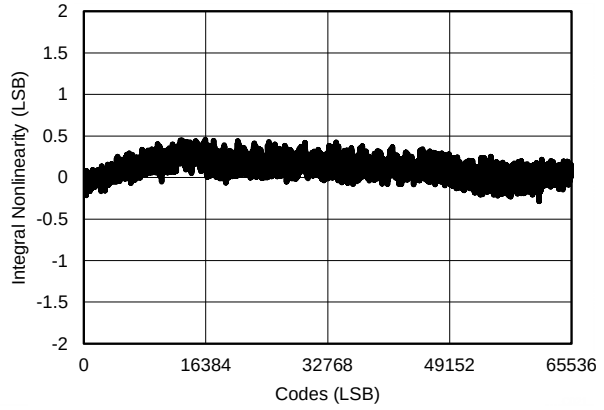


Range = ±0.625 × V_{REF}

図 19. Typical INL for All Codes

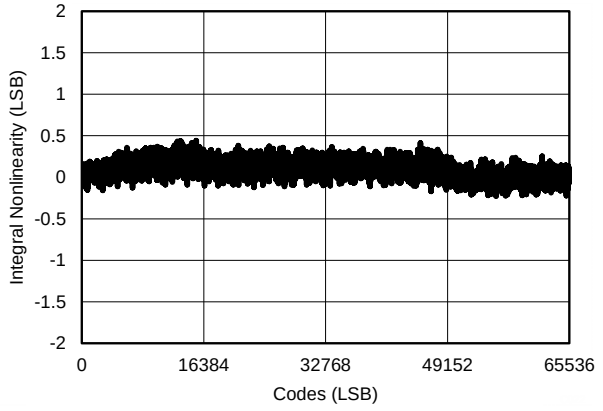
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



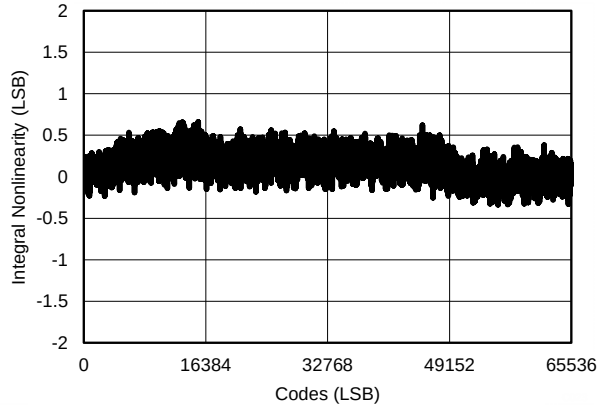
Range = 2.5 × V_{REF}

図 20. Typical INL for All Codes



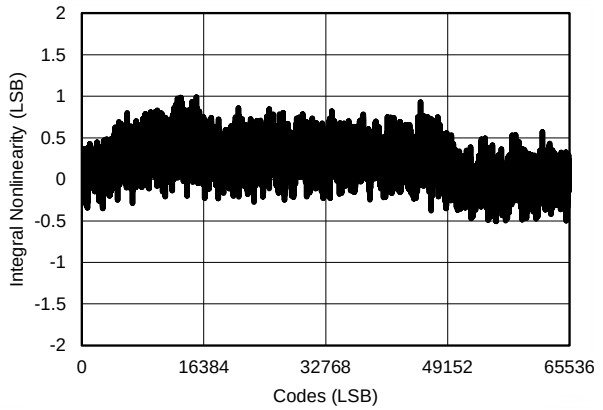
Range = 1.25 × V_{REF}

図 21. Typical INL for All Codes



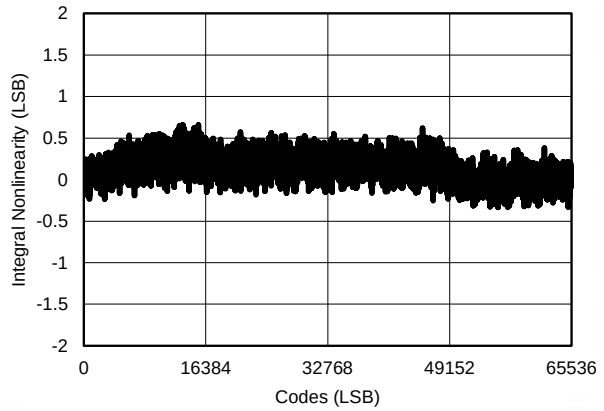
Range = ±0.3125 × V_{REF}

図 22. Typical INL for All Codes



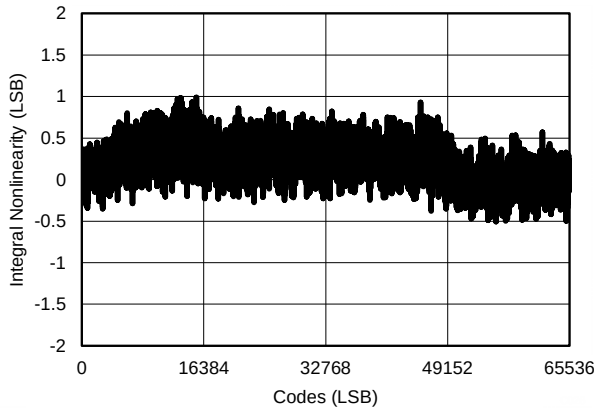
Range = ±0.15625 × V_{REF}

図 23. Typical INL for All Codes



Range = 0.625 × V_{REF}

図 24. Typical INL for All Codes

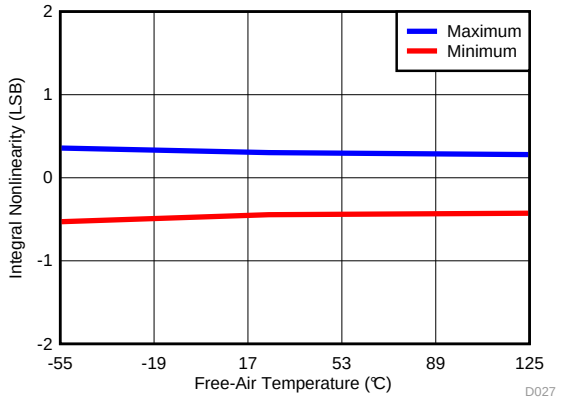


Range = 0.3125 × V_{REF}

図 25. Typical INL for All Codes

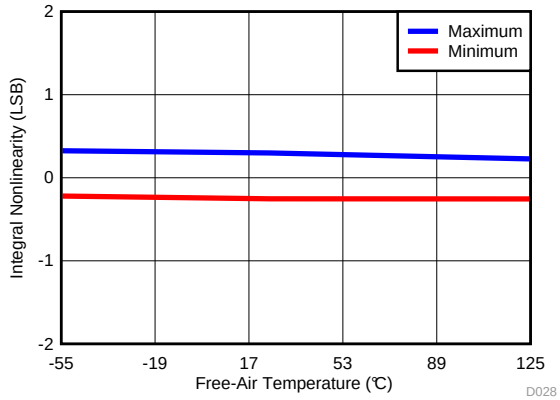
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



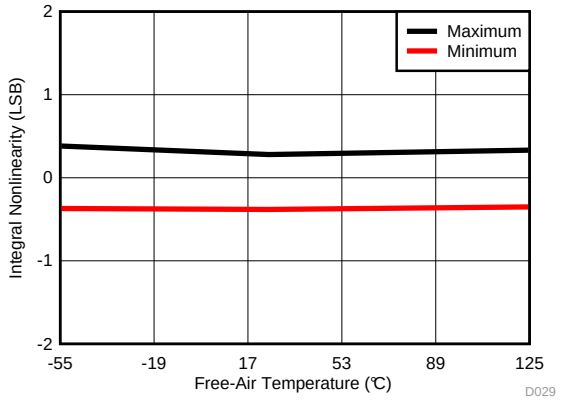
Range = ±2.5 × V_{REF}

図 26. INL vs Temperature (±2.5 × V_{REF})



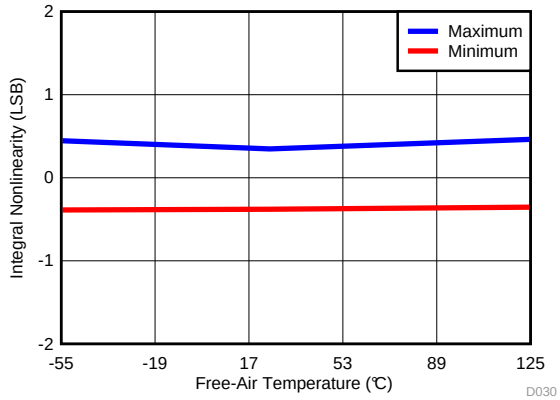
Range = ±1.25 × V_{REF}

図 27. INL vs Temperature (±1.25 × V_{REF})



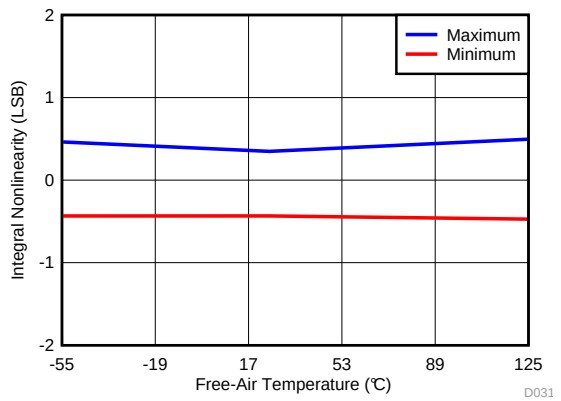
Range = ±0.625 × V_{REF}

図 28. INL vs Temperature (±0.625 × V_{REF})



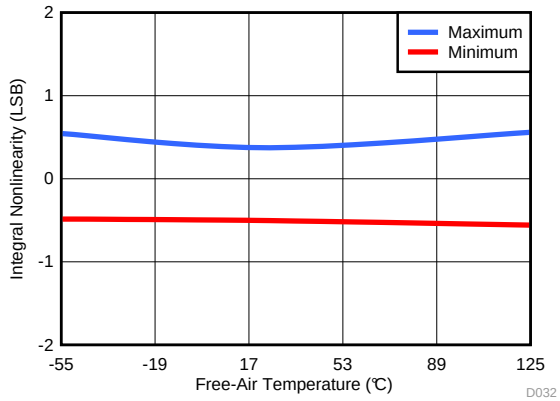
Range = 2.5 × V_{REF}

図 29. INL vs Temperature (2.5 × V_{REF})



Range = 1.25 × V_{REF}

図 30. INL vs Temperature (1.25 × V_{REF})

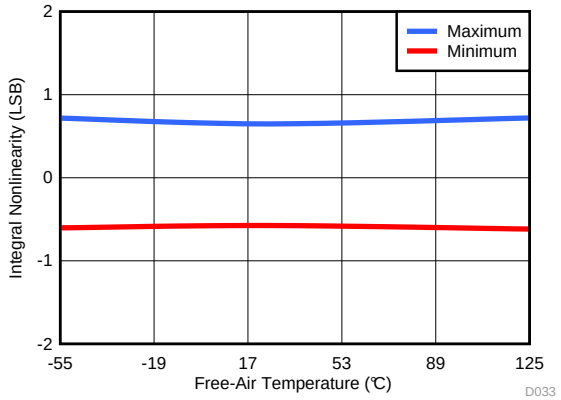


Range = ±0.3125 × V_{REF}

図 31. INL vs Temperature (±0.3125 × V_{REF})

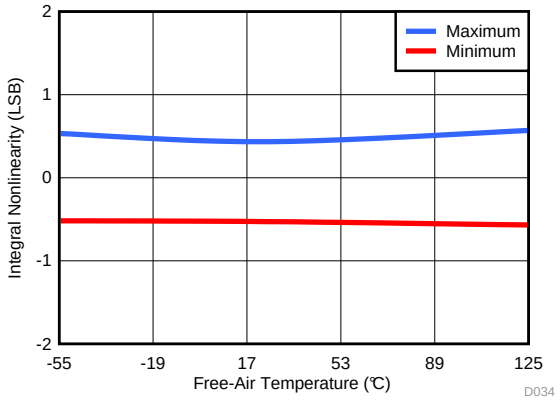
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



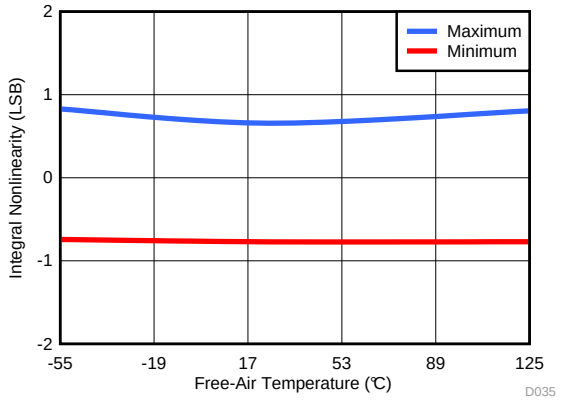
Range = ±0.15625 × V_{REF}

図 32. INL vs Temperature (±0.15625 × V_{REF})



Range = 0.625 × V_{REF}

図 33. INL vs Temperature (0.625 × V_{REF})



Range = 0.3125 × V_{REF}

図 34. INL vs Temperature (0.3125 × V_{REF})

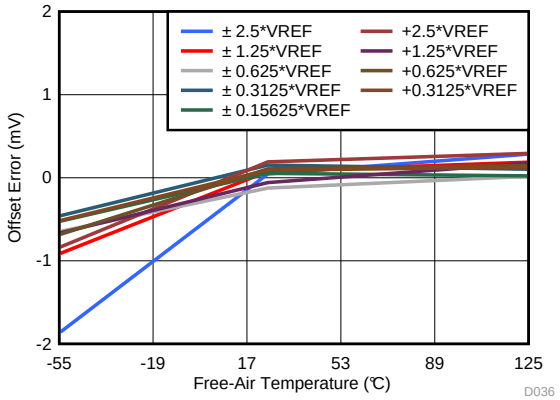
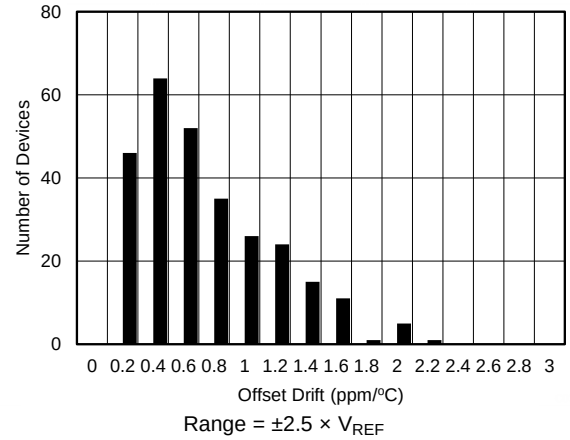
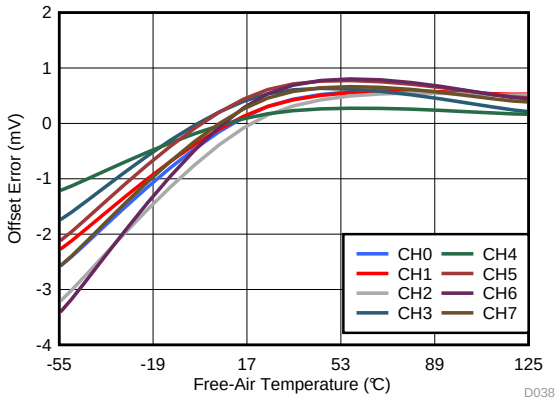


図 35. Offset Error vs Temperature Across Input Ranges



Range = ±2.5 × V_{REF}

図 36. Typical Histogram for Offset Drift



Range = ±2.5 × V_{REF}

図 37. Offset Error vs Temperature Across Channels

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

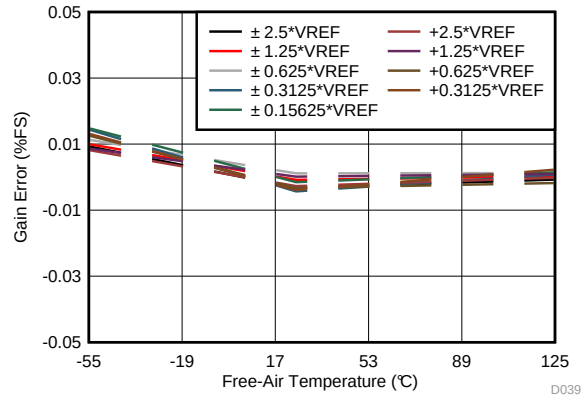
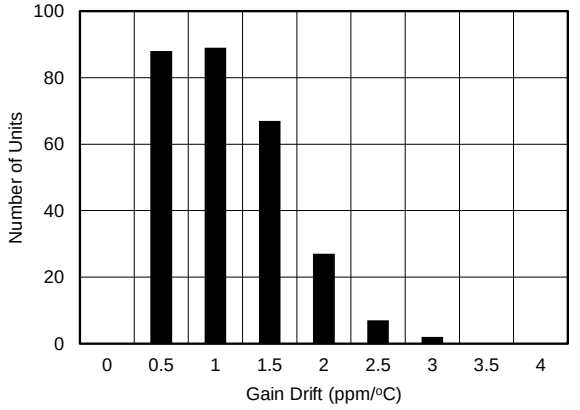
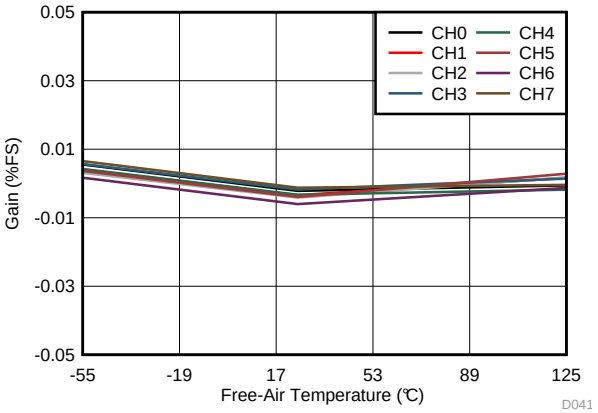


図 38. Gain Error vs Temperature Across Input Ranges



Range = ±2.5 × V_{REF}

図 39. Typical Histogram for Gain Error Drift



Range = ±2.5 × V_{REF}

図 40. Gain Error vs Temperature Across Channels

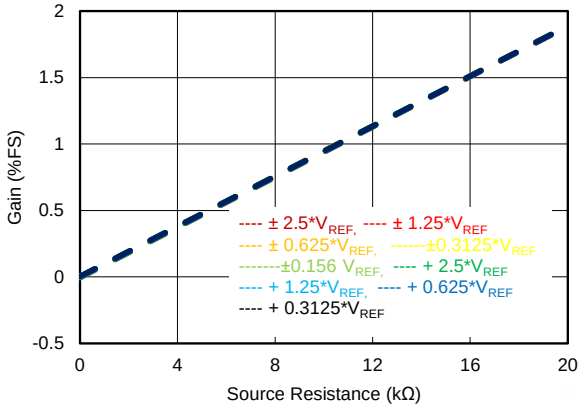
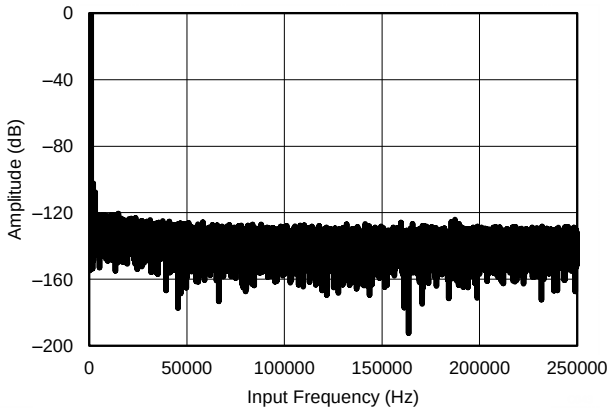
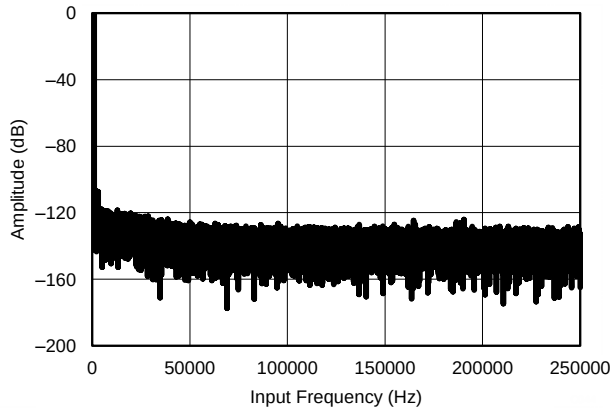


図 41. Gain Error vs External Resistance (R_{EXT})



Number of points = 64k, f_{IN} = 1 kHz, SNR = 92.3 dB, SINAD = 91.9 dB, THD = 101 dB, SFDR = 104 dB

図 42. Typical FFT Plot (±2.5 × V_{REF})

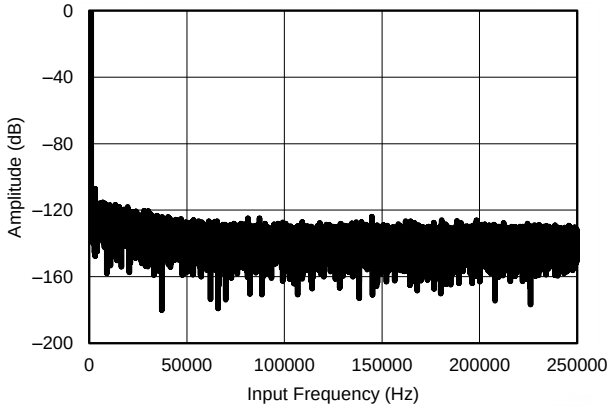


Number of points = 64k, f_{IN} = 1 kHz, SNR = 91.4 dB, SINAD = 91.2 dB, THD = 105 dB, SFDR = 107 dB

図 43. Typical FFT Plot (±1.25 × V_{REF})

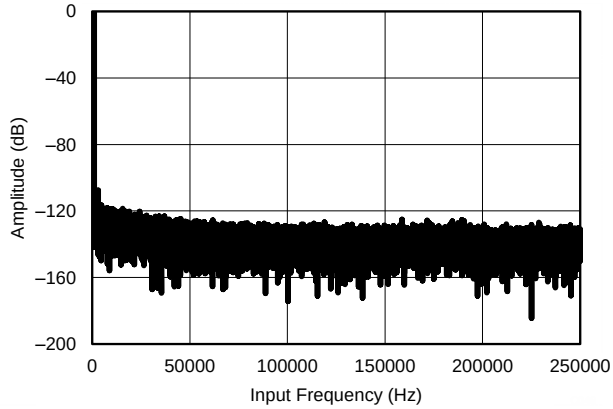
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



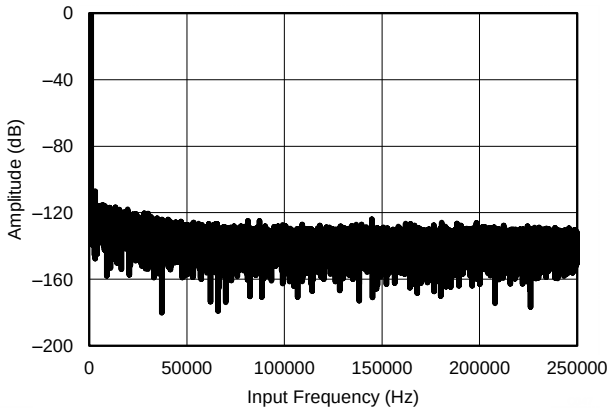
Number of points = 64k, f_{IN} = 1 kHz, SNR = 89.6 dB, SINAD = 89.5 dB, THD = 106 dB, SFDR = 107 dB

図 44. Typical FFT Plot (±0.625 × V_{REF})



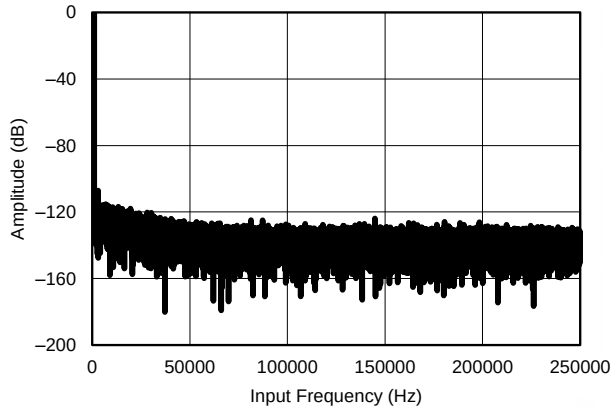
Number of points = 64k, f_{IN} = 1 kHz, SNR = 90.93 dB, SINAD = 90.48 dB, THD = 100 dB, SFDR = 102 dB

図 45. Typical FFT Plot (2.5 × V_{REF})



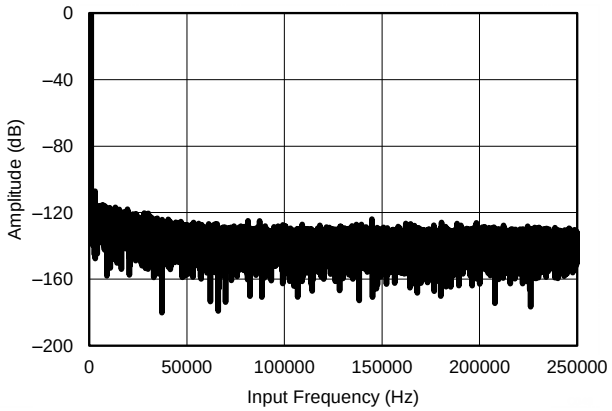
Number of points = 64k, f_{IN} = 1 kHz, SNR = 89.6 dB, SINAD = 89.5 dB, THD = –106 dB, SFDR = 107 dB

図 46. Typical FFT Plot (1.25 × V_{REF})



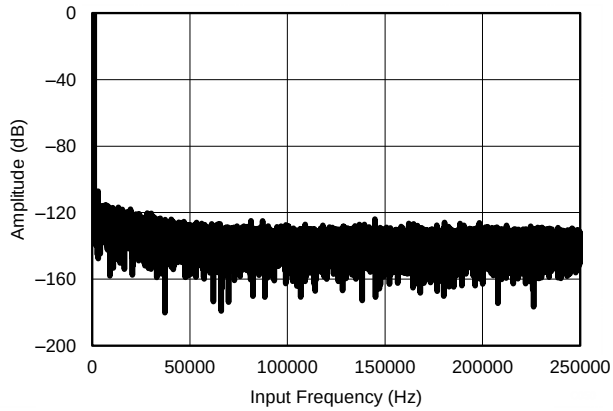
Number of points = 64k, f_{IN} = 1 kHz, SNR = 83.55 dB, SINAD = 83.5 dB, THD = –104 dB, SFDR = 107 dB

図 47. Typical FFT Plot (±0.3125 × V_{REF})



Number of points = 64k, f_{IN} = 1 kHz, SNR = 77.6 dB, SINAD = 77.6 dB, THD = –106 dB, SFDR = 107 dB

図 48. Typical FFT Plot (±0.15625 × V_{REF})

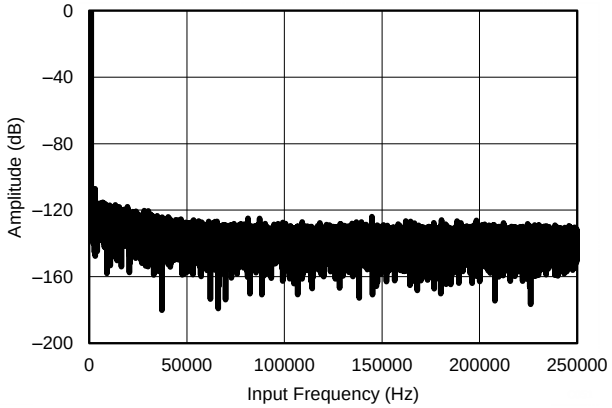


Number of points = 64k, f_{IN} = 1 kHz, SNR = 83.55 dB, SINAD = 83.5 dB, THD = –103 dB, SFDR = 107 dB

図 49. Typical FFT Plot (0.625 × V_{REF})

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



Number of points = 64k, f_{IN} = 1 kHz, SNR = 77.55 dB, SINAD = 77.5 dB, THD = –100 dB, SFDR = 107 dB

図 50. Typical FFT Plot (0.3125 × V_{REF})

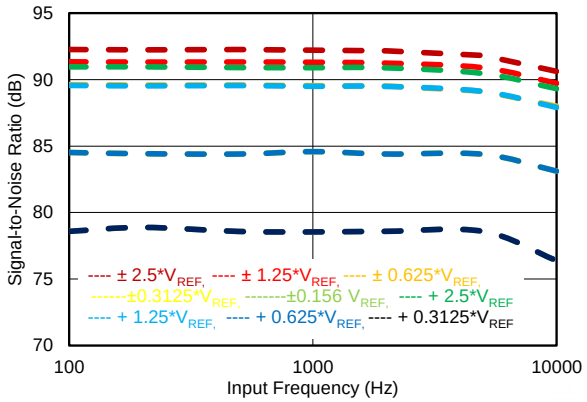
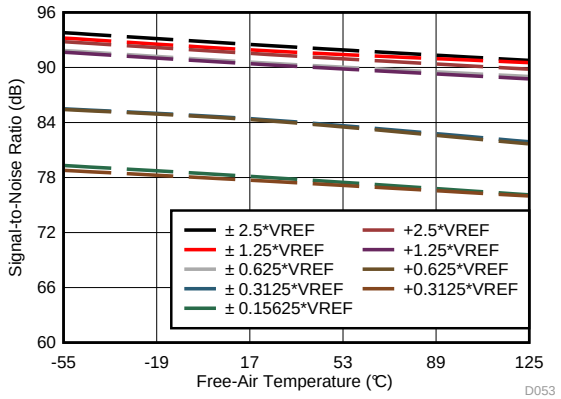


図 51. SNR vs Input Frequency



f_{IN} = 1 kHz

図 52. SNR vs Temperature

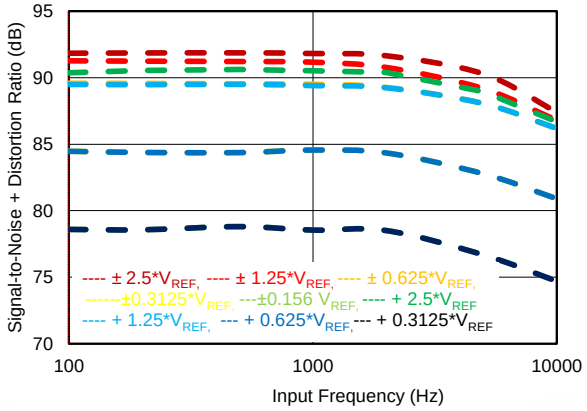
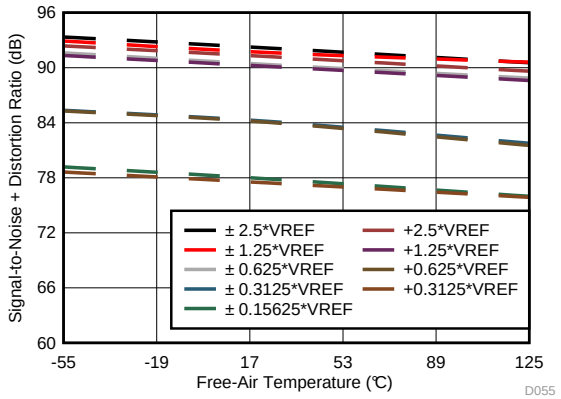


図 53. SINAD vs Input Frequency



f_{IN} = 1 kHz

図 54. SINAD vs Temperature

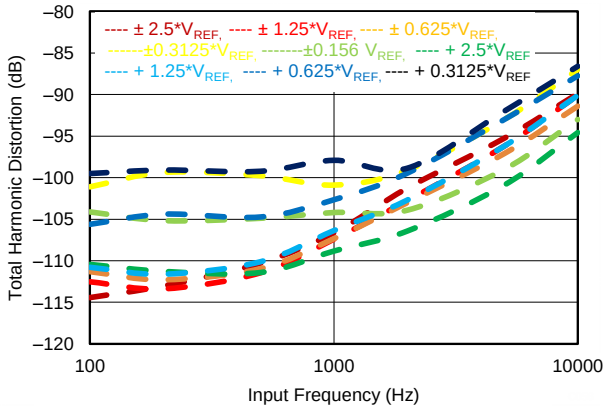
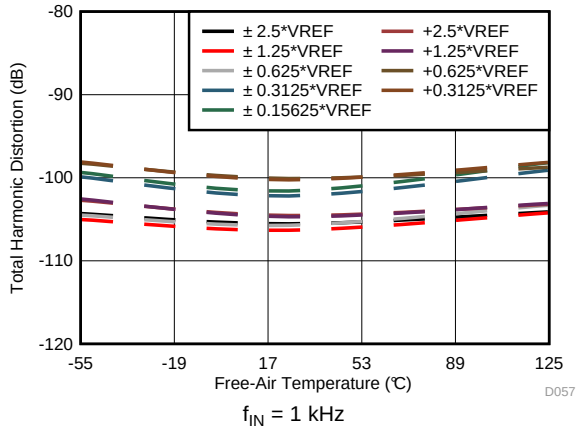


図 55. THD vs Input Frequency

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)



f_{IN} = 1 kHz

図 56. THD vs Temperature

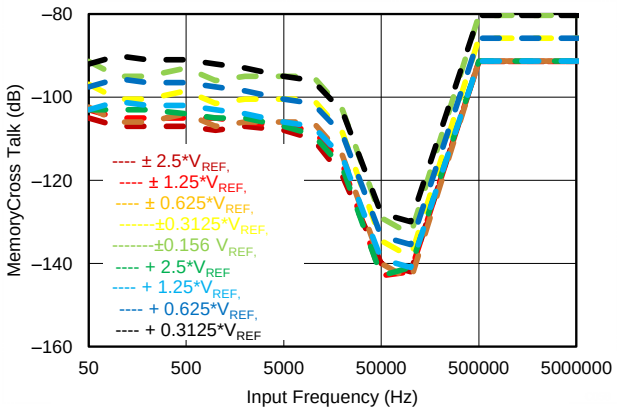


図 57. Memory Crosstalk vs Frequency

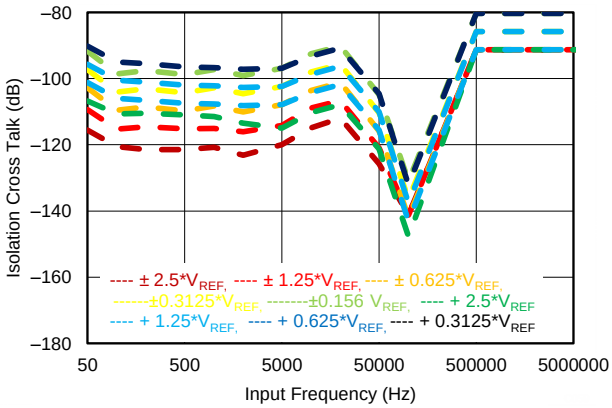
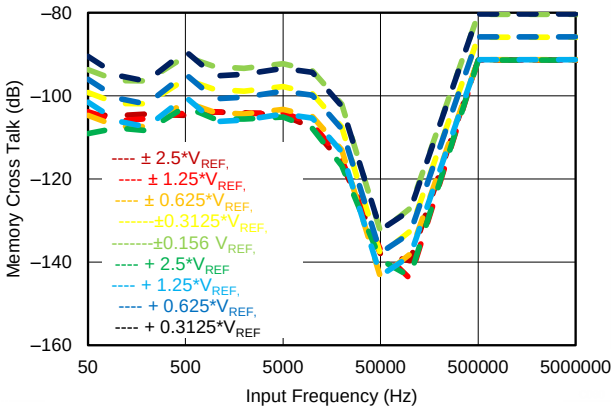
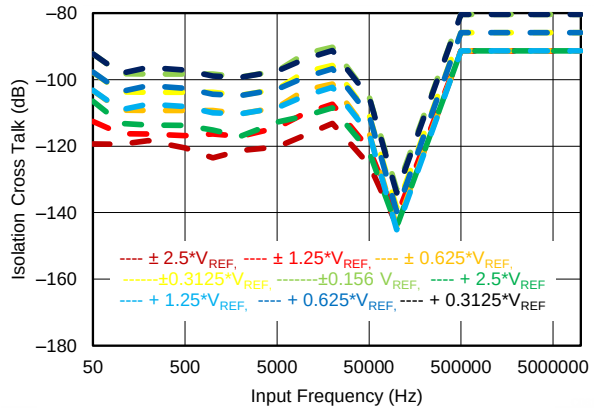


図 58. Isolation Crosstalk vs Frequency



Input = 2 × maximum input voltage

図 59. Memory Crosstalk vs Frequency for Overrange Inputs



Input = 2 × maximum input voltage

図 60. Isolation Crosstalk vs Frequency for Overrange Inputs

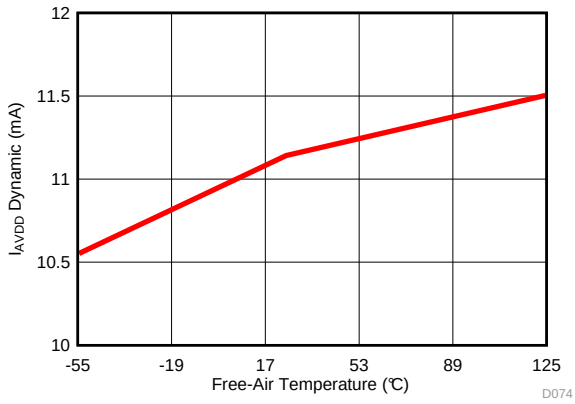


図 61. AVDD Current vs Temperature (f_S = 500 kSPS)

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 4.096 V, and f_{SAMPLE} = 500 kSPS (unless otherwise noted)

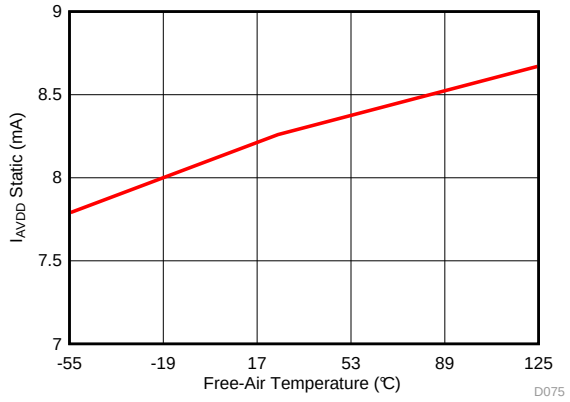


図 62. AVDD Current vs Temperature (During Sampling)

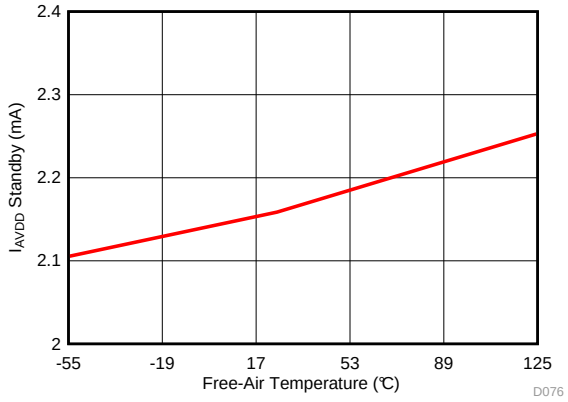


図 63. AVDD Current vs Temperature (STANDBY)

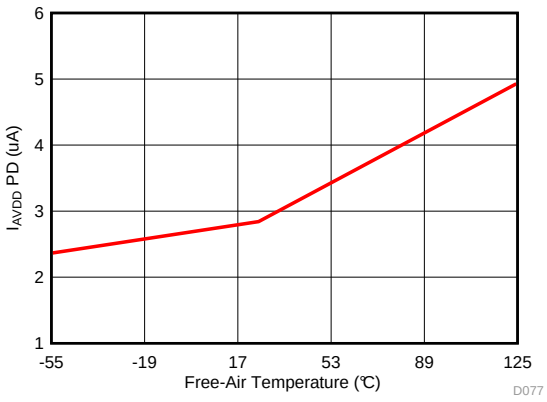


図 64. AVDD Current vs Temperature (Power Down)

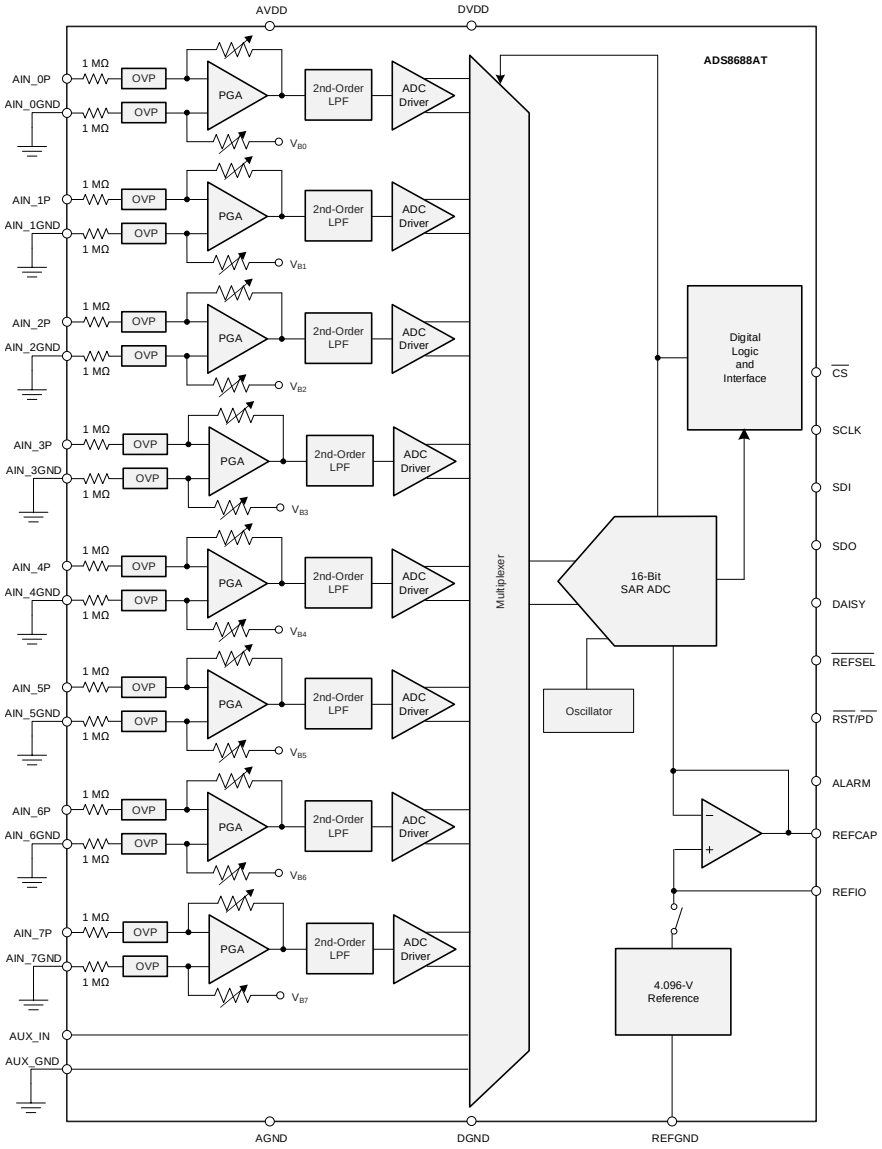
7 Detailed Description

7.1 Overview

The ADS8688AT is a 16-bit data acquisition system with 8-channel analog inputs. Each analog input channel consists of an overvoltage protection circuit, a programmable gain amplifier (PGA), and a second-order, antialiasing filter that conditions the input signal before being fed into an 8-channel analog multiplexer (MUX). The output of the MUX is digitized using a 16-bit analog-to-digital converter (ADC), based on the successive approximation register (SAR) architecture. This overall system can achieve a maximum throughput of 500 kSPS, combined across all channels. The device features a 4.096-V internal reference with a fast-settling buffer and a simple SPI-compatible serial interface with daisy-chain (DAISY) and ALARM features.

The device operates from a single 5-V analog supply and can accommodate true bipolar input signals up to $\pm 2.5 \times V_{REF}$. The device offers a constant 1-MΩ resistive input impedance irrespective of the sampling frequency or the selected input range. The integration of multichannel precision analog front-end circuits with high input impedance and a precision ADC operating from a single 5-V supply offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

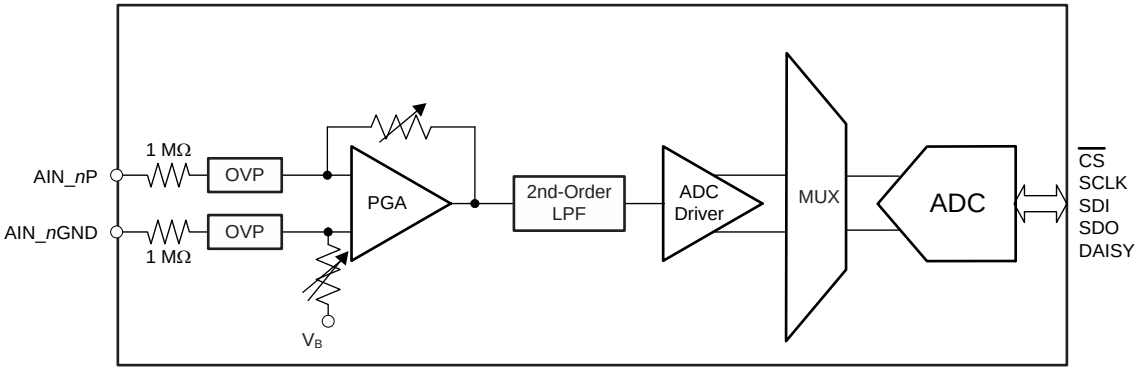
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS8688AT has eight analog input channels, such that the positive inputs AIN_*n*P *(n = 0 to 7)* are the single-ended analog inputs and the negative inputs AIN_*n*GND are tied to GND. 図 65 shows the simplified circuit schematic for each analog input channel, including the input overvoltage protection circuit, PGA, low-pass filter (LPF), high-speed ADC driver, and analog multiplexer.



NOTE: n = 0 to 7.

図 65. Front-End Circuit Schematic for Each Analog Input Channel

The device can support multiple unipolar or bipolar, single-ended input voltage ranges based on the configuration of the program registers. As explained in the *range select registers*, the input voltage range for each analog channel can be configured to bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, ±0.625 × V_{REF}, ±0.3125 × V_{REF}, and ±0.15625 × V_{REF} or unipolar 0 to 2.5 × V_{REF}, 0 to 1.25 × V_{REF}, 0 to 0.625 × V_{REF}, and 0 to 0.3125 × V_{REF}. With the internal or external reference voltage set to 4.096 V, the input ranges of the device can be configured to bipolar ranges of ±10.24 V, ±5.12 V, ±2.56 V, ±1.28 V, and ±0.64 V or unipolar ranges of 0 V to 10.24 V, 0 V to 5.12 V, 0 V to 2.56 V, and 0 V to 1.28 V. Any of these input ranges can be assigned to any analog input channel of the device. For instance, the ±2.5 × V_{REF} range can be assigned to AIN_1P, the ±1.25 × V_{REF} range can be assigned to AIN_2P, the 0 to 2.5 × V_{REF} range can be assigned to AIN_3P, and so forth.

The device samples the voltage difference (AIN_*n*P – AIN_*n*GND) between the selected analog input channel and the AIN_*n*GND pin. The device allows a ±0.1-V range on the AIN_*n*GND pin for all analog input channels. This feature is useful in modular systems where the sensor or signal-conditioning block is further away from the ADC on the board and when a difference in the ground potential of the sensor or signal conditioner from the ADC ground is possible. In such cases, running separate wires from the AIN_*n*GND pin of the device to the sensor or signal-conditioning ground is recommended.

If the analog input pins (AIN_*n*P) to the device are left floating, the output of the ADC corresponds to an internal biasing voltage. The output from the ADC must be considered as invalid if the device is operated with floating input pins. This condition does not cause any damage to the device, which is fully functional when a valid input voltage is applied to the pins.

7.3.2 Analog Input Impedance

Each analog input channel in the device presents a constant resistive impedance of 1 MΩ. The input impedance is independent of either the ADC sampling frequency, the input signal frequency, or range. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage front-end drivers. In most applications, the signal sources or sensor outputs can be directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

In order to maintain the dc accuracy of the system, matching the external source impedance on the AIN_*n*P input pin with an equivalent resistance on the AIN_*n*GND pin is recommended. This matching helps to cancel any additional offset error contributed by the external resistance.

Feature Description (continued)

7.3.3 Input Overvoltage Protection Circuit

The ADS8688AT features an internal overvoltage protection circuit on each of the eight analog input channels. Use these protection circuits as a secondary protection scheme to protect the device. Using external protection devices against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions is highly recommended. 図 66 shows the conceptual block diagram of the internal overvoltage protection (OVP) circuit.

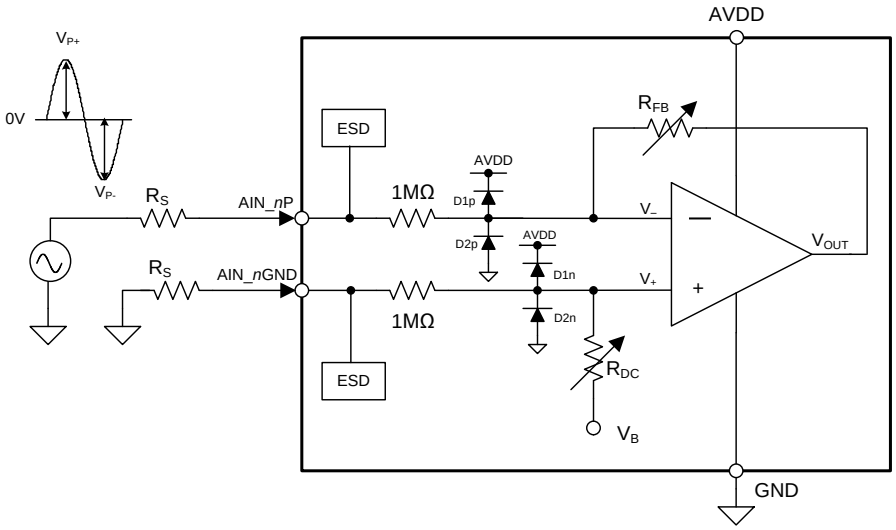


図 66. Input Overvoltage Protection Circuit Schematic

As shown in 図 66, the combination of the 1-MΩ input resistors along with the PGA gain-setting resistors (R_{FB} and R_{DC}) limit the current flowing into the input pins. A combination of antiparallel diodes (D1 and D2) are added on each input pin to protect the internal circuitry and set the overvoltage protection limits.

表 1 explains the various operating conditions for the device when the device is powered on. 表 1 indicates that when the AVDD pin of the device is connected to the proper supply voltage (AVDD = 5 V), the internal overvoltage protection circuit can withstand up to ±20 V on the analog input pins.

表 1. Input Overvoltage Protection Limits When AVDD = 5 V(1)

INPUT CONDITION (V_{OVP} = ±20 V)		TEST CONDITION	ADC OUTPUT	COMMENTS
$\|V_{IN}\| < \|V_{RANGE}\|$	Within operating range	All input ranges	Valid	Device functions as per data sheet specifications
$\|V_{RANGE}\| < \|V_{IN}\| < \|V_{OVP}\|$	Beyond operating range but within overvoltage range	All input ranges	Saturated	ADC output is saturated, but device is internally protected (not recommended for extended time)
$\|V_{IN}\| > \|V_{OVP}\|$	Beyond overvoltage range	All input ranges	Saturated	This usage condition may cause irreversible damage to the device

(1) GND = 0 V, AIN_*n*GND = 0 V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0 Ω.

The results indicated in 表 1 are based on an assumption that the analog input pins are driven by very low impedance sources (R_S is approximately 0 Ω). However, if the sources driving the inputs have higher impedance, the current flowing through the protection diodes reduces further, thereby increasing the OVP voltage range. Higher source impedance results in gain errors and contributes to overall system noise performance.

図 67 shows the voltage versus current response of the internal overvoltage protection circuit when the device is powered on. According to this current-to-voltage (I-V) response, the current flowing into the device input pins is limited by the 1-MΩ input impedance. However, for voltages beyond ±20 V, the internal node voltages surpass the break-down voltage for internal transistors, thus setting the limit for overvoltage protection on the input pins.

The same overvoltage protection circuit also provides protection to the device when the device is not powered on and AVDD is floating. This condition can arise when the input signals are applied before the ADC is fully powered on. 表 2 lists the overvoltage protection limits for this condition.

表 2. Input Overvoltage Protection Limits When AVDD = Floating(1)

INPUT CONDITION (V_{OVP} = ±11 V)		TEST CONDITION	ADC OUTPUT	COMMENTS
$\|V_{IN}\| < \|V_{OVP}\|$	Within overvoltage range	All input ranges	Invalid	Device is not functional but is protected internally by the OVP circuit
$\|V_{IN}\| > \|V_{OVP}\|$	Beyond overvoltage range	All input ranges	Invalid	This usage condition may cause irreversible damage to the device

(1) AVDD = floating, GND = 0 V, AIN_*n*GND = 0 V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0 Ω.

図 68 shows the voltage versus current response of the internal overvoltage protection circuit when the device is not powered on. According to this I-V response, the current flowing into the device input pins is limited by the 1-MΩ input impedance. However, for voltages beyond ±11 V, the internal node voltages surpass the break-down voltage for internal transistors, thus setting the limit for overvoltage protection on the input pins.

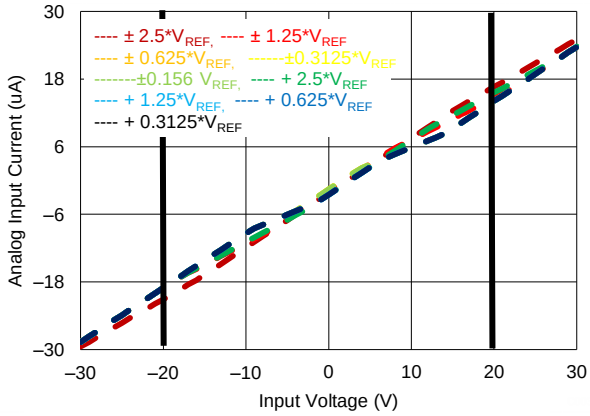


図 67. I-V Curve for an Input OVP Circuit

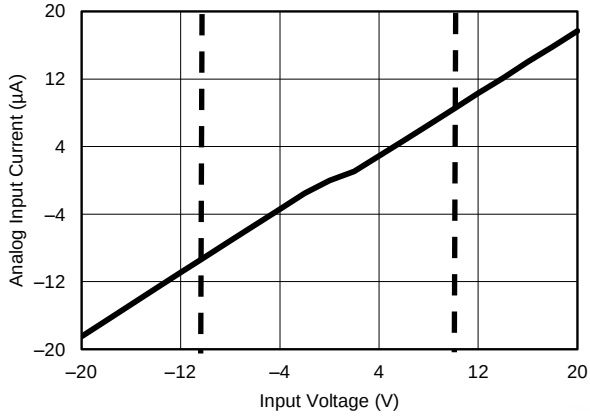


図 68. I-V Curve for an Input OVP Circuit (AVDD = Floating)

7.3.4 Programmable Gain Amplifier (PGA)

The device offers a programmable gain amplifier (PGA) at each individual analog input channel, which converts the original single-ended input signal into a fully differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can be accordingly adjusted by setting the Range_CH*n*[3:0] *(n = 0 to 7)* bits in the program register. The default or power-on state for the Range_CH*n*[3:0] bits is 0000, which corresponds to an input signal range of ±2.5 × V_{REF}. 表 3 lists the various configurations of the Range_CH*n*[3:0] bits for the different analog input voltage ranges.

The PGA uses a very highly matched network of resistors for multiple gain configurations. Matching between these resistors and the amplifiers across all channels is accurately trimmed to keep the overall gain error low across all channels and input ranges.

表 3. Input Range Selection Bits Configuration

ANALOG INPUT RANGE (V)	Range_CH*n*[3:0]			
	BIT 3	BIT 2	BIT 1	BIT 0
±2.5 × V_{REF}	0	0	0	0
±1.25 × V_{REF}	0	0	0	1
±0.625 × V_{REF}	0	0	1	0
±0.3125 × V_{REF}	0	0	1	1
±0.15625 × V_{REF}	1	0	1	1
0 to 2.5 × V_{REF}	0	1	0	1
0 to 1.25 × V_{REF}	0	1	1	0
0 to 0.625 × V_{REF}	0	1	1	1
0 to 0.3125 × V_{REF}	1	1	1	1

7.3.5 Second-Order, Low-Pass Filter (LPF)

In order to mitigate the noise of the front-end amplifiers and gain resistors of the PGA, each analog input channel of the ADS8688AT features a second-order, antialiasing LPF at the output of the PGA. 図 69 and 図 70 show the magnitude and phase response of the analog antialiasing filter, respectively. For maximum performance, the –3-dB cutoff frequency for the antialiasing filter is typically set to 15 kHz. The performance of the filter is consistent across all input ranges supported by the ADC.

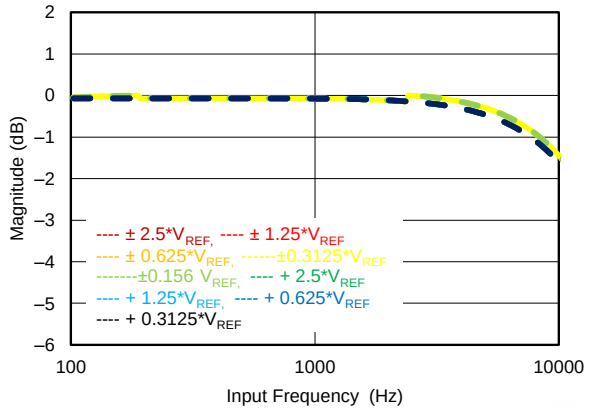


図 69. Second-Order LPF Magnitude Response

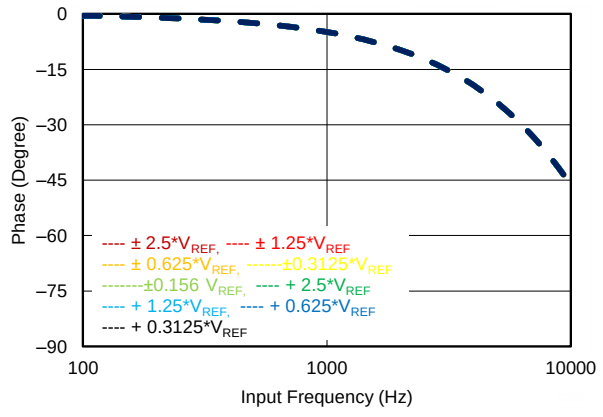


図 70. Second-Order LPF Phase Response

7.3.6 ADC Driver

In order to meet the performance of a 16-bit, SAR ADC at the maximum sampling rate (500 kSPS), the sample-and-hold capacitors at the input of the ADC must be successfully charged and discharged during the acquisition time window. This drive requirement at the inputs of the ADC necessitates the use of a high-bandwidth, low-noise, and stable amplifier buffer. Such an input driver is integrated in the front-end signal path of each analog input channel of the device. During transition from one channel of the multiplexer to another channel, the fast integrated driver ensures that the multiplexer output settles to a 16-bit accuracy within the acquisition time of the ADC, irrespective of the input levels on the respective channels.

7.3.7 Multiplexer (MUX)

The ADS8688AT features an integrated 8-channel analog multiplexer. For each analog input channel, the voltage difference between the positive analog input AIN_*n*P and the negative ground input AIN_*n*GND is conditioned by the analog front-end circuitry before being fed into the multiplexer. The output of the multiplexer is directly sampled by the ADC. The multiplexer in the device can scan these analog inputs in either manual or auto-scan mode, as explained in the *Channel Sequencing Modes* section. In manual mode (MAN_Ch_n), the channel is selected for every sample via a register write; in auto-scan mode (AUTO_RST), the channel number is incremented automatically on every $\overline{CS}$ falling edge after the present channel is sampled. The analog inputs can be selected for an auto scan with register settings (see the *auto-scan sequencing control registers*). The device automatically scans only the selected analog inputs in ascending order.

The maximum overall throughput for the ADS8688AT is specified at 500 kSPS across all channels. The per channel throughput is dependent on the number of channels selected in the multiplexer scanning sequence. For example, the throughput per channel is equal to 250 kSPS if only two channels are selected, but is equal to 125 kSPS per channel if four channels are selected, and so forth.

See 表 7 for command register settings to switch between the auto-scan mode and manual mode for individual analog channels.

7.3.8 Reference

The ADS8688AT can operate with either an internal voltage reference or an external voltage reference using the internal buffer. The internal or external reference selection is determined by an external $\overline{REFSEL}$ pin. The device has a built-in buffer amplifier to drive the actual reference input of the internal ADC core for maximizing performance.

7.3.8.1 Internal Reference

The device has an internal 4.096-V (nominal value) reference. In order to select the internal reference, the REFSEL pin must be tied low or connected to AGND. When the internal reference is used, REFIO (pin 5) becomes an output pin with the internal reference value. 図 71 shows that placing a 10-µF (minimum) decoupling capacitor between the REFIO pin and REFGND (pin 6) is recommended. The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The use of a smaller capacitor value allows higher reference noise in the system, thus degrading SNR and SINAD performance. Do not use the REFIO pin to drive external ac or dc loads because REFIO has limited current output capability. The REFIO pin can be used as a source if followed by a suitable op amp buffer (such as the OPA320).

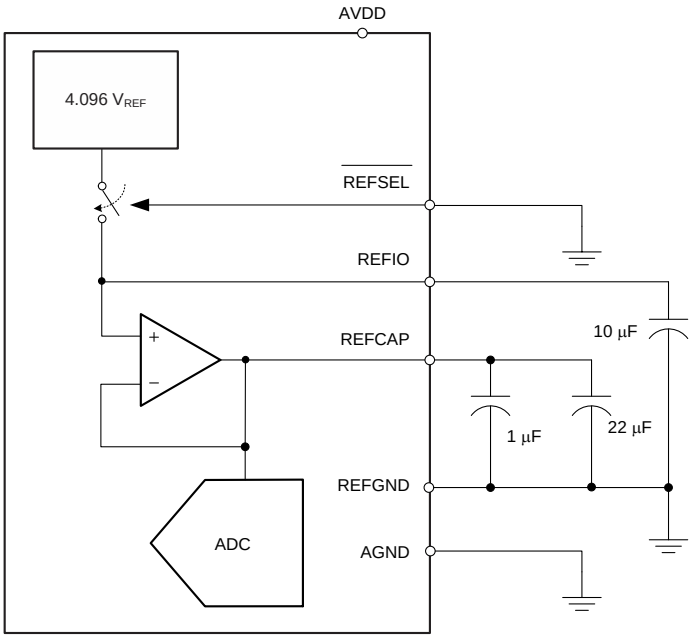


図 71. Device Connections for Using an Internal 4.096-V Reference

The device internal reference is trimmed to a maximum initial accuracy of ±1 mV. The histogram in 図 72 shows the distribution of the internal voltage reference output taken from more than 3300 production devices.

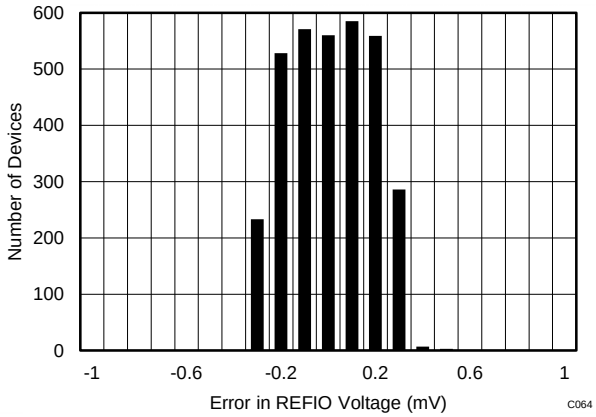


図 72. Internal Reference Accuracy at Room Temperature Histogram

The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical or thermal stress. Heating the device when being soldered to a printed circuit board (PCB) and any subsequent solder reflow is a primary cause for shifts in the V_{REF} value. The main cause of thermal hysteresis is a change in die stress and therefore is a function of the package, die-attach material, and molding compound, as well as the layout of the device itself.

In order to illustrate this effect, 80 devices were soldered using lead-free solder paste with the manufacturer suggested reflow profile, as explained in application report SNOA550. The internal voltage reference output is measured before and after the reflow process and 図 73 shows the typical shift in value. Although all tested units exhibit a positive shift in their output voltages, negative shifts are also possible. The histogram in 図 73 shows the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, which is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is to be exposed to multiple reflows, solder the ADS8688AT in the later pass to minimize device exposure to thermal stress.

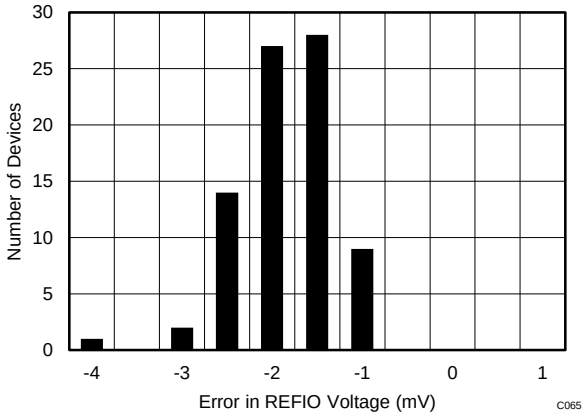


図 73. Solder Heat Shift Distribution Histogram

The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –55°C to +125°C. 図 74 shows the variation of the internal reference voltage across temperature for different values of the AVDD supply voltage. The typical specified value of the reference voltage drift over temperature is 6 ppm/°C (図 75) and the maximum specified temperature drift is equal to 17 ppm/°C.

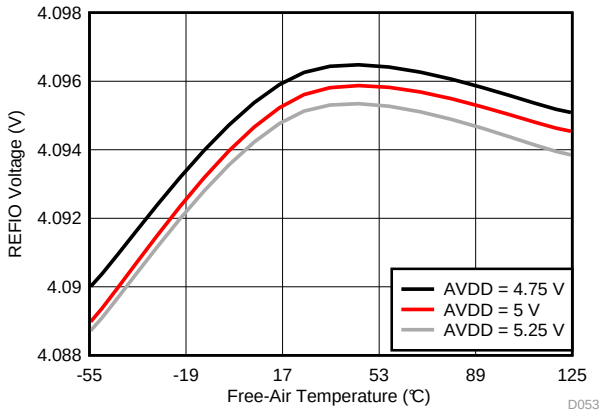
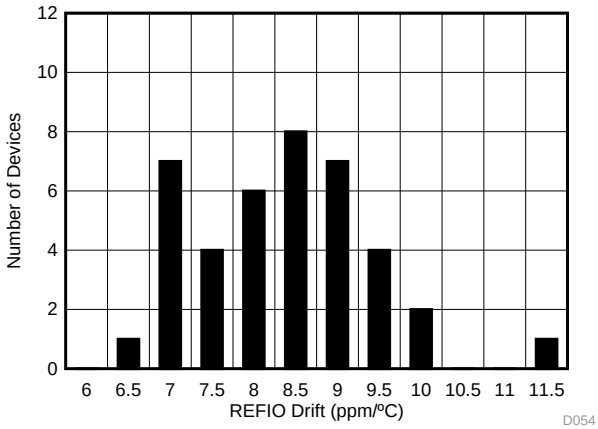


図 74. Variation of the Internal Reference Output (REFIO) Across Supply and Temperature



AVDD = 5 V, number of devices = 30, ΔT = –55°C to +125°C

図 75. Internal Reference Temperature Drift Histogram

7.3.8.2 External Reference

For applications that require a better reference voltage or a common reference voltage for multiple devices, the ADS8688AT offers a provision to use an external reference along with an internal buffer to drive the ADC reference pin. In order to select the external reference mode, either tie the $\overline{\text{REFSEL}}$ pin high or connect this pin to the DVDD supply. In this mode, an external 4.096-V reference must be applied at REFIO (pin 5), which becomes an input pin. Any low-power, low-drift, or small-size external reference can be used in this mode because the internal buffer is optimally designed to handle the dynamic loading on the REFCAP pin, which is internally connected to the ADC reference input. The output of the external reference must be appropriately filtered to minimize the resulting effect of the reference noise on system performance. 図 76 shows a typical connection diagram for this mode.

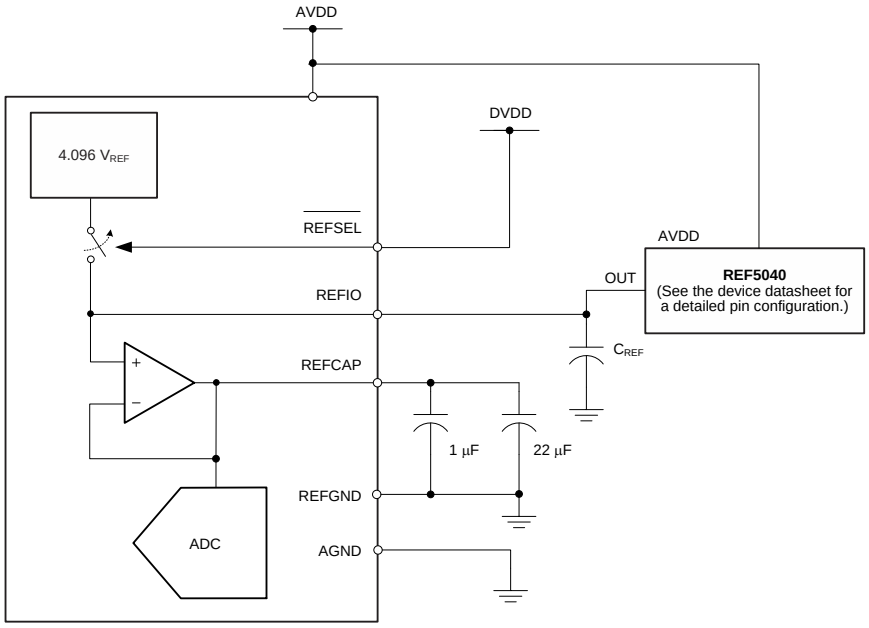


図 76. Device Connections for Using an External 4.096-V Reference

The output of the internal reference buffer appears at the REFCAP pin. A minimum capacitance of 10 µF must be placed between REFCAP (pin 7) and REFGND (pin 6). Place another capacitor of 1 µF as close to the REFCAP pin as possible for decoupling high-frequency signals. Do not use the internal buffer to drive external ac or dc loads because of the limited current output capability of this buffer.

The performance of the internal buffer output is very stable across the entire operating temperature range of –55°C to +125°C. 図 77 shows the variation in the REFCAP output across temperature for different values of the AVDD supply voltage. The typical specified value of the reference buffer drift over temperature is 0.6 ppm/°C (図 78) and the maximum specified temperature drift is equal to 4.5 ppm/°C.

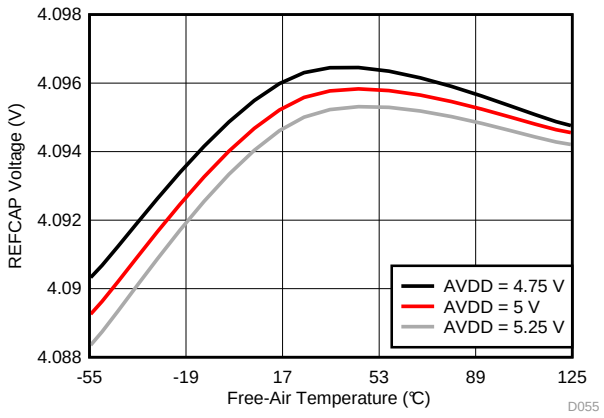
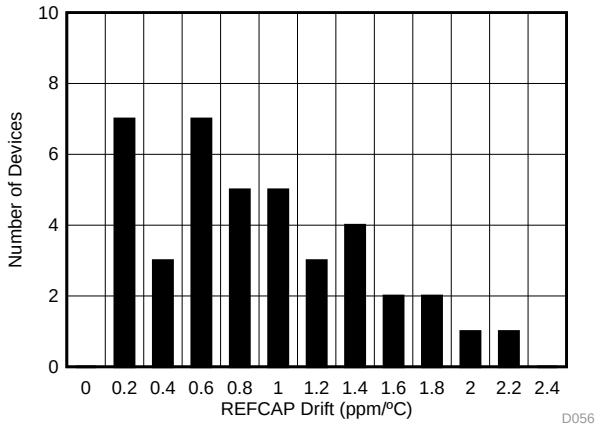


図 77. Variation of the Reference Buffer Output (REFCAP) vs Supply and Temperature



AVDD = 5 V, number of devices = 30, ΔT = –55°C to 125°C

図 78. Reference Buffer Temperature Drift Histogram

7.3.9 Auxiliary Channel

The device includes a single-ended auxiliary input channel (AUX_IN and AUX_GND). The AUX channel provides direct interface to an internal, high-precision, 16-bit ADC through the multiplexer because this channel does not include the front-end analog signal conditioning that the other analog input channels have. The AUX channel supports a single unipolar input range of 0 V to V_{REF} because there is no front-end PGA. The input signal on the AUX_IN pin can vary from 0 V to V_{REF}, whereas the AUX_GND pin must be tied to AGND.

When a conversion is initiated, the voltage between these pins is sampled directly on an internal sampling capacitor (75 pF, typical). The input current required to charge the sampling capacitor is determined by several factors, including the sampling rate, input frequency, and source impedance. For slow applications that use a low-impedance source, the inputs of the AUX channel can be directly driven. When the throughput, input frequency, or the source impedance increases, a driving amplifier must be used at the input to achieve good ac performance from the AUX channel. Some key requirements of the driving amplifier are discussed in the *Input Driver for the AUX Channel* section.

The AUX channel in the ADS8688AT offers a true 16-bit performance with no missing codes. 図 79 and 図 80 show some typical performance characteristics of the AUX channel.

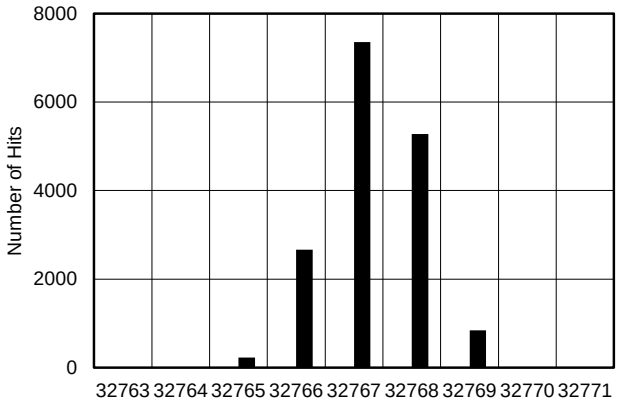


図 79. DC Histogram for Mid-Scale Input (AUX Channel)

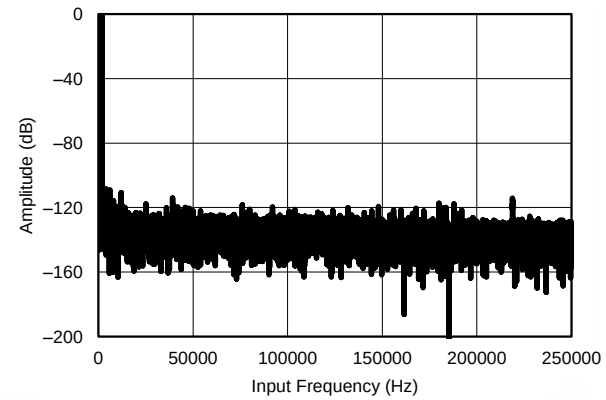


図 80. Typical FFT Plot (AUX Channel)

7.3.9.1 Input Driver for the AUX Channel

For applications that use the AUX input channels at high throughput and high input frequency, a driving amplifier with low output impedance is required to meet the ac performance of the internal 16-bit ADC. Some key specifications of the input driving amplifier are discussed below:

- *Small-signal bandwidth.* The small-signal bandwidth of the input driving amplifier must be much higher than the bandwidth of the AUX input to ensure that there is no attenuation of the input signal resulting from the bandwidth limitation of the amplifier. In a typical data acquisition system, a low cut-off frequency, antialiasing filter is used at the inputs of a high-resolution ADC. The amplifier driving the antialiasing filter must have a low closed-loop output impedance for stability, thus implying a higher gain bandwidth for the amplifier. Higher small-signal bandwidth also minimizes the harmonic distortion at higher input frequencies. In general, 式 1 can be uses as a basis to calculate the amplifier bandwidth requirements.

$$GBW \geq 4 \times f_{-3\,dB} \quad (1)$$

  where:
  - f_{-3dB} is the 3-dB bandwidth of the RC filter

- *Distortion.* In order to achieve the distortion performance of the AUX channel, the distortion of the input driver (as shown in 式 2) must be at least 10 dB lower than the specified distortion of the internal ADC.

$$THD_{AMP} \leq THD_{ADC} - 10(dB) \quad (2)$$

- *Noise.* Careful considerations must be made to select a low-noise, front-end amplifier in order to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. As 式 3 explains, noise from the input driver circuit is band-limited by the low cut-off frequency of the input antialiasing filter.

$$N_G \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (3)$$

where:

- $V_{1\,/\,f\_AMP\_PP}$ is the peak-to-peak flicker noise
- e_{n_RMS} is the amplifier broadband noise density in nV/$\sqrt{Hz}$
- N_G is the noise gain of the front-end circuit, which is equal to 1 in a buffer configuration

7.3.10 ADC Transfer Function

The ADS8688AT is a multichannel device that supports single-ended, bipolar, and unipolar input ranges on all input channels. The output of the device is in straight binary format for both bipolar and unipolar input ranges. The format for the output codes is the same across all analog channels.

図 81 shows the ideal transfer characteristic for each ADC channel for all input ranges. The full-scale range (FSR) for each input signal is equal to the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The LSB size is equal to FSR / 2^{16} = FSR / 65536 because the resolution of the ADC is 16 bits. For a reference voltage of V_{REF} = 4.096 V, 表 4 lists the LSB values corresponding to the different input ranges.

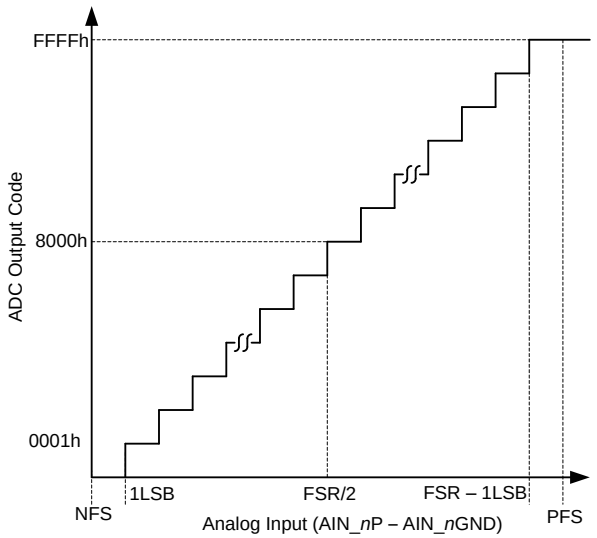


図 81. 16-Bit ADC Transfer Function (Straight-Binary Format)

表 4. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096 V)

INPUT RANGE (V)	POSITIVE FULL-SCALE (V)	NEGATIVE FULL-SCALE (V)	FULL-SCALE RANGE (V)	LSB (µV)
±2.5 × V_{REF}	10.24	–10.24	20.48	312.50
±1.25 × V_{REF}	5.12	–5.12	10.24	156.25
±0.625 × V_{REF}	2.56	–2.56	5.12	78.125
±0.3125 × V_{REF}	1.28	–1.28	2.56	39.0625
±0.15625 × V_{REF}	0.64	–0.64	1.28	19.53125
0 to 2.5 × V_{REF}	10.24	0	10.24	156.25
0 to 1.25 × V_{REF}	5.12	0	5.12	78.125
0 to 0.625 × V_{REF}	2.56	0	2.56	39.0625
0 to 0.3125 × V_{REF}	1.28	0	1.28	19.53125

7.3.11 Alarm Feature

The device has an active-high ALARM output on pin 35. The ALARM signal is synchronous and changes its state on the 16th falling edge of the SCLK signal. A high level on ALARM indicates that the alarm flag has tripped on one or more channels of the device. This pin can be wired to interrupt the host input. When an ALARM interrupt is received, the alarm flag registers are read to determine which channels have an alarm. The device features independently programmable alarms for each channel. There are two alarms per channel (a low and a high alarm) and each alarm threshold has a separate hysteresis setting.

The ADS8688AT sets a high alarm when the digital output for a particular channel exceeds the high alarm upper limit [high alarm threshold (T) + hysteresis (H)]. The alarm resets when the digital output for the channel is less than or equal to the high alarm lower limit (high alarm T – H – 2). 図 82 shows this function.

Similarly, the lower alarm is triggered when the digital output for a particular channel falls below the low alarm lower limit (low alarm threshold T – H – 1). The alarm resets when the digital output for the channel is greater than or equal to the low alarm higher limit (low alarm T + H + 1). 図 83 shows this function.

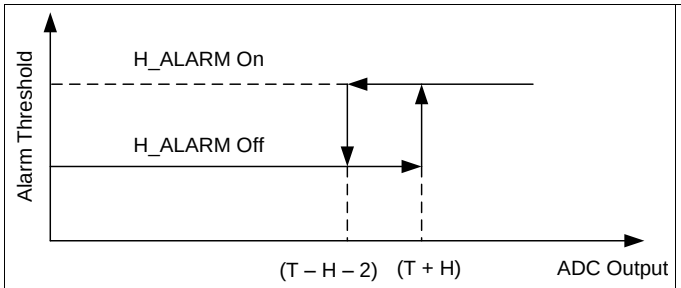


図 82. High-ALARM Hysteresis

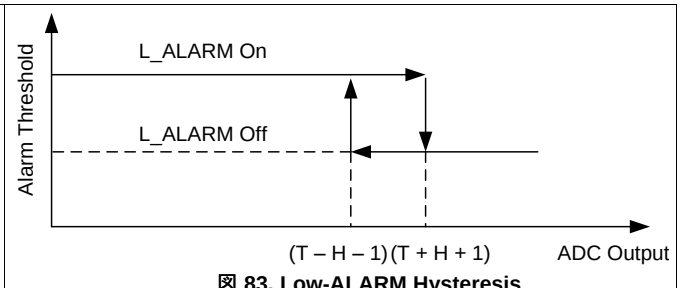


図 83. Low-ALARM Hysteresis

図 84 depicts a functional block diagram for a single-channel alarm. There are two flags for each high and low alarm: active alarm flag and tripped alarm flag; see the alarm flag registers for more details. The active alarm flag is triggered when an alarm condition is encountered for a particular channel; the active alarm flag resets when the alarm shuts off. A tripped alarm flag sets an alarm condition in the same manner as for an active alarm flag. However, the tripped alarm flag remains latched and resets only when the appropriate alarm flag register is read.

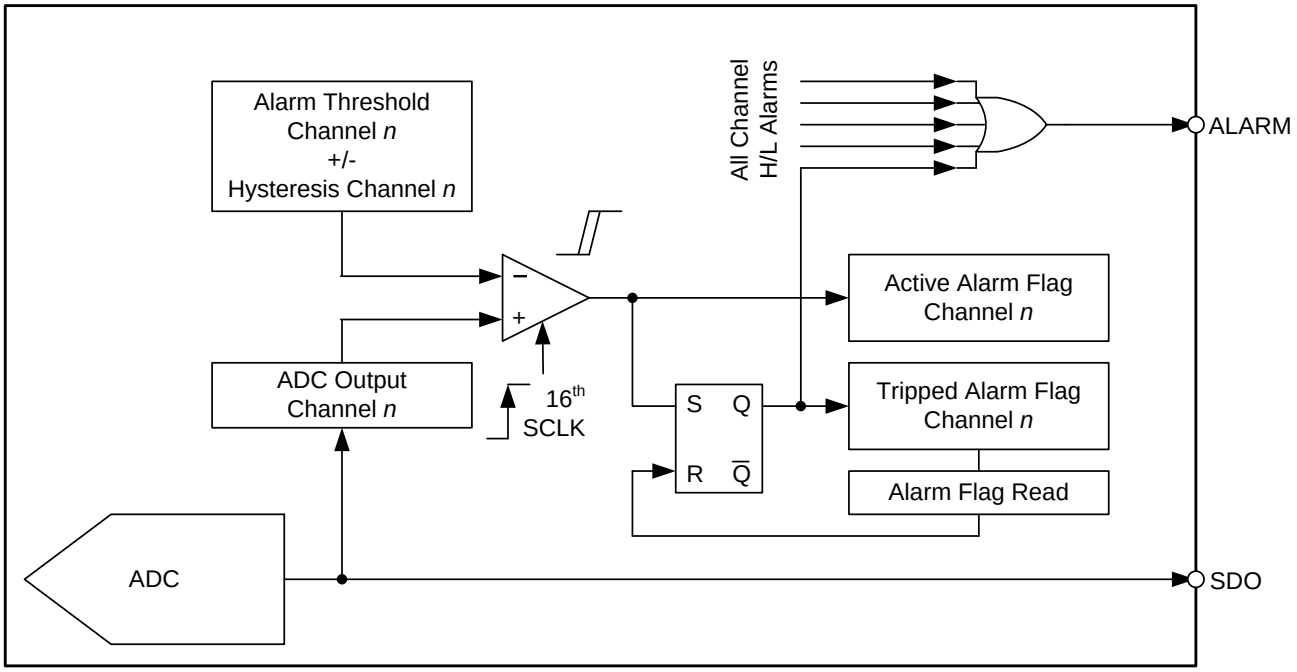


図 84. Alarm Functionality Schematic

7.4 Device Functional Modes

7.4.1 Device Interface

7.4.1.1 Digital Pin Description

図 85 shows the digital data interface for the ADS8688AT.

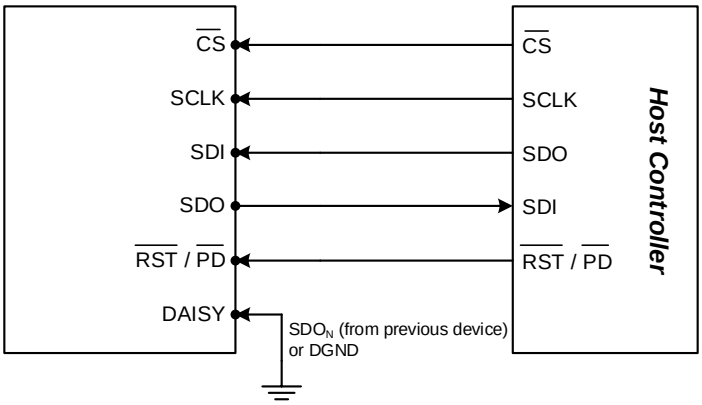


図 85. Pin Configuration for the Digital Interface

The signals shown in 図 85 are summarized as follows:

7.4.1.1.1 $\overline{CS}$ (Input)

$\overline{CS}$ indicates an active-low, chip-select signal. $\overline{CS}$ is also used as a control signal to trigger a conversion on the falling edge. Each data frame begins with the falling edge of the $\overline{CS}$ signal. The analog input channel to be converted during a particular frame is selected in the previous frame. On the $\overline{CS}$ falling edge, the devices sample the input signal from the selected channel and a conversion is initiated using the internal clock. The device settings for the next data frame can be input during this conversion process. When the $\overline{CS}$ signal is high, the ADC is considered to be in an idle state.

7.4.1.1.2 SCLK (Input)

This pin indicates the external clock input for the data interface. All synchronous accesses to the device are timed with respect to the falling edges of the SCLK signal.

7.4.1.1.3 SDI (Input)

SDI is the serial data input line. SDI is used by the host processor to program the internal device registers for device configuration. At the beginning of each data frame, the $\overline{CS}$ signal goes low and the data on the SDI line are read by the device at every falling edge of the SCLK signal for the next 16 SCLK cycles. Any changes made to the device configuration in a particular data frame are applied to the device on the subsequent falling edge of the $\overline{CS}$ signal.

7.4.1.1.4 SDO (Output)

SDO is the serial data output line. SDO is used by the device to output conversion data. The size of the data output frame varies depending on the register setting for the SDO format; see 表 14. A low level on $\overline{CS}$ releases the SDO pin from the Hi-Z state. SDO is kept low for the first 15 SCLK falling edges. The MSB of the output data stream is clocked out on SDO on the 16th SCLK falling edge, followed by the subsequent data bits on every falling edge thereafter. The SDO line goes low after the entire data frame is output and goes to a Hi-Z state when $\overline{CS}$ goes high.

Device Functional Modes (continued)

7.4.1.1.5 DAISY (Input)

DAISY is a serial input pin. When multiple devices are connected in daisy-chain mode, as illustrated in 図 88, the DAISY pin of the first device in the chain is connected to GND. The DAISY pin of every subsequent device is connected to the SDO output pin of the previous device, and the SDO output of the last device in the chain goes to the SDI of the host processor. If an application uses a stand-alone device, the DAISY pin is connected to GND.

7.4.1.1.6 $\overline{\text{RST}}/\overline{\text{PD}}$ (Input)

$\overline{\text{RST}}/\overline{\text{PD}}$ is a dual-function pin. 図 86 shows the timing of this pin and 表 5 explains the usage of this pin.

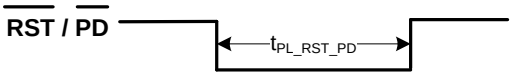


図 86. $\overline{\text{RST}}/\overline{\text{PD}}$ Pin Timing

表 5. $\overline{\text{RST}}/\overline{\text{PD}}$ Pin Functionality

CONDITION	DEVICE MODE
40 ns < $t_{PL\_RST\_PD}$ ≤ 100 ns	The device is in RST mode and does not enter PWR_DN mode.
100 ns < $t_{PL\_RST\_PD}$ < 400 ns	The device is in RST mode and may or may not enter PWR_DN mode. This setting is not recommended.
$t_{PL\_RST\_PD}$ ≥ 400 ns	The device enters PWR_DN mode and the program registers are reset to default value.

The device can be placed into power-down (PWR_DN) mode by pulling the $\overline{\text{RST}}/\overline{\text{PD}}$ pin to a logic low state for at least 400 ns. The $\overline{\text{RST}}/\overline{\text{PD}}$ pin is asynchronous to the clock; thus, $\overline{\text{RST}}/\overline{\text{PD}}$ can be triggered at any time regardless of the status of other pins (including the analog input channels). When the device is in power-down mode, any activity on the digital input pins (apart from the $\overline{\text{RST}}/\overline{\text{PD}}$ pin) is ignored.

The program registers in the device can be reset to their default values (RST) by pulling the $\overline{\text{RST}}/\overline{\text{PD}}$ pin to a logic low state for no longer than 100 ns. This input is asynchronous to the clock. When $\overline{\text{RST}}/\overline{\text{PD}}$ is pulled back to a logic high state, the device is placed in normal mode. One valid write operation must be executed on the program register in order to configure the device, followed by an appropriate command (AUTO_RST or MAN) to initiate conversions.

When the $\overline{\text{RST}}/\overline{\text{PD}}$ pin is pulled back to a logic high level, the device wakes-up in a default state in which the program registers are reset to their default values.

7.4.1.2 Data Acquisition Example

This section provides an example of how a host processor can use the device interface to configure the device internal registers as well as convert and acquire data for sampling a particular input channel. The timing diagram shown in 図 87 provides further details.

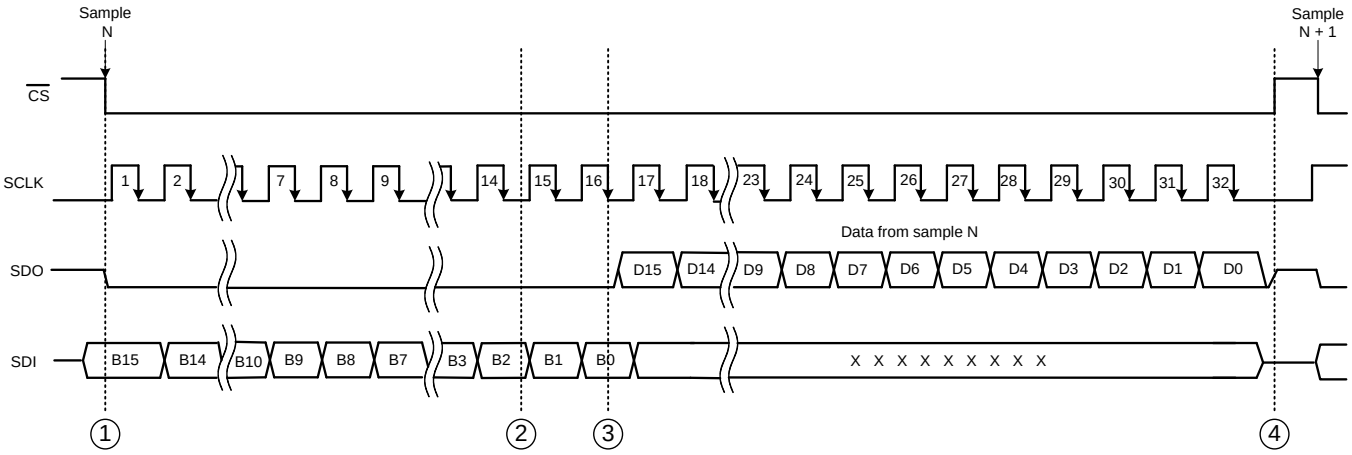


図 87. Device Operation Using the Serial Interface Timing Diagram

There are four events shown in 図 87, which are described below:

- ***Event 1:*** The host initiates a data conversion frame through a falling edge of the $\overline{CS}$ signal. The analog input signal at the instant of the $\overline{CS}$ falling edge is sampled by the ADC and conversion is performed using an internal oscillator clock. The analog input channel converted during this frame is selected in the previous data frame. The internal register settings of the device for the next conversion can be input during this data frame using the SDI and SCLK inputs. Initiate SCLK at this instant and latch data on the SDI line into the device on every SCLK falling edge for the next 16 SCLK cycles. At this instant, SDO goes low because the device does not output internal conversion data on the SDO line during the first 16 SCLK cycles.
- ***Event 2:*** During the first 16 SCLK cycles, the device completes the internal conversion process and data are now ready within the converter. However, the device does not output data bits on SDO until the 16th falling edge appears on the SCLK input. Because the ADC conversion time is fixed (the maximum value is given in the *Electrical Characteristics* table), the 16th SCLK falling edge must appear after the internal conversion is over, otherwise data output from the device is incorrect. Therefore, the SCLK frequency cannot exceed a maximum value, as provided in the *Timing Requirements: Serial Interface* table.
- ***Event 3:*** At the 16th falling edge of the SCLK signal, the device reads the LSB of the input word on the SDI line. The device does not read anything from the SDI line for the remaining data frame. On the same edge, the MSB of the conversion data is output on the SDO line and can be read by the host processor on the subsequent falling edge of the SCLK signal. For 16 bits of output data, the LSB can be read on the 32nd SCLK falling edge. The SDO outputs 0 on subsequent SCLK falling edges until the next conversion is initiated.
- ***Event 4:*** When the internal data from the device is received, the host terminates the data frame by deactivating the $\overline{CS}$ signal to high. The SDO output goes into a Hi-Z state until the next data frame is initiated, as explained in Event 1.

7.4.1.3 Host-to-Device Connection Topologies

The digital interface of the ADS8688AT offers a lot of flexibility in the ways that a host controller can exchange data or commands with the device. A typical connection between a host controller and a stand-alone device is illustrated in 図 85. However, there are applications that require multiple ADCs but the host controller has limited interfacing capability. This section describes two connection topologies that can be used to address the requirements of such applications.

7.4.1.3.1 Daisy-Chain Topology

図 88 shows a typical connection diagram with multiple devices in daisy-chain mode. The $\overline{CS}$, SCLK, and SDI inputs of all devices are connected together and controlled by a single $\overline{CS}$, SCLK, and SDO pin of the host controller, respectively. The $DAISY_1$ input pin of the first ADC in the chain is connected to DGND, the SDO_1 output pin is connected to the $DAISY_2$ input of ADC_2, and so forth. The SDO_N pin of the Nth ADC in the chain is connected to the SDI pin of the host controller. The devices do not require any special hardware or software configuration to enter daisy-chain mode.

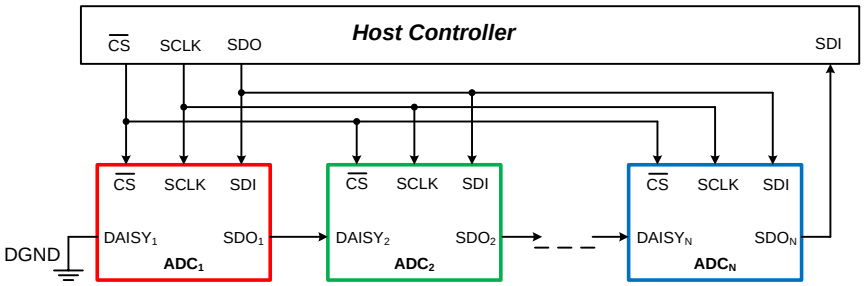


図 88. Daisy-Chain Connection Schematic

図 89 shows a typical timing diagram for three devices connected in daisy-chain mode.

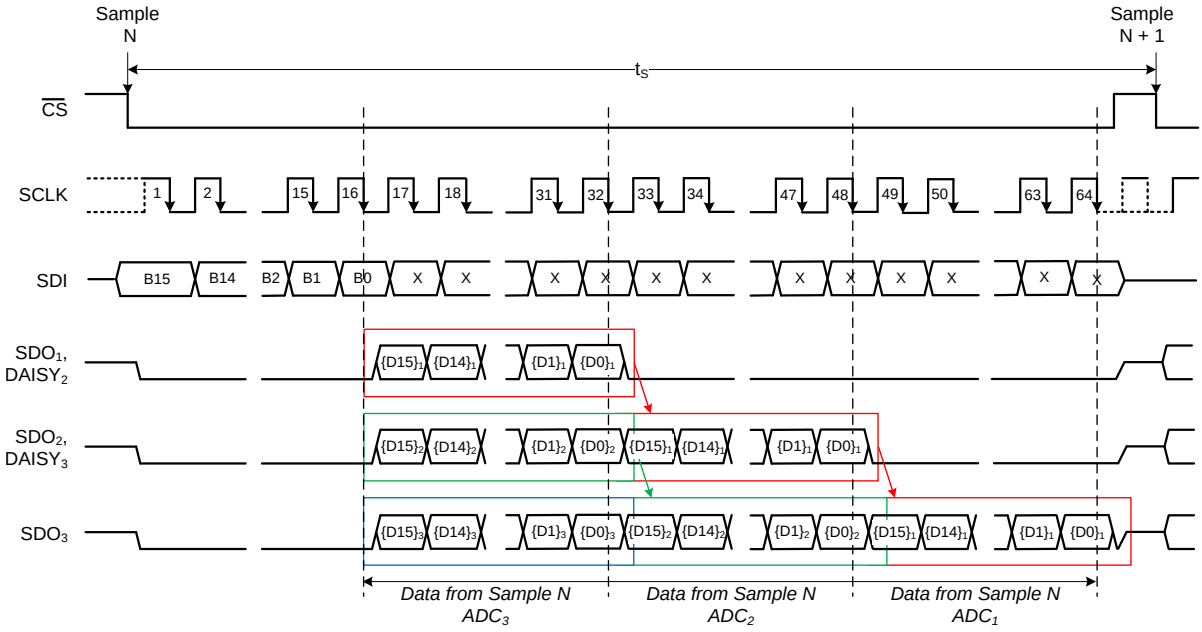


図 89. Three Devices Connected in Daisy-Chain Mode Timing Diagram

At the falling edge of the $\overline{CS}$ signal, all devices sample the input signal at their respective selected channels and enter into conversion phase. For the first 16 SCLK cycles, the internal register settings for the next conversion can be entered using the SDI line that is common to all devices in the chain. During this time period, the SDO outputs for all devices remain low. At the end of conversion, every ADC in the chain loads its own conversion result into an internal 16-bit shift register. At the 16th SCLK falling edge, every ADC in the chain outputs the MSB bit on its own SDO output pin. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DAISY pin and shifts out the next bit of data on its SDO pin. Therefore, the digital host receives the data of ADC_N, followed by the data of $ADC_{N–1}$, and so forth (in MSB-first fashion). In total, a minimum of 16 × N SCLK falling edges are required to capture the outputs of all N devices in the chain. This example uses three devices in a daisy-chain connection, so 3 × 16 = 48 SCLK cycles are required to capture the outputs of all devices in the chain along with the 16 SCLK cycles to input the register settings for the next conversion, resulting in a total of 64 SCLK cycles for the entire data frame. The overall throughput of the system is proportionally reduced with the number of devices connected in a daisy-chain configuration.

The following points must be noted about the daisy-chain configuration illustrated in 図 88:

- The SDI pins for all devices are connected together so each device operates with the same internal configuration. This limitation can be overcome by spending additional host controller resources to control the $\overline{CS}$ or SDI input of devices with unique configurations.
- If the number of devices connected in daisy-chain is more than four, loading increases on the shared output lines from the host controller ($\overline{CS}$, SDO, and SCLK). This increased loading can lead to digital timing errors. This limitation can be overcome by using digital buffers on the shared outputs from the host controller before feeding the shared digital lines into additional devices.

7.4.1.3.2 Star Topology

図 90 shows a typical connection diagram with multiple devices in the star topology. The SDI and SCLK inputs of all devices are connected together and are controlled by a single SDO and SCLK pin of the host controller, respectively. Similarly, the SDO outputs of all devices are tied together and connected to the SDI input pin of the host controller. The $\overline{CS}$ input pin of each device is individually controlled by separate $\overline{CS}$ control lines from the host controller.

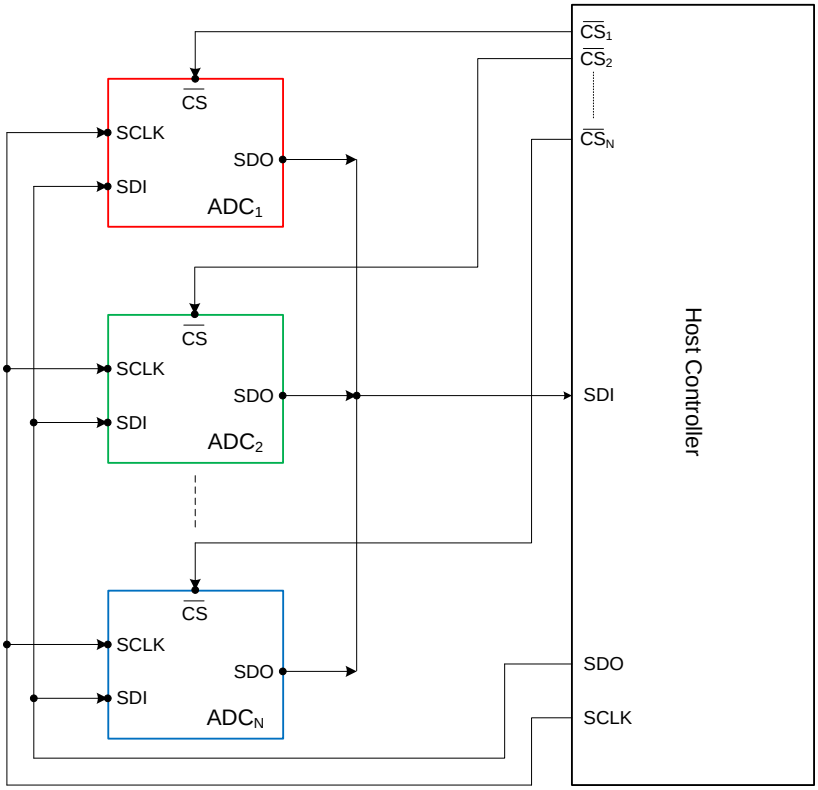


図 90. Star Topology Connection Schematic

The timing diagram for a typical data frame in the star topology is the same as in a stand-alone device operation, as illustrated in 図 87. The data frame for a particular device starts with the falling edge of the $\overline{CS}$ signal and ends when the $\overline{CS}$ signal goes high. Because the host controller provides separate $\overline{CS}$ control signals for each device in this topology, devices can be selected in any order and conversions can be initiated by bringing down the $\overline{CS}$ signal for that particular device. As explained in 図 87, when $\overline{CS}$ goes high at the end of each data frame, the SDO output of the device is placed into a Hi-Z state. Therefore, the shared SDO line in the star topology is controlled only by the device with an active data frame ($\overline{CS}$ is low). In order to avoid any conflict related to multiple devices driving the SDO line at the same time, ensure that the host controller pulls down the $\overline{CS}$ signal for only one device at any particular time.

TI recommends connecting a maximum of four devices in the star topology. Beyond that, loading may increase on the shared output lines from the host controller (SDO and SCLK). This loading can lead to digital timing errors. This limitation can be overcome by using digital buffers on the shared outputs from the host controller before being fed into additional devices.

7.4.2 Device Modes

The ADS8688AT supports multiple modes of operation that are software programmable. After powering up, the device is placed into idle mode and does not perform any function until a command is received from the user. 表 7 lists all commands to enter the different modes of the device. After power-up, the program registers wake up with the default values and require appropriate configuration settings before performing any conversion. The diagram in 図 91 explains how to switch the device from one mode of operation to another.

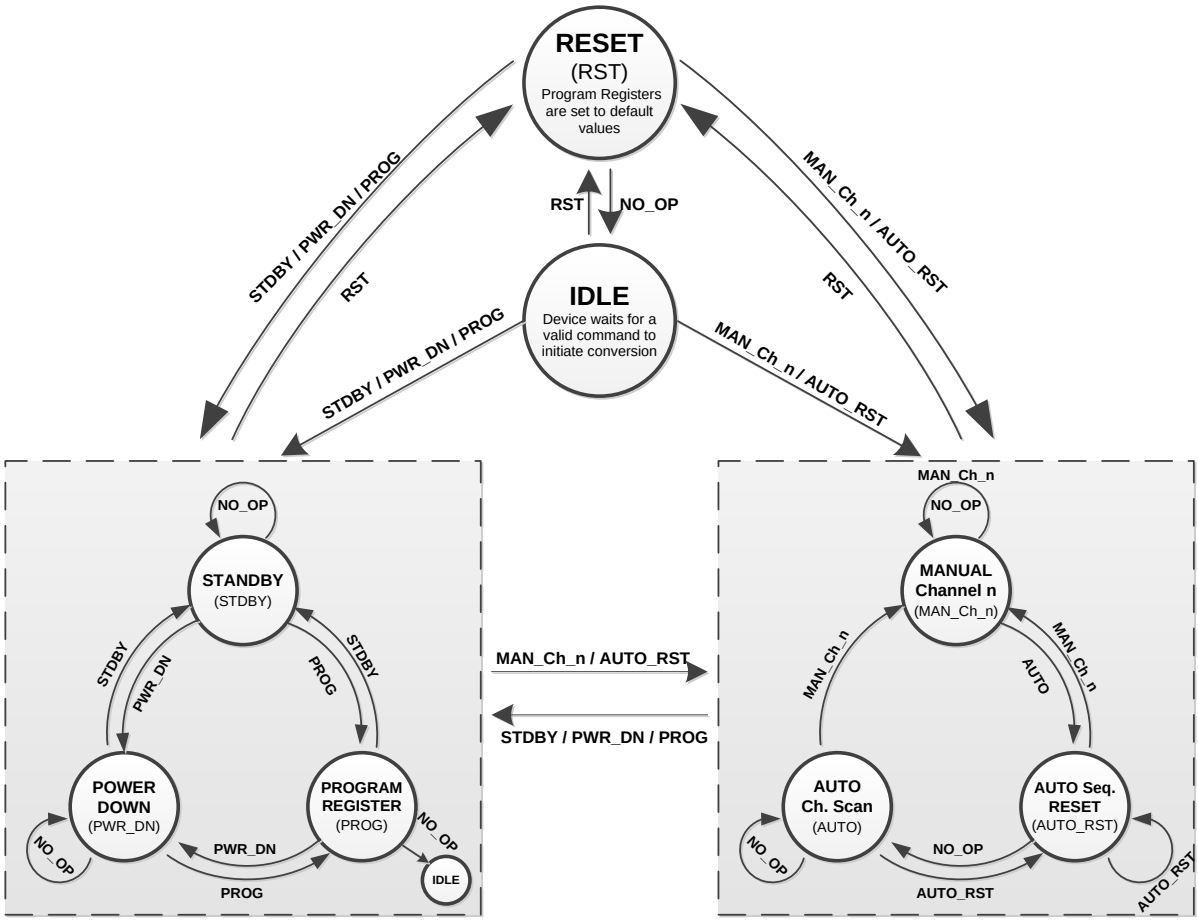


図 91. State Transition Diagram

7.4.2.1 Continued Operation in the Selected Mode (NO_OP)

Holding the SDI line low continuously (equivalent to writing a 0 to all 16 bits) during device operation continues device operation in the last selected mode (STDBY, PWR_DN, AUTO_RST, or MAN_Ch_n). In this mode, the device follows the same settings that are already configured in the program registers.

If a NO_OP condition occurs when the device is performing any read or write operation in the program register (PROG mode), then the device retains the current settings of the program registers. The device goes back to IDLE mode and waits for a proper command to be entered before executing the program register read or write configuration.

7.4.2.2 Frame Abort Condition (FRAME_ABORT)

As explained in the *Data Acquisition Example* section, the device digital interface is designed such that each data frame starts with a falling edge of the $\overline{CS}$ signal. During the first 16 SCLK cycles, the device reads the 16-bit command word on the SDI line. The device waits to execute the command until the last bit of the command is received, which is latched on the 16th SCLK falling edge. During this operation, the $\overline{CS}$ signal must stay low. If the $\overline{CS}$ signal goes high for any reason before the data transmission is complete, the device goes into an INVALID state and waits for a proper command to be written. This condition is called the FRAME_ABORT condition. When the device is operating in this INVALID mode, any read operation on the device returns invalid data on the SDO line. The output of the ALARM pin continues to reflect the status of input signal on the previously selected channel.

7.4.2.3 STANDBY Mode (STDBY)

The device supports a low-power standby mode (STDBY) in which only part of the circuit is powered down. The internal reference and buffer is not powered down, and therefore, the device can be quickly powered up in 20 µs on exiting the STDBY mode. When the device comes out of STDBY mode, the program registers are not reset to the default values.

To enter STDBY mode, execute a valid write operation as shown in 図 92 to the command register with a STDBY command of 8200h. The command is executed and the device enters STDBY mode on the next $\overline{CS}$ rising edge following this write operation. The device remains in STDBY mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during the subsequent data frames. When the device operates in STDBY mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in STDBY mode. The program register read operation can take place normally during this mode.

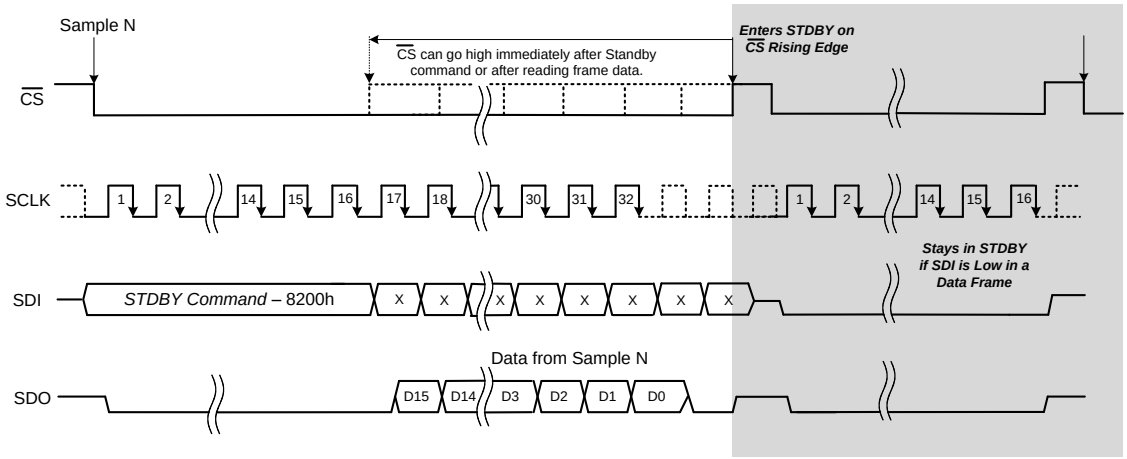


図 92. Enter and Remain in STDBY Mode Timing Diagram

In order to exit STDBY mode, as shown in 図 93, a valid 16-bit write command must be executed to enter auto (AUTO_RST) or manual (MAN_CH_n) scan mode. The device starts exiting STDBY mode on the next $\overline{CS}$ rising edge. At the next $\overline{CS}$ falling edge, the device samples the analog input at the channel selected by the MAN_CH_n command or the first channel of the AUTO_RST mode sequence. To ensure that the input signal is sampled correctly, keep the minimum width of the $\overline{CS}$ signal at 20 µs after exiting STDBY mode so the device internal circuitry can be fully powered up and biased properly before taking the sample. The data output for the selected channel can be read during the same data frame, as explained in 図 87.

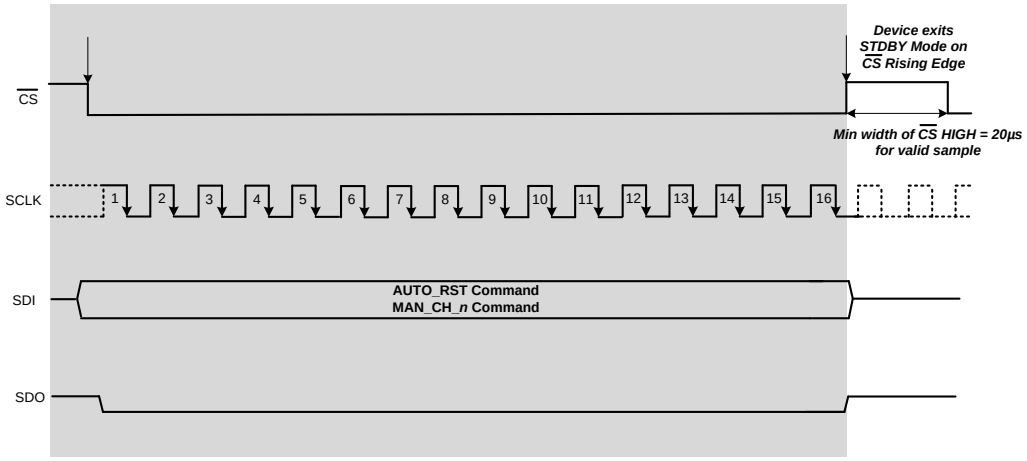


図 93. Exit STDBY Mode Timing Diagram

7.4.2.4 Power-Down Mode (PWR_DN)

The device supports a hardware and software power-down mode (PWR_DN) in which all internal circuitry is powered down, including the internal reference and buffer. A minimum time of 15 ms is required for the device to power up and convert the selected analog input channel after exiting PWR_DN mode, if the device is operating in the internal reference mode ($\overline{REFSEL}$ = 0). The hardware power-down mode for the device is explained in the ***$\overline{RST}$/PD (Input)*** section. The primary difference between the hardware and software power-down modes is that the program registers are reset to default values when the devices wake up from hardware power-down, but the previous settings of the program registers are retained when the devices wake up from software power-down.

To enter PWR_DN mode using software, execute a valid write operation as depicted in 図 94 on the command register with a software PWR_DN command of 8300h. The command is executed and the device enters PWR_DN mode on the next $\overline{CS}$ rising edge following this write operation. The device remains in PWR_DN mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during the subsequent data frames. When the device operates in PWR_DN mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in PWR_DN mode. The program register read operation can take place normally during this mode.

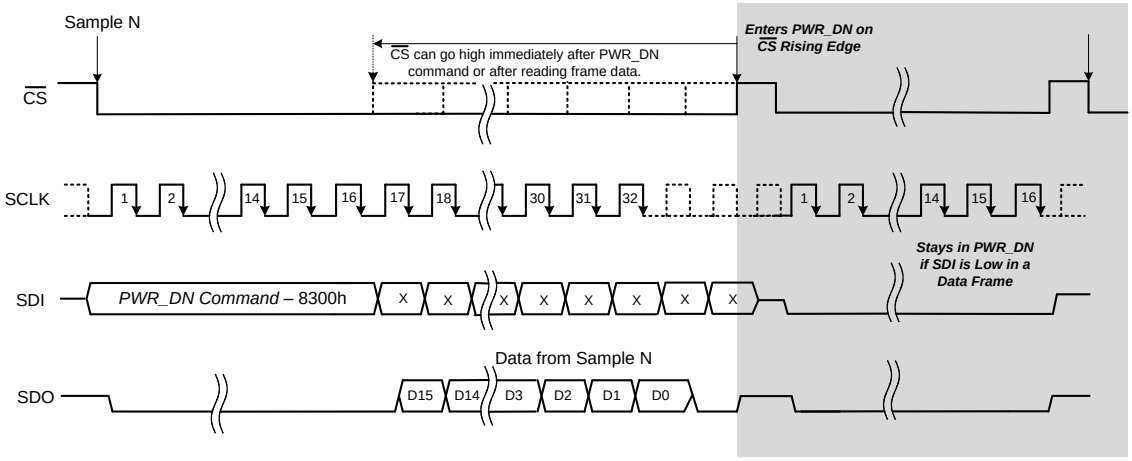


図 94. Enter and Remain in PWR_DN Mode Timing Diagram

In order to exit from PWR_DN mode, as shown in 図 95, a valid 16-bit write command must be executed. The device comes out of PWR_DN mode on the next $\overline{CS}$ rising edge. For operation in internal reference mode ($\overline{REFSEL}$ = 0), 15 ms are required for the device to power-up the reference and other internal circuits and settle to the required accuracy before valid conversion data are output for the selected input channel.

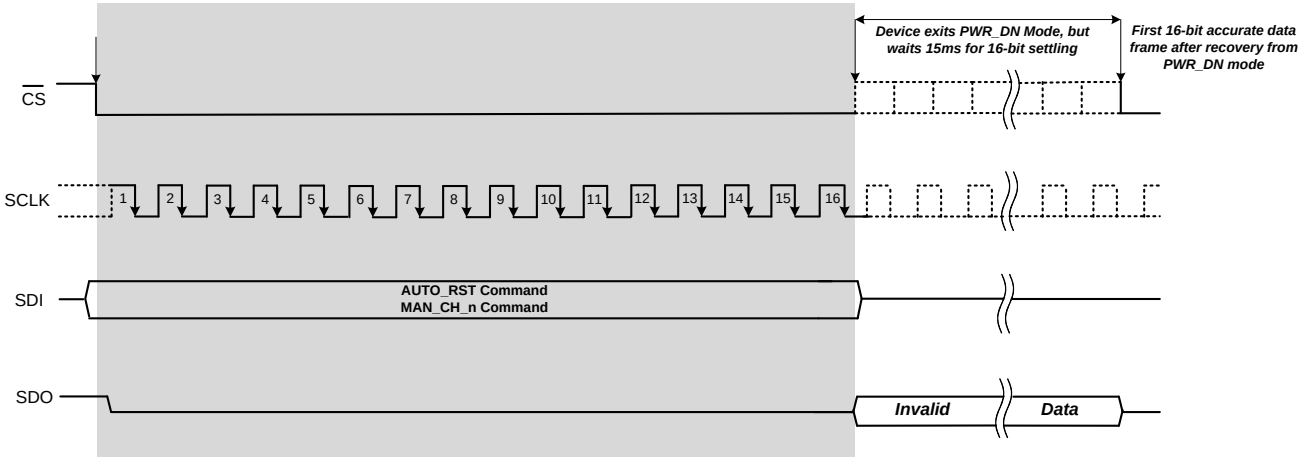


図 95. Exit PWR_DN Mode Timing Diagram

7.4.2.5 Auto Channel Enable With Reset (AUTO_RST)

The device can be programmed as explained in 図 96 to scan the input signal on all analog channels automatically by writing a valid auto channel sequence with a reset (AUTO_RST, A000h) command in the command register. As shown in 図 96, the $\overline{CS}$ signal can be pulled high immediately after the AUTO_RST command or after reading the output data of the frame. However, in order to accurately acquire and convert the input signal on the first selected channel in the next data frame, the command frame must be a complete frame of 32 SCLK cycles.

The sequence of channels for the automatic scan can be configured by the AUTO SCAN sequencing control register (01h to 02h) in the program register; see the *Program Register Map* section. In this mode, the device continuously cycles through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the program register. On completion of the sequence, the device returns to the lowest count channel in the program register and repeats the sequence. The input voltage range for each channel in the auto-scan sequence can be configured by setting the *range select registers* of the program registers.

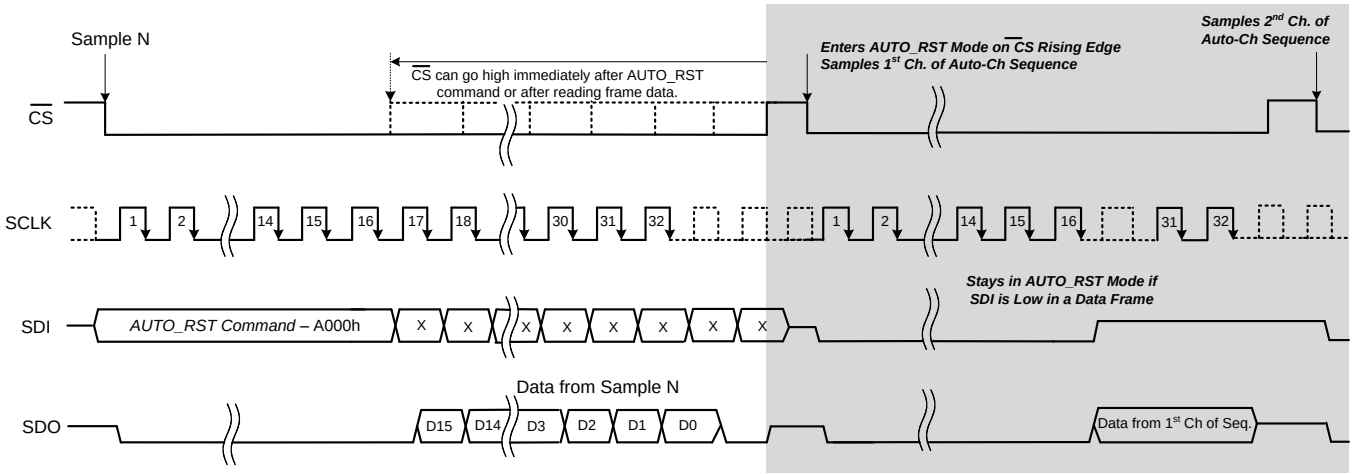


図 96. Enter AUTO_RST Mode Timing Diagram

The device remains in AUTO_RST mode if no other valid command is executed and SDI is kept low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during subsequent data frames. If the AUTO_RST command is executed again at any time during this mode of operation, then the sequence of the scanned channels is reset. The device returns to the lowest count channel of the auto-scan sequence in the program register and repeats the sequence. The timing diagram in 図 97 shows this behavior using an example in which channels 0 to 2 are selected in the auto sequence. For switching between AUTO_RST mode and MAN_Ch_n mode; see the *Channel Sequencing Modes* section.

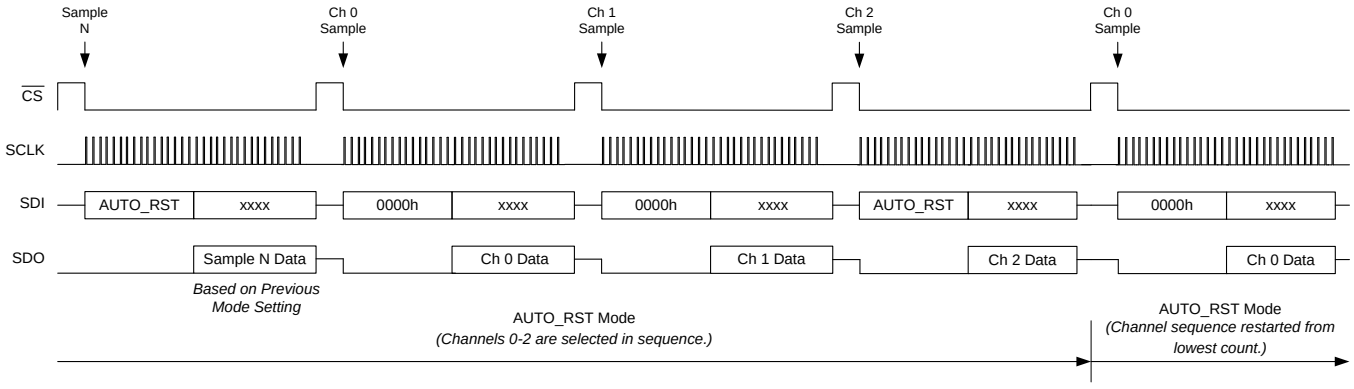


図 97. Device Operation Example in AUTO_RST Mode

7.4.2.6 Manual Channel n Select (MAN_Ch_n)

The device can be programmed to convert a particular analog input channel by operating in manual channel *n* scan mode (MAN_Ch_n). This programming is done as shown in 図 98 by writing a valid manual channel *n* select command (MAN_Ch_n) in the command register. As shown in 図 98, the $\overline{CS}$ signal can be pulled high immediately after the MAN_Ch_n command or after reading the output data of the frame. However, in order to accurately acquire and convert the input signal on the next channel, the command frame must be a complete frame of 32 SCLK cycles. See 表 7 for a list of commands to select individual channels during MAN_Ch_n mode.

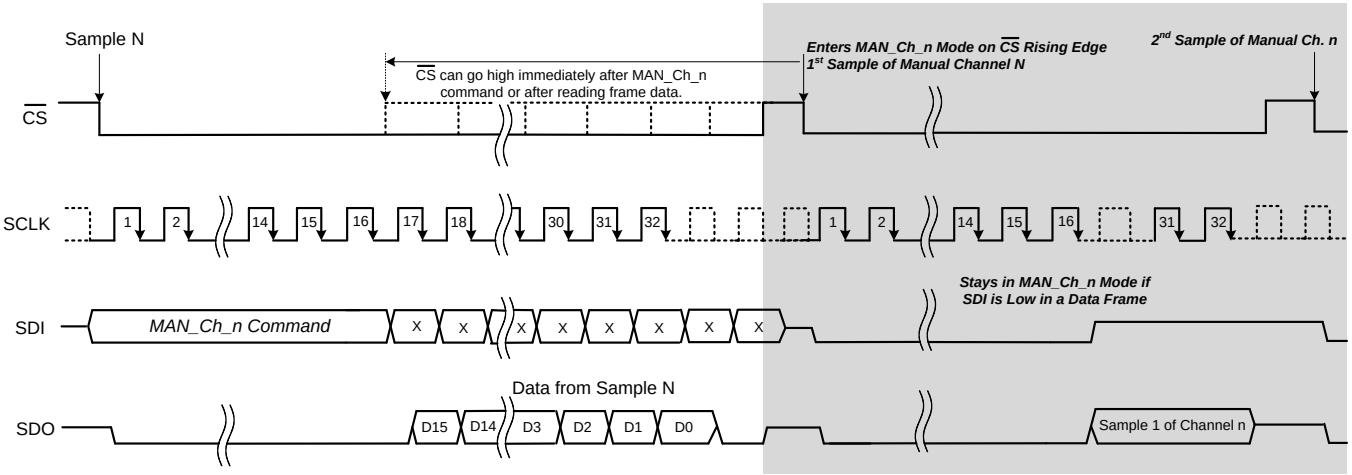


図 98. Enter MAN_Ch_*n* Scan Mode Timing Diagram

The manual channel *n* select command (MAN_Ch_n) is executed and the device samples the analog input on the selected channel on the $\overline{CS}$ falling edge of the next data frame following this write operation. The input voltage range for each channel in the MAN_Ch_n mode can be configured by setting the *range select registers* in the program registers. The device continues to sample the analog input on the same channel if no other valid command is executed and SDI is kept low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during subsequent data frames. The timing diagram in 図 99 shows this behavior using an example in which channel 1 is selected in the manual sequencing mode. For switching between MAN_Ch_n mode and AUTO_RST mode; see the *Channel Sequencing Modes* section.

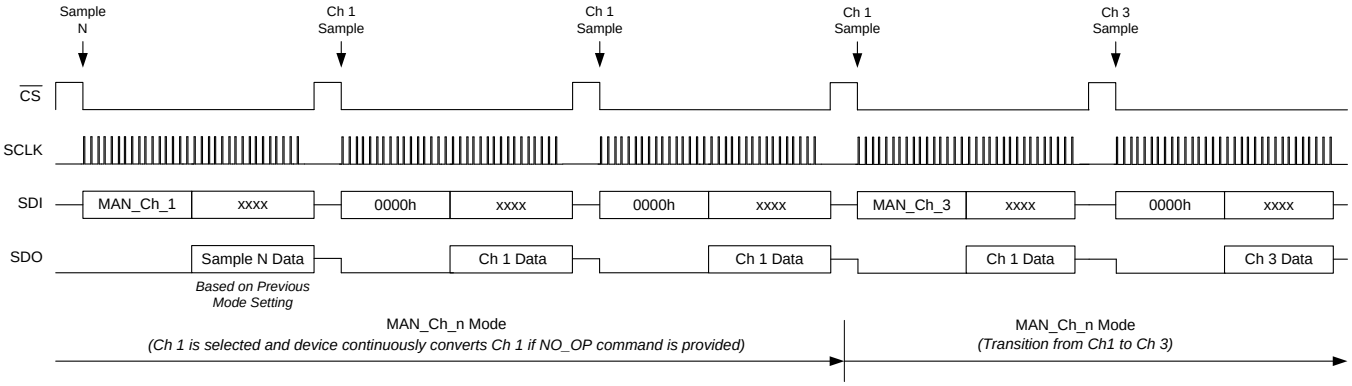


図 99. Device Operation in MAN_Ch_n Mode

7.4.2.7 Channel Sequencing Modes

The device offers two channel sequencing modes: AUTO_RST and MAN_Ch_n.

In AUTO_RST mode, the channel number automatically increments in every subsequent frame. As explained in the auto-scan sequencing control registers, the analog inputs can be selected for an automatic scan with a register setting. The device automatically scans only the selected analog inputs in ascending order. The unselected analog input channels can also be powered down for optimizing power consumption in this mode of operation. The auto-mode sequence can be reset at any time during an automatic scan (using the AUTO_RST command). When the reset command is received, the ongoing auto-mode sequence is reset and restarts from the lowest selected channel in the sequence.

In MAN_Ch_n mode, the same input channel is selected during every data conversion frame. The input command words to select individual analog channels in MAN_Ch_n mode are listed in 表 7. If a particular input channel is selected during a data frame, then the analog inputs on the same channel are sampled during the next data frame. 図 100 shows the SDI command sequence for transitions from AUTO_RST to MAN_Ch_n mode.

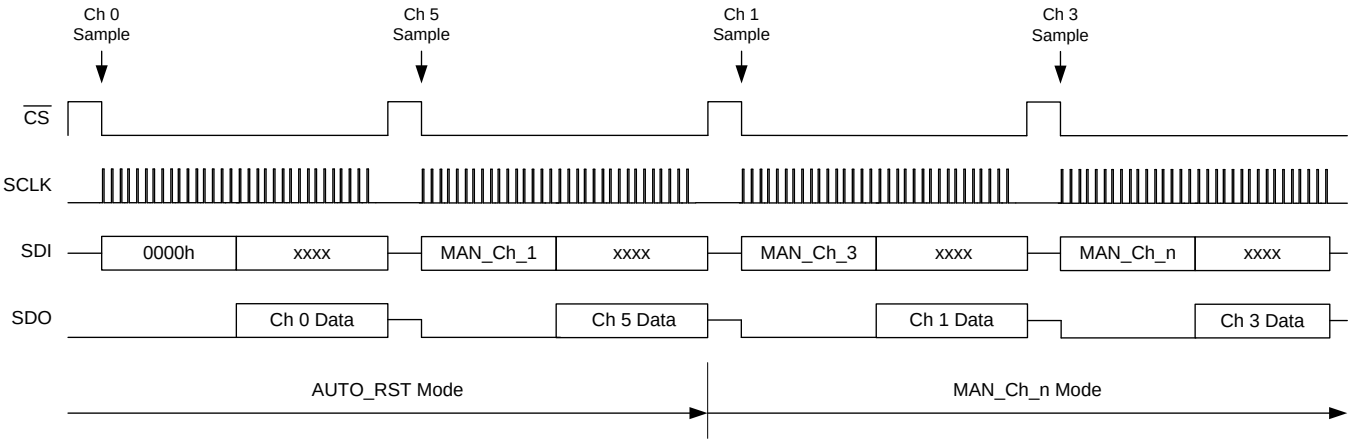


図 100. Transitioning From AUTO_RST to MAN_Ch_n Mode (Channels 0 and 5 are Selected for Auto Sequence)

図 101 shows the SDI command sequence for transitions from MAN_Ch_n to AUTO_RST mode. Each SDI command is executed on the next CS falling edge. A RST command can be issued at any instant during any channel sequencing mode, after which the device is placed into a default power-up state in the next data frame.

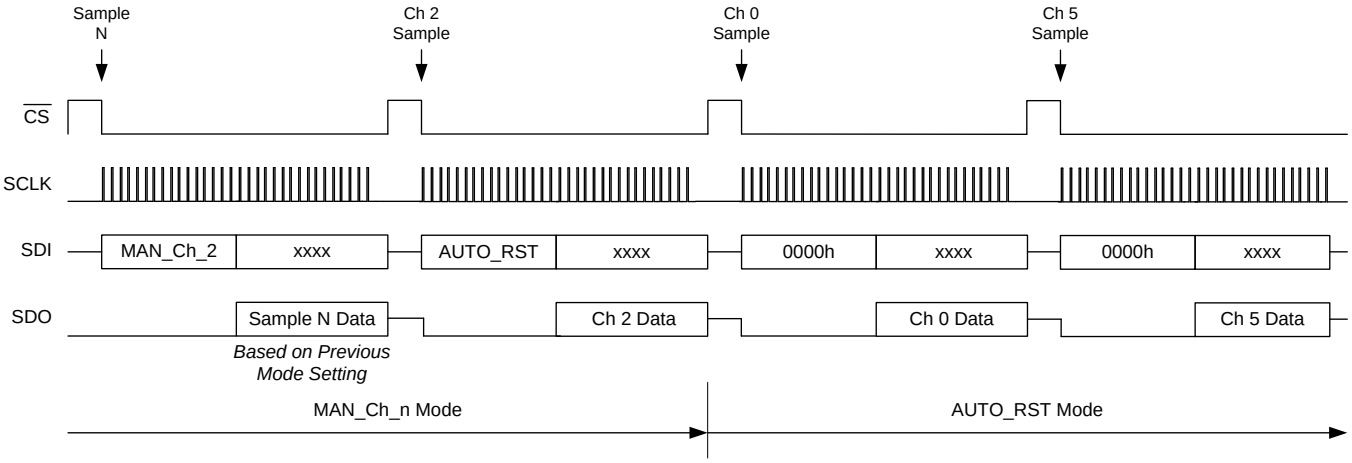


図 101. Transitioning From MAN_Ch_n to AUTO_RST Mode (Channels 0 and 5 are Selected for Auto Sequence)

7.4.2.8 Reset Program Registers (RST)

The device supports a hardware and software reset (RST) mode in which all program registers are reset to their default values. The device can be put into RST mode using a hardware pin, as explained in the ***RST/PD (Input)*** section.

The device program registers can be reset to their default values, as shown in 図 102, during any data frame by executing a valid write operation on the command register with a RST command of 8500h. The device remains in RST mode if no valid conversion command (AUTO_RST or MAN_Ch_n) is executed and SDI remains low (see the *Continued Operation in the Selected Mode (NO_OP)* section) during the subsequent data frames. When the device operates in RST mode, the program register settings can be updated (as explained in the *Program Register Read/Write Operation* section) using 16 SCLK cycles. However, if 32 complete SCLK cycles are provided, then the device returns invalid data on the SDO line because there is no ongoing conversion in RST mode. The values of the program register can be read normally during this mode. A valid AUTO_RST or MAN_CH_n channel selection command must be executed for initiating a conversion on a particular analog channel using the default program register settings.

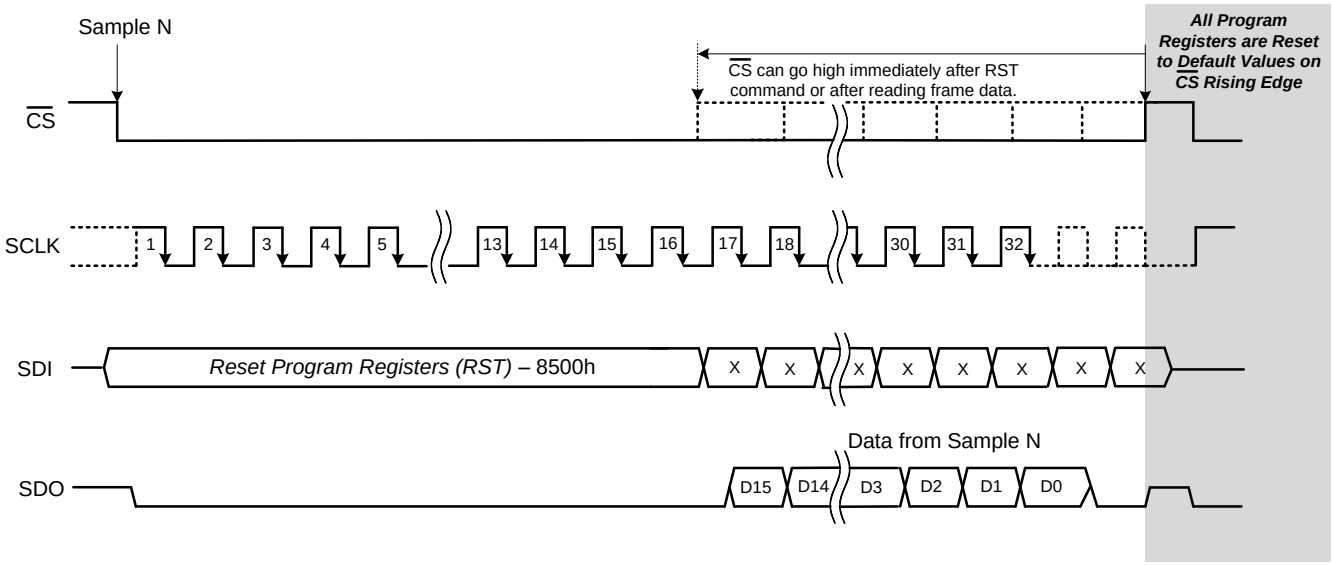


図 102. Reset Program Registers (RST) Timing Diagram

7.5 Register Maps

The internal registers of the ADS8688AT are categorized into two categories: command registers and program registers.

The command registers are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values.

The program registers are used to select the sequence of channels for AUTO_RST mode, select the SDO output format, control input range settings for individual channels, control the ALARM feature, reading the alarm flags, and programming the alarm thresholds for each channel.

Register Maps (continued)

表 6 lists the access codes used for the ADS8688AT registers.

表 6. ADS8688AT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1 Command Register Description

The command register is a 16-bit, write-only register that is used to set the operating modes of the ADS8688AT. The settings in this register are used to select the channel sequencing mode (AUTO_RST or MAN_Ch_n), configure the device in standby (STDBY) or power-down (PWR_DN) mode, and reset (RST) the program registers to their default values. 表 7 lists all command settings for this register. During power-up or reset, the default content of the command register is all 0's and the device waits for a command to be written before being placed into any mode of operation. See 図 1 for a typical timing diagram for writing a 16-bit command into the device. The device executes the command at the end of this particular data frame when the $\overline{CS}$ signal goes high.

表 7. Command Register Map

REGISTER	MSB BYTE								LSB BYTE	COMMAND (Hex)	OPERATION IN NEXT FRAME
	B15	B14	B13	B12	B11	B10	B9	B8	B[7:0]		
Continued Operation (NO_OP)	0	0	0	0	0	0	0	0	0000 0000	0000h	Continue operation in previous mode
Standby (STDBY)	1	0	0	0	0	0	1	0	0000 0000	8200h	Device is placed into standby mode
Power Down (PWR_DN)	1	0	0	0	0	0	1	1	0000 0000	8300h	Device is powered down
Reset Program Registers (RST)	1	0	0	0	0	1	0	1	0000 0000	8500h	Program register is reset to default
Auto Ch. Sequence With Reset (AUTO_RST)	1	0	1	0	0	0	0	0	0000 0000	A000h	Auto mode enabled following a reset
Manual Ch 0 Selection (MAN_Ch_0)	1	1	0	0	0	0	0	0	0000 0000	C000h	Channel 0 input is selected
Manual Ch 1 Selection (MAN_Ch_1)	1	1	0	0	0	1	0	0	0000 0000	C400h	Channel 1 input is selected
Manual Ch 2 Selection (MAN_Ch_2)	1	1	0	0	1	0	0	0	0000 0000	C800h	Channel 2 input is selected
Manual Ch 3 Selection (MAN_Ch_3)	1	1	0	0	1	1	0	0	0000 0000	CC00h	Channel 3 input is selected
Manual Ch 4 Selection (MAN_Ch_4)	1	1	0	1	0	0	0	0	0000 0000	D000h	Channel 4 input is selected
Manual Ch 5 Selection (MAN_Ch_5)	1	1	0	1	0	1	0	0	0000 0000	D400h	Channel 5 input is selected
Manual Ch 6 Selection (MAN_Ch_6)	1	1	0	1	1	0	0	0	0000 0000	D800h	Channel 6 input is selected
Manual Ch 7 Selection (MAN_Ch_7)	1	1	0	1	1	1	0	0	0000 0000	DC00h	Channel 7 input is selected
Manual AUX Selection (MAN_AUX)	1	1	1	0	0	0	0	0	0000 0000	E000h	AUX channel input is selected

7.5.2 Program Register Description

The program register is a 16-bit register used to set the operating modes of the ADS8688AT. The settings in this register are used to select the channel sequence for AUTO_RST mode, configure the device ID in daisy-chain mode, select the SDO output format, control input range settings for individual channels, control the ALARM feature, reading the alarm flags, and programming the alarm thresholds for each channel. All program settings for this register are listed in 表 10. During power-up or reset, the different program registers in the device wake up with their default values and the device waits for a command to be written before being placed into any mode of operation.

7.5.2.1 Program Register Read/Write Operation

The program register is a 16-bit read or write register. There must be a minimum of 24 SCLKs after the $\overline{CS}$ falling edge for any read or write operation to the program registers. When $\overline{CS}$ goes low, the SDO line goes low as well. The device receives the command (see 表 8 and 表 9) through SDI where the first seven bits (bits 15-9) represent the register address and the eighth bit (bit 8) is the write or read instruction.

For a write cycle, the next eight bits (bits 7-0) on SDI are the desired data for the addressed register. Over the next eight SCLK cycles, the device outputs this 8-bit data that is written into the register. This data readback allows verification to determine if the correct data are entered into the device. 図 103 shows a typical timing diagram for a program register write cycle.

表 8. Write Cycle Command Word

PIN	REGISTER ADDRESS (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	DATA (Bits 7-0)
SDI	ADDR[6:0]	1	DIN[7:0]

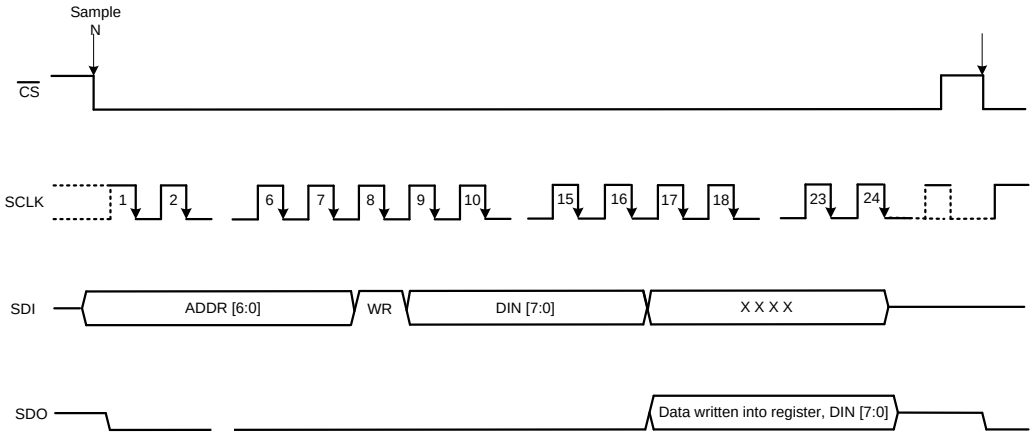


図 103. Program Register Write Cycle Timing Diagram

For a read cycle, the next eight bits (bits 7-0) on SDI are *don't care* bits and SDO stays low. From the 16th SCLK falling edge and onwards, SDO outputs the 8-bit data from the addressed register during the next eight clocks, in MSB-first fashion. 図 104 shows a typical timing diagram for a program register read cycle.

表 9. Read Cycle Command Word

PIN	REGISTER ADDRESS (Bits 15-9)	WR/$\overline{RD}$ (Bit 8)	DATA (Bits 7-0)
SDI	ADDR[6:0]	0	XXXXX
SDO	0000 000	0	DOUT[7:0]

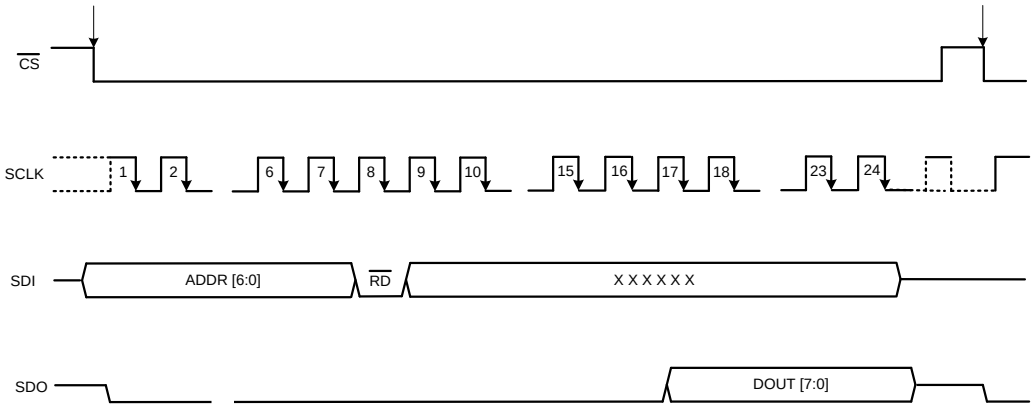


図 104. Program Register Read Cycle Timing Diagram

7.5.2.2 Program Register Map

This section provides a bit-by-bit description of each program register.

表 10. Program Register Map

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	REGISTER BITS							
			7	6	5	4	3	2	1	0
AUTO SCAN SEQUENCING CONTROL										
AUTO_SEQ_EN	01h	FFh	CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Channel Power Down	02h	00h	CH7_PD	CH6_PD	CH5_PD	CH4_PD	CH3_PD	CH2_PD	CH1_PD	CH0_PD
DEVICE FEATURES SELECTION CONTROL										
Feature Select	03h	00h	DEV[1:0]		0	ALARM_EN	0	SDO [2:0]		
RANGE SELECT REGISTERS										
Channel 0 Input Range	05h	00h	0	0	0	0	Range Select Channel 0[3:0]			
Channel 1 Input Range	06h	00h	0	0	0	0	Range Select Channel 1[3:0]			
Channel 2 Input Range	07h	00h	0	0	0	0	Range Select Channel 2[3:0]			
Channel 3 Input Range	08h	00h	0	0	0	0	Range Select Channel 3[3:0]			
Channel 4 Input Range	09h	00h	0	0	0	0	Range Select Channel 4[3:0]			
Channel 5 Input Range	0Ah	00h	0	0	0	0	Range Select Channel 5[3:0]			
Channel 6 Input Range	0Bh	00h	0	0	0	0	Range Select Channel 6[3:0]			
Channel 7 Input Range	0Ch	00h	0	0	0	0	Range Select Channel 7[3:0]			
ALARM FLAG REGISTERS (Read-Only)										
ALARM Overview Tripped-Flag	10h	00h	Tripped Alarm Flag Ch7	Tripped Alarm Flag Ch6	Tripped Alarm Flag Ch5	Tripped Alarm Flag Ch4	Tripped Alarm Flag Ch3	Tripped Alarm Flag Ch2	Tripped Alarm Flag Ch1	Tripped Alarm Flag Ch0
ALARM Ch 0-3 Tripped-Flag	11h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
ALARM Ch 0-3 Active-Flag	12h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
ALARM Ch 4-7 Tripped-Flag	13h	00h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
ALARM Ch 4-7 Active-Flag	14h	00h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.

表 10. Program Register Map (continued)

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	REGISTER BITS							
			7	6	5	4	3	2	1	0
ALARM THRESHOLD REGISTERS										
Ch 0 Hysteresis	15h	00h	CH0_HYST[7:0]							
Ch 0 High Threshold MSB	16h	FFh	CH0_HT[15:8]							
Ch 0 High Threshold LSB	17h	FFh	CH0_HT[7:0]							
Ch 0 Low Threshold MSB	18h	00h	CH0_LT[15:8]							
Ch 0 Low Threshold LSB	19h	00h	CH0_LT[7:0]							
…	…	…	See the alarm threshold setting registers for details regarding the ALARM threshold settings registers.							
Ch 7 Hysteresis	38h	00h	CH7_HYST[7:0]							
Ch 7 High Threshold MSB	39h	FFh	CH7_HT[15:8]							
Ch 7 High Threshold LSB	3Ah	FFh	CH7_HT[7:0]							
Ch 7 Low Threshold MSB	3Bh	00h	CH7_LT[15:8]							
Ch 7 Low Threshold LSB	3Ch	00h	CH7_LT[7:0]							
COMMAND READ BACK (Read-Only)										
Command Read Back	3Fh	00h	COMMAND_WORD[7:0]							

7.5.2.3 Program Register Descriptions

7.5.2.3.1 Auto-Scan Sequencing Control Registers

In AUTO_RST mode, the device automatically scans the preselected channels in ascending order with a new channel selected for every conversion. Each individual channel can be selectively included in the auto channel sequencing. For channels not selected for auto sequencing, the analog front-end circuitry can be individually powered down.

7.5.2.3.1.1 Auto-Scan Sequence Enable Register (address = 01h)

This register selects individual channels for sequencing in AUTO_RST mode. The default value for this register is FFh, which implies that in default condition all channels are included in the auto-scan sequence. If no channels are included in the auto sequence (that is, the value for this register is 00h), then channel 0 is selected for conversion by default.

図 105. AUTO_SEQ_EN Register

7	6	5	4	3	2	1	0
CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 11. AUTO_SEQ_EN Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_EN	R/W	1h	Channel 7 enable. 0 = Channel 7 is not selected for sequencing in AUTO_RST mode 1 = Channel 7 is selected for sequencing in AUTO_RST mode
6	CH6_EN	R/W	1h	Channel 6 enable. 0 = Channel 6 is not selected for sequencing in AUTO_RST mode 1 = Channel 6 is selected for sequencing in AUTO_RST mode
5	CH5_EN	R/W	1h	Channel 5 enable. 0 = Channel 5 is not selected for sequencing in AUTO_RST mode 1 = Channel 5 is selected for sequencing in AUTO_RST mode
4	CH4_EN	R/W	1h	Channel 4 enable. 0 = Channel 4 is not selected for sequencing in AUTO_RST mode 1 = Channel 4 is selected for sequencing in AUTO_RST mode
3	CH3_EN	R/W	1h	Channel 3 enable. 0 = Channel 3 is not selected for sequencing in AUTO_RST mode 1 = Channel 3 is selected for sequencing in AUTO_RST mode
2	CH2_EN	R/W	1h	Channel 2 enable. 0 = Channel 2 is not selected for sequencing in AUTO_RST mode 1 = Channel 2 is selected for sequencing in AUTO_RST mode
1	CH1_EN	R/W	1h	Channel 1 enable. 0 = Channel 1 is not selected for sequencing in AUTO_RST mode 1 = Channel 1 is selected for sequencing in AUTO_RST mode
0	CH0_EN	R/W	1h	Channel 0 enable. 0 = Channel 0 is not selected for sequencing in AUTO_RST mode 1 = Channel 0 is selected for sequencing in AUTO_RST mode

7.5.2.3.1.2 Channel Power Down Register (address = 02h)

This register powers down individual channels that are not included for sequencing in AUTO_RST mode. The default value for this register is 00h, which implies that in default condition all channels are powered up. If all channels are powered down (that is, the value for this register is FFh), then the analog front-end circuits for all channels are powered down and the output of the ADC contains invalid data. If the device is in MAN-Ch_n mode and the selected channel is powered down, then the device yields invalid output that can also trigger a false alarm condition.

図 106. Channel Power Down Register

7	6	5	4	3	2	1	0
CH7_PD	CH6_PD	CH5_PD	CH4_PD	CH3_PD	CH2_PD	CH1_PD	CH0_PD
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 12. Channel Power Down Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_PD	R/W	0h	Channel 7 power-down. 0 = The analog front-end on channel 7 is powered up and channel 7 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 7 is powered down and channel 7 cannot be included in the AUTO_RST sequence
6	CH6_PD	R/W	0h	Channel 6 power-down. 0 = The analog front-end on channel 6 is powered up and channel 6 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 6 is powered down and channel 6 cannot be included in the AUTO_RST sequence
5	CH5_PD	R/W	0h	Channel 5 power-down. 0 = The analog front-end on channel 5 is powered up and channel 5 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 5 is powered down and channel 5 cannot be included in the AUTO_RST sequence
4	CH4_PD	R/W	0h	Channel 4 power-down. 0 = The analog front-end on channel 4 is powered up and channel 4 can be included in the AUTO_RST sequence 1 = The analog front-end on channel 4 is powered down and channel 4 cannot be included in the AUTO_RST sequence
3	CH3_PD	R/W	0h	Channel 3 power-down. 0 = The analog front-end on channel 3 is powered up and channel 3 can be included in the AUTO_RST sequence 1 = The analog front end on channel 3 is powered down and channel 3 cannot be included in the AUTO_RST sequence
2	CH2_PD	R/W	0h	Channel 2 power-down. 0 = The analog front end on channel 2 is powered up and channel 2 can be included in the AUTO_RST sequence 1 = The analog front end on channel 2 is powered down and channel 2 cannot be included in the AUTO_RST sequence
1	CH1_PD	R/W	0h	Channel 1 power-down. 0 = The analog front end on channel 1 is powered up and channel 1 can be included in the AUTO_RST sequence 1 = The analog front end on channel 1 is powered down and channel 1 cannot be included in the AUTO_RST sequence
0	CH0_PD	R/W	0h	Channel 0 power-down. 0 = The analog front end on channel 0 is powered up and channel 0 can be included in the AUTO_RST sequence 1 = The analog front end on channel 0 is powered down and channel 0 cannot be included in the AUTO_RST sequence

7.5.2.3.2 Device Features Selection Control Register (address = 03h)

The bits in this register can be used to configure the device ID for daisy-chain operation, enable the ALARM feature, and configure the output bit format on SDO.

図 107. Feature Select Register

7	6	5	4	3	2	1	0
DEV[1:0]		0	ALARM_EN	0	SDO[2:0]		
R/W-0h		R-0h	R/W-0h	R-0h	R/W-0h		

表 13. Feature Select Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DEV[1:0]	R/W	0h	Device ID bits. 00 = ID for device 0 in daisy-chain mode 01 = ID for device 1 in daisy-chain mode 10 = ID for device 2 in daisy-chain mode 11 = ID for device 3 in daisy-chain mode
5	0	R	0h	Must always be set to 0
4	0	R/W	0h	ALARM feature enable. 0 = ALARM feature is disabled 1 = ALARM feature is enabled
3	0	R	0h	Must always be set to 0
2-0	SDO[2:0]	R/W	0h	SDO data format bits (see 表 14).

表 14. Description of Program Register Bits for SDO Data Format

SDO FORMAT SDO[2:0]	BEGINNING OF THE OUTPUT BIT STREAM	OUTPUT FORMAT			
		BITS 24-9	BITS 8-5	BITS 4-3	BITS 2-0
000	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	SDO pulled low		
001	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	SDO pulled low	
010	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	SDO pulled low
011	16th SCLK falling edge, no latency	Conversion result for selected channel (MSB-first)	Channel address(1)	Device address(1)	Input range(1)

(1) 表 15 lists the bit descriptions for these channel addresses, device addresses, and input range.

表 15. Bit Description for the SDO Data

BIT	BIT DESCRIPTION
24-9	16 bits of conversion result for the channel represented in MSB-first format.
8-5	Four bits of channel address. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7
4-3	Two bits of device address (mainly useful in daisy-chain mode).
2-0	Three LSB bits of input voltage range (see the range select registers).

7.5.2.3.3 Range Select Registers (addresses 05h-0Ch)

Address 05h corresponds to channel 0, address 06h corresponds to channel 1, address 07h corresponds to channel 2, address 08h corresponds to channel 3, address 09h corresponds to channel 4, address 0Ah corresponds to channel 5, address 0Bh corresponds to channel 6, and address 0Ch corresponds to channel 7.

These registers allow the selection of input ranges for all individual channels. The default value for these registers is 00h.

図 108. Channel *n* Input Range Registers

7	6	5	4	3	2	1	0
0	0	0	0	Range_CH*n*[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-0h			

表 16. Channel *n* Input Range Registers Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0h	Must always be set to 0
3-0	Range_CH*n*[3:0]	R/W	0h	Input range selection bits for channel n (n = 0 to 7). 0000 = Input range is set to ±2.5 × V_{REF} 0001 = Input range is set to ±1.25 × V_{REF} 0010 = Input range is set to ±0.625 × V_{REF} 0011 = Input range is set to ±0.3125 × V_{REF} 1011 = Input range is set to ±0.15625 × V_{REF} 0101 = Input range is set to 0 to 2.5 × V_{REF} 0110 = Input range is set to 0 to 1.25 × V_{REF} 0111 = Input range is set to 0 to 0.625 × V_{REF} 1111 = Input range is set to 0 to 0.3125 × V_{REF}

7.5.2.3.4 Alarm Flag Registers (Read-Only)

The alarm conditions related to individual channels are stored in these registers. The flags can be read when an alarm interrupt is received on the ALARM pin. There are two types of flag for every alarm: active and tripped. The active flag is set to 1 under the alarm condition (when data cross the alarm limit) and remains so as long as the alarm condition persists. The tripped flag turns on the alarm condition similar to the active flag, but remains set until read. This feature relieves the device from having to track alarms.

7.5.2.3.4.1 ALARM Overview Tripped-Flag Register (address = 10h)

The ALARM overview tripped-flags register contains the logical OR of high or low tripped alarm flags for all eight channels.

図 109. ALARM Overview Tripped-Flag Register

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch7	Tripped Alarm Flag Ch6	Tripped Alarm Flag Ch5	Tripped Alarm Flag Ch4	Tripped Alarm Flag Ch3	Tripped Alarm Flag Ch2	Tripped Alarm Flag Ch1	Tripped Alarm Flag Ch0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 17. ALARM Overview Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Tripped Alarm Flag Ch7	R	0h	Tripped alarm flag for all analog channels at a glance. Each individual bit indicates a tripped alarm flag status for each channel, as per the alarm flags register for channels 7 to 0, respectively. 0 = No alarm detected 1 = Alarm detected
6	Tripped Alarm Flag Ch6	R	0h	
5	Tripped Alarm Flag Ch5	R	0h	
4	Tripped Alarm Flag Ch4	R	0h	
3	Tripped Alarm Flag Ch3	R	0h	
2	Tripped Alarm Flag Ch2	R	0h	
1	Tripped Alarm Flag Ch1	R	0h	
0	Tripped Alarm Flag Ch0	R	0h	

7.5.2.3.4.2 Alarm Flag Registers: Tripped and Active (address = 11h to 14h)

There are two alarm thresholds (high and low) per channel, with two flags for each threshold. An active alarm flag is enabled when an alarm is triggered (when data cross the alarm threshold) and remains enabled as long as the alarm condition persists. A tripped alarm flag is enabled in the same manner as an active alarm flag, but remains latched until read. Registers 11h to 14h in the program registers store the active and tripped alarm flags for all individual eight channels.

図 110. ALARM Ch0-3 Tripped-Flag Register (address = 11h)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 18. ALARM Ch0-3 Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Tripped alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

図 111. ALARM Ch0-3 Active-Flag Register (address = 12h)

7	6	5	4	3	2	1	0
Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 19. ALARM Ch0-3 Active-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 0 to 3)	R	0h	Active alarm flag high, low for channel n (n = 0 to 3) Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

図 112. ALARM Ch4-7 Tripped-Flag Register (address = 13h)(1)

7	6	5	4	3	2	1	0
Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

(1) This register is not included in the 4-channel version of the device. A write operation on this register has no effect on device behavior. A read operation on this register outputs all 1's on the SDO line.

表 20. ALARM Ch4-7 Tripped-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Tripped Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Tripped alarm flag high, low for channel n (n = 4 to 7). Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

図 113. ALARM Ch4-7 Active-Flag Register (address = 14h)(1)

7	6	5	4	3	2	1	0
Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

(1) This register is not included in the 4-channel version of the device. A write operation on this register has no effect on device behavior. A read operation on this register outputs all 1's on the SDO line.

表 21. ALARM Ch4-7 Active-Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Active Alarm Flag Ch n Low or High (n = 4 to 7)	R	0h	Active alarm flag high, low for channel n (n = 4 to 7). Each individual bit indicates an active high or low alarm flag status for each channel, as per the alarm flags register for channels 0 to 7. 0 = No alarm detected 1 = Alarm detected

7.5.2.3.5 Alarm Threshold Setting Registers

The ADS8688AT features individual high and low alarm threshold settings for each channel. Each alarm threshold is 16 bits wide with 8-bit hysteresis, which is the same for both high and low threshold settings. This 40-bit setting is accomplished through five 8-bit registers associated with every high and low alarm.

NAME	ADDR	REGISTER BITS							
		7	6	5	4	3	2	1	0
Ch 0 Hysteresis	15h	CH0_HYST[7:0]							
Ch 0 High Threshold MSB	16h	CH0_HT[15:8]							
Ch 0 High Threshold LSB	17h	CH0_HT[7:0]							
Ch 0 Low Threshold MSB	18h	CH0_LT[15:8]							
Ch 0 Low Threshold LSB	19h	CH0_LT[7:0]							
Ch 1 Hysteresis	1Ah	CH1_HYST[7:0]							
Ch 1 High Threshold MSB	1Bh	CH1_HT[15:8]							
Ch 1 High Threshold LSB	1Ch	CH1_HT[7:0]							
Ch 1 Low Threshold MSB	1Dh	CH1_LT[15:8]							
Ch 1 Low Threshold LSB	1Eh	CH1_LT[7:0]							
Ch 2 Hysteresis	1Fh	CH2_HYST[7:0]							
Ch 2 High Threshold MSB	20h	CH2_HT[15:8]							
Ch 2 High Threshold LSB	21h	CH2_HT[7:0]							
Ch 2 Low Threshold MSB	22h	CH2_LT[15:8]							
Ch 2 Low Threshold LSB	23h	CH2_LT[7:0]							
Ch 3 Hysteresis	24h	CH3_HYST[7:0]							
Ch 3 High Threshold MSB	25h	CH3_HT[15:8]							
Ch 3 High Threshold LSB	26h	CH3_HT[7:0]							
Ch 3 Low Threshold MSB	27h	CH3_LT[15:8]							
Ch 3 Low Threshold LSB	28h	CH3_LT[7:0]							
Ch 4 Hysteresis	29h	CH4_HYST[7:0]							
Ch 4 High Threshold MSB	2Ah	CH4_HT[15:8]							
Ch 4 High Threshold LSB	2Bh	CH4_HT[7:0]							
Ch 4 Low Threshold MSB	2Ch	CH4_LT[15:8]							
Ch 4 Low Threshold LSB	2Dh	CH4_LT[7:0]							
Ch 5 Hysteresis	2Eh	CH5_HYST[7:0]							
Ch 5 High Threshold MSB	2Fh	CH5_HT[15:8]							
Ch 5 High Threshold LSB	30h	CH5_HT[7:0]							
Ch 5 Low Threshold MSB	31h	CH5_LT[15:8]							
Ch 5 Low Threshold LSB	32h	CH5_LT[7:0]							
Ch 6 Hysteresis	33h	CH6_HYST[7:0]							
Ch 6 High Threshold MSB	34h	CH6_HT[15:8]							
Ch 6 High Threshold LSB	35h	CH6_HT[7:0]							
Ch 6 Low Threshold MSB	36h	CH6_LT[15:8]							
Ch 6 Low Threshold LSB	37h	CH6_LT[7:0]							
Ch 7 Hysteresis	38h	CH7_HYST[7:0]							
Ch 7 High Threshold MSB	39h	CH7_HT[15:8]							
Ch 7 High Threshold LSB	3Ah	CH7_HT[7:0]							
Ch 7 Low Threshold MSB	3Bh	CH7_LT[15:8]							
Ch 7 Low Threshold LSB	3Ch	CH7_LT[7:0]							

図 114. Ch n Hysteresis Registers

7	6	5	4	3	2	1	0
CHn_HYST[7:0]							
R/W-0h							

表 22. Channel *n* Hysteresis Register Field Descriptions (n = 0 to 7)

Bit	Field	Type	Reset	Description
7-0	Channel *n* Hysteresis[7-0]	R/W	0h	These bits set the channel high and low alarm hysteresis for channel *n (n = 0 to 7)* For example, bits 7-0 of the channel 0 register (address 15h) set the channel 0 alarm hysteresis. 00000000 = No hysteresis 00000001 = ±1-LSB hysteresis 00000010 to 11111110 = ±2-LSB to ±254-LSB hysteresis 11111111 = ±255-LSB hysteresis

図 115. Ch n High Threshold MSB Registers

7	6	5	4	3	2	1	0
CHn_HT[15:8]							
R/W-1h							

表 23. Channel *n* High Threshold MSB Register Field Descriptions (n = 0 to 7)

Bit	Field	Type	Reset	Description
7-0	CH*n*_HT[15:8]	R/W	1h	These bits set the MSB byte for the 16-bit channel *n* high alarm. For example, bits 7-0 of the channel 0 register (address 16h) set the MSB byte for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the channel 0 high threshold MSB register (address 16h) are set to AAh and bits 7-0 of the channel 0 high threshold LSB register (address 17h) are set to FFh. 0000 0000 = MSB byte is 00h 0000 0001 = MSB byte is 01h 0000 0010 to 1110 1111 = MSB byte is 02h to FEh 1111 1111 = MSB byte is FFh

図 116. Ch n High Threshold LSB Registers

7	6	5	4	3	2	1	0
CHn_HT[7:0]							
R/W-1h							

表 24. Channel *n* High Threshold LSB Register Field Descriptions (n = 0 to 7)

Bit	Field	Type	Reset	Description
7-0	CH*n*_HT[7-0]	R/W	1h	These bits set the LSB for the 16-bit channel *n* high alarm. For example, bits 7-0 of the channel 0 register (address 17h) set the LSB for the channel 0 high alarm threshold. The channel 0 high alarm threshold is AAFFh when bits 7-0 of the channel 0 high threshold MSB register (address 16h) are set to AAh and bits 7-0 of the channel 0 high threshold LSB register (address 17h) are set to FFh. 0000 0000 = LSB byte is 00h 0000 0001 = LSB byte is 01h 0000 0010 to 1111 1110 = LSB byte is 02h to FEh 1111 1111 = LSB byte is FFh

図 117. Ch n Low Threshold MSB Registers

7	6	5	4	3	2	1	0
CHn_LT[15:8]							
R/W-0h							

表 25. Channel *n* Low Threshold MSB Register Field Descriptions (n = 0 to 7)

Bit	Field	Type	Reset	Description
7-0	CH*n*_LT[15:8]	R/W	0h	These bits set the MSB byte for the 16-bit channel *n* low alarm. For example, bits 7-0 of the channel 0 register (address 18h) set the MSB byte for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the channel 0 low threshold MSB register (address 18h) are set to AAh and bits 7-0 of the channel 0 low threshold LSB register (address 19h) are set to FFh. 0000 0000 = MSB byte is 00h 0000 0001 = MSB byte is 01h 0000 0010 to 1110 1111 = MSB byte is 02h to FEh 1111 1111 = MSB byte is FFh

図 118. Ch n Low Threshold LSB Registers

7	6	5	4	3	2	1	0
CHn_LT[7:0]							
R/W-0h							

表 26. Channel *n* Low Threshold MSB Register Field Descriptions (n = 0 to 7)

Bit	Field	Type	Reset	Description
7-0	CH*n*_LT[7-0]	R/W	00h	These bits set the LSB for the 16-bit channel *n* low alarm. For example, bits 7-0 of the channel 0 register (address 19h) set the LSB for the channel 0 low alarm threshold. The channel 0 low alarm threshold is AAFFh when bits 7-0 of the channel 0 low threshold MSB register (address 18h) are set to AAh and bits 7-0 of the channel 0 low threshold LSB register (address 19h) are set to FFh. 0000 0000 = LSB byte is 00h 0000 0001 = LSB byte is 01h 0000 0010 to 1110 1111 = LSB byte is 02h to FEh 1111 1111 = LSB byte is FFh

7.5.2.3.6 Command Read-Back Register (address = 3Fh)

This register allows the device mode of operation to be read. On execution of this command, the device outputs the command word executed in the previous data frame. The output of the command register appears on SDO from the 16th falling edge onwards in an MSB-first format. All information regarding the command register is contained in the first eight bits and the last eight bits are 0 (see 表 7), thus the command read-back operation can be stopped after the 24th SCLK cycle.

図 119. Command Read-Back Register

7	6	5	4	3	2	1	0
COMMAND_WORD[15:8]							
R-0h							

表 27. Command Read-Back Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COMMAND_WORD[15:8]	R	0h	Command executed in previous data frame.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADS8688AT is a fully integrated data acquisition system based on a 16-bit SAR ADC. The device includes an integrated analog front-end for each input channel and an integrated precision reference with a buffer. As such, this device does not require any additional external circuits for driving the reference or analog input pins of the ADC.

8.2 Typical Applications

8.2.1 Phase-Compensated, 8-Channel, Multiplexed Data Acquisition System for Power Automation

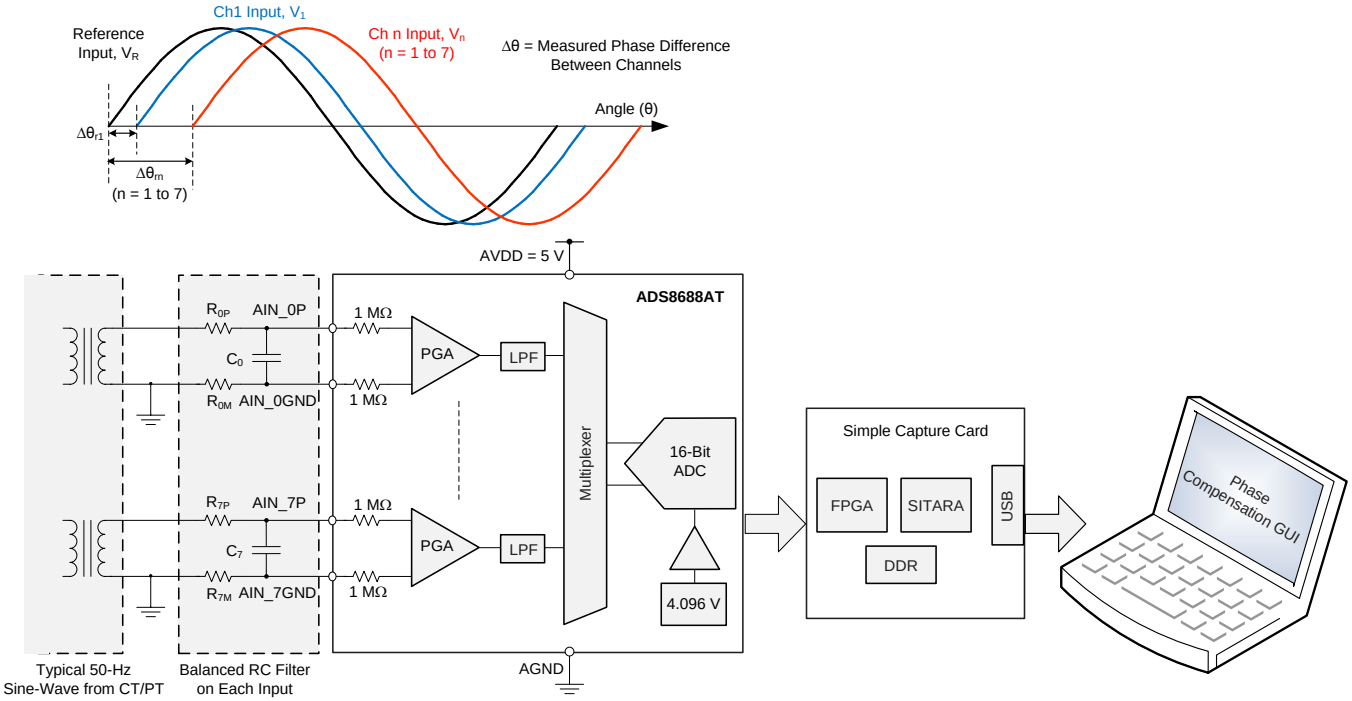


図 120. 8-Channel, Multiplexed Data Acquisition System for Power Automation

8.2.1.1 Design Requirements

In modern power grids, accurately measuring the electrical parameters of the various areas of the power grid is extremely critical. This measurement helps determine the operating status and running quality of the grid. Such accurate measurements also help diagnose potential problems with the power network so that these problems can be resolved quickly without having any significant service disruption. The key electrical parameters include amplitude, frequency, and phase, which are important for calculating the power factor, power quality, and other parameters of the power system.

Typical Applications (continued)

The phase angle of the electrical signal on the power network buses is a special interest to power system engineers. The primary objective for this design is to accurately measure the phase and phase difference between the analog input signals in a multichannel data acquisition system. When multiple input channels are sampled in a sequential manner as in a multiplexed ADC, an additional phase delay is introduced between the channels. Thus, the phase measurements are not accurate. However, this additional phase delay is constant and can be compensated in application software.

The key design requirements are given below:

- Single-ended sinusoidal input signal with a ±10-V amplitude and typical frequency (f_{IN} = 50 Hz).
- Design an 8-channel multiplexed data acquisition system using a 16-bit SAR ADC.
- Design a software algorithm to compensate for the additional phase difference between the channels.

8.2.1.2 Detailed Design Procedure

The application circuit and system diagram for this design is illustrated in 図 120. This design includes a complete hardware and software implementation of a multichannel data acquisition system for power automation applications.

This system can be designed using the ADS8688AT, which is a 16-bit, 500-kSPS, 8-channel, multiplexed input, SAR ADC with integrated precision reference and analog front-end circuitry for each channel. The ADC supports bipolar input ranges up to ±10.24 V with a single 5-V supply and provides minimum latency in data output resulting from the SAR architecture. The integration offered by this device makes the ADS8688AT an ideal selection for such applications, because the integrated signal conditioning helps minimize system components and avoids the need for generating high-voltage supply rails. The overall system-level dc precision (gain and offset errors) and low temperature drift offered by this device helps system designers achieve the desired system accuracy without calibration. In most applications, using passive RC filters or multi-stage filters in front of the ADC is preferred to reduce the noise of the input signal.

The software algorithm implemented in this design uses the discrete fourier transform (DFT) method to calculate and track the input signal frequency, obtain the exact phase angle of the individual signal, calculate the phase difference, and implement phase compensation. The entire algorithm has four steps:

- Calculate the theoretical phase difference introduced by the ADC resulting from multiplexing input channels
- Estimate the frequency of the input signal using frequency tracking and DFT techniques
- Calculate the phase angle of all signals in the system based on the estimated frequency
- Compensate the phase difference for all channels using the theoretical value of an additional MUX phase delay calculated in the first step

8.2.1.3 Application Curve

表 28 and 図 121 summarize the performance for this design. In this example, multiple sinusoidal input signals of an amplitude at ±10 V are applied to the inputs of the ADC. The initial phase angle is the same for all signals, but the input frequency is varied from 45 Hz to 55 Hz. The phase error in the last column of 表 28 reflects the measurement accuracy of this design.

表 28. Theoretical and Measured Phase Difference

INPUT TEST CONDITION	THEORETICAL PHASE ERROR(1)	MEASURED PHASE ERROR(2)	PHASE ERROR AFTER COMPENSATION(3)
Phase difference (consecutive channels)	0.036°	0.036145°	0.000145°
Phase difference (farthest channels, channel 0 to channel 7)	0.252°	0.249964°	0.002036°

(1) Theoretical phase difference introduced by multiplexing is calculated based on the formula: $\Delta\varphi = (f_{IN} / f_{ADC}) \times N \times 360°$, where N = integral gap between two channels in the multiplexer sequence; f_{IN} = input signal frequency; and f_{ADC} = 500 kSPS, maximum throughput of the ADC.
(2) Measured phase value (before compensation) includes phase difference between any two channels resulting from multiplexing ADC inputs.
(3) The algorithm subtracts theoretical phase difference from the measured phase to compensate for the phase difference resulting from the MUX inputs.

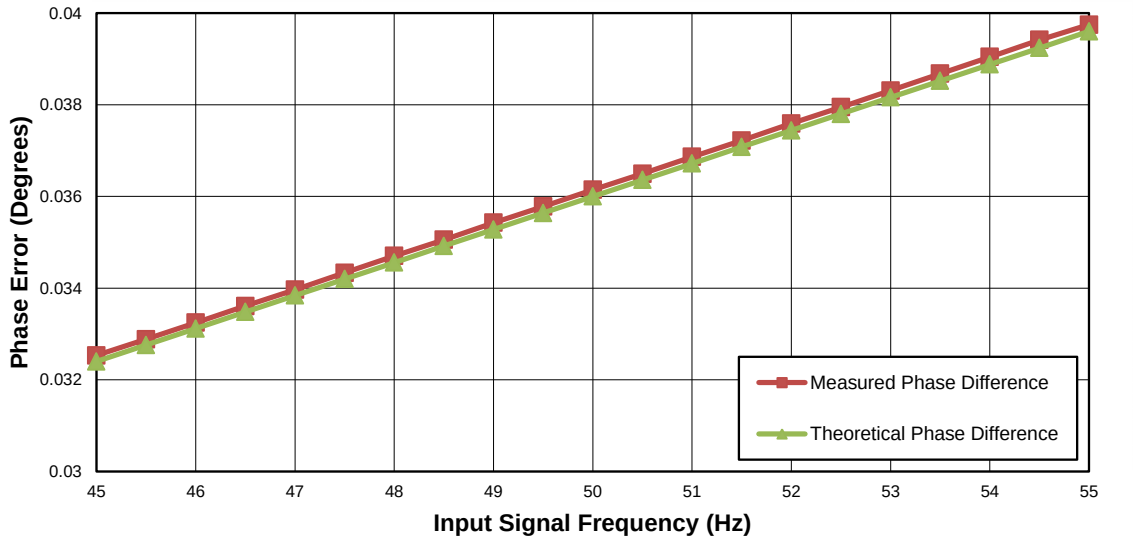


図 121. Measured and Theoretical Phase Difference Between Consecutive Channels

For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *Phase Compensated 8-Channel, Multiplexed Data Acquisition System for Power Automation Reference Design*.

8.2.2 16-Bit, 8-Channel, Integrated Analog Input Module for Programmable Logic Controllers (PLCs)

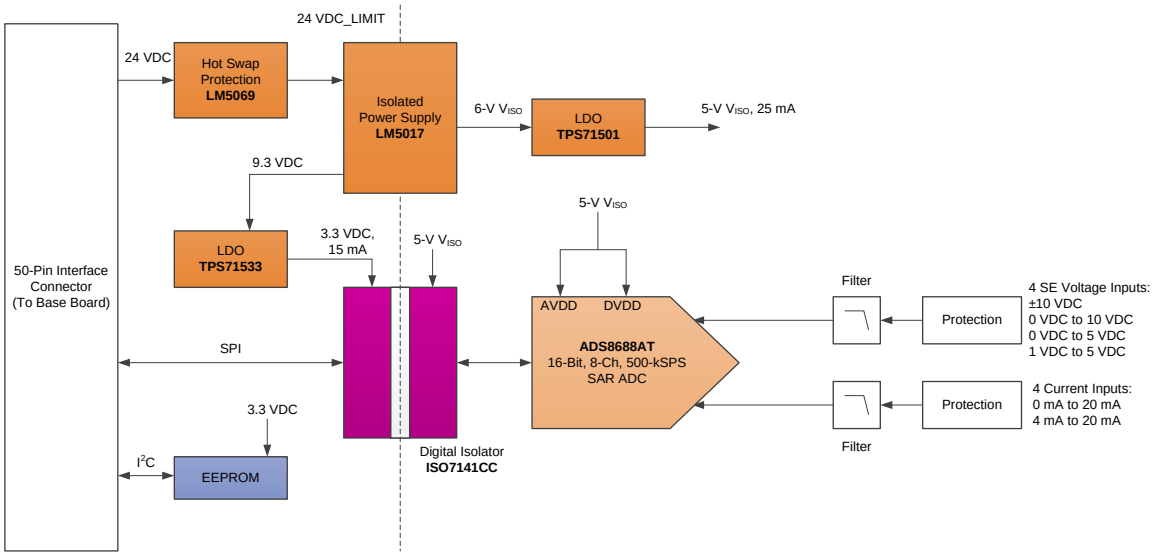


図 122. 16-Bit, 8-Channel, Integrated Analog Input Module for PLCs

8.2.2.1 Design Requirements

This reference design provides a complete solution for a single-supply industrial control analog input module. The design is suitable for process control end equipment, such as programmable logic controllers (PLCs), distributed control systems (DCSs), and data acquisition systems (DAS) modules that must digitize standard industrial current inputs, and bipolar or unipolar input voltage ranges up to ±10 V. In an industrial environment, the analog voltage and current ranges typically include ±2.5 V, ±5 V, ±10 V, 0 V to 5 V, 0 V to 10 V, 4 mA to 20 mA, and 0 mA to 20 mA. This reference design can measure all standard industrial voltage and current inputs. Eight channels are provided on the module, and each channel can be configured as a current or voltage input with software configuration.

The key design requirements are given below:

- Up to eight channels of user-programmable inputs:
  - Voltage inputs (with a typical Z_{IN} of 1 MΩ): ±10 V, ±5 V, ±2.5 V, 0 V to 10 V, and 0 V to 5 V
  - Current inputs (with a Z_{IN} of 300 Ω): 0 mA to 20 mA, 4 mA to 20 mA, and ±20 mA
- A 16-bit SAR ADC with SPI
- Accuracy of ≤ 0.2% at 25°C over the entire input range of voltage and current inputs
- Onboard isolated fly-buck™ power supply with inrush current protection
- Slim-form factor 96 mm × 50.8 mm × 10 mm (L × W × H)
- LabView-based GUI for signal-chain analysis and functional testing
- Designed to comply with IEC61000-4 standards for ESD, EFT, and surge

8.2.2.2 Detailed Design Procedure

The application circuit and system diagram for this design is illustrated in 図 122.

The module has eight analog input channels, and each channel can be configured as a current or voltage input with software configuration. This design can be implemented using the ADS8688AT, 16-bit, 8-channel, single-supply SAR ADC with an on-chip PGA and reference. The on-chip PGA provides a high-input impedance (typically 1 MΩ) and filters noise interference. The on-chip, 4.096-V, ultra-low drift voltage reference is used as the reference for the ADC core.

Digital isolation is achieved using an ISO7141CC and ISO1541. The host microcontroller communicates with a TCA6408A (an 8-bit, I^2C, I/O expander over an I^2C bus). The ISO1541D is a bidirectional, I^2C isolator that isolates the I^2C lines for the TCA6408A. The TCA6408A controls the low R_{ON} opto-switch that is used to switch between voltage-to-current input modes. The input channel configuration is done in microcontroller firmware.

A low-cost, constant, on-time, synchronous buck regulator in fly-buck configuration with an external transformer (LM5017) generates the isolated power supply. The LM5017 has a wide input supply range, making this device ideal for accepting a 24-V industrial supply. This transformer can accept up to 100 V, thereby making reliable transient protection of the input supply more easily achievable. The fly-buck power supply isolates and steps the input voltage down to 6 V. The supply then provides that voltage to the TPS70950 (the low dropout regulator) to generate 5 V to power the ADS8688AT and other circuitry. The LM5017 also features a number of other safety and reliability functions, such as undervoltage lockout (UVLO), thermal shutdown, and peak current limit protection.

Input analog signals are protected against high-voltage, fast-transient events often expected in an industrial environment. The protection circuitry makes use of the transient voltage suppressor (TVS) and ESD diodes. The RC low-pass mode filters are used on each analog input before the input reaches the ADS8688AT, thus eliminating any high-frequency noise pickups and minimizing aliasing.

8.2.2.3 Application Curve

表 29 summarizes the performance for this design.

表 29. Measurement Results Summary for PLC Analog Input Module Design

SERIAL NUMBER	PARAMETER	INPUT RANGE	ADS8688AT SPECIFICATION	MEASURED RESULT
1	SNR (dB)	±10 V	90 dB (min)	90.85 dB
		0 V 10 V	88.5 dB (min)	89.52 dB
		0 V to 5 V	87.5 dB (min)	88.48 dB
2	ENOB (Bits)	±10 V	14.66	14.80
		0 V 10 V	14.41	14.58
		0 V to 5 V	14.24	14.41
3	Maximum INL (LSB)	±10 V	2	1.77
		0 V 10 V	2	1.64
		0 V to 5 V	2	1.35
4	Minimum INL (LSB)	±10 V	–2	–1.47
		0 V 10 V	–2	–1.36
		0 V to 5 V	–2	–1.37

図 123 shows the accuracy performance for this design for the ±10.24-V input range.

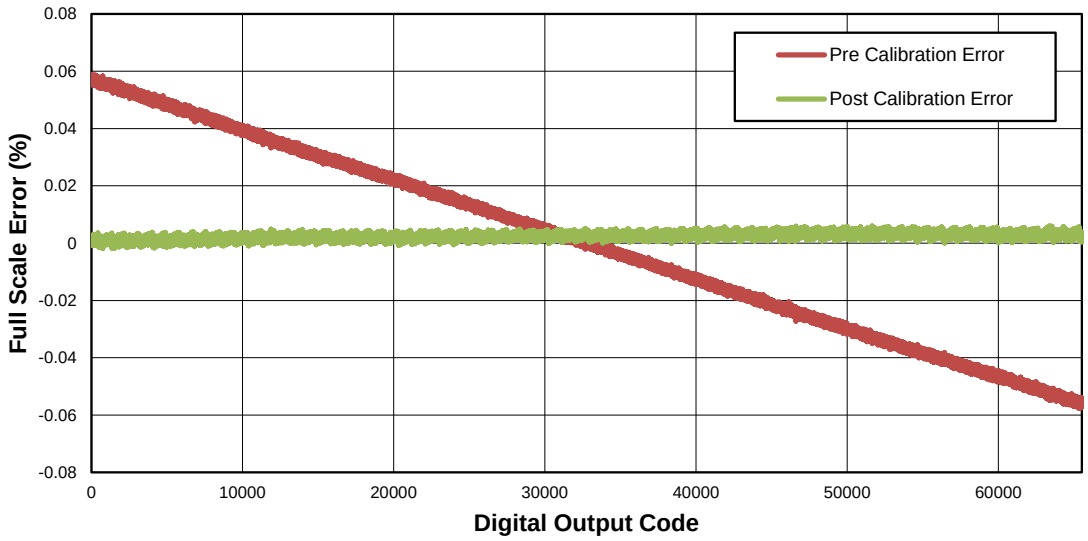


図 123. System Accuracy Performance in ±2.5 × V_{REF} Input Range

TI Precision Designs

For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *16-Bit, 8-Channel, Integrated Analog Input Module for Programmable Logic Controllers (PLCs)*.

9 Power Supply Recommendations

The device uses two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

The AVDD supply pins must be decoupled with AGND by using a minimum 10-µF and 1-µF capacitor on each supply. Place the 1-µF capacitor as close to the supply pins as possible. Place a minimum 10-µF decoupling capacitor very close to the DVDD supply to provide the high-frequency digital switching current. The effect of using the decoupling capacitor is illustrated in the difference between the power-supply rejection ratio (PSRR) performance of the device. 図 124 shows the PSRR of the device without using a decoupling capacitor. 図 125 shows that the PSRR improves when the decoupling capacitors are used.

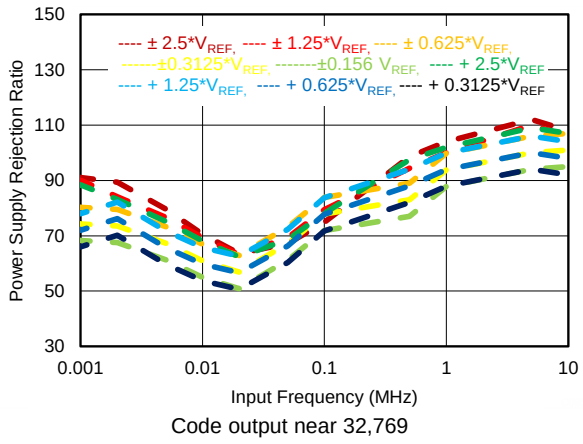


図 124. PSRR Without a Decoupling Capacitor

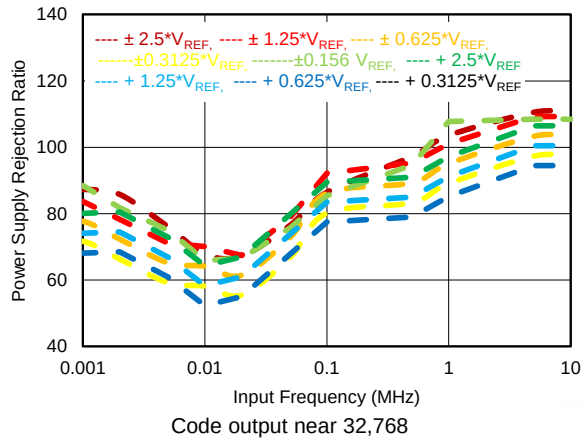


図 125. PSRR With a Decoupling Capacitor

10 Layout

10.1 Layout Guidelines

図 126 illustrates a PCB layout example for the ADS8688AT.

- Partition the PCB into analog and digital sections. Care must be taken to ensure that the analog signals are kept away from the digital lines. This layout helps keep the analog input and reference input signals away from the digital noise. In this layout example, the analog input and reference signals are routed on the lower side of the board and the digital connections are routed on the top side of the board.
- Using a single dedicated ground plane is strongly encouraged.
- Power sources to the ADS8688AT must be clean and well-bypassed. TI recommends using a 1-μF, X7R-grade, 0603-size ceramic capacitor with at least a 10-V rating in close proximity to the analog (AVDD) supply pins. For decoupling the digital (DVDD) supply pin, a 10-μF, X7R-grade, 0805-size ceramic capacitor with at least a 10-V rating is recommended. Placing vias between the AVDD, DVDD pins and the bypass capacitors must be avoided. All ground pins must be connected to the ground plane using short, low impedance paths.
- There are two decoupling capacitors used for the REFCAP pin. The first is a small, 1-μF, X7R-grade, 0603-size ceramic capacitor placed close to the device pins for decoupling the high-frequency signals and the second is a 22-μF, X7R-grade, 1210-size ceramic capacitor to provide the charge required by the reference circuit of the device. Both of these capacitors must be directly connected to the device pins without any vias between the pins and capacitors.
- The REFIO pin also must be decoupled with a 10-μF ceramic capacitor, if the internal reference of the device is used. The capacitor must be placed close to the device pins.
- For the auxiliary channel, the fly-wheel RC filter components must be placed close to the device. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

10.2 Layout Example

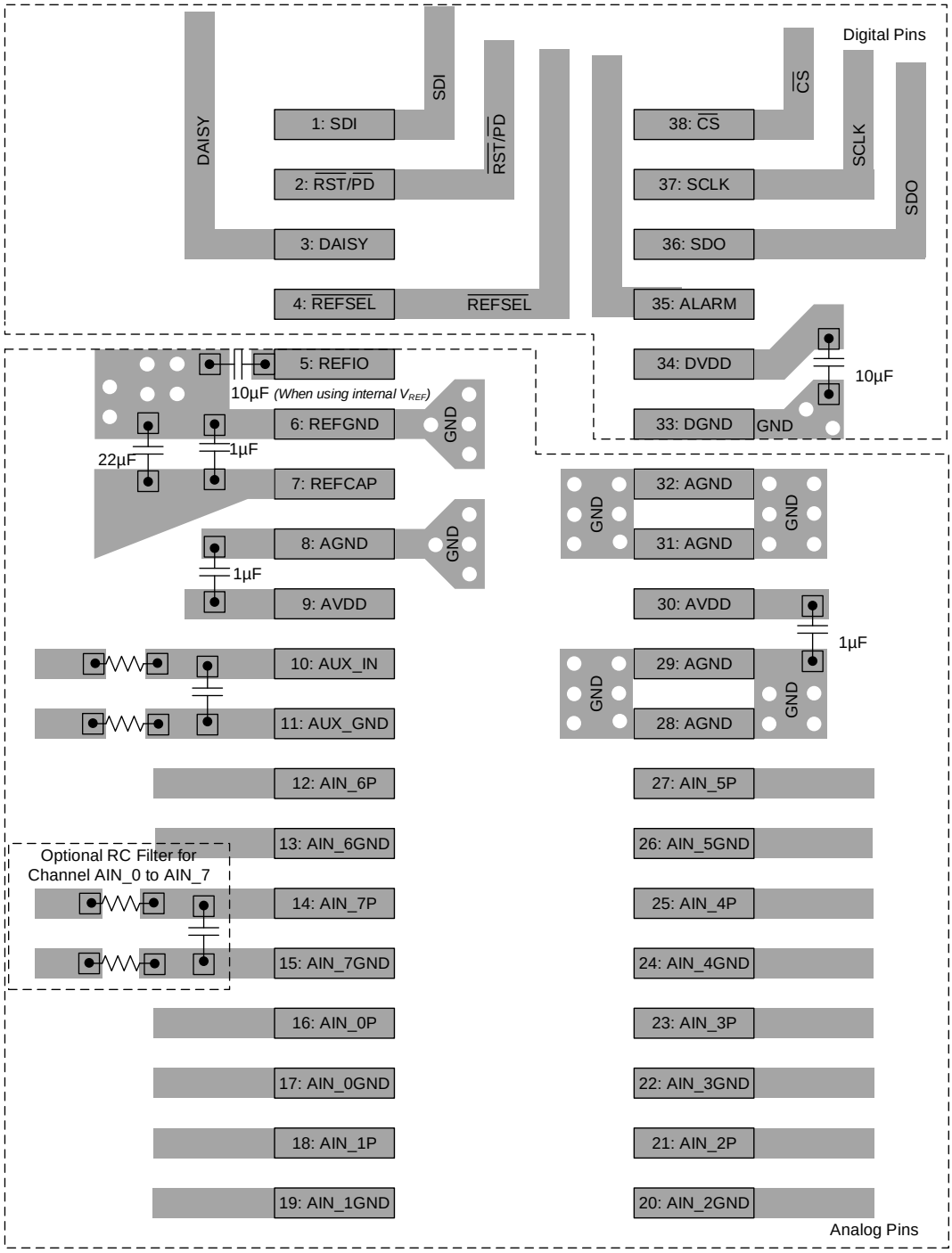


図 126. Board Layout for the ADS8688AT

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『ISO154x 低消費電力の双方向I^2Cアイソレータ』
- 『ISO71xxCC 4242V_{PK}、フットプリントの小さい低消費電力、トリプルおよびクワッド・チャネルのデジタル・アイソレータ』
- 『LM5017 100V、600mA、コンスタント・オンタイム方式同期整流降圧レギュレータ』
- 『OPA320 高精度、20MHz、0.9pA、低ノイズ、RRIO、シャットダウン搭載のCMOSオペアンプ』
- 『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』
- 『TCA6408A 割り込み出力、リセット、構成レジスタ内蔵の8ビットI^2C/SMBus I/Oエクスパンダ』
- 『TPS709 150mA、30V、1μA IQ、イネーブル機能付きの電圧レギュレータ』
- 『AN-2029 取り扱いおよびプロセスの推奨事項』アプリケーション・レポート
- 『16ビット、8チャネル、ソフトウェア構成可能な、プログラマブル・ロジック・コントローラ(PLC)用のアナログ入力モジュール』
- 『電力自動化用の位相補償、8チャネル、多重化データ収集システムのリファレンス・デザイン』

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

fly-buck, E2E are trademarks of Texas Instruments.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8688ATDBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ADS8688AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

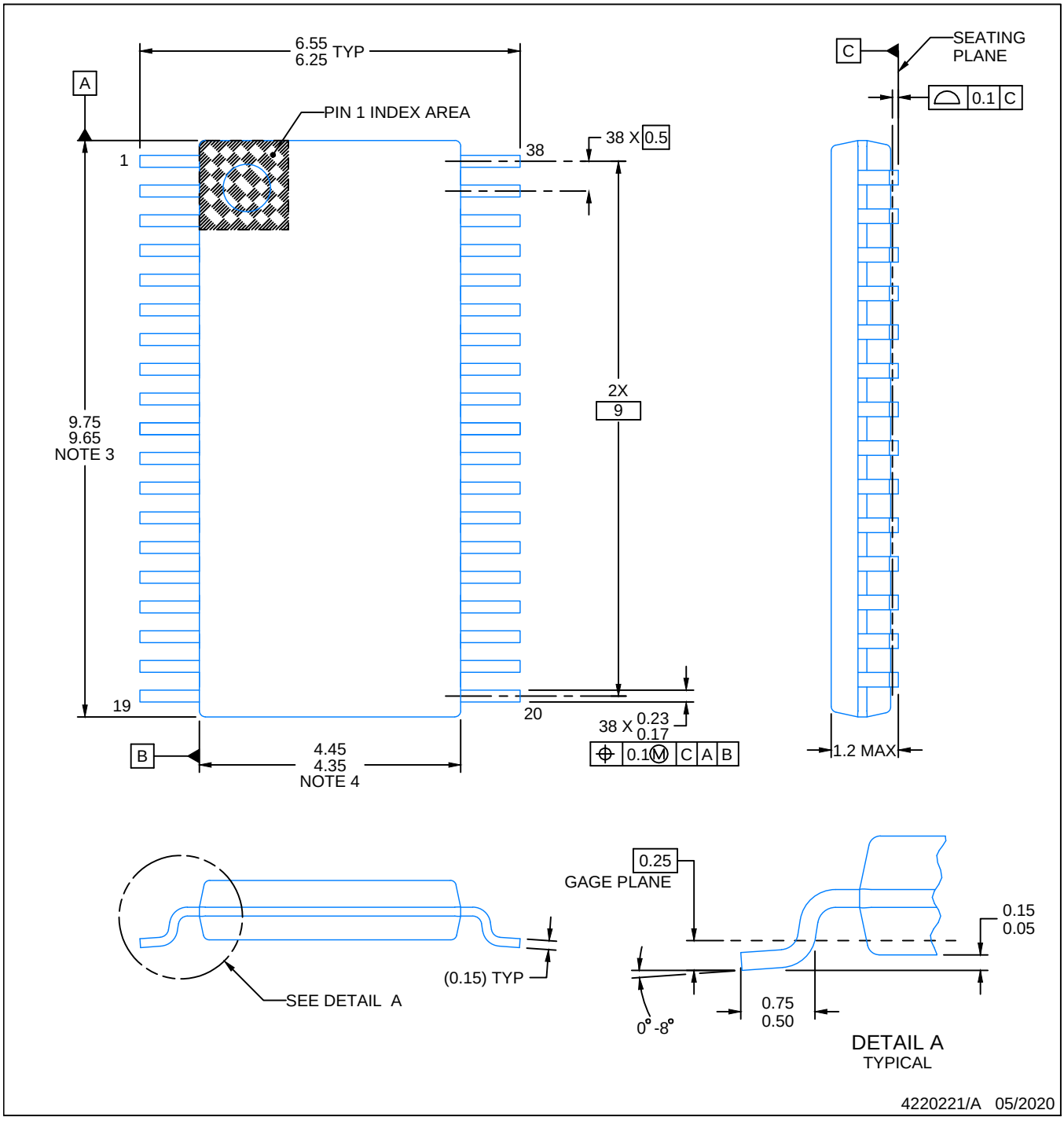
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBT0038A

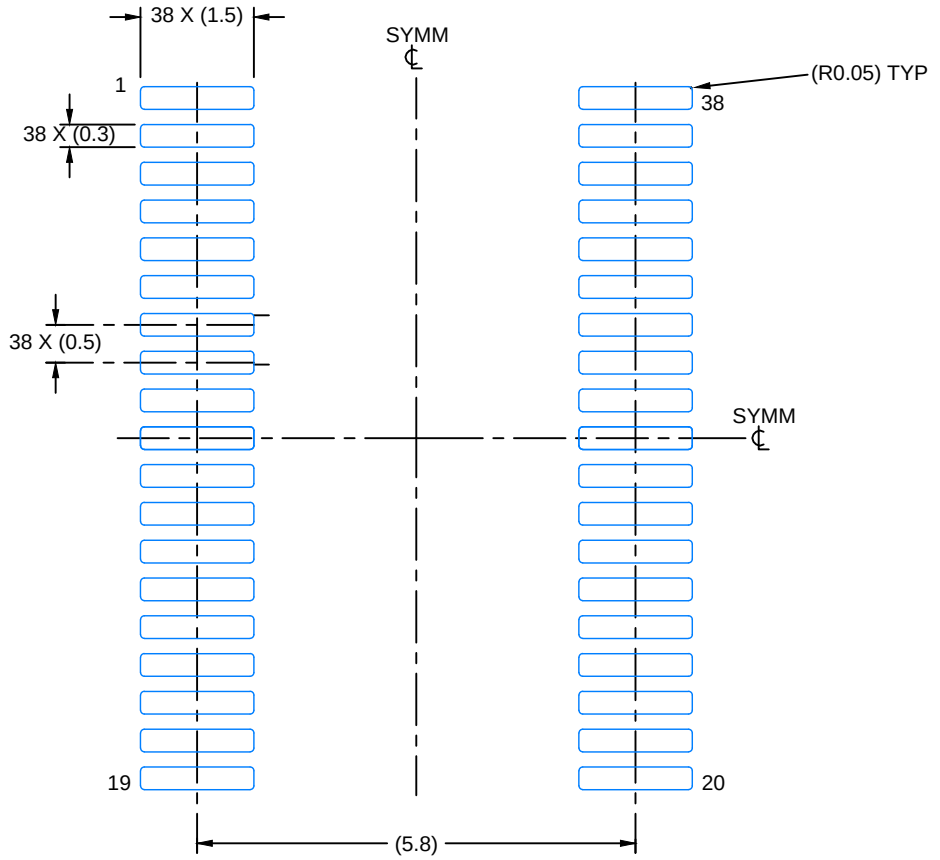
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

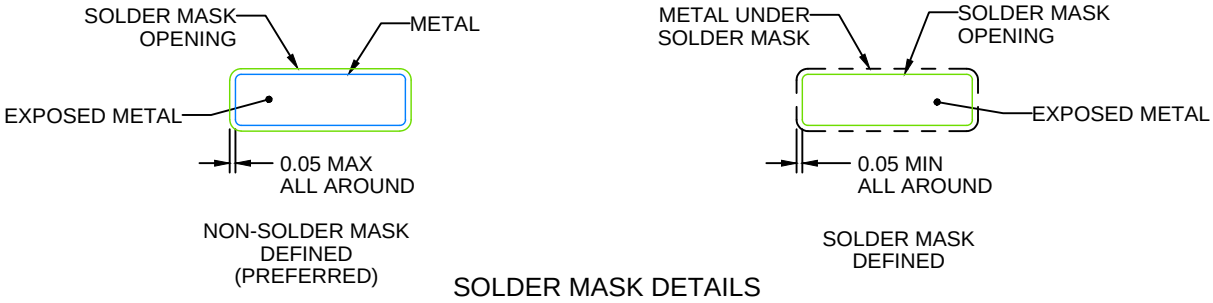


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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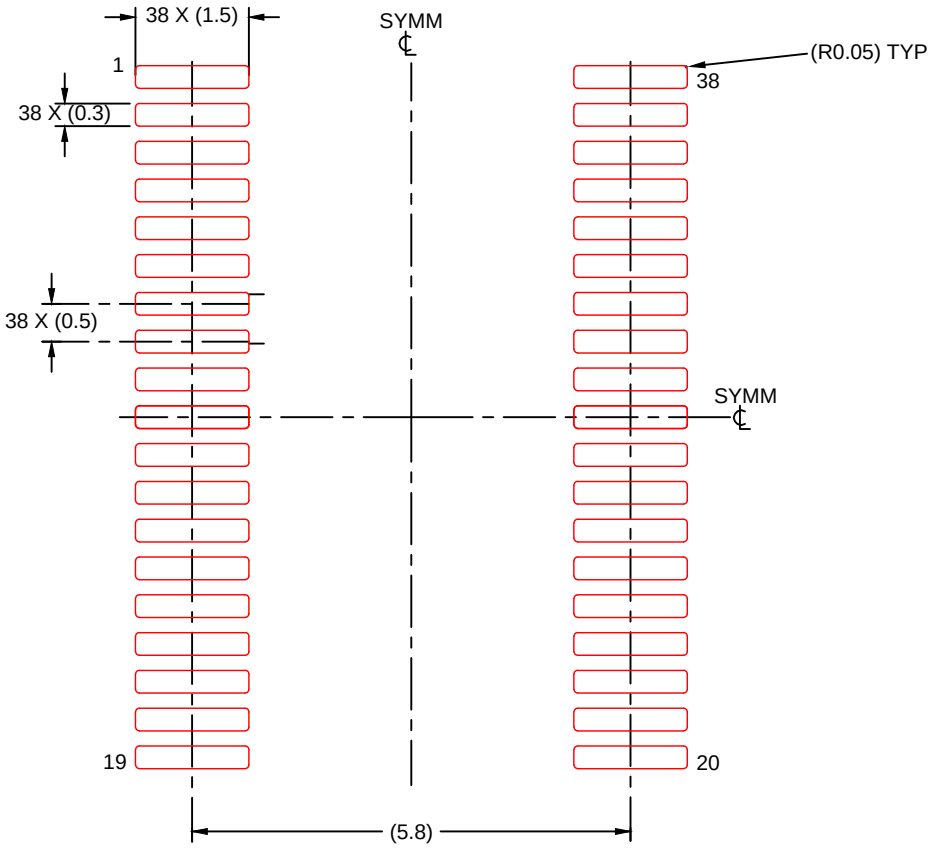
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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