

AFE539F1-Q1 車載用、定電力放電向け 10 ビット・スマート・アナログ・フロント・エンド、PWM 出力付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: -40°C ~ +125°C, T_A
- 定電力散逸制御ステート・マシン
 - 10 ビット A/D コンバータ (ADC) 入力
 - デューティ・サイクル 7 ビットのパルス幅変調 (PWM) 出力
 - 不揮発性メモリ (NVM) からのスタンドアロン動作
- I²C/SPI を自動検出
 - V_{IH}: 1.62V (V_{DD} = 5.5V の場合)
- VREF/MODE ピンにより、プログラミング・モードとスタンドアロン・モードのどちらかを選択
- ユーザーがプログラム可能な NVM
- 内部、外部、VDD の基準電圧
- 幅広い動作範囲
 - 電源: 1.8V ~ 5.5V
- 超小型パッケージ: 16 ピン WQFN (3mm × 3mm)

2 アプリケーション

- 車載用 DC リンク・コンデンサ放電回路
- エレベータ主制御パネル

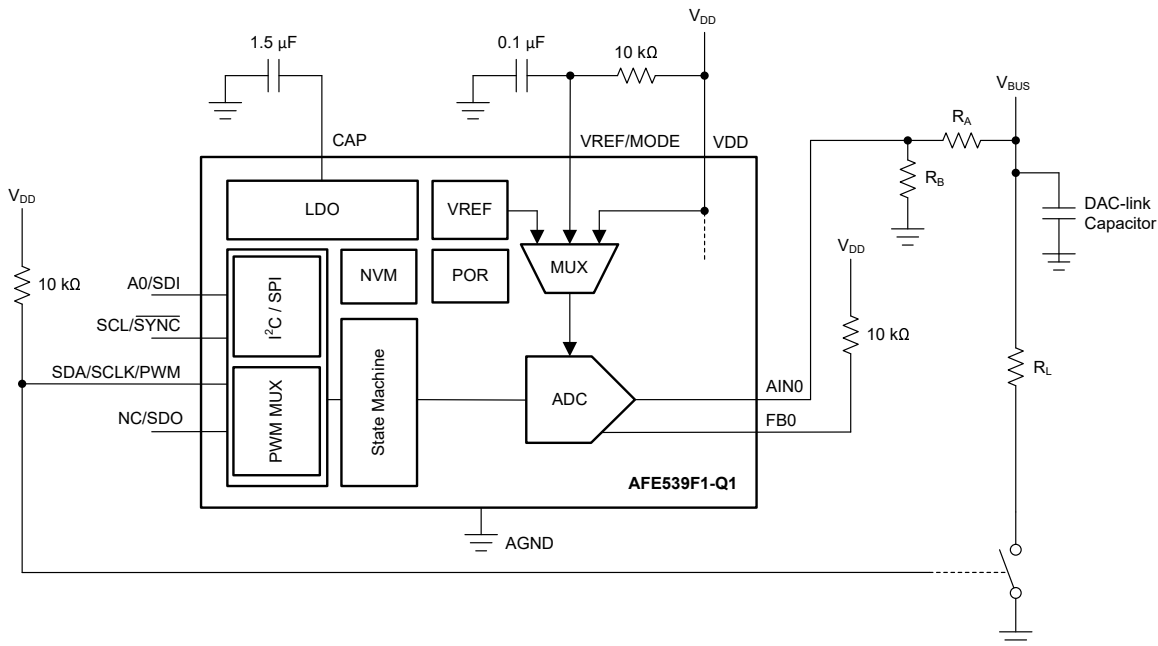
3 概要

AFE539F1-Q1 は、定電力散逸制御を目的とした 10 ビットのスマート・アナログ・フロント・エンド (AFE) です。AFE539F1-Q1 は、抵抗性負荷において定電力散逸を必要とするあらゆる場所で、印加電圧にかかわらず独立に使用できます。AFE539F1-Q1 は、ADC 入力と PWM 出力を備えています。このデバイスは、定電力散逸コントローラとしてあらかじめプログラムされたステート・マシンを内蔵しています。AFE539F1-Q1 は、車載用 DC リンク・コンデンサ放電回路や、一般的な定電力加熱アプリケーション向けの優れた選択肢になります。AFE539F1-Q1 は、NVM にプログラムされたパラメータとは独立して動作するため、このスマート AFE をプロセッサレス・アプリケーションや設計の再利用に使用できます。また、このデバイスは、I²C と SPI の自動検出、および内部基準電圧を備えています。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ・サイズ ⁽²⁾
AFE539F1-Q1	RTE (WQFN, 16)	3mm × 3mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



AFE539F1-Q1 を使用した定電力放電回路



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4 Revision History

DATE	REVISION	NOTES
July 2023	*	Initial release

5 Pin Configuration and Functions

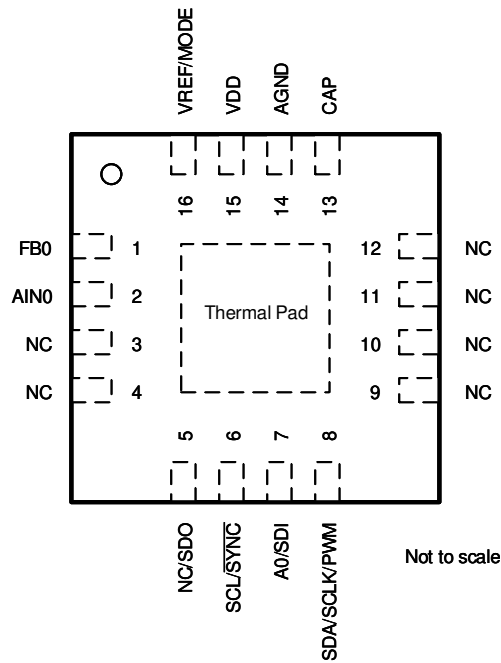


图 5-1. RTE Package, 16-pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	FB0	Input	Connect this pin to VDD with a pullup resistor.
2	AIN0	Input	Analog input for ADC0.
3	NC	—	Not connected.
4	NC	—	Not connected.
5	NC/SDO	Input/ Output	This pin is configurable as SDO. For SDO function, connect this pin to the IO voltage with an external pullup resistor. Leave this pin unconnected if not configured as SDO.
6	SCL/SYNC	Output	I ² C serial interface clock or SPI chip select input. Connect this pin to the IO voltage using an external pullup resistor.
7	A0/SDI	Input	Address configuration input for I ² C or serial data input for SPI. In A0 function, connect this pin to VDD, AGND, SDA, or SCL for address configuration. In SDI function, this pin does not need to be pulled up or pulled down.
8	SDA/ SCLK/PWM	Input/ Output	Bidirectional I ² C serial data bus or SPI clock input. Connect this pin to the IO voltage using an external pullup resistor. This pin acts as the PWM output for constant power-dissipation control. Pull the VREF/MODE pin high to enable PWM output.
9	NC	—	Not connected.
10	NC	—	Not connected.
11	NC	—	Not connected.
12	NC	—	Not connected.
13	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 μ F) between CAP and AGND.
14	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	Power	Supply voltage: 1.8 V to 5.5 V

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
16	VREF/ MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 μ F) between VREF/MODE and AGND. Use a pullup resistor to VDD when the external reference is not used. Make sure that this pin does not ramp up before VDD. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. In interface select mode. Pull this pin low to enable I ² C/SPI communication. Pull this pin high to enable PWM output.
Thermal pad	Thermal Pad	Ground	Connect the thermal pad to AGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage, V _{DD} to AGND	-0.3	6	V
	Digital inputs to AGND	-0.3	V _{DD} + 0.3	V
	V _{FBX} to AGND	-0.3	V _{DD} + 0.3	V
	A _{IN0} to AGND	-0.3	V _{DD} + 0.3	V
V _{REF}	External reference, V _{REF} to AGND	-0.3	V _{DD} + 0.3	V
	Current into any pin except the AIN0, VDD, and AGND pins	-10	10	mA
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level 2	±2000	V	
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)		±750
			All pins		±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Positive supply voltage to ground (AGND)	1.7		5.5	V
V _{REF}	External reference to ground (AGND)	1.7		V _{DD}	V
V _{IH}	Digital input high voltage, 1.7 V < V _{DD} ≤ 5.5 V	1.62			V
V _{IL}	Digital input low voltage			0.4	V
C _{CAP}	External capacitor on CAP pin	0.5		15	µF
T _A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AFE539F1-Q1	
		RTE (WQFN)	
		16 PINS	
			UNIT
R _{θJA}	Junction-to-ambient thermal resistance	49	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50	°C/W
R _{θJB}	Junction-to-board thermal resistance	24.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	24.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	8.7	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics: ADC Input

minimum and maximum specifications at $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and typical specifications at $T_A = 25^{\circ}\text{C}$, $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, reference input tied to VDD, gain = 1 ×, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
INL	Integral nonlinearity ^{(1) (2)}		-2		2	LSB
DNL	Differential nonlinearity ^{(1) (2)}		-1		1	LSB
	Offset error ^{(1) (2)}	$1.7\text{ V} \leq V_{DD} < 2.7\text{ V}$	-5	0	5	mV
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-5	0	5	
	Gain error ^{(1) (2)}		-1		1	%FSR
INPUT						
	Input voltage range	External $V_{REF} = V_{DD}$	0		V_{DD}	V
DYNAMIC PERFORMANCE						
	Data rate ⁽²⁾	ADC averaging setting is 4 samples	1406		2008	SPS
	Sampling capacitor			10		pF

- (1) For external reference and internal reference $V_{DD} \geq 1.21 \times \text{gain} + 0.2\text{ V}$, between end-point codes: 8d to 1016d.
 (2) Specified by design and characterization, not production tested.

6.6 Electrical Characteristics: General

minimum and maximum specifications at $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and typical specifications at $T_A = 25^{\circ}\text{C}$, $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, reference input tied to VDD, gain = 1 × and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
	Initial accuracy	$T_A = 25^{\circ}\text{C}$ for all measurements	1.1979	1.212	1.224	V
	Reference output temperature coefficient ^{(1) (2)}				60	ppm/ $^{\circ}\text{C}$
EXTERNAL REFERENCE						
	External reference input range		1.7		V_{DD}	V
	V_{REF} input impedance ⁽¹⁾			192		k Ω
EEPROM						
	Endurance ⁽¹⁾	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		20000		Cycles
		$T_A = 125^{\circ}\text{C}$		1000		
	Data retention ⁽¹⁾			50		Years
	EEPROM programming write cycle time ⁽¹⁾				200	ms
	Device boot-up time ⁽¹⁾	Time taken from power valid ($V_{DD} \geq 1.7\text{ V}$) to output valid state (output state as programmed in EEPROM), 0.5- μF capacitor on the CAP pin		5		ms
DIGITAL INPUTS						
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into VDD	Sleep mode, internal reference powered down, external reference at 5.5 V			28	μA
		Sleep mode, internal reference enabled, additional current through internal reference		10		
	Current flowing into VDD ⁽¹⁾	ADC channel enabled, internal reference enabled, additional current through internal reference			12.5	$\mu\text{A-ch}$
		Normal operation, state-machine enabled			900	μA

(1) Specified by design and characterization, not production tested.

(2) Measured at -40°C and $+125^{\circ}\text{C}$ and calculated the slope.

6.7 Timing Requirements: I²C Standard Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{ V} \leq V_{pull-up} \leq V_{DD}$

		MIN	NOM	MAX	UNIT
f _{SCLK}	SCL frequency			100	kHz
t _{BUF}	Bus free time between stop and start conditions	4.7			μs
t _{HDSTA}	Hold time after repeated start	4			μs
t _{SUSTA}	Repeated start setup time	4.7			μs
t _{SUSTO}	Stop condition setup time	4			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	250			ns
t _{LOW}	SCL clock low period	4700			ns
t _{HIGH}	SCL clock high period	4000			ns
t _F	Clock and data fall time			300	ns
t _R	Clock and data rise time			1000	ns
t _{VDDAT}	Data valid time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			3.45	μs
t _{VDACK}	Data valid acknowledge time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			3.45	μs

6.8 Timing Requirements: I²C Fast Mode

all input signals are timed from VIL to 70% of $V_{pull-up}$, $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{ V} \leq V_{pull-up} \leq V_{DD}$

		MIN	NOM	MAX	UNIT
f _{SCLK}	SCL frequency			400	kHz
t _{BUF}	Bus free time between stop and start conditions	1.3			μs
t _{HDSTA}	Hold time after repeated start	0.6			μs
t _{SUSTA}	Repeated start setup time	0.6			μs
t _{SUSTO}	Stop condition setup time	0.6			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	100			ns
t _{LOW}	SCL clock low period	1300			ns
t _{HIGH}	SCL clock high period	600			ns
t _F	Clock and data fall time			300	ns
t _R	Clock and data rise time			300	ns
t _{VDDAT}	Data valid time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			0.9	μs
t _{VDACK}	Data valid acknowledge time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			0.9	μs

6.9 Timing Requirements: I²C Fast Mode Plus

all input signals are timed from VIL to 70% of $V_{pull-up}$, $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, and $1.7\text{ V} \leq V_{pull-up} \leq V_{DD}$

		MIN	NOM	MAX	UNIT
f _{SCLK}	SCL frequency			1	MHz
t _{BUF}	Bus free time between stop and start conditions	0.5			μs
t _{HDSTA}	Hold time after repeated start	0.26			μs
t _{SUSTA}	Repeated start setup time	0.26			μs
t _{SUSTO}	Stop condition setup time	0.26			μs
t _{HDDAT}	Data hold time	0			ns
t _{SUDAT}	Data setup time	50			ns
t _{LOW}	SCL clock low period	0.5			μs
t _{HIGH}	SCL clock high period	0.26			μs
t _F	Clock and data fall time			120	ns
t _R	Clock and data rise time			120	ns
t _{VDDAT}	Data valid time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			0.45	μs
t _{VDACK}	Data valid acknowledge time, R = 360 Ω, C _{trace} = 23 pF, C _{probe} = 10 pF			0.45	μs

6.10 Timing Requirements: SPI Write Operation

all input signals are specified with $t_r = t_f = 1 \text{ V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$, $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			50	MHz
t_{SCLKHIGH}	SCLK high time	9			ns
t_{SCLKLOW}	SCLK low time	9			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	18			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	50			ns
t_{DACWAIT}	Sequential update wait time (time between subsequent $\overline{\text{SYNC}}$ rising edges) for same channel	2			μs

6.11 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with $t_r = t_f = 1 \text{ V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$, $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, and $\text{FSDO} = 0$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			1.25	MHz
t_{SCLKHIGH}	SCLK high time	350			ns
t_{SCLKLOW}	SCLK low time	350			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	400			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	400			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	1			μs
t_{SDODLY}	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$, $C_L = 20 \text{ pF}$			300	ns

6.12 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with $t_r = t_f = 1 \text{ V/ns}$ (10% to 90% of V_{IO}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$, $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$, $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, and $\text{FSDO} = 1$

		MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency			2.5	MHz
t_{SCLKHIGH}	SCLK high time	175			ns
t_{SCLKLOW}	SCLK low time	175			ns
t_{SDIS}	SDI setup time	8			ns
t_{SDIH}	SDI hold time	8			ns
t_{CSS}	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	300			ns
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	300			ns
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time	1			μs
t_{SDODLY}	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$, $C_L = 20 \text{ pF}$			300	ns

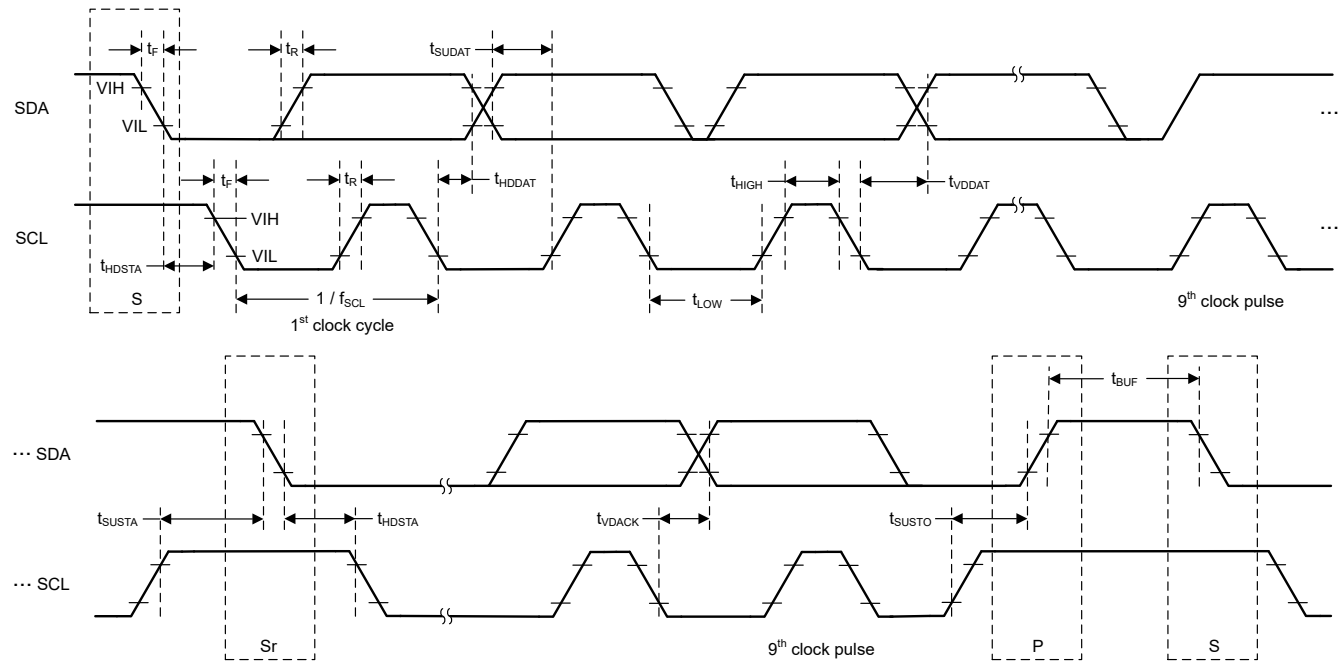
6.13 Timing Requirements: PWM Output

all input signals are timed from VIL to 70% of $V_{pull-up}$, $1.7 V \leq V_{DD} \leq 5.5$, $-40^{\circ}C \leq T_A \leq +125^{\circ}C$, and $1.7 V \leq V_{pull-up} \leq V_{DD}$

		MIN	NOM	MAX	UNIT
f_{PWMOUT}	PWM frequency ⁽¹⁾	0.218		48.828	kHz
t_{PWMOHI}	PWM high time	1			μs
t_{PWMOLO}	PWM low time	1			μs
$t_{PWMODTY}$	PWM duty cycle	0		100	%

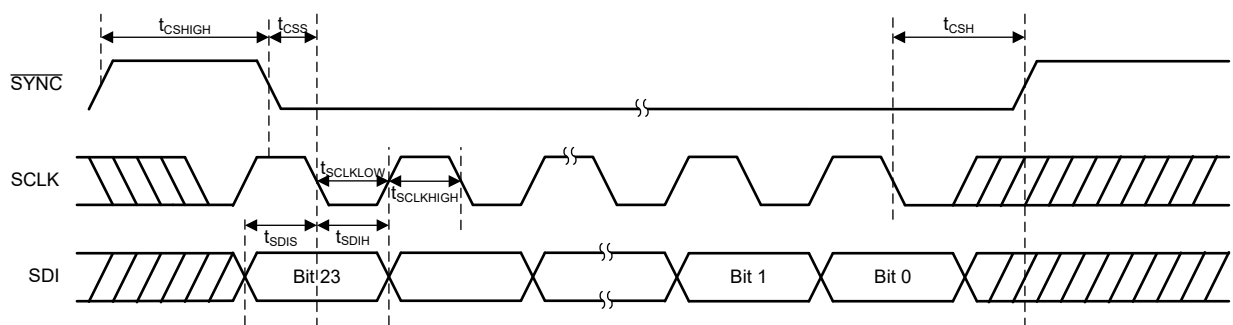
(1) The frequency range does not account for the internal oscillator frequency error.

6.14 Timing Diagrams

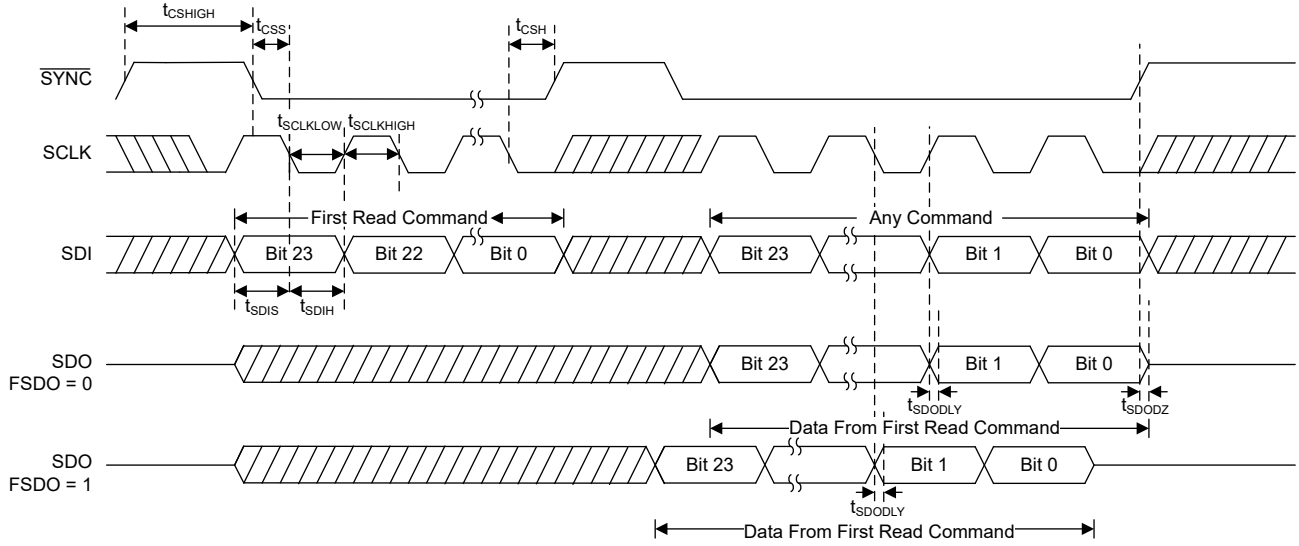


S: Start bit, Sr: Repeated start bit, P: Stop bit

6-1. I²C Timing Diagram



6-2. SPI Write Timing Diagram



6-3. SPI Read Timing Diagram

6.15 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{ V}$, external reference = 5.5 V, and gain = 1 × (unless otherwise noted)

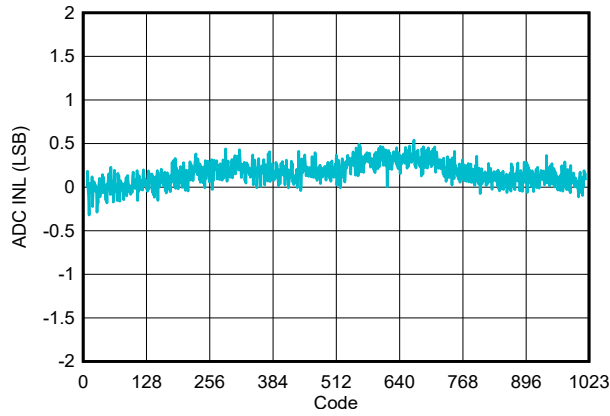


图 6-4. ADC INL vs Digital Output Code

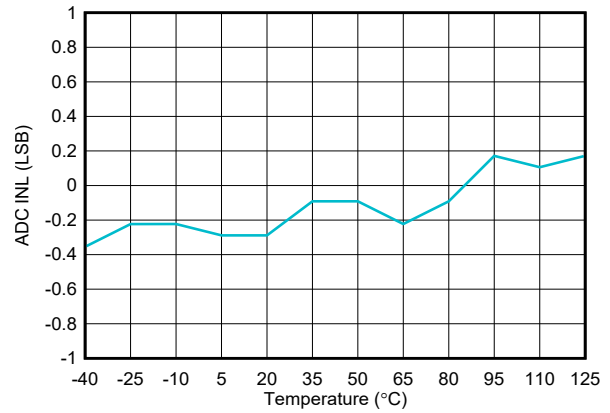


图 6-5. ADC INL vs Temperature

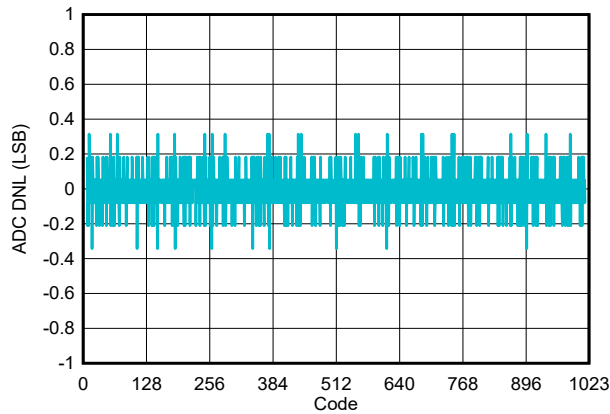


图 6-6. ADC DNL vs Digital Output Code

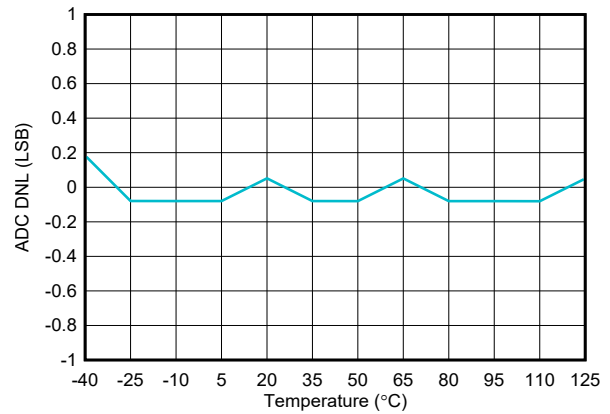


图 6-7. ADC DNL vs Temperature

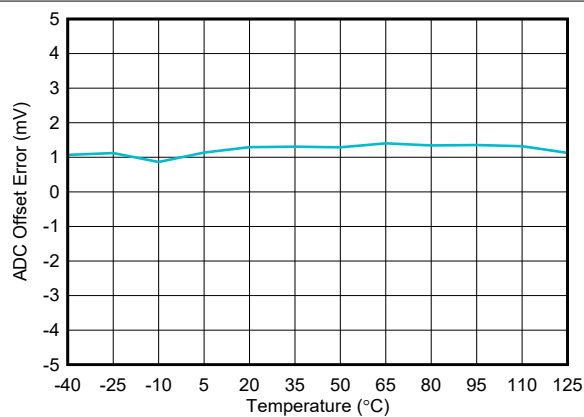


图 6-8. ADC Offset Error vs Temperature

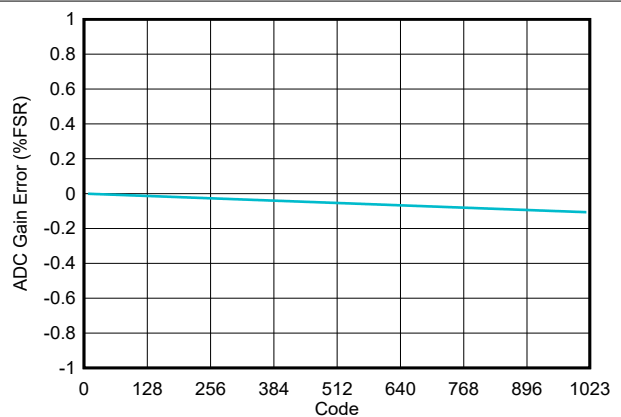
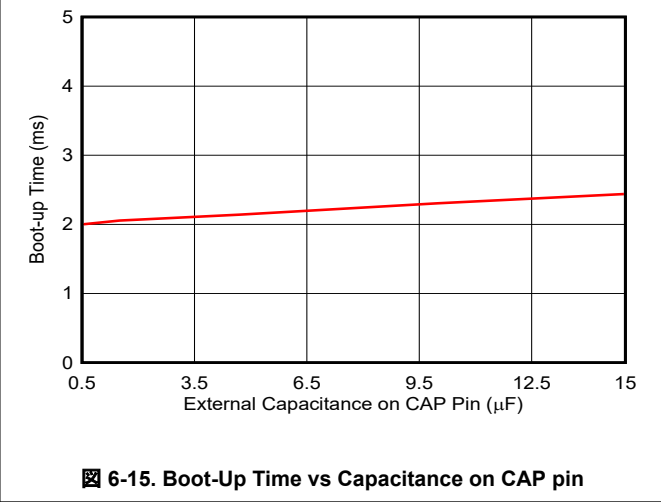
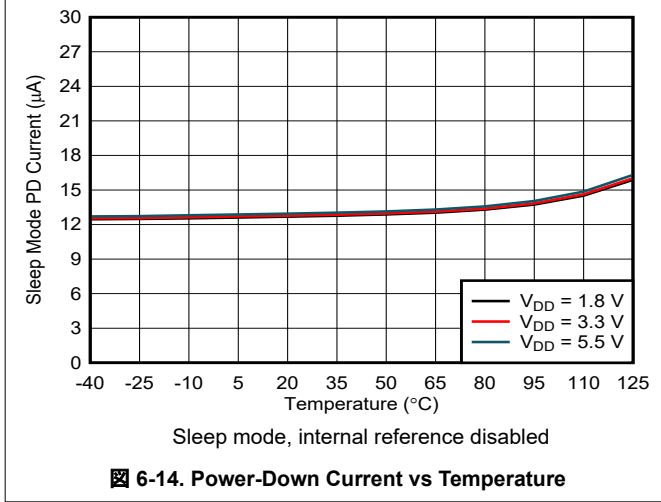
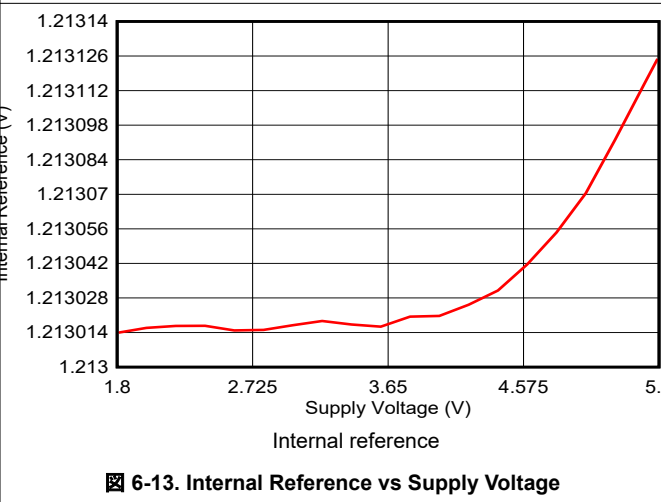
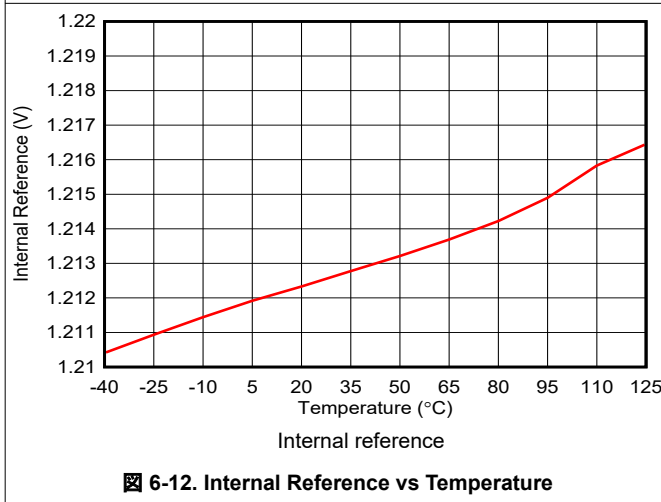
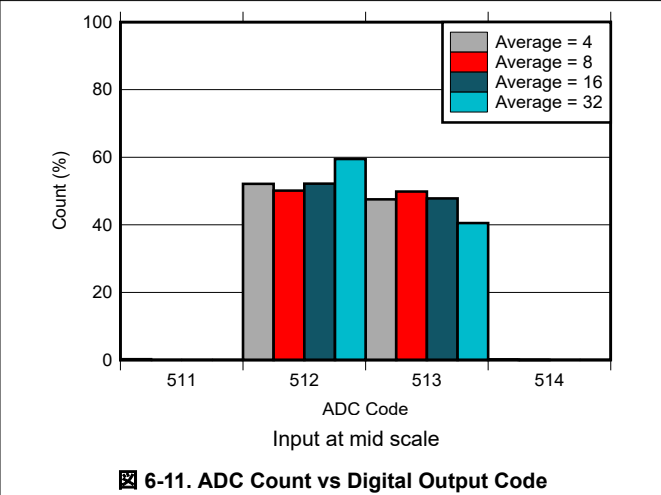
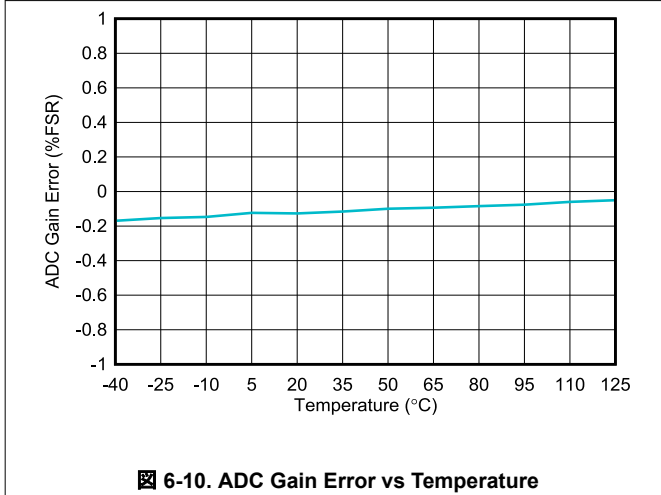


图 6-9. ADC Gain Error vs Digital Output Code

6.15 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5.5\text{ V}$, external reference = 5.5 V, and gain = 1 × (unless otherwise noted)



7 Detailed Description

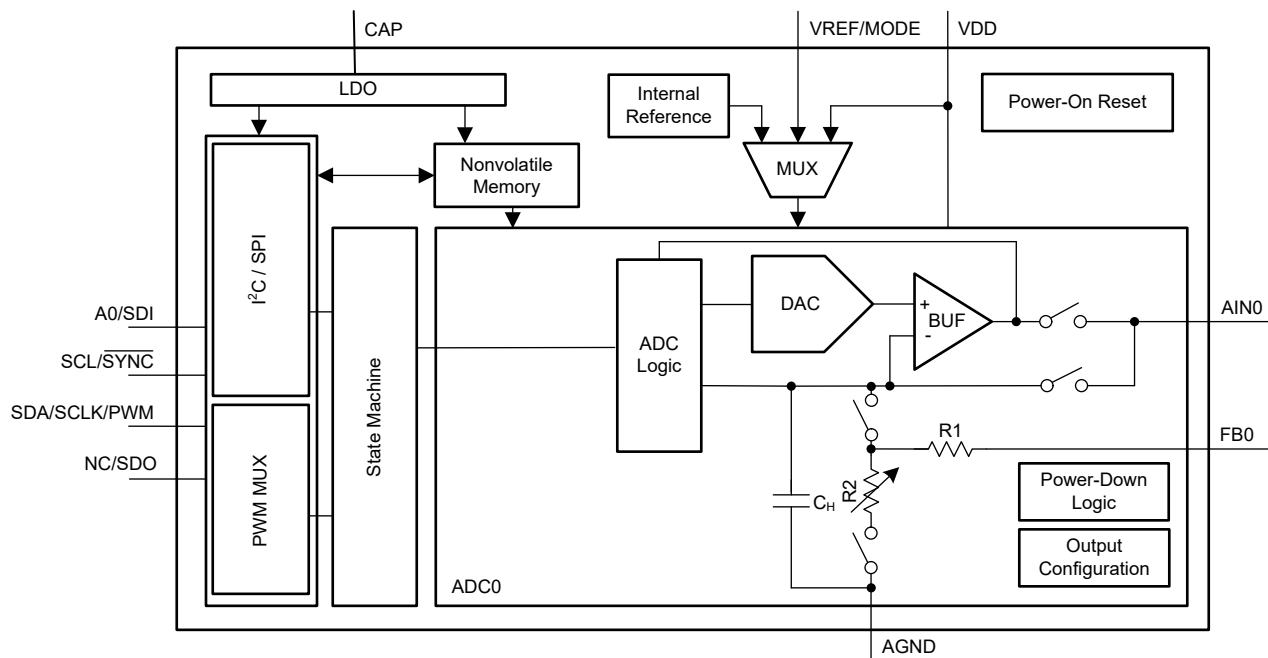
7.1 Overview

The AFE539F1-Q1 is a 10-bit smart analog front end (AFE) with PWM output and ADC input. The SDA/SCLK pin is re-purposed as the PWM output when the VREF/MODE pin is held high.

The AFE539F1-Q1 provides a preprogrammed state machine that functions as a constant power-dissipation or heating controller. This device contains nonvolatile memory (NVM), an internal reference, automatically detects I²C and SPI, and a general-purpose input. The device supports Hi-Z power-down modes by default, which can be configured to 10 k Ω -AGND or 100 k Ω -AGND using the NVM. The AFE539F1-Q1 has a power-on-reset (POR) circuit that makes sure all the registers start with default or user-programmed settings using NVM. The AFE539F1-Q1 operates with either an internal reference, external reference, or with power supply as the reference.

The AFE539F1-Q1 supports I²C standard mode (100Kbps), fast mode (400Kbps), and fast mode plus (1Mbps). The I²C interface can be configured with four device addresses using the A0 pin. The SPI mode supports a three-wire interface by default, with up to 25-MHz SCLK input. The NC/SDO input can be configured as SDO in the NVM for SPI read capability. The AFE539F1-Q1 is designed for constant power dissipation in automotive DC-link capacitor discharge circuits and constant power heating applications. The state machine and NVM enable *processor-less* operation. Because of the *smart* feature set, the AFE539F1-Q1 is called a smart AFE.

7.2 Functional Block Diagram

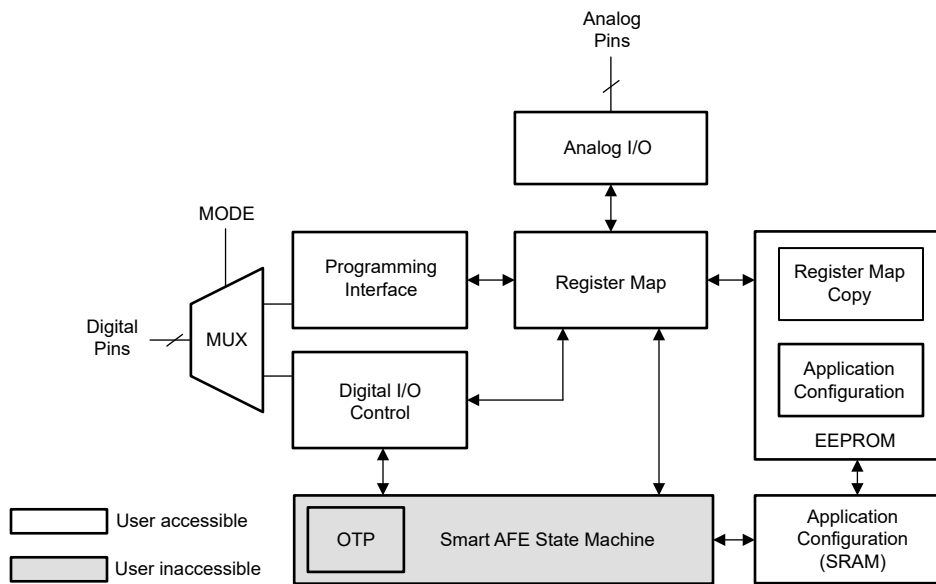


7.3 Feature Description

7.3.1 Smart Analog Front End (AFE) Architecture

The AFE539F1-Q1 smart analog front end (AFE) consists of a 10-bit analog-to-digital converter (ADC) input and a 7-bit duty-cycle pulse-width modulation (PWM) output. The ADC uses a successive-approximation register (SAR) architecture. The DAC inside the ADC uses a string architecture. The PWM output is multiplexed with one of the digital interface pins. セクション 7.2 shows the smart AFE architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply. The device has an internal voltage reference of 1.21 V. There is an option to select an external reference on the VREF/MODE pin or use the power supply as a reference. The ADC uses one of these three reference options.

The AFE539F1-Q1 features a preprogrammed state machine supporting constant power-dissipation control operation. 図 7-1 shows the digital architecture of the smart AFE with the interconnections between different functional blocks. This state machine allows the user to program the coefficients and input-output parameters. The state machine can be disabled by writing to the STATE-MACHINE-CONFIG0 register. The user configurations are stored in the NVM and the state machine can be operated in standalone mode without interfacing to a processor (*processor-less operation*).




7-1. Smart AFE Architecture

7.3.2 Programming Interface

The AFE539F1-Q1 have five digital I/O pins that control I²C, SPI, PWM, and mode selection. The VREF/MODE pin must be at logic low to enable the programming interface. These devices automatically detect I²C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I²C interface uses the A0 pin to select from among four address options. The SPI is a three-wire interface by default. No readback capability is available in three-wire SPI mode. The NC/SDO pin can be configured as the SDO function in the register map and then programmed into the NVM. With the NC/SDO pin acting as SDO, the SPI works as a four-wire interface. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I²C: SCL, SDA, A0
- SPI: SCLK, SDI, $\overline{\text{SYNC}}$, NC/SDO

All the digital pins are open drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external resistors.

7.3.3 Nonvolatile Memory (NVM)

The AFE539F1-Q1 contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain set values in the absence of a power supply. The highlighted gray cells in the *Register Map* show all the register bits that can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG bit autoresets. The NVM-BUSY bit in the GENERAL-STATUS register is set to 1 by the device when an NVM write or reload operation is ongoing. During this time, the device blocks all read and write operations from and to the device. The NVM-BUSY bit is set to 0 after the write or reload operation is complete; at this point, all read and write operations from and to the device are allowed. The default value for all the registers in the AFE539F1-Q1 is loaded from NVM as soon as a POR event is issued.

The AFE539F1-Q1 also implements a NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. The NVM-reload operation overwrites the register map with the stored data from the NVM. After completion, the device autoresets this bit to 0. During the NVM-RELOAD operation, the NVM-BUSY bit is set to 1.

7.3.3.1 NVM Cyclic Redundancy Check (CRC)

The AFE539F1-Q1 implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in the AFE539F1-Q1:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time the NVM program operation (write or reload) is performed and during the device boot up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

7.3.3.1.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see [セクション 7.3.5](#)) command, or cycle power to the device. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

7.3.3.1.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see [セクション 7.3.5](#)) command or cycle power to the device. A permanent failure in the NVM makes the device unusable.

7.3.4 Power-On Reset (POR)

The AFE539F1-Q1 includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the AFE539F1-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in [Figure 7-2](#), to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.65 V, a POR does not occur.

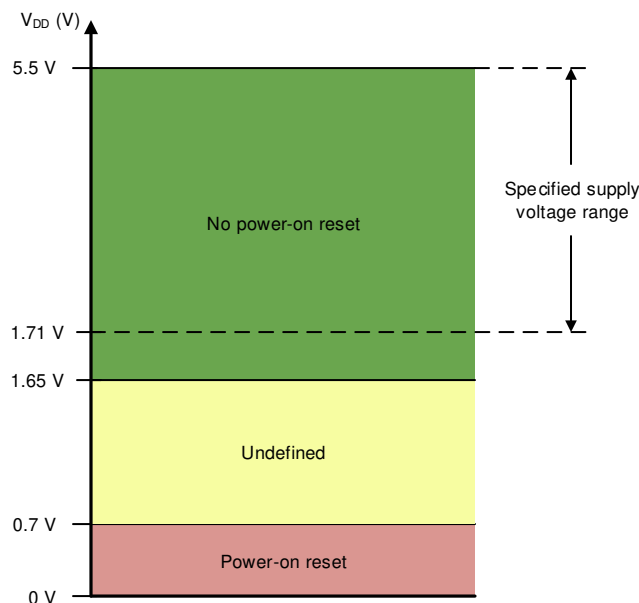


Figure 7-2. Threshold Levels for V_{DD} POR Circuit

7.3.5 External Reset

An external reset to the device can be triggered through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

7.3.6 Register-Map Lock

The AFE539F1-Q1 implements a register-map lock feature that prevents an accidental or unintended write to the registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I²C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

7.4 Device Functional Modes

7.4.1 Analog-to-Digital Converter (ADC) Mode

Channel 0 of the AFE539F1-Q1 acts as an ADC. The ADC is controlled by the state-machine in this device. The transfer function of the ADC is given in 式 1.

$$\text{ADC_DATA} = \left(\text{INTEGER} \right) \left(\frac{V_{\text{IN}}}{V_{\text{FS}}} \right) \times 2^N \quad (1)$$

where:

- ADC_DATA is the output of the ADC available to the state machine and is limited to (2^N-1) .
- V_{IN} is the input voltage at the AIN0 pin.
- V_{FS} is the full-scale input voltage, as provided in 表 7-1.
- N is the number of ADC bits = 10.
- INTEGER denotes integer division.

表 7-1. Full Scale Analog Input (V_{FS})

REFERENCE (VREF)	GAIN	V_{FS}
Power supply	1 ×	VDD / 3
External	1 ×	VREF / 3
Internal	1.5 ×	(VREF × GAIN) / 3
	2 ×	(VREF × GAIN) / 3
	3 ×	(VREF × GAIN) / 6
	4 ×	(VREF × GAIN) / 6

7.4.1.1 Voltage Reference Selection

图 7-3 shows the three possible voltage reference options with the AFE539F1-Q1: the power supply as reference, internal reference, or external reference (VREF/MODE pin). The REF-GAIN field in the REF-GAIN-CONFIG register selects the reference and the respective gain. The full scale ADC voltage changes based on the voltage reference selection.

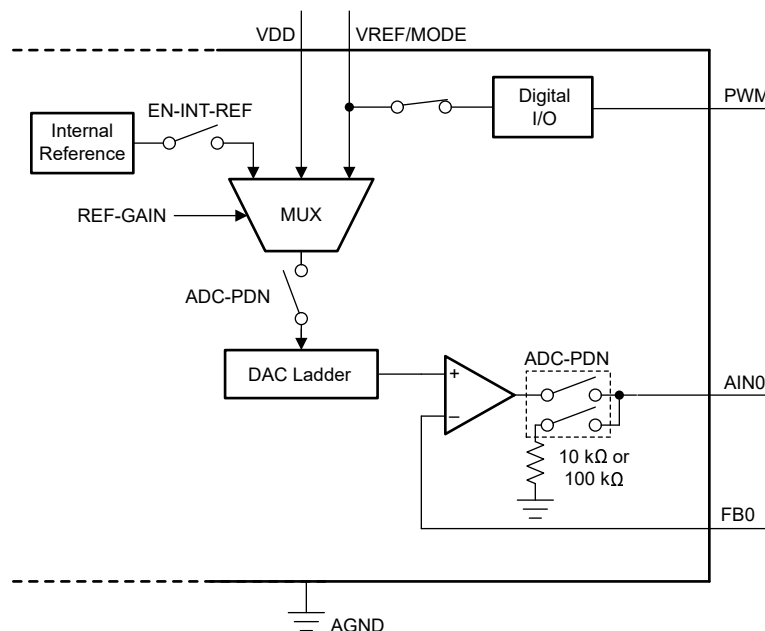


图 7-3. Voltage Reference Selection and Power-Down Logic

7.4.1.1.1 Power-Supply as Reference

By default, the AFE539F1-Q1 operates with the power-supply pin (VDD) as a reference. The gain at the output stage is always 1 ×.

7.4.1.1.2 Internal Reference

The AFE539F1-Q1 contains an internal reference. To enable the internal reference, write 1 to the EN-INT-REF bit in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the REF-GAIN field in the REF-GAIN-CONFIG register to select the internal reference and also to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the ADC full scale voltage (V_{FS}).

7.4.1.1.3 External Reference

The AFE539F1-Q1 provides an external reference input. Select the external reference option by configuring the REF-GAIN field in the REF-GAIN-CONFIG register appropriately. The external reference can be between 1.8 V and VDD.

注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

7.4.2 Pulse-Width Modulation (PWM) Mode

The AFE539F1-Q1 provides the 7-bit duty-cycle PWM output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable PWM functionality. [表 7-2](#) lists all the possible PWM frequency configurations using the PWM-FREQ bits in the PWM-FREQUENCY SRAM register.

表 7-2. PWM Frequency Configuration

SRAM REGISTER	PWM-FREQ BIT FIELD	PWM FREQUENCY (kHz)	DUTY CYCLE (%) FOR CODE 1	DUTY CYCLE (%) FOR CODE 126
PWM-FREQUENCY (0x23 [4:0])	0	Invalid	N/A	N/A
	1	48.828	4.88	95.12
	2	24.414	2.44	97.56
	3	16.276	1.63	98.37
	4	12.207	1.22	98.44
	5	8.138	0.81	98.44
	6	6.104	0.78	98.44
	7	3.052	0.78	98.44
	8	2.035	0.78	98.44
	9	1.526	0.78	98.44
	10	1.221	0.78	98.44
	11	1.017	0.78	98.44
	12	0.872	0.78	98.44
	13	0.763	0.78	98.44
	14	0.678	0.78	98.44
	15	0.610	0.78	98.44
	16	0.555	0.78	98.44
	17	0.509	0.78	98.44
	18	0.470	0.78	98.44
	19	0.436	0.78	98.44
	20	0.407	0.78	98.44
	21	0.381	0.78	98.44
	22	0.359	0.78	98.44
	23	0.339	0.78	98.44
	24	0.321	0.78	98.44
	25	0.305	0.78	98.44
	26	0.291	0.78	98.44
	27	0.277	0.78	98.44
	28	0.265	0.78	98.44
	29	0.254	0.78	98.44
	30	0.244	0.78	98.44
	31	0.218	0.78	98.44

The duty cycle of the PWM is proportional to the 7-bit code, 0d to 126d. As [表 7-3](#) shows, the code 127d corresponds to 100% duty cycle. The duty cycle 99.22% (127d/128d) is skipped to achieve 100% duty cycle using a 7-bit code. The PWM duty-cycle setting is done by the state machine and is not exposed to the user.

表 7-3. PWM Duty Cycle Setting

CODE	DUTY-CYCLE	DESCRIPTION
0	0%	Always 0
1	0.78%	Minimum linear duty cycle
x	(x/128)%	x is the code between 2d and 125d, both included
126	98.44%	Maximum linear duty cycle

表 7-3. PWM Duty Cycle Setting (continued)

CODE	DUTY-CYCLE	DESCRIPTION
127	100%	Always 1. The duty cycle 99.22% (127d/128d) is skipped.

7.4.3 Constant Power-Dissipation Control

The AFE539F1-Q1 can be used in applications where constant power dissipation is desired on a resistive load independently on applied voltage. Power dissipation in a fixed resistive load is inversely proportional to the resistance. When the voltage across the resistance varies, for example, in a discharging circuit, constant power can be achieved by modulating the effective resistance seen by the discharge circuit. [图 7-4](#) shows an example circuit to create a variable effective resistance from a fixed resistive load using a PWM signal. The effective resistance is the load resistance divided by the PWM duty cycle.

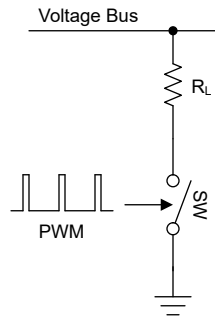


图 7-4. PWM-modulated Resistor

The AFE539F1-Q1 generates a PWM signal with a duty cycle dependent on the voltage applied to the ADC input. The AFE539F1-Q1 has a 10-bit ADC input with selectable reference voltage (V_{REF}). The AFE539F1-Q1 calculates the PWM duty cycle so that a constant dissipated power of the resistor is maintained.

The AFE539F1-Q1 runs a PWM duty cycle update loop that sets the duty cycle (D) according to [式 2](#).

$$D = \frac{K \times 2^{15}}{(\text{ADC_DATA})^2} = \frac{K \times (V_{FS})^2}{(V_{IN})^2 \times 2^5} \quad (2)$$

where:

- ADC_DATA is the decimal equivalent of the output from the ADC available to the state machine.
- V_{IN} is the ADC input voltage.
- V_{FS} is the full-scale ADC input voltage, as listed in [表 7-1](#).
- K is a user-configurable function-coefficient with a value of 16-bit integer (range: 1 to 65535) as programmed in the FUNCTION-COEFFICIENT register.

The duty cycle of the PWM output of the AFE539F1-Q1 has 7-bit resolution which means the minimum duty cycle as well as the step size is about 0.78%. The PWM can achieve 100% saturation, the lower and upper PWM value limit is user-configurable as well to accommodate specific application requirements. The constant power achieved with this pulse-width modulated resistor can be expressed accordingly as [式 3](#).

$$P_{\text{const}} = \frac{K_2 \times (V_{FS})^2}{R_L} \quad (3)$$

where:

- R_L is the load resistance.
- K_2 is a constant that is a function of the function-coefficient, K and the attenuation factor between the bus voltage and the full-scale ADC input.

[式 3](#) expresses that the theoretical constant power is independent on the input voltage. The power depends on the load resistance value and value of the constant, K_2 . However, the PWM is updated in discrete steps, the calculated constant power is in reality a power limit.

7.5 Programming

7.5.1 SPI Programming Mode

An SPI access cycle for AFE539F1-Q1 is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for AFE539F1-Q1 is 24 bits long. Therefore, the $\overline{\text{SYNC}}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{\text{SYNC}}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When $\overline{\text{SYNC}}$ is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

表 7-4 and 図 7-5 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

表 7-4. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Identifies the communication as a read or write command to the address register: R/W = 0 sets a write operation. R/W = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are <i>don't care</i> values.

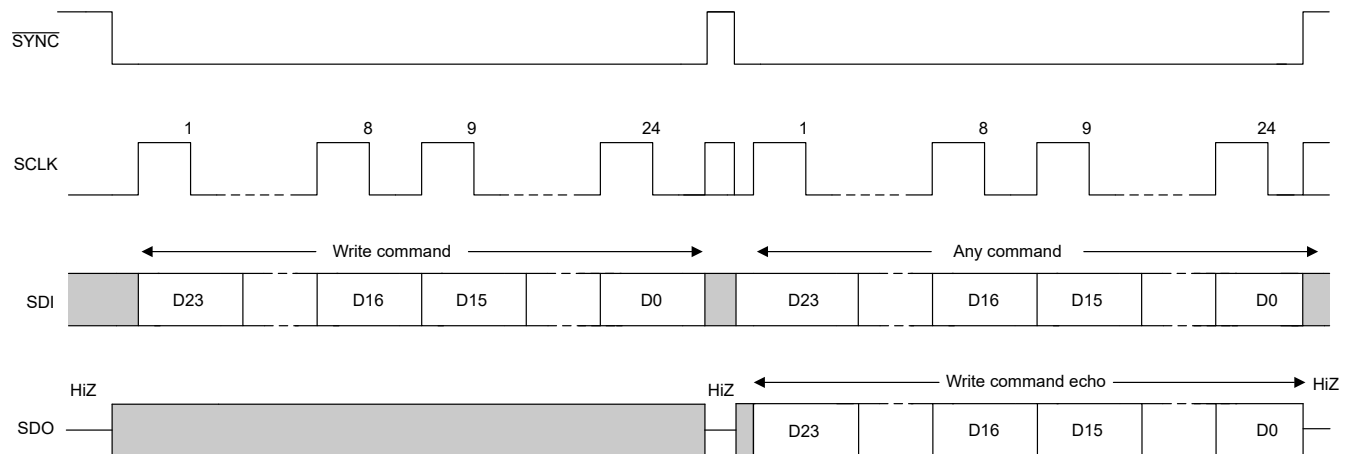
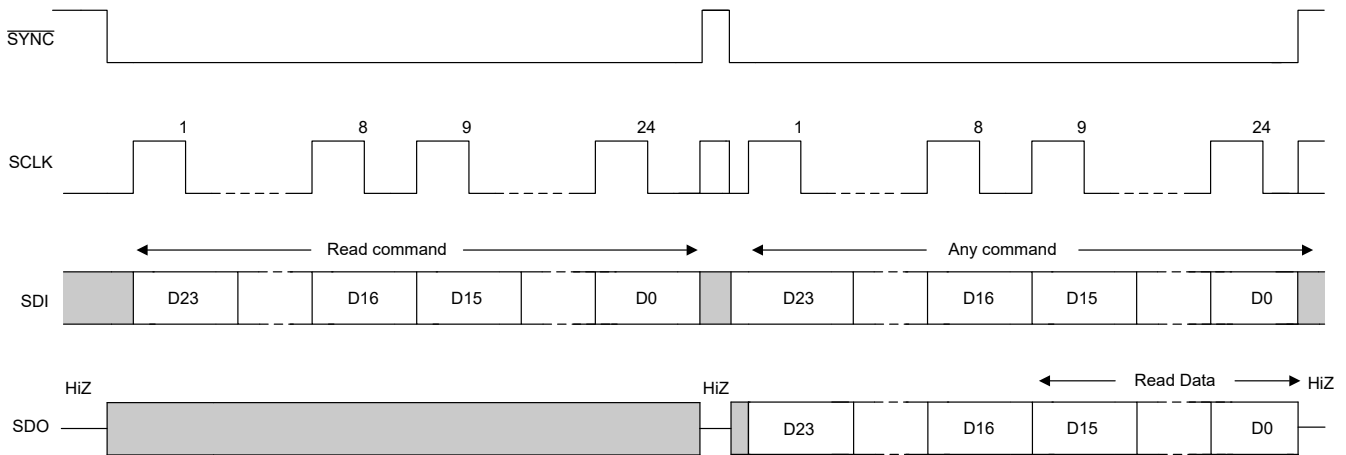


図 7-5. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in 表 7-5 and 図 7-6. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit, as shown in 図 6-3.

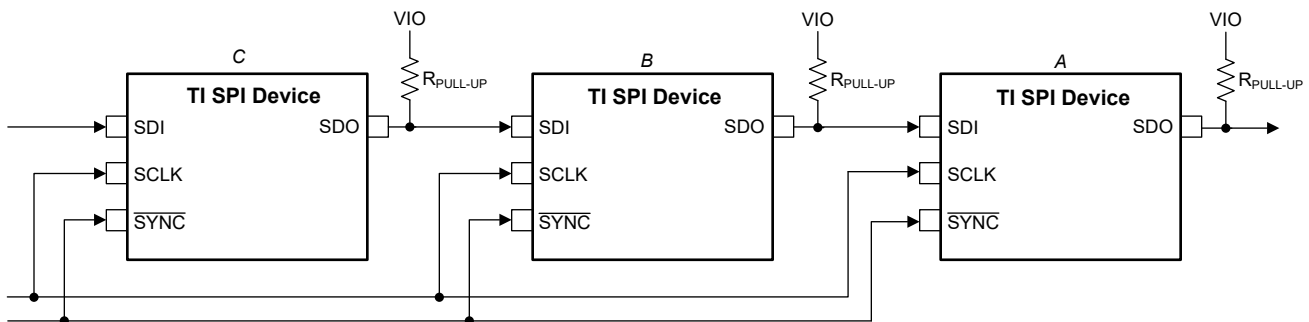
表 7-5. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/W	Echo R/W from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle

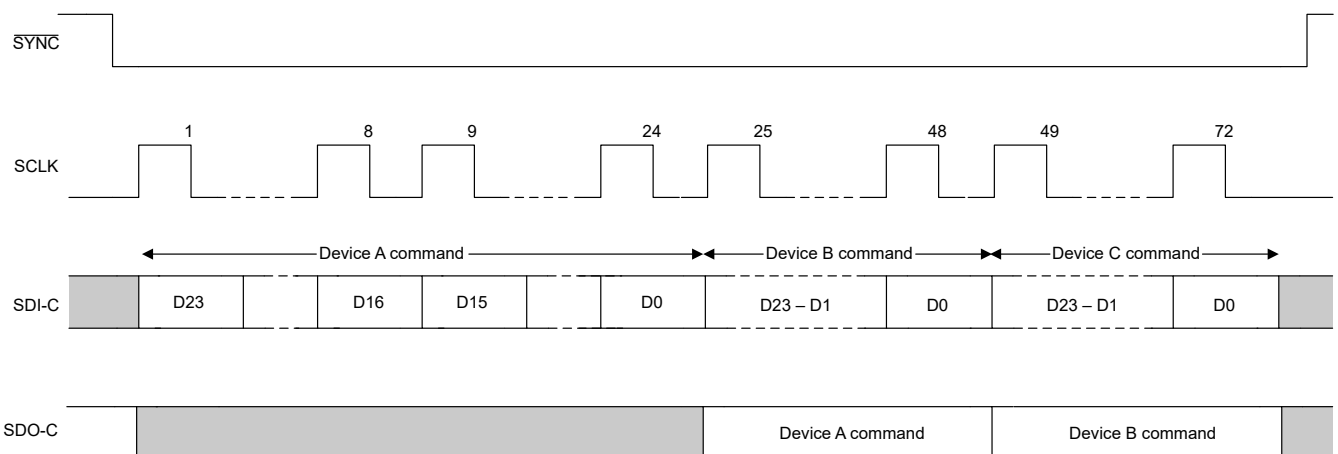


7-6. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. In daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device, as shown in [7-7](#). The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. [7-8](#) describes the packet format for the daisy-chain write cycle.



7-7. SPI Daisy-Chain Connection



7-8. SPI Daisy-Chain Write Cycle

7.5.2 I²C Programming Mode

The AFE539F1-Q1 has a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I²C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through the open drain I/O pins, SDA and SCL.

The I²C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I²C bus is typically a microcontroller or digital signal processor (DSP). The AFE539F1-Q1 operates as a target on the I²C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

Typically, the AFE539F1-Q1 operates as a target receiver. A controller writes to the AFE539F1-Q1, a target receiver. However, if a controller requires the AFE539F1-Q1 internal register data, the AFE539F1-Q1 operates as a target transmitter. In this case, the controller reads from the AFE539F1-Q1. According to I²C terminology, read and write refer to the controller.

The AFE539F1-Q1 supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The AFE539F1-Q1 supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in [Figure 7-9](#).

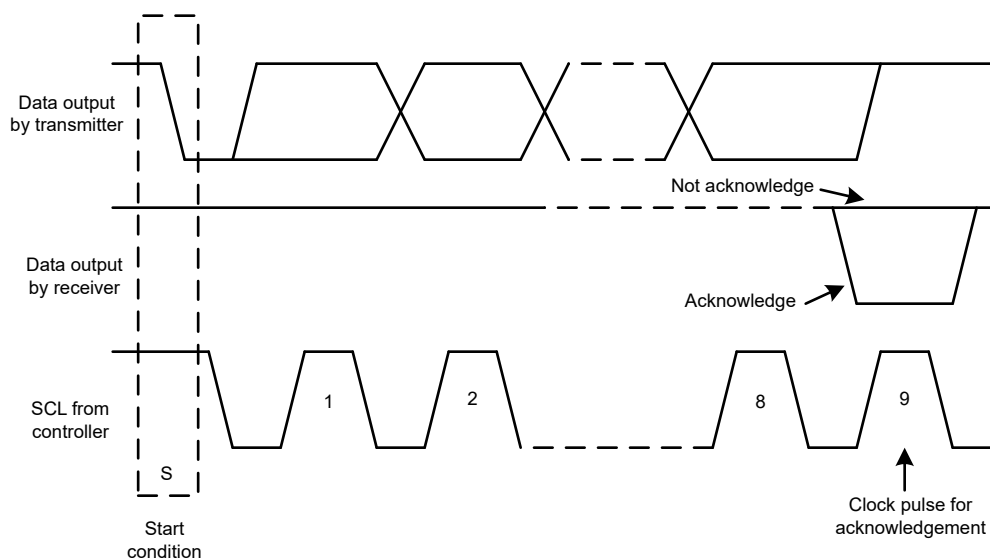


Figure 7-9. Acknowledge and Not Acknowledge on the I²C Bus

7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in [Figure 7-10](#). All I²C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/\bar{W}) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in [Figure 7-11](#). All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in [Figure 7-9](#). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit (R/\bar{W} bit 0) or receive (R/\bar{W} bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in [Figure 7-10](#). This action releases the bus and stops the communication link with the addressed target. All I²C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.

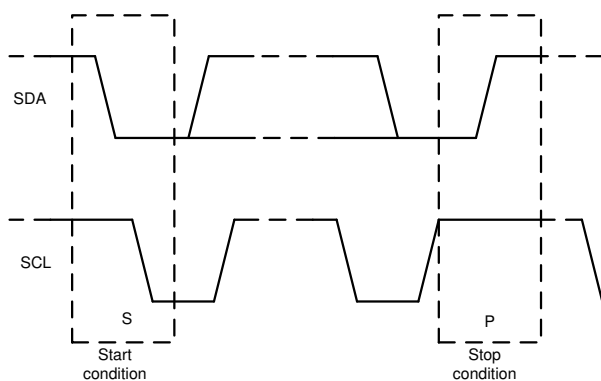


Figure 7-10. Start and Stop Conditions

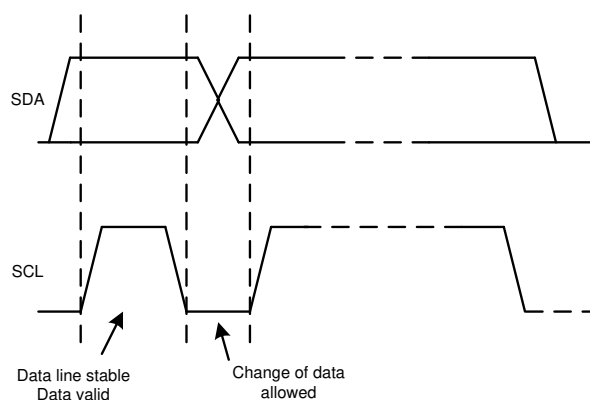


Figure 7-11. Bit Transfer on the I²C Bus

7.5.2.2 I²C Update Sequence

For a single update, the AFE539F1-Q1 requires a start condition, a valid I²C address byte, a command byte, and two data bytes, as listed in 表 7-6.

表 7-6. Update Sequence

MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the AFE539F1-Q1 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in 図 7-12. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C address byte selects the AFE539F1-Q1.

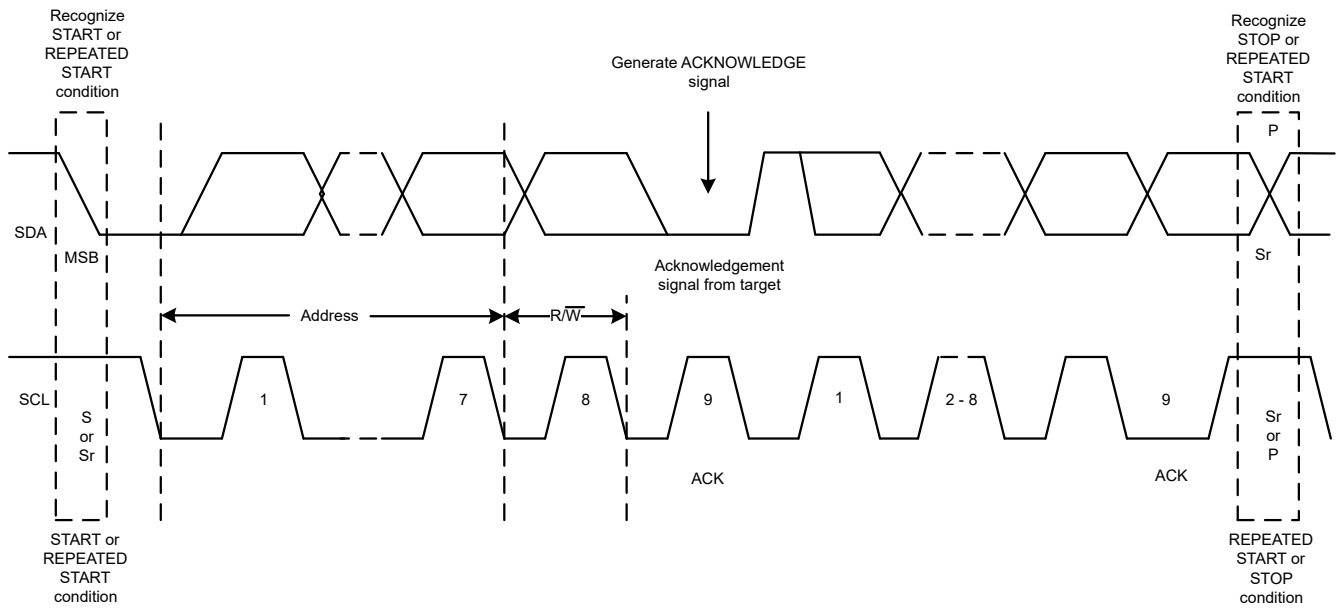


図 7-12. I²C Bus Protocol

The command byte sets the operating mode of the selected AFE539F1-Q1 device. For a data update to occur when the operating mode is selected by this byte, the AFE539F1-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The AFE539F1-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum update rate is limited to 10Ksps. Using fast mode plus (clock = 1 MHz), the maximum update rate is limited to 25Ksps. When a stop condition is received, the AFE539F1-Q1 device releases the I²C bus and awaits a new start condition.

7.5.2.2.1 Address Byte

The address byte, as shown in 表 7-7, is the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to 表 7-8.

表 7-7. Address Byte

COMMENT	MSB							LSB
	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
—								R/W
General address	1	0	0	1	See 表 7-8 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

表 7-8. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The AFE539F1-Q1 supports broadcast addressing, which is used for synchronously updating or powering down multiple AFE539F1-Q1 devices. When the broadcast address is used, the AFE539F1-Q1 responds regardless of the address pin state. Broadcast is supported only in write mode.

7.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

7.5.2.3 I²C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/\overline{W} bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/\overline{W} bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

表 7-9. Read Sequence

S	MSB	...	R/W (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/W (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	ADDRESS BYTE セクション 7.5.2.2.1				COMMAND BYTE セクション 7.5.2.2.2				Sr	ADDRESS BYTE セクション 7.5.2.2.1				MSDB				LSDB			
	From Controller			Target	From Controller			Target		From Controller			Target	From Target			Controller	From Target			Controller

7.6 Register Maps

表 7-10. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
REF-GAIN-CONFIG	X		REF-GAIN				RESERVED									
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	ADC-PDN		RESERVED									
COMMON-TRIGGER	DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
COMMON-PWM-TRIG	RESERVED															START-FUNCTION
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	RESERVED				NVM-BUSY	DEVICE-ID						VERSION-ID		
INTERFACE-CONFIG	X			TIMEOUT-EN	X								FSDO-EN	X	SDO-EN	
STATE-MACHINE-CONFIG0	RESERVED											SM-ABORT	SM-START	SM-EN		
SRAM-CONFIG	X							SRAM-ADDR								
SRAM-DATA	SRAM-DATA															
MAX-OUTPUT	RESERVED								MAX-OUTPUT							
MIN-OUTPUT	RESERVED								MIN-OUTPUT							
FUNCTION-COEFFICIENT	FUNCTION-COEFFICIENT															
PWM-FREQUENCY	RESERVED										PWM-FREQ					

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

表 7-11. Register Names

I ² C/SPI ADDRESS (COMMAND BYTE)	SRAM ADDRESS	REGISTER NAME	SECTION
00h	—	NOP	セクション 7.6.1
15h	—	REF-GAIN-CONFIG	セクション 7.6.2
1Fh	—	COMMON-CONFIG	セクション 7.6.3
20h	—	COMMON-TRIGGER	セクション 7.6.4
21h	—	COMMON-PWM-TRIG	セクション 7.6.5
22h	—	GENERAL-STATUS	セクション 7.6.6
26h	—	INTERFACE-CONFIG	セクション 7.6.7
27h	—	STATE-MACHINE-CONFIG0	セクション 7.6.8
2Bh	—	SRAM-CONFIG	セクション 7.6.9
2Ch	—	SRAM-DATA	セクション 7.6.10
—	20h	MAX-OUTPUT	セクション 7.6.11
—	21h	MIN-OUTPUT	セクション 7.6.12
—	22h	FUNCTION-COEFFICIENT	セクション 7.6.13
—	23h	PWM-FREQUENCY	セクション 7.6.14

7.6.1 NOP Register (address = 00h) [reset = 0000h]

☒ 7-13. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0h															

表 7-12. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

7.6.2 REF-GAIN-CONFIG Register (address = 15h) [reset = 0401h]

☒ 7-14. REF-GAIN-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		REF-GAIN				RESERVED									
X-0h		R/W-001				R/W-001h									

表 7-13. REF-GAIN-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care.
12-10	REF-GAIN	R/W	001	000: Gain = 1 ×, external reference on VREF/MODE pin. 001: Gain = 1 ×, VDD as reference (default). 010: Gain = 1.5 ×, internal reference. 011: Gain = 2 ×, internal reference. 100: Gain = 3 ×, internal reference. 101: Gain = 4 ×, internal reference. Others: NA.
9-0	RESERVED	R/W	001h	Always write 001h.

7.6.3 COMMON-CONFIG Register (address = 1Fh) [reset = 13FFh]

☒ 7-15. COMMON-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	ADC-PDN		RESERVED									
R/W-0h	R/W-0h	R/W-0h	R/W-1	R/W-0h		R/W-3FFh									

表 7-14. COMMON-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	1	0: Disable internal reference 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11	ADC-PDN	R/W	0	00: Power-up ADC. 01: Power-down ADC with 10 KΩ to AGND. 10: Power-down ADC with 100 KΩ to AGND. 11: Power-down ADC with Hi-Z to AGND.
10-0	RESERVED	R/W	3FFh	Always write 3FFh.

7.6.4 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

☒ 7-16. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED				NVM-PROG	NVM-RELOAD		
R/W-0h				R/W-0h				R/W-00h				R/W-0h	R/W-0h		

表 7-15. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0h	0101: Device unlocking password. Others: Don't care.
11-8	RESET	W	0h	1010: POR reset triggered. This field is self-resetting. Others: Don't care.
7-2	RESERVED	R/W	00h	Always write 0.
1	NVM-PROG	R/W	0	0: NVM write not triggered. 1: NVM write triggered. This bit is self-resetting.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered. 1: Reload data from NVM to register map. This bit is self-resetting.

7.6.5 COMMON-PWM-TRIG Register (address = 21h) [reset = 0001h]

☒ 7-17. COMMON-PWM-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														START-FUNCTION	
R/W-0000h														R/W-0h	

表 7-16. COMMON-PWM-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0000h	Always write 0000h.
0	START-FUNCTION	R/W	0	0: Stop PWM generation. 1: Invalid. This bit is automatically set by the state machine.

7.6.6 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

☒ 7-18. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	X				NVM-BUSY	DEVICE-ID					VERSION-ID			
R-0h	R-0h	X-00h				R-0h	R-0h					R-0h			

表 7-17. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading. 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this error condition.
13	X	X	00h	Don't care.
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	19h	Device identifier.
1-0	VERSION-ID	R	0	Version identifier.

7.6.7 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

☒ 7-19. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		TIMEOUT-EN	X					FSDO-EN	X	SDO-EN					
X-0h		R/W-0h	X-0h					R/W-0h	X-0h	R/W-0h					

表 7-18. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	X	X	0h	Don't care.
12	TIMEOUT-EN	R/W	0	0: I ² C timeout disabled. 1: I ² C timeout enabled.
11 - 3	X	X	0h	Don't care.
2	FSDO-EN	R/W	0	0: Fast SDO disabled. 1: Fast SDO enabled.
1	X	X	0	Don't care.
0	SDO-EN	R/W	0	0: SDO disabled. 1: SDO enabled.

7.6.8 STATE-MACHINE-CONFIG0 Register (address = 27h) [reset = 0003h]

☒ 7-20. STATE-MACHINE-CONFIG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												SM-ABORT	SM-START	SM-EN	
R/W-0h												R/W-0h	R/W-0h	R/W-0h	

表 7-19. STATE-MACHINE-CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R/W	0000h	Always write 0.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	0	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	0	0: State machine disabled. 1: State machine enabled.

7.6.9 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

☒ 7-21. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

表 7-20. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

7.6.10 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

☒ 7-22. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

表 7-21. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. Data are written to or read from the address configured in the SRAM-CONFIG register.

7.6.11 MAX-OUTPUT Register (SRAM address = 20h) [reset = 007Fh]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-23. MAX-OUTPUT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAX-OUTPUT							
R/W-0000h								R/W-7Fh							

表 7-22. MAX-OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0000h	Always write 0000h.
6-0	MAX-OUTPUT	R/W	7Fh	7-bit maximum limit for PWM output.

7.6.12 MIN-OUTPUT Register (SRAM address = 21h) [reset = 0000h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-24. MIN-OUTPUT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIN-OUTPUT							
R/W-0000h								R/W-00h							

表 7-23. MIN-OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0000h	Always write 0000h.
6-0	MIN-OUTPUT	R/W	00h	7-bit minimum limit for PWM output.

7.6.13 FUNCTION-COEFFICIENT Register (SRAM address = 22h) [reset = 01F4h]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-25. FUNCTION-COEFFICIENT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNCTION-COEFFICIENT															
R/W-01F4h															

表 7-24. FUNCTION-COEFFICIENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FUNCTION-COEFFICIENT	R/W	01F4h	16-bit function coefficient (K) as specified in 式 2 and 式 3.

7.6.14 PWM-FREQUENCY Register (SRAM address = 23h) [reset = 000Bh]

注

This register address is mapped to SRAM. Use the SRAM-CONFIG and SRAM-DATA registers to read and write.

図 7-26. PWM-FREQUENCY Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PWM-FREQ				
R/W-000h											R/W-0Bh				

表 7-25. PWM-FREQUENCY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	000h	Always write 000h.
15-0	SRAM-DATA	R/W	0Bh	5-bit PWM frequency setting as specified in 表 7-2 .

8 Application and Implementation

注

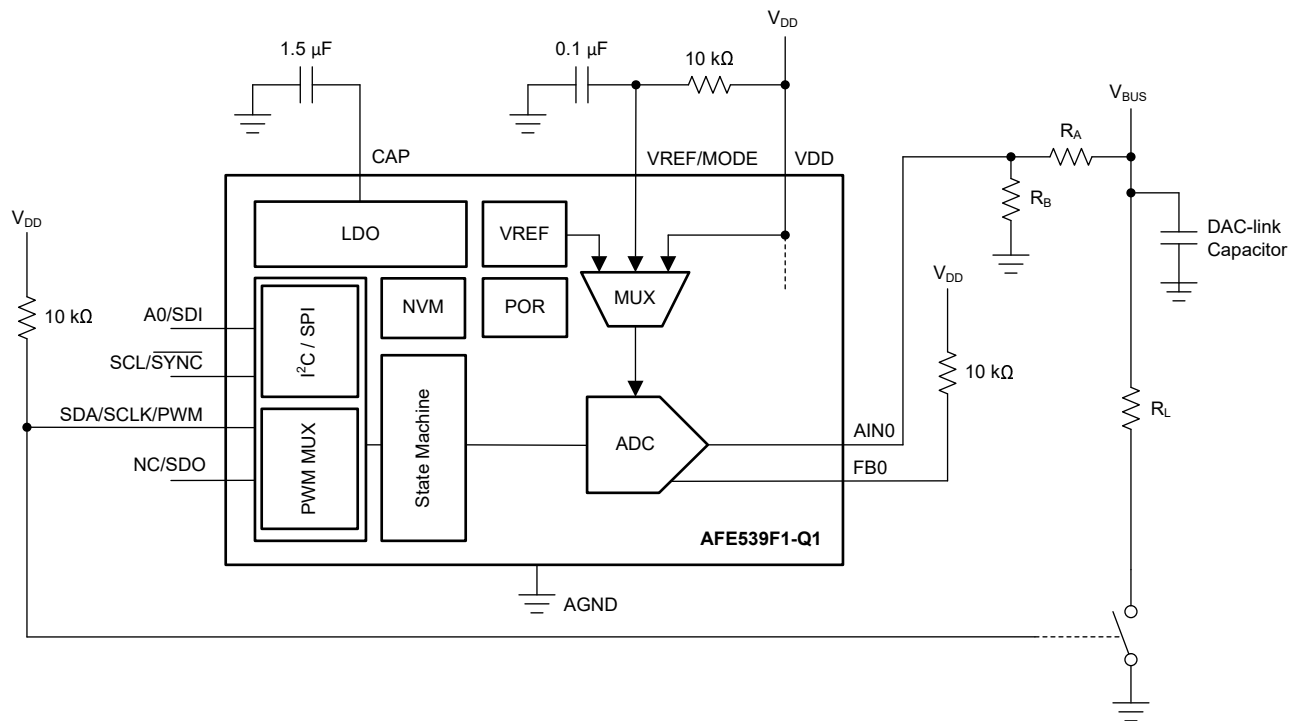
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AFE539F1-Q1 is a smart analog front end (AFE) that includes an ADC channel, PWM output, NVM, internal reference, and are available in a tiny 3-mm × 3-mm package. The AFE539F1-Q1 have an integrated state machine that is pre-programmed as a constant power output controller. The ADC has a full-scale of $V_{DD}/3$. Use an external attenuator when the input exceeds this range. The PWM provides a 7-bit duty-cycle output on the SDA/SCLK/PWM pin. Pull the VREF/MODE pin high to enable the PWM output. Pulling the VREF/MODE pin low enables the I²C or SPI programming mode. The application parameters are programmed in the device using I²C or SPI and stored in the NVM.

8.2 Typical Application

This design uses the AFE539F1-Q1 to maintain constant power dissipation on a restive load, independent of the applied voltage. Modulating the power resistor via a switch can change the effective resistance and maintain constant power as the supply voltage (V_{BUS}) changes. The AFE539F1-Q1 has an integrated state machine that converts the ADC input to a PWM output based on the transfer function in 式 2. Parameters such as the PWM frequency, maximum and minimum duty cycle outputs, and the K term in 式 2 are user programmable and can be saved in the NVM. The control loop runs standalone without the need for a processor after initial programming. Use this circuit in constant power heating, or automotive DC-link capacitor discharge applications. [图 8-1](#) shows an example schematic for this application.



Constant Power Discharge Circuit

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
PWM Frequency	3.052 kHz
Bus voltage (V _{BUS})	48 V
Load resistance (R _L)	5 Ω
Power dissipation limit	50 W
Maximum duty cycle	100%
Minimum duty cycle	0%

8.2.2 Detailed Design Procedure

Use VDD (5 V) as reference with gain 1 × to achieve an input range of (VDD/3) = 1.67 V, using 表 7-1. With a bus voltage of 48 V and ADC input range of 1.67 V, the external attenuation required is 28.74. Therefore, the attenuation resistors can be chosen as R_A = 100 kΩ and R_B = 3.6 kΩ. To limit the power dissipation to 50 W, the effective load resistance (R_{L-eff}) is calculated as (V_{BUS}²/P) = 46.08 Ω. That means a minimum duty-cycle of (R_L/R_{L-eff}) = 10.85% is required. In a 7-bit scale, 10.85% corresponds to 13.89d. The required function coefficient, K can be calculated using 式 4 to be 443.6d (0x01BC).

$$K = \frac{D_{\text{MIN}} \times (\text{ADC} - \text{DATA}_{\text{MAX}})^2}{2^{15}} \quad (4)$$

The PWM output pin is an open drain output. The PWM output pin must be pulled up to the desired IO voltage using an external resistor. The PWM frequency is set in the PWM-FREQUENCY SRAM location (SRAM: 0x23). 表 7-2 defines the codes for each available frequency. This example uses a PWM frequency of 3.052 kHz. Set the maximum and minimum PWM duty cycles limits in the MAX-OUTPUT and MIN-OUTPUT SRAM locations. The PWM duty cycle output is configured by a 7-bit code. The maximum code is 127d. 127d sets the PWM duty cycle to 100%. 表 7-3 provides more details about PWM duty cycle computation in AFE539F1-Q1.

Follow these guidelines to setup the registers on AFE539F1-Q1:

- Set the VREF/MODE pin low to enable the digital pins for programming mode.
- Stop the state machine before updating the application parameters by writing 0 to the STATE-MACHINE-CONFIG0 register.
- If the PWM generator is already running, stop the PWM generator before any changes to the PWM frequency take effect. Write a 0 to the START-FUNCTION field in the COMMON-PWM-TRIG register (0x21) to stop the PWM generator. The PWM generator automatically starts when the state machine is enabled.
- Set all of the application parameters shown in 表 8-2. Use these locations to save the settings in NVM.
- Configure the reference for the ADC in the REF-GAIN-CONFIG register.
- Power on the ADC channel using the COMMON-CONFIG register.
- Start the state machine by writing 0x3 to the STATE-MACHINE-CONFIG0.
- Trigger an NVM write by setting the NVM-PROG bit in the COMMON-TRIGGER register (0x20) to 1.
- Set the VREF/MODE pin high to enable the digital pins for standalone mode. This is required to see the PWM output on the digital pin.

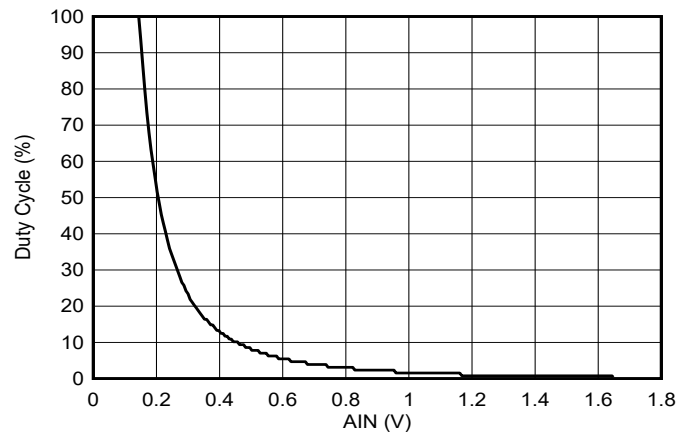
表 8-2. Application Parameters

REGISTER FIELD NAME	ADDRESS[FIELD]	ADDRESS LOCATION
MAX-OUTPUT	0x20[6:0]	SRAM
MIN-OUTPUT	0x21[6:0]	SRAM
FUNCTION-COEFFICIENT	0x22[15:0]	SRAM
PWM-FREQUENCY	0x23[4:0]	SRAM
REF-GAIN-CONFIG	0x15[12:10][4:0]	Register
COMMON-CONFIG	0x1F[15:0]	Register
STATE-MACHINE-CONFIG0	0x27[2:0]	Register

The pseudocode for this application example is as follows:

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <MSB DATA>, <LSB DATA>
//Stop the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x01
//Stop the PWM generator
WRITE COMMON-PWM-TRIG(0x21), 0x00, 0x00
//Set the PWM frequency to 3.052 kHz
WRITE PWM-FREQUENCY(SRAM 0x23), 0x00, 0x07
//Set the maximum and minimum PWM duty cycles
WRITE MAX-OUTPUT(SRAM 0x20), 0x00, 0x7F
WRITE MIN-OUTPUT(SRAM 0x21), 0x00, 0x00
//Set the function coefficient (K)
WRITE FUNCTION-COEFFICIENT(SRAM 0x22), 0x01, 0xBC
//Set the ADC reference to VDD (this is the device default)
WRITE REF-GAIN-CONFIG(0x15), 0x04, 0x01
//Power on ADC
WRITE COMMON-CONFIG(0x1F), 0x03, 0xFF
//Start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
//Pull the VREF/MODE pin high to enter standalone mode
```

8.2.3 Application Curve



8-1. PWM Duty Cycle vs Input Voltage

8.3 Power Supply Recommendations

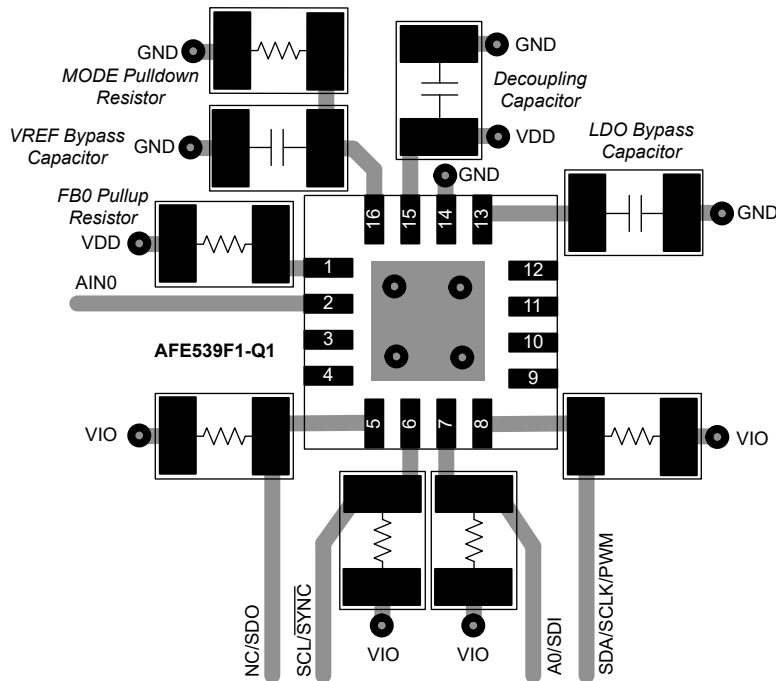
The AFE539F1-Q1 do not require specific power-supply sequencing. These devices require a single power supply, V_{DD} . However, make sure the external voltage reference is applied after V_{DD} powers on. Use a 0.1- μF decoupling capacitor for the V_{DD} pin. Use a bypass capacitor with a value approximately 1.5 μF for the CAP pin.

8.4 Layout

8.4.1 Layout Guidelines

The AFE539F1-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

8.4.2 Layout Example



8-2. Layout Example

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

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9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE539F1RTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A59F1Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

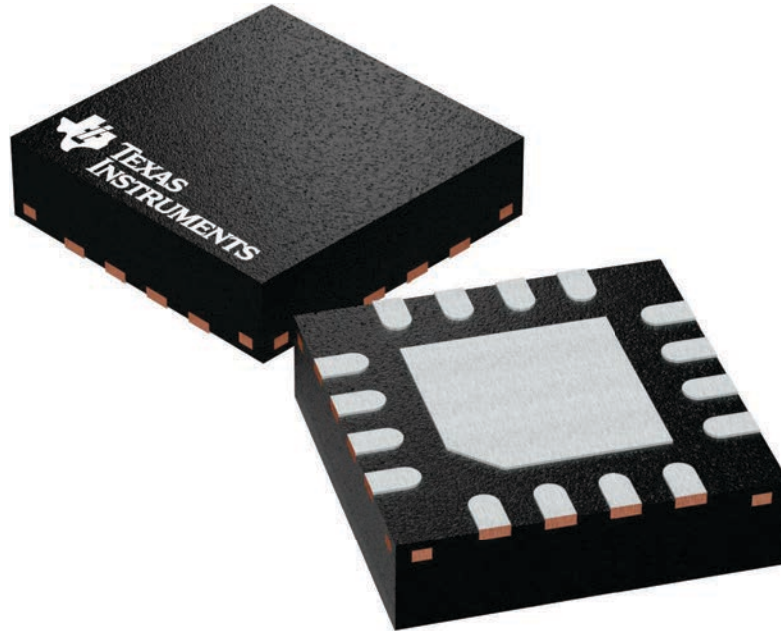
RTE 16

WQFN - 0.8 mm max height

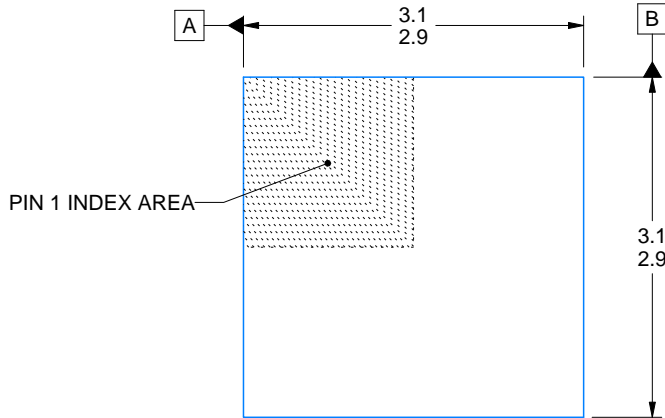
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

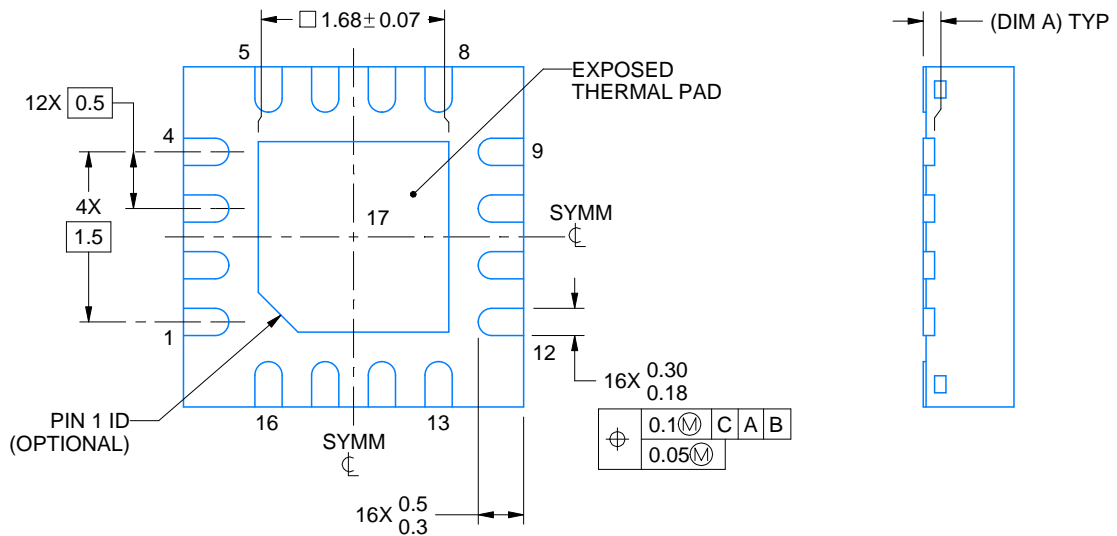
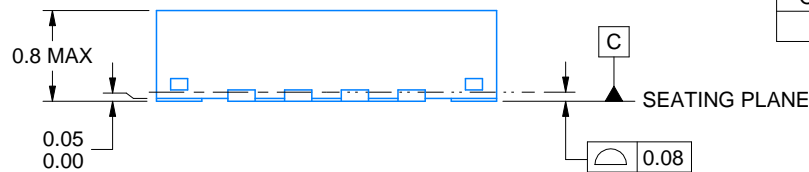
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

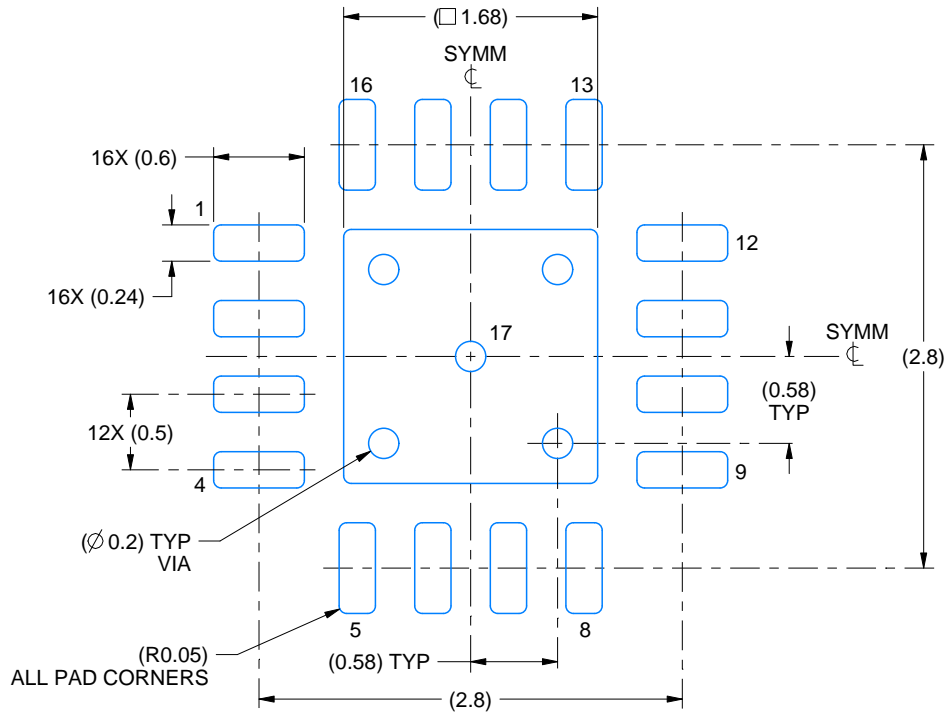
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

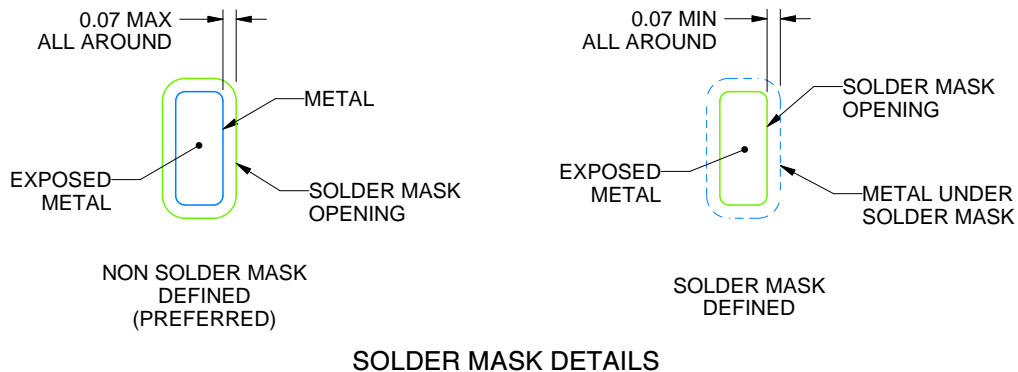
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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