AM26LV31 低電圧、高速のクワッド差動ライン ドライバ

1 特長

- 最高 32MHz のスイッチング速度
- 3.3V 単一電源で動作
- 伝搬遅延時間:8ns (標準値)
- パルス スキュー時間:500ps (標準値)
- 大出力電流:±30 mA
- 制御された立ち上がりおよび立ち下がり時間:3ns (標準値)
- 100Ω 負荷での
  差動出力電圧:1.5V (標準値)
- 非常に低い消費電力:
  - DC:0.3mW (最大値)
  - 全チャネル 32MHz (無負荷):385mW (標準値)
- 3.3V 電源で 5V ロジック入力を許容
- AM26C31、AM26LS31、MB571 の、低電圧でピン互換の代替品
- 電源オフ状況での高い出力インピーダンス
- ドライバ出力の短絡保護回路
- プラスチックのスモール アウトライン (D、NS) パッケージ オプションを選択可能

2 アプリケーション

- モータ制御:ブラシレス DC およびブラシ付き DC
- フィールド トランスミッタ:温度センサおよび圧力センサ
- Modbus 使用の温度センサまたはコントローラ

3 概要

AM26LV31C および AM26LV31I は、BiCMOS のクワッド差動、3-state 出力のライン ドライバです。TIA/EIA-422-B および ITU 勧告 V.11 ドライバと同様な設計で、電源電圧範囲が低くなっています。

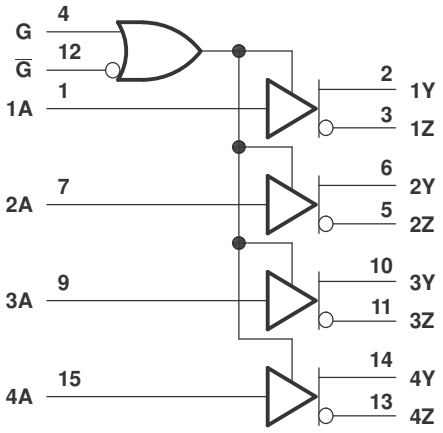
これらのデバイスは、最高 32MHz のスイッチング速度で、平衡化されたバス転送を行うよう最適化されています。出力には、ツイストペア伝送ラインなど平衡化されたラインを駆動するための、非常に大きな電流能力があり、電源オフ状況では高インピーダンスになります。イネーブル機能は 4 つのドライバすべてに共通で、アクティブ HIGH またはアクティブ LOW のイネーブル入力を選択できます。AM26LV31C と AM26LV31I は、テキサス・インスツルメンツ独自の LinIMPACT-C60™ テクノロジーを使用して設計されて おり、速度を犠牲にすることなく超低消費電力を実現しています。これらのデバイスは、AM26LV32 クワッド ライン レシーバとともに使用したとき、最高のパフォーマンスを発揮します。

AM26LV31C は 0℃～70℃での動作が規定されています。AM26LV31I は -45℃～85℃での動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AM26LV31C	SOIC (D) 16	9.9mm × 6mm
AM26LV31I	SOIC (D) 16	9.9mm × 6mm
	SO (NS) 16	10.2mm × 7.8mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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4 Pin Configuration and Functions

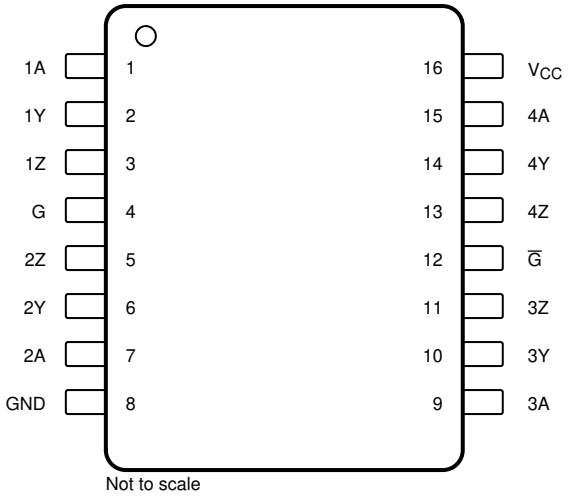


図 4-1. D or NS Package, SOIC 16 Pins (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Driver 1 input
2	1Y	O	Driver 1 output
3	1Z	O	Driver 1 inverted output
4	G	I	Active high enable
5	2Z	O	Driver 2 inverted output
6	2Y	O	Driver 2 output
7	2A	I	Driver 2 input
8	GND	—	Ground pin
9	3A	I	Driver 3 input
10	3Y	O	Driver 3 output
11	3Z	O	Driver 3 inverted output
12	$\overline{G}$	I	Active low enable
13	4Z	O	Driver 4 inverted output
14	4Y	O	Driver 4 output
15	4A	I	Driver 4 input
16	V_{CC}	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage range, V_{CC} (2)	–0.3	6	V
Input voltage range, V_I	–0.3	6	V
Output voltage range, V_O	–0.3	6	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–30	mA
I_{OL}	Low-level output current				30	mA
T_A	Operating free-air temperature	AM26LV31C	0		70	°C
		AM26LV31I	–45		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	NS (SO) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = 18mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	I_{OH} = –12mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8V,	I_{OH} = 12mA		0.8	1.05	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 100Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage			1.3	1.55	1.9	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.2	V
I_O	Output current with power off	V_O = –0.25V or 6V,	V_{CC} = 0			±100	µA
I_{OZ}	Off-state (high-impedance state) output current	V_O = –0.25V or 6V,	G = 0.8V or $\overline{G}$ = 2V			±100	µA
I_H	High-level input current	V_{CC} = 0 or 3V,	V_I = 5.5V			10	µA
I_L	Low-level input current	V_{CC} = 3.6V,	V_I = 0			–10	µA
I_{OS}	Short-circuit output current	V_{CC} = 3.6V,	V_O = 0			–200	mA
I_{CC}	Supply current (all drivers)	V_I = V_{CC} or GND,	No load			100	µA
C_{pd}	Power-dissipation capacitance (all drivers)(3)	No load			160		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 図 6-2		4	8	20	ns
t_{PHL}	Propagation delay time, high- to low-level output			4	8	20	ns
t_t	Transition time (t_r or t_f)				3		ns
SR	Slew rate, single-ended output voltage	See Note (2) and 図 6-2			0.3	1	V/ns
t_{PZH}	Output-enable time to high level	See 図 6-3			10	20	ns
t_{PZL}	Output-enable time to low level	See 図 6-4			10	20	ns
t_{PHZ}	Output-disable time from high level	See 図 6-3			10	20	ns
t_{PLZ}	Output-disable time from low level	See 図 6-4			10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32MHz,	See Note (3)		0.5	3	ns
$t_{sk(o)}$	Skew limit	f = 32MHz				3	ns
$t_{sk(lim)}$	Skew limit (device to device)	f = 32 MHz,	See Note (4)			3	ns

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C
(2) Slew rate is defined by 式 1
(3) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(4) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

$$SR = \frac{90\%\,(V_{OH} - V_{OL}) - 10\%\,(V_{OH} - V_{OL})}{t_f}$$, the differential slew rate of V_{CC} is 2 x SR. (1)

5.7 Typical Characteristics

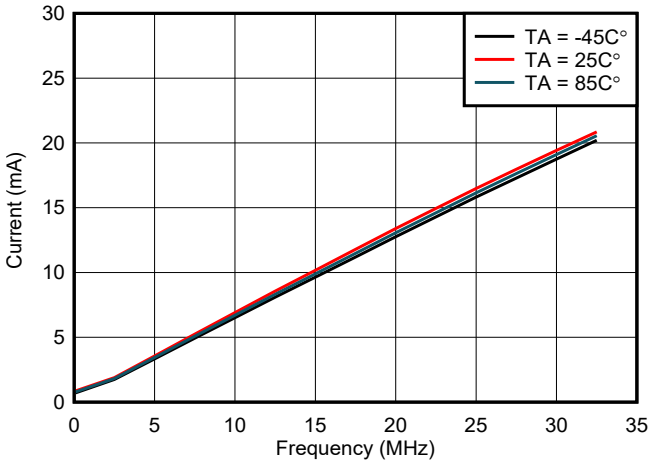


図 5-1. Current vs Frequency

6 Parameter Measurement Information

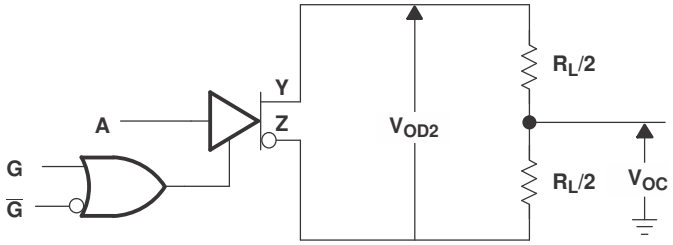
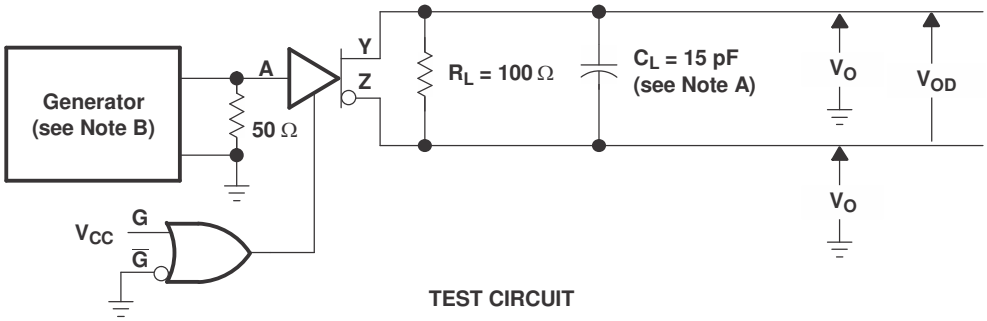
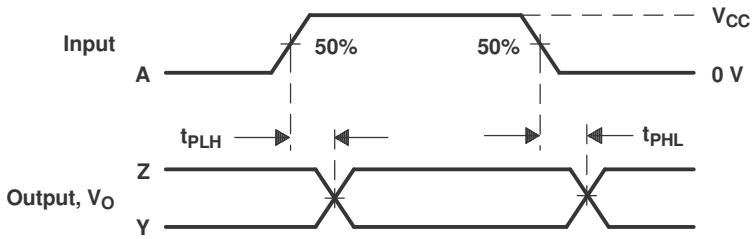


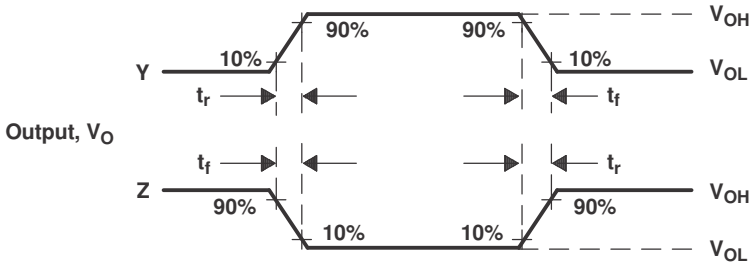
図 6-1. Differential and Common-Mode Output Voltages



TEST CIRCUIT



PROPAGATION DELAY TIMES

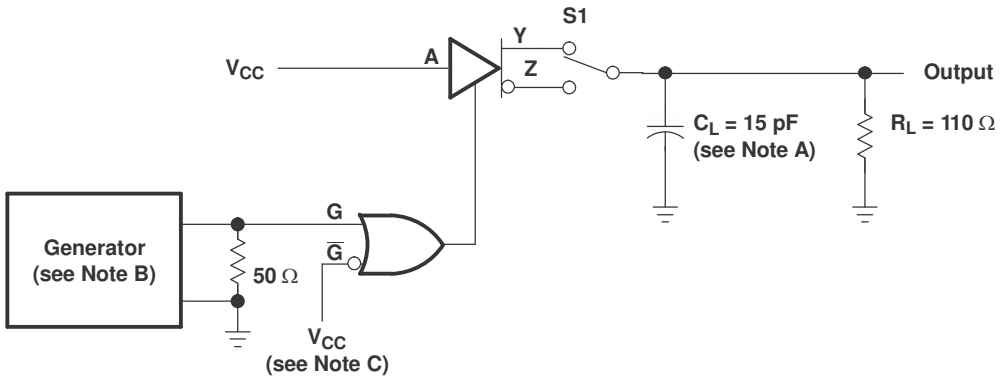


RISE AND FALL TIMES

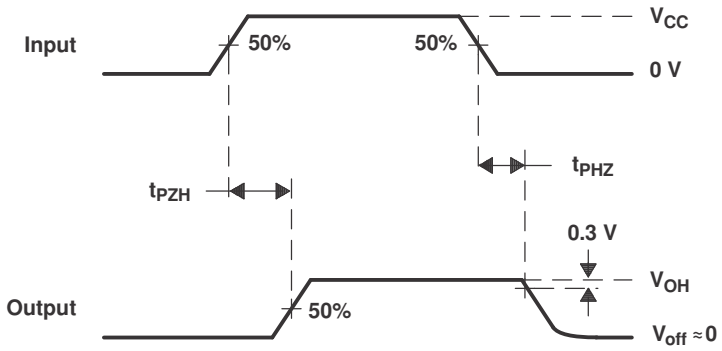
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 10MHz, Z_O = 50Ω, 50%v duty cycle, t_r and t_f ≤ 10ns.

図 6-2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}



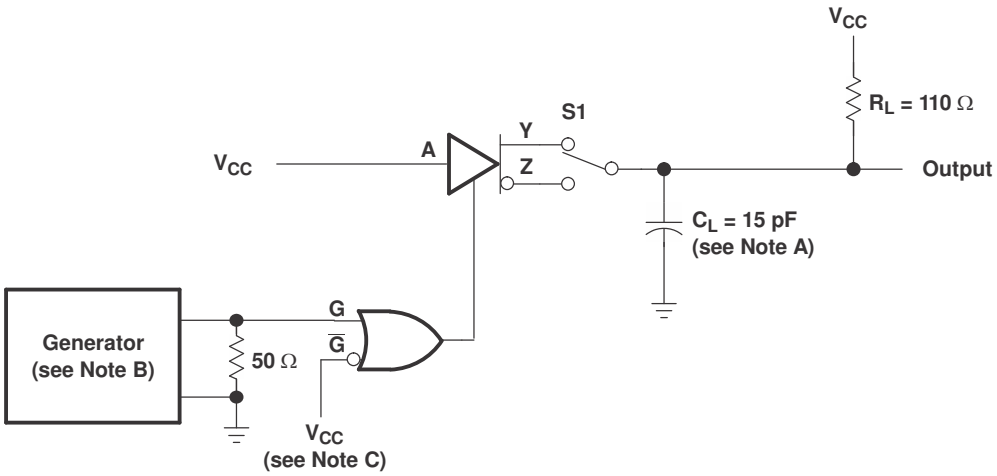
TEST CIRCUIT



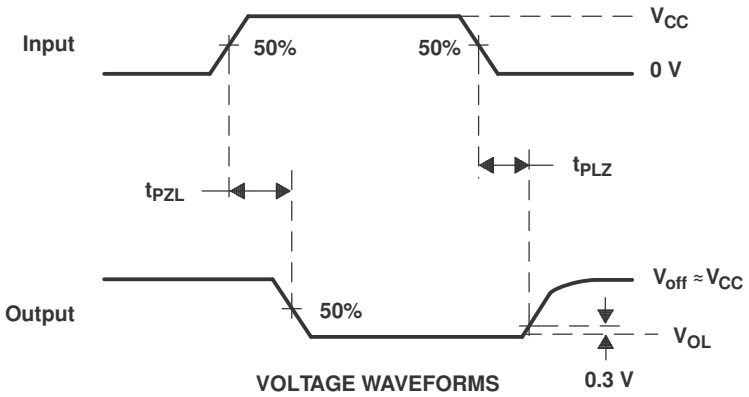
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

図 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, 50%v duty cycle, t_r and t_f (10% to 90%) ≤ 2ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

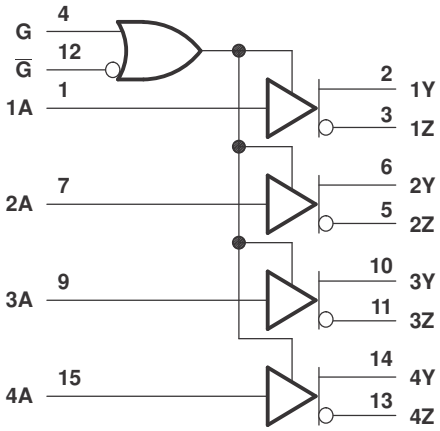
図 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

7 Detailed Description

7.1 Overview

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. The devices are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with a single 3.3-V power supply. The drivers also integrate active-high and active-low enables for precise device control.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Active high and active low

The devices can be configured using the G and G logic inputs to select transmitter output. A logic high on the G pin or a logic low on the G pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

7.3.2 Operates from a 3.3-V Supply with up to 5-V Logic

While the transmitters operate from a single 3.3-V rail, the logic can operate off the same rail or another 5-V rail, making designs much more flexible to communicate to controllers.

7.3.3 High Speed Transmission

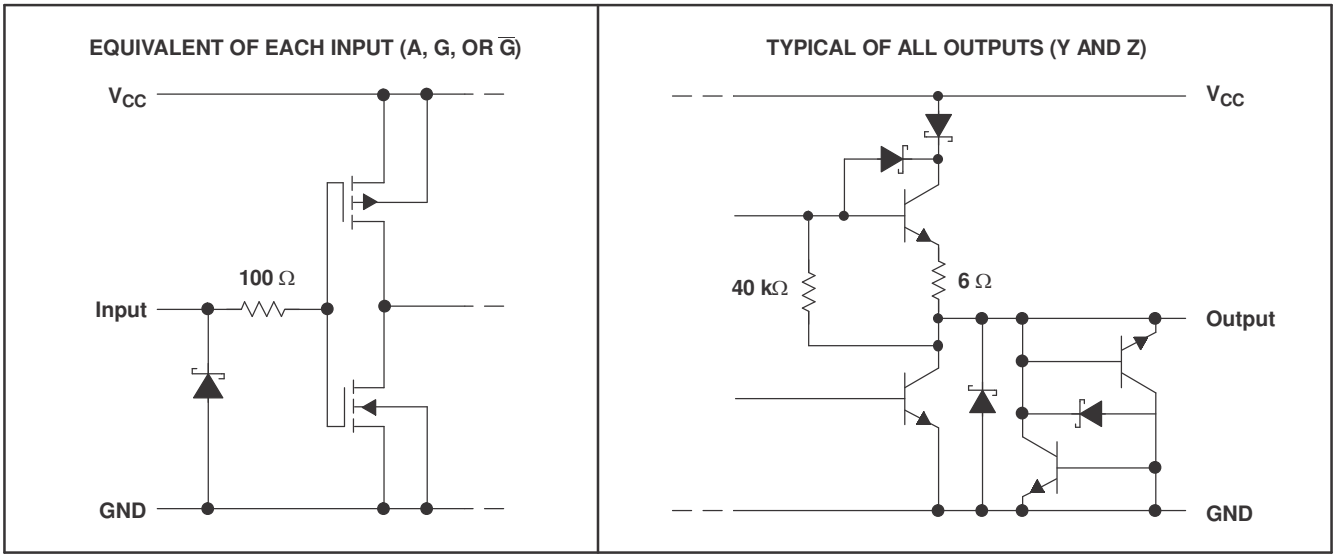
The AM26LV31C and AM26LV31I are optimized for balanced-bus transmission at switching rates up to 32 MHz. The devices are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

7.4 Device Functional Modes

表 7-1. Function Table(1)

INPUT A	ENABLES G	ENABLES $\overline{G}$	OUTPUTS Y	OUTPUTS Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)



ll resistor values are nominal.

図 7-1. Schematic (Each Driver)

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. If termination is used, it can be placed at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26LV31C and AM26LV32C, respectively, were tested at room temperature with a 3.3-V supply voltage. The first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

8.2 Typical Application

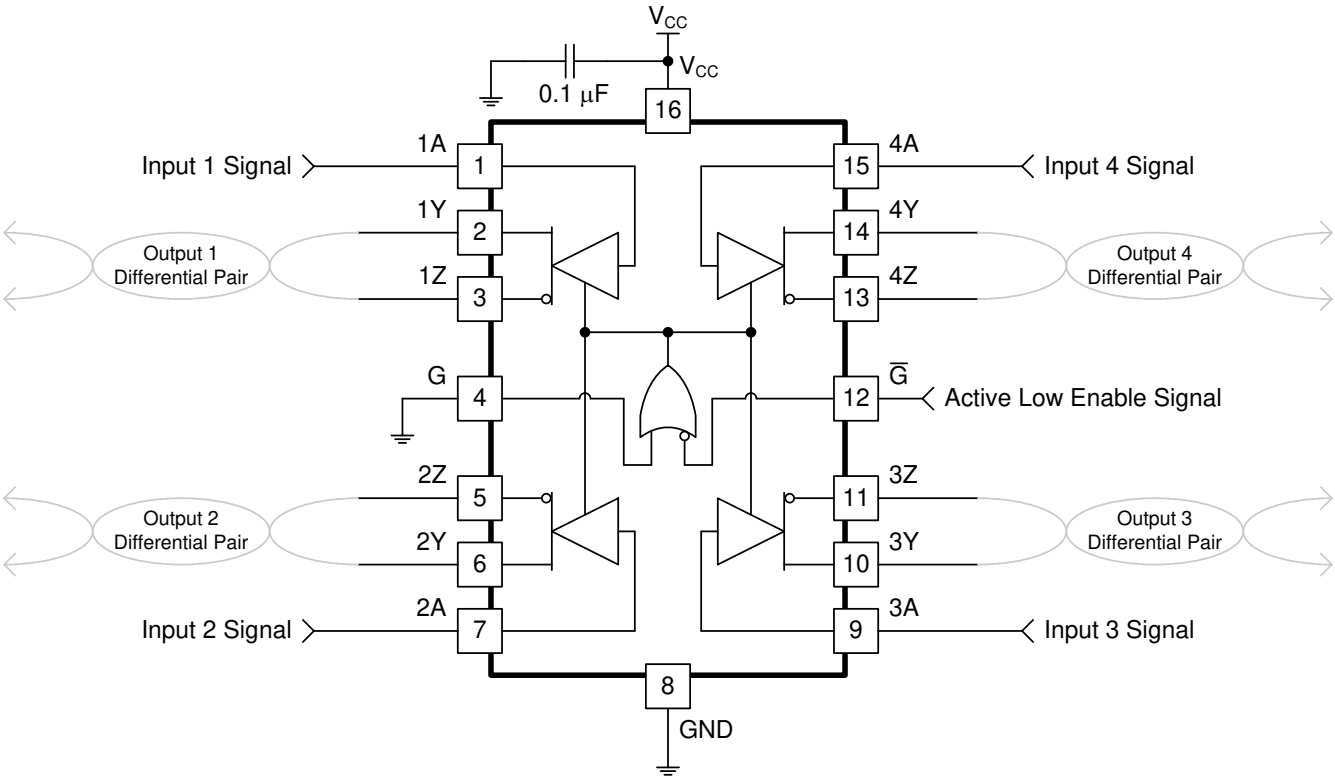


図 8-1. Differential Terminated Configuration With All Channels and Active Low Enable Used

8.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, RT, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80 Ω to 120 Ω.

This example requires the following:

- 3.3-V power source
- RS-485 bus operating at 32 MHz or less
- Connector that ensures the correct polarity for port pins

8.2.2 Detailed Design Procedure

Ensure values in Absolute Maximum Ratings are not exceeded. Supply voltage, V_{IH}, and V_{IL} must comply with Recommended Operating Conditions.

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to ensure 200 mV on the A-B port, if the drive is in high impedance state (see Failsafe in RS-485 data buses).

8.2.3 Application Curves

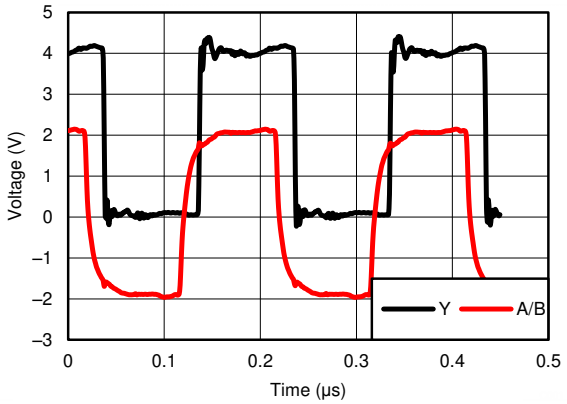


図 8-2. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place a 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between supply pin and ground, placed as close to the device as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

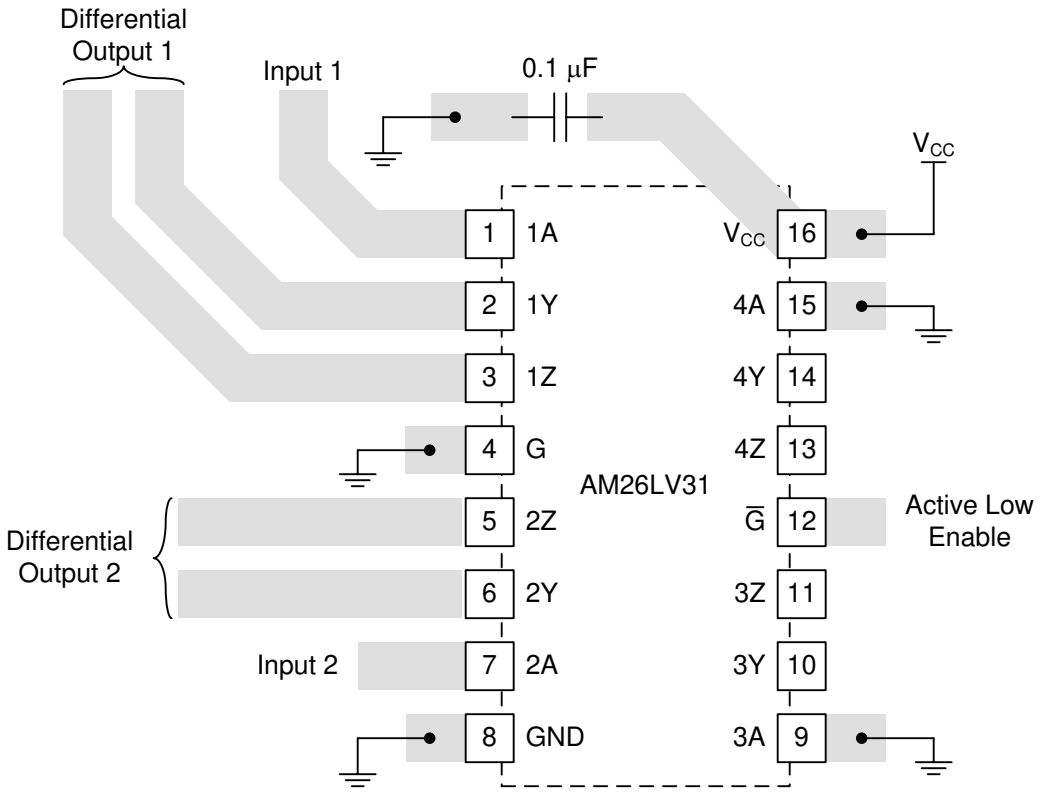


図 8-3. Trace Layout on PCB and Recommendations

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (April 2018) to Revision I (April 2024)	Page
• 「製品情報」を「パッケージ情報」表に変更	1
• Changed the *Thermal Information* table values	4
• Changed 図 5-1	6
• Changed the Note B in 図 6-2	7

Changes from Revision G (May 2005) to Revision H (April 2018)	Page
• 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• Changed the t_{PLH} and t_{PHL} MAX value From: 12 ns To: 20 ns in the *Switching Characteristics*	5
• Changed the $t_{sk(p)}$ and $t_{sk(o)}$ MAX value From: 1.5 ns To: 3 ns in the *Switching Characteristics*	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV31CD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26LV31C	
AM26LV31CDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26LV31C	
AM26LV31CDRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26LV31C	
AM26LV31CNSR	OBSOLETE	SOP	NS	16		TBD	Call TI	Call TI	0 to 70	26LV31	
AM26LV31ID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-45 to 85	AM26LV31I	
AM26LV31IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 85	AM26LV31I	Samples
AM26LV31INSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 85	26LV31I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

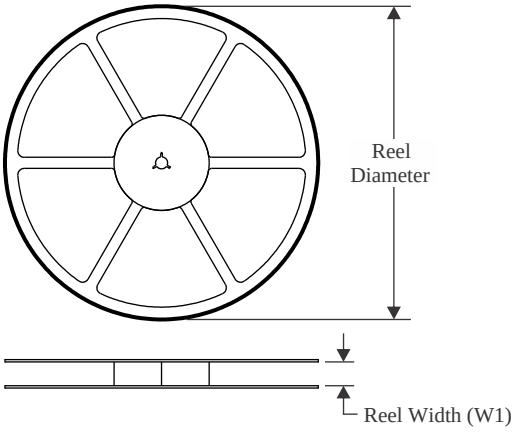
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

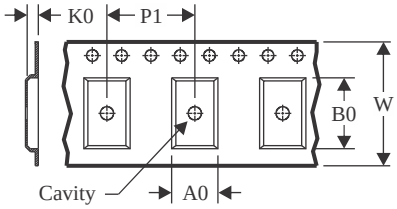
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

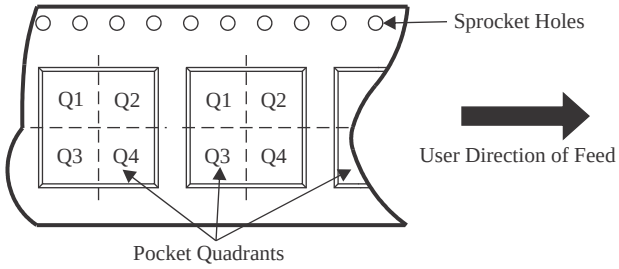


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

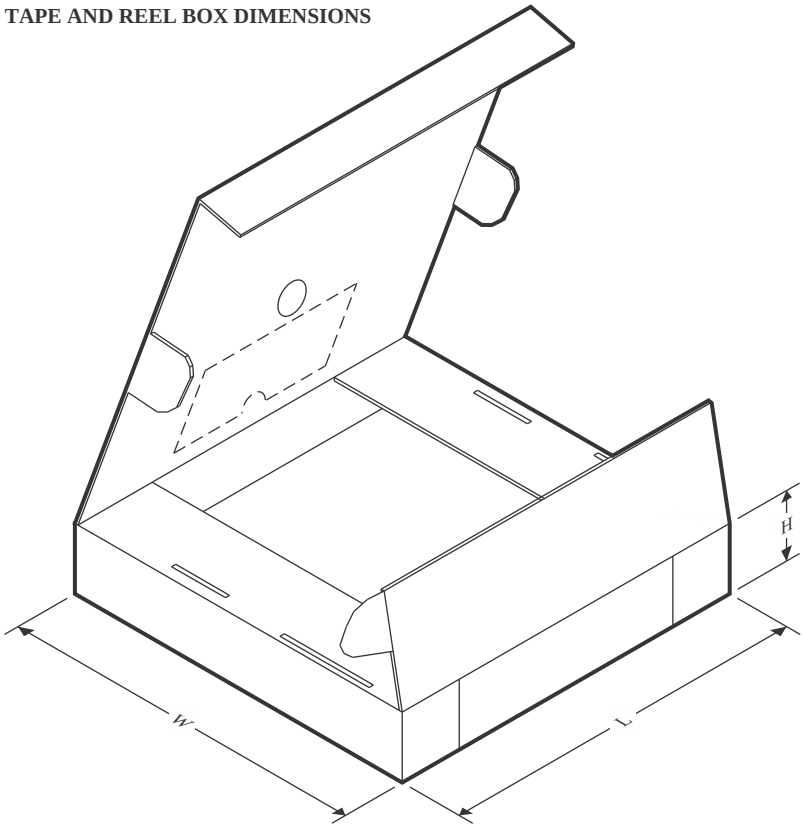
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31INSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

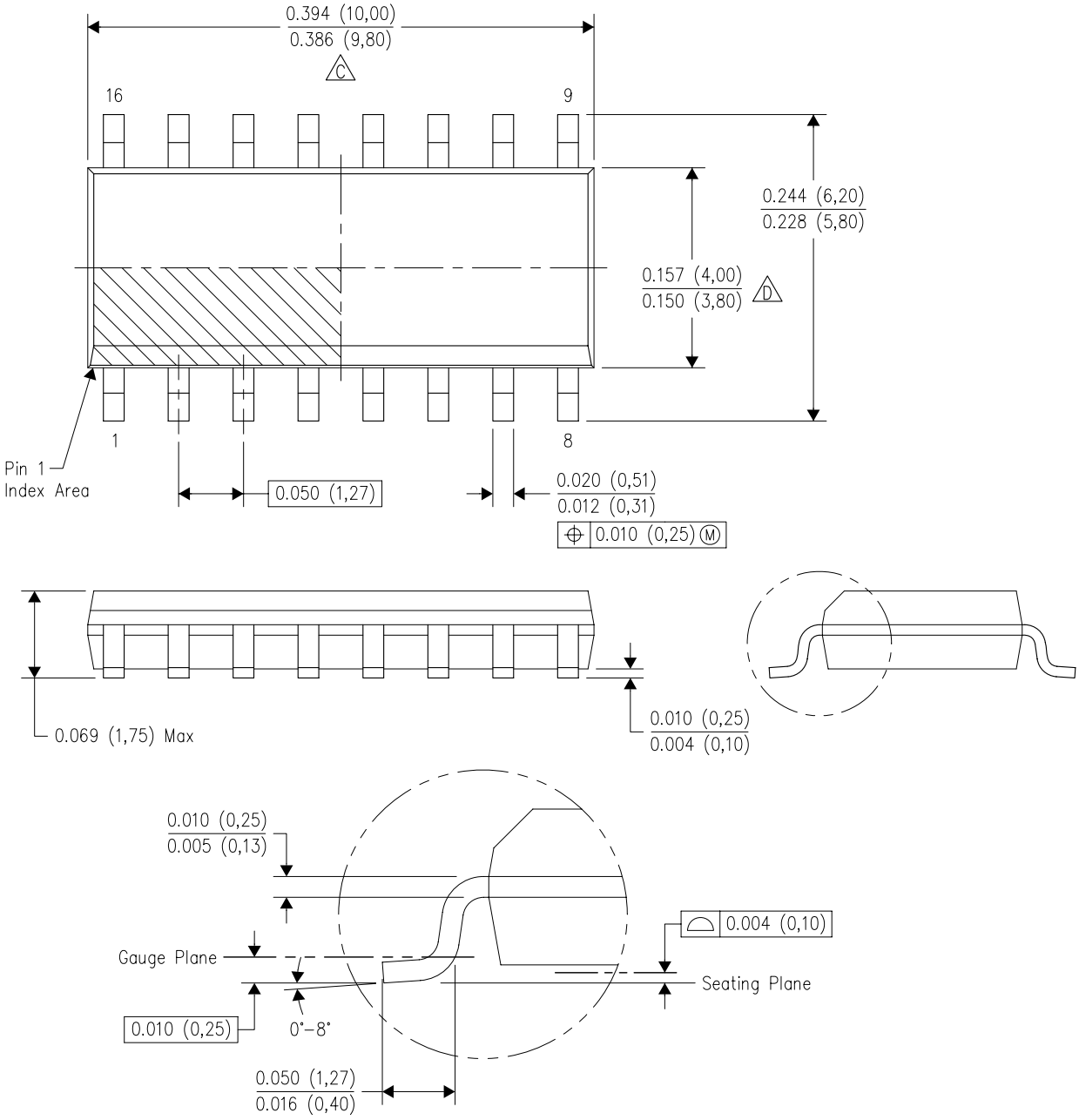
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31IDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LV31IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV31INSR	SOP	NS	16	2000	356.0	356.0	35.0
AM26LV31INSR	SOP	NS	16	2000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

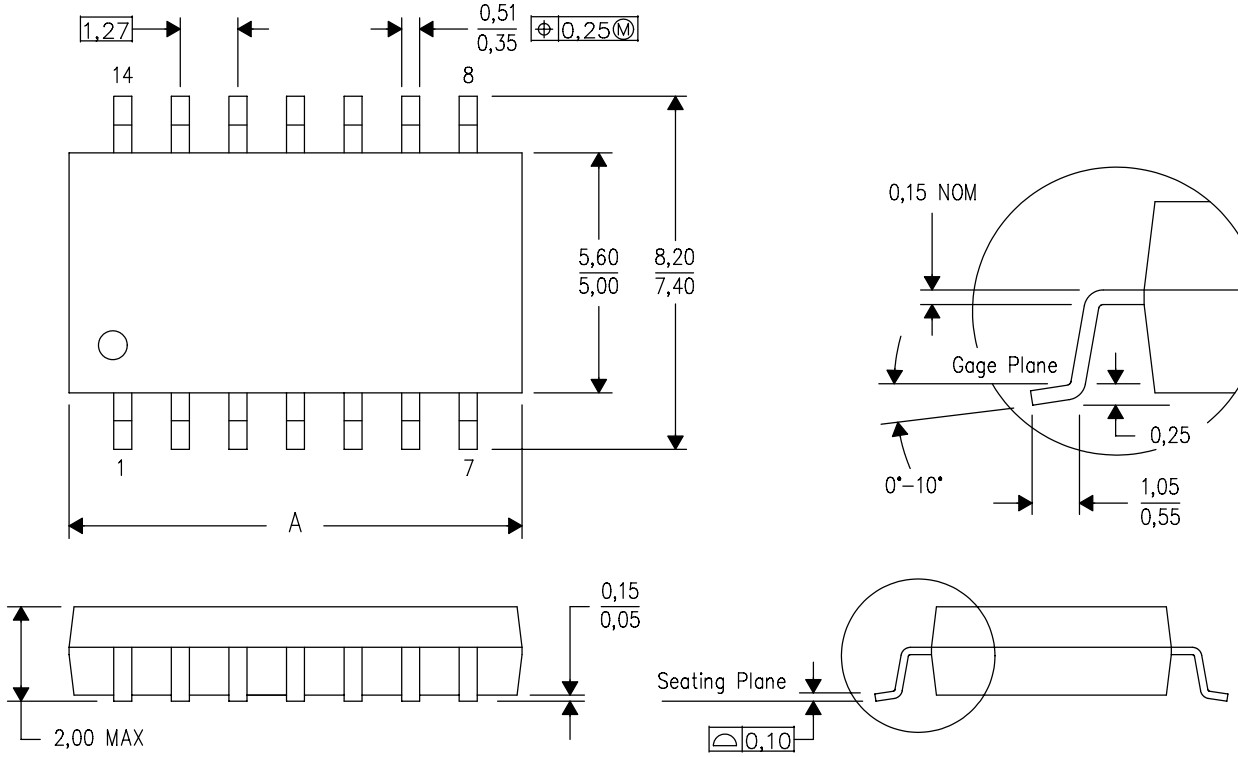


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

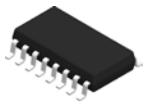
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

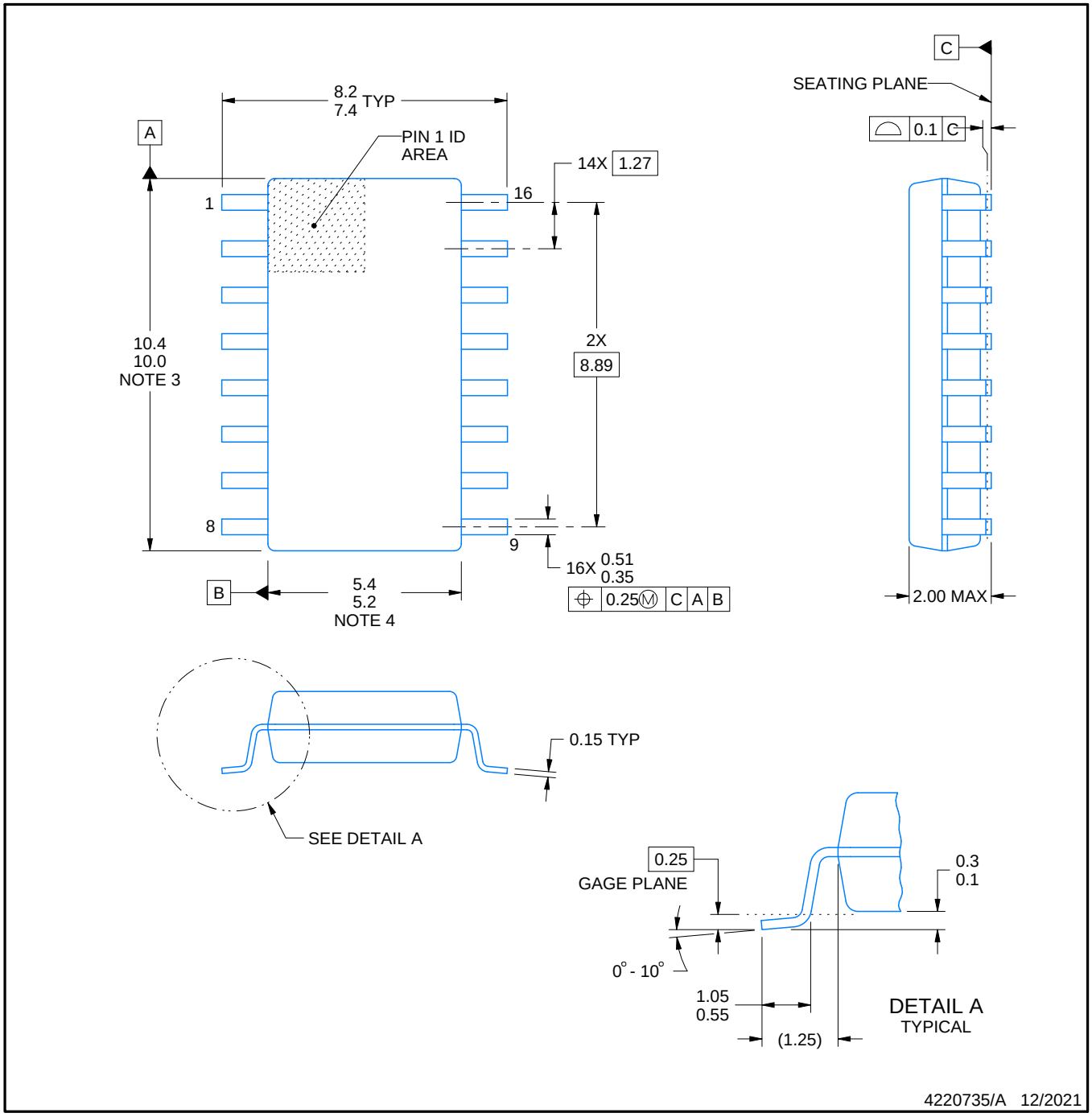


PACKAGE OUTLINE

NS0016A

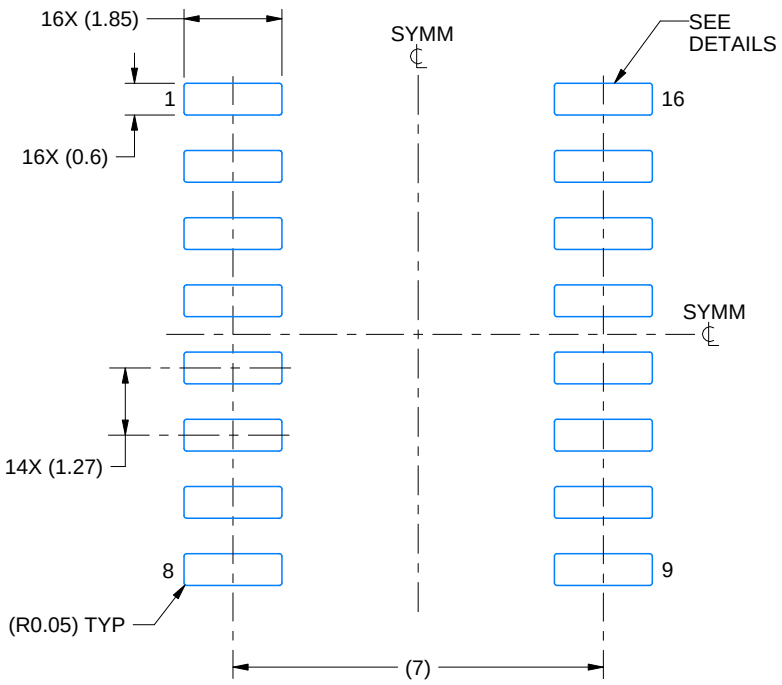
SOP - 2.00 mm max height

SOP

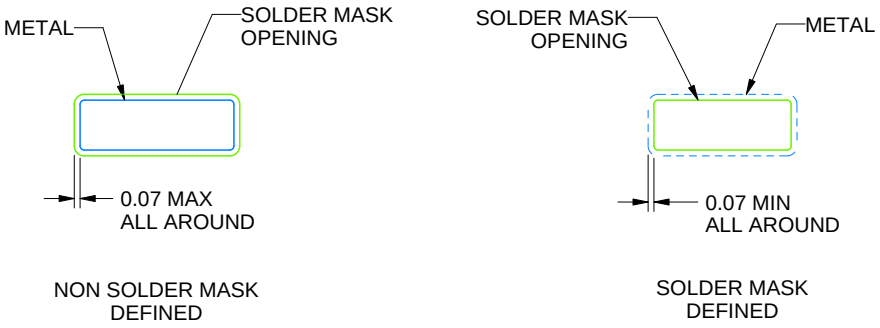


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

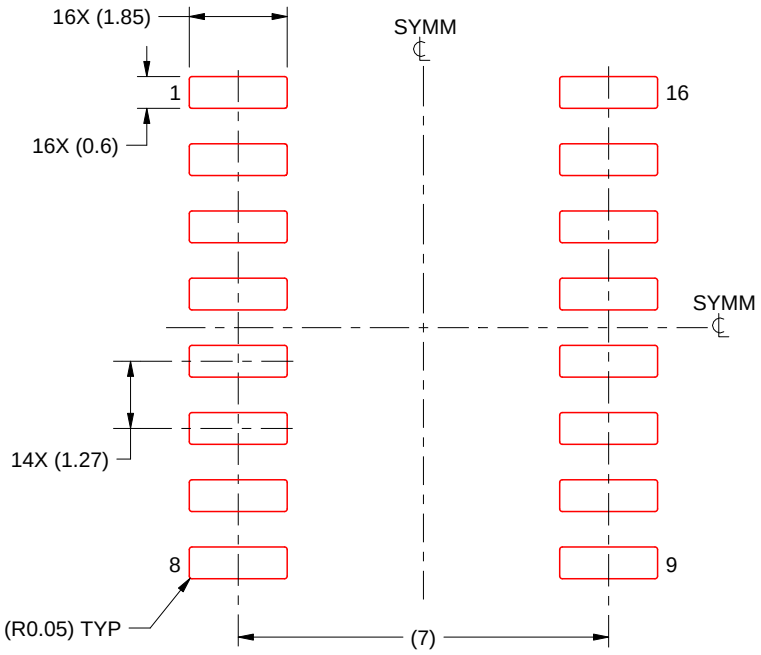
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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