

AMC1300B-Q1 車載用、高精度、 $\pm 250\text{mV}$ 入力、強化絶縁アンプ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, T_A
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- シャント抵抗を用いた電流測定用に最適化された $\pm 250\text{mV}$ の入力電圧範囲
- 固定ゲイン: 8.2V/V
- 小さな DC 誤差:
 - オフセット誤差: $\pm 0.2\text{mV}$ (最大値)
 - オフセット・ドリフト: $\pm 0.9\mu\text{V}/^{\circ}\text{C}$ (最大値)
 - ゲイン誤差: $\pm 0.3\%$ (最大値)
 - ゲイン・ドリフト: $\pm 30\text{ppm}/^{\circ}\text{C}$ (最大値)
 - 非線形性: 0.03% (最大値)
- ハイサイド、ローサイドとも 3.3V または 5V で動作可能
- フェイルセーフ出力
- 高 CMTI: $100\text{kV}/\mu\text{s}$ (最小値)
- 低 EMI、CISPR-11 および CISPR-25 規格に準拠
- 安全関連の認証:
 - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧: 7071V_{PK}
 - UL 1577 に準拠した絶縁耐圧: $5000\text{V}_{\text{RMS}}$ (1 分間)

2 アプリケーション

- 次のような機器で使用するシャント抵抗方式電流センシング:
 - HEV/EV 充電パイル
 - HEV/EV のオンボード・チャージャ (OBC)
 - HEV/EV の DC/DC コンバータ
 - HEV/EV のトラクション・インバータ

3 概要

AMC1300B-Q1 は高精度の絶縁型アンプで、磁気干渉に対して高い耐性のある絶縁バリアにより、入力側と出力側の回路が分離されています。この絶縁バリアは、DIN EN IEC 60747-17 (VDE 0884-17) および UL1577 に従って最大 5kV_{RMS} の強化ガルバニック絶縁を達成していることが認証されており、最大 $1.5\text{kV}_{\text{RMS}}$ の使用電圧に対応しています。

この絶縁バリアは、各種の同相電圧レベルで動作するシステム領域を分離し、危険な電圧と損傷から低電圧側を保護します。

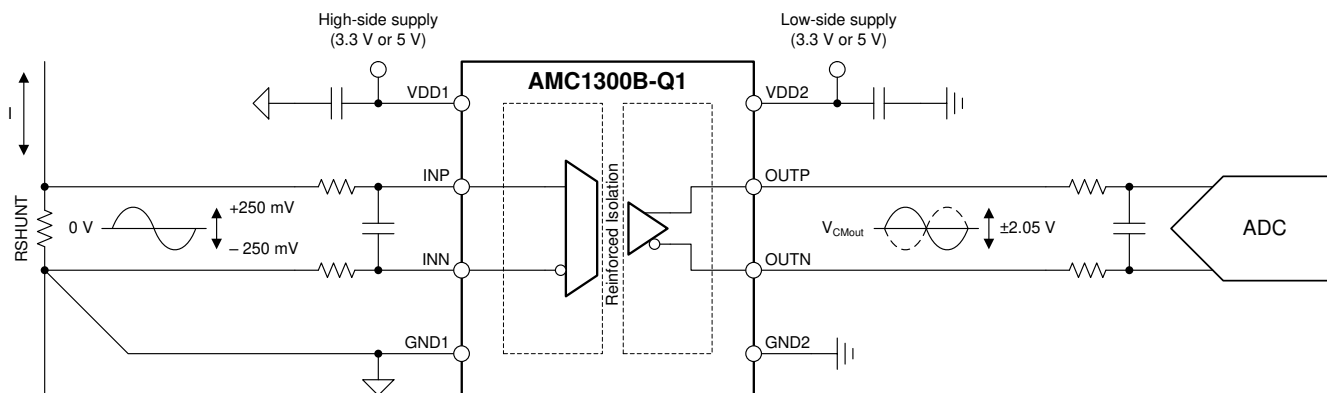
AMC1300B-Q1 の入力は、低インピーダンスのシャント抵抗またはその他の信号レベルが小さい低インピーダンス電圧源と直接接続できるように最適化されています。優れた DC 精度と小さい温度ドリフトにより、車載用温度範囲全体 ($-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$) にわたって、PFC 段、DC/DC コンバータ、トラクション・インバータ、OBC の高精度電流制御に対応できます。

シャント喪失およびハイサイド電源喪失検出機能を内蔵しているため、システム・レベルの設計と診断が簡単に行えます。

製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
AMC1300B-Q1	SOIC (8)	5.85mm × 7.50mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (January 2021) to Revision B (June 2022)	Page
• 絶縁規格を「DIN VDE V 0884-11 (VDE V 0884-11)」から「DIN EN IEC 60747-17 (VDE 0884-17)」に変更。それに応じて「絶縁仕様」と「安全関連認証」の表を更新.....	1
• 「特長」の一覧に機能安全対応の箇条書きを追加.....	1
• Changed external clearance (CLR) from ≥ 9 mm to ≥ 8.5 mm.....	6
• Changed C_{IO} from ~ 1 pF to ~ 1.5 pF.....	6

Changes from Revision * (April 2020) to Revision A (January 2021)	Page
• Changed external clearance (CLR) from ≥ 8.5 mm to ≥ 9 mm.....	6
• Changed TCV_{OS} from ± 3 $\mu V/^{\circ}C$ to ± 0.9 $\mu V/^{\circ}C$	8
• Changed TCE_G from ± 50 ppm/ $^{\circ}C$ to ± 30 ppm/ $^{\circ}C$	8
• Changed $VDD1_{UV}$ from 1.75 V (min) / 2.53 V (typ) / 2.7 V (max) to 2.4 V (min) / 2.6 V (typ) / 2.8 V (max).....	8

5 Pin Configuration and Functions

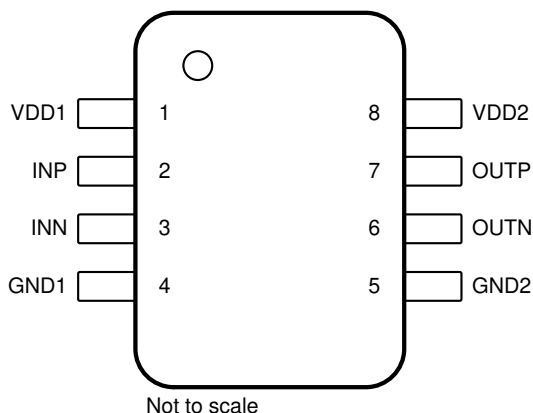


图 5-1. DWV Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply. ⁽¹⁾
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. ⁽²⁾
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. ⁽²⁾
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply. ⁽¹⁾

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Layout](#) section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see⁽¹⁾

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	−0.3	6.5	V
	Low-side VDD2 to GND2	−0.3	6.5	
Analog input voltage	INP, INN	GND1 − 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T _J		150	°C
	Storage, T _{stg}	−65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ , HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
V _{Clipping}	Differential input voltage before clipping output	V _{IN} = V _{INP} − V _{INN}		±320		mV
V _{FSR}	Specified linear differential full-scale voltage	V _{IN} = V _{INP} − V _{INN}	−250		250	mV
V _{CM}	Operating common-mode input voltage	(V _{INP} + V _{INN}) / 2 to GND1	−0.16		VDD1 − 2.1	V
TEMPERATURE RANGE						
T _A	Specified ambient temperature		−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC1300B-Q1	UNIT
		DWV (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	85.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	26.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	41.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P _D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
P _{D1}	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
P _{D2}	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V _{RMS}
		At DC voltage	2120	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	7000	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	8400	
V _{IMP}	Maximum impulse voltage ⁽³⁾	Tested in air, 1.2/50-μs waveform per IEC 62368-1	9800	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽⁴⁾	Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	V _{PK}
q _{pd}	Apparent charge ⁽⁵⁾	Method a, after input/output safety test subgroups 2 and 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.5 V _{PP} at 1 MHz	~1.5	pF
R _{IO}	Insulation resistance, input to output ⁽⁶⁾	V _{IO} = 500 V at T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V at 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5000 V _{RMS} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6000 V _{RMS} , t = 1 s (100% production test)	5000	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current	R _{θJA} = 85.4°C/W, VDDx = 5.5 V, T _J = 150°C, T _A = 25°C			266	mA
I _S	Safety input, output, or supply current	R _{θJA} = 85.4°C/W, VDDx = 3.6 V, T _J = 150°C, T _A = 25°C			407	mA
P _S	Safety input, output, or total power	R _{θJA} = 85.4°C/W, T _J = 150°C, T _A = 25°C			1464	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.

T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum junction temperature.

P_S = I_S × VDD_{max}, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.9 Electrical Characteristics

minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $\text{INN} = \text{GND1}$; typical specifications are at $T_A = 25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V _{CMov}	Common-mode overvoltage detection level	(V _{INP} + V _{INN}) / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level		60			mV
V _{OS}	Input offset voltage ⁽¹⁾	Initial, at T _A = 25°C, INP = INN = GND1	–0.2	±0.01	0.2	mV
TCV _{OS}	Input offset drift ^{(1) (4)}		–0.9	±0.1	0.9	µV/°C
CMRR	Common-mode rejection ratio	f _{IN} = 0 Hz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–100			dB
		f _{IN} = 10 kHz, V _{CM min} ≤ V _{CM} ≤ V _{CM max}	–98			
R _{IN}	Single-ended input resistance	INN = GND1	19			kΩ
R _{IND}	Differential input resistance		22			kΩ
I _{IB}	Input bias current	INP = INN = GND1; I _{IB} = (I _{IBP} + I _{IBN}) / 2	–41	–30	–24	µA
I _{IO}	Input offset current	I _{IO} = I _{IBP} – I _{IBN} ; INP = INN = GND1	±5			nA
C _{IN}	Single-ended input capacitance	INN = GND1, f _{IN} = 275 kHz	2			pF
C _{IND}	Differential input capacitance	f _{IN} = 275 kHz	1			pF
ANALOG OUTPUT						
	Nominal gain		8.2			V/V
E _G	Gain error ⁽¹⁾	at T _A = 25°C	–0.3%	±0.04%	0.3%	
TCE _G	Gain drift ^{(1) (5)}		–30	±5	30	ppm/°C
	Nonlinearity ⁽¹⁾		–0.03%	±0.01%	0.03%	
THD	Total harmonic distortion ⁽³⁾	f _{IN} = 10 kHz	–85			dB
	Output noise	INP = INN = GND1, f _{IN} = 0 Hz, BW = 100 kHz brickwall filter	230			µV _{RMS}
SNR	Signal-to-noise ratio	f _{IN} = 1 kHz, BW = 10 kHz	81.5	85		dB
		f _{IN} = 10 kHz, BW = 100 kHz	72			
PSRR	Power-supply rejection ratio ⁽²⁾	PSRR vs VDD1, at DC	–103			dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple	–96			
		PSRR vs VDD2, at DC	–106			
		PSRR vs VDD2, 100-mV and 10-kHz ripple	–86			
V _{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
V _{CLIPout}	Clipping differential output voltage	V _{OUT} = (V _{OUTP} – V _{OUTN}); V _{IN} = V _{INP} – V _{INN} > V _{Clipping}	–2.52	±2.49	2.52	V
V _{Failsafe}	Failsafe differential output voltage	V _{CM} ≥ V _{CMov} , or VDD1 missing	–2.63	–2.57	–2.53	V
BW	Output bandwidth		250	310		kHz
R _{OUT}	Output resistance	On OUTP or OUTN	< 0.2			Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2	14			mA
CMTI	Common-mode transient immunity	GND1 – GND2 = 1 kV	100	150		kV/µs

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD1} = 3.0\text{ V}$ to 5.5 V , $V_{DD2} = 3.0\text{ V}$ to 5.5 V , $\text{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $\text{INN} = \text{GND1}$; typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
VDD1 _{UV}	VDD1 undervoltage detection threshold voltage	VDD1 falling	2.4	2.6	2.8	V
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

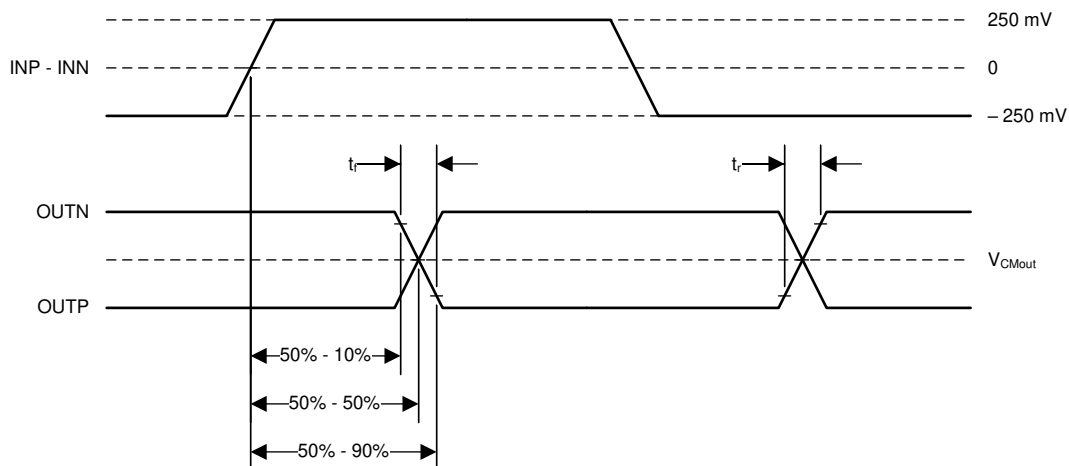
- (1) The typical value includes one standard deviation (σ) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:
 $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / \text{TempRange}$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (-40 to 125°C).
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:
 $TCE_G (\text{ppm}) = ((E_{G,MAX} - E_{G,MIN}) / \text{TempRange}) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (-40 to 125°C).

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

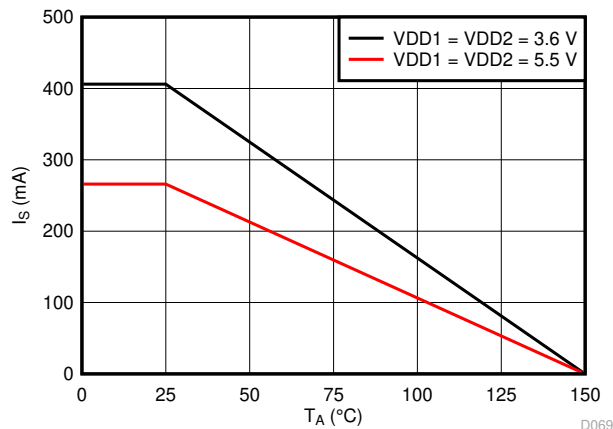
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time		1.3		μs
t_f	Output signal fall time		1.3		μs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output	1	1.5	μs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output	1.6	2.1	μs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output	2.5	3	μs
t_{AS}	Analog settling time	V_{DD1} step to 3.0 V with $V_{DD2} \geq 3.0\text{ V}$, to V_{OUTP} , V_{OUTN} valid, 0.1% settling	500		μs

6.11 Timing Diagram

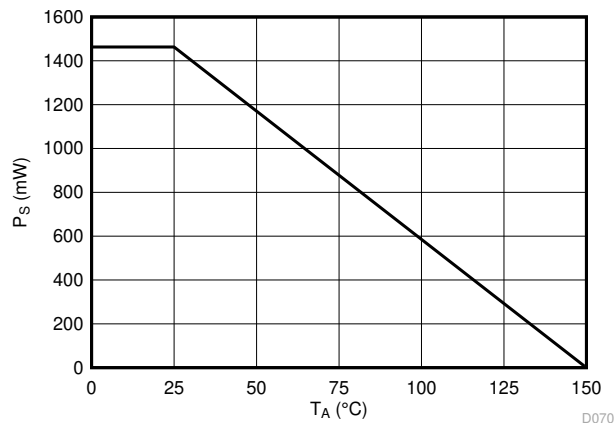


6-1. Rise, Fall, and Delay Time Definition

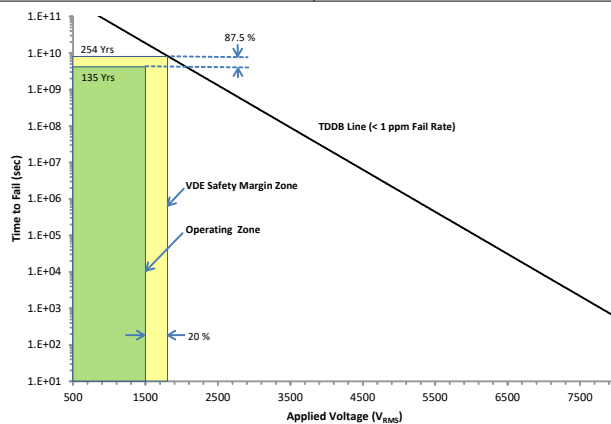
6.12 Insulation Characteristics Curves



6-2. Thermal Derating Curve for Safety-Limiting Current per VDE



6-3. Thermal Derating Curve for Safety-Limiting Power per VDE

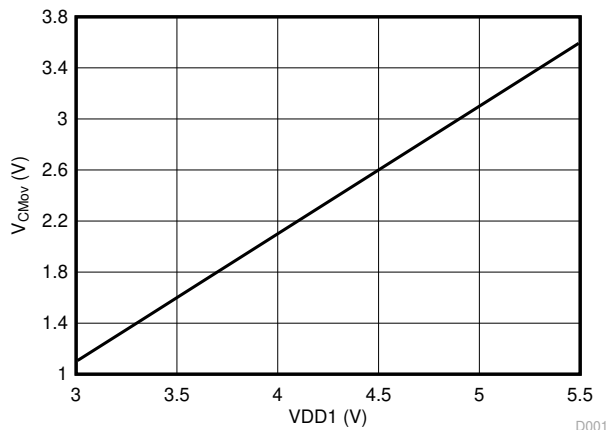


T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS} , operating lifetime = 135 year

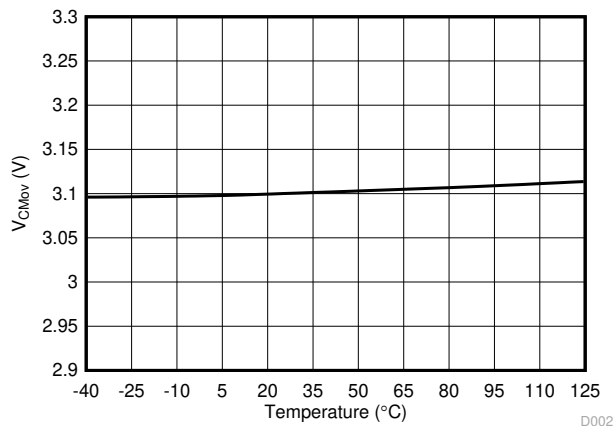
6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

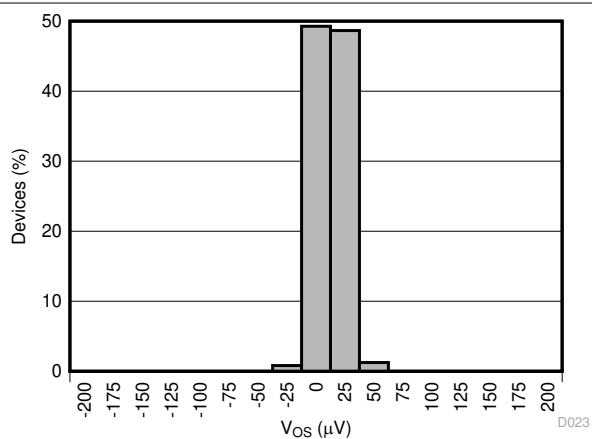
at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)



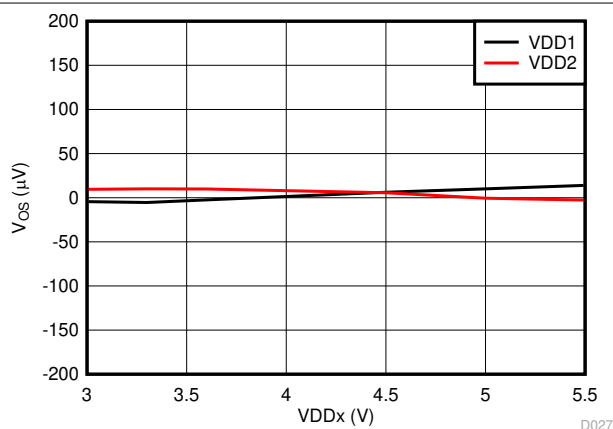
6-5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage



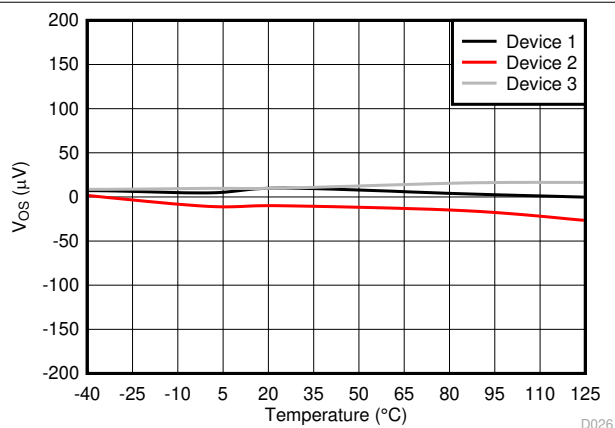
6-6. Common-Mode Overvoltage Detection Level vs Temperature



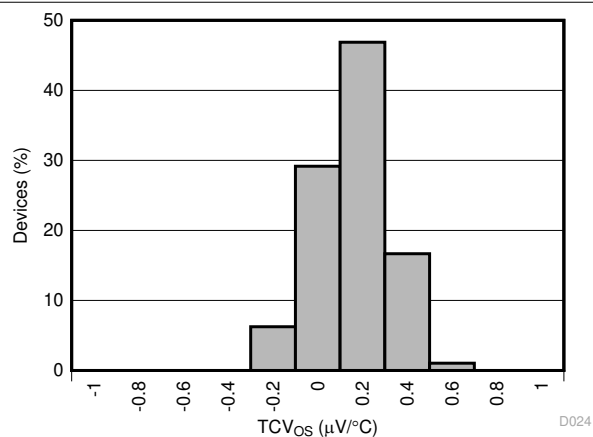
6-7. Input Offset Voltage Histogram



6-8. Input Offset Voltage vs Supply Voltage



6-9. Input Offset Voltage vs Temperature



6-10. Input Offset Drift Histogram

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

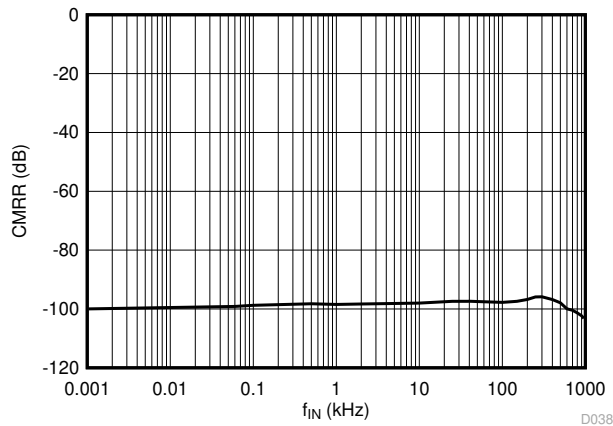


Figure 6-11. Common-Mode Rejection Ratio vs Input Frequency

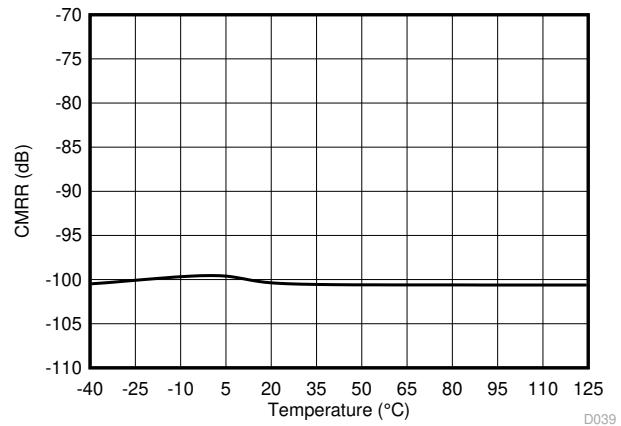


Figure 6-12. Common-Mode Rejection Ratio vs Temperature

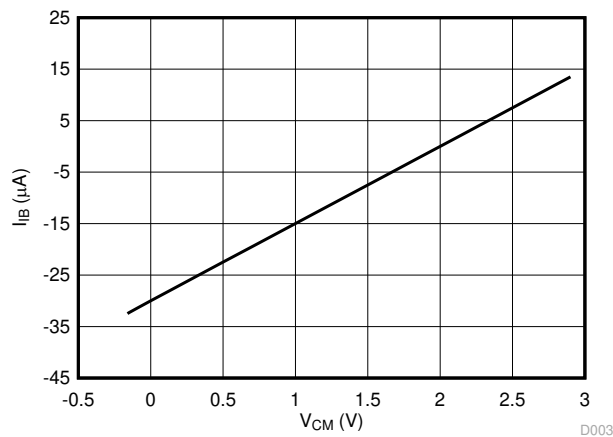


Figure 6-13. Input Bias Current vs Common-Mode Input Voltage

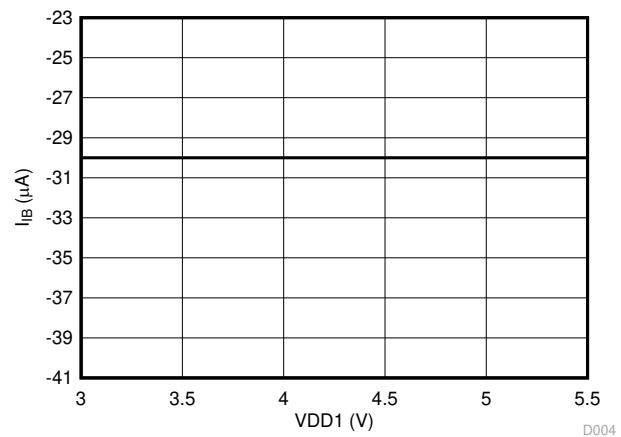


Figure 6-14. Input Bias Current vs High-Side Supply Voltage

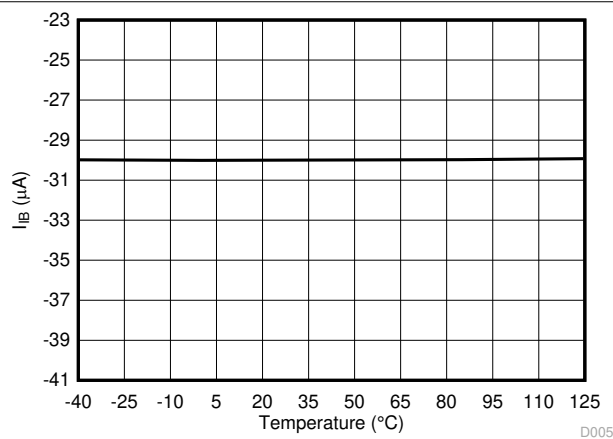


Figure 6-15. Input Bias Current vs Temperature

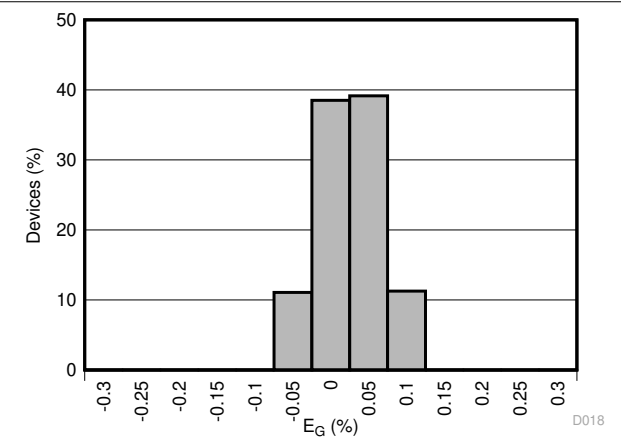


Figure 6-16. Gain Error Histogram

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

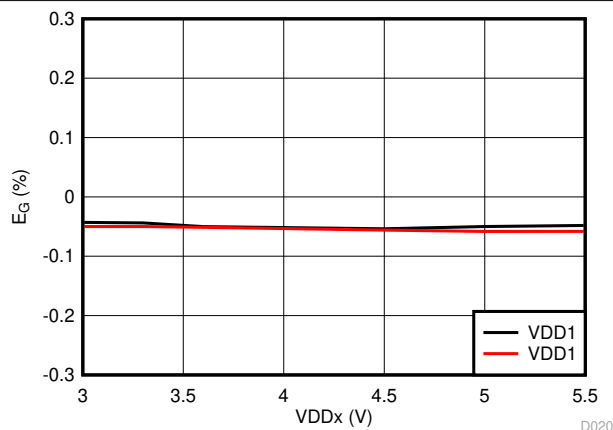


Figure 6-17. Gain Error vs Supply Voltage

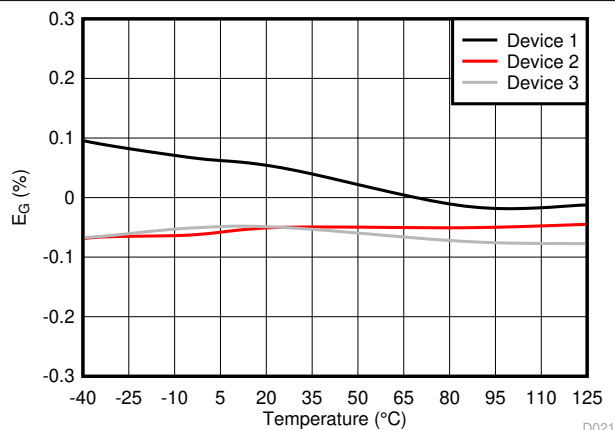


Figure 6-18. Gain Error vs Temperature

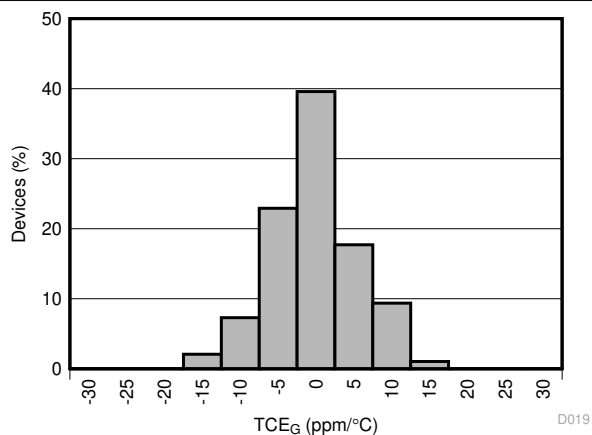


Figure 6-19. Gain Error Drift Histogram

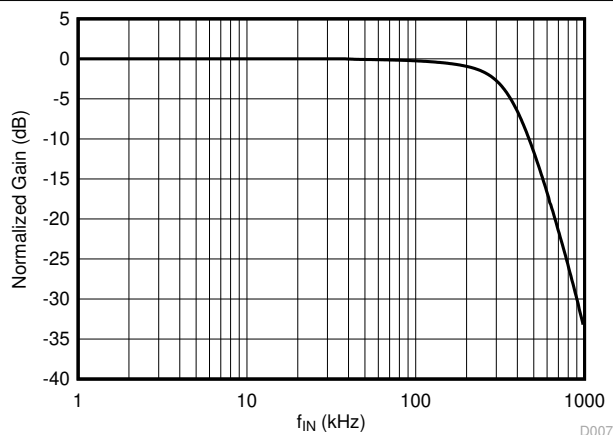


Figure 6-20. Normalized Gain vs Input Frequency

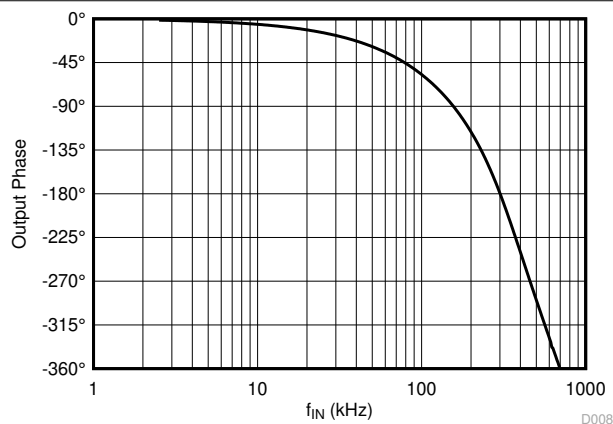


Figure 6-21. Output Phase vs Input Frequency

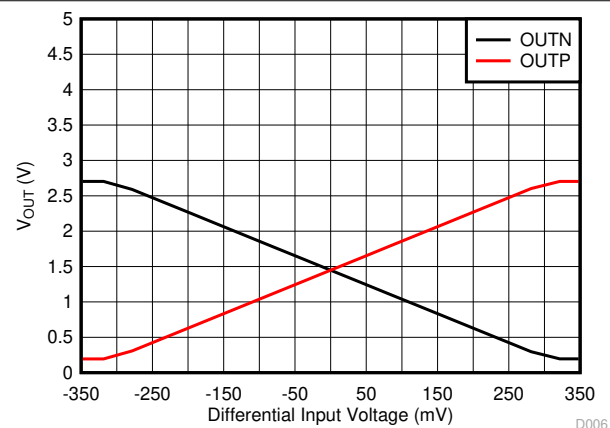
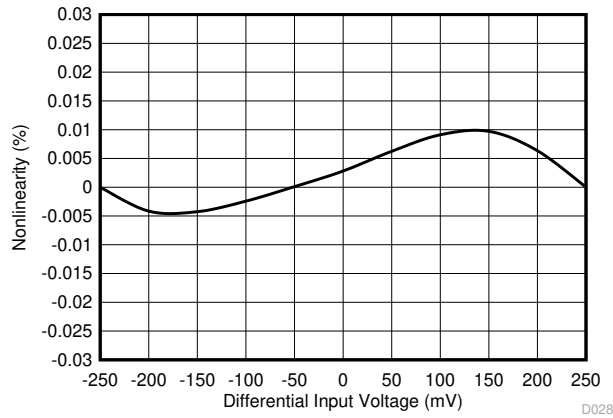


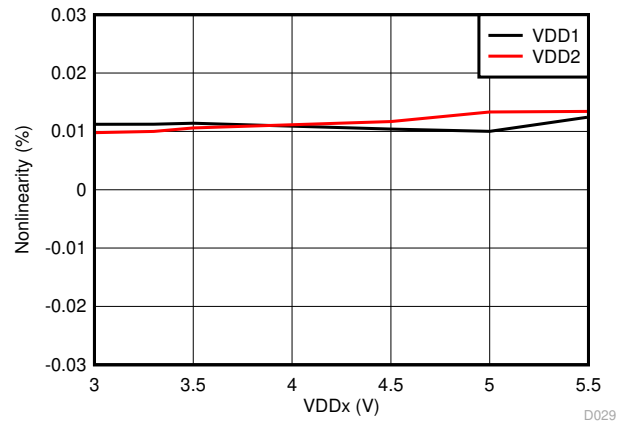
Figure 6-22. Output Voltage vs Input Voltage

6.13 Typical Characteristics (continued)

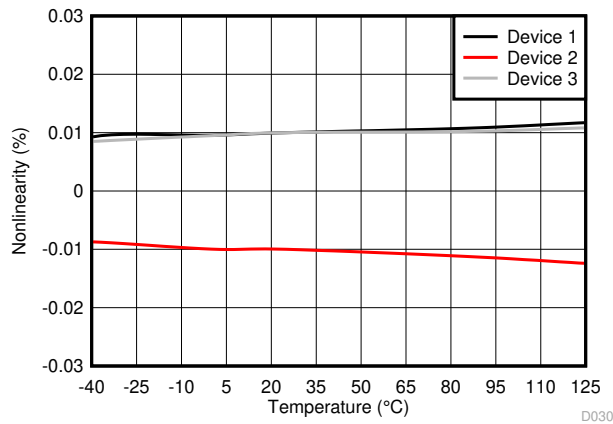
at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)



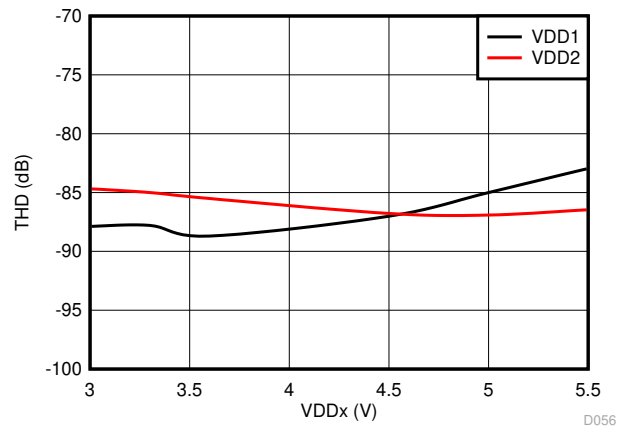
6-23. Nonlinearity vs Input Voltage



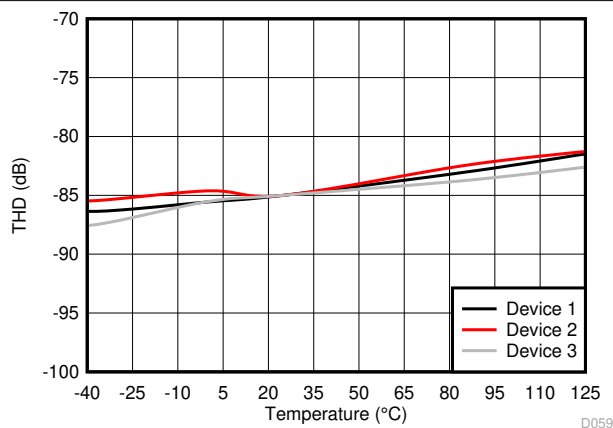
6-24. Nonlinearity vs Supply Voltage



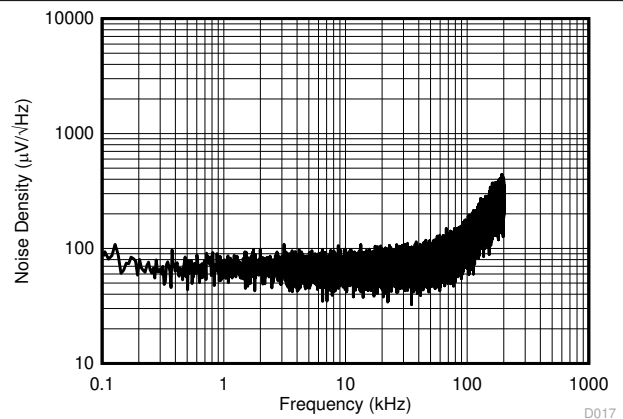
6-25. Nonlinearity vs Temperature



6-26. Total Harmonic Distortion vs Supply Voltage



6-27. Total Harmonic Distortion vs Temperature



6-28. Input-Referred Noise Density vs Frequency

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

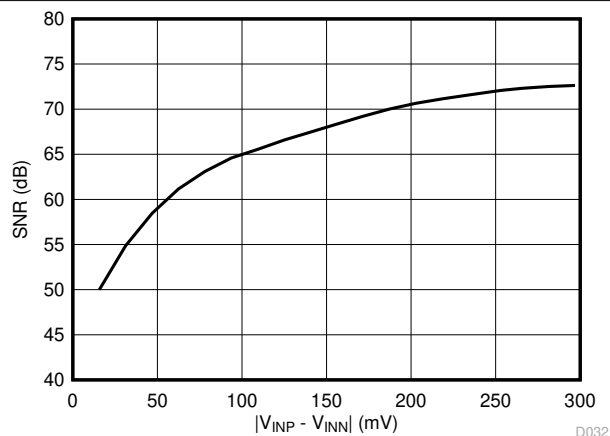


Figure 6-29. Signal-to-Noise Ratio vs Input Voltage

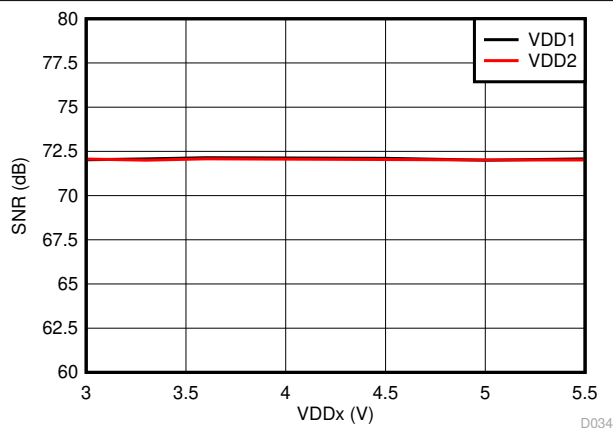


Figure 6-30. Signal-to-Noise Ratio vs Supply Voltage

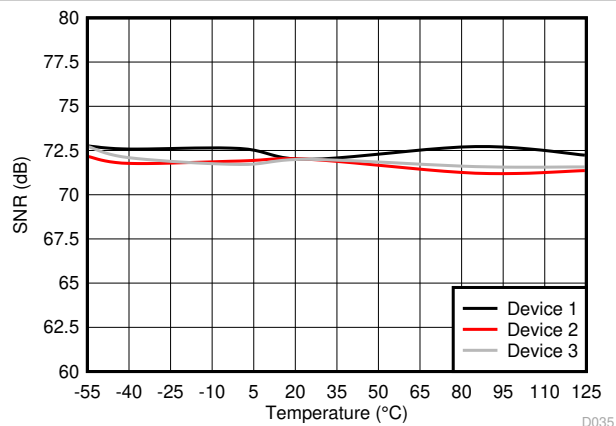


Figure 6-31. Signal-to-Noise Ratio vs Temperature

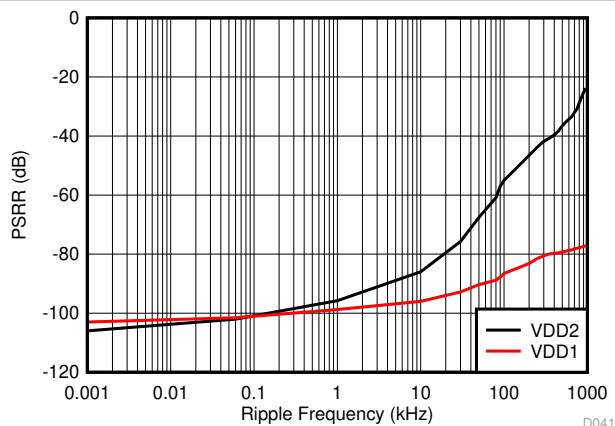


Figure 6-32. Power-Supply Rejection Ratio vs Ripple Frequency

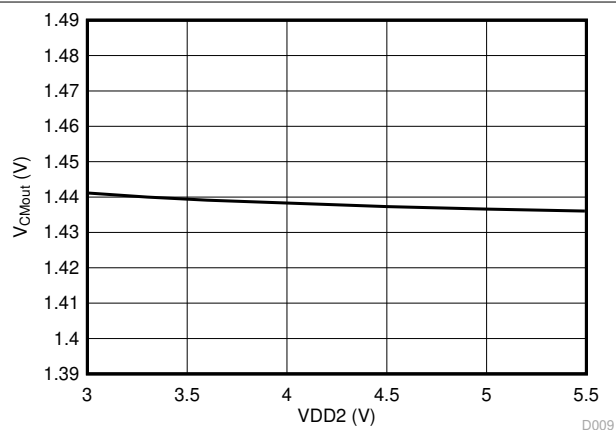


Figure 6-33. Output Common-Mode Voltage vs Low-Side Supply Voltage

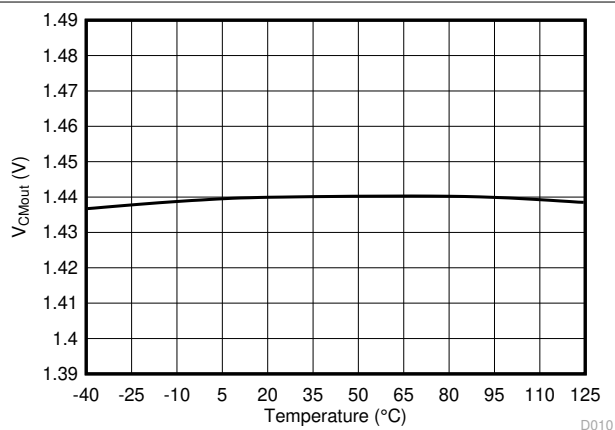


Figure 6-34. Output Common-Mode Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and $f_{IN} = 10$ kHz (unless otherwise noted)

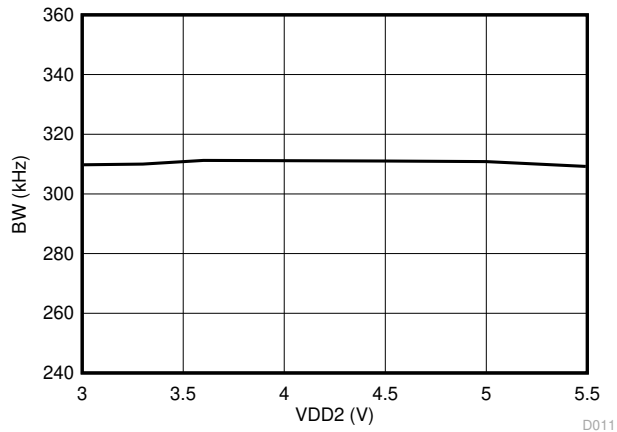


Figure 6-35. Output Bandwidth vs Low-Side Supply Voltage

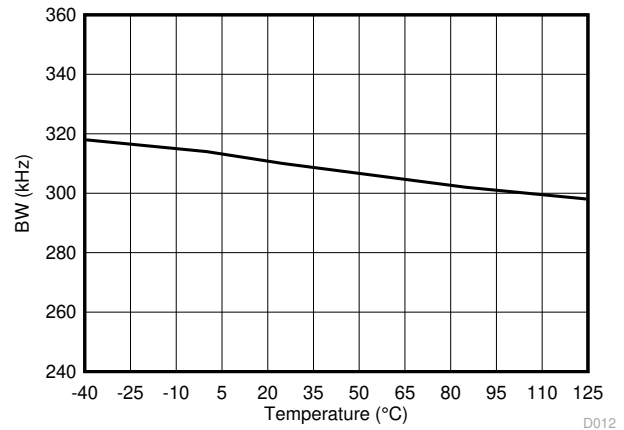


Figure 6-36. Output Bandwidth vs Temperature

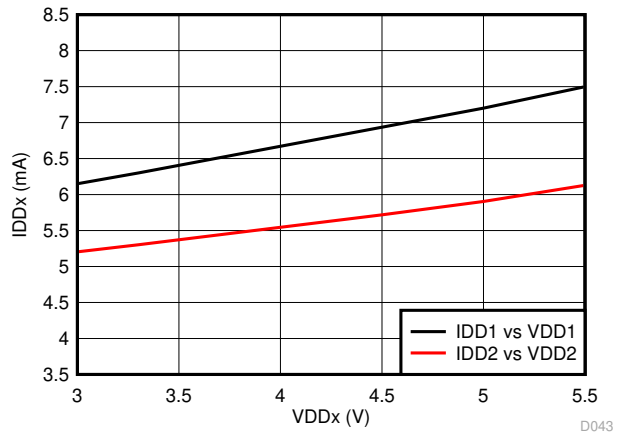


Figure 6-37. Supply Current vs Supply Voltage

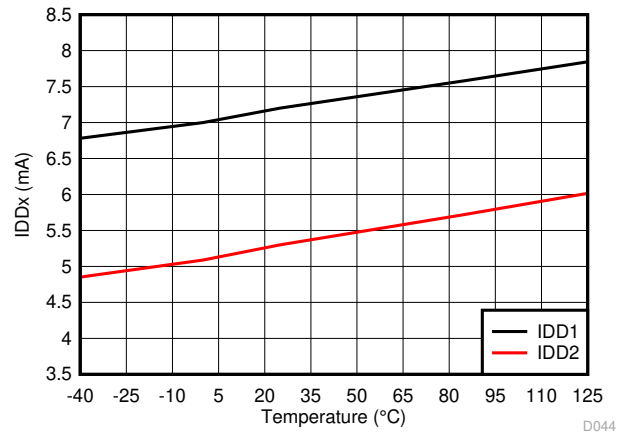


Figure 6-38. Supply Current vs Temperature

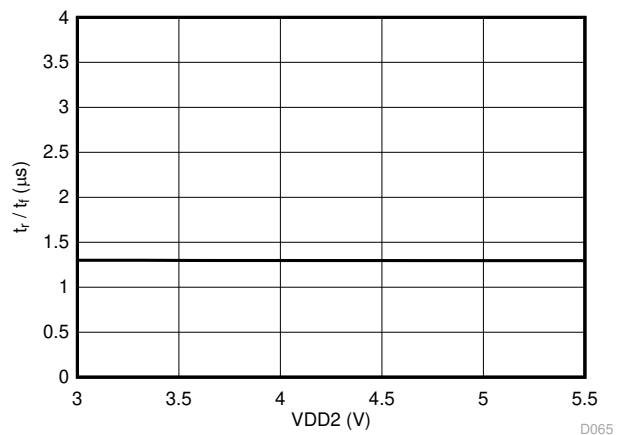


Figure 6-39. Output Rise and Fall Time vs Low-Side Supply

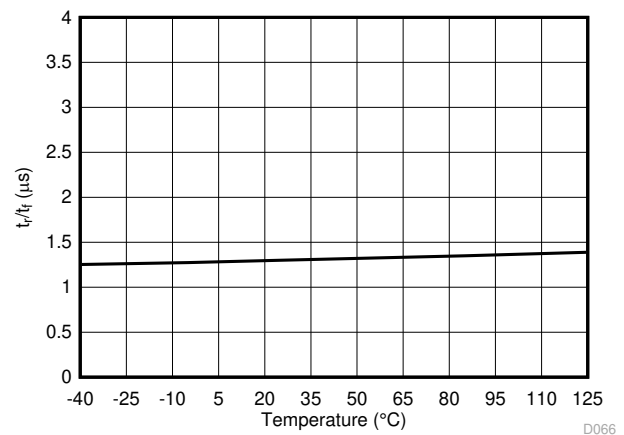
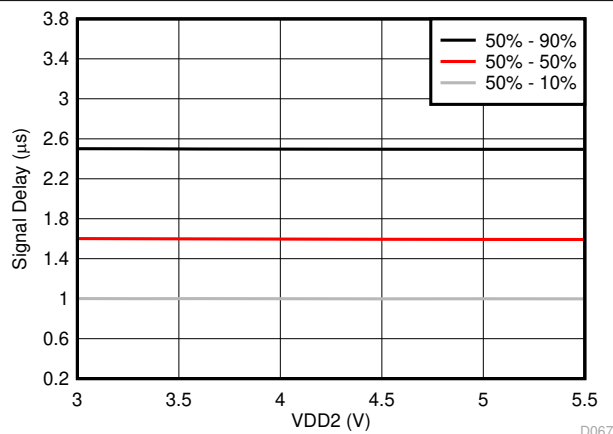


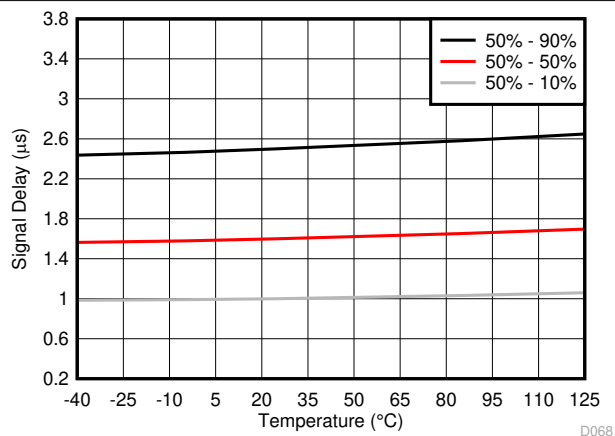
Figure 6-40. Output Rise and Fall Time vs Temperature

6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = –250 mV to 250 mV, INN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



6-41. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage



6-42. V_{IN} to V_{OUT} Signal Delay vs Temperature

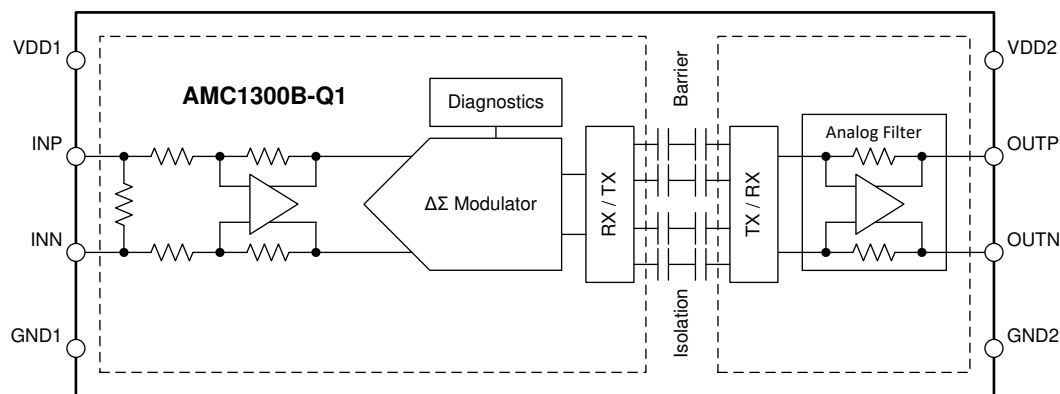
7 Detailed Description

7.1 Overview

The AMC1300B-Q1 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO₂-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application report](#). The digital modulation used in the AMC1300B-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1300B-Q1 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND} . The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the [Absolute Maximum Ratings](#) table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the [Recommended Operating Conditions](#) table.

7.3.2 Isolation Channel Signal Transmission

The AMC1300B-Q1 uses an on-off keying (OOK) modulation scheme, as shown in [Figure 7-1](#), to transmit the modulator output bitstream across the SiO₂-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1300B-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the 4th-order analog filter. The AMC1300B-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

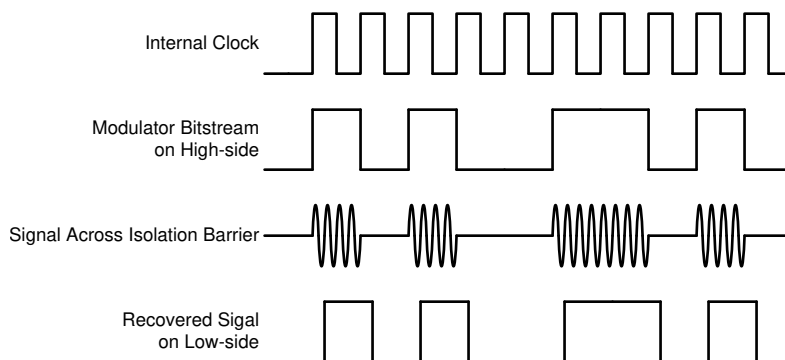


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC1300B-Q1 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ($V_{INP} - V_{INN}$) in the range from -250 mV to 250 mV , the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV , the differential output voltage ($V_{OUTP} - V_{OUTN}$) is 2.05 V . At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout} , as specified in the [Electrical Characteristics](#) table. For absolute differential input voltages greater than 250 mV but less than 320 mV , the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in [Figure 7-2](#), if the differential input voltage exceeds the $V_{Clipping}$ value.

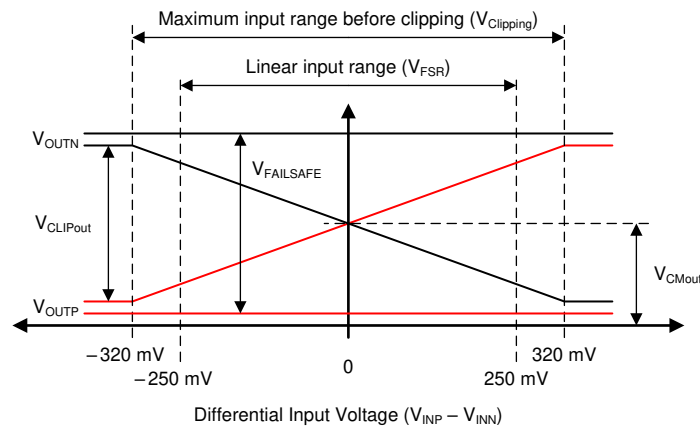


Figure 7-2. Output Behavior of the AMC1300B-Q1

The AMC1300B-Q1 offers a failsafe feature that simplifies diagnostics on system level. [Figure 7-2](#) shows the failsafe mode, in which the AMC1300B-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The failsafe output is active in two cases:

- When the high-side supply is missing or below the V_{DD1UV} threshold
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the common-mode overvoltage detection level V_{CMov}

Use the maximum $V_{FAILSAFE}$ voltage specified in the [Electrical Characteristics](#) table as a reference value for failsafe detection on system level.

7.4 Device Functional Modes

The AMC1300B-Q1 is operational when the power supplies V_{DD1} and V_{DD2} are applied, as specified in the [Recommended Operating Conditions](#) table.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC1300B-Q1 a high-performance solution for automotive applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

8.2 Typical Application

The AMC1300B-Q1 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

図 8-1 shows the AMC1300B-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1300B-Q1. The AMC1300B-Q1 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1300B-Q1 ensure reliable and accurate operation even in high-noise environments.

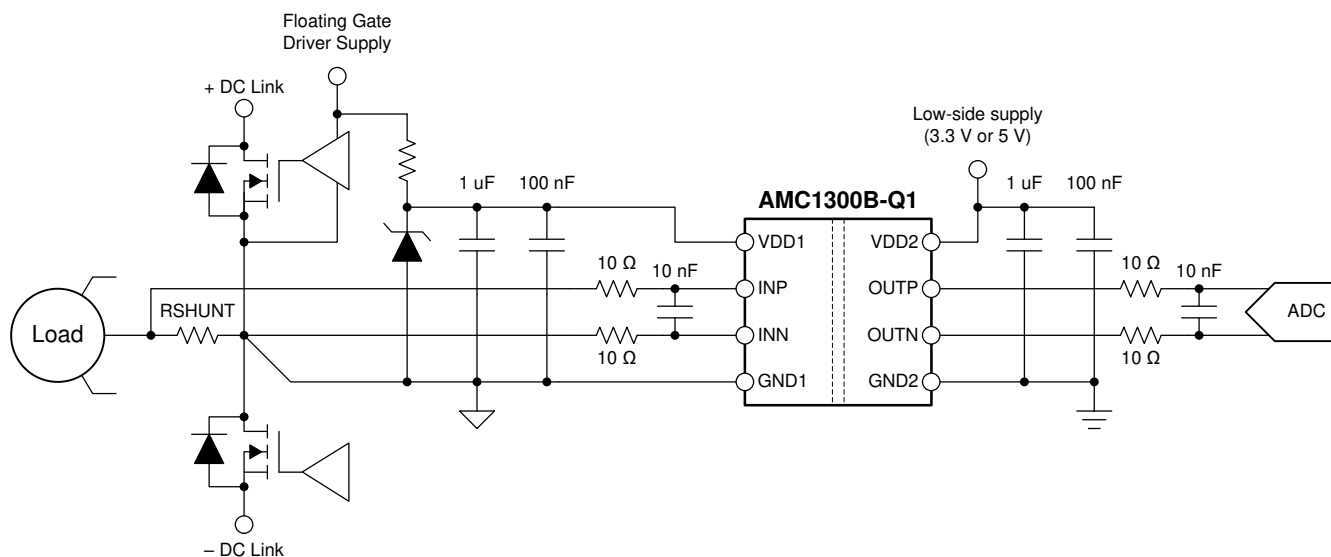


図 8-1. Using the AMC1300B-Q1 for Current Sensing in a Typical Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±250 mV (maximum)
Signal delay (50% V_{IN} to 90% OUTP, OUTN)	3 μ s (maximum)

8.2.2 Detailed Design Procedure

In 图 8-1, the high-side power supply (VDD1) for the AMC1300B-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1300B-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1300B-Q1 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the [Layout](#) section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions when selecting the value of the shunt resistor, R_{SHUNT} :

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC-filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the $\Delta\Sigma$ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 图 8-2 achieves excellent performance.

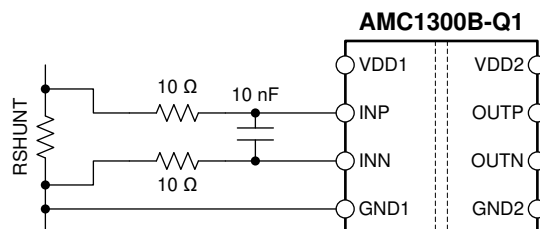


图 8-2. Differential Input Filter

8.2.2.3 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLVx313-Q1-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With $R1 = R2 = R3 = R4$, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, $R1 = R2 = R3 = R4 = 3.3\text{ k}\Omega$ and $C1 = C2 = 330\text{ pF}$ yields good performance.

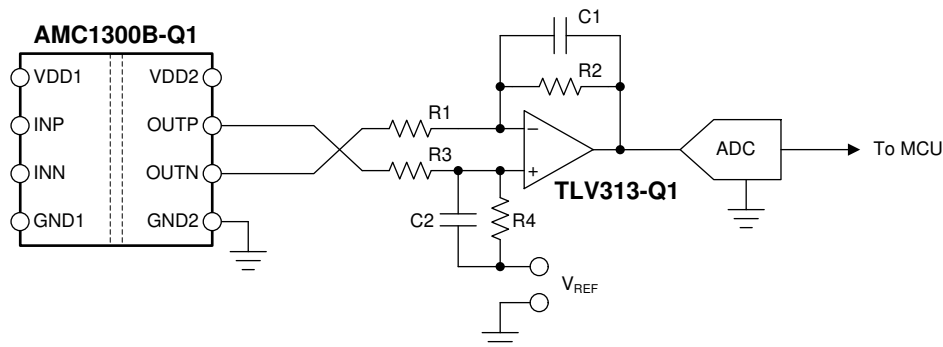


Figure 8-3. Connecting the AMC1300B-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power](#) reference guides, available for download at www.ti.com.

8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1300B-Q1.

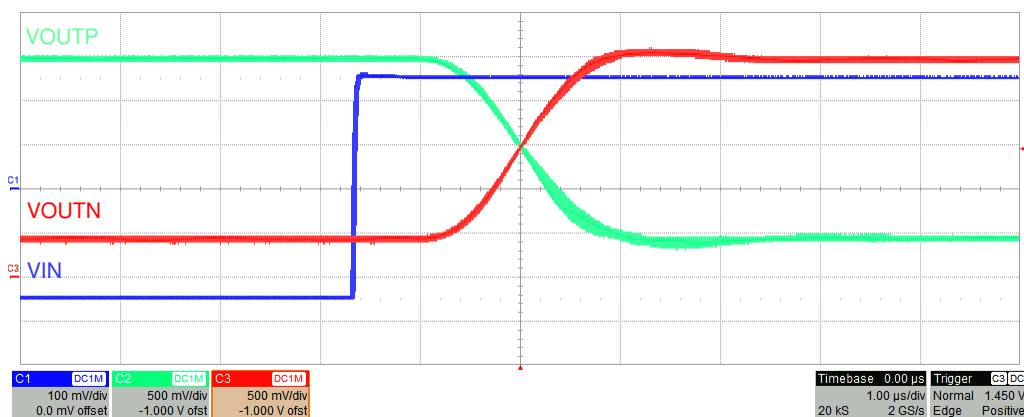


Figure 8-4. Step Response of the AMC1300B-Q1

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1300B-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the device outputs the fail-safe voltage as described in the [Analog Output](#) section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the [Layout](#) section for more details.

9 Power Supply Recommendations

The AMC1300B-Q1 does not require any specific power up sequencing. The high-side power-supply (VDD1) is decoupled with a low-ESR 100-nF capacitor (C1) parallel to a low-ESR 1-μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR 100-nF capacitor (C3) parallel to a low-ESR 1-μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in [Figure 9-1](#)) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.

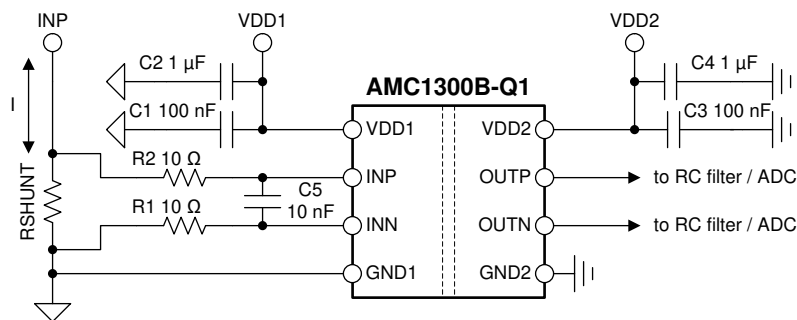


Figure 9-1. Decoupling of the AMC1300B-Q1

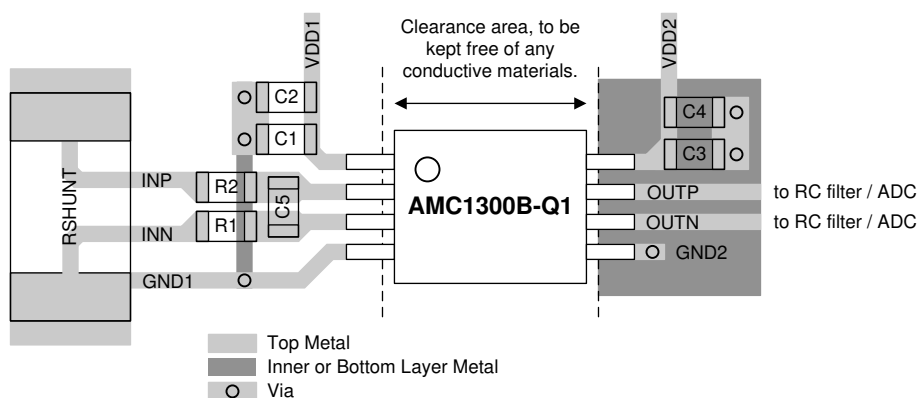
Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

10 Layout

10.1 Layout Guidelines

☒ 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300B-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300B-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example



☒ 10-1. Recommended Layout of the AMC1300B-Q1

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application report](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application report](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application report](#)
- Texas Instruments, [TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems data sheet](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1300BQDWVRQ1	Active	Production	SOIC (DWV) 8	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MC1300BQ
AMC1300BQDWVRQ1.A	Active	Production	SOIC (DWV) 8	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MC1300BQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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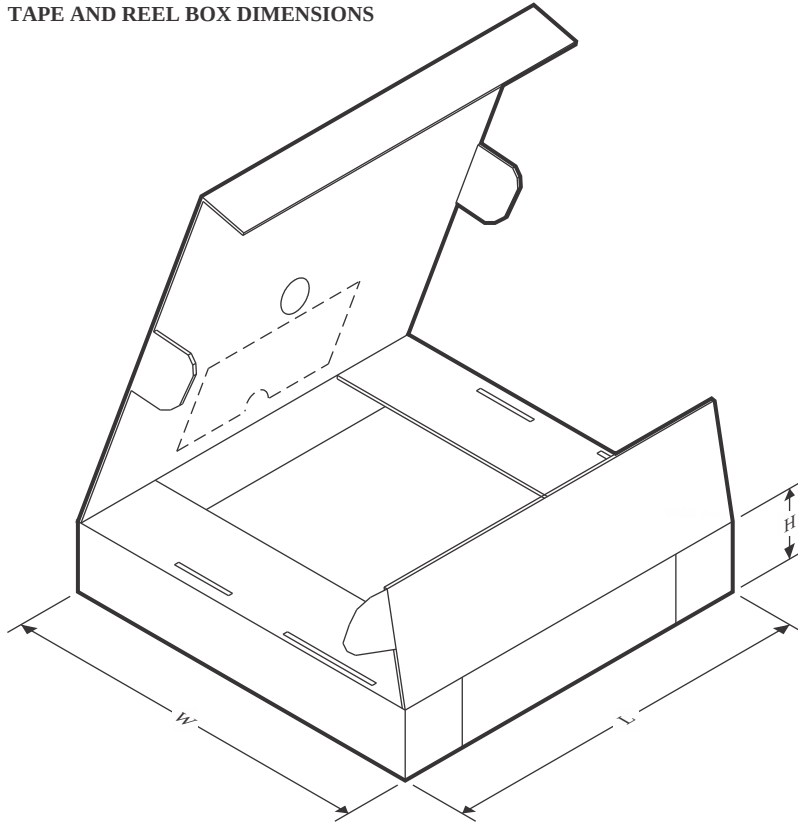
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1300BQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



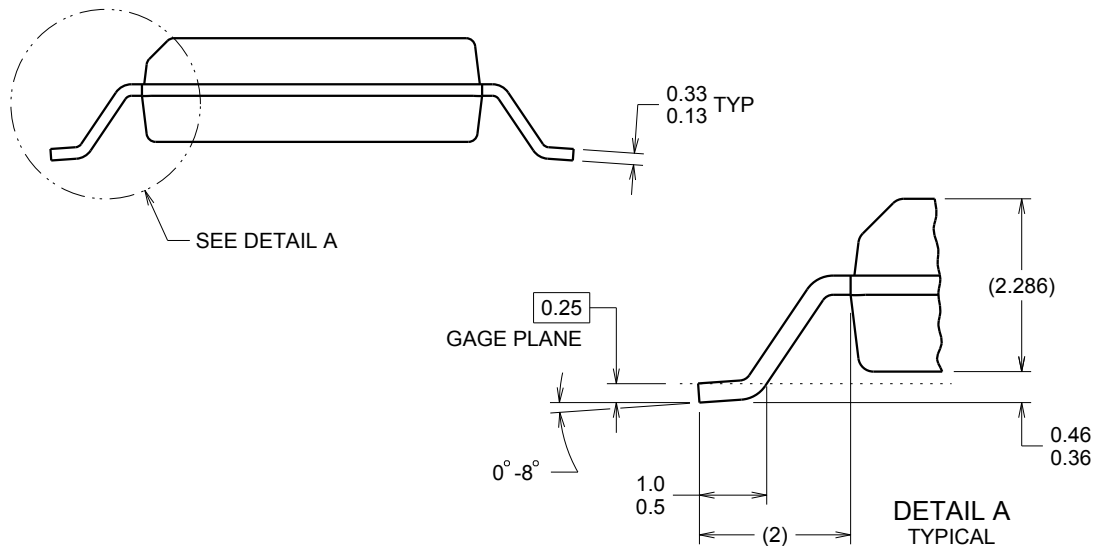
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1300BQDWVRQ1	SOIC	DWV	8	1000	353.0	353.0	32.0

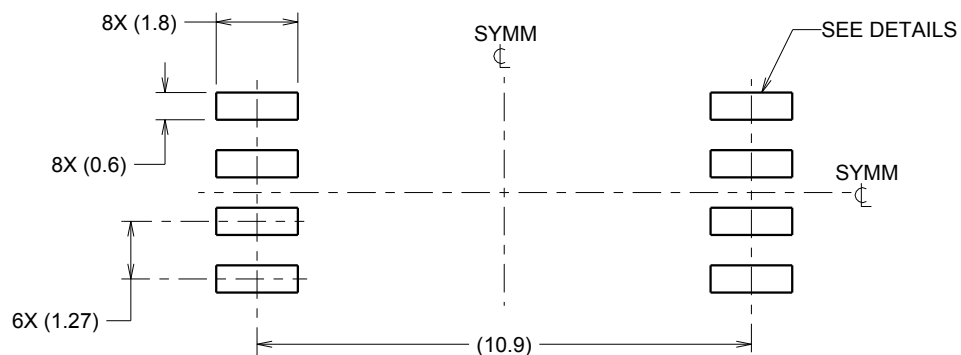
SOIC - 2.8 mm max height

The drawing shows a 16-pin connector with the following specifications:

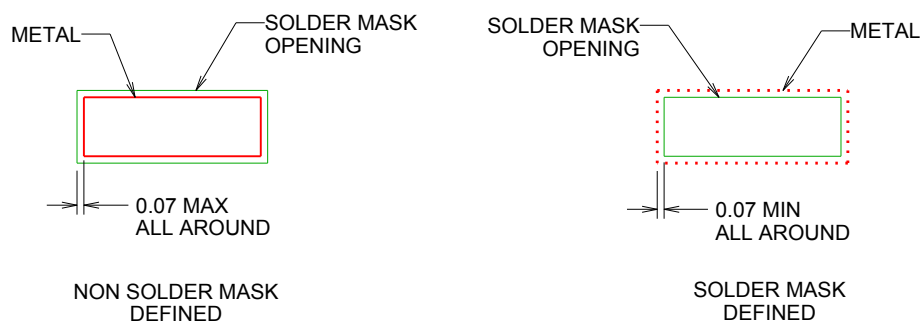
- Top View:**
 - Overall width: 11.5 ± 0.25 TYP
 - Overall height: 5.95 to 5.75 (NOTE 3)
 - Pin 1 ID Area: Indicated by a circle and arrow.
 - Pin pitch: 2.54 (implied by 16 pins in 4 rows).
 - Pin 1 location: 7.6 from the left edge, 7.4 from the bottom edge (NOTE 4).
 - Pin 16 location: 6×1.27 from the right edge.
 - Pin 17 location: 2×3.81 from the bottom edge.
 - Pin 18 location: 8×0.51 to 0.31 from the bottom edge.
- Side View:**
 - Seating Plane: Indicated by a horizontal line.
 - Pin height: 2.8 MAX.
- Detail View:**
 - Feature: 0.25 (M)
 - Feature: C (A)
 - Feature: B (S)



1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

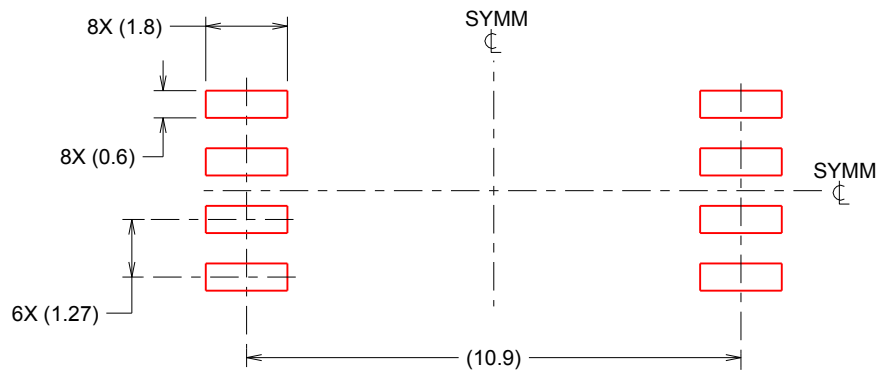


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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