

# AMC1400-Q1 車載用、高精度、 $\pm 250\text{mV}$ 入力、強化絶縁型アンプ

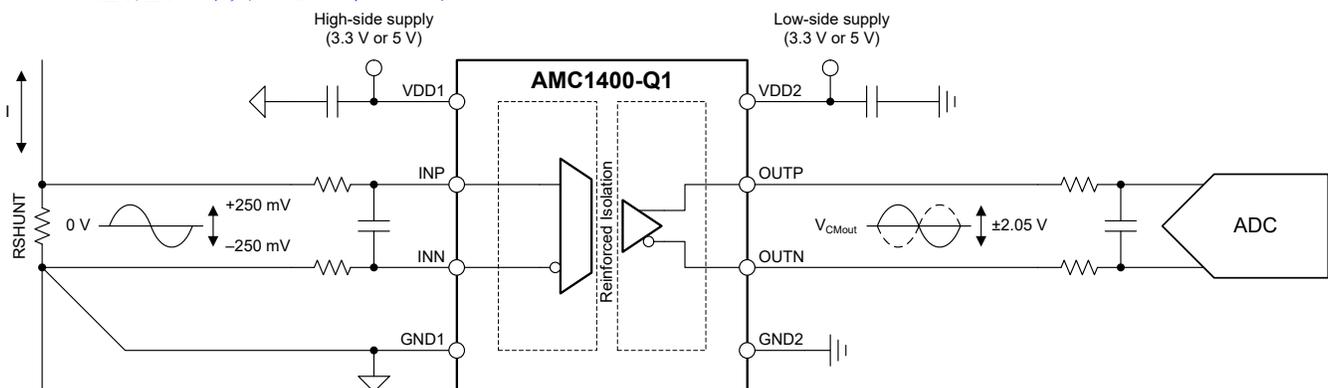
## 15mm ストレッチ SOIC パッケージ

### 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ 、 $T_A$
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- シャント抵抗を用いた電流測定用に最適化された  $\pm 250\text{mV}$  の入力電圧範囲
- 固定ゲイン: 8.2V/V
- 小さな DC 誤差:
  - オフセット誤差:  $\pm 0.2\text{mV}$  (最大値)
  - オフセット・ドリフト:  $\pm 0.9\mu\text{V}/^{\circ}\text{C}$  (最大値)
  - ゲイン誤差:  $\pm 0.3\%$  (最大値)
  - ゲイン・ドリフト:  $\pm 30\text{ppm}/^{\circ}\text{C}$  (最大値)
  - 非線形性: 0.03% (最大値)
- ハイサイド、ローサイドとも 3.3V または 5V で動作可能
- ハイサイド電源喪失の検出機能
- 高 CMTI:  $100\text{kV}/\mu\text{s}$  (最小値)
- 低 EMI、CISPR-11 および CISPR-25 規格に準拠
- 安全関連の認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:  $10600\text{V}_{\text{PK}}$
  - UL 1577 に準拠した絶縁耐圧:  $7500\text{V}_{\text{RMS}}$  (1 分間)

### 2 アプリケーション

- 次のような機器で使用するシャント抵抗方式電流センシング:
  - HEV/EV 充電パイル
  - HEV/EV のオンボード充電器 (OBC)
  - HEV/EV の DC/DC コンバータ
  - HEV/EV のトラクション・インバータ



代表的なアプリケーション

### 3 概要

AMC1400-Q1 は高精度の絶縁型アンプで、磁気干渉に対して高い耐性のある絶縁バリアにより、入力側と出力側の回路が分離されています。このバリアは、DIN EN IEC 60747-17 (VDE 0884-17) および UL1577 規格に従って最大  $7.5\text{kV}_{\text{RMS}}$  の強化絶縁を達成していることが認証され、最大  $2\text{kV}_{\text{RMS}}$  の使用電圧に対応しています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離し、電氣的損傷を生じさせる可能性がある電圧やオペレータに害を及ぼす可能性がある電圧から低電圧側を保護します。

AMC1400-Q1 の入力は、低インピーダンスのシャント抵抗またはその他の信号レベルが小さい低インピーダンス電圧源と直接接続できるように最適化されています。優れた DC 精度と小さい温度ドリフトにより、高い同相電圧、高い標高、または汚染度の高い環境で動作する必要がある力率補正 (PFC) 段、DC/DC コンバータ、トラクション・インバータ、その他のアプリケーションの高精度電流制御に対応できます。

AMC1400-Q1 は、ストレッチ 8 ピン SOIC パッケージで供給され、車載用アプリケーション向けに AEC-Q100 認定済みであり、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  の温度範囲に対応しています。

#### パッケージ情報<sup>(1)</sup>

部品番号	パッケージ	本体サイズ (公称)
AMC1400-Q1	SOIC (8)	6.40mm × 14.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	7.1 Overview.....	<b>17</b>
<b>2 アプリケーション</b> .....	<b>1</b>	7.2 Functional Block Diagram.....	<b>17</b>
<b>3 概要</b> .....	<b>1</b>	7.3 Feature Description.....	<b>17</b>
<b>4 Revision History</b> .....	<b>2</b>	7.4 Device Functional Modes.....	<b>19</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>8 Application and Implementation</b> .....	<b>20</b>
<b>6 Specifications</b> .....	<b>4</b>	8.1 Application Information.....	<b>20</b>
6.1 Absolute Maximum Ratings.....	<b>4</b>	8.2 Typical Application.....	<b>20</b>
6.2 ESD Ratings.....	<b>4</b>	8.3 Best Design Practices.....	<b>25</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	8.4 Power Supply Recommendations.....	<b>26</b>
6.4 Thermal Information.....	<b>5</b>	8.5 Layout.....	<b>27</b>
6.5 Power Ratings.....	<b>5</b>	<b>9 Device and Documentation Support</b> .....	<b>28</b>
6.6 Insulation Specifications.....	<b>6</b>	9.1 Documentation Support.....	<b>28</b>
6.7 Safety-Related Certifications.....	<b>7</b>	9.2 Receiving Notification of Documentation Updates... <b>28</b>	
6.8 Safety Limiting Values.....	<b>7</b>	9.3 サポート・リソース.....	<b>28</b>
6.9 Electrical Characteristics.....	<b>8</b>	9.4 Trademarks.....	<b>28</b>
6.10 Switching Characteristics.....	<b>9</b>	9.5 Electrostatic Discharge Caution.....	<b>28</b>
6.11 Timing Diagram.....	<b>9</b>	9.6 Glossary.....	<b>28</b>
6.12 Insulation Characteristics Curves.....	<b>10</b>	<b>10 Mechanical, Packaging, and Orderable          Information</b> .....	<b>28</b>
6.13 Typical Characteristics.....	<b>11</b>		
<b>7 Detailed Description</b> .....	<b>17</b>		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2022	*	Initial Release

## 5 Pin Configuration and Functions

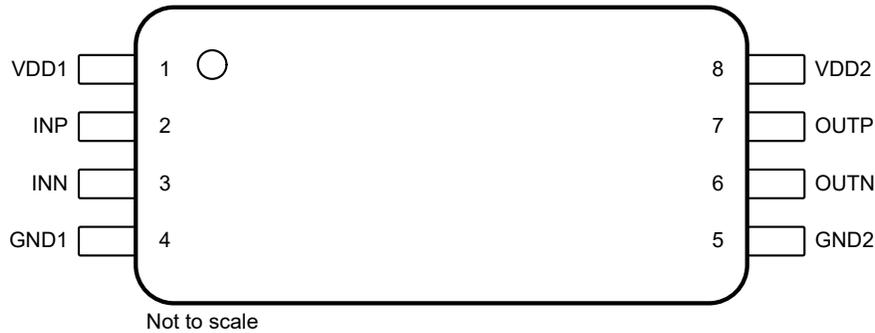


图 5-1. DWL Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply. <sup>(1)</sup>
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. <sup>(2)</sup>
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage. <sup>(2)</sup>
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply. <sup>(1)</sup>

(1) See the [Power Supply Recommendations](#) section for power-supply decoupling recommendations.

(2) See the [Layout](#) section for details.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	-0.3	6.5	V
	Low-side VDD2 to GND2	-0.3	6.5	
Analog input voltage	INP, INN	GND1 - 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 - 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> , HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>						
	High-side power supply	VDD1 to GND1	3	5	5.5	V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
<b>ANALOG INPUT</b>						
V <sub>Clipping</sub>	Differential input voltage before clipping output	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>	±320			mV
V <sub>FSR</sub>	Specified linear differential full-scale voltage	V <sub>IN</sub> = V <sub>INP</sub> - V <sub>INN</sub>	-250		250	mV
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to GND1	-0.16		VDD1 - 2.1	V
<b>ANALOG OUTPUT</b>						
C <sub>LOAD</sub>	Capacitive load	On OUTP or OUTN to GND2			500	pF
C <sub>LOAD</sub>	Capacitive load	OUTP to OUTN			250	pF
R <sub>LOAD</sub>	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Specified ambient temperature		-40	25	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DWL (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$P_D$	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
$P_{D1}$	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
		VDD1 = 5.5 V	54	
$P_{D2}$	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
		VDD2 = 5.5 V	45	

## 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>				
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 14.7	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 15.7	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
<b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	2800	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum-rated isolation working voltage	At AC voltage (sine wave)	2000	V <sub>RMS</sub>
		At DC voltage	2800	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	10600	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	12720	
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50-μs waveform per IEC 62368-1	9800	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a, after input/output safety test subgroups 2 and 3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s, V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s, V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1 MHz	~1.5	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
<b>UL1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 7500 V <sub>RMS</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 9000 V <sub>RMS</sub> , t = 1 s (100% production test)	7500	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier are tied together, creating a two-pin device.

## 6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: 40040142 (pending)	File number: E181974

## 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 63.2°C/W, VDDx = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			550	mA
		R <sub>θJA</sub> = 63.2°C/W, VDDx = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			360	
P <sub>S</sub>	Safety input, output, or total power	R <sub>θJA</sub> = 63.2°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1980	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$ , where VDD<sub>max</sub> is the maximum supply voltage for high-side and low-side.

## 6.9 Electrical Characteristics

minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $I_{NP} = -250\text{ mV}$  to  $+250\text{ mV}$ , and  $I_{NN} = \text{GND1}$ ; typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>ANALOG INPUT</b>						
$V_{OS}$	Input offset voltage <sup>(1) (2)</sup>	$T_A = 25^\circ\text{C}$ , $I_{NP} = I_{NN} = \text{GND1}$		-0.2	$\pm 0.01$ 0.2	mV
$TCV_{OS}$	Input offset drift <sup>(1) (2) (4)</sup>			-0.9	$\pm 0.1$ 0.9	$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$f_{IN} = 0\text{ Hz}$ , $V_{CM\ min} \leq V_{CM} \leq V_{CM\ max}$		-100		dB
		$f_{IN} = 10\text{ kHz}$ , $V_{CM\ min} \leq V_{CM} \leq V_{CM\ max}$		-98		
$R_{IN}$	Single-ended input resistance	$I_{NN} = \text{GND1}$		19		k $\Omega$
$R_{IND}$	Differential input resistance			22		k $\Omega$
$I_{IB}$	Input bias current	$I_{NP} = I_{NN} = \text{GND1}$ ; $I_{IB} = (I_{IBP} + I_{IBN}) / 2$		-41	-30 -24	$\mu\text{A}$
$I_{IO}$	Input offset current	$I_{IO} = I_{IBP} - I_{IBN}$ ; $I_{NP} = I_{NN} = \text{GND1}$		$\pm 5$		nA
$C_{IN}$	Single-ended input capacitance	$I_{NN} = \text{GND1}$ , $f_{IN} = 275\text{ kHz}$		2		pF
$C_{IND}$	Differential input capacitance	$f_{IN} = 275\text{ kHz}$		1		pF
<b>ANALOG OUTPUT</b>						
	Nominal gain			8.2		V/V
$E_G$	Gain error <sup>(1)</sup>	$T_A = 25^\circ\text{C}$		-0.3%	$\pm 0.04\%$ 0.3%	
$TCE_G$	Gain drift <sup>(1) (5)</sup>			-30	$\pm 5$ 30	ppm/ $^\circ\text{C}$
	Nonlinearity <sup>(1)</sup>			-0.03%	$\pm 0.01\%$ 0.03%	
THD	Total harmonic distortion <sup>(3)</sup>	$f_{IN} = 10\text{ kHz}$		-85		dB
	Output noise	$I_{NP} = I_{NN} = \text{GND1}$ , $f_{IN} = 0\text{ Hz}$ , BW = 100 kHz brickwall filter		230		$\mu\text{V}_{RMS}$
SNR	Signal-to-noise ratio	$f_{IN} = 1\text{ kHz}$ , BW = 10 kHz		81.5	85	dB
		$f_{IN} = 10\text{ kHz}$ , BW = 100 kHz		72		
PSRR	Power-supply rejection ratio <sup>(2)</sup>	PSRR vs $V_{DD1}$ , at DC		-100		dB
		PSRR vs $V_{DD1}$ , 100-mV and 10-kHz ripple		-96		
		PSRR vs $V_{DD2}$ , at DC		-106		
		PSRR vs $V_{DD2}$ , 100-mV and 10-kHz ripple		-86		
$V_{CMout}$	Common-mode output voltage			1.39	1.44 1.49	V
$V_{CLIPout}$	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} - V_{OUTN})$ ; $ V_{IN}  =  V_{INP} - V_{INN}  >  V_{Clipping} $		-2.52	$\pm 2.49$ 2.52	V
$V_{Failsafe}$	Failsafe differential output voltage	$V_{DD1}$ missing		-2.63	-2.57 -2.53	V
BW	Output bandwidth			250	310	kHz
$R_{OUT}$	Output resistance	On $O_{UTP}$ or $O_{UTN}$		< 0.2		$\Omega$
	Output short-circuit current	On $O_{UTP}$ or $O_{UTN}$ , sourcing or sinking, $I_{NN} = \text{GND1}$ , outputs shorted to either $\text{GND2}$ or $V_{DD2}$		14		mA
CMTI	Common-mode transient immunity			100	150	kV/ $\mu\text{s}$

### 6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD1} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{DD2} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $\text{INP} = -250\text{ mV}$  to  $+250\text{ mV}$ , and  $\text{INN} = \text{GND1}$ ; typical specifications are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
VDD1 <sub>UV</sub>	VDD1 undervoltage detection threshold	VDD1 rising	2.5	2.7	2.9	V
		VDD1 falling	2.4	2.6	2.8	
VDD2 <sub>UV</sub>	VDD2 undervoltage detection threshold	VDD2 rising	2.2	2.45	2.65	V
		VDD2 falling	1.85	2.0	2.2	
IDD1	High-side supply current	$3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$		6.3	8.5	mA
		$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$		7.2	9.8	
IDD2	Low-side supply current	$3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$		5.3	7.2	mA
		$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$		5.9	8.1	

- (1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:  

$$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$$
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:  

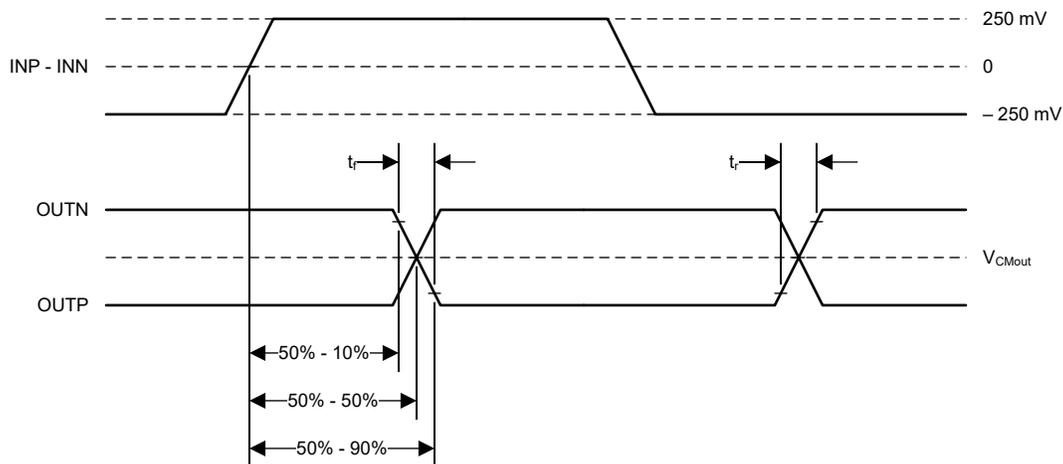
$$TCE_G (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25^{\circ}\text{C})} \times TempRange) \times 10^6$$

### 6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

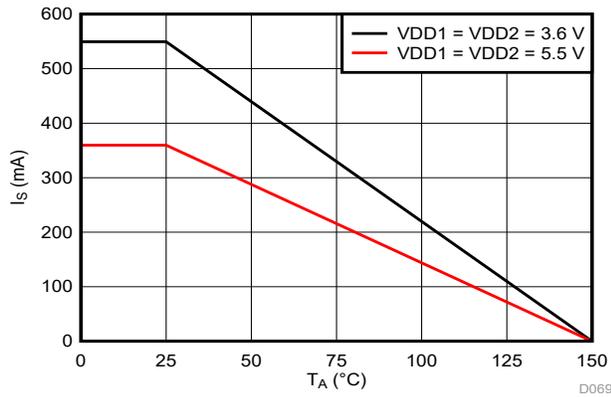
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output signal rise time			1.3		$\mu\text{s}$
$t_f$	Output signal fall time			1.3		$\mu\text{s}$
	$V_{INx}$ to $V_{OUTx}$ signal delay (50% - 10%)	Unfiltered output		1	1.5	$\mu\text{s}$
	$V_{INx}$ to $V_{OUTx}$ signal delay (50% - 50%)	Unfiltered output		1.6	2.1	$\mu\text{s}$
	$V_{INx}$ to $V_{OUTx}$ signal delay (50% - 90%)	Unfiltered output		2.5	3	$\mu\text{s}$
$t_{AS}$	Analog settling time	VDD1 step to 3.0 V with $V_{DD2} \geq 3.0\text{ V}$ , to $V_{OUTP}$ , $V_{OUTN}$ valid, 0.1% settling		500		$\mu\text{s}$

### 6.11 Timing Diagram

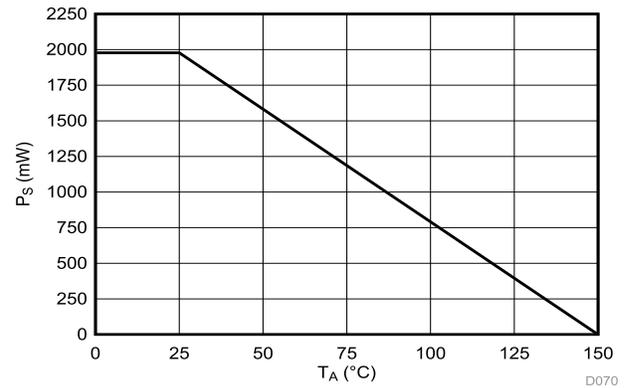


**6-1. Rise, Fall, and Delay Time Definition**

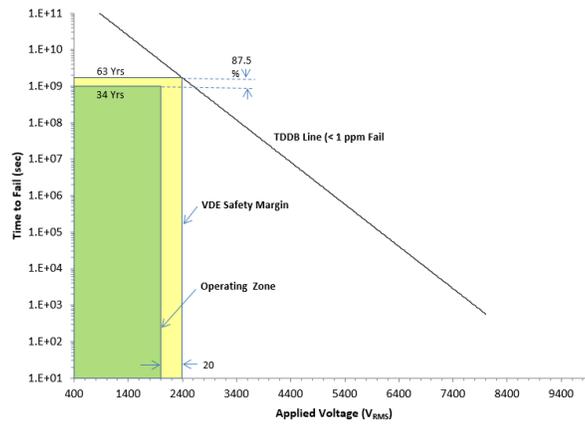
## 6.12 Insulation Characteristics Curves



**6-2. Thermal Derating Curve for Safety-Limiting Current per VDE**



**6-3. Thermal Derating Curve for Safety-Limiting Power per VDE**



$T_A$  up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 2000  $V_{RMS}$ , operating lifetime = 34 year

**6-4. Reinforced Isolation Capacitor Lifetime Projection**

### 6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)

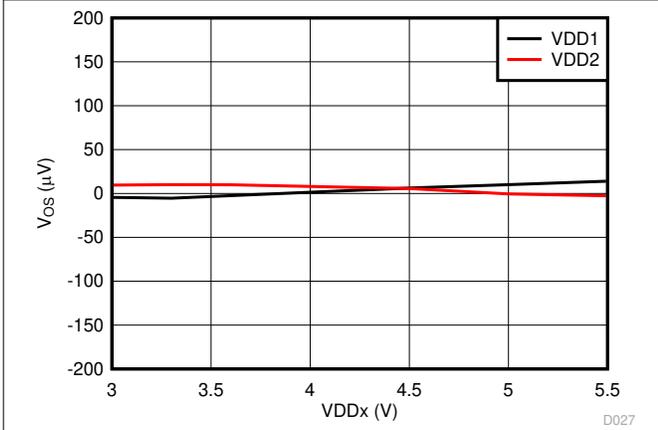


Figure 6-5. Input Offset Voltage vs Supply Voltage

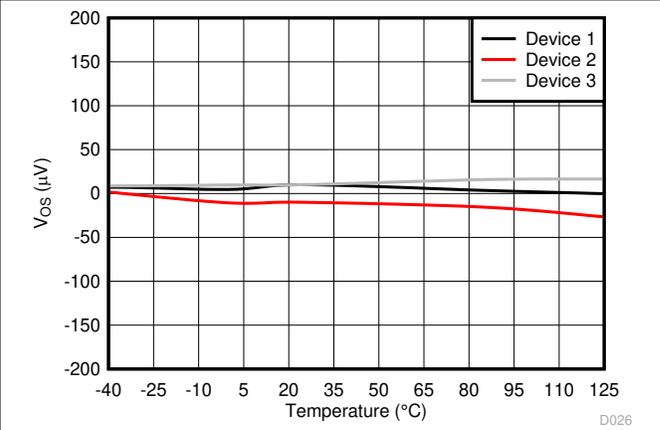


Figure 6-6. Input Offset Voltage vs Temperature

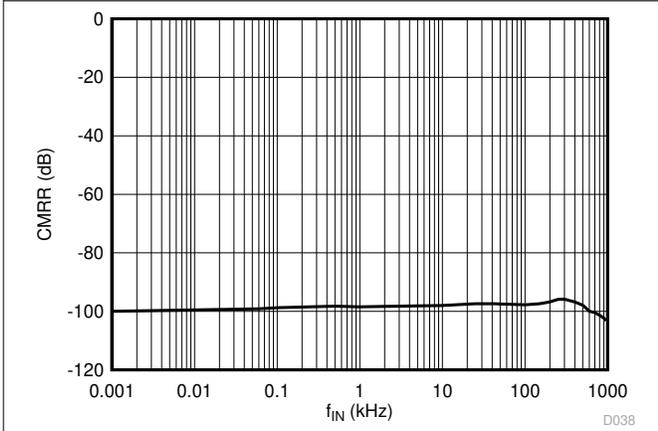


Figure 6-7. Common-Mode Rejection Ratio vs Input Frequency

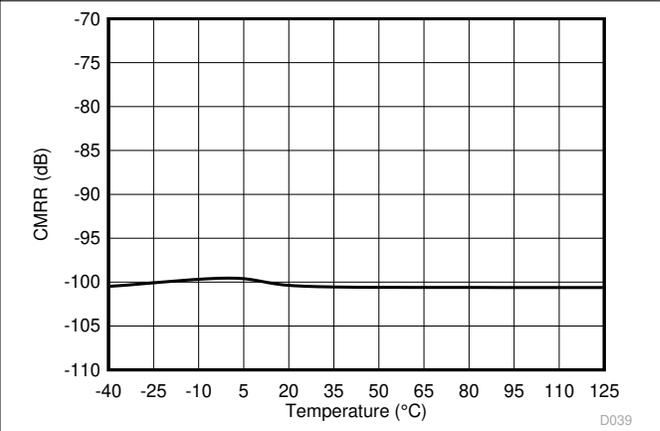


Figure 6-8. Common-Mode Rejection Ratio vs Temperature

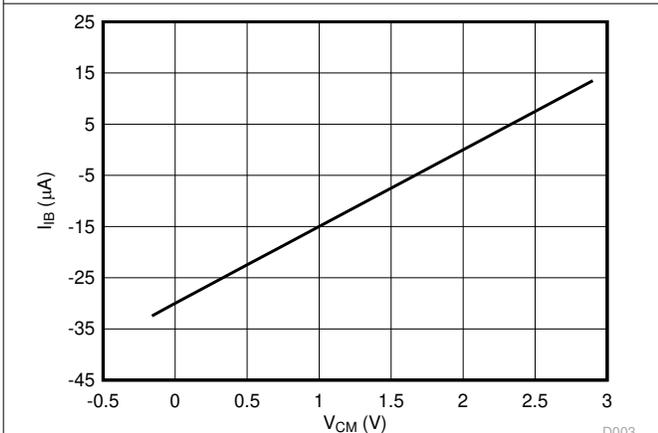


Figure 6-9. Input Bias Current vs Common-Mode Input Voltage

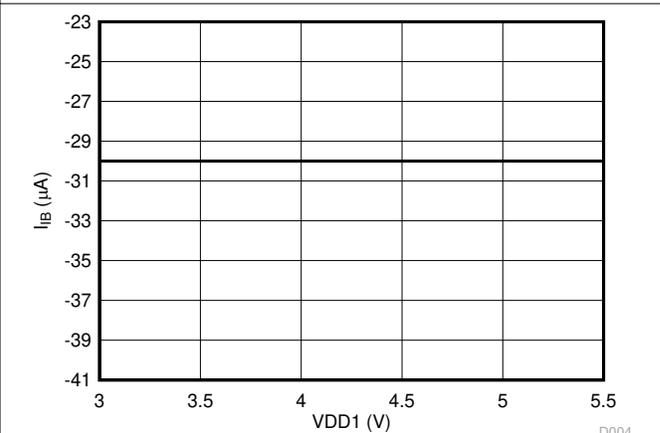
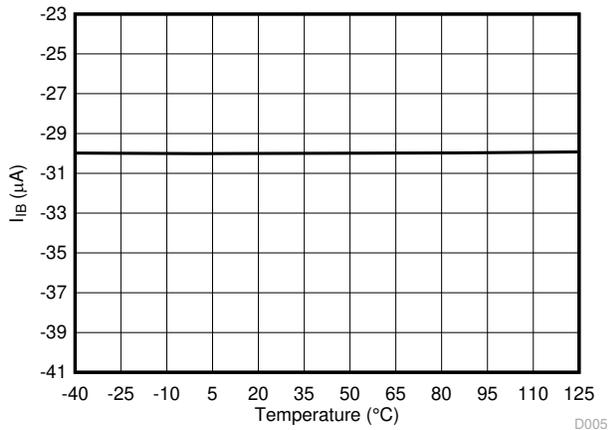


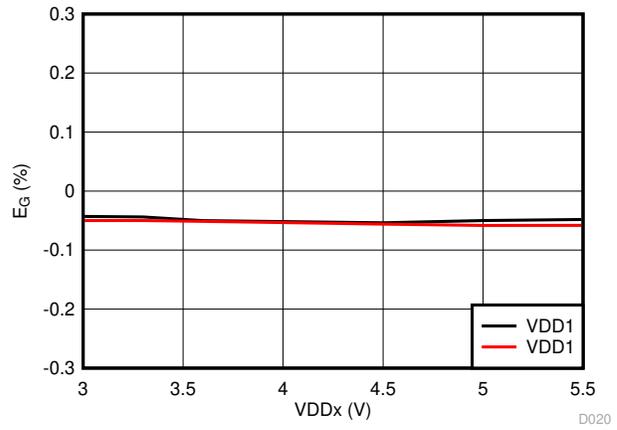
Figure 6-10. Input Bias Current vs High-Side Supply Voltage

### 6.13 Typical Characteristics (continued)

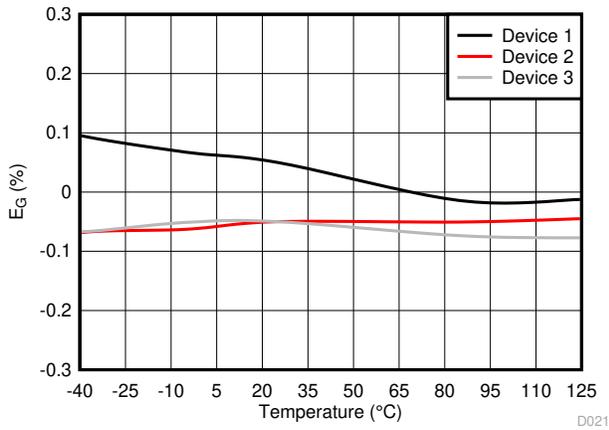
at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)



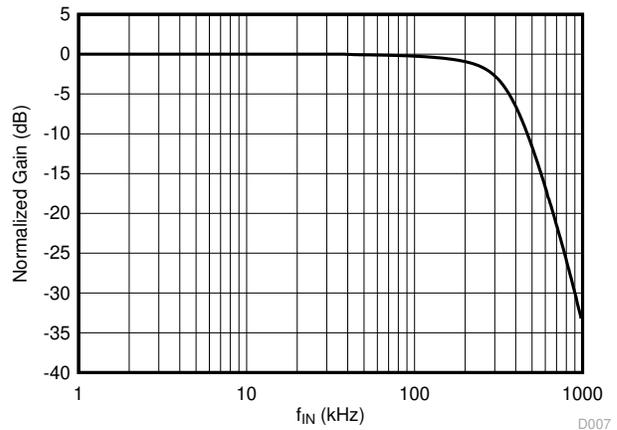
6-11. Input Bias Current vs Temperature



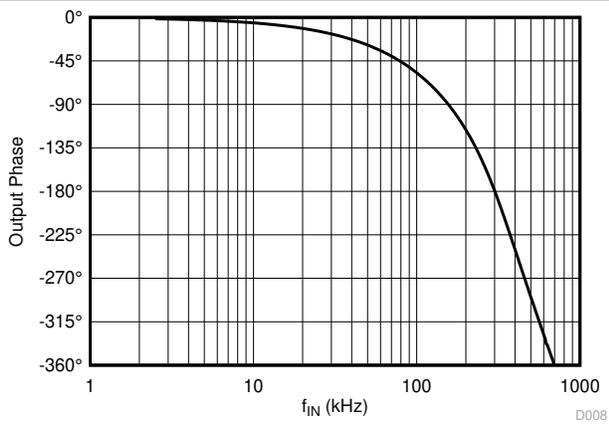
6-12. Gain Error vs Supply Voltage



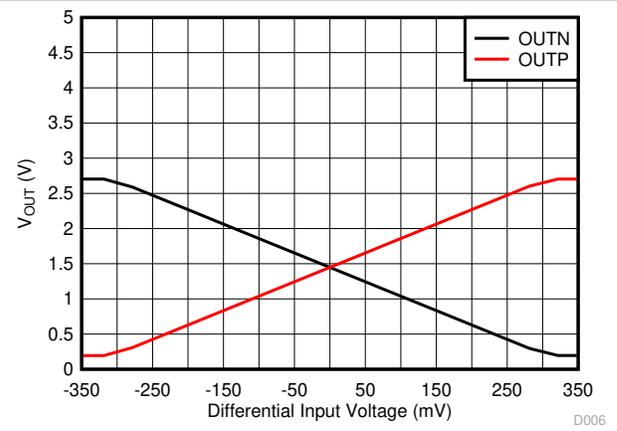
6-13. Gain Error vs Temperature



6-14. Normalized Gain vs Input Frequency



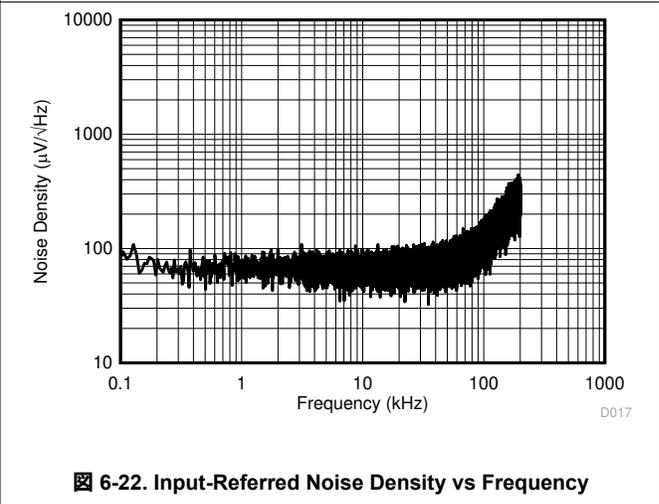
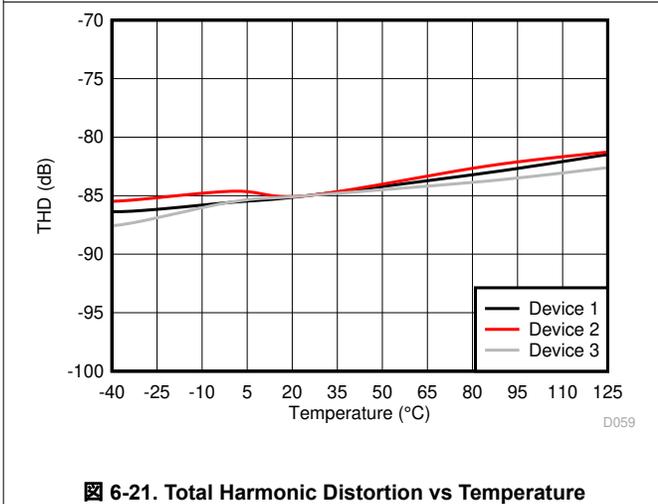
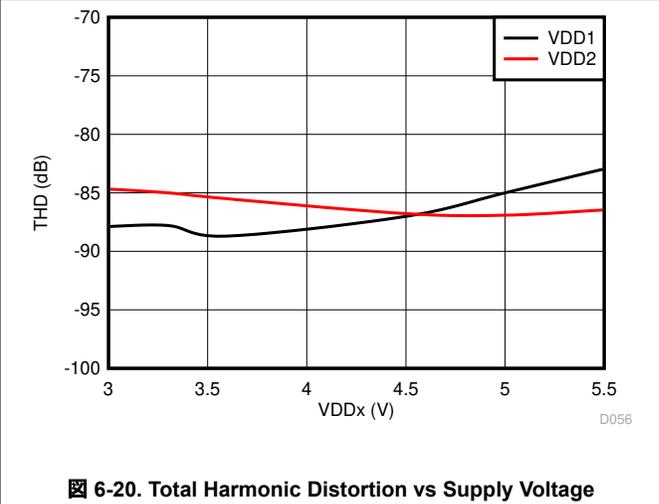
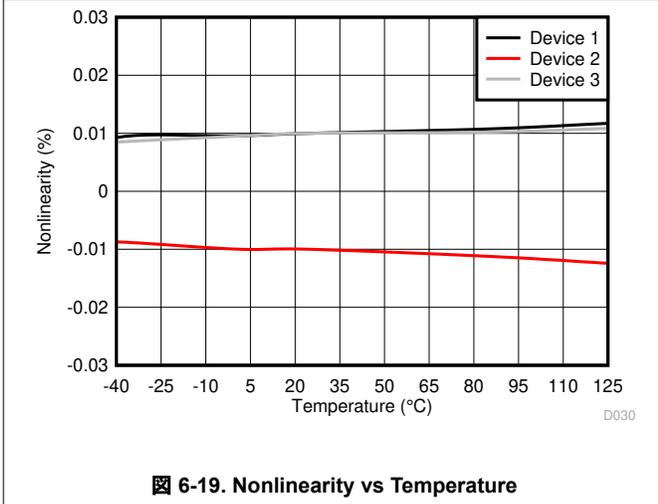
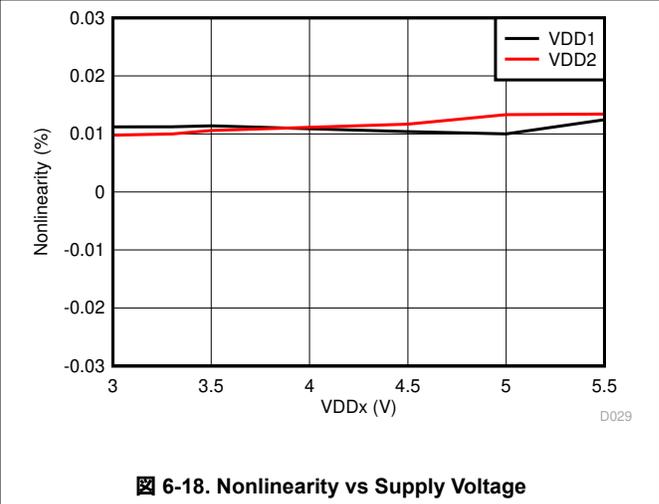
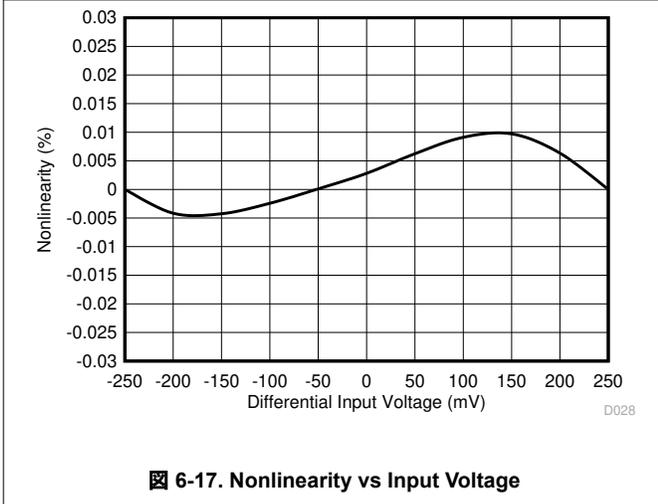
6-15. Output Phase vs Input Frequency



6-16. Output Voltage vs Input Voltage

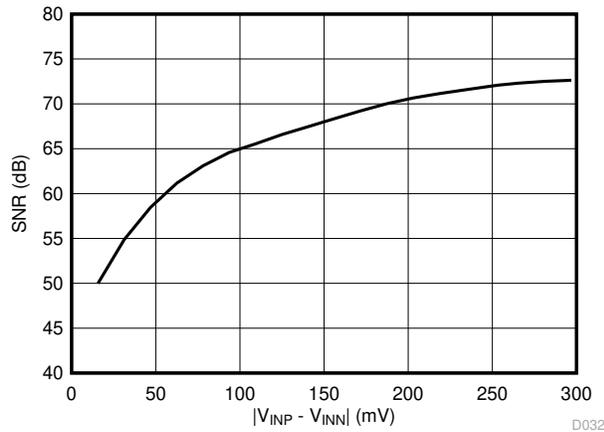
### 6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)

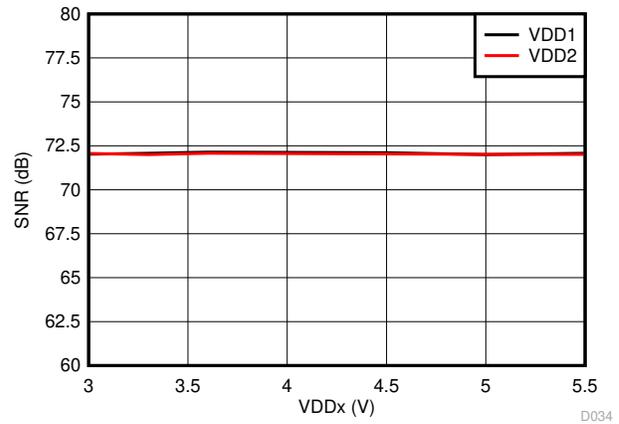


### 6.13 Typical Characteristics (continued)

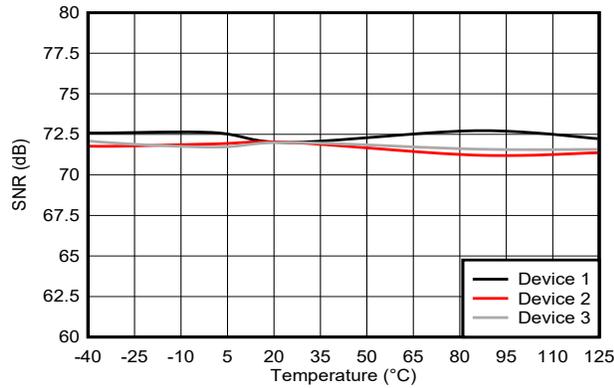
at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)



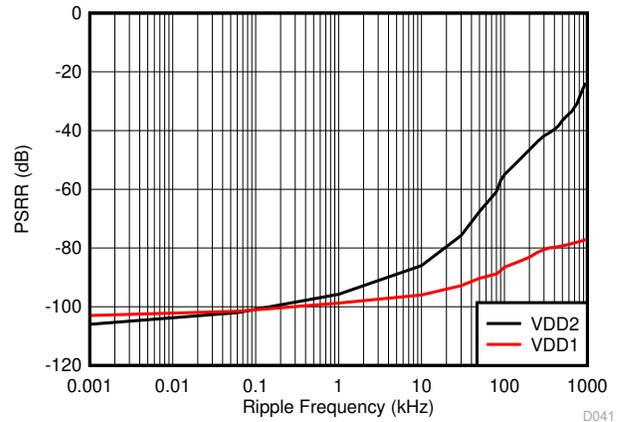
6-23. Signal-to-Noise Ratio vs Input Voltage



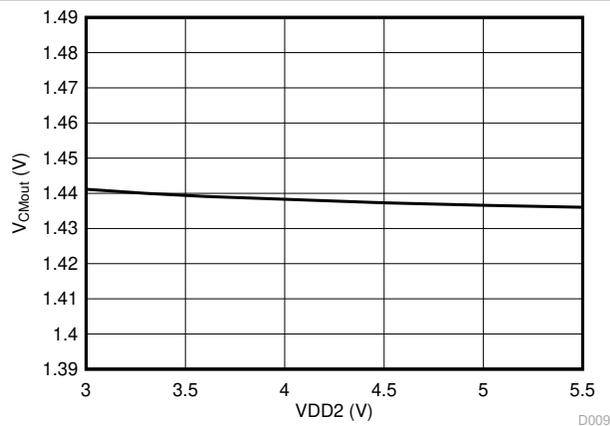
6-24. Signal-to-Noise Ratio vs Supply Voltage



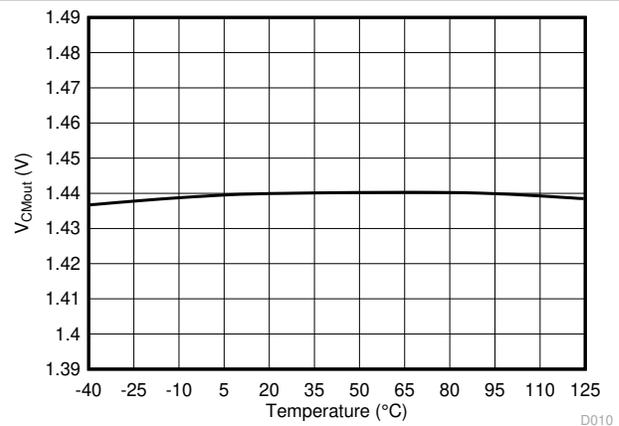
6-25. Signal-to-Noise Ratio vs Temperature



6-26. Power-Supply Rejection Ratio vs Ripple Frequency



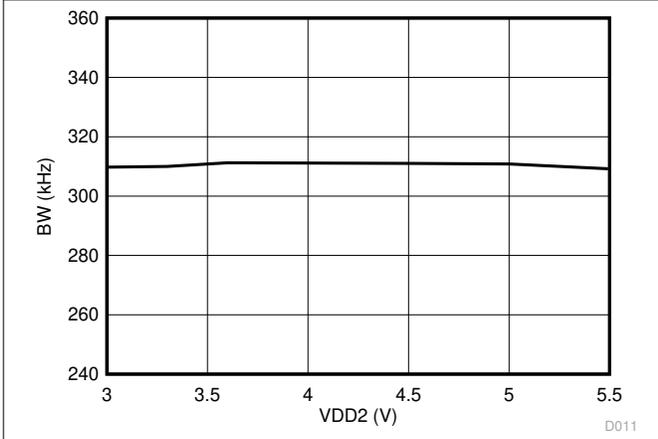
6-27. Output Common-Mode Voltage vs Low-Side Supply Voltage



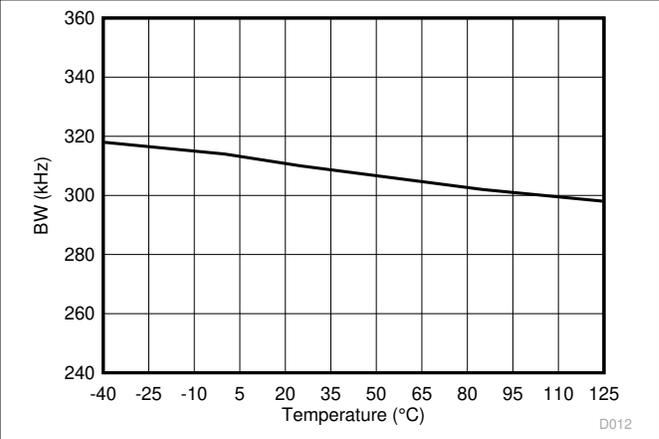
6-28. Output Common-Mode Voltage vs Temperature

### 6.13 Typical Characteristics (continued)

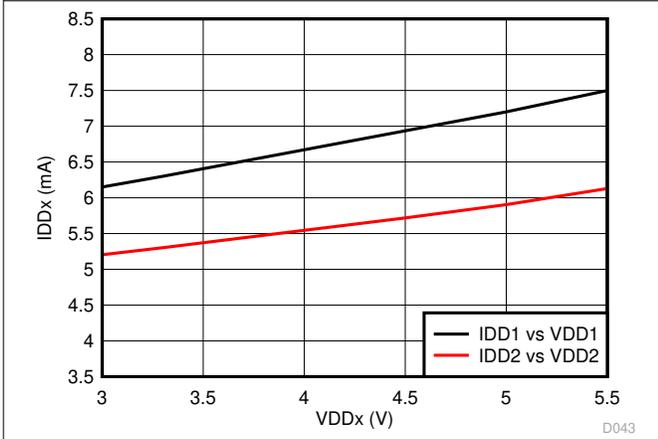
at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)



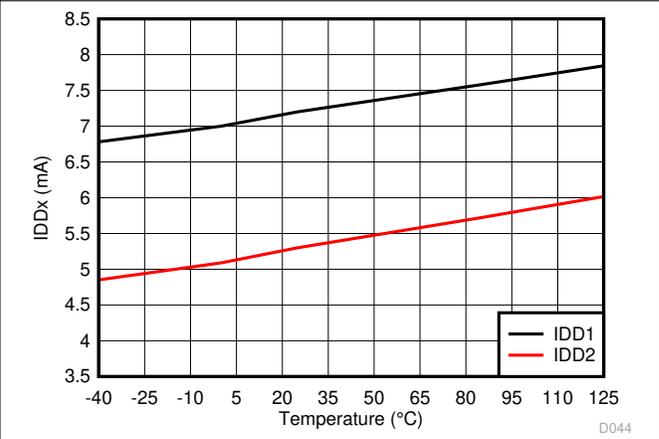
6-29. Output Bandwidth vs Low-Side Supply Voltage



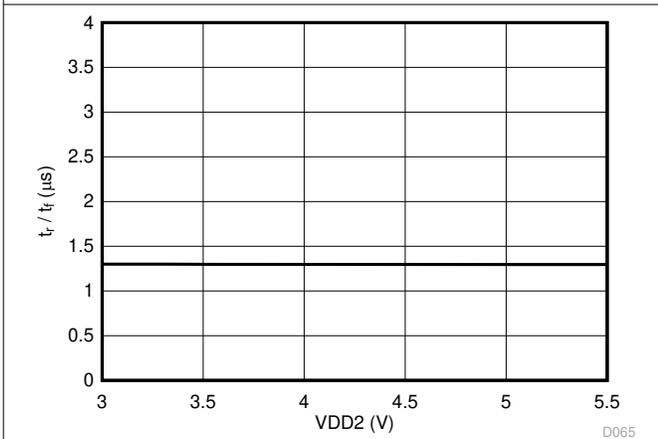
6-30. Output Bandwidth vs Temperature



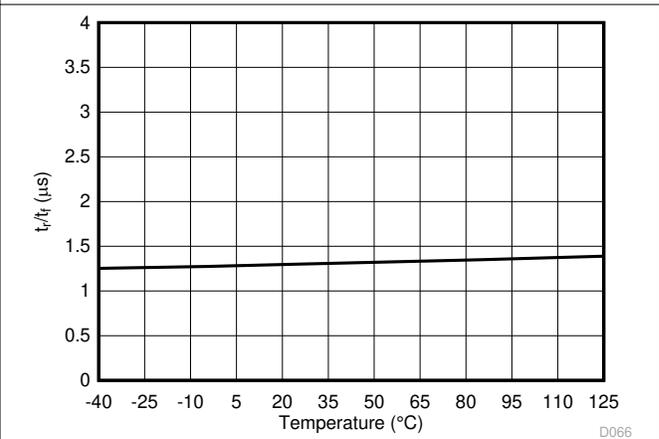
6-31. Supply Current vs Supply Voltage



6-32. Supply Current vs Temperature



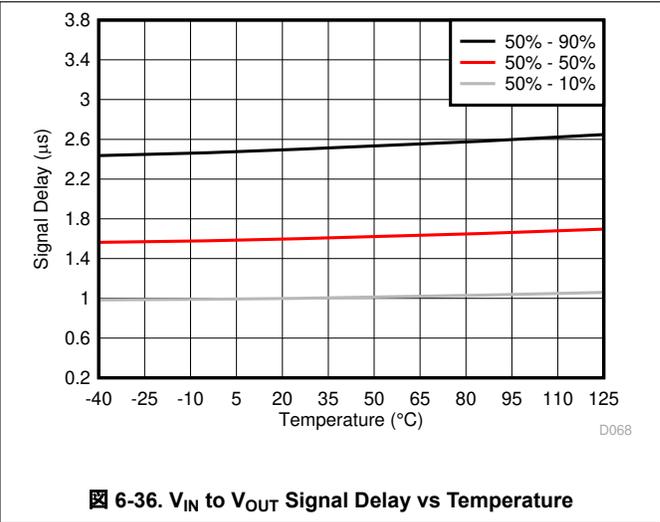
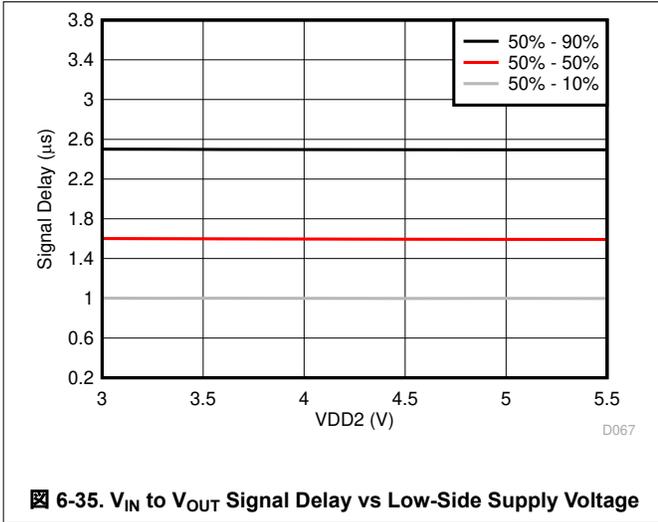
6-33. Output Rise and Fall Time vs Low-Side Supply



6-34. Output Rise and Fall Time vs Temperature

### 6.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN} = 10$  kHz (unless otherwise noted)



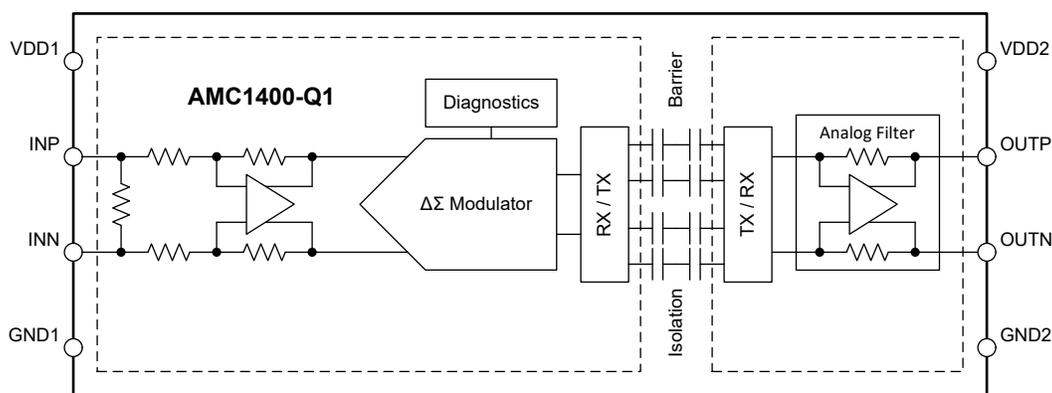
## 7 Detailed Description

### 7.1 Overview

The AMC1400-Q1 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUP and OUTN pins that is proportional to the input signal.

The SiO<sub>2</sub>-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the [ISO72x Digital Isolator Magnetic-Field Immunity application report](#). The digital modulation used in the AMC1400-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Analog Input

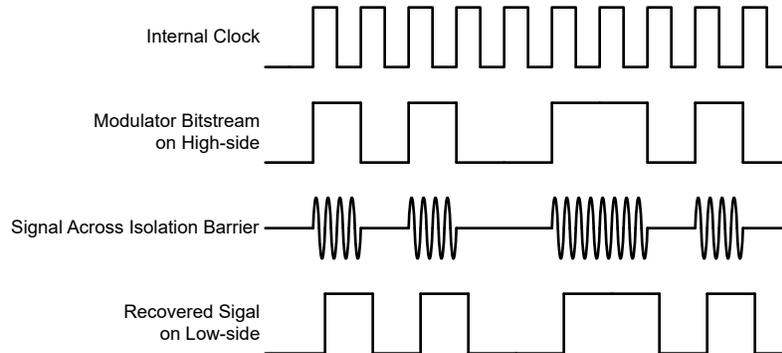
The differential amplifier input stage of the AMC1400-Q1 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of  $R_{IND}$ . The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the [Isolation Channel Signal Transmission](#) section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages  $V_{INP}$  or  $V_{INN}$  exceed the range specified in the [Absolute Maximum Ratings](#) table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range ( $V_{FSR}$ ) and within the common-mode input voltage range ( $V_{CM}$ ), as specified in the [Recommended Operating Conditions](#) table.

### 7.3.2 Isolation Channel Signal Transmission

The AMC1400-Q1 uses an on-off keying (OOK) modulation scheme, as shown in [Figure 7-1](#), to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the [Functional Block Diagram](#) transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1400-Q1 is 480 MHz.

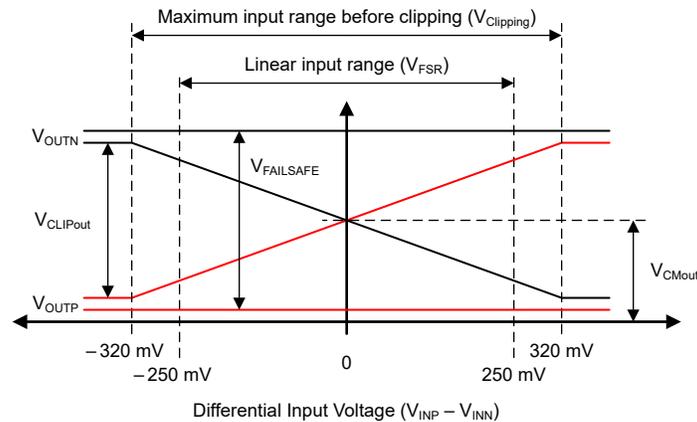
The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1400-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.



**Figure 7-1. OOK-Based Modulation Scheme**

### 7.3.3 Analog Output

The AMC1400-Q1 offers a differential analog output comprised of the OOUTP and OOUTN pins. For differential input voltages ( $V_{INP} - V_{INN}$ ) in the range from  $-250\text{ mV}$  to  $+250\text{ mV}$ , the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of  $250\text{ mV}$ , the differential output voltage ( $V_{OOUTP} - V_{OOUTN}$ ) is  $2.05\text{ V}$ . At zero input (INP shorted to INN), both pins output the same common-mode output voltage  $V_{CMout}$ , as specified in the [Electrical Characteristics](#) table. For absolute differential input voltages greater than  $250\text{ mV}$  but less than  $320\text{ mV}$ , the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of  $V_{CLIPout}$ , as shown in [Figure 7-2](#), if the differential input voltage exceeds the  $V_{Clipping}$  value.



**Figure 7-2. Output Behavior of the AMC1400-Q1**

The AMC1400-Q1 offers a fail-safe feature that simplifies diagnostics on a system level. [Figure 7-2](#) shows the fail-safe mode, in which the AMC1400-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- When the high-side supply is missing or below the  $V_{DD1UV}$  threshold
- When the common-mode input voltage, that is  $V_{CM} = (V_{INP} + V_{INN}) / 2$ , exceeds the common-mode overvoltage detection level  $V_{CMov}$

Use the maximum  $V_{FAILSAFE}$  voltage specified in the [Electrical Characteristics](#) table as a reference value for fail-safe detection on a system level.

### 7.4 Device Functional Modes

The AMC1400-Q1 is operational when the power supplies  $V_{DD1}$  and  $V_{DD2}$  are applied, as specified in the [Recommended Operating Conditions](#) table.

## 8 Application and Implementation

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### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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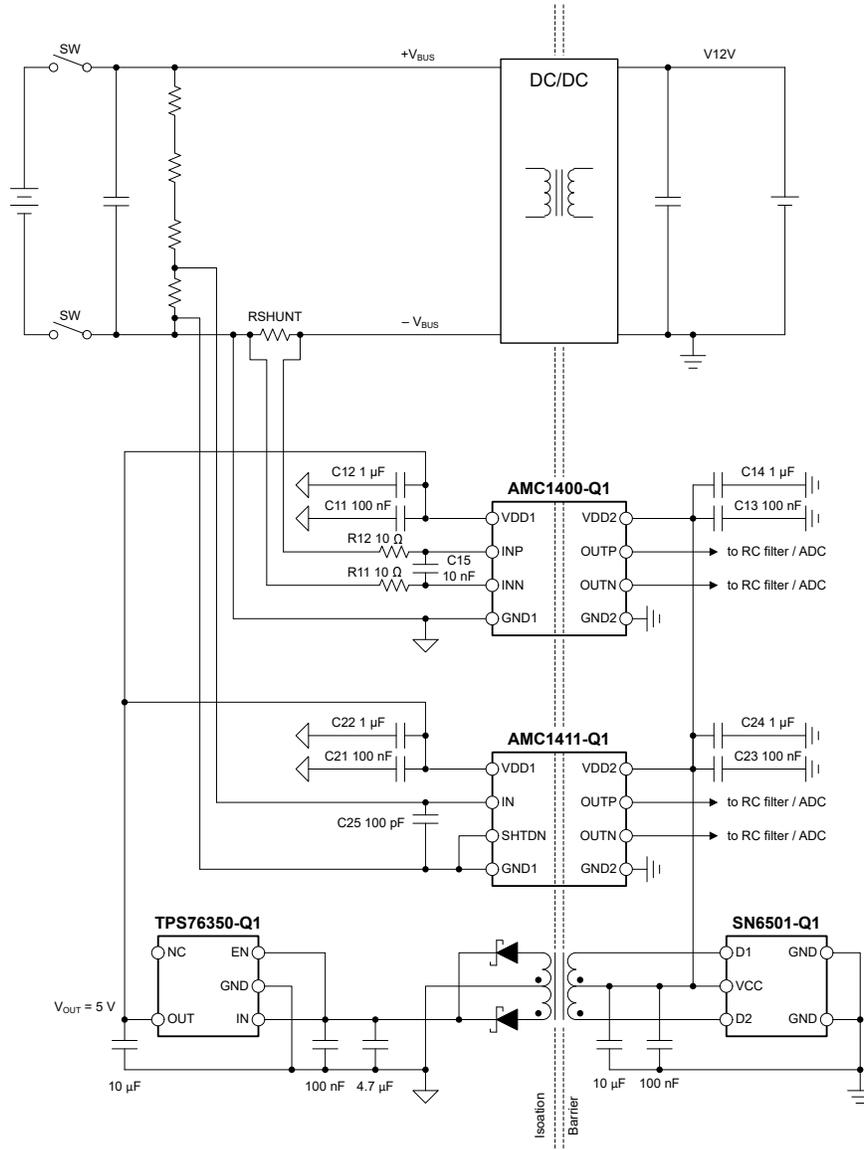
### 8.1 Application Information

With its stretched SOIC package, the AMC1400-Q1 is specifically designed for isolated, high precision, shunt-based current sensing in applications with 800-V and higher working voltages. This device is designed for operating in harsh environments with a high pollution degree or high altitudes.

### 8.2 Typical Application

 8-1 depicts a simplified block diagram of a DC/DC converter for an 800-V battery system where the AMC1400-Q1 is used to measure the input current on the high-voltage side. The DC bus current flows through a shunt resistor (RSHUNT) and produces a voltage drop that is sensed by the AMC1400-Q1. The AMC1400-Q1 outputs a differential analog voltage that is proportional to the input signal and galvanically isolated from the high-voltage side. The differential output voltage is typically routed to an analog-to-digital converter (ADC) of a microcontroller (MCU) to complete the current-sensing signal chain. The [AMC1411-Q1](#) is used in the same application for measuring the DC bus voltage. Both devices share a common high-side power supply based on the [SN6501-Q1](#) push-pull driver and a transformer that supports the desired isolation voltage ratings.

The stretched SOIC package, differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1400-Q1 ensure reliable and accurate operation in high-noise environments while meeting IEC standards for reinforced isolation at 1 kV and higher working voltages.




**8-1. Using the AMC1400-Q1 for Current Sensing in a Typical Application**

## 8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

**表 8-1. Design Requirements**

PARAMETER	VALUE
DC bus voltage	1000 V (maximum)
Overvoltage category	II
Pollution degree	2
Altitude	≤4000 m
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Transient peak DC/DC input current	10 A
Nominal DC/DC input current	4 A
Voltage drop across RSHUNT for a linear response	±250 mV (maximum)
Maximum voltage drop across RSHUNT before clipping	±320 mV (maximum)

## 8.2.2 Detailed Design Procedure

The value of the shunt resistor (RSHUNT) is selected such that the transient peak input current to the DC/DC converter (10 A) produces a voltage drop across the shunt resistor that matches the linear full-scale input range of the AMC1400-Q1 (250 mV). Consider the following two restrictions when selecting the value of the shunt resistor:

- The voltage drop across the shunt caused by the nominal-rated DC link current range must not exceed the recommended differential input voltage range for a linear response:  $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output:  $|V_{SHUNT}| \leq |V_{Clipping}|$

In this example, a 25-mΩ shunt resistor is selected (RSHUNT = 250 mV / 10 A).

At the nominal-rated current, the power dissipation in the shunt resistor is  $R \times I^2 = 25 \text{ m}\Omega \times (4 \text{ A})^2 = 0.4 \text{ W}$ . For surface-mounted shunts, the heat is mainly dissipated via the device terminals and the printed circuit board (PCB) traces. The power rating of a shunt is typically specified for a 70°C terminal temperature and derated for higher temperatures. This rating ensures that the shunt itself does not exceed its specified maximum operating temperature at the rated power dissipation. Careful PCB design is required not to exceed the terminal temperature at the rated power dissipation. Using wide copper traces to spread the heat over a larger area of the PCB, heat sinks, and air flow can improve the thermal design.

### 8.2.2.1 Insulation Coordination

Electrical insulation must be designed to withstand the rated impulse voltage, temporary overvoltage, and the working voltage. In addition, the physical distance between exposed metal parts on the high- and low-voltage sides must meet the minimum creepage and clearance requirements for the rated working voltage and transient overvoltages.

The ISO 17409:2020 standard specifies that an electrical road vehicle must be designed to withstand a minimum impulse voltage of 2500 V. The minimum *clearance* to support a 2500-V impulse voltage is 1.5 mm for basic isolation and 3.0 mm for reinforced isolation, according to Table F.2 of the IEC60664-1 standard. The equipment is designed to operate at altitudes up to 4000 m above sea level and the minimum clearance must be increased to  $1.29 \times 3 \text{ mm} = 4 \text{ mm}$  (rounded up). The factor of 1.29 is taken from table A.2 of the IEC60664-1 standard. The AMC1400-Q1 provides a minimum clearance of 14.7 mm and easily meets the requirement.

The maximum temporary overvoltage, a voltage that must be sustained for 60 s, is typically determined by the formula  $2 \times V_{WM} + 1000 \text{ V}$ , where  $V_{WM}$  is the maximum working voltage that can occur under normal operating conditions. In this example,  $V_{WM}$  equals the maximum DC bus voltage (1000 V) and the maximum temporary overvoltage is calculated to be 3000 V<sub>PK</sub> ( $2 \times 1000 \text{ V} + 1000 \text{ V} = 3000 \text{ V}$ ). If the overvoltage test (also known as the *HiPot test*) is performed for 1 s only, the test voltage must be multiplied with a factor of 1.2 times and becomes 3600 V ( $1.2 \times 3000 \text{ V} = 3600 \text{ V}$ ). The minimum *clearance* to support a 3600-V temporary overvoltage is 5.5 mm for basic isolation and 8.0 mm for reinforced isolation. These values are taken from Table 9 of the IEC61800-5-1 standard. The equipment is designed to operate at altitudes up to 4000 m above sea level and the minimum clearance must be increased to  $1.29 \times 8 \text{ mm} = 10.5 \text{ mm}$  (rounded up). The factor of 1.29 is taken from Table A.2 of the IEC60664-1 standard. The AMC1400-Q1 provides a minimum clearance of 14.7 mm and easily meets the requirement.

The working voltage in this example is 1000 V<sub>DC</sub> and is lower than the maximum working voltage ( $V_{IOWM}$ ) of 2800 V<sub>DC</sub>) that the AMC1400-Q1 supports.

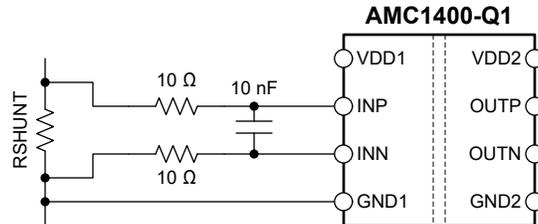
Finally, the minimum *creepage* distance for a working voltage of 1000 V<sub>DC</sub>, insulating material group I, pollution degree 2, and reinforced isolation is  $2 \times 5 \text{ mm} = 10 \text{ mm}$  according to IEC60664-1 Table F.4. The 5-mm value for the 1000-V basic insulation is doubled for reinforced isolation. The AMC1400-Q1 provides a minimum creepage of 15.7 mm and provides significant margin against the minimum requirement.

### 8.2.2.2 Input Filter Design

Place an RC filter in front of the isolated amplifier to improve the signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the  $\Delta\Sigma$  modulator
- The input bias current does not generate a significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

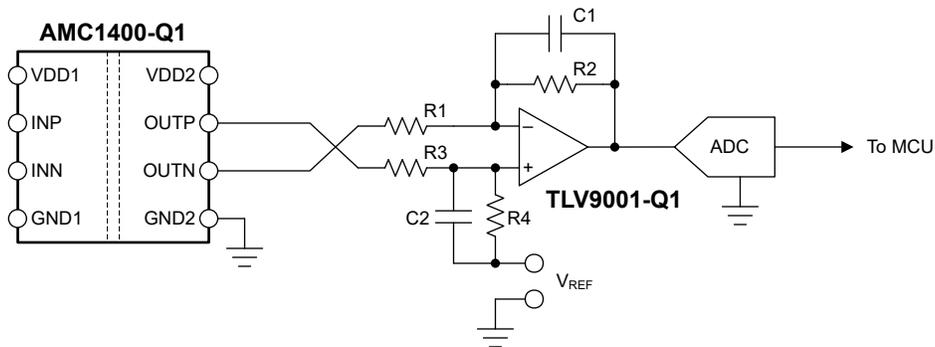
For most applications, the structure shown in [Figure 8-2](#) achieves excellent performance.



**Figure 8-2. Differential Input Filter**

### 8.2.2.3 Differential to Single-Ended Output Conversion

[Figure 8-3](#) shows an example of a TLV9001-Q1-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With  $R1 = R2 = R3 = R4$ , the output voltage equals  $(V_{OUTP} - V_{OUTN}) + V_{REF}$ . Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications,  $R1 = R2 = R3 = R4 = 3.3 \text{ k}\Omega$  and  $C1 = C2 = 330 \text{ pF}$  yields good performance.

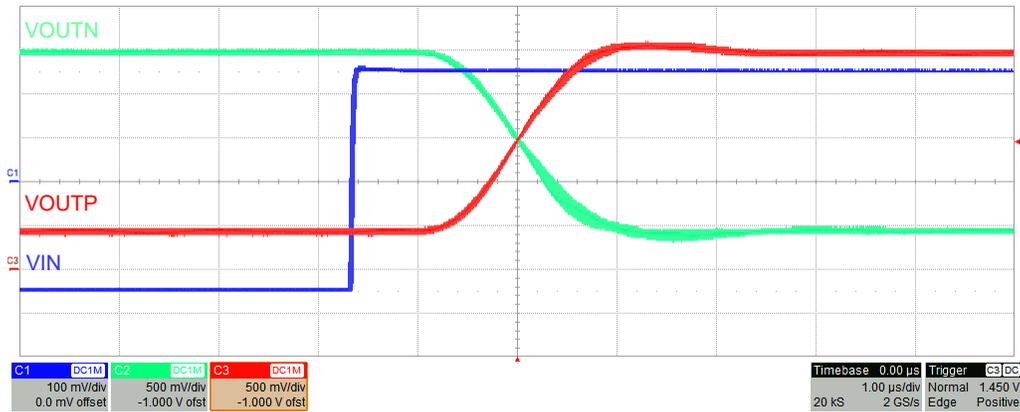


**Figure 8-3. Connecting the AMC1400-Q1 Output to a Single-Ended Input ADC**

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the [18-Bit, 1MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise](#) and [18-Bit Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guides](#), available for download at [www.ti.com](http://www.ti.com).

### 8.2.3 Application Curve

One important aspect of a power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. [Figure 8-4](#) shows the typical full-scale step response of the AMC1400-Q1.



**Figure 8-4. Step Response of the AMC1400-Q1**

### 8.3 Best Design Practices

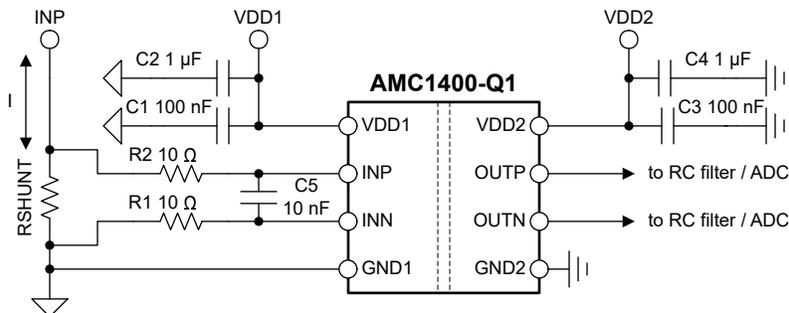
Do not leave the inputs of the AMC1400-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the output voltage may not be valid.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range, as specified in the [Recommended Operating Conditions](#) table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the [Layout](#) section for more details.

## 8.4 Power Supply Recommendations

The AMC1400-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1- $\mu$ F capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1- $\mu$ F capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in [Figure 8-5](#)) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.



**Figure 8-5. Decoupling of the AMC1400-Q1**

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

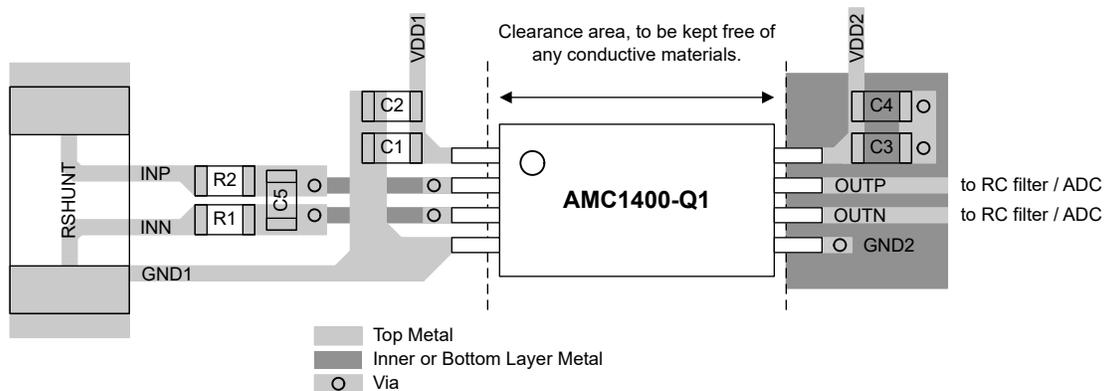
## 8.5 Layout

### 8.5.1 Layout Guidelines

 8-6 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1400-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1400-Q1 and keep the layout of both connections symmetrical.

The ground pin (GND1) of the AMC1400-Q1 is connected to the same end of the shunt resistor that is connected to the negative input pin (INN) of the AMC1400-Q1. If a four-pin shunt is used, the input pins (INN and INP) of the AMC1400-Q1 are connected to the inner leads, and the GND1 pin is connected to the outer lead on the INN-side of the shunt resistor. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device.

### 8.5.2 Layout Example



 8-6. Recommended Layout of the AMC1400-Q1

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [ISO72x Digital Isolator Magnetic-Field Immunity application note](#)
- Texas Instruments, [TLV900x-Q1 Low-Power RRIO 1-MHz Automotive Operational Amplifier data sheet](#)
- Texas Instruments, [TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators data sheet](#)
- Texas Instrument, [SN6501-Q1 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Distortion and Noise reference guide](#)
- Texas Instruments, [18-Bit, 1-MSPS Data Acquisition Block \(DAQ\) Optimized for Lowest Power reference guide](#)
- Texas Instruments, [Isolated Amplifier Voltage Sensing Excel Calculator design tool](#)
- Texas Instruments, [Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier technical white paper](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 サポート・リソース

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">AMC1400QDWLRQ1</a>	Active	Production	SOIC (DWL)   8	500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1400Q
AMC1400QDWLRQ1.A	Active	Production	SOIC (DWL)   8	500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1400Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF AMC1400-Q1 :

- Catalog : [AMC1400](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

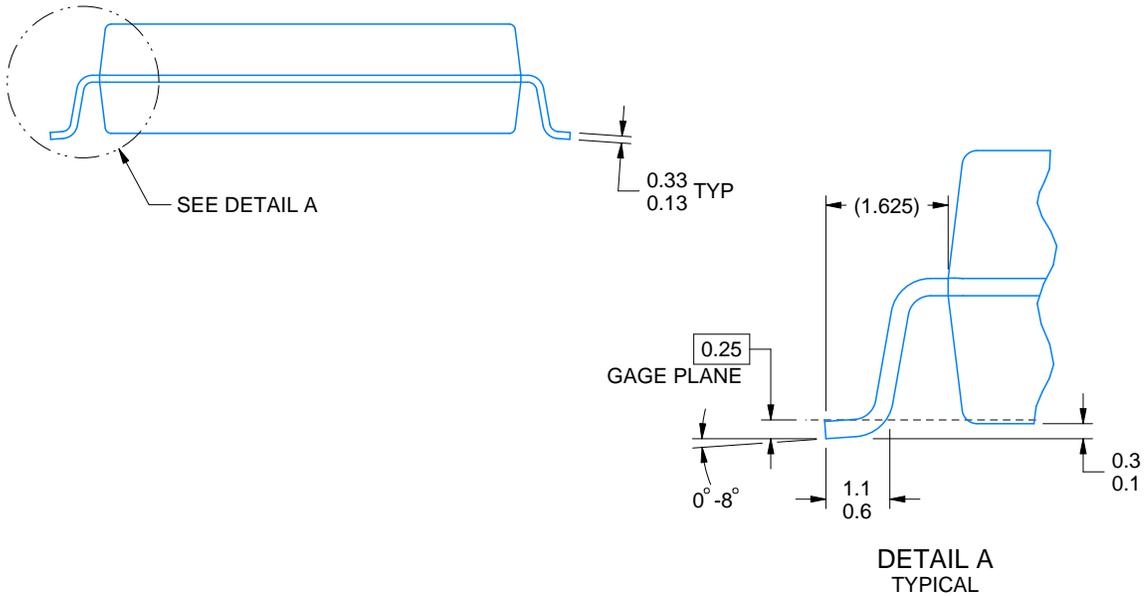
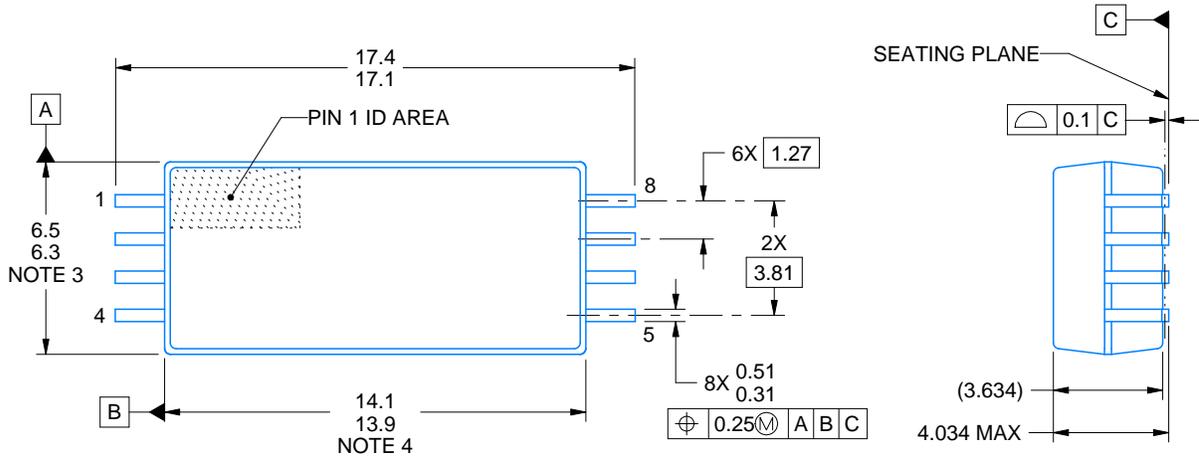
# DWL0008A



## PACKAGE OUTLINE

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



4224743/A 01/2019

**NOTES:**

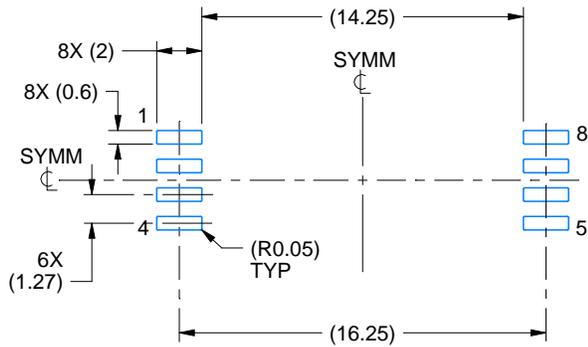
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

# EXAMPLE BOARD LAYOUT

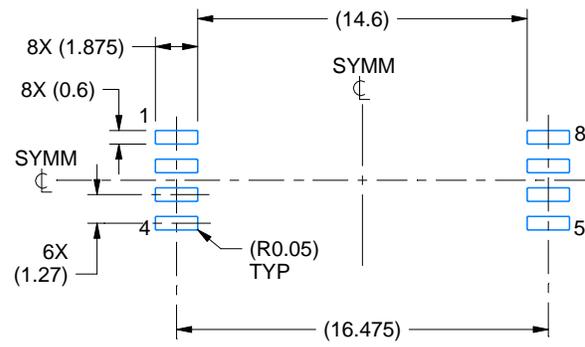
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SOIC - 4.034 mm max height

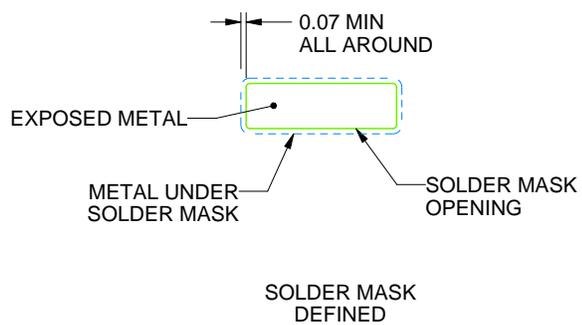
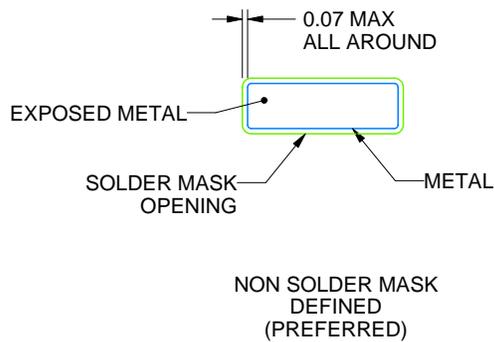
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
STANDARD  
EXPOSED METAL SHOWN  
SCALE:3X



LAND PATTERN EXAMPLE  
PCB CLEARANCE & CREEPAGE OPTIMIZED  
EXPOSED METAL SHOWN  
SCALE:3X



SOLDER MASK DETAILS

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NOTES: (continued)

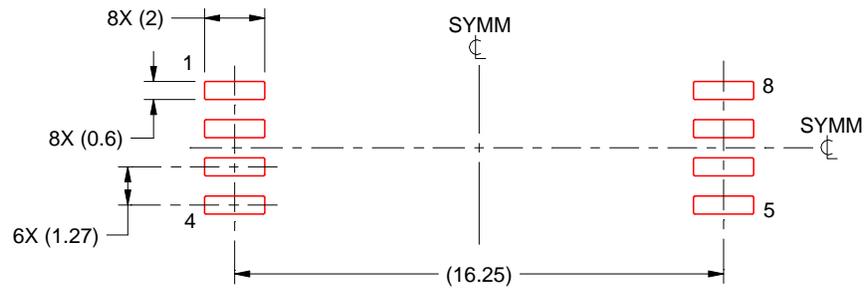
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

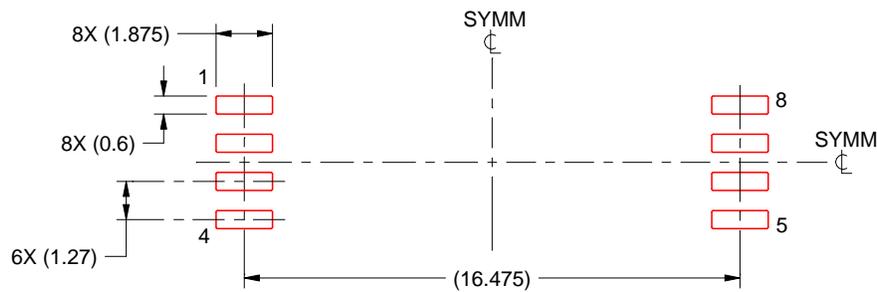
DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
STANDARD  
BASED ON 0.125 mm THICK STENCIL  
SCALE:4X



SOLDER PASTE EXAMPLE  
PCB CLEARANCE & CREEPAGE OPTIMIZED  
BASED ON 0.125 mm THICK STENCIL  
SCALE:4X

4224743/A 01/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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