BQ21080 I²C 制御、1 セル、0.8A リニア・バッテリ・チャージャ、パワー・パスおよび出荷モード付き

1 特長

- 800mA パワー・パス・リニア・バッテリ・チャージャ
  - バッテリ間充電と USB アダプタ用に最適化された入力動作電圧範囲:3.0V～5.9V
  - 許容入力電圧 25V
  - 精度 0.5% のバッテリ・レギュレーション電圧を 3.6V～4.65V の間で 10mV 刻みで設定可能
  - 5mA～800mA の設定可能な高速充電電流
  - 55mΩ バッテリー FET オン抵抗
  - 最大 2.5A の放電電流で高いシステム負荷に対応
  - 終止電流を最小 0.5mA まで設定可能
  - JEITA サポートを含む NTC 充電プロファイルのスレッショルドを設定可能
  - システムを回復させるためのパワー・サイクルおよび先進リセット機能
- システム電源およびバッテリ充電用のパワー・パス管理
  - バッテリ電圧トラッキングと入力パススルーのオプションに加えて、4.4V～4.9V の範囲でレギュレートされたシステム電圧 (SYS)
  - 設定可能な入力電流制限
  - システム用にアダプタ電源またはバッテリ電源を選択可能
  - 動的なパワー・パス管理により、弱いアダプタからの充電を最適化
- 超低静止電流モード
  - 30nA シャットダウン・モード
  - 3.2μA 出荷モード、ボタン・プレス・ウェイク付き
  - 4μA バッテリ単独モード
  - 45μA 入力アダプタ Iq (スリープ・モード)
- 1 つの押しボタンによるウェイクアップおよびリセット入力
- フォルト保護機能内蔵
  - 入力過電圧保護 (V_{IN_OVP})
  - バッテリ低電圧保護 (V_{BUVLO})
  - バッテリ短絡保護 (BATSC)
  - バッテリ過電流保護 (BATOCP)
  - 入力電流制限保護 (ILIM)
  - サーマル・レギュレーション (TREG) およびサーマル・シャットダウン (TSHUT)
  - バッテリ過熱フォルト保護 (TS)
  - ウォッチドッグおよび安全タイマ・フォルト
  - システム短絡保護
  - システム過電圧保護

2 アプリケーション

- TWS ヘッドセットと充電ケース
- スマート眼鏡、AR、VR
- スマート・ウォッチ、その他のウェアラブル・デバイス
- リテール・オートメーションおよびペイメント
- ビル・オートメーション

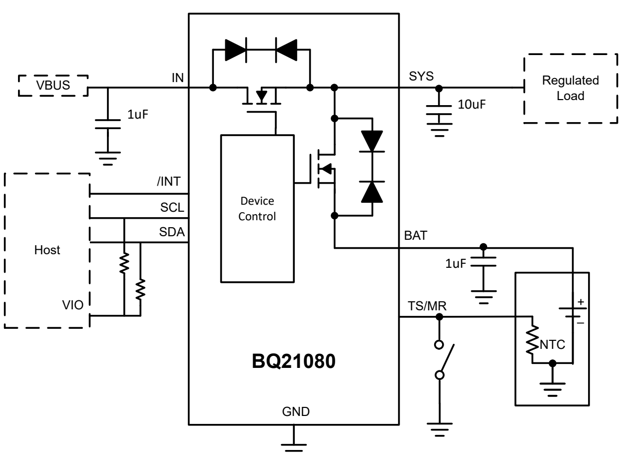
3 概要

BQ21080 は、小さなソリューション・サイズと、バッテリ寿命を延長するための低い静止電流に重点を置いたリニア・バッテリ・チャージャ IC です。このデバイスは 8 ボール・チップスケール・パッケージで供給され、製造での HDI PCB プロセスが必要ないため、PCB コストを削減できます。このデバイスは、最大 800mA の充電および最大 2.5A のシステム負荷をサポートできます。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
BQ21080	DSBGA (8)	1.6mm × 1.1mm

(1) 利用可能なパッケージについては、データシートの末尾にある注文情報を参照してください。



簡略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2023	*	Initial Release

5 Description (continued)

The battery is charged using a standard Li-ion or LiFePO4 charge profile with three phases: precharge, constant current and constant voltage. Thermal regulation provides the maximum charge current while managing the device temperature. The charger is also optimized for battery to battery charging with 3-V minimum input voltage operation and can withstand 25-V absolute maximum line transients. The device integrates a single push-button input and reset circuitry to reduce the total solution footprint.

6 Pin Configuration and Functions

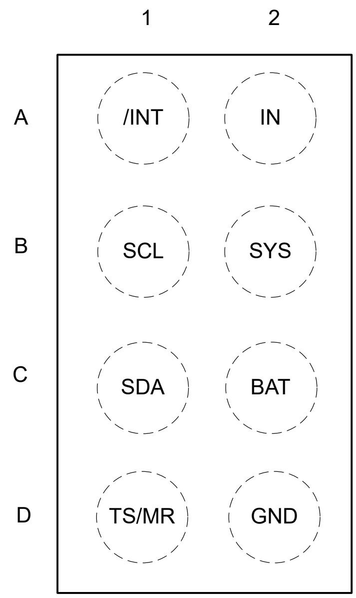


図 6-1. YBG Package 8-Pin DSBGA (Top View)

表 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
IN	A2	P	DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 µF of capacitance using a ceramic capacitor.
SYS	B2	P	Regulated System Output. Connect at least 10-µF ceramic capacitor (at least >1 µF of ceramic capacitance with DC bias derating) from SYS to GND as close to the SYS and GND pins as possible.
BAT	C2	P	Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 µF of ceramic capacitance.
GND	D2	-	Ground connection. Connect to the ground plane of the circuit.
SCL	B1	I/O	I^2C Interface Clock. Connect SCL to the logic rail through a 10-kΩ pullup resistor.
SDA	C1	I/O	I^2C Interface Data. Connect SDA to the logic rail through a 10-kΩ pullup resistor.
/INT	A1	O	INT is an open-drain output that signals fault interrupts. When a fault occurs, a 128-µs active low pulse is sent out as an interrupt for the host. INT is enabled/disabled using the MASK_INT bit in the control register. Can be pulled up to the logic rail through a 1-kΩ to 20-kΩ resistor.
TS/MR	D1	I/O	Manual Reset Input/ NTC thermistor pin. TS/MR is a general purpose input that must be held low for greater than t_{LPRESS} to go into Ship mode or perform a hardware reset. It can also be used to detect shorter button press durations such as t_{WAKE1} and t_{WAKE2} TSMR may be driven by a momentary push-button or a MOS switch. The TSMR pin can also have an NTC thermistor connected on to it.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Input Voltage	IN	-0.3	25	V
Voltage	All other pins	-0.3	5.5	V
Input Current (DC)	IN		1.1	A
SYS Discharge Current(DC)	SYS		1.5	A
SYS Discharge Current (tpulse <20ms)	SYS		2.5	A
Output Sink Current	/INT		20	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC		BQ21080 YBG (DSBGA) 8 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (EVM[(2)])	65	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[(1)])	107.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) 1oz Copper, 2-layer board

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBAT	Battery Voltage Range	2.2		4.6	V
VIN	Input Voltage Range	2.7		5.5	V

7.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IIN	Input Current Range (IN to SYS)			1.1	A
IBAT	Battery Discharge Current (BAT to SYS)			1.5	A
TJ	Operating Junction Temperature Range	-40		125	°C

7.5 Electrical Characteristics

VIN = 5V, VBAT = 3.6V. TJ =25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{Q_IN}	Input supply quiescent current	VBAT = 3.6V, VIN = 5V, Charge enabled, ICHG = 0mA, SYSREG = 4.5V		0.75	2	mA
I_{Q_IN}	Input supply quiescent current	VBAT = 3.6V, VIN = 5V, Charge enabled, ICHG = 0mA, SYSREG = Passthrough		0.660	1.5	mA
I_{SLEEP_IN}	SLEEP input current	VIN = 3.6V, VBAT = 3.7V		45		µA
I_{Q_BAT}	Battery quiescent current	V_{IN} <V_{UVLO} , VBAT =3.6V, Push-button function enabled, 0°C < T_J < 85°C		4	7.5	µA
$I_{BAT\_SHUTDOWN}$	Battery discharge current in Ship Mode	VIN = 0V, Ship Mode, VBAT = 3.6V, Adapter Sense wake enabled.		30		nA
I_{BAT_SHIP}	Battery discharge current in Ship Mode	VBAT = 3.6V, Push button function enabled (average current), 0°C < T_J < 85°C		3.2	4.5	µA
POWER-PATH MANAGEMENT AND INPUT						
V_{IN_OP}	Input voltage operating range		3		5.5	V
V_{IN_UVLOZ}	Exit IN undervoltage lock-out	IN rising			3	V
V_{IN_UVLO}	Enter IN undervoltage lock-out	IN falling			2.7	V
V_{IN_LOWV}	IN voltage to start charging	IN rising		3	3.15	V
V_{IN_LOWVZ}	IN voltage to stop charging	IN falling		2.95	3.1	V
V_{IN_PORZ}	IN voltage threshold to enter shipmode	IN falling	1.09	1.3	1.66	V
V_{SLEEPZ}	Exit sleep mode threshold	IN rising, VIN - VBAT, VBAT= 4V	100	135	185	mV
V_{SLEEP}	Sleep mode threshold hysteresis	IN falling, VIN - VBAT, VBAT= 4V		72		mV
V_{IN_OVP}	VIN overvoltage rising threshold	IN rising	5.5	5.7	5.9	V
$V_{IN\_OV\_HYS}$	IN overvoltage hysteresis	IN falling		125		mV
I_{BAT_OCP}	BATOCP(Reverse OCP only)	VBAT = 3.6V, IBAT_OCP= 00		0.5		A
		VBAT = 3.6V, IBAT_OCP= 01		1		A
		VBAT = 3.6V, IBAT_OCP= 10		1.5		A
		VBAT = 3.6V, IBAT_OCP= 11		Disabled		A
VBSUP1	Enter supplement mode threshold	VBAT = 3.6V, VBAT > V_{BUVLO}, VSYS< VBAT-VBSUP1		40		mV
VBSUP2	Exit supplement mode threshold	V_{BAT} > V_{BUVLO}, VSYS>VBAT-VBSUP2		20		mV
ILIM	Input Current Limit	VIN = 5V, ILIM =50mA	40	50	60	mA
		VIN = 5V, ILIM =100mA	80	90	98	mA
		VIN = 5V, ILIM= 300mA	270	300	330	mA
		VIN = 5V, ILIM= 500mA	450	475	498	mA
		VIN = 5V, ILIM= 1050mA	995	1050	1100	mA

7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ =25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INDPM_ACC}	VINDPM accuracy	VINDPM target is not disabled	-3		3	%
V_{INDPM}	Input voltage threshold when input current is reduced	VINDPM target =4.2V		4.2		V
V_{DPPM}	SYS voltage threshold when charge current is reduced	VBAT = 3.6V, VSYS = V_{DPPM} + VBAT before charge current is reduced.		0.1		V
$V_{SYS\_REG\_ACCURACY}$	Programmable SYS regulation accuracy	All settings, ISYS from 0-0.5A, VIN = VSYS_REG + VIN_MIN_TH, All settings except passthrough mode and battery tracking mode	–3		3	%
		ISYS = 100mA, VIN = VSYS_REG + VIN_MIN_TH, All settings except passthrough mode and battery tracking mode	–2		2	%
V_{MINSYS}	Minimum SYS voltage when in battery tracking mode	VBAT < 3.6V		3.8		V
V_{SYS_TRACK}	Voltage regulation threshold for SYS when VBAT >3.6V in battery tracking mode	VBAT = 4V, VSYS = VBAT + V_{SYS_TRACK}		225		mV
R_{SYS_PD}	SYS pull down resistance	V_{SYS} = 3.6V		25		Ω
BATTERY CHARGER						
R_{ON_BAT}	Battery FET on-resistance	VBAT = 4.5V, IBAT =500mA		55	110	mΩ
R_{ON_IN}	Input FET on-resistance	IN = 5V, IIN = 1A		270	350	mΩ
V_{REG_RANGE}	Typical BAT charge voltage regulation range	10mV steps, programmabe through I^2C	3.5		4.65	V
V_{REG_ACC}	BAT charge voltage accuracy, summary for all settings	All VBATREG settings, typical measurement at VBATREG = 4.2V	–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range	V_{OUT} > V_{LOWV}	5		800	mA
I_{CHG_ACC}	Charge current accuracy	VIN = 5V, Fastcharge >=40mA	–10		10	%
I_{CHG_ACC}	Charge current accuracy	Fastcharge current = 40mA	36	40	44	mA
I_{CHG_ACC}	Charge current accuracy	Fastcharge current = 630mA	567	630	693	mA
I_{PRECHG}	Typical pre-charge current, as percentage of ICHG	V_{OUT} < V_{LOWV}		20		%
I_{PRECHG_ACC}	Precharge current accuracy	Fastcharge current >=40mA	–10		10	%
I_{TERM_ACC}	Termination current accuracy	IBAT = 3mA (IFCHG = 30mA) Tj = 25°C	–10		10	%
I_{TERM_ACC}	Termination current accuracy	IBAT = 3mA (IFCHG = 30mA) Tj = 25°C	2.7		3.3	mA
V_{LOWV}	Pre-charge to fast-charge transition threshold	VLOWVSEL = 3.0V, VBAT rising	2.9	3	3.1	V
V_{LOWV}	Pre-charge to fast-charge transition threshold	VLOWVSEL = 2.8V, VBAT rising	2.7	2.8	2.9	V
V_{LOWV_HYS}	Battery LOWV hysteresis	All settings		100		mV

7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ =25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUVLO}	Battery UVLO, VBAT falling	BUVLO setting = b000		3		V
	Battery UVLO, VBAT falling	BUVLO setting = b011		2.8		V
	Battery UVLO, VBAT falling	BUVLO setting = b100		2.6		V
	Battery UVLO, VBAT falling	BUVLO setting = b101		2.4		V
	Battery UVLO, VBAT falling	BUVLO setting = b110		2.2		V
	Battery UVLO, VBAT falling	BUVLO setting = b111		2.0		V
V_{BUVLO_HYS}	Battery UVLO hysteresis, VBAT rising	Any BUVLO Setting, value above VBAT, VIN = 5V	110	150	190	mV
V_{BATPOR}	Battery only power up voltage, VBAT rising	-40C < Tj < 125C	3.08	3.21	3.46	V
V_{RCH}	Battery recharge threshold	BAT falling, VRCH bit = 0	75	100	130	mV
		BAT falling, VRCH bit = 1	175	200	230	mV
V_{BATSC}	Short on battery threshold for trickle charge, VBAT rising		1.6	1.8	2.0	V
V_{BATSC_HYS}	Battery short circuit voltage hysteresis			200		mV
I_{BATSC}	Trickle Charge Current	VBAT<V_{BATSC}		8		mA
TERMPERATURE REGULATION AND TEMPERATURE SHUTDOWN						
T_{REG}	Typical junction temperature regulation	THERM_REG = 00		100		°C
T_{REG}	Typical junction temperature regulation	THERM_REG = 11		Disabled		
T_{SHUT_RISING}	Thermal shutdown rising threshold	Temperature increasing		150		°C
$T_{SHUT\_FALLING}$	Thermal shutdown falling threshold	Temperature decreasing		135		°C
BATTERY NTC MONITOR						
I_{TS_BIAS}	TS nominal bias current		36.5	38	39.5	µA
V_{T1_Entry}	Cold - 00 @ Approx. 0°C, default	VIN = 5V	0.9575	1.0075	1.0575	V
V_{T5_Entry}	Cool - 00 @ Approx. 10°C, default	VIN = 5V	0.6350	0.6700	0.7025	V
V_{T6_Entry}	Warm - 00 @ Approx. 45°C, default	VIN = 5V	0.1730	0.1850	0.198	V
V_{T7_Entry}	Hot - 00 @ Approx. 60°C, default	VIN = 5V	0.1050	0.1150	0.1250	V
V_{T1_Exit}	Cold - 00 @ Approx. 5°C, default	VIN = 5V	0.7775	0.8200	0.8600	V
V_{T5_Exit}	Cool - 00 @ Approx. 15°C, default	VIN = 5V	0.5225	0.5500	0.5775	V
V_{T6_Exit}	Warm - 00 @ Approx. 41°C, default	VIN = 5V	0.2080	0.2200	0.235	V
V_{T7_Exit}	Hot - 00 @ Approx. 55°C, default	VIN = 5V	0.1250	0.1350	0.1450	V
V_{TS_ENZ}	TS monitoring enable threshold VTSMR<VTS_ENZ for TS function to be enabled	TS Rising, VIN = 5V	1.8	2.1	2.8	V
V_{TS_CLAMP}	TS maximum voltage clamp	TS open-circuit (float), VIN = 5V	2.2	2.8	3.3	V
PUSH BUTTON TIMERS AND THRESHOLDS						
I_{TSMR}	Adapter present		36.5	38	39.5	µA
I_{TSMR}	Battery only mode			60		µA
V_{TSMR}	TSMR voltage to detect a button press event, battery only mode				90	mV
V_{TSMR}	TSMR voltage to detect a button press event, adapter present				90	mV

7.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ =25°C unless otherwise noted.

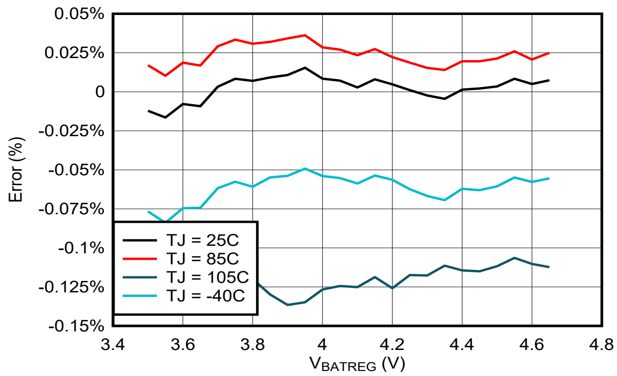
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE1}	WAKE1 Timer. Time from TSMR low detection	MR_WAKE1_TIMER = 0		300		ms
		MR_WAKE1_TIMER = 1		1		s
t_{WAKE2}	WAKE2 Timer. Time from TSMR low detection	MR_WAKE2_TIMER = 0		2		s
		MR_WAKE2_TIMER = 1		3		s
t_{RESET_WARN}	RESET_WARN Timer. Time prior to HW RESET	MR_RESET_WARN = 0	0.9	1	1.1	s
t_{LPRESS}	Long Press timer. Time from button press detection to long press action.	MR_LPRESS = 00	4.5	5	5.5	s
		MR_LPRESS = 01	9	10	11	s
		MR_LPRESS = 10	13.5	15	16.5	s
		MR_LPRESS = 11	18	20	22	s
$t_{RESTART(AUTOWAKE)}$	RESTART Timer. Time from HW Reset to SYS power up	AUTOWAKE = 00		0.5		s
		AUTOWAKE = 01		1		s
		AUTOWAKE = 10		2		s
		AUTOWAKE = 11		4		s
BATTERY CHARGING TIMERS						
t_{MAXCHG}	Charge safety timer	Programmable range	180		720	min
t_{PRECHG}	Precharge safety timer			0.25 * t_{MAXCHG}		
I2C INTERFACE						
V_{IL}	Input low threshold level	VPULLUP = 1.8V, SDA and SCL			0.4	V
V_{IH}	Input high threshold level	VPULLUP = 1.8V, SDA and SCL	1.3			V
V_{OL}	Output low threshold level	IL = 5mA, sink current, V_{PULLUP} =1.8V			0.4	V
I_{LKG}	High-Level leakage current	V_{PULLUP} = 1.8V			1	µA
LOGIC PINS						
V_{OL}	Output low threshold level	IL = 5mA, sink current, V_{PULLUP} =3.3V, /INT pin			0.4	V
I_{LKG}	High-Level leakage current	V_{PULLUP} = 3.3V, /INT pin			1	µA

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
INPUT					
$t_{VIN\_OVPZ\_DGL}$	VIN_OVP deglitch, VIN falling		30		ms
t_{SLEEP_DGL}	Deglitch time to enter SLEEP, VIN falling		64		µs
BATTERY CHARGER					
t_{REC_SC}	Recovery time, BATOCP during Discharge Mode		250		ms
t_{RETRY_SC}	Retry window for SYS or BAT short circuit recovery(BATOCP)		2		s
t_{BUVLO}	Deglitch time to disconnect the BATFET when VBAT < V_{BUVLO} setting		60		µs
$t_{TS\_DUTY\_ON}$	TS turnon-time (battery only mode)		4		ms
$t_{TS\_DUTY\_OFF}$	TS turnoff time (battery only mode)		196		ms
DIGITAL CLOCK, WATCHDOG and PUSHBUTTON					
t_{WDOG}	I2C interface reset timer, adjustable	40	160	Disabled	s
$t_{I2CRESET}$	I2C interface inactive reset timer		500		ms
$t_{SHIPWAKE}$	Wake timer to count for shipmode (WAKE2 DefaultTimer)		2		s

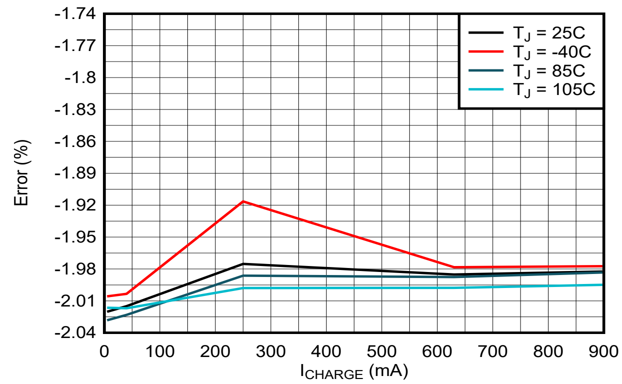
7.7 Typical Characteristics

VIN = 5 V, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, C_{BAT} = 1 µF (unless otherwise specified)



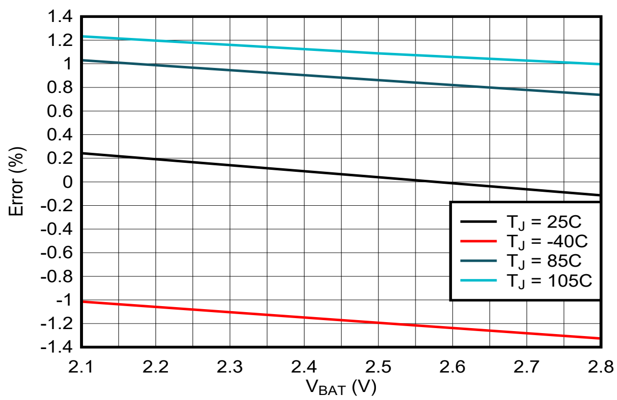
VIN = 5 V

図 7-1. Battery Regulation Voltage Accurary vs VBATREG Setting



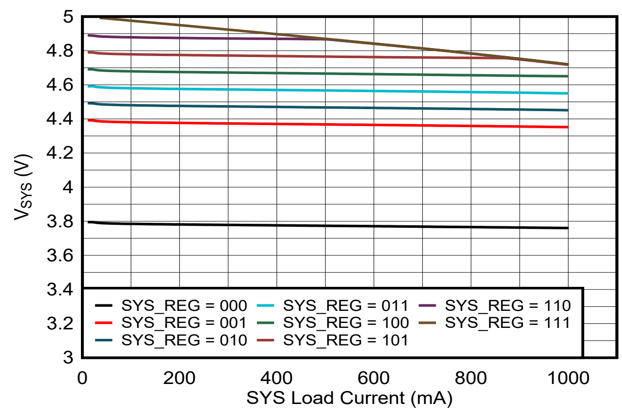
VIN = 5 V VBAT = 3.1 V

図 7-2. Charge Current Accuracy vs ICHARGE Setting



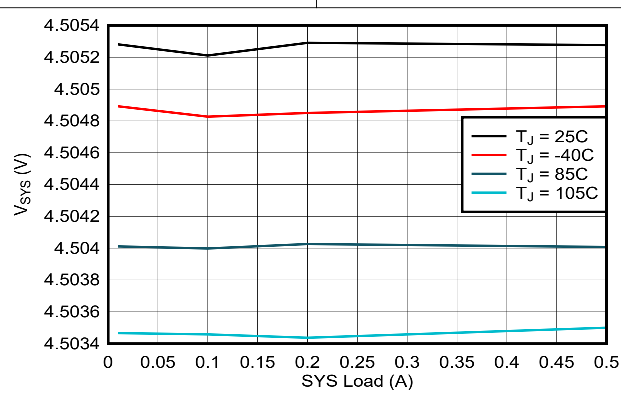
VIN = 5 V ICHG = 100 mA

図 7-3. Precharge Accuracy vs Battery Voltage



VIN = 5 V VBAT = 0 V

図 7-4. SYS Load Regulation



VIN = 5 V SYS_REG_CTRL = 010 (4.5 V)

図 7-5. SYS Load Regulation vs Temperature

8 Detailed Description

8.1 Overview

The BQ21080 integrates a linear charger that allows the battery to be charged with a programmable charge current of up to 800 mA. In addition to the charge current, other charging parameters can be programmed through I^2C such as the precharge, termination, battery regulation voltage, and input current limit.

The power path allows the system to be powered from a regulated output, SYS, even when the battery is deeply discharged or charging, by drawing power from IN pin. It also prioritizes the system load in SYS, reducing the charging current, if necessary, in order support the load when input power is limited. If the input supply is removed and the battery voltage level is above V_{BUVLO}, SYS will automatically and seamlessly switch to battery power.

Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, thermal regulation, V_{DPPM}, and V_{INDPM}. During the charging process, all loops are enabled and the one that is dominant takes control.

The device supports multiple battery chemistries for single-cell applications, through adjustable battery regulation voltage regulation (V_{BATREG}) and charge current (I_{CHG}) options.

8.1.1 Battery Charging Process

When a valid input source is connected (V_{IN} > V_{UVLO} and V_{BAT}+V_{SLEEPZ} ≤ V_{IN} < V_{IN_OVP}), the state of the CHARGE_DISABLE bit and the TSMR pin determines whether a charge cycle is initiated. When the CHARGE_DISABLE bit is set to disable charging, V_{HOT} < V_{TS} < V_{COLD} and a valid input source is connected, the battery discharge FET is turned off, preventing any charging of the battery. Note that supplement behavior is independent of the CHARGE_DISABLE bit.

The following figure illustrates a typical charge cycle.

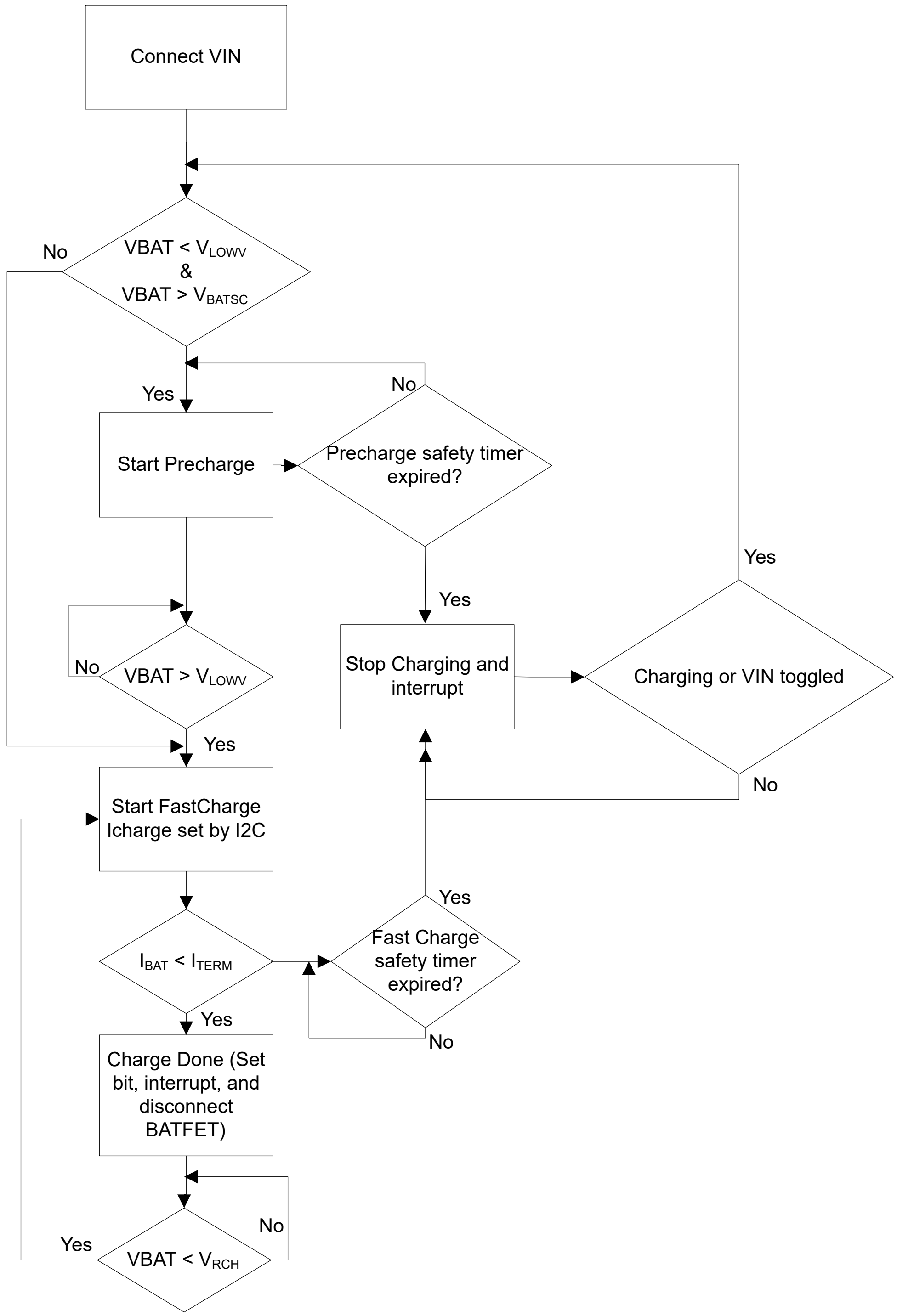


図 8-1. Charger Flow Diagram

8.1.1.1 Trickle Charge

In order to prevent damage to the battery, the device will charge the battery at a much lower current level (IBATSC) when the battery voltage (VBAT) is below the VBATSC threshold. During trickle charge, the device still counts against the precharge safety timer. Rather trickle charge and precharge are counting against the same duration of 25% of the fast charge timer.

8.1.1.2 Precharge

When battery voltage is above the V_{BATSC} but lower than V_{LOWV} threshold, the battery is charged with the precharge current level. The precharge current (IPRECHARGE) can be programmed through I^2C and can be adjusted by the host. Once the battery voltage reaches V_{LOWV}, the charger will then operate in Fast Charge mode, charging the battery at ICHG.

During precharge, the safety timer is set to 25% of the safety timer value during fast charge. In the case where termination is disabled, precharge current is set to 20% of fast charge current setting.

8.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the Constant Current (CC) and Constant Voltage (CV) loops. When the CC loop is dominant, the battery is charged at the maximum charge current level I_{CHG}, unless there is a TS fault condition (JEITA operation), VINDPM is active, thermal regulation or DPPM is active. (See respective sections for details on these modes of operation). Once the battery voltage approaches the battery regulation target, the CV loops becomes more dominant and the charging current starts tapering off. Once the charging current reaches the termination current (I_{TERM}) the charge is done, Charge_done status is set. If the I^2C setting of VBATREG is set higher than 4.65 V, the battery regulation voltage is still maintained at 4.65 V. The device will switch to fastcharge mode based on VLOWV setting on the register map.

8.1.1.4 Termination

The device will automatically terminate charging once the charge current reaches ITERM, which is programmable through I^2C. After termination the charger will operate in high impedance mode, disabling the BATFET to disconnect the battery. Power is provided to the system (SYS) by IN supply as long as $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEPZ}$ and $V_{IN} < V_{IN\_OVP}$.

Termination is only enabled when the charger CV loop is active in fast charge operation. Termination is disabled if the charge current reaches I_{TERM} while the VINDPM, DPPM, or thermal regulation loops are active. The charger will only go into the termination when the current drops to I_{TERM} due to the battery reaching the target voltage and not due to the charge current limitation imposed by the previously mentioned controlled loops.

Post termination, the battery FET is disabled and the voltage on BAT pin is monitored to check if it has dropped to the VRCH threshold. If it does, a new charge cycle is established. The safety timers are reset. During charging or even when charge is done, a higher SYS load will be supported through the supplement operation.

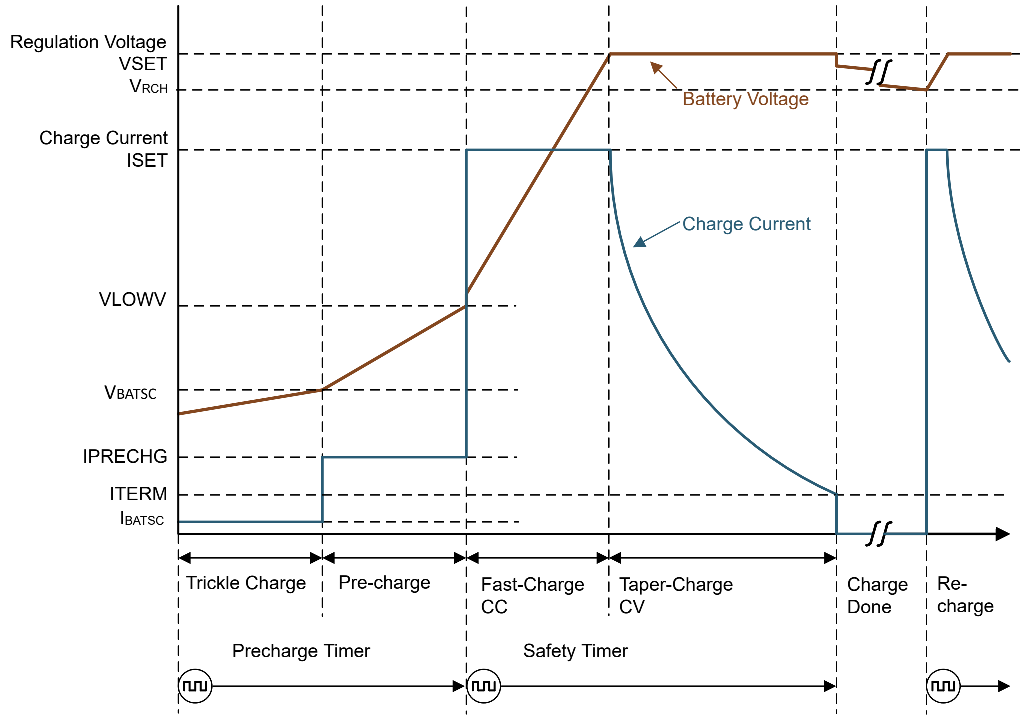


図 8-2. Typical Charging Profile of a Battery

8.2 Functional Block Diagram

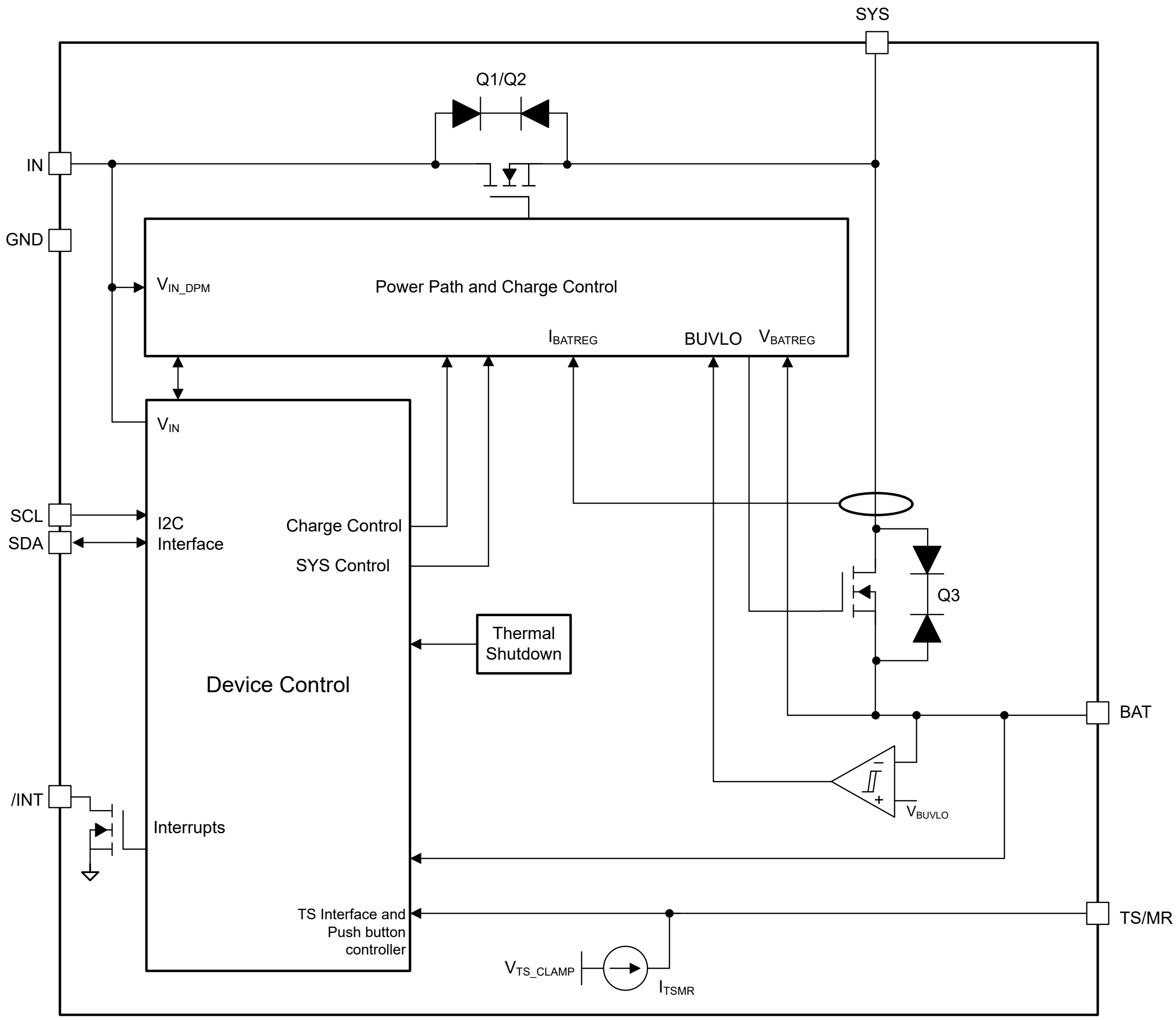


図 8-3. Functional Block Diagram

8.3 Feature Description

8.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a point where charging could be interrupted due to adapter voltage crashing below VINDPM value. This is done by reducing the current drawn by the charger enough to keep V_{IN} > VINDPM setting.

During the normal charging process, if the input power source is not able to support the programmed or default charging current and system load, the supply voltage decreases. Once the supply drops to VINDPM, the input DPM current and voltage loops will reduce the input current through the blocking FETs Q1 and Q2 to prevent the further drop of the supply. The VINDPM threshold is programmable through the I^2C register and can be completely disabled. This is set through the VINDPM_0 and VINDPM_1 selection bits. When the device enters this mode, the charge current may be lower than the set value and the VINDPM_ACTIVE_STAT bit is set. If the 2x timer is set through the 2XTMR_EN bit, the safety timer is extended while VINDPM is active. Additionally, termination is disabled when VINDPM is active.

8.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power path management circuitry monitors the input voltage and current continuously. The current into IN is shared at SYS between charging the battery and powering the system load at SYS. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If SYS drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET (Q3). If SYS falls below the supplement mode threshold after BATFET charging current is reduced to zero, the part will enter supplement mode. SYS voltage is maintained above battery voltage when the DPPM loop is in control. Battery termination is disabled when the DPPM loop is active.

The VDPPM threshold is typically 100 mV above VBAT. The VDPPM disable bit (VDPPM_DIS = b1) will allow the charger to operate with lower headroom on VSYS. In VBAT tracking mode where VSYS is VBAT+225 mV, disabling this bit will have no effect.

8.3.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at SYS reduces further. When the SYS voltage drops below the battery voltage to V_{BSUP1}, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the SYS pin rises within the battery voltage to V_{BSUP2}. During supplement mode, the battery supplement current is not regulated, however, the BATOCP protection circuit is active if enabled. Battery termination is disabled while in supplement mode. Battery voltage has to be higher than the battery undervoltage lockout threshold (VBUVLO) in order to supplement the system.

8.3.4 SYS Power Control (SYS_MODE bit control)

The device also offers the option to control SYS through the I^2C SYS_MODE bits. These bits can force SYS to be supplied by BAT instead of IN (even if $V_{IN} > V_{BAT} + V_{SLEEP}$), disconnect SYS from either supply, pull SYS down or leave it floating. The table below shows the device behavior based on SYS_MODE setting:

表 8-1. Settings

SYS_MODE	DESCRIPTION	SYS SUPPLY	SYS PULLDOWN
00	Normal Operation	IN or BAT	Off except during HW reset
01	Force BAT power (IN disconnected)	BAT	Off except during HW reset
10	SYS Off –Floating	None	Off
11	SYS Off – Pulled Down	None	On

SYS_MODE = 00

This is the default state/normal operation of the device. SYS will be powered from IN if $V_{IN} > V_{UVLO}$, V_{IN} > VBAT + V_{SLEEPZ}, and $V_{IN} < V_{IN\_OVP}$. SYS will powered by BAT if these conditions are not met. SYS will only be disconnected from IN or BAT and pulled down when a HW Reset occurs or the device goes into Ship mode.

SYS_MODE = 01

When this configuration is set, SYS will be powered by BAT if $V_{BAT} > V_{BUVLO}$ regardless of V_{IN} state. This allows the host to minimize the current draw from the adapter while it is still connected as needed in the system. If SYS_MODE = 01 is set while $V_{BAT} < V_{BUVLO}$, the SYS_MODE = 01 setting will be ignored and the device will go to SYS_MODE = 00. In the same manner, if the adapter (V_{IN}) is removed and then connected the device will also switch to SYS_MODE = 00. This prevents the device from needing a POR in order to restore power to the system thereby allowing battery charging. If SYS_MODE = 01 is set during charging, charging will be stopped and the battery will start to provide power to SYS as needed. The behavior is similar to that when the input adapter is disconnected.

SYS_MODE = 10

When this configuration is set, SYS will be disconnected and left floating. The device remains on and active. Toggling V_{IN}(V_{IN} <V_{INUVLO}) will reset SYS_MODE to 00.

SYS_MODE = 11

When this configuration is set, SYS will be disconnected and pulled down to ground. Toggling V_{IN} will reset SYS_MODE to 00.

8.3.4.1 SYS Pulldown Control

The device has an internal pulldown on the SYS pin which is enabled in the following cases:

表 8-2. States

STATE	NOTES
Shipmode	Pulldown on SYS is enabled once the device enters shipmode and after disconnecting the BATFET
HW_RESET	Pulldown on SYS is enabled after the BATFET and input blocking FETs are disconnected and retained until the autowake timer expires
SYS_MODE = 11 (SYS pulldown mode)	Pulldown on SYS is enabled after the BATFET and input blocking FETs are disconnected and retained until either an I^2C transaction is issued to change SYS_MODE or VIN is toggled.

8.3.5 SYS Regulation

The device includes a SYS voltage regulation loop. By regulating the SYS voltage the device prevents downstream devices connected to SYS from being exposed to voltages as high as V_{IN_OVP}. SYS regulation is only active when V_{IN} > V_{UVLO}, V_{IN} > V_{BAT} + V_{SLEEPZ} and V_{IN} < V_{IN_OVP} rather than meeting the VIN_Powergood condition.

The SYS voltage regulation target can be controlled through the SYS_REG_CTRL_2:0 bits in the SYS_REG register to either track the battery, set to a fixed voltage, or enable pass through modes.

In battery tracking mode, the minimum voltage is at the V_{MINSYS} value for a battery < 3.6 V. As battery voltage increases VSYS is regulated to 225 mV above battery. If V_{IN} < V_{MINSYS} and VIN_Powergood is still active, then SYS will be in dropout.

In fixed voltage mode, SYS voltage is regulated to a target set by the host ranging from 4.4 V to 4.9 V. If V_{IN} voltage is less than the SYS target voltage, then the device will be in dropout mode.

In pass through mode, the SYS path is unregulated and the V_{SYS} voltage is equal to V_{IN}.

表 8-3. SYS Voltage Regulation Settings

SYS_REG_CTRL	VSYS TARGET
000	VBAT + 225 mV (3.8 V minimum)
001	4.4
010 (default)	4.5
011	4.6
100	4.7
101	4.8
110	4.9
111	Pass through

8.3.6 ILIM Control

The input current limit can be controlled through I^2C by selecting the the ILIM bits.

If the ILIM clamp is active, the ILIM_ACTIVE_STAT bit is set.

MASK_ILIM will prevent an interrupt from being issued but does not override the ILIM behavior itself. The ILIM value can be programmed dynamically through the I^2C by the host. The ILIM settings of 100mA and 500mA are designed to be the maximum value to support standard systems.

8.3.7 Protection Mechanisms

8.3.7.1 Input Overvoltage Protection

Input overvoltage protection protects the device and downstream components connected to SYS, and BAT against damage from overvoltage on the input supply. When VIN > V_{IN_OVP}, a VIN overvoltage condition is determined to exist. During the VIN overvoltage condition, the device turns the input FET OFF, battery discharge FET ON, sends a single 128-μs pulse on INT, and the fault bit (VIN_OVP_FAULT_FLAG) is updated over I^2C. The VIN_PGOOD_STAT bit also is affected by the VIN overvoltage condition as the VIN powergood condition will fail. Once the VIN overvoltage condition is removed ($V_{IN} \le V_{IN\_OVP} - V_{IN\_OV\_HYS}$), the VIN_OVP_STAT bit is cleared and the device returns to normal operation. Thereafter, a VIN powergood condition is determined if VIN > VBAT + V_{SLEEPZ} and VIN > V_{IN_UVLO}.

8.3.7.2 Battery Undervoltage Lockout

In order to prevent deep discharge of the battery the device integrates a battery undervoltage lockout feature which will disengage the BAT to SYS path when voltage at the battery drops below the programmed BUVLO setting present in the CHARGERCTRL1 register. BUVLO status can also be read when a valid voltage on VIN is present.

8.3.7.3 System Overvoltage Protection

The system overvoltage protection is to prevent SYS from overshooting to a high voltage due to the input supply. SYS_OVP will momentarily disconnect the blocking FETs and re-engage when the thresholds have dropped to less than the SYS_OVP_FALLING threshold.

The SYS_OVP_RISING threshold is typically 105% of the target SYS voltage and the SYS_OVP_FALLING threshold is 102.5% of the target SYS voltage.

8.3.7.4 System Short Protection

When a valid adapter is connected to the device, the device turns ON the input blocking FET for 5 ms and it detects the SYS pin to be shorted (voltage on SYS <1.6V). In this scenario, the device will turn OFF the input FET for ~200 μs and turn it back ON for 5 ms for SYS to rise above 1.6V. If after 10 tries, the SYS short still persists, the device will turn OFF SYS until adapter is connected again.

8.3.7.5 Battery Overcurrent Protection

In order to protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the current on the battery FET exceeds IBAT_OCP. If the BATOCP limit is reached, the battery discharge FET is turned off and the device starts operating in hiccup mode, re-enabling the BATFET t_{REC_SC} (250 ms) after being turned OFF by the overcurrent condition. If the overcurrent condition is triggered upon retry for 4 to 7 consecutive times in a 2-s window, the BATFET shall then remain off until a valid VIN is connected (VIN = VIN_POWERGOOD). If the overcurrent condition and hiccup operation occur while in supplement mode where VIN is already present, VIN must be toggled in order for the BATFET to be enabled and start another detection cycle.

8.3.7.6 Safety Timer and Watchdog Timer

At the beginning of each charge cycle mode (Precharge or Fast Charge), the device starts the respective mode safety timer. If charging has not terminated before the programmed safety time, t_{MAXCHG} expires or the device does not exit the precharge mode before t_{PRECHG} expires, charging is disabled. The precharge safety time, t_{PRECHG}, is 25% of t_{MAXCHG}. When a safety timer fault occurs, a single 128-μs pulse is sent on the INT pin and the STAT and FAULT bits of the status registers are updated over I^2C.

The charge enable bit or input power must be toggled in order to clear the safety timer fault.

If the safety timer has expired, the device will produce an interrupt and update the SAFETY_TMR_FAULT_FLAG bit on the register map. The safety timer duration is programmable using the SAFETY_TIMER_1:0 bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2XTMR_EN bit that doubles the safety timer duration to prevent premature safety timer expiration when the charge current is reduced by a high load on SYS (DPM operation- causing VDPPM to be enabled), VINDPM, thermal regulation, or a NTC (JEITA) condition. When the 2XTMR_EN bit is set, the timer is allowed to run at half speed when any loop is active other than CC or CV. In the event where during CC mode the battery voltage drops to push the charger into precharge mode, (due to a large load on battery, thermal events, and so forth) the safety timer will reset counting through precharge and then resetting the fast charge safety timer. If the device entered battery supplement mode while in precharge, CC or CV mode, while the charger is not disabled, the device will suspend the safety timer until charging can resume again. This prevents the safety timer from resetting when a supplement condition is caused.

In addition to the safety timer, the device contains a watchdog timer that monitors the host through the I^2C interface. The watchdog timer is enabled by default and may be disabled by the host through an I^2C transaction. Once the initial transaction is received, the watchdog timer is started. The watchdog timer is reset by any transaction by the host using the I^2C interface. If the watchdog timer expires without a reset from the I^2C interface, all charger parameters registers (ICHG, IPRECHARGE, ITERM,VLOWV, and so forth) are reset to the default values. The watchdog timer can be set through the WATCHDOG_SEL_1:0 bits either in battery only mode or when an adapter is present.

表 8-4. Watchdog Settings

WATCHDOG_SEL_1:0	ACTION
00	Device will only perform a software reset after 160s of the last I^2C transaction
01	Device will issue a HW_Reset after 160s of last I^2C transation
10	Device will issue a HW_Reset after 40s of the last I^2C transaction
11	Watchdog functionality is completely disabled

8.3.7.7 Thermal Protection and Thermal Regulation

During operation, to protect the device from damage due to overheating, the junction temperature of the die, T_J, is monitored. When T_J reaches T_{SHUT_RISING}, the device stops charging operation and VSYS is shutdown. If in the case where $T_J > T_{SHUT\_RISING}$ prior to power being applied to the device (either battery or adapter), the input FET or BATFET will not turn ON, regardless of the TSMR pin. Thereafter if temperature falls below $T_{SHUT\_FALLING}$, the device will automatically power up if VIN is present or if in battery only mode.

During the charging process, to prevent overheating in the device, the device monitors the junction temperature of the die and reduces the charging current once T_J reaches the thermal regulation threshold (T_{REG}) based on bits set by the THERM_REG setting. If the charge current is reduced to 0, the battery supplies the current needed to supply the SYS output. Thermal regulation can be disabled through I^2C.

Ensure that system power dissipation is under the limit of the device. The power dissipated by the device can be calculated using the following equation:

$$P_{DISS} = P_{SYS} + P_{BAT}$$

Where:

$$P_{SYS} = (V_{IN} – V_{SYS}) * I_{IN}$$

$$P_{BAT} = (V_{SYS} – V_{BAT}) * I_{BAT}$$

The die junction temperature, T_J, can be estimated based on the expected board performance using the following equation:

$$T_J = T_A + \theta_{JA} * P_{DISS}$$

θ_{JA} is largely driven by board layout. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*. Under typical conditions, the time spent in this state is very short.

8.3.8 Pushbutton Wake and Reset Input

The pushbutton function implemented through the TSMR pin has three main functions. First, it serves as a means to wake the device from ultra-low power modes like ship mode. Second, it serves as a short button press detector, sending an interrupt to the host when the button driving the TSMR pin has been pressed for Wake1, Wake2, or long press durations. This allows the implementation of different functions in the end application such as menu selection and control. Finally it serves as a means to get the device into ship mode or reset the system by performing a power cycle/ hardware reset (shut down SYS and automatically powering it back on) after detecting a long button press. The timing for the short and long button press duration is programmable through I^2C for added flexibility and allows system designers to customize the end user experience of a specific application. Note that if a specific timer duration is changed through I^2C while that timer is active and has not expired, the new programmed value will be ignored until the timer expires and/or is reset by new push button action. In battery only mode the device will automatically pulse the TSMR current source ON for $t_{TS\_DUTY\_ON}$ duration and turn it OFF for $t_{TS\_DUTY\_OFF}$ duration to check if a button is pressed. If a button press is registered, the device will begin counting against Wake1, Wake2 or long press durations. This button press detection routine in battery only mode is run as long as it is enabled by the EN_PUSH bit. When a valid adapter is present, the TSMR current source is always ON to monitor charging.

8.3.8.1 Pushbutton Wake or Short Button Press Functions

There are two programmable wake or short button press timers, WAKE1 and WAKE2. There are no specific actions taken by the t_{WAKE1} or t_{WAKE2} durations other than issuing an interrupt and updating the wake registers. For a wake from shipmode event when the button press is enabled, the push button has to be low for $t_{shipwake}$ before the device can turn ON the SYS rail.

In the case where a valid V_{IN} ($V_{IN} > V_{UVLO}$) is connected prior to the $t_{shipwake}$ timer expiring, the device will exit shipmode immediately regardless of the TS/MR or wake timer state. Refer to セクション 8.5 for more details.

8.3.8.2 Pushbutton Reset or Long Button Press Functions

Depending on the configuration set on the pushbutton long press action register bits, the device will perform a shipmode entry or hardware reset or completely ignore the long button press action.

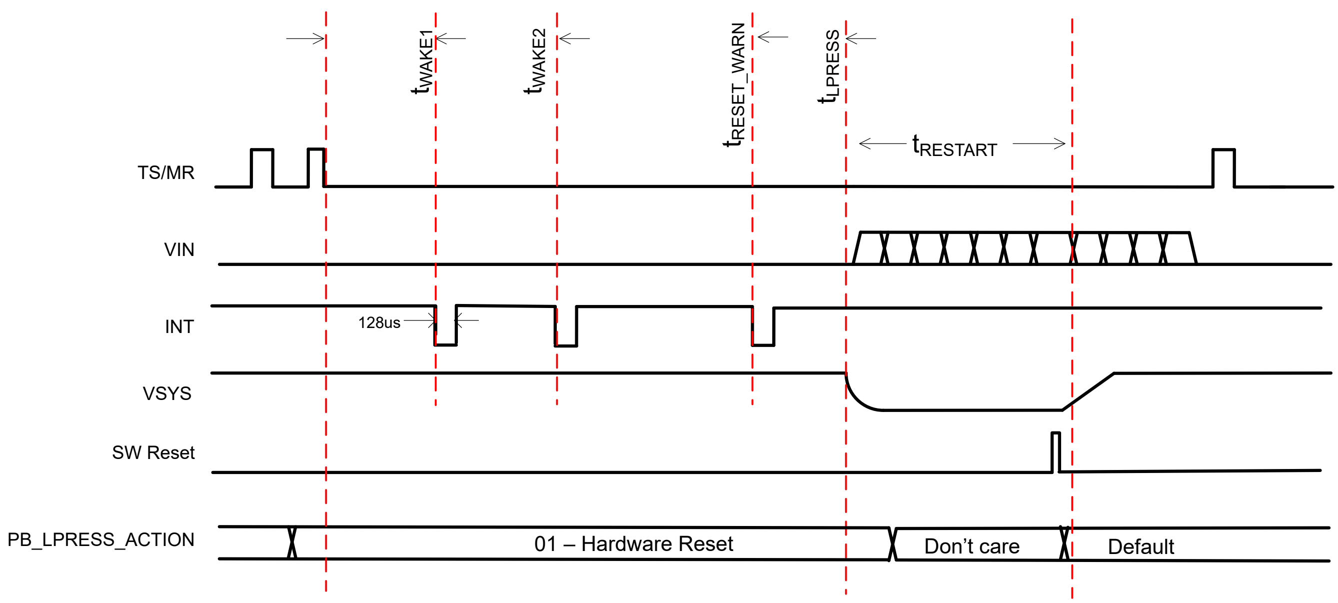


図 8-4. Pushbutton Long Press Reset

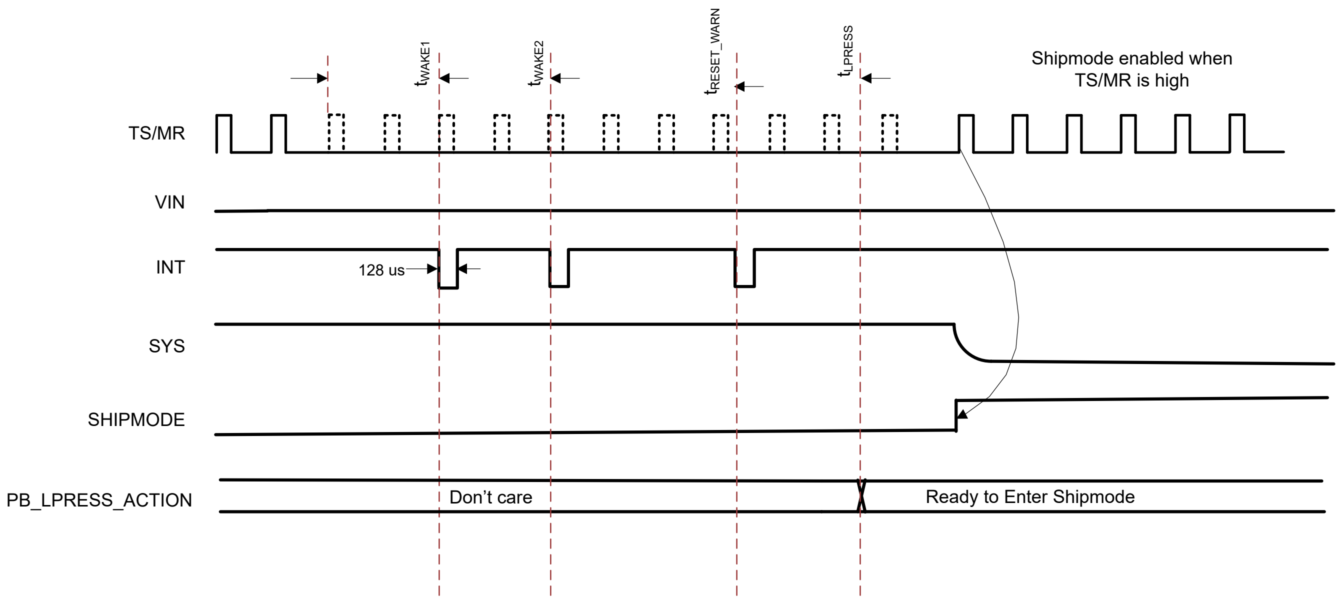


図 8-5. Pushbutton Long Press Shipmode

8.3.9 15-Second Timeout for HW Reset

Based on the I^2C register bit WATCHDOG_15S_ENABLE the device can perform a HW reset/power cycle in the same manner a long button press or HW_RESET would. This 15-second watchdog or timeout is gated upon $V_{IN} > V_{VBAT} + V_{SLEEPZ}$ so that the HW reset would only occur if the host does not respond after a charger is connected and VIN_PGOOD_STAT is set.

If the charger is connected and the host responds before the 15-second watchdog expires, the part continues in normal operation and starts the normal 50-second watchdog timer if enabled. The 15-second watchdog may be enabled/disabled through I^2C with the WATCHDOG_15S_ENABLE bit.

8.3.10 Hardware Reset

The BQ21080 is capable of a hardware reset to completely powercycle the system. This is partcularly useful when a soft reset on the MCU or host fails to work. Below is a sequence of events during a hadware reset:

1. Turn OFF (if adapter is present) input blocking FET (Q1/Q2)
2. Turn OFF battery FET (Q3)
3. Engage pulldown on SYS
4. Start the Autowake timer
5. Once the Autowake timer expires, disconnect the pulldown on SYS
6. Reset all registers to default
7. Turn ON battery FET and input FET (if applicable)

8.3.11 Software Reset

When a software reset is issued either through a watchdog action configurable through the WATCHDOG_SEL bits or register reset configurable through the REG_RST bit, the device will reset all of the registers to the defaults. Any bits loaded through OTP memory are also loaded. If the device was waiting to go to shipmode (all conditions for entering ship are fulfilled except adapter removal), a hardware or software reset will cancel the pending shipmode request. If the shipmode request was written through I^2C, the host can cancel the ship entry by clearing the bit before shipmode entry has happened.

8.3.12 Interrupt Indicator (/INT) Pin

The device contains an open-drain output that signals its status and is valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent.

The /INT pin is normally in high impedance and is pulled low for 128 µs when an interrupt condition occurs. When a fault or status change occurs or any other condition that generates an interrupt, a 128-µs pulse (/INT pin pulled down) is sent on /INT to notify the host.

Interrupts can be masked through I^2C. If the interrupt condition occurs while the interrupt is masked an interrupt pulse will not be sent. If the interrupt is unmasked while the fault condition is still present, an interrupt pulse will not be sent until the /INT trigger condition occurs while unmasked. Below are a list of interrupts that can be masked through I^2C.

表 8-5. Mask Bit

MASK BIT	ACTION
ILIM_INT_MASK	Do not issue an /INT pulse when ILIM limiting occurs
VDPM_INT_MASK	Do not issue an /INT pulse when VINDPM or DDPM is active
TS_INT_MASK	Do not issue an /INT pulse when any of the TS events have occured.
TREG_INT_MASK	Do not issue an /INT pulse when TREG is actively reducing the current
PG_INT_MASK	Do not issue an /INT pulse when VIN meets VIN_PG condition
BAT_INT_MASK	Do not issue an /INT pulse when BATOCP or BUVLO event is triggered
CHG_STATUS_INT_MASK	Do not send an interrupt anytime there is a charging status change.

8.3.13 External NTC Monitoring (TS)

8.3.13.1 TS Biasing and Function

The device can be configured to meet JEITA requirements or a simpler HOT/COLD function only. Additionally, the TS charger control function can be disabled through the TS_EN bit. This will only disable the TS charge action but the faults are still reported based on the TS voltage. To satisfy the JEITA requirements, four temperature thresholds are monitored: cold battery threshold, cool battery threshold, warm battery threshold, and hot battery threshold. These temperatures correspond to the VCOLD, VCOOL, VWARM, and VHOT thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to the value programmed in the TS_Setting register/bit TS_ICHG_0. When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced by 100 mV or 200 mV based on the value programmed in the TS_VRCG_0 bit within the TS_Setting register.

For devices where the TS function is not needed, tie a 10-kΩ resistor to the TS pin.

There is an active voltage clamp present on this device which will prevent the voltage on the TSMR pin from rising above the VTS_CLAMP threshold. This will particularly be ON when the TSMR pin is floating. The bit TS_OPEN_STAT is set when this clamp is active. This will also be ON regardless of the TS_EN bit. The interrupt is asserted as long as the TS_INT mask is not written.

The bits TS_HOT/TS_COLD, TS_WARM, and TS_COOL will allow these thresholds to be adjusted. The hysteresis will also move along with these thresholds. When the TS_WARM condition occurs, the device will lower the battery target regulation voltage by TS_VRCG but will not modify the VBAT_CTRL register.

The TS_ICHG bit will reduce charging current based on the factor described in the register map when the TSMR pin hits a TS_COOL condition. The TREG function will still be based on this reduced threshold.

The TS_VRCG_0 bit will reduce the charging voltage when the TSMR pin hits the TS_WARM threshold. The factor will be based on the register map.

When the button is detected as pressed (TSMR pin low) during the charging process, charging will be momentarily suspended until the button is high again. When charging is disabled in any of the TS faults, trickle charging is also disabled. In a TS fault where the current is reduced (COOL), the trickle charging current is not altered.

8.3.14 I²C Interface

The BQ21080 device uses a fully compliant I²C interface to program and read control parameters, status bits, and so on. I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA, and SCL. A controller device, usually a micro-controller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A peripheral device receives and transmits data on the bus under control of the controller device.

The BQ21080 works as a peripheral and supports the following data transfer modes, as defined in the I²C Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements.

Register contents remain intact as long as VBAT or VIN voltages remains above their respective UVLO levels.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The BQ21080 device 7-bit address is 0×6A (shifted 8-bit address is 0xD4).

8.3.14.1 F/S Mode Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 図 8-6. All I²C-compatible devices should recognize a start condition.

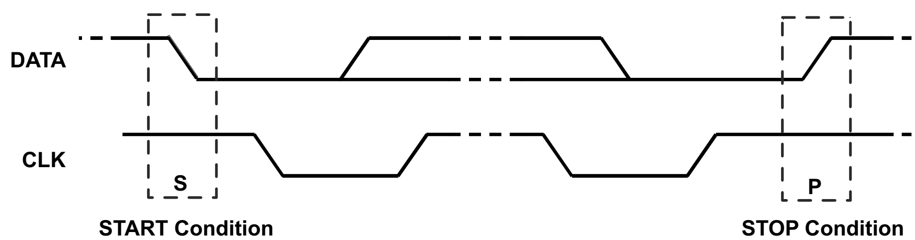


図 8-6. START and STOP Condition

The controller then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the controller ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 8-7). All devices recognize the address sent by the controller and compare it to their internal fixed addresses. Only the peripheral device with a matching address generates an acknowledge (see 図 8-8) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a peripheral has been established.

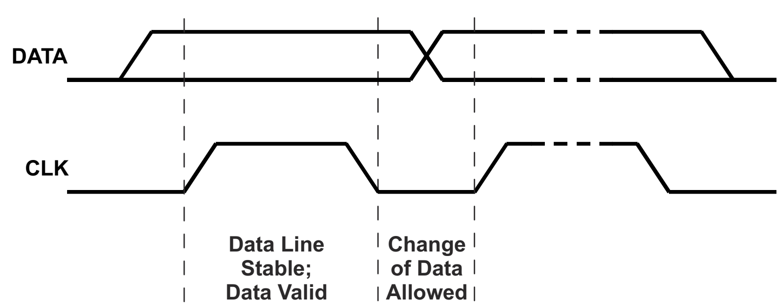


図 8-7. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the peripheral (R/W bit 0) or receive data from the peripheral (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the controller or by the peripheral, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 8-6). This releases the bus and stops the communication link with the addressed peripheral. All I²C compatible devices must recognize the stop condition. Upon receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the controller needs to send a STOP condition to prevent the peripheral I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section results in FFh being read out.

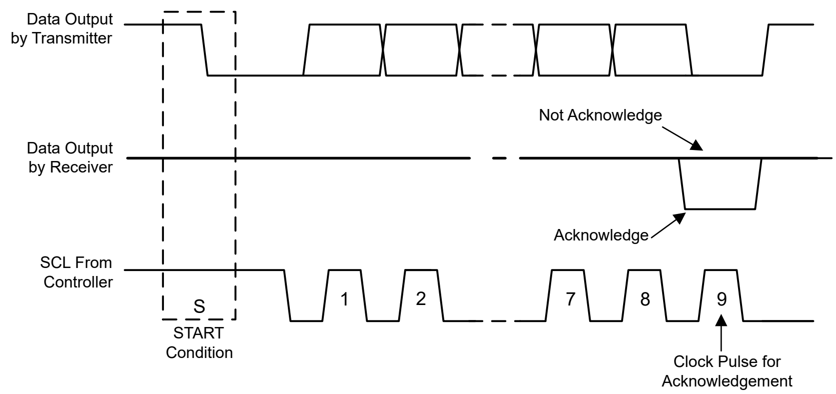


図 8-8. Acknowledge on the I²C Bus

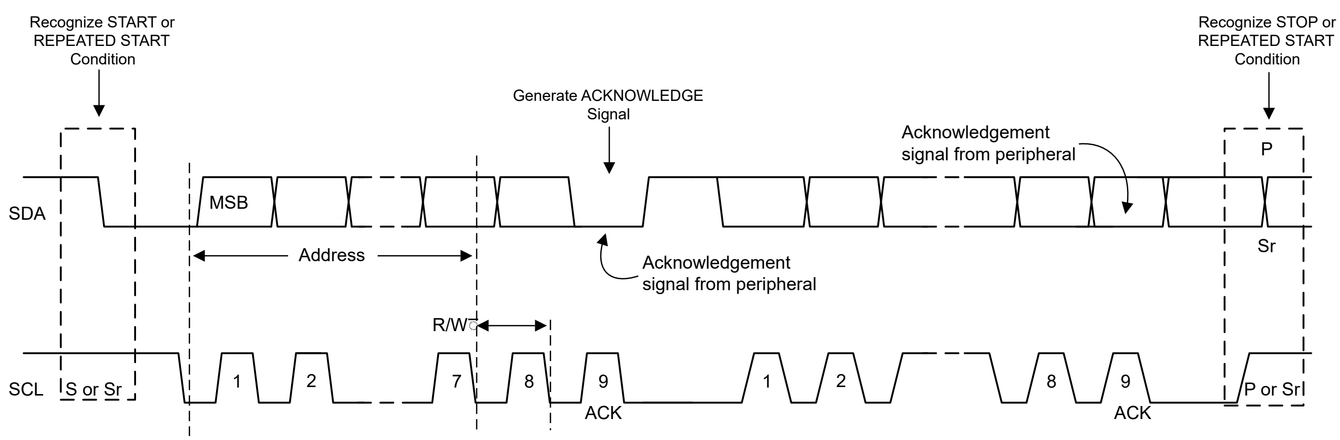


図 8-9. Bus Protocol

8.4 Device Functional Modes

The BQ21080 has four main modes of operation: Battery Mode, Ship Mode, Charge/Adapter Mode when a supply is connected to IN, and Shutdown mode. The table below summarizes the functions that are active for each operation mode.

表 8-6. Function Availability Based on Primary Mode of Operation

FUNCTION	CHARGE/ADAPTER MODE	BATTERY MODE	SHIP MODE	SHUTDOWN MODE
Input overvoltage	Yes	Yes	No	No
Input undervoltage	Yes	Yes	Yes	Yes
Battery overcurrent	Yes, if enabled	Yes	Yes, if enabled	No
Battery undervoltage	Yes	Yes	No	No
Input DPM	Yes, if enabled	No	No	No

表 8-6. Function Availability Based on Primary Mode of Operation (continued)

FUNCTION	CHARGE/ADAPTER MODE	BATTERY MODE	SHIP MODE	SHUTDOWN MODE
Dynamic power path management	Yes, if enabled	No	No	No
BATFET	Yes	Yes	No	No
TS measurement	Yes	No	No	No
Battery charging	Yes, if enabled	No	No	No
ILIM	Yes (Register Value)	No	No	No
Pushbutton input	Yes	Yes, if enabled	Yes	No
INT output	Yes	Yes	No	No
I^2C	Yes	Yes	No	No

8.5 Register Maps

8.5.1 I2C レジスタ

表 8-7 に、I2C レジスタに対してメモリマップされたレジスタを示します。表 8-7 にないレジスタ・オフセット・アドレスはすべて予約済みと見なして、レジスタの内容は変更しないでください。

表 8-7. I2C レジスタ

オフセット	略称	レジスタ名	セクション
0h	STAT0	チャージャのステータス	STAT0 レジスタ (オフセット = 0h) [リセット = X]
1h	STAT1	チャージャのステータスと障害	STAT1 レジスタ (オフセット = 1h) [リセット = X]
2h	FLAG0	チャージャ・フラグ・レジスタ	FLAG0 レジスタ (オフセット = 2h) [リセット = X]
3h	VBAT_CTRL	バッテリ電圧制御	VBAT_CTRL レジスタ (オフセット = 3h) [リセット = 46h]
4h	ICHG_CTRL	高速充電電流制御	ICHG_CTRL レジスタ (オフセット = 4h) [リセット = 05h]
5h	CHARGECTRL0	チャージャ・コントロール 0	CHARGECTRL0 レジスタ (オフセット = 5h) [リセット = 2Ch]
6h	CHARGECTRL1	チャージャ・コントロール 1	CHARGECTRL1 レジスタ (オフセット = 6h) [リセット = 56h]
7h	IC_CTRL	IC 制御	IC_CTRL レジスタ (オフセット = 7h) [リセット = 84h]
8h	TMR_ILIM	タイマおよび入力電流制限制御	TMR_ILIM レジスタ (オフセット = 8h) [リセット = 4Dh]
9h	SHIP_RST	シップモード、リセット、プッシュボタン制御	SHIP_RST レジスタ (オフセット= 9h) [リセット= 11h]
Ah	SYS_REG	SYS レギュレーション電圧制御	SYS_REG レジスタ (オフセット= Ah) [リセット= 40h]
Bh	TS_CONTROL	TS 制御	TS_CONTROL レジスタ (オフセット = Bh) [リセット = 00h]
Ch	MASK_ID	マスクとデバイス ID	MASK_ID レジスタ (オフセット = Ch) [リセット = C0h]

表の小さなセルに収まるように、複雑なビット・アクセス・タイプを記号で表記しています。表 8-8 に、このセクションでアクセス・タイプに使用しているコードを示します。

表 8-8. I2C のアクセス・タイプ・コード

アクセス・タイプ	コード	説明
読み取りタイプ		
R	R	読み取り
RC	R C	読み出し後 クリア
書き込みタイプ		
W	W	書き込み
リセットまたはデフォルト値		
-n		リセット後の値またはデフォルト値

8.5.1.1 STAT0 レジスタ (オフセット = 0h) [リセット = X]

表 8-9 に、STAT0 の詳細を示します。

概略表に戻ります。

表 8-9. STAT0 レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	TS_OPEN_STAT	R	X	TS オープン・ステータス 1b0 = TSMR ピンがオープンでない 1b1 = TSMR ピンがオープン
6-5	CHG_STAT_1:0	R	X	充電ステータス・インジケータ 2b00 = 充電中は充電なし。 2b01 = 定電流充電 (トリクル充電 / プリチャージまたは高速充電モード) 2b10 = 定電圧充電 2b11 = 充電完了または充電がホストによってディセーブルされている。
4	ILIM_ACTIVE_STAT	R	X	入力電流制限アクティブ 1b0 = アクティブではない 1b1 = アクティブ
3	VDPPM_ACTIVE_STAT	R	X	VDPPM モード・アクティブ 1b0 = アクティブではない 1b1 = アクティブ
2	VINDPM_ACTIVE_STAT	R	X	VINDPM モード・アクティブ 1b0 = アクティブではない 1b1 = アクティブ
1	THERMREG_ACTIVE_STAT	R	X	サーマル・レギュレーション・アクティブ 1b0 = アクティブではない 1b1 = アクティブ
0	VIN_PGOOD_STAT	R	X	VIN パワー・グッド 1b0 = VIN パワー・グッドなし 1b1 = VIN パワー・グッド

8.5.1.2 STAT1 レジスタ (オフセット = 1h) [リセット = X]

表 8-10 に、STAT1 の詳細を示します。

概略表に戻ります。

表 8-10. STAT1 レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	VIN_OVP_STAT	R	1b0	VIN_OVP フォルト 1b0 = アクティブではない 1b1 = アクティブ

表 8-10. STAT1 レジスタのフィールドの説明 (continued)

ビット	フィールド	タイプ	リセット	説明
6	BUVLO_STAT	R	X	バッテリ UVLO ステータス 1b0 = アクティブではない 1b1 = アクティブ
5	RESERVED	R	X	予約済み
4-3	TS_STAT_1:0	R	2b00	TS ステータス 2b00 = 通常 2b01 = VTS < VHOT または VTS > VCOLD (充電中断) 2b10 = VCOOL < VTS < VCOLD (充電電流を TS_Registers で設定された値で低減) 2b11 = VWARM > VTS > VHOT (充電電圧を TS_Registers で設定された値で低減)
2	SAFETY_TMR_FAULT_FLAG	RC	1b0	安全タイマの期限切れフォルトは、CE がトグルされた後でのみクリアされます。 1b0 = アクティブではない 1b1 = アクティブ
1	WAKE1_FLAG	RC	1b0	Wake 1 タイマ・フラグ 1b0 = Wake 1 条件を満たしていません 1b1 = Wake 1 条件を満たしています
0	WAKE2_FLAG	RC	1b0	Wake 2 タイマ・フラグ 1b0 = Wake 2 条件を満たしていません 1b1 = Wake 2 条件を満たしています

8.5.1.3 FLAG0 レジスタ (オフセット = 2h) [リセット = X]

表 8-11 に、FLAG0 の詳細を示します。

概略表に戻ります。

表 8-11. FLAG0 レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	TS_FAULT	RC	X	TS フォルト 1b0 = TS フォルトが検出されない 1b1 = TS フォルトが検出された
6	ILIM_ACTIVE_FLAG	RC	X	ILIM アクティブ 1b0 = ILIM フォルトが検出されない 1b1 = ILIM フォルトが検出された
5	VDPPM_ACTIVE_FLAG	RC	X	VDPPM フラグ 1b0 = VDPPM フォルトが検出されない 1b1 = VDPPM フォルトが検出された
4	VINDPM_ACTIVE_FLAG	RC	X	VINDPM フラグ 1b0 = VINDPM フォルトが検出されない 1b1 = VINDPM フォルトが検出された
3	THERMREG_ACTIVE_FLAG	RC	X	サーマル・レギュレーション・フラグ 1b0 = サーマル・レギュレーションが検出されない 1b1 = サーマル・レギュレーションが発生した
2	VIN_OVP_FAULT_FLAG	RC	X	VIN_OVP フラグ 1b0 = VIN_OVP フォルトが検出されない 1b1 = VIN_OVP フォルトが検出された
1	BUVLO_FAULT_FLAG	RC	X	バッテリ低電圧フラグ 1b0 = バッテリ低電圧フォルトが検出されない 1b1 = バッテリ低電圧フォルトが検出された

表 8-11. FLAG0 レジスタのフィールドの説明 (continued)

ビット	フィールド	タイプ	リセット	説明
0	BAT_OCP_FAULT	RC	X	バッテリ過電流保護 1b0 = バッテリ過電流状態が検出されない 1b1 = バッテリ過電流状態が検出された

8.5.1.4 VBAT_CTRL レジスタ (オフセット = 3h) [リセット = 46h]

表 8-12 に、VBAT_CTRL の詳細を示します。

概略表に戻ります。

表 8-12. VBAT_CTRL レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	RESERVED	R/W	1b0	予約済み
6-0	VBATREG_6:0	R/W	7b1000110	バッテリ・レギュレーション電圧 VBATREG = 3.5V + VBATREG_CODE * 10mV。最大プログラマブル電圧 = 4.65V

8.5.1.5 ICHG_CTRL レジスタ (オフセット = 4h) [リセット = 05h]

表 8-13 に、ICHG_CTRL の詳細を示します。

概略表に戻ります。

表 8-13. ICHG_CTRL レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	CHG_DIS	R/W	1b0	充電ディセーブル 1b0 = バッテリ充電イネーブル 1b1 = バッテリ充電ディセーブル
6-0	ICHG_6:0	R/W	7b0000101	ICHG の場合 <= 35mA = ICHGCODE + 5mA (ICHG の場合) > 35mA = 40 + ((ICHGCODE-31) * 10) mA。最大プログラマブル電流 = 800mA

8.5.1.6 CHARGECTRL0 レジスタ (オフセット = 5h) [リセット = 2Ch]

表 8-14 に、CHARGECTRL0 の詳細を示します。

概略表に戻ります。

表 8-14. CHARGECTRL0 レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	RESERVED	R/W	1b0	予約済み
6	IPRECHG	R/W	1b0	プリチャージ電流 = 項の x 倍 1b0 = プリチャージは 2x 項 1b1 = プリチャージは項
5-4	ITERM_1:0	R/W	2b10	終端電流 = Icharge の % 2b00 = ディセーブル 2b01 = ICHG の 5% 2b10 = ICHG の 10% 2b11 = ICHG の 20%
3-2	VINDPM_1:0	R/W	2b11	VINDPM レベルの選択 2b00 = 4.2V 2b01 = 4.5V 2b10 = 4.7V 2b11 = ディセーブル

表 8-14. CHARGECTRL0 レジスタのフィールドの説明 (continued)

ビット	フィールド	タイプ	リセット	説明
1-0	THERM_REG_1:0	R/W	2b00	サーマル・レギュレーション・スレッショルド 2b00 = 100C 2b11 = ディセーブル

8.5.1.7 CHARGECTRL1 レジスタ (オフセット = 6h) [リセット = 56h]

表 8-15 に、CHARGECTRL1 の詳細を示します。

概略表に戻ります。

表 8-15. CHARGECTRL1 レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7-6	IBAT_OCP_1:0	R/W	2b01	バッテリ放電電流制限 2b00 = 500mA 2b01 = 1000mA 2b10 = 1500mA 2b11 = ディセーブル
5-3	BUVLO_2:0	R/W	3b010	バッテリ低電圧ロックアウトの立ち下がりスレッショルド。 3b000 = 3.0V 3b001 = 3.0V 3b010 = 3.0V 3b011 = 2.8V 3b100 = 2.6V 3b101 = 2.4V 3b110 = 2.2V 3b111 = 2.0V
2	CHG_STATUS_INT_MASK	R/W	1b1	充電ステータス割り込みをマスク 1b0 = 充電ステータスの変更があるときはいつでも充電ステータス割り込みをイネーブルする。 1b1 = 充電ステータス割り込みをマスク
1	ILIM_INT_MASK	R/W	1b1	ILIM フォルト割り込みをマスク 1b0 = ILIM 割り込みをイネーブル 1b1 = ILIM 割り込みをマスク
0	VDPM_INT_MASK	R/W	1b0	VINDPM および VDPPM 割り込みをマスク 1b0 = VINDPM および VDPPM 割り込みをイネーブル 1b1 = VINDPM および VDPPM 割り込みをマスク

8.5.1.8 IC_CTRL レジスタ (オフセット = 7h) [リセット = 84h]

表 8-16 に、IC_CTRL の詳細を示します。

概略表に戻ります。

表 8-16. IC_CTRL レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	TS_EN	R/W	1b1	TS 自動機能 1b0 = TS 自動機能がディセーブル (充電制御のみがディセーブル。TS 監視がイネーブル) 1b1 = TS 自動機能がイネーブル
6	VLOWV_SEL	R/W	1b0	プリチャージ電圧スレッショルド (VLOWV) 1b0 = 3V 1b1 = 2.8V
5	VRCH_0	R/W	1b0	再充電電圧スレッショルド 1b0 = 100mV 1b1 = 200mV

表 8-16. IC_CTRL レジスタのフィールドの説明 (continued)

ビット	フィールド	タイプ	リセット	説明
4	2XTMR_EN	R/W	1b0	タイマが遅い 1b0 = タイマはいつでも遅くなりません 1b1 = CC または CV 以外の制御では、タイマは 2 倍遅くなります
3-2	SAFETY_TIMER_1:0	R/W	2b01	高速充電タイマ 2b00 = 3 時間高速充電 2b01 = 6 時間高速充電 2b10 = 12 時間高速充電 2b11 = 安全タイマをディセーブルにする
1-0	WATCHDOG_SEL_1:0	R/W	2b00	ウォッチドッグの選択 2b00 = 160s デフォルトのレジスタ値 2b01 = 160s HW_RESET 2b10 = 40s HW_RESET 2b11 = ウォッチドッグ機能をディセーブルにする

8.5.1.9 TMR_ILIM レジスタ (オフセット = 8h) [リセット = 4Dh]

表 8-17 に、TMR_ILIM の詳細を示します。

概略表に戻ります。

表 8-17. TMR_ILIM レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7-6	MR_LPRESS_1:0	R/W	2b01	プッシュ・ボタン長押し時間タイマ 2b00 = 5s 2b01 = 10s 2b10 = 15s 2b11 = 20s
5	MR_RESET_VIN	R/W	1b0	ハードウェア・リセット条件 1b0 = 長押し時間が満たされたときにリセットを送信 1b1 = 長押し時間が満たされ、VIN_Powergood のときにリセットを送信
4-3	AUTOWAKE_1:0	R/W	2b01	自動ウェークアップ・タイマ再開 2b00 = 0.5s 2b01 = 1s 2b10 = 2s 2b11 = 4s
2-0	ILIM_2:0	R/W	3b101	入力電流制限設定 3b000 = 50mA 3b001 = 100mA (最大値) 3b010 = 200mA 3b011 = 300mA 3b100 = 400mA 3b101 = 500mA (最大値) 3b110 = 700mA 3b111 = 1100mA

8.5.1.10 SHIP_RST レジスタ (オフセット= 9h) [リセット= 11h]

表 8-18 に、SHIP_RST の詳細を示します。

概略表に戻ります。

表 8-18. SHIP_RST レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	REG_RST	R/W	1b0	ソフトウェア・リセット 1b0 = 何もしない 1b1 = ソフトウェア・リセット

表 8-18. SHIP_RST レジスタのフィールドの説明 (continued)

ビット	フィールド	タイプ	リセット	説明
6-5	EN_RST_SHIP_1:0	R/W	2b00	出荷モード・イネーブルとハードウェア・リセット 2b00 = 何もしない 2b01 = アダプタ挿入時にのみウェークアップ付きのシャットダウン・モードをイネーブルにする 2b10 = ボタン押下時またはアダプタ挿入時にェークアップ付きの出荷モードをイネーブルにする 2b11 = ハードウェア・リセット
4-3	PB_LPRESS_ACTION_1:0	R/W	2b10	プッシュ・ボタンの長押しアクション 2b00 = 何もしない 2b01 = ハードウェア・リセット 2b10 = 出荷モードをイネーブルにする 2b11 = シャットダウン・モードをイネーブルにする
2	WAKE1_TMR	R/W	1b0	Wake 1 タイマ・セット 1b0 = 300ms 1b1 = 1s
1	WAKE2_TMR	R/W	1b0	WAKE 2 タイマ・セット 1b0 = 2s 1b1 = 3s
0	EN_PUSH	R/W	1b1	バッテリのみでプッシュ・ボタンとリセット機能をイネーブルにする 1b0 = ディセーブルにする 1b1 = イネーブルにする

8.5.1.11 SYS_REG レジスタ (オフセット= Ah) [リセット= 40h]

表 8-19 に、SYS_REG の詳細を示します。

概略表に戻ります。

表 8-19. SYS_REG レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7-5	SYS_REG_CTRL_2:0	R/W	3b010	SYS レギュレーション電圧 3b000 = バッテリ・トラッキング・モード 3b001 = 4.4V 3b010 = 4.5V 3b011 = 4.6V 3b100 = 4.7V 3b101 = 4.8V 3b110 = 4.9V 3b111 = パススルー (VSYS は VIN)
4	RESERVED	R/W	1b0	予約済み
3-2	SYS_MODE_1:0	R/W	2b00	SHIPMODE を除いて SYS をどのような状態で供給するかを設定する 2b00 = SYS は VIN が存在する場合または VBAT のとき給電される 2b01 = SYS は VIN が存在しても VBAT のみから給電される 2b10 = SYS を切断し、フローティングのままにする 2b11 = SYS をプルダウンで切断する
1	WATCHDOG_15S_ENABLE	R/W	1b0	I2C ウォッチドッグ 1b0 = モード・ディセーブル 1b1 = VIN の接続後に I2C トランザクションがない場合、15 秒後に HW リセットを実行する
0	VDPPM_DIS	R/W	1b0	VDPPM をディセーブルにする 1b0 = VDPPM をイネーブルにする 1b1 = VDPPM をデセーブルにする

8.5.1.12 TS_CONTROL レジスタ (オフセット = Bh) [リセット = 00h]

表 8-20 に、TS_CONTROL の詳細を示します。

概略表に戻ります。

表 8-20. TS_CONTROL レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7-6	TS_HOT	R/W	2b00	TS ホット・スレッショルド・レジスタ 2b00 = デフォルト 60C 2b01 = 65C 2b10 = 50C 2b11 = 45C
5-4	TS_COLD	R/W	2b00	TS コールド・スレッショルド・レジスタ 2b00 = デフォルト 0C 2b01 = 3C 2b10 = 5C 2b11 = -3C
3	TS_WARM	R/W	1b0	TS ウォーム・スレッショルド 1b0 = デフォルト 45C 1b1 = ディセーブル
2	TS_COOL	R/W	1b0	TS クール・スレッショルド・レジスタ 1b0 = デフォルト 10C 1b1 = ディセーブル
1	TS_ICHG	R/W	1b0	TS 機能により減少した場合の高速充電電流 1b0 = 0.5 * ICHG 1b1 = 0.2 * ICHG
0	TS_VRCG	R/W	1b0	ウォーム時の目標バッテリ電圧の低下 1b0 = VBATREG -100mV 1b1 = VBATREG -200mV

8.5.1.13 MASK_ID レジスタ (オフセット = Ch) [リセット = C0h]

表 8-21 に、MASK_ID の詳細を示します。

概略表に戻ります。

表 8-21. MASK_ID レジスタのフィールドの説明

ビット	フィールド	タイプ	リセット	説明
7	TS_INT_MASK	R/W	1b1	TS をマスク 1b0 = TS 割り込みをイネーブル 1b1 = TS 割り込みをマスク
6	TREG_INT_MASK	R/W	1b1	TREG をマスク 1b0 = TREG 割り込みをイネーブル 1b1 = TREG 割り込みをマスク
5	BAT_INT_MASK	R/W	1b0	BATOCP および BUVLO をマスク 1b0 = BOCP および BUVLO 割り込みをイネーブル 1b1 = BOCP および BUVLO 割り込みをマスク
4	PG_INT_MASK	R/W	1b0	PG および VINOVP をマスク 1b0 = PG および VINOVP 割り込みをイネーブル 1b1 = PG および VINOVP 割り込みをマスク
3-0	Device_ID	R	4b0000	デバイス ID 4b0000 = BQ21080

9 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

A typical application of the BQ21080 consists of the device configured as an I^2C controlled single cell Li-ion battery charger and power path manager or battery applications such as smart watches and wireless headsets. A battery thermistor may be connected to the TS pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the TS/MR pin input to a push button to send interrupts to the host as a button is pressed or to allow the application end user to reset the system.

9.2 Typical Application

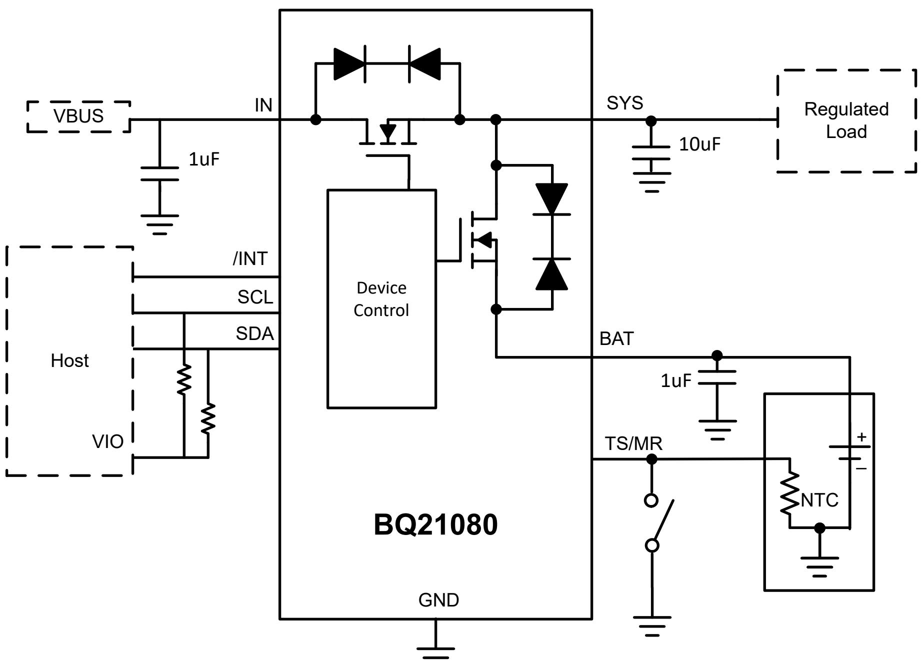


図 9-1. Typical Application

9.2.1 Design Requirements

The design requirements for the following design example are shown in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
IN supply voltage	5 V
Battery regulation voltage	4.2 V

9.2.2 Detailed Design Procedure

9.2.2.1 Input (IN/SYS) Capacitors

Low ESR ceramic capacitors such as X7R or X5R are preferred for input decoupling capacitors and should be placed as close as possible to the supply and ground pins for the IC. Due to the voltage derating of the capacitors, it is recommended that 25-V rated capacitors are used for the IN and SYS pins which can normally operate at 5 V. After derating the minimum capacitance must be higher than 1 µF.

9.2.2.2 TS

The ground connection for the NTC must be made as close as possible to the GND pin of the device or kelvin connected to it to minimize any error in TS measurement due to IR drops on the ground board lines.

If the system designer does not wish to use the TS function for charging control, a 10-kΩ resistor must be connected from TS to ground.

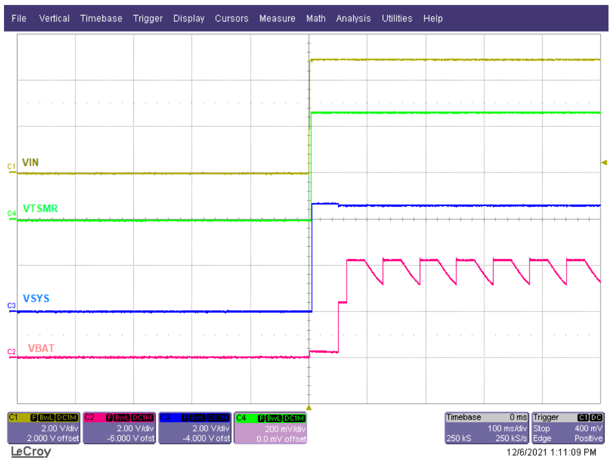
9.2.2.3 Recommended Passive Components

表 9-2. Passive Components

		MIN	NOM	MAX	UNIT
C_{SYS}	Capacitance on SYS pin	1	10	100	µF
C_{BAT}	Capacitance on BAT pin	1	1	-	µF
C_{IN}	IN input bypass capacitance	1	1	10	µF

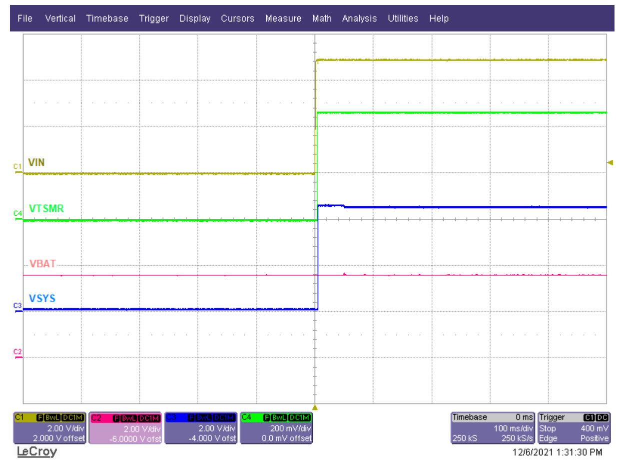
9.2.3 Application Curves

C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{IN} = 5 V, V_{OUT} = 3.8 V, I_{CHG} = 10 mA (unless otherwise specified)



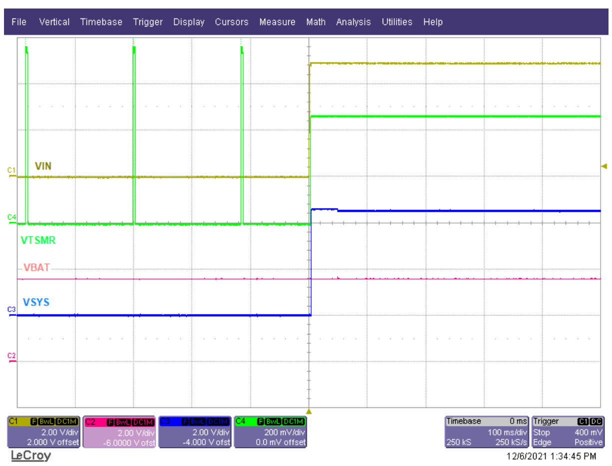
VIN = 5 V VBAT = Floating

図 9-2. Power Up with IN Supply Insertion with No Battery



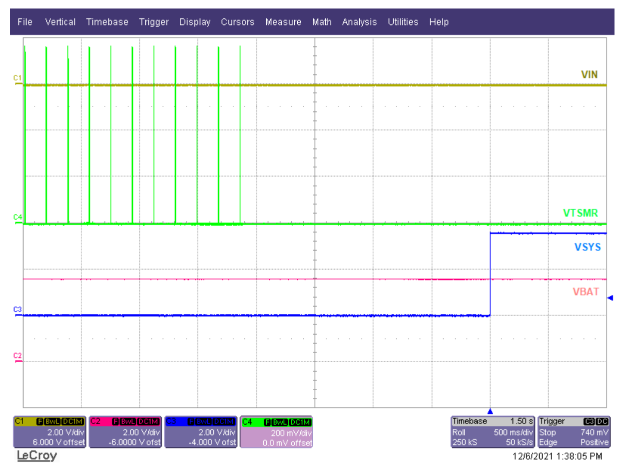
VIN = 5 V VBAT = 3.6 V

図 9-3. Power Up from Shutdown Mode with VIN Supply Insertion



VIN = 0 V → 5 V VBAT = 3.8 V

図 9-4. Power Up from Shipmode with VIN Insertion



MR_LPRESS = 00 (5s Long Press Timer)

図 9-5. Power Up from Shipmode with /TSMR Button Press

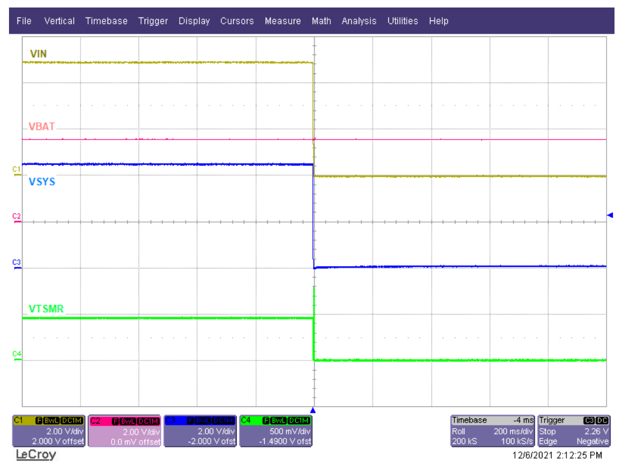
MR_LPRESS = 00 (5s Long Press Timer)
PB_LPRESS_ACTION = 01 (Hardware Reset)

図 9-6. Hardware Reset with /TSMR Press

MR_LPRESS = 00 (5s Long Press Timer)
PB_LPRESS_ACTION = 10

図 9-7. Enter Shipmode with Push Button Long Press

図 9-8. Hardware Reset Through I²C

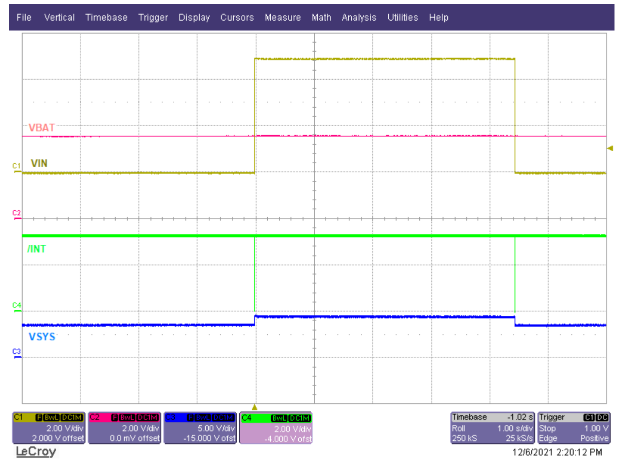


EN_RST_SHIP = 01 (enable shutdown with wake on adapter insert only)

図 9-9. Shutdown Entry on VIN Removal

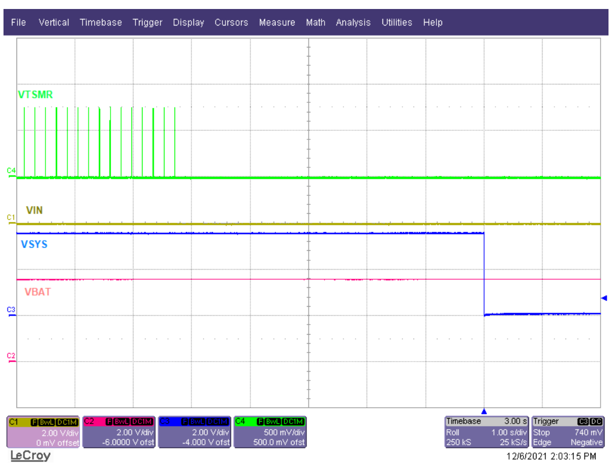
EN_RST_SHIP = 10 (enable shutdown with wake on adapter insert only)

図 9-10. Shipmode Entry on VIN Removal



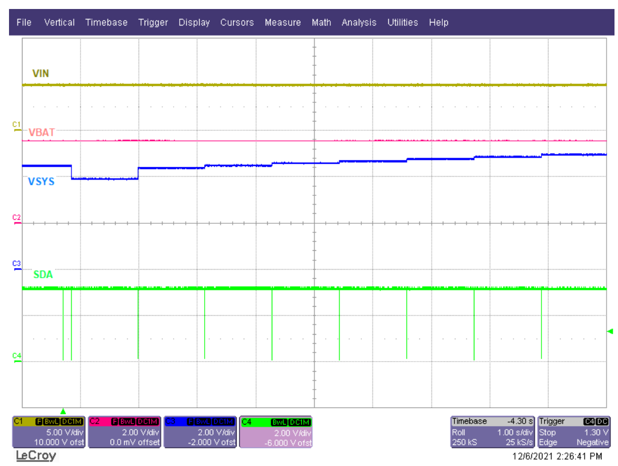
V_{IN} = 0 V → 5 V → 0 V

図 9-11. Power Good Interrupt on /INT



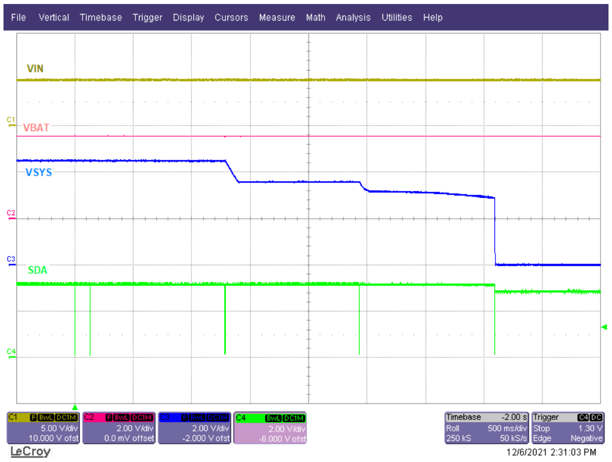
VIN = 0 V
PB_LPRESS_ACTION = 11 (enable shutown mode)
MR_LPRESS = 00 (5 seconds)

図 9-12. Shutdown Mode Entry with Push Button Long Press



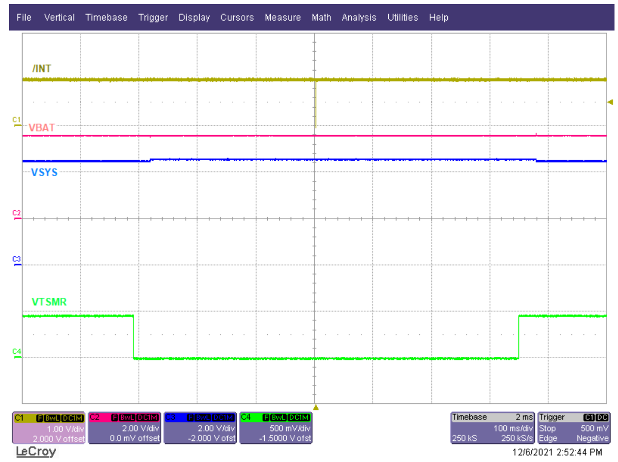
SYS_REG_CTRL = 000 → 111 in steps

図 9-13. SYS Regulation Sweep



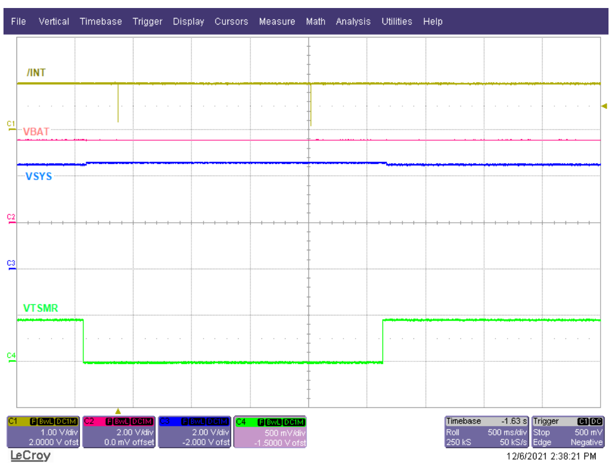
SYS_MODE = 00 → 01 → 10 → 11

図 9-14. SYS Mode Sweep



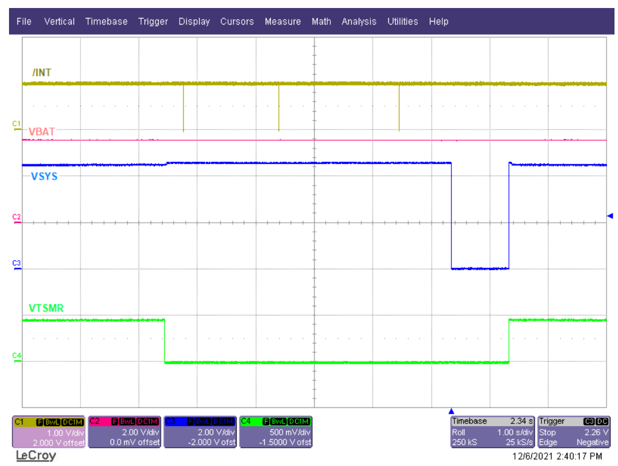
VIN = 5 V

図 9-15. Wake1 Interrupt with VIN Present



VIN = 5 V

図 9-16. Wake2 Interrupt with VIN Present



VIN = 5 V

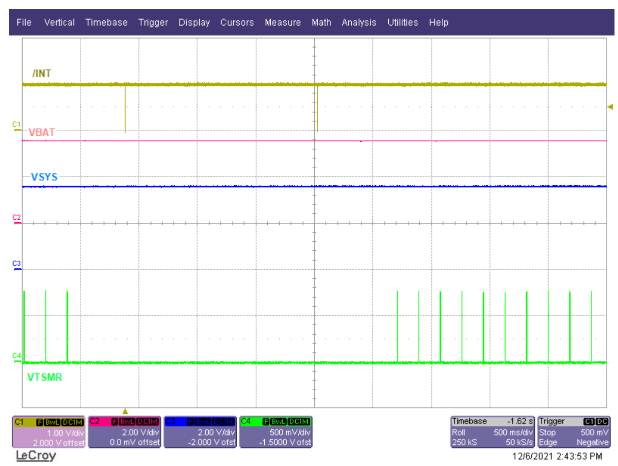
MR_LPRESS = 00 (5 seconds)

PB_LPRESS_ACTION = Hardware Reset

図 9-17. Long Press Interrupt with VIN Present

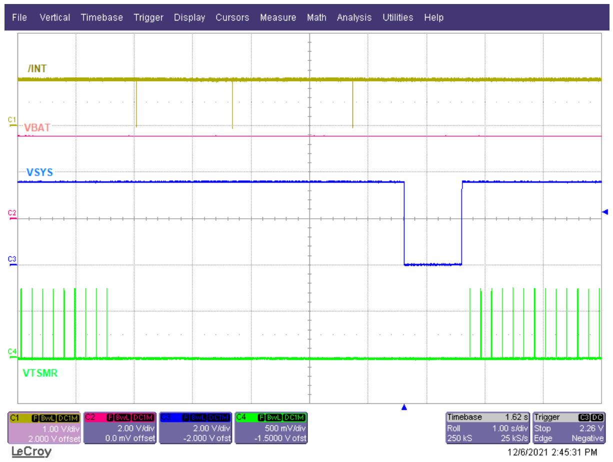
VIN = 0 V

図 9-18. Wake1 Interrupt without VIN



VIN = 5 V

図 9-19. Wake2 Interrupt without VIN Present



VIN = 0 V

MR_LPRESS = 00 (5 seconds)

PB_LPRESS_ACTION = 11 (Hardware Reset)

図 9-20. Long Press Interrupt without VIN Present

10 Power Supply Recommendations

The BQ21080 requires the adapter or IN supply to be between 2.7 V and 5.5 V. The battery voltage must be higher than 3.15 V or V_{BUVLO} to ensure proper operation.

11 Layout

11.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND, the capacitor from SYS to GND and BAT to GND should be placed as close as possible to the device, with short trace runs to IN, SYS, BAT and GND.Have solid ground plane that is tied to the GND bump
- The pushbutton GND should be connected close to the device as possible.
- The high current charge paths into IN, SYS and BAT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.

11.2 Layout Example

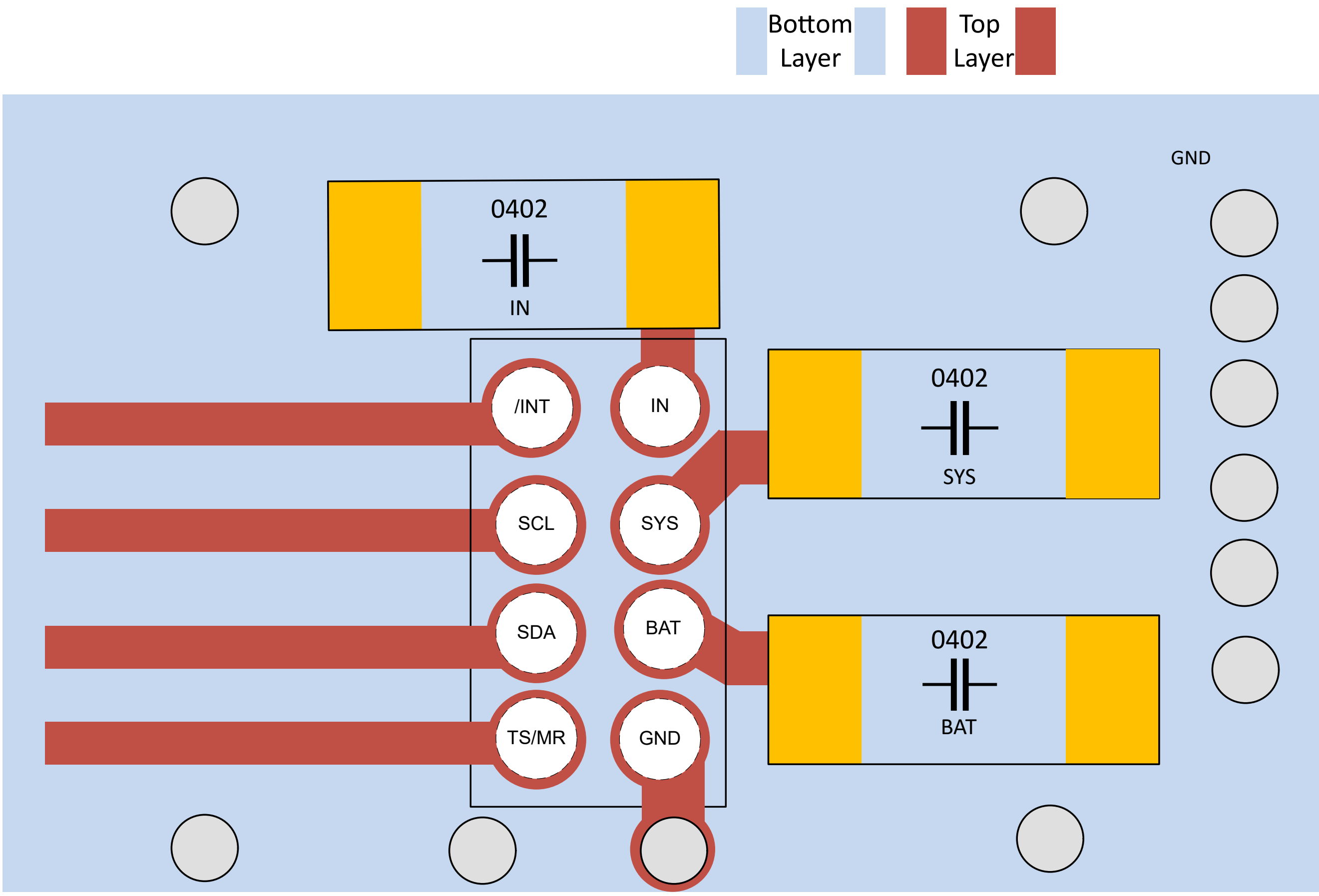


図 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

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12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

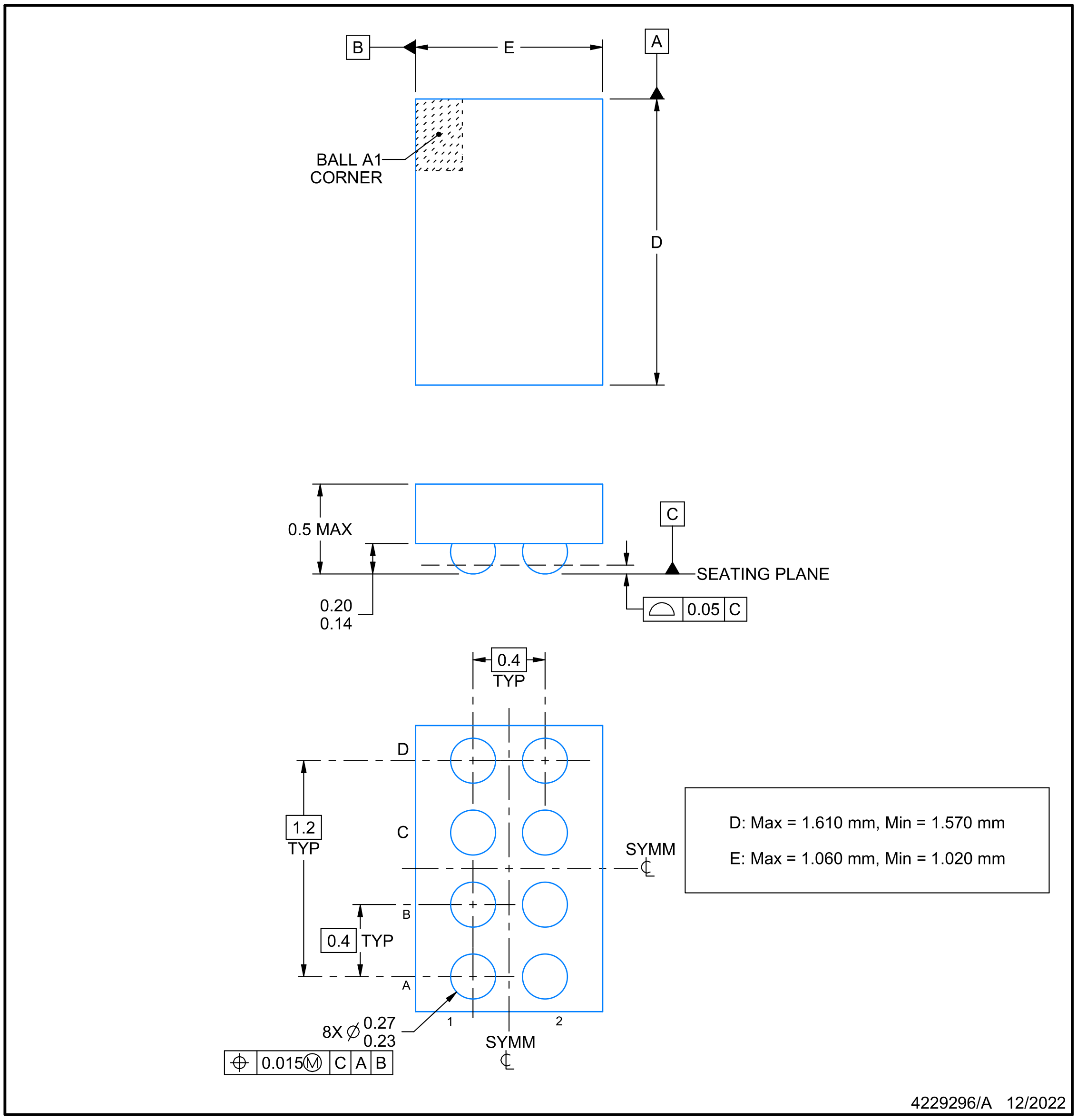
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YBG0008-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

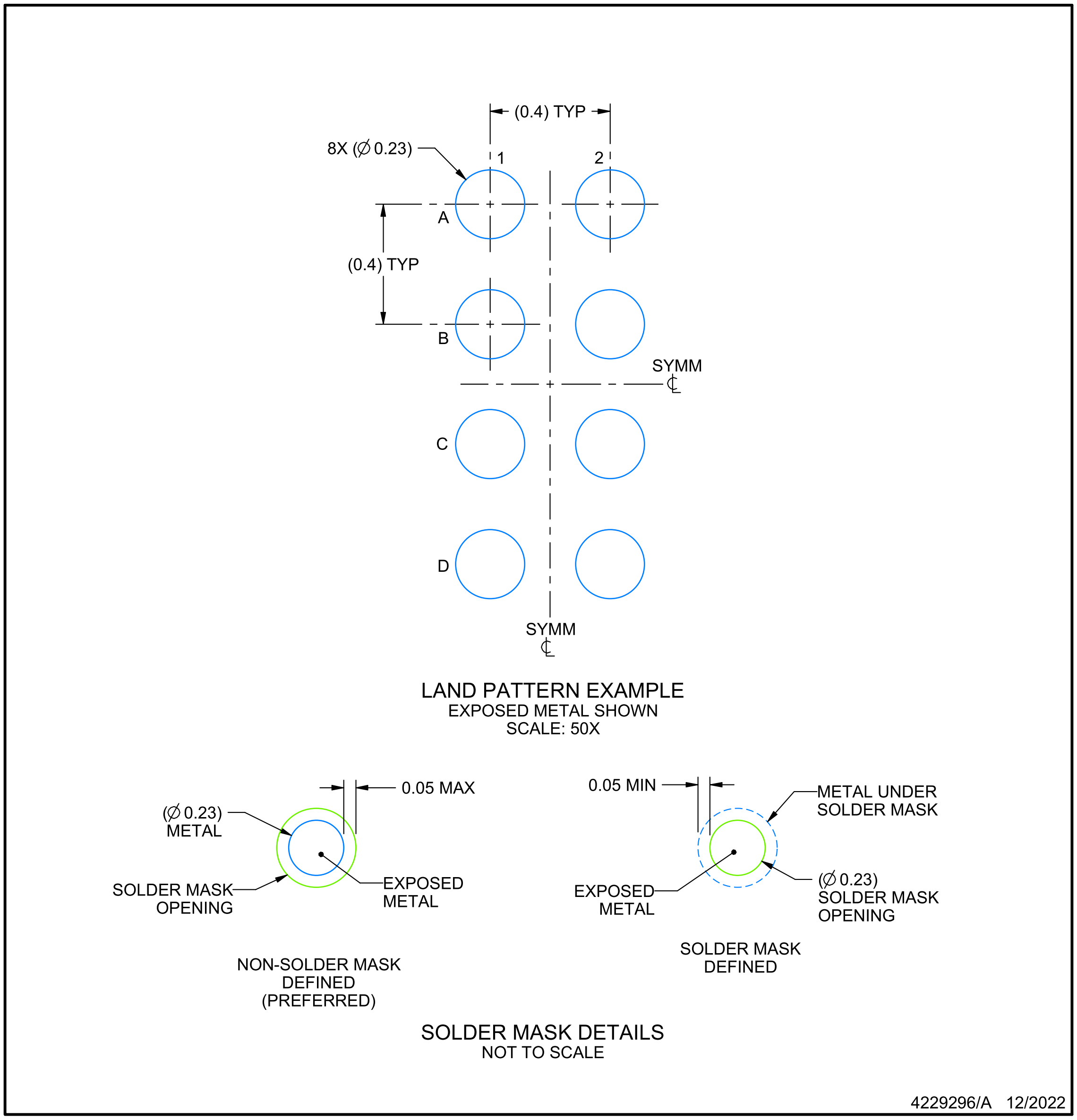
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YBG0008-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

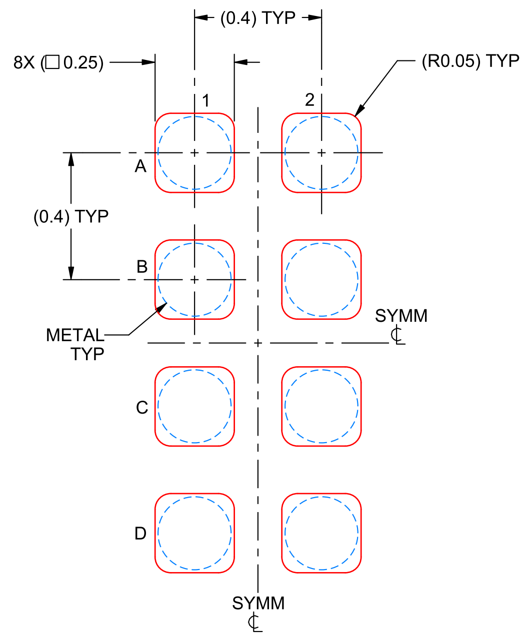
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0008-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4229296/A 12/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

TEXAS INSTRUMENTS
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ21080YBGR	ACTIVE	DSBGA	YBG	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B080	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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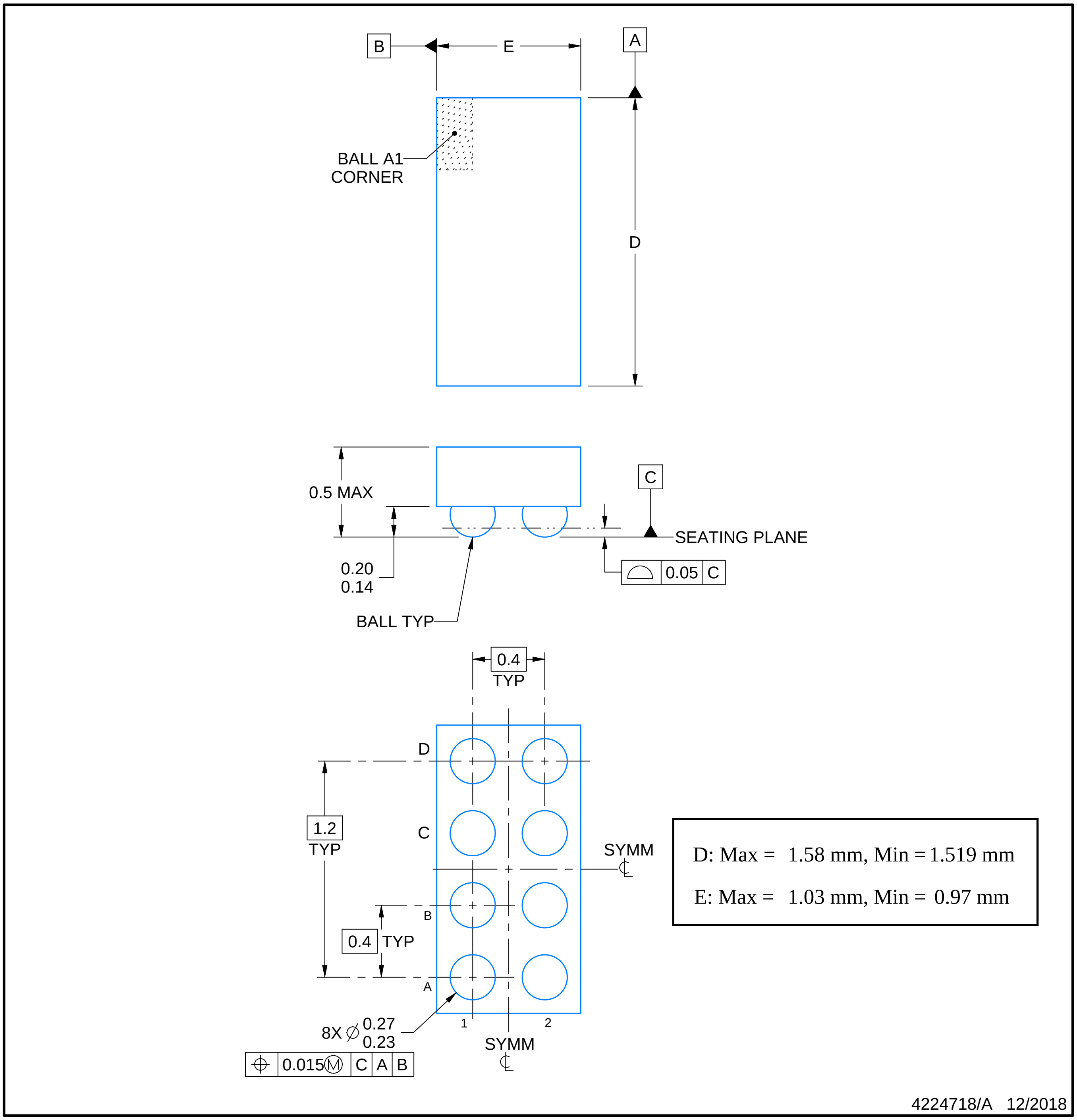
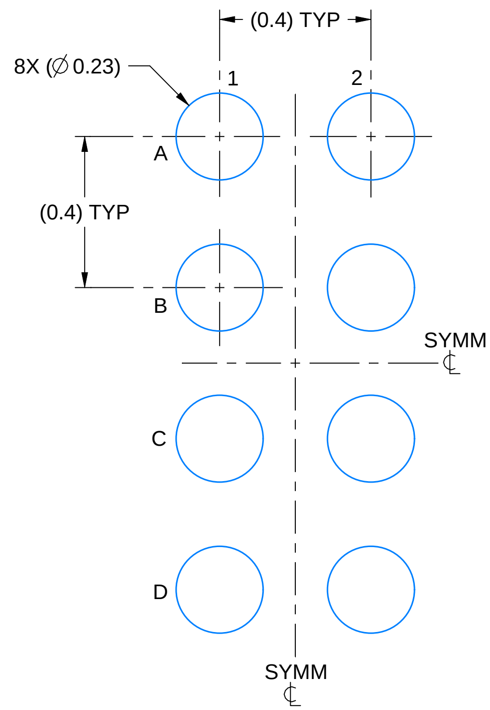
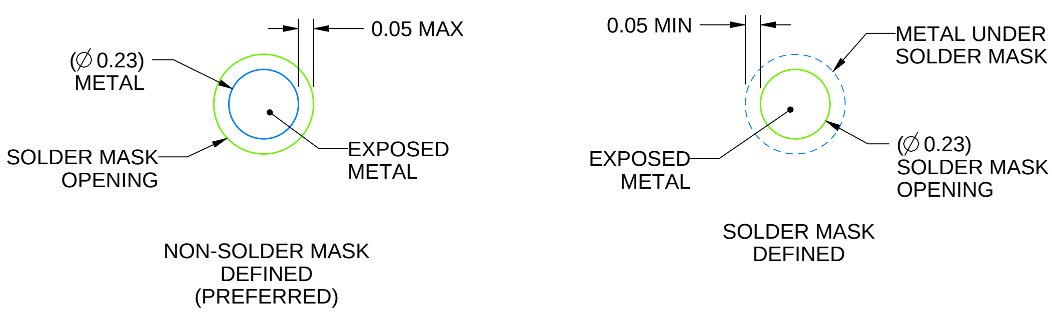


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

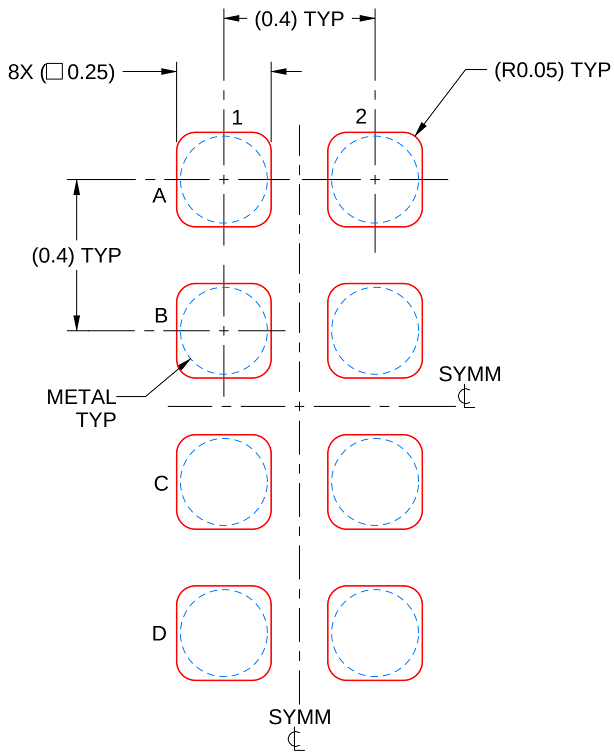


SOLDER MASK DETAILS
NOT TO SCALE

4224718/A 12/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4224718/A 12/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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