

# BQ77216 3~16 直列セル・リチウムイオン向け電圧／温度保護、内部遅延タイマ付き

## 1 特長

- 3 直列セルから 16 直列セルまでの保護
- 高精度過電圧保護
  - 25°Cで ±10mV
  - 0°C~60°Cで ±20mV
- 3.55V~5.1V の過電圧保護オプション
- 1.0V~3.5V の低電圧保護オプション
- 断線検出
- 過熱保護
- セルをランダムに接続可能
- 機能安全対応
- 固定の内部遅延タイマ
- 固定の検出スレッシュホルド
- 固定の出力駆動タイプ (COUT と DOUT のそれぞれ)
  - アクティブ HIGH またはアクティブ LOW
  - 6V へのアクティブ High 駆動
  - オープン・ドレイン、外部から VDD にプルアップ可能
- 低消費電力  $I_{CC} \approx 1\mu A$  ( $V_{CELL(ALL)} < V_{OV}$ )
- セル入力あたりのリーク電流: 100nA 未満 (断線検出が無効の場合)
- パッケージの占有面積オプション:
  - リード付きの 24 ピン TSSOP、0.65mm ピン・ピッチ

## 2 アプリケーション

- 次のものに使用されるリチウムイオン・バッテリー・パックの保護:
  - モバイル園芸用具
  - モバイル電動工具
  - コードレス掃除機
  - UPS バッテリー・バックアップ
  - 小型電動車両 (電動自転車、電動スクーター、ペダル・アシスト自転車)

## 3 概要

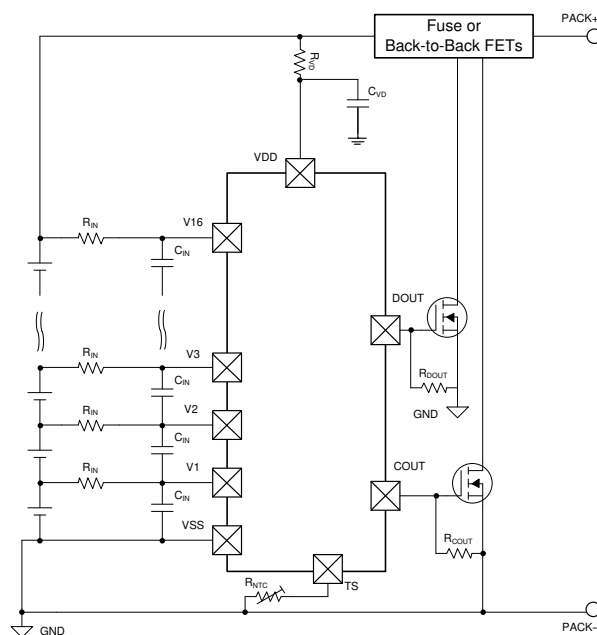
BQ77216 製品ファミリは、リチウムイオン バッテリー パックシステムに対する、過電圧 (OVP)、低電圧 (UVP)、断線 (OW)、および過熱 (OT) の保護など、電圧と温度に関する幅広い監視機能を提供します。各セルの過電圧、低電圧、断線条件を別々に監視できます。外部 NTC サーミスタを追加すると、本デバイスは過熱条件を検出できます。

BQ77216 デバイスでは、過電圧、低電圧、断線、過熱のいずれかの条件を検出すると、内部遅延タイマが起動します。遅延タイマが満了すると、各出力はアクティブ状態 (構成により HIGH または LOW) にトリガされます。

### 製品情報表

部品番号	パッケージ	本体サイズ (公称)
BQ7721600 <sup>(1)</sup>	TSSOP (24)	4.40mm × 7.80mm (6.40mm × 7.80mm、リード含む)

- (1) 利用可能なカタログ・パッケージについては、このデータシートの末尾にある注文情報および [Device Comparison Table](#) を参照してください。



概略回路図



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## 4 概要 (続き)

過電圧の場合はフォルトが検出されると COUT ピンがトリガされ、低電圧の場合はフォルトが検出されると DOUT ピンがトリガされます。過熱または断線フォルトが検出されると、DOUT と COUT の両方がトリガされます。生産ライン・テストを迅速に行えるよう、BQ77216 デバイスは遅延時間を大幅に短縮したカスタマ・テスト・モード (CTM) を備えています。

## 5 Device Comparison Table

表 5-1. BQ77216 Device Comparison

PART NUMBER	T <sub>A</sub>	PACKAGE	PACKAGE DESIGNATOR	OVP (V)	OV HYSTERESIS (V)	OVP DELAY	UVP (V)	UVP DELAY
BQ7721600	-40°C to 110°C	24-Pin TSSOP	PW	4.325	0.100	1 s	2.25	1 s
BQ7721602	-40°C to 110°C	24-Pin TSSOP	PW	4.325	0.100	1 s	2.25	1 s
BQ7721603	-40°C to 110°C	24-Pin TSSOP	PW	4.3	0.100	2 s	2	2 s
BQ7721605	-40°C to 110°C	24-Pin TSSOP	PW	4.225	0.100	1 s	2.6	1 s
BQ7721606	-40°C to 110°C	24-Pin TSSOP	PW	4.275	0.100	1 s	2.5	1 s
BQ7721607	-40°C to 110°C	24-Pin TSSOP	PW	4.25	0.100	4 s	2.5	2 s
BQ7721609	-40°C to 110°C	24-Pin TSSOP	PW	4.35	0.200	4 s	Disabled	
BQ7721610	-40°C to 110°C	24-Pin TSSOP	PW	4.25	0.100	4 s	2.5	2 s
BQ7721611	-40°C to 110°C	24-Pin TSSOP	PW	3.8	0.200	4 s	1.5	1 s
BQ7721612	-40°C to 110°C	24-Pin TSSOP	PW	3.6	0.200	2 s	2.0	2 s
BQ7721613	-40°C to 110°C	24-Pin TSSOP	PW	4.25	0.100	4 s	2.0	2 s
BQ7721614	-40°C to 110°C	24-Pin TSSOP	PW	3.9	0.100	4 s	1.85	2 s
BQ7721615	-40°C to 110°C	24-Pin TSSOP	PW	4.23	0.100	4 s	2.0	2 s
BQ7721616	-40°C to 110°C	24-Pin TSSOP	PW	4.18	0.100	4 s	2.0	2 s

表 5-2. BQ77216 Device Comparison (continued)

PART NUMBER	UV HYSTERESIS (V)	OTC (°C)	UTC (°C)	OW	LATCH	OUTPUT DRIVE	TAPE AND REEL
BQ7721600	0.100	70	NA	Enabled	Disabled	Active Low	BQ7721600PWR
BQ7721602	0.100	70	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721602PWR
BQ7721603	0.100	75	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721603PWR
BQ7721605	0.200	75	NA	Disabled	Disabled	Active High, 6-V Drive	BQ7721605PWR
BQ7721606	0.200	75	NA	Disabled	Disabled	Active High, 6-V Drive	BQ7721606PWR
BQ7721607	0.100	83	-30	Enabled	Disabled	Active High, 6-V Drive	BQ7721607PWR
BQ7721609	Disabled	83	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721609PWR
BQ7721610	0.100	83	NA	Enabled	Disabled	Active High, 6-V Drive (COUT) Active Low (DOUT)	BQ7721610PWR
BQ7721611	0.200	70	NA	Disabled	Disabled	Active High, 6-V Drive	BQ7721611PWR
BQ7721612	0.200	75	NA	Disabled	Disabled	Active Low	BQ7721612PWR
BQ7721613	0.200	83	-30	Enabled	Disabled	Active High, 6-V Drive	BQ7721613PWR
BQ7721614	0.100	75	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721614PWR
BQ7721615	0.200	83	-20	Disabled	Disabled	Active High, 6-V Drive	BQ7721615PWR
BQ7721616	0.200	80	-20	Disabled	Disabled	Active High, 6-V Drive	BQ7721616PWR

## 6 Pin Configuration and Functions

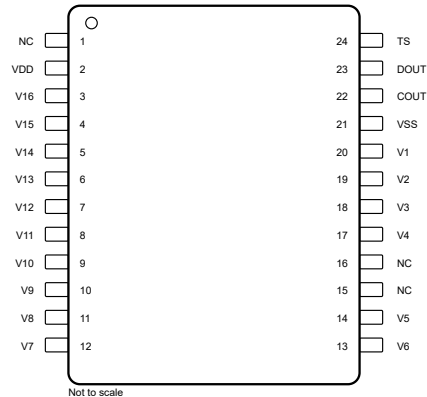


表 6-1. 24-Lead Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1	NC	—	Not electrically connected and can be left floating
2	VDD	P	Power supply
3	V16	I	Sense input for positive voltage of the sixteenth cell from the bottom of the stack
4	V15	I	Sense input for positive voltage of the fifteenth cell from the bottom of the stack
5	V14	I	Sense input for positive voltage of the fourteenth cell from the bottom of the stack
6	V13	I	Sense input for positive voltage of the thirteenth cell from the bottom of the stack
7	V12	I	Sense input for positive voltage of the twelfth cell from the bottom of the stack
8	V11	I	Sense input for positive voltage of the eleventh cell from the bottom of the stack
9	V10	I	Sense input for positive voltage of the tenth cell from the bottom of the stack
10	V9	I	Sense input for positive voltage of the ninth cell from the bottom of the stack
11	V8	I	Sense input for positive voltage of the eighth cell from the bottom of the stack
12	V7	I	Sense input for positive voltage of the seventh cell from the bottom of the stack
13	V6	I	Sense input for positive voltage of the sixth cell from the bottom of the stack
14	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
15	NC	—	Not electrically connected and can be left floating
16	NC	—	Not electrically connected and can be left floating
17	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
18	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
19	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
20	V1	I	Sense input for positive voltage of the lowest cell in the stack
21	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
22	COUT	O	Output drive for overvoltage, open wire, undertemperature, and overtemperature. It can be left floating if not used.
23	DOUT	O	Output drive for undervoltage, open wire, undertemperature, and overtemperature. It can be left floating if not used.
24	TS	I	Temperature sensor input. If not used, connect it with a 10-kΩ resistor to VSS.

I = Input, O = Output, P = Power Connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VDD – VSS	–0.3	85	V
Input voltage range	Vn – VSS where n = 1 to 16	–0.3	85	V
	TS	–0.3	1.5	V
Output voltage range	COUT – VSS, DOUT – VSS	–0.3	85	V
Functional temperature, T <sub>FUNC</sub>		–40	110	°C
Storage temperature, T <sub>STG</sub>		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage <sup>(1)</sup>	5		75	V
V <sub>IN</sub>	Input voltage range of Vn - Vn-1 where n = 2 to 16 and V1 - VSS	0		5	V
	TS	0		1.5	V
V <sub>CTM</sub>	Customer Test Mode Entry V <sub>DD</sub> > V16 + V <sub>CTM</sub>	12		13	V
C <sub>TS</sub>	Total capacitance on the TS Pin			200	pF
T <sub>A</sub>	Ambient temperature	–40		85	°C
T <sub>J</sub>	Junction temperature	–65		150	°C

- (1) V<sub>DD</sub> is equal to top of stack voltage

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DEVICE	UNIT
		PW (TSSOP)	
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.7	°C/W

## 7.4 Thermal Information (続き)

THERMAL METRIC <sup>(1)</sup>		DEVICE		
		PW (TSSOP)		
		24 PINS		
UNIT				
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 DC Characteristics

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 58\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  to  $75\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OVER VOLTAGE PROTECTION (OV)</b>						
$V_{OV}$	OV Detection Range		3.55		5.1	V
$V_{OV\_STEP}$	OV Detection Steps			25		mV
$V_{OV\_HYS}$	OV Detection Hysteresis	Selected OV Hysteresis depends on the part number. See the device selection table for details.		$V_{OV} - 100$		mV
		Selected OV Hysteresis depends on the part number. See the device selection table for details.		$V_{OV} - 200$		mV
$V_{OV\_ACC}$	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
	OV Detection Accuracy	$0^\circ\text{C} \leq T_A \leq 60^\circ\text{C}$	-20		20	mV
	OV Detection Accuracy	$-40^\circ\text{C} \leq T_A \leq 110^\circ\text{C}$	-50		50	mV
<b>UNDER VOLTAGE PROTECTION (UV)</b>						
$V_{UV}$	UV Detection Range		1.0		3.5	V
$V_{UV\_STEP}$	UV Detection Steps			50		mV
$V_{UV\_HYS}$	UV Detection Hysteresis	Selected UV Hysteresis depends on the part number. See the device selection table for details.		$V_{UV} + 100$		mV
		Selected UV Hysteresis depends on the part number. See the device selection table for details.		$V_{UV} + 200$		mV
$V_{UV\_ACC}$	UV Detection Accuracy	$T_A = 25^\circ\text{C}$	-30		30	mV
	UV Detection Accuracy	$-40 \leq T_A \leq 110^\circ\text{C}$	-50		50	mV
$V_{UV\_MIN}$	UV Detection Disabled Threshold	$V_n - V_{n-1}$ where $n = 2$ to $16$ and $V_1 - V_{SS}$	450	500	550	mV
<b>OVER TEMPERATURE PROTECTION (OT)</b>						
$T_{OT}$	OT Detection Range	Available options: $62^\circ\text{C}$ , $65^\circ\text{C}$ , $70^\circ\text{C}$ , $75^\circ\text{C}$ , $80^\circ\text{C}$ , $83^\circ\text{C}$	62.0		83.0	°C
$R_{OT\_EXT}$	OT Detection External Resistance	$62^\circ\text{C}$		2850		$\Omega$
		$65^\circ\text{C}$		2570		
		$70^\circ\text{C}$		2195		
		$75^\circ\text{C}$		1915		
		$80^\circ\text{C}$		1651		
		$83^\circ\text{C}$		1525		
$T_{OT\_ACC}^{(1)}$	OT Detection Accuracy		-5		5	°C

## 7.5 DC Characteristics (続き)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 58\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  to  $75\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{OT\_HYS}$ (2)	OT Detection Hysteresis			-10		$^\circ\text{C}$
				4186		$\Omega$
				3530		$\Omega$
$R_{NTC}$	Internal Pullup Resistor	After TI Factory Trim	19.5	20	20.6	$\text{k}\Omega$
<b>OPEN WIRE PROTECTION (OW)</b>						
$V_{OW}$	OW Detection Threshold	$V_n < V_{n-1}$ where $n = 2$ to $16$		-200		mV
		$V_1 - V_{SS}$		500		mV
$V_{OW\_HYS}$	OW Detection Hysteresis	$V_n < V_{n-1}$ where $n = 1$ to $16$		$V_{OW} + 100$		mV
$V_{OW\_ACC}$	OW Detection Accuracy	$-40^\circ\text{C} \leq T_A \leq 110^\circ\text{C}$	-25		25	mV
<b>SUPPLY AND LEAKAGE CURRENT</b>						
$I_{CC}$	Supply Current	No fault detected		2	3.5	$\mu\text{A}$
$I_{IN}$ (2)	Input Current at $V_x$ Pins	$V_n - V_{n-1}$ and $V_1 - V_{SS} = 4\text{ V}$ , where $n = 2$ to $16$ , Open Wire Enabled	-0.3		0.3	$\mu\text{A}$
		$V_n - V_{n-1}$ and $V_1 - V_{SS} = 4\text{ V}$ , where $n = 2$ to $16$ , Open Wire Disabled	-0.1		0.1	$\mu\text{A}$
<b>OUTPUT DRIVE, COUT and DOUT, CMOS ACTIVE HIGH VERSIONS ONLY</b>						
$V_{OUT\_AH}$	Output Drive Voltage for COUT and DOUT, Active High 6V	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $I_{OH} = 100\ \mu\text{A}$ measured out of COUT, DOUT pin	6			V
	Output Drive Voltage for COUT and DOUT, Active High VDD	$V_{DD} - V_{COUT}$ or $V_{DOUT}$ , $V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$ , where $n = 2$ to $16$ , $I_{OH} = 10\ \mu\text{A}$ measured out of COUT, DOUT pin	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V	$V_{DD} - V_{COUT}$ or $V_{DOUT}$ , if 15 of 16 cells are short-circuited and only one cell remains powered and $> V_{OV}$ , $V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\ \mu\text{A}$ ,	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V and VDD	$V_n - V_{n-1}$ and $V_1 - V_{SS} < V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $I_{OH} = 100\ \mu\text{A}$ measured into pin		250	400	mV
$R_{OUT\_AH}$	Internal Pullup Resistor		80	100	120	$\text{k}\Omega$
$I_{OUT\_AH\_H}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $\text{OUT} = 0\text{ V}$ . Measured out of COUT, DOUT pin			4.5	mA
$I_{OUT\_AH\_L}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V_1 - V_{SS} < V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $\text{OUT} = V_{DD}$ . Measured into COUT, DOUT pin	0.3		3	mA
<b>OUTPUT DRIVE, COUT and DOUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY</b>						
$V_{OUT\_AL}$	Output Drive Voltage for COUT and DOUT, Active Low	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $I_{OH} = 100\ \mu\text{A}$ measured into COUT, DOUT pin		250	400	mV
$I_{OUT\_AL\_L}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V_1 - V_{SS} > V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $\text{OUT} = V_{DD}$ . Measured into COUT, DOUT pin	0.3		3	mA
$I_{OUT\_AL\_H}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V_1 - V_{SS} < V_{OV}$ , where $n = 2$ to $16$ , $V_{DD} = 58\text{ V}$ , $\text{OUT} = V_{DD}$ . Measured out of COUT, DOUT pin			100	nA

(1) Assured by Design. This accuracy assumes the external resistance is within  $\pm 2\%$  of the  $R_{OT\_EXT}$  values for the corresponding temperature threshold.

(2) Assured by Design

## 7.6 Timing Requirements

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 58\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  to  $85\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OV\_DELAY}$	OV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
				4		s
$t_{UV\_DELAY}$	UV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
$t_{OT\_DELAY}$	OT Delay Time		4		s	
$t_{OW\_DELAY}$	OW Delay Time		4		s	
$t_{DELAY\_ACC}$	Delay Time Accuracy	For 0.25-s, 0.5-s delays	-128		128	ms
$t_{DELAY\_ACC}$	Delay Time Accuracy	For 1-s delays	-150		150	ms
$t_{DELAY\_DR}$	Delay time drift across operating temp	For all delays other than 0.25-s, 0.5-s, 1-s delays	-10%		10%	
$t_{CTM\_DELAY}$	Fault Detection Delay Time during Customer Test Mode	See Customer Test Mode.		50		ms



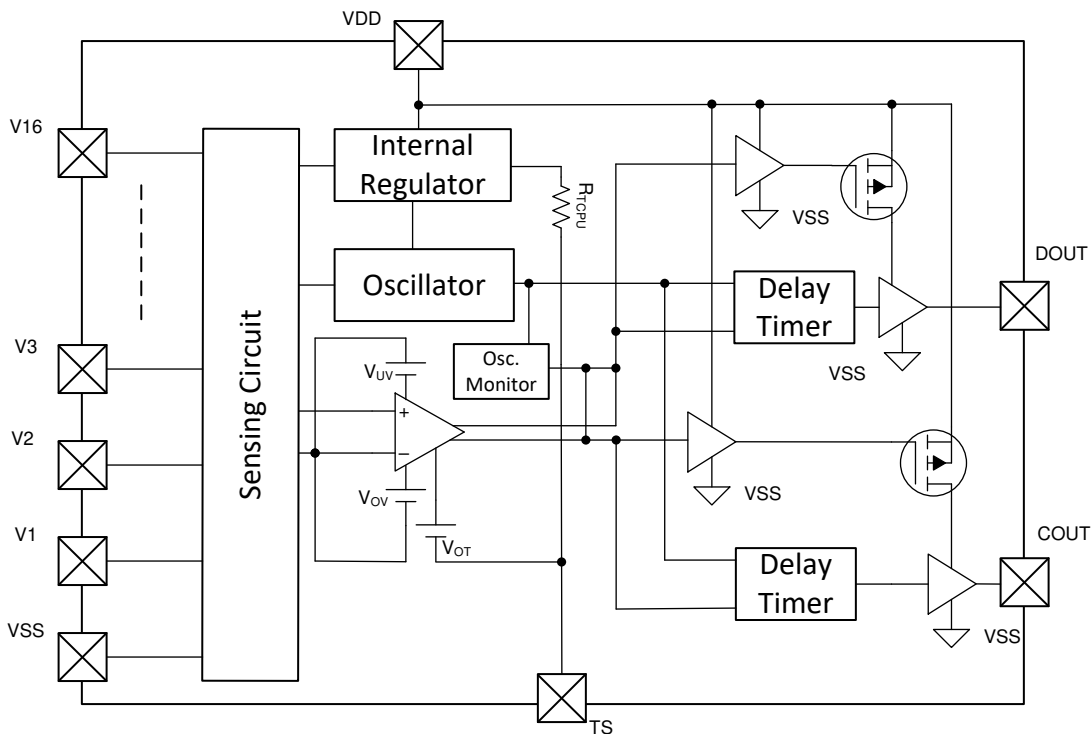
## 8 Detailed Description

### 8.1 Overview

The BQ77216 family of devices provides a range of voltage and temperature monitoring including overvoltage (OVP), undervoltage (UVP), open wire (OW), and overtemperature (OT) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, undervoltage, and open-wire conditions. With the addition of an external NTC thermistor, the device can detect overtemperature conditions. An internal delay timer is initiated upon detection of an overvoltage, undervoltage, open-wire, or overtemperature condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low, depending on the configuration). The overvoltage triggers the COUT pin if a fault is detected, and undervoltage triggers the DOUT pin if a fault is detected. If an undertemperature, overtemperature, or open-wire fault is detected, then both the DOUT and COUT are triggered.

For quicker production-line testing, the BQ77216 device provides a Customer Test Mode (CTM) with greatly reduced delay time.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Voltage Fault Detection

In the BQ77216 device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{OV}$ . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the COUT pin goes from inactive to active state. The timer is reset if the cell voltage falls below the recovery threshold ( $V_{OV} - V_{OV\_HYS}$ ). Undervoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{UV}$ . If any cell voltage falls below the programmed UV value, a timer circuit is activated. When the timer expires, the DOUT pin goes from inactive to active state. The timer is reset if the cell voltage rises below the recovery threshold ( $V_{UV} + V_{UV\_HYS}$ ).

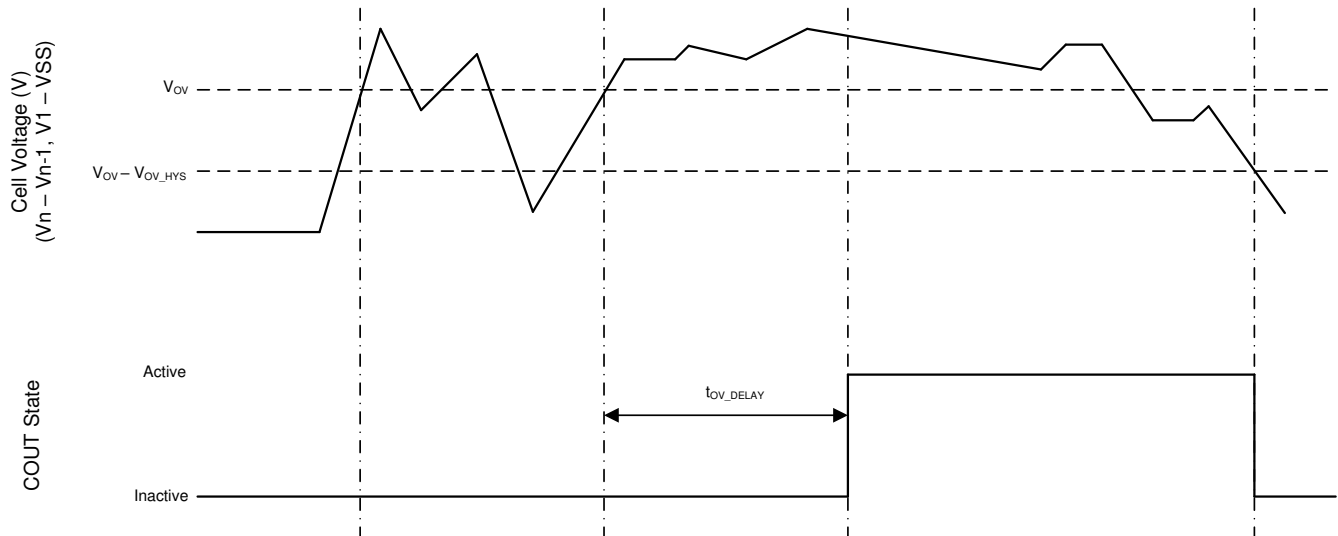


図 8-1. Timing for Overvoltage Sensing

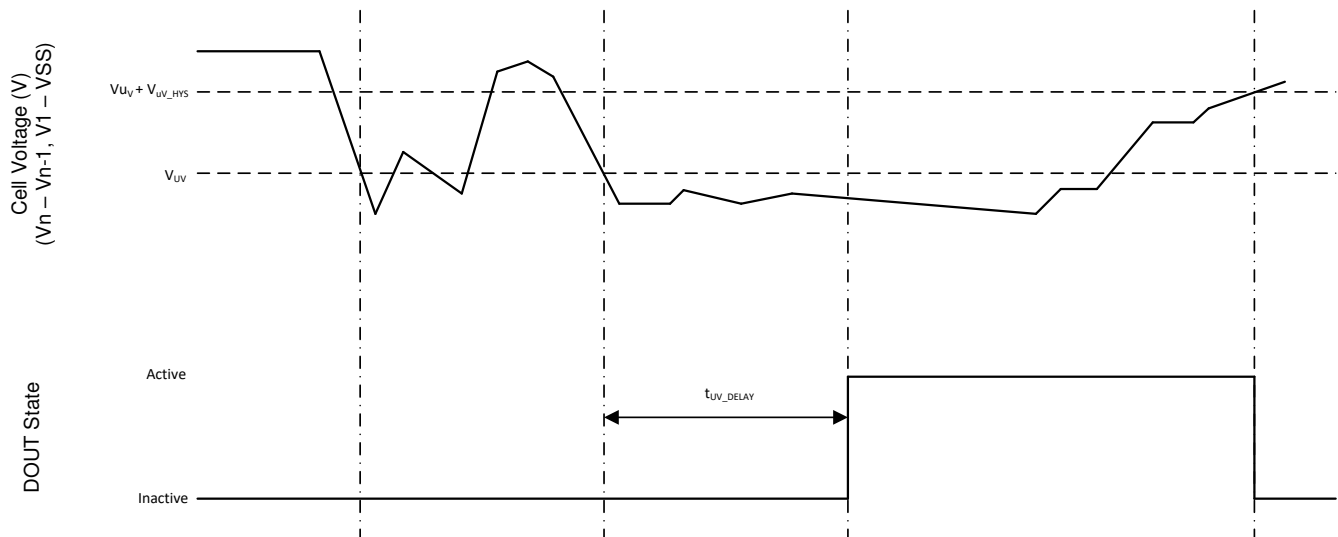


図 8-2. Timing for Undervoltage Sensing

### 8.3.2 Open-Wire Fault Detection

In the BQ77216 device, each cell input is monitored independently to determine if the input is connected to a cell or not by applying a 50- $\mu$ A pull down current to ground that is activated for 128  $\mu$ s every 128 ms. If the device detects that  $V_n < V_{n-1} - V_{OW}$  V, then a timer is activated. When the timer expires, the COUT and DOUT pins go from an inactive to active state. The timer is reset if the cell input rises above or below the recovery threshold ( $V_{OW} + V_{OW\_HYS}$ ).

### 8.3.3 Temperature Fault Detection

In the BQ77216 device, the TS pin is ratiometrically monitored with an internal pullup resistance  $R_{NTC}$ . Overtemperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance,  $R_{OT\_EXT}$ . If the resistance falls below the programmed OT value, a timer circuit is activated. When the timer expires, the COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance rises above the recovery threshold ( $R_{OT} + R_{OT\_HYS}$ ). Under temperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance,  $R_{UT\_EXT}$ . If the resistance rises above the programmed UT value, a timer circuit is activated. When the timer expires, the

COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance falls below above the recovery threshold ( $R_{OT} - R_{OT\_HYS}$ ) If external capacitance is added to the TS pin, it needs to be within the spec limit shown in recommended operating conditions.

注

Texas Instruments does not recommend adding an external capacitor to the TS pin. The capacitance on this pin will affect the TS measurement accuracy if greater than  $C_{TS}$ .

### 8.3.4 Oscillator Health Check

The device can detect if the internal oscillator slows down below the  $f_{OSC\_FAULT}$  threshold. When this occurs then the COUT and DOUT go from inactive to active state. If the oscillator returns to normal then the fault recovers.

### 8.3.5 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input are required for noise filtering and stable voltage monitoring.

### 8.3.6 Output Drive, COUT and DOUT

These pins serve as the fault signal outputs and may be ordered in either active HIGH with drive to 6 V or active LOW options configured through internal OTP.

The COUT and DOUT respond per the following table when a fault is detected if the specific fault is enabled.

表 8-1. Fault Detection vs COUT and DOUT Action

FAULT Detected	COUT	DOUT
Overvoltage	Active	Inactive
Undervoltage	Inactive	Active
Open Wire	Active	Active
Overtemperature	Active	Active
Oscillator Health	Active	Active

### 8.3.7 The LATCH Function

The device can be enabled to latch the fault signal, which effectively disables the recovery functions of all fault detections. The only way to recover from a fault state when the latch is enabled is a POR of the device.

### 8.3.8 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

## 8.4 Device Functional Modes

### 8.4.1 NORMAL Mode

When COUT and DOUT are inactive (no fault detected), the device operates in NORMAL mode and monitors for voltage, open-wire, and temperature faults.

The COUT and DOUT pins are inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

### 8.4.2 FAULT Mode

FAULT mode is entered if the COUT or DOUT pins are activated. The OUT pin is either pulled high internally if configured as active high or is pulled low internally if configured as active low. When COUT and DOUT are deactivated, the device returns to NORMAL mode.

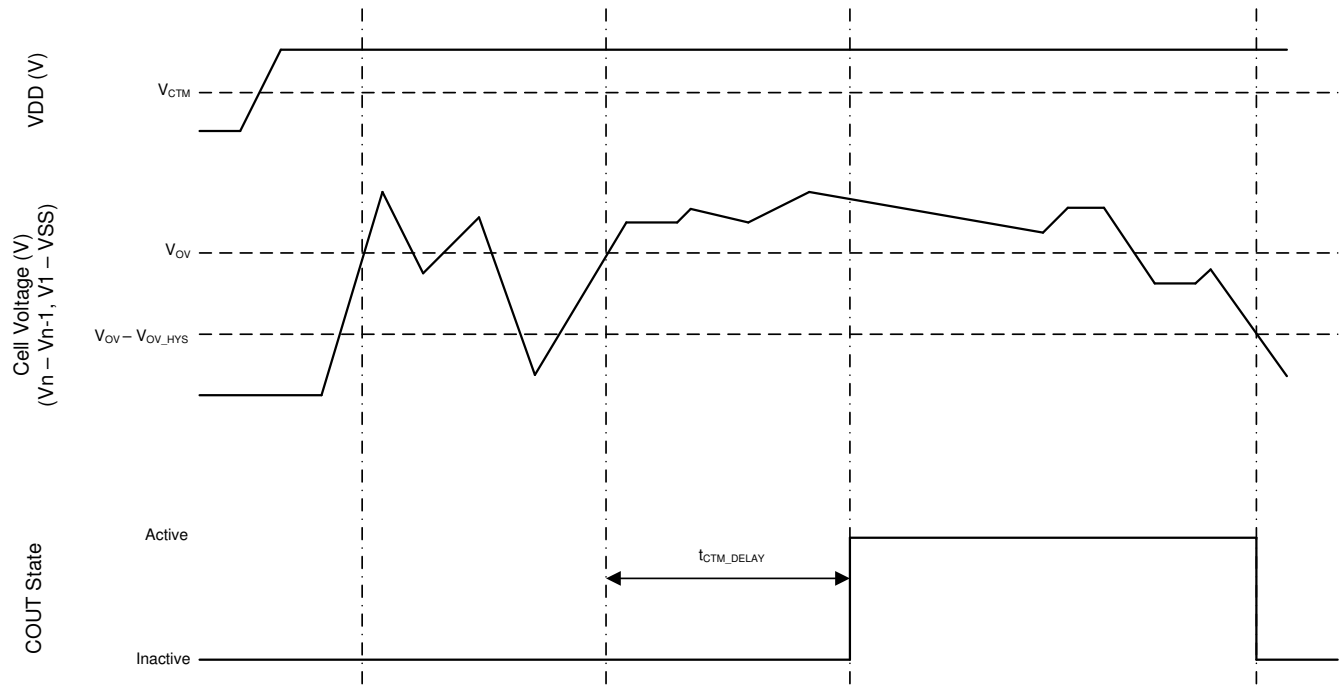
### 8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least  $V_{CTM}$  higher than V16 (see [Figure 8-3](#)). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V16 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

#### 注意

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages ( $V_{Cn}-V_{Cn-1}$ ) and ( $V1-VSS$ ). Stressing the pins beyond the rated limits may cause permanent damage to the device.

[Figure 8-3](#) shows the timing for the Customer Test Mode.



**Figure 8-3. Timing for Customer Test Mode**

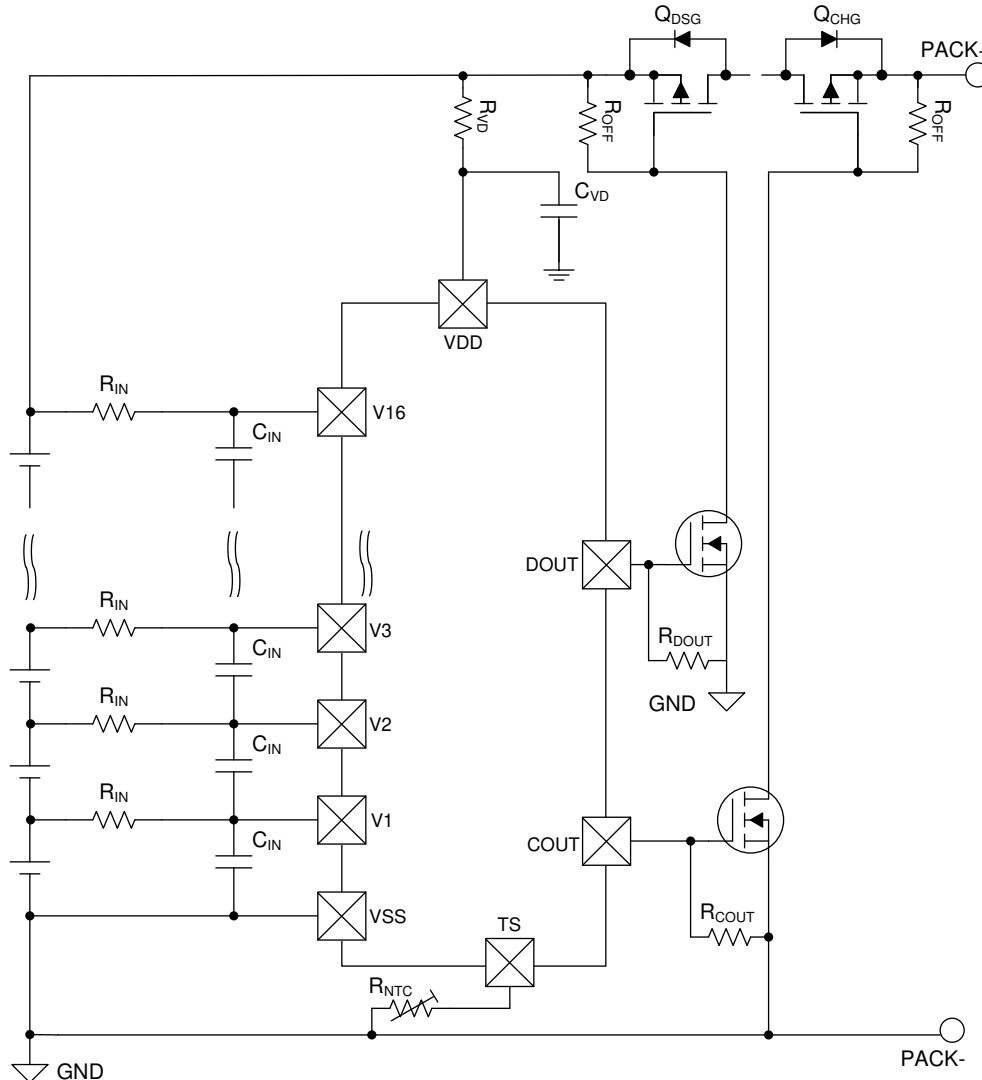
## 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements.



9-1. Application Configuration

#### 9.1.1 Design Requirements

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements. 9-1 shows each external component.

表 9-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	$R_{IN}$	900	1000	1100	$\Omega$
Voltage monitor filter capacitance	$C_{IN}$	0.01		0.1	$\mu\text{F}$
Supply voltage filter resistance	$R_{VD}$	100	300	1K	$\Omega$
Supply voltage filter capacitance	$C_{VD}$	0.05	0.1	1	$\mu\text{F}$

## 注

The device is calibrated using an  $R_{IN}$  value = 1 k $\Omega$ . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and  $V_{OV}$  trigger level.

## 9.1.2 Detailed Design Procedure

図 9-2 shows the measurement for current consumption for the product for both VDD and Vx.

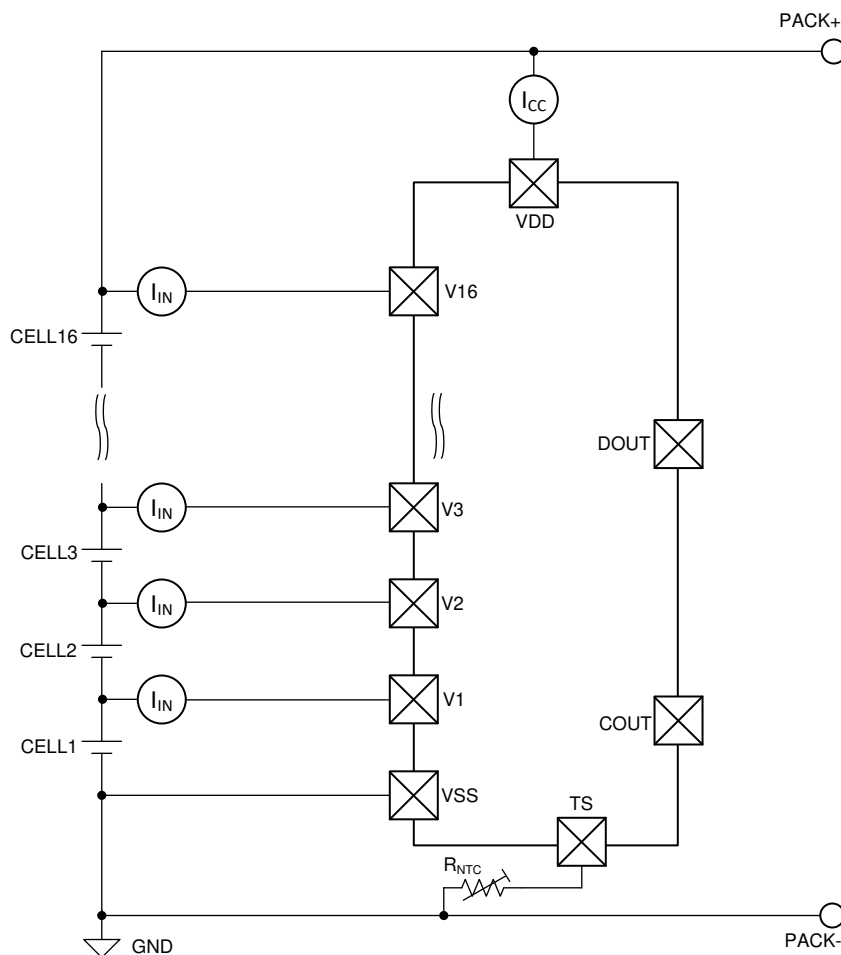


図 9-2. Configuration for IC Current Consumption Test

## 9.1.2.1 Cell Connection Sequence

The BQ77216 device can be connected to the array of cells in any order without damaging the device.

During cell attachment, the device could detect a fault if the cells are not connected within a fault detection delay period. If this occurs, then COUT and/or DOUT could transition from inactive to active. Both COUT and DOUT can be tied to VSS or VDD to prevent any change in output state during cell attach.

## 9.2 Systems Example

In this application example, the choice of a FUSE or FETs is required on the COUT and DOUT pins—configured as an active-high drive to 6-V outputs.

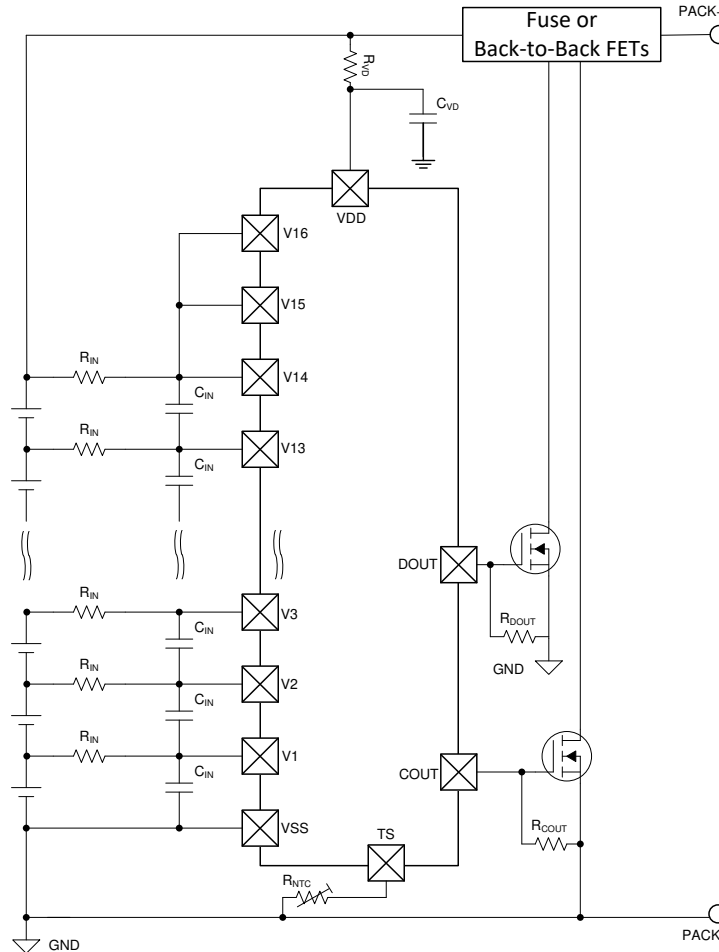
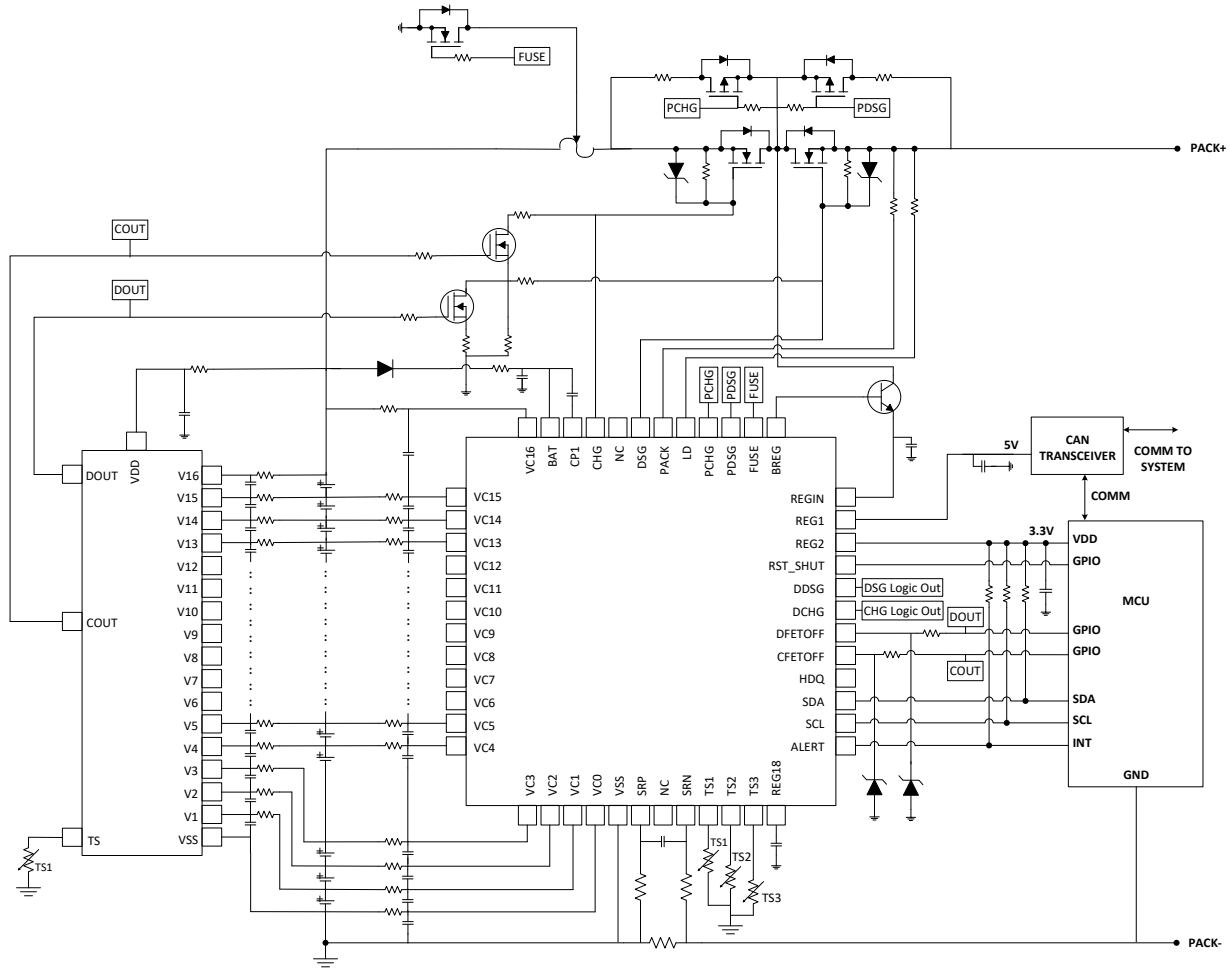


図 9-3. 14-Series Cell Configuration with Active High 6-V Option

When pairing with the BQ769x2 or BQ76940 devices, the top cell must be used. For the BQ77216 device to drive the CHG and DSG FETs, the active high 6-V option is preferred. Its COUT and DOUT are controlling two N-CH FETs to jointly control the CHG and DSG FETs with the monitoring device. For such joint architecture, the open-wire feature of the BQ77216 device may be affected if the primary protector or monitor device is actively measuring the cells. Care is needed to ensure the  $V_{OW}$  spec of the BQ77216 device is met or to choose a version of the BQ77216 device with open wire disabled. When working with a BQ769x2 device, set the LOOP\_SLOW to 0x11 to ensure the BQ77216  $V_{OW}$  spec is met.





**9-4. BQ77216 with BQ76952**

## 10 Power Supply Recommendations

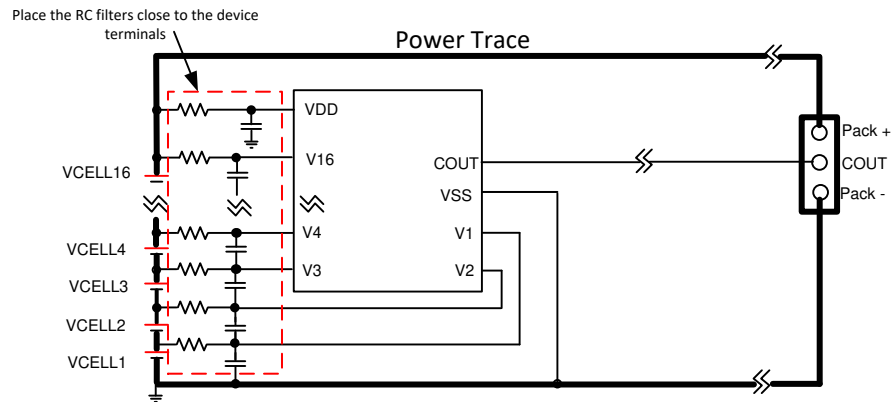
The maximum power supply of this device is 85 V on VDD.

## 11 Layout

### 11.1 Layout Guidelines

- Ensure the RC filters for the Vn and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL– terminal.

### 11.2 Layout Example



☒ 11-1. Example Layout

## 12 Device and Documentation Support

### 12.1 サード・パーティ製品に関する免責事項

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### 12.2 ドキュメントの更新通知を受け取る方法

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### 12.3 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの [使用条件](#) を参照してください。

### 12.4 Trademarks

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (July 2023) to Revision J (November 2023)	Page
• Updated the <a href="#">Device Comparison Table</a> .....	3
• Updated the TS pin description.....	4
• Added the undertemperature protection description.....	10
Changes from Revision H (March 2023) to Revision I (July 2023)	Page
• Updated the <a href="#">Device Comparison Table</a> .....	3
Changes from Revision G (July 2022) to Revision H (March 2023)	Page
• Updated the <a href="#">Device Comparison Table</a> .....	3

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7721600PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721600	<a href="#">Samples</a>
BQ7721602PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721602	<a href="#">Samples</a>
BQ7721603PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721603	<a href="#">Samples</a>
BQ7721605PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721605	<a href="#">Samples</a>
BQ7721606PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721606	<a href="#">Samples</a>
BQ7721607PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721607	<a href="#">Samples</a>
BQ7721609PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721609	<a href="#">Samples</a>
BQ7721610PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721610	<a href="#">Samples</a>
BQ7721611PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721611	<a href="#">Samples</a>
BQ7721612PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721612	<a href="#">Samples</a>
BQ7721613PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721613	<a href="#">Samples</a>
BQ7721614PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721614	<a href="#">Samples</a>
BQ7721615PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721615	<a href="#">Samples</a>
BQ7721616PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721616	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7721600PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721602PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721603PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721605PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721606PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721607PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721609PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721610PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721611PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721612PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721613PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721614PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721615PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721616PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7721600PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721602PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721603PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721605PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721606PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721607PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721609PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721610PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721611PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721612PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721613PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721614PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721615PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721616PWR	TSSOP	PW	24	2000	356.0	356.0	35.0



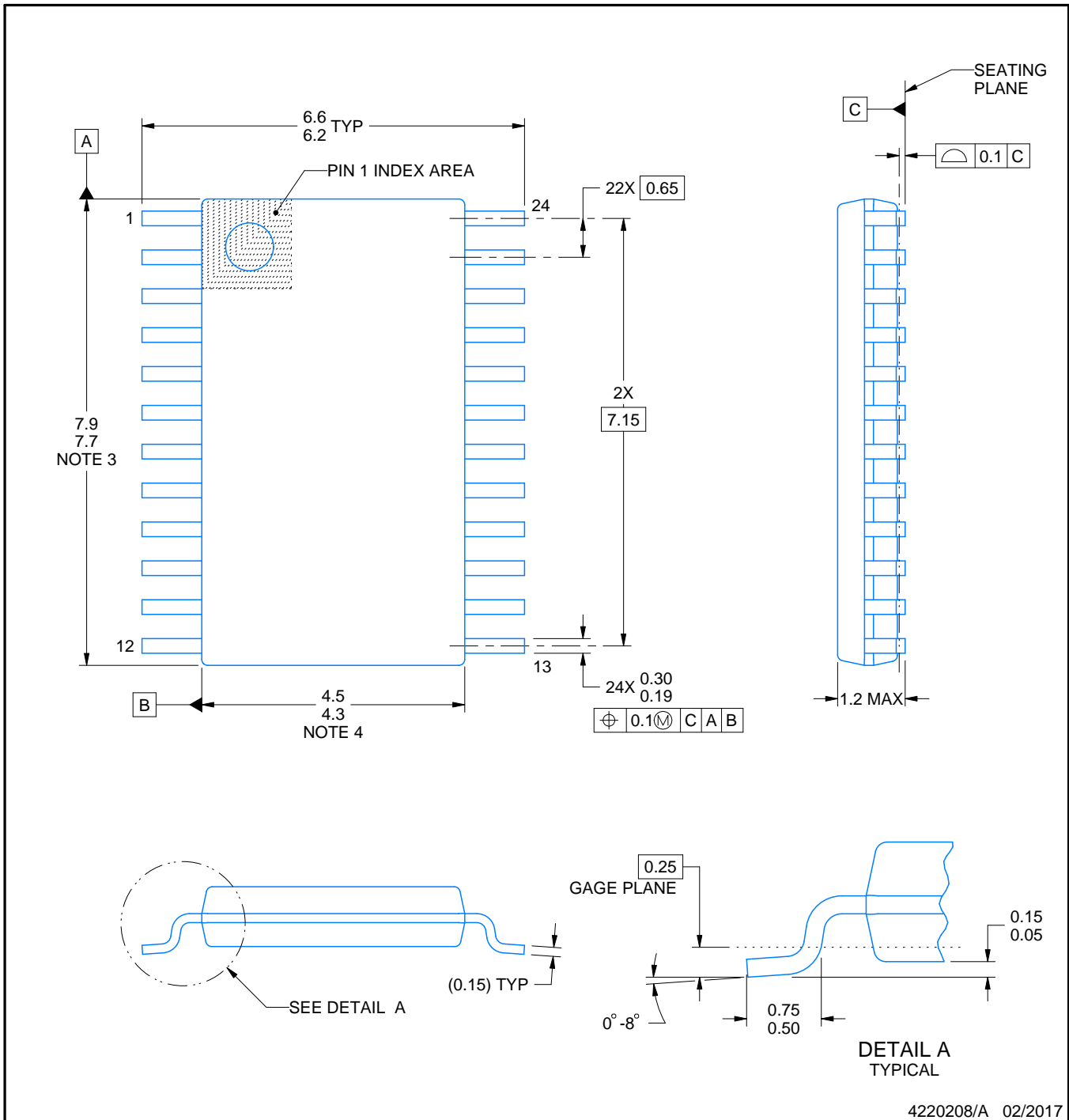
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

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