CC2340R5-Q1 SimpleLink™ Bluetooth® 5.3 Low Energy ワイヤレス MCU

1 特長

ワイヤレス マイクロコントローラ

- 車載アプリケーション用に AEC-Q100 グレード 2 認定済み
- 最適化された 48MHz Arm® Cortex®-M0+ プロセッサ
- 512KB のインシステム プログラマブル フラッシュ
- ブートローダーおよびドライバ用の 12KB の ROM
- 36KB の超低リーク SRAM。スタンバイ モードでの RAM の完全保持
- Bluetooth® 5.3 Low Energy と互換性のある 2.4GHz RF トランシーバ
- バラン内蔵
- OTA (Over-The-Air) アップグレードに対応
- SWD (Serial Wire Debug)

低い消費電力

- MCU の消費電流:
  - 2.6mA (アクティブ モード、CoreMark®)
  - 53µA/MHz (CoreMark® 実行中)
  - 710nA 未満のスタンバイ モード、RTC、36KB RAM
  - 165nA (シャットダウン モード、ウェイクアップ オンピン)
- 無線の消費電流:
  - 5.3mA (RX)
  - 5.1mA (TX、0dBm)
  - 11.0mA 未満 (TX、+8dBm)

無線プロトコルのサポート

- Bluetooth® 5.3 Low Energy

高性能の無線

- -102dBm (Bluetooth® Low Energy、125kbps)
- -96.5dBm (Bluetooth® Low Energy、1Mbps)
- 温度補償付きで最大 +8dBm の出力電力

法規制の順守

- 以下の規格への準拠を目的としたシステムに最適:
  - EN 300 328 (ヨーロッパ)
  - FCC CFR47 Part 15
  - ARIB STD-T66 (日本)

MCU のペリフェラル

- 19 個の I/O パッド
  - 2 つの IO パッド SWD、GPIO と多重化
  - 2 つの IO パッド LFXT、GPIO と多重化
  - 15 個の DIO (アナログまたはデジタル IO)
- 3 × 16 ビットおよび 1 × 24 ビット汎用タイマ、直交デコード モードをサポート
- 12 ビット ADC、1.2Msps、外部リファレンス付き、267ksps、内部リファレンス付き、8 個の外部 ADC 入力
- 1 つの低消費電力コンパレータ
- 1 つの UART
- 1 つ の SPI
- 1 つの I^2C
- リアルタイム クロック (RTC)
- 温度およびバッテリ モニタを内蔵
- ウォッチドッグ タイマ

セキュリティを実現する機能

- AES 128 ビット暗号化アクセラレータ
- オンチップ アナログ ノイズからの乱数発生器

開発ツールとソフトウェア

- LP-EM-CC2340R5 LaunchPad 開発キット
- SimpleLink™ CC23xx ソフトウェア開発キット (SDK)
- SmartRF™ Studio による容易な無線構成
- SysConfig システム コンフィギュレーション ツール

動作範囲

- オンチップの降圧型 DC/DC コンバータ
- 1.71V～3.8V の単一電源電圧
- T_j:-40～+125°C
- HBM ESD 分類レベル 2
- CDM ESD 分類レベル C3

RoHS 準拠のパッケージ

- ウェッタブル フランク付き 5mm × 5mm RHB QFN32 (19 GPIO)

2 アプリケーション

- 車載用
  - カー アクセスとセキュリティ システム
    - パッシブ エントリ パッシブ スタート (PEPS)
    - リモート キーレス エントリ (RKE)
  - 先進運転支援システム (ADAS)
  - タイヤ空気圧監視システム (TPMS)

3 概要

SimpleLink™ CC2340R5-Q1 デバイスは、Bluetooth 5 Low Energy 車載用アプリケーションを対象とした AEC-Q100 準拠のワイヤレス マイクロコントローラ (MCU) です。このデバイスは、タイヤ空気圧監視システム (TPMS) や、パッシブ エントリ パッシブ スタート (PEPS) で使用されるキー フォブを含むカー アクセスなどのアプリケーションで低消費電力のワイヤレス通信に最適化されており、やリモート キーレス エントリ (RKE)、ケーブルの代替、スマートフォンの接続をサポートします。このデバイスの主な機能は次のとおりです。

- 以下の Bluetooth® 5 機能に対応ハイ スピード モード (2Mbps PHY)、長距離 (LE コードの 125kbps および 500kbps PHY)、Privacy 1.2.1 およびチャネル選択アルゴリズム #2、および Bluetooth® 4.2 およびそれ以前の Low Energy 仕様の主要機能に対する下位互換性とサポート。
- SimpleLink™ CC23xx ソフトウェア開発キット (SDK) に含まれる、完全認定済み Bluetooth® 5.3 ソフトウェア プロトコル スタック。
- RTC が動作し、RAM 全体を保持しながら 0.71µA 未満の超低スタンバイ電流により、特にスリープ時間が長いアプリケーションで、バッテリ駆動時間を大幅に延長できます。
- バルンを内蔵して基板レイアウトの部品表 (BOM) を削減。
- Bluetooth® Low Energy での優れた無線感度と堅牢性 (選択度、ブロッキング) 性能 (バランを内蔵し、125kbps の LE Coded PHY で -102dBm)。

CC2340R5-Q1 デバイスは SimpleLink™ MCU プラットフォームに属しています。本プラットフォームは、シングル コア SDK (ソフトウェア開発キット) と豊富なツール セットを備えた使いやすい共通の開発環境を共有する Wi-Fi®、*Bluetooth* Low Energy、Thread、Zigbee、Sub-1GHz MCU、ホスト MCU で構成されています。SimpleLink™ プラットフォームは一度で統合を実現でき、製品ラインアップのどのデバイスの組み合わせでも設計に追加できるので、設計要件変更の際もコードの 100% 再利用が可能です。詳細については、SimpleLink™ MCU プラットフォームを参照してください。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)
CC2340R52E0WRHBRQ1	QFN32	5.00mm × 5.00mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については、セクション 12 のパッケージ オプションに関する付録、または テキサス・インスツルメンツの Web サイトを参照してください。

4 機能ブロック図

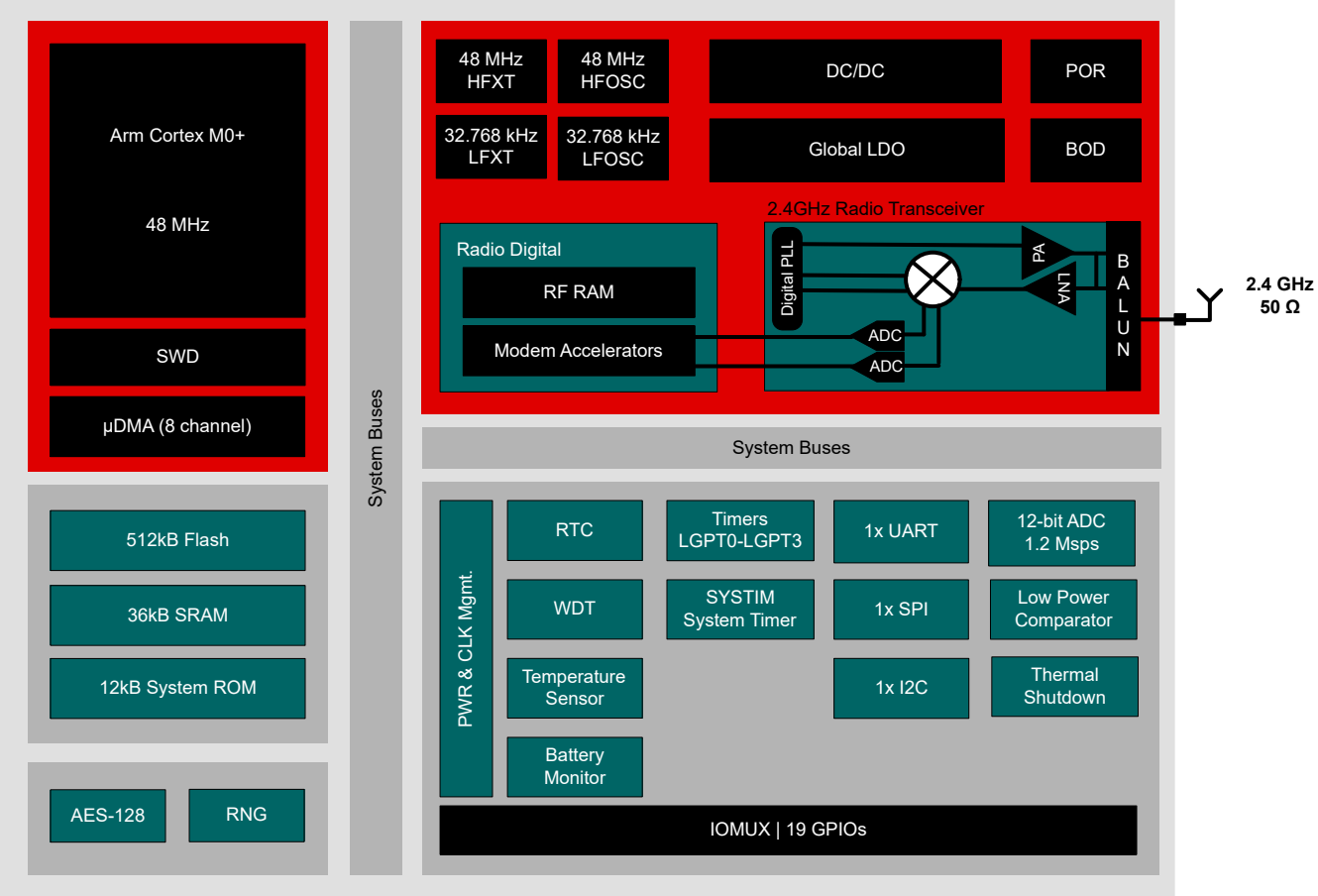

図 4-1. CC2340R5-Q1 ブロック図

Table of Contents

5 Device Comparison

Device	RADIO SUPPORT											FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE					
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	mioty	Wi-SUN®	Sidewalk	*Bluetooth*® LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 X 4 mm VQFN (24)	4 X 4 mm VQFN (32)	5 X 5 mm VQFN (32)	5 X 5 mm VQFN (40)	7 X 7 mm VQFN (48)	8 X 8 mm VQFN (64)
CC1310	X		X	X								32-128	16-20 + 8	10-30		X	X		X	
CC1311R3	X		X	X								352	32 + 8	22-30				X	X	
CC1311P3	X		X	X							X	352	32 + 8	26					X	
CC1312R	X		X	X	X							352	80 + 8	30					X	
CC1312R7	X		X	X	X	X				X		704	144 + 8	30					X	
CC1314R10	X		X	X	X	X				X		1024	256 + 8	30-46					X	X
CC1352R	X	X	X	X	X		X	X	X	X		352	80 + 8	28					X	
CC1354R10	X	X	X	X	X		X	X	X	X		1024	256 + 8	28-42					X	X
CC1352P	X	X	X	X	X		X	X	X	X	X	352	80 + 8	26					X	
CC1352P7	X	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26					X	
CC1354P10	X	X	X	X	X	X	X	X	X	X	X	1024	256 + 8	26-42					X	X
CC2340R2[(1)]		X					X	X				256	28	12	X					
CC2340R5[(2)]		X					X	X	X			512	36	12-26	X			X		
CC2340R5-Q1							X					512	36	19			X			
CC2640R2F							X					128	20 + 8	10-31		X	X		X	
CC2642R							X					352	80 + 8	31					X	
CC2642R-Q1							X					352	80 + 8	31					X	
CC2651R3		X					X	X				352	32 + 8	23-31				X	X	
CC2651P3		X					X	X			X	352	32 + 8	22-26				X	X	
CC2652R		X					X	X	X	X		352	80 + 8	31					X	
CC2652RB		X					X	X	X	X		352	80 + 8	31					X	
CC2652R7		X					X	X	X	X		704	144 + 8	31					X	
CC2652P		X					X	X	X	X	X	352	80 + 8	26					X	
CC2652P7		X					X	X	X	X	X	704	144 + 8	26					X	
CC2662R-Q1		X										352	80 + 8	31					X	
CC2674R10		X					X	X	X	X		1024	256 + 8	31-45					X	X
CC2674P10		X					X	X	X	X	X	1024	256 + 8	26-45					X	X

(1) ZigBee and Proprietary RF enabled by a future software update
(2) ZigBee and Thread support enabled by a future software update

6 Pin Configuration and Functions

6.1 Pin Diagram – RHB Package (Top View)

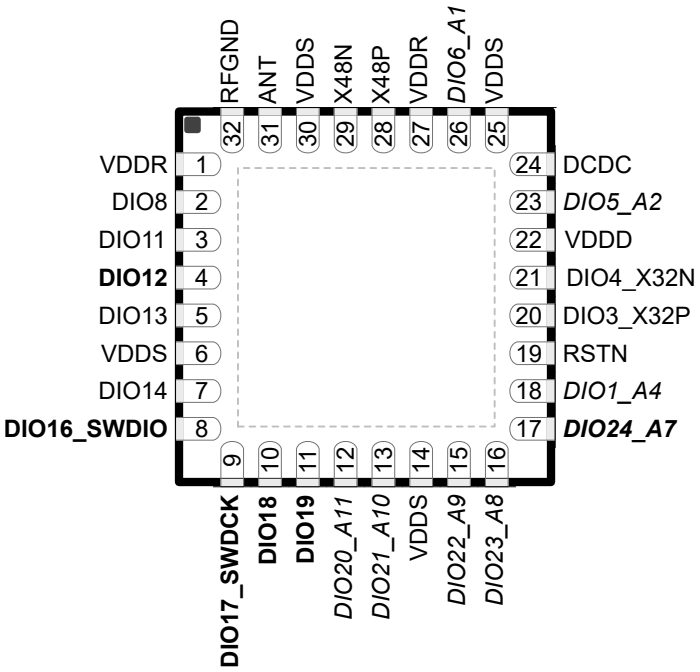

図 6-1. RHB (5-mm × 5-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in 図 6-1 in **bold** have high-drive capabilities:

- Pin 4, DIO12
- Pin 8, DIO16_SWDIO
- Pin 9, DIO17_SWDCK
- Pin 10, DIO18
- Pin 11, DIO19
- Pin 17, DIO24_A7

The following I/O pins marked in 図 6-1 in *italics* have analog capabilities:

- Pin 12, DIO20_A11
- Pin 13, DIO21_A10
- Pin 15, DIO22_A9
- Pin 16, DIO23_A8
- Pin 17, DIO24_A7
- Pin 18, DIO1_A4
- Pin 23, DIO5_A2
- Pin 26, DIO6_A1

6.2 Signal Descriptions – RHB Package

表 6-1. Signal Descriptions – RHB Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
EGP	—	—	GND	Ground – exposed ground pad(1)
VDDR	1	—	Power	Internal 1.5-V supply, must be powered from the internal DC/DC converter or the internal LDO(2) (3) (4)
DIO8	2	I/O	Digital	GPIO
DIO11	3	I/O	Digital	GPIO
DIO12	4	I/O	Digital	GPIO, high-drive capability
DIO13	5	I/O	Digital	GPIO
VDDS	6	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO14	7	I/O	Digital	GPIO
DIO16_SWDIO	8	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO17_SWDCK	9	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO18	10	I/O	Digital	GPIO, high-drive capability
DIO19	11	I/O	Digital	GPIO, high-drive capability
DIO20_A11	12	I/O	Digital or Analog	GPIO, analog capability
DIO21_A10	13	I/O	Digital or Analog	GPIO, analog capability
VDDS	14	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO22_A9	15	I/O	Digital or Analog	GPIO, analog capability
DIO23_A8	16	I/O	Digital or Analog	GPIO, analog capability
DIO24_A7	17	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO1_A4	18	I/O	Digital or Analog	GPIO, analog capability
RSTN	19	I	Digital	Reset, active low. No internal pullup resistor
DIO3_X32P	20	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 1, Optional TCXO input
DIO4_X32N	21	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 2
VDDD	22	—	Power	For decoupling of internal 1.28-V regulated core-supply. Connect an external 1 µF decoupling capacitor.(2)
DIO5_A2	23	I/O	Digital or Analog	GPIO, analog capability
DCDC	24	—	Power	Switching node of internal DC/DC converter(5)
VDDS	25	—	Power	1.71-V to 3.8-V analog supply(5)
DIO6_A1	26	I/O	Digital or Analog	GPIO, analog capability
VDDR	27	—	Power	Internal 1.5-V supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(2) (3) (4)
X48P	28	—	Analog	48-MHz crystal oscillator pin 1
X48N	29	—	Analog	48-MHz crystal oscillator pin 2
VDDS	30	—	Power	1.71-V to 3.8-V analog supply(5)
ANT	31	I/O	RF	2.4 GHz TX, RX
RFGND	32	—	RFGND	RF Ground

(1) EPG is the only non-RF ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(2) Do not supply external circuitry from this pin.
(3) VDDR pins 1 and 27 must be tied together on the PCB.
(4) Output from internal DC/DC and LDO is trimmed to 1.5 V.
(5) For more details, see the technical reference manual listed in セクション 10.3.

6.3 Connections for Unused Pins and Modules – RHB Package

表 6-2. Connections for Unused Pins – RHB Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	2–5 7 10–11	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	8	NC, GND, or VDDS	GND or VDDS
	DIO17_SWDCK	9	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	12–13 15–18 23 26	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	20	NC or GND	NC
	DIO4_X32N	21		
DC/DC converter(2)	DCDC	24	NC	NC
	VDDS	6, 14, 25, 30	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF DCDC capacitor must be kept on the VDDR net.

6.4 RHB Peripheral Pin Mapping

表 6-3. RHB (QFN32) Peripheral Pin Mapping

PIN NO. QFN32	PIN NAME	SIGNAL NAME	SIGNAL TYPE	PIN MUX ENCODING	SIGNAL DIRECTION
1	VDDR	VDDR	—	N/A	N/A
2	DIO8	GPIO8	I/O	0	I/O
		SPI0SCLK		1	I/O
		UART0RTS		2	O
		T1C0N		3	O
		I2C0SDA		4	I/O
		T0C0N		5	O
		DTB3		7	O
3	DIO11	GPIO11	I/O	0	I/O
		SPI0CSN		1	I/O
		T1C2N		2	O
		T0C0		3	O
		LRFD0		4	O
		SPI0MISO		5	I/O
		DTB9		7	O
4	DIO12	GPIO12	I/O	0	I/O
		SPI0MISO		1	I/O
		SPI0MOSI		2	I/O
		UART0RXD		3	I
		T1C1		4	O
		I2C0SDA		5	I/O
		DTB0		7	O

表 6-3. RHB (QFN32) Peripheral Pin Mapping (続き)

PIN NO. QFN32	PIN NAME	SIGNAL NAME	SIGNAL TYPE	PIN MUX ENCODING	SIGNAL DIRECTION
5	DIO13	GPIO13	I/O	0	I/O
		SPI0MISO		1	I/O
		SPI0MOSI		2	I/O
		UART0TXD		3	O
		T0C0N		4	O
		T1F		5	O
		DTB4		7	O
6	VDDS	VDDS	—	N/A	N/A
7	DIO14	DIO14	I/O	0	N/A
		T3C2		1	O
		T1C2N		2	O
		LRFD5		3	O
		T1F		4	O
8	DIO16_SWDIO	GPIO16	I/O	0	I/O
		SPI0MOSI		1	I/O
		UART0RXD		2	I
		I2C0SDA		3	I/O
		T1C2		4	O
		T1C0N		5	O
9	DIO17_SWDCK	GPIO17	I/O	0	I/O
		SPI0SCLK		1	I/O
		UART0TXD		2	O
		I2C0SCL		3	I/O
		T1C1N		4	O
		T0C2		5	O
		DTB11		7	O
10	DIO18	GPIO18	I/O	0	I/O
		T3C0		1	O
		LPCO		2	O
		UART0TXD		3	O
		SPI0SCLK		4	I/O
		DTB12		7	O
11	DIO19	GPIO19	I/O	0	I/O
		T3C1		1	O
		T2PE		2	O
		SPI0MOSI		4	I/O
		DTB13		7	O

表 6-3. RHB (QFN32) Peripheral Pin Mapping (続き)

PIN NO. QFN32	PIN NAME	SIGNAL NAME	SIGNAL TYPE	PIN MUX ENCODING	SIGNAL DIRECTION
12	DIO20_A11	GPIO20	I/O	0	I/O
		LPCO		1	O
		UART0TXD		2	O
		UART0RXD		3	I
		T1C0		4	O
		SPI0MISO		5	I/O
		ADC11		6	I
		DTB1		7	O
13	DIO21_A10	GPIO21	I/O	0	I/O
		UART0CTS		1	I
		T1C1N		2	O
		T0C1		3	O
		SPI0MISO		4	I/O
		LRFD1		5	O
		ADC10/LPC+		6	I
		DTB2		7	O
14	VDDS	VDDS	—	N/A	N/A
15	DIO22_A9	GPIO22	I/O	0	I/O
		T2C0		1	O
		UART0RXD		2	I
		T3C1N		3	O
		ADC9		6	I
		DTB14		7	O
16	DIO23_A8	GPIO23	I/O	0	I/O
		T2C1		1	O
		T3C2N		3	O
		ADC8/LPC+/LPC-		6	I
17	DIO24_A7	GPIO24	I/O	0	I/O
		SPI0SCLK		1	I/O
		T1C0		2	O
		T3C0		3	O
		T0PE		4	O
		I2C0SCL		5	I/O
		ADC7/LPC+/LPC-		6	I
		DTB5		7	O
18	DIO1_A4	GPIO1	I/O	0	I/O
		T3C1		1	O
		LRFD7		2	O
		T1F		3	O
		UART0RTS		4	O
		ADC4		5	I
		DTB15		6	O
19	RTSN	RSTN	—	N/A	N/A

表 6-3. RHB (QFN32) Peripheral Pin Mapping (続き)

PIN NO. QFN32	PIN NAME	SIGNAL NAME	SIGNAL TYPE	PIN MUX ENCODING	SIGNAL DIRECTION
20	DIO3_X32P	GPIO3	I/O	0	I/O
		LFCI		1	I
		T0C1N		2	O
		LRFD0		3	O
		T3C1		4	O
		T1C2		5	O
		LFXT_P		6	I
		DTB7		7	O
21	DIO4_X32N	GPIO4		0	I/O
		T0C2N		1	O
		UART0TXD		2	O
		LRFD1		3	O
		SPI0MOSI		4	I/O
		T0C2		5	O
		LFXT_N		6	I
		DTB8		7	O
22	VDDD	VDDD	—	N/A	N/A
23	DIO5_A2	GPIO5	I/O	1	I/O
		T2C2		2	O
		LRFD6		3	O
		ADC2		6	I
24	DCDC	DCDC	—	N/A	N/A
25	VDDS	VDDS	—	N/A	N/A
26	DIO6_A1	GPIO6	I/O	0	I/O
		SPI0CSN		1	I/O
		I2C0SCL		2	I/O
		T1C2		3	O
		LRFD2		4	O
		UART0TXD		5	O
		ADC1/AREF+		6	I
		DTB6		7	O
27	VDDR	VDDR	—	N/A	N/A
28	X48P	X48P	—	N/A	N/A
29	X48N	X48N	—	N/A	N/A
30	VDDS	VDDS	—	N/A	N/A
31	ANT	ANT	—	N/A	N/A
32	RFGND	RFGND	—	N/A	N/A
	GND_TAB		—	N/A	N/A

6.5 RHB Peripheral Signal Descriptions

表 6-4. RHB (QFN32) Peripheral Signal Descriptions

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN32			
ADC	ADC11	12	I/O	I	HP ADC channel 11 input
	ADC10	13			HP ADC channel 10 input
	ADC9	15			HP ADC channel 9 input
	ADC8	16			HP ADC channel 8 input
	ADC7	17			HP ADC channel 7 input
	ADC6	—			ADC channel 6 input
	ADC5	—			ADC channel 5 input
	ADC4	18			ADC channel 4 input
	ADC3	—			ADC channel 3 input
	ADC2	23			ADC channel 2 input
	ADC1	26			HP ADC channel 1 input
	ADC0	—			HP ADC channel 0 input
ADC Reference	AREF+	26	I/O	I	ADC external voltage reference, positive terminal
	AREF-	0			ADC external voltage reference, negative terminal
Analog Test Bus	ATEST0	12	I/O	O	Analot test bus output 0
	ATEST1	13			Analog test bus output 1
	FLTP3	13	I/O	O	Flash testpad output 3
	FLTP1	19			Flashtestpad output 1
Clock	X32P	20	I/O	I	32-kHz crystal oscillator pin 1, Optional TCXO input
	X32N	21	I/O	I	32-kHz crystal oscillator pin 2
	X48P	28	—	I	48-MHz crystal oscillator pin 1
	X48N	29	—	I	48-MHz crystal oscillator pin 2
	CLKMIN	—	I/O	I	TDC or HFOSC tracking loop reference clock input
	LFCI	20	I/O	I	Low frequency clock input (LFXT bypass clock from pin)
Comparator	LPC0	—	I/O	O	Low power comparator output
		10			
		12			
Comparator Input	LPC+	13	I/O	I	Low power comparator positive input terminal
		16			
		17			
	LPC-	16			Lower power comparator negative input terminal
		17			

表 6-4. RHB (QFN32) Peripheral Signal Descriptions (続き)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN32			
Digital Test Bus	DTB3	2	I/O	O	Digital test bus output 3
	DTB9	3			Digital test bus output 9
	DTB0	4			Digital test bus output 0
	DTB4	5			Digital test bus output 4
	DTB10	8			Digital test bus output 10
	DTB11	9			Digital test bus output 11
	DTB12	10			Digital test bus output 12
	DTB13	11			Digital test bus output 13
	DTB1	12			Digital test bus output 1
	DTB2	13			Digital test bus output 2
	DTB14	15			Digital test bus output 14
	DTB5	17			Digital test bus output 5
	DTB15	18			Digitial test bus output 15
	DTB7	20			Digital test bus output 7
	DTB8	21			Digital test bus output 8
	DTB6	26			Digital test bus output 6
GPIO	GPIO8	2	I/O	I/O	General-purpose input or output
	GPIO9	—			
	GPIO10	—			
	GPIO11	3			
	GPIO12	4			
	GPIO13	5			
	GPIO14	7			
	GPIO15	—			
	GPIO16	8			
	GPIO27	9			
	GPIO18	10			
	GPIO19	11			
	GPIO20	12			
	GPIO21	13			
	GPIO22	15			
	GPIO23	16			
	GPIO24	17			
	GPIO25	—			
	GPIO0	—			
	GPIO1	18			
	GPIO2	—			
	GPIO3	20			
	GPIO4	21			
	GPIO5	23			
	GPIO6	26			
	GPIO7	—			

表 6-4. RHB (QFN32) Peripheral Signal Descriptions (続き)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN32			
I^2C	I2C0_SCL	9	I/O	I/O	I^2C clock data
		17			
		—			
		26			
	I2C0_SDA	2	I/O	I/O	I^2C data
		4			
		8			
		—			
LRF Digital Output	LRFD3	—	I/O	O	LRF digital ouptut 3
	LRFD0	3			LRF digital output 0
		20			
	LRFD5	7			LRF digital output 5
	LRFD1	13			LRF digital output 1
		21			
	LRFD7	18			LRF digital output 7
	LRFD6	23			LRF digital output 6
	LRFD2	26			LRF digital output 2
	LRFD4	—			LRF digital output 4
Power	VDDR	1	—	—	Internal supply
		27			
	VDDS	6	—	—	1.71-V to 3.8V DIO supply
		14			
		25			
		30			
	VDDD	22	—	—	For decoupling of internal 1.28-V regulated core-supply.
	DCDC	24	—	—	Switching node of internal DC/DC converter
Reset	RSTN	19	—	—	Global main device reset (active low)
RF	ANT	31			50 ohm RF port
RF Gound	RFGND	32	—	—	RF Ground reference

表 6-4. RHB (QFN32) Peripheral Signal Descriptions (続き)

FUNCTION	SIGNAL NAME	Pin No. QFN32	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
SPI	SPI0SCLK	2	I/O	I/O	General SPI clock
		9			
		10			
		17			
	SPI0POCI	3	I/O	I/O	SPI POCI
		4			
		5			
		12			
		13			
		—			
	SPI0CSN	3	I/O	I/O	SPI chip select
		—			
		26			
	SPI0PICO	4	I/O	I/O	SPI PICO
		5			
		8			
		11			
		21			
SWD	SWDIO	8	I/O	I/O	JTAG/SWD TCK. Reset default pinout.
	SWDCK	9	I/O	I	JTAG/SWD TMS. Reset default pinout.
Timers - Capture/ Compare	T0C0	3	I/O	I/O	Capture/compare Output-0 from Timer-0
	T0C1	13			Capture/compare Output-1 from Timer-0
	T0C2	9			Capture/compare Output-2 from Timer-0
		21			
	T1C0	12	I/O	I/O	Capture/compare Output-0 from Timer-1
		17			
	T1C1	4			Capture/compare Output-1 from Timer-1
	T1C2	8			Capture/compare Output-2 from Timer-1
		20			
		26			
	T2C0	15	I/O	I/O	Capture/compare Output-0 from Timer-2
	T2C1	16			Capture/compare Output-1 from Timer-2
	T2C2	23			Capture/compare Output-2 from Timer-2
	T3C0	—	I/O	I/O	Capture/compare Output-0 from Timer-3
		10			
		17			
	T3C1	11			Capture/compare Output-1 from Timer-3
		18			
		20			
		—			
	T3C2	7			Capture/compare Output-2 from Timer-3
		—			

表 6-4. RHB (QFN32) Peripheral Signal Descriptions (続き)

FUNCTION	SIGNAL NAME	Pin No.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN32			
Timers - Complementary Capture/ Compare	T0C0N	2	I/O	O	Complementary compare/PWM Output-0 from Timer-0
		5			
	T0C1N	20			Complementary compare/PWM Output-1 from Timer-0
	T0C2N	21			Complementary compare/PWM Output-2 from Timer-0
	T1C0N	2	I/O	O	Complementary compare/PWM Output-0 from Timer-1
		8			
	T1C1N	9			Complementary compare/PWM Output-1 from Timer-1
		13			
	T1C2N	3			Complementary compare/PWM Output-2 from Timer-1
		7			
	T2C0N	—	I/O	O	Complementary compare/PWM Output-0 from Timer-2
	T2C1N	—			Complementary compare/PWM Output-1 from Timer-2
	T2C2N	—			Complementary compare/PWM Output-2 from Timer-2
	T3C0N	—	I/O	O	Complementary compare/PWM Output-0 from Timer-3
	T3C1N	15			Complementary compare/PWM Output-1 from Timer-3
	T3C2N	16			Complementary compare/PWM Output-2 from Timer-3
Timers - Fault input	T1F	5	I/O	I	Fault input for Timer-1
		7			
		18			
Timers - Prescaler Event	T2PE	—	I/O	O	Prescaler event ouput from Timer-2
		11			
	T0PE	17	I/O	O	Prescaler eveny ouput from Timer-0
		—			
UART	UART0TXD	5	I/O	O	UART0 TX data
		9			
		10			
		12			
		21			
		26			
	UART0RXD	4	I/O	I	UART0 RX data
		—			
		8			
		12			
		15			
	UART0CTS	13	I/O	I	UART0 clear-to-send input (active low)
		—			
	UART0RTS	2	I/O	O	UART0 request-to-send (active low)
		18			

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
VDDS	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(3)		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins X48P and X48N		–0.3	1.24	V
V_{in_adc}	Voltage on ADC input		0	VDDS	V
	Input level, RF pins			5	dBm
P_{max}	Environmental Pressure			1400	kPa
A_{max}	Static Acceleration			2000	g
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIOs.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) (3) (4)	All pins except ANT pin	±2000	V
			ANT pin	±1000	V
		Charged device model (CDM), per AEC Q100-011(2) (4)	All pins except ANT pin	±500	V
			ANT pin	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process
(3) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification
(4) The ANT pin is an RF type pin, per Table 7-1 and complies with recommended ESD limits per JEP and AEC specifications listed above

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (2)	–40	125	°C
Operating junction temperature(1) (2)	–40	125	°C
Operating supply voltage (VDDS)	1.71	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(3)	0	1	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
(2) For thermal resistance details, refer to *Thermal Resistance Characteristics* table in this document.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10-µF VDDS input capacitor must be used to ensure compliance with this slew rate.

7.4 DCDC

When measured on the CC2340R5 reference design with T_c = 25 °C and DCDC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for DCDC operation (1) (2)		2.2	3.0	3.8	V

(1) When the supply voltage drops below the DCDC operation min voltage, the device automatically transitions to use GLDO regulator on-chip.
(2) A 10uH and 10uF load capacitor are required on the VDDR voltage rail. They should be placed close to the DCDC output pin.

7.5 Global LDO (GLDO)

When measured on the CC2340R5 reference design with T_c = 25 °C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for GLDO operation (1)		1.71	3.0	3.8	V

(1) A 10 µF capacitor is recommended at VDDR pin.

7.6 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS_BOD					
Brownout rising threshold (1)			1.68		V
Brownout falling threshold (1)			1.67		V
POR					
power-on reset power-up level			1.5		V
power-on reset power-down level			1.45		V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RSTN pin.

7.7 Battery Monitor

Measured on the CC2340R5 reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			22		mV
Range		1.7		3.8	V
Accuracy	VDDS = 3.0 V		30		mV

7.8 Temperature Sensor

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy	-40 °C to 125 °C		-15/+9(1)		°C

(1) Raw output from PMUD register.

7.9 Power Consumption - Power Modes

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption with DCDC				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	2.6	mA
I_{core}	Active	MCU running CoreMark from Flash at 48MHz	53	µA / MHz
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	0.8	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	0.8	mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	1.1	mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	1.2	mA
I_{core}	Standby	RTC running, 36kB RAM retention LFOSC, DCDC recharge current setting (ipeak = 1)	0.71	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT, DCDC recharge current setting (ipeak = 1)	0.74	µA
Core Current consumption with GLDO				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	4.1	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	1.2	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	1.3	mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	1.5	mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	1.7	mA
I_{core}	Standby	RTC running, 36kB RAM retention LFOSC, default GLDO recharge current setting	1.1	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT default GLDO recharge current setting	1.15	µA
Reset, Shutdown Current Consumption				
I_{core}	Reset	Reset. RSTN pin asserted or VDDS below power-on-reset threshold	165	nA
I_{core}	Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled	165	nA
Peripheral Current Consumption				
I_{peri}	RF	Delta current, clock enabled, RF subsystem idle	40	µA
I_{peri}	Timers	Delta current with clock enabled, module is idle, one LGPT timer	2.4	µA
I_{peri}	I2C	Delta current with clock enabled, module is idle	10.6	µA
I_{peri}	SPI	Delta current with clock enabled, module is idle	3.4	µA
I_{peri}	UART	Delta current with clock enabled, module is idle	24.5	µA
I_{peri}	CRYPTO (AES)	Delta current with clock enabled, module is idle	3.8	µA

7.10 Power Consumption - Radio Modes

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DCDC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, system bus off (1)	5.3	mA
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, DCDC OFF, system bus off (1)	9	mA
I_{TX}	Radio transmit current	-8 dBm output power setting 2440 MHz system bus off (1)	4.5	mA
I_{TX}	Radio transmit current	0 dBm output power setting 2440 MHz system bus off (1)	5.1	mA
I_{TX}	Radio transmit current	0 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	9.0	mA
I_{TX}	Radio transmit current	+4 dBm output power setting 2440 MHz system bus off (1)	7.9	mA
I_{TX}	Radio transmit current	+6 dBm output power setting 2440 MHz system bus off (1)	9.0	mA
I_{TX}	Radio transmit current	+8 dBm output power setting 2440 MHz system bus off (1)	10.7	mA
I_{TX}	Radio transmit current	+8 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	19	mA

(1) System bus off refers to device idle mode, DMA disabled, flash disabled

7.11 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		KB
Supported flash erase cycles before failure, full bank(1) (2)		30			k Cycles
Supported flash erase cycles before failure, single sector(3)		60			k Cycles
Maximum number of write operations per row before sector erase(4)				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash retention	125 °C	10			Years
Flash sector erase current	Average delta current		1.2		mA
Flash sector erase time(5)	0 erase cycles		2.2		ms
Flash write current	Average delta current, full sector at a time		1.7		mA
Flash write time(5)	full sector (2kB) at a time, 0 erase cycles		8.3		ms

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Aborting flash during erase or program modes is not a safe operation.
(3) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(5) This number is dependent on Flash aging and increases over time and erase cycles

7.12 Thermal Resistance Characteristics

THERMAL METRIC	THERMAL METRIC	PACKAGE	UNIT
		RHB (VQFN)	
		32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.6	°C/W (1)
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	°C/W (1)
$R_{\theta JB}$	Junction-to-board thermal resistance	12.7	°C/W (1)
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W (1)

THERMAL METRIC	THERMAL METRIC	PACKAGE	UNIT
		RHB (VQFN)	
		32 PINS	
ψ_{JB}	Junction-to-board characterization parameter	12.6	°C/W (1)
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W (1)

(1) °C/W = degrees Celsius per watt.

7.13 Thermal Shutdown

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OP}	Operating supply voltage		1.71		3.8	V
T_{jun}	Operating junction temperature		96		150	°C
T_{rstrel}	Reset release temperature		101.8		114	°C
I_{core_TSD}	Current consumption in thermal shutdown mode (up to 150C)				100	µA

7.14 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2510	MHz

7.15 Bluetooth Low Energy - Receive (RX)

When measured on the CC2340R 5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–102		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–122/ 122) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 31 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		47 / 42 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		49 / 45 (3)		dB
Selectivity, ±6 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		52 / 48 (3)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		54 / 49 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, Image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 42 (3)		dB
500 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–99		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–122 / 122) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90/ 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–4.5		dB
Selectivity, ±1 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		42 / 31 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		45 / 41 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		46 / 42 (3)		dB
Selectivity, ±6 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		50 / 45 (3)		dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		51 / 46 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB

When measured on the CC2340R 5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, Image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 41 (3)		dB
1 Mbps (LE 1M)					
Receiver sensitivity	BER = 10^{-3}		–96.5		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–225 /225) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		39 / 28 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		38 / 38 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		47 / 35 (3)		dB
Selectivity, ±5 MHz or more(2)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(2)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		28		dB
Selectivity, image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 38 (3)		dB
Out-of-band blocking(4)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–10		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–10		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)		–2		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–37		dBm
Spurious emissions, 30 to 1000 MHz(5)	Measurement in a 50-Ω single-ended load.		< –59		dBm
Spurious emissions, 1 to 12.75 GHz(5)	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range (6)			70		dB
RSSI accuracy			±4		dB
RSSI resolution			1		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Measured at SMA connector, BER = 10^{-3}		2		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–225 / 225) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90/ 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –67 dBm, modulated interferer in channel,BER = 10^{-3}		–8		dB
Selectivity, ±2 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		40 / 32 (3)		dB

When measured on the CC2340R 5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±6 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		46 / 40 (3)		dB
Selectivity, image frequency(2)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		5		dB
Selectivity, image frequency ±2 MHz(2)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–8 / 32 (3)		dB
Out-of-band blocking(4)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–10		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Actual performance exceeding Bluetooth specification
(2) Numbers given as I/C dB
(3) X / Y, where X is +N MHz and Y is –N MHz
(4) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(5) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
(6) The device will saturate at -30dB.

7.16 Bluetooth Low Energy - Transmit (TX)

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Delivered to a single-ended 50-Ω load through integrated balun		8		dBm
Output power programmable range	Delivered to a single-ended 50-Ω load through integrated balun		28		dB

7.17 2.4 GHz RX/TX CW

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Spurious emissions and harmonics						
Spurious emissions[1]	f < 1 GHz, outside restricted bands	+8 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics (ETSI)			< –30		dBm
Harmonics [1]	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

7.18 Timing and Switching Characteristics

7.18.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RSTN low duration	1			µs

7.18.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset/Shutdown to Active[1]	GLDO default charge current setting, VDDR capacitor fully charged [2]		350-450		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). DCDC ON, default recharge current configuration		33-43 [3]		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). GLDO ON, default recharge current configuration		33-50 [3]		µs
MCU, Idle to Active	Flash enabled in idle mode		3		µs
MCU, Idle to Active	Flash disabled in idle mode		14		µs

(1) Wakeup time includes device ROM bootcode execution time. The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
(2) This is the best case reset/shutdown to active time (including ROM bootcode operation), for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time
(3) Depending on VDDR capacitor voltage level.

7.18.3 Clock Specifications

7.18.3.1 48 MHz Crystal Oscillator (HFXT)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(4)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance(5) (6) C_L = 9 pF			35	Ω
	Equivalent series resistance(5) (6) C_L = 8 pF			50	Ω
	Equivalent series resistance(5) (6) C_L = 7 pF			60	Ω
	Equivalent series resistance(5) (6) 5 pF ≤ C_L ≤ 6 pF			80	Ω
C_L	Crystal load capacitance(1)	5	7(2)	9	pF
Start-up time (3)	Until clock is qualified		200		µs

(1) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations.
(2) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the SysConfig.
(3) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(4) Tai-Saw TZ3908AAAO43 has been validated for CC2340R5 design.
(5) The max ESR value will be reduced if the crystal has a shunt capacitance of C0 > 1pF
(6) Startup margin ≥10

7.18.3.2 48 MHz RC Oscillator (HFOSC)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±3		%
Calibrated frequency accuracy (1)		±0.25		%

(1) Accuracy relative to the calibration source (HFXT)

7.18.3.3 32 kHz Crystal Oscillator (LFXT)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
Supported crystal load capacitance	6		12	pF
ESR		30	100	kΩ

7.18.3.4 32 kHz RC Oscillator (LFOSC)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.768 (1)		kHz

(1) When using LFOSC as source for the low frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

7.19 Peripheral Characteristics

7.19.1 UART

7.19.1.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

7.19.2 SPI

7.19.2.1 SPI Characteristics

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted).

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fSCLK 1/tsclk	SPI clock frequency	Controller Mode and Peripheral Mode (1) 2.7V ≤ VDDS < 3.8V			12	MHz
		Controller Mode and Peripheral Mode (1) VDDS < 2.7V			8	MHz
DC_{SCK}	SCK Duty Cycle		45	50	55	%

(1) Assume interfacing with ideal SPI controller and SPI peripheral devices

7.19.2.2 SPI Controller Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK\_H/L}$	SCLK High or Low time		$(t_{SPI}/2) - 1$	$t_{SPI}/2$	$(t_{SPI}/2) + 1$	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid,C_L = 20 pF			13	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.19.2.3 SPI Timing Diagrams - Controller Mode

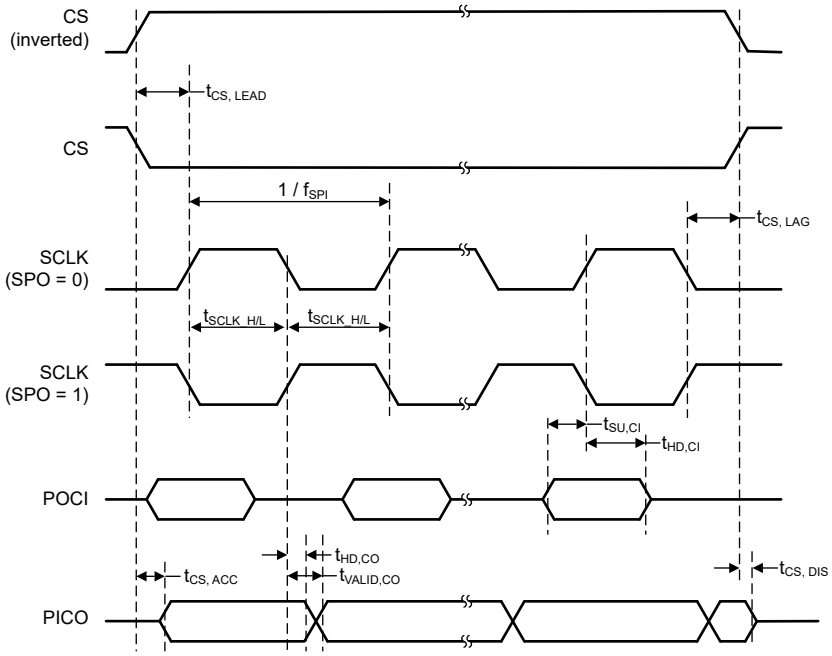

図 7-1. SPI Timing Diagram - Controller Mode, SPH = 0

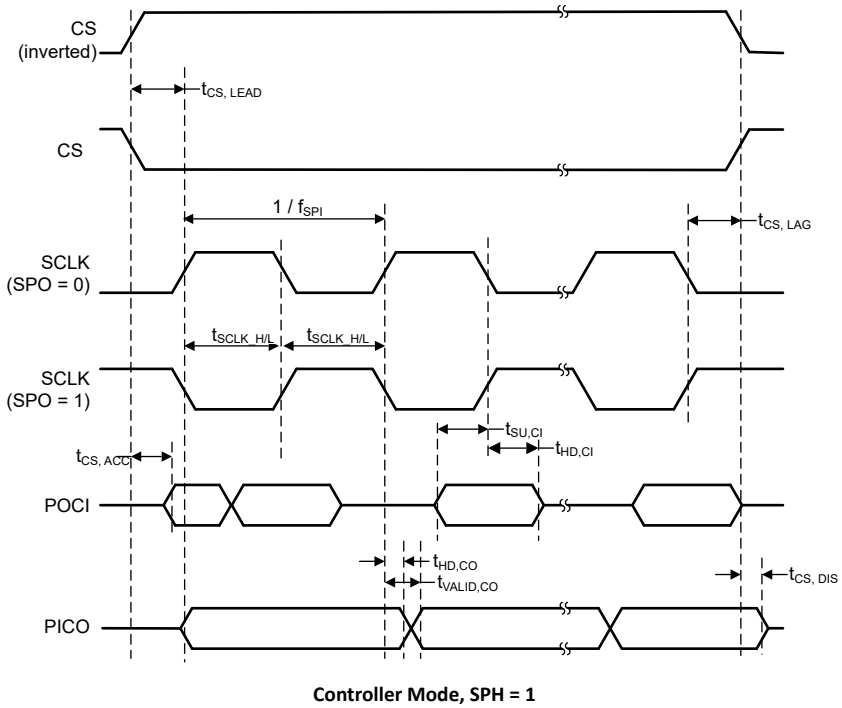

図 7-2. SPI Timing Diagram - Controller Mode, SPH = 1

7.19.2.4 SPI Peripheral Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted),

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 3.3V			35	ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 1.8V			50	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 3.3V			35	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance	VDDS = 1.8V			50	ns
$t_{SU.PI}$	PICO input data setup time		13			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20 pF, 3.3V			35	ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20 pF, 1.8V			50	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.19.2.5 SPI Timing Diagrams - Peripheral Mode

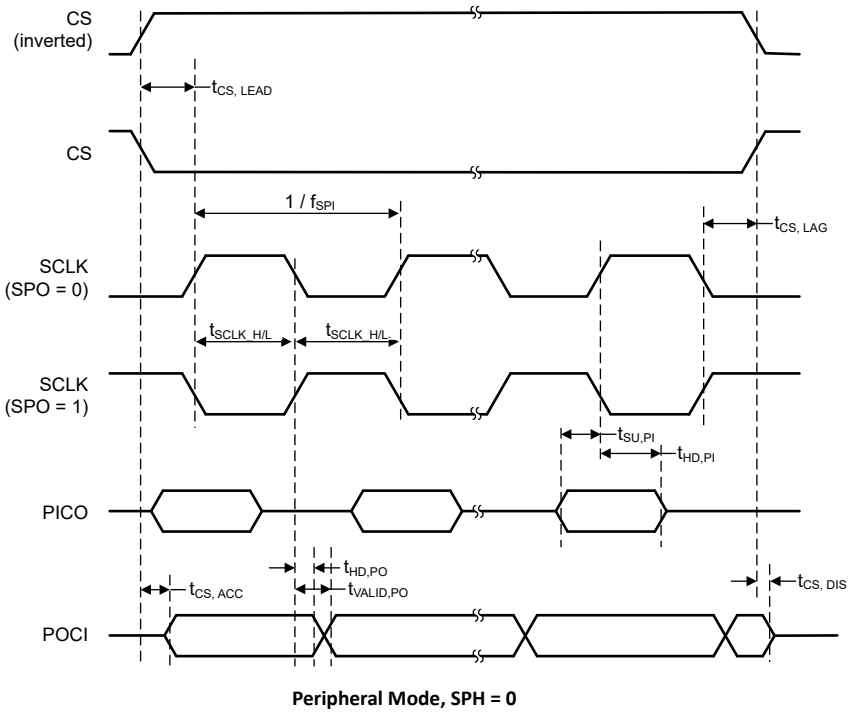

図 7-3. SPI Timing Diagram - Peripheral Mode, SPH = 0

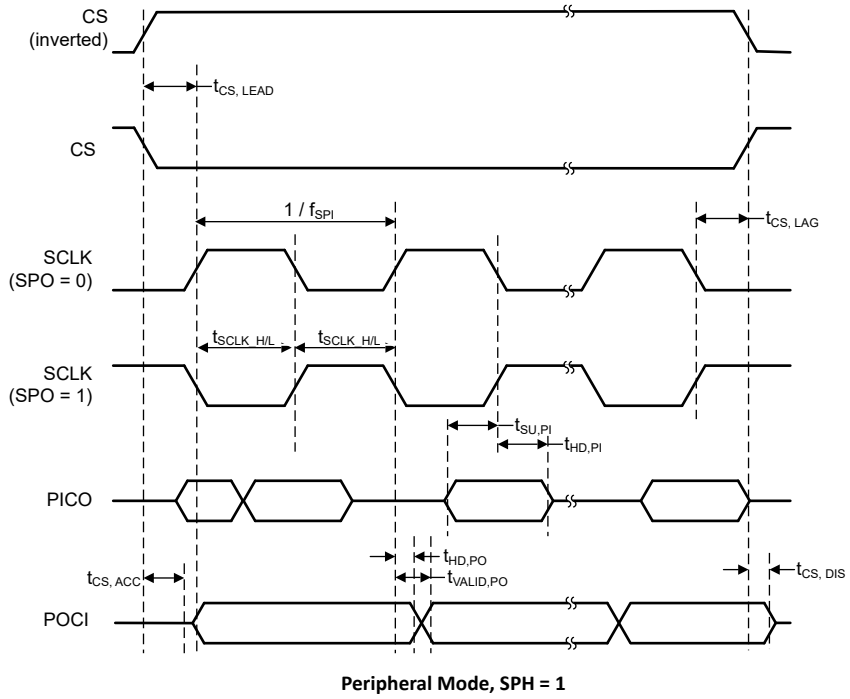

図 7-4. SPI Timing Diagram - Peripheral Mode, SPH = 1

7.19.3 I²C

7.19.3.1 I2C

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100kHz	4.0			µs
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} > 100kHz	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100kHz	4.7			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} > 100kHz	0.6			µs
$t_{HD,DAT}$	Data hold time		0			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100kHz	250			ns
$t_{SU,DAT}$	Data setup time	f_{SCL} > 100kHz	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100kHz	4.0			µs
$t_{SU,STO}$	Setup time for STOP	f_{SCL} > 100kHz	0.6			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100kHz	4.7			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} > 100kHz	1.3			µs
t_{SP}	Pulse duration of spikes supressed by input deglitch filter		50			ns

7.19.3.2 I²C Timing Diagram

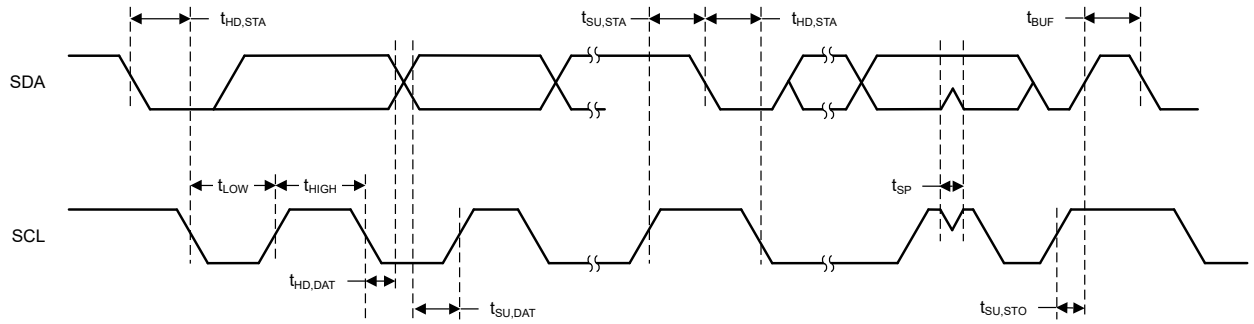

図 7-5. I²C Timing Diagram

7.19.4 GPIO

7.19.4.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO VOH at 10 mA load	high-drive GPIOs only, max drive setting	1.15	1.54		V
GPIO VOL at 10 mA load	high-drive GPIOs only, max drive setting		0.25	0.50	V
GPIO VOH at 2 mA load	standard drive GPIOs	1.27	1.60		V
GPIO VOL at 2 mA load	standard drive GPIOs		0.19	0.35	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	39	66	109	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	10	21	40	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	0.91	1.11	1.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	0.59	0.75	0.91	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.26	0.35	0.44	V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 10 mA load	high-drive GPIOs only, max drive setting	2.47			V
GPIO VOL at 10 mA load	high-drive GPIOs only, max drive setting			0.25	V
GPIO VOH at 2 mA load	standard drive GPIOs	2.52			V
GPIO VOL at 2 mA load	standard drive GPIOs			0.20	V
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	170	262	393	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	60	110	172	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	1.76	1.98	2.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	1.26	1.52	1.79	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.40	0.47	0.54	V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

7.19.5 ADC

7.19.5.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(2)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins Ax	0		VDDS	V
$I_{(ADC)}$ single-ended mode	Operating supply current into VDDS terminal	RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADCREF_EN = 0), VeREF+ = VDDS		480		µA
		RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADCREF_EN = 0), ADCREF = 2.5V		365		
$C_{I\ GPIO}$	Input capacitance into a single terminal			5	7	pF
$R_{I\ GPIO}$	Input MUX ON-resistance			0.5	1	kΩ
ADC Switching Characteristics						
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			267 (1)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			308 (1)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			400 (1)	ksps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			1.2 (1)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			1.33 (1)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			1.6 (1)	Msps
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x0 (12-bit)		14		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x1 (10-bit)		12		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x2 (8-bit)		9		cycles
t_{Sample}	Sampling time	RES = 0x0 (12-bit), R_S = 25 Ω, C_{pext} = 10 pF. +/- 0.5 LSB settling	250			ns
$t_{VSUPPLY/3(sample)}$	Sample time required when Vsupply/3 channel is selected		20			µs
ADC Linearity Parameters						
E_I	Integral linearity error (INL) for single-ended inputs	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 2		LSB
E_D	Differential linearity error (DNL)	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 1		LSB
E_O	Offset error	12-bit Mode, External reference, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		1.98		LSB
E_O	Offset error	12-bit Mode, Internal reference, V_{R+} = ADCREF = 2.5V		1.02		LSB
E_G	Gain error	External Reference, V_{R+} = VeREF+ = VDDS , VDD= 1.71-->3.8		+/- 2		LSB
E_G	Gain error	Internal reference, V_{R+} = ADCREF = 2.5V		+/- 40		LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x1 (10-bit)		9.9		bit

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(2)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		11.2		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V} , RES = 0x1 (10-bit)		9.6		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		10.4		bit
ENOB	Effective number of bits	VDDS reference, RES = 0x0 (12-bit)		11.2		bit
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		69.18		dB
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		64.37		dB
SINAD	Signal-to-noise and distortion ratio	VDDS reference, RES = 0x0 (12-bit)		69.18		dB
ADC External Reference						
EXTREF	Positive external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF+)	1.4		VDDS	V
EXTREF	Negative external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF-)			0	V
ADC Temperature Diode, Supply Monitor						
Temp_diode Accuracy	Temperature Error	ADC input channel: Temp diode voltage, Error calculated in temperature range: -30C to +40C, with single point calibration (2)		+/- 3		C
ADC Internal Input: V_{SUPPLY} / 3 Accuracy	V_{supply} voltage divider accuracy for supply monitoring	ADC input channel: Vsupply monitor		+/- 1		%
ADC Internal Input: $I_{Vsupply / 3}$	V_{supply} voltage divider current consumption	ADC input channel Vsupply monitor. V_{supply}=VDDS=3.3V		10		µA
ADC Internal and VDDS Reference						
VDDSREF	Positive ADC reference voltage	ADC reference sourced from VDDS		VDDS		V
ADCREF	Internal ADC Reference Voltage	ADCREF_EN = 1, ADCREF_VSEL = 0, VDDS = 1.71V - VDDSmax		1.4		V
		ADCREF_EN = 1, ADCREF_VSEL = 1, VDDS = 2.7V - VDDSmax		2.5		V
I_{ADCREF}	Operating supply current into VDDA terminal with internal reference ON	ADCREF_EN = 1, VDDA = 1.7V to VDDAmax, ADCREF_VSEL = {0,1}		80		µA
t_{ON}	Internal ADC Reference Voltage power on-time	ADCREF_EN = 1		2		µs

(1) Measured with 48MHz HFOSC
(2) Using IEEE Std 1241-2010 for terminology and test methods

7.19.6 Comparators

7.19.6.1 Ultra-low power comparator

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		KHz
Voltage Divider Accuracy	Input voltage range is between VDDS/4 and VDDS		98		%
Offset	Measured at V_{DDS} / 2 (Errors seen when using two external inputs)		+/- 27.3		mV
Decision time	Step from –50 mV to 50 mV		1	3	Clock Cycle
Comparator enable time	COMP_LP disable → enable, VIN+, VIN- from pins, Overdrive ≥ 20 mV		70		µs
Current consumption	Including using VDDS/2 as internal reference at VIN- comparator terminal		370		nA

7.20 Typical Characteristics

All measurements in this section are done with T_c = 25 °C and V_{DDS} = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions* for device limits. Values exceeding these limits are for reference only.

7.20.1 MCU Current

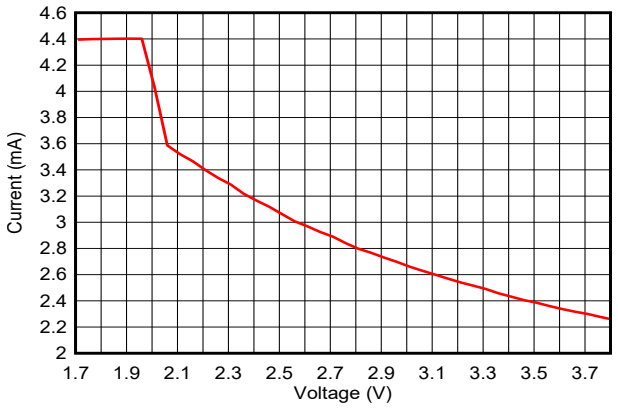

図 7-6. Active Mode (MCU) Current vs. Supply Voltage (VDDS) (Running CoreMark)

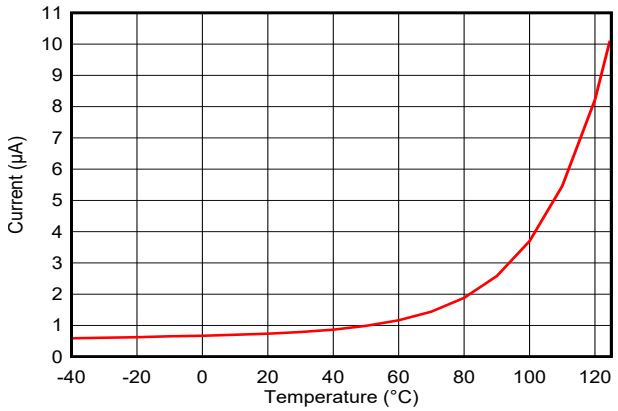

図 7-7. Standby Mode (MCU) Current vs. Temperature (RAM and partial register retention, RTC)

7.20.2 RX Current

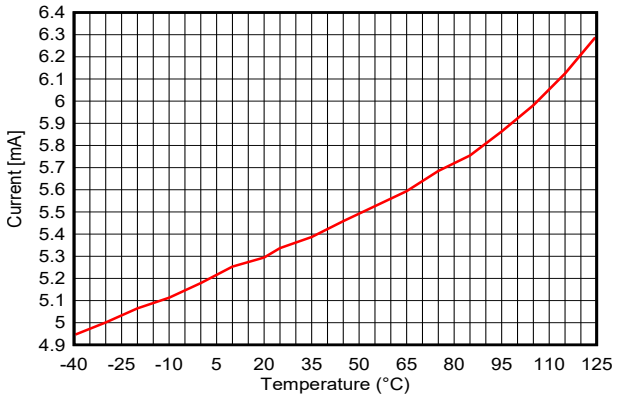

図 7-8. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

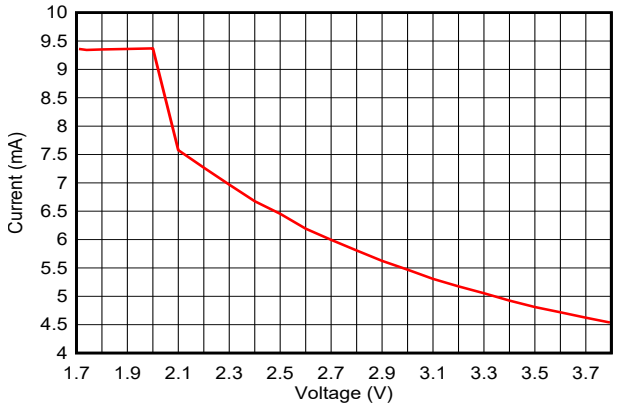

図 7-9. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

7.20.3 TX Current

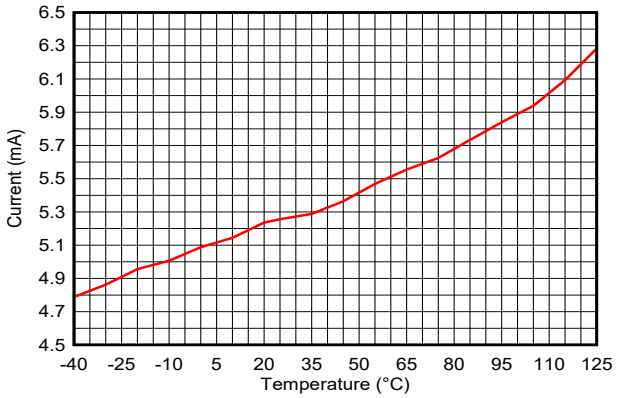

図 7-10. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

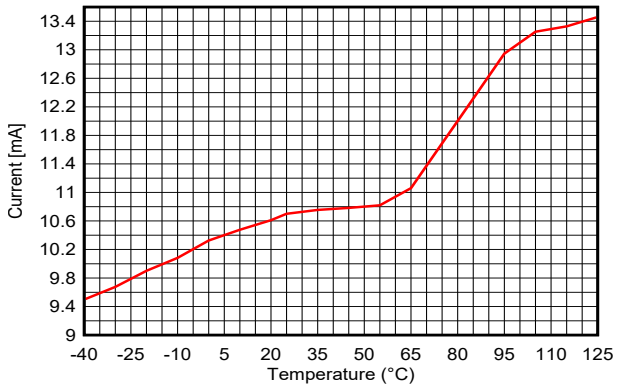

図 7-11. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, +8 dBm)

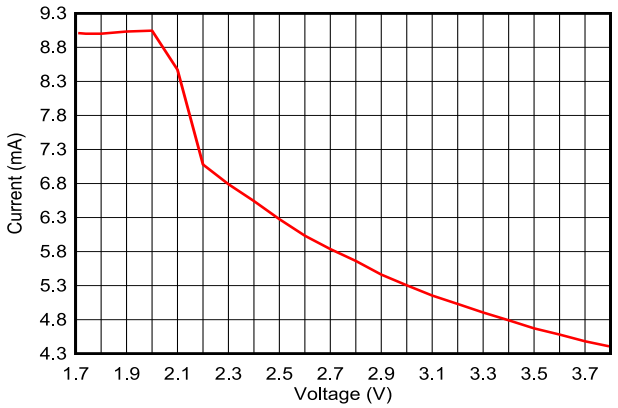

図 7-12. TX Current vs. Supply Voltage, VDDS (BLE 1 Mbps, 2.44 GHz, 0 dBm)

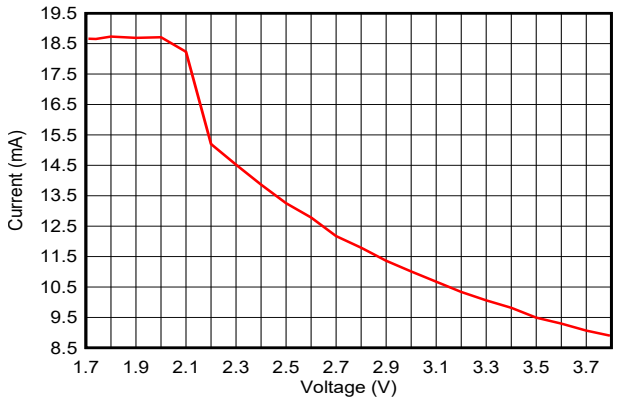

図 7-13. TX Current vs. Supply Voltage, VDDS (BLE 1 Mbps, 2.44 GHz, +8 dBm)

表 7-1 shows typical TX current and output power for different output power settings.

表 7-1. Typical TX Current and Output Power

2.4 GHz, VDDS = 3.0 V, DCDC=On, Temperature = 25 °C (Measured on LP-EM-CC2340R5)			
txPowerTable Index	**TX Power Setting [dBm] (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
13	8	7.7	10.7
12	7	7.1	9.5
11	6	6.3	8.9
10	5	5.5	8.3
9	4	4.5	7.9
8	3	3.7	7.5
7	2	2.4	7.1
6	1	1.0	5.4
5	0	0.4	5.1
4	-4	-3.1	4.8
3	-8	-7.3	4.5
2	-12	-10.9	4.2
1	-16	-15.1	4.0
0	-20	-19.0	3.8

7.20.4 RX Performance

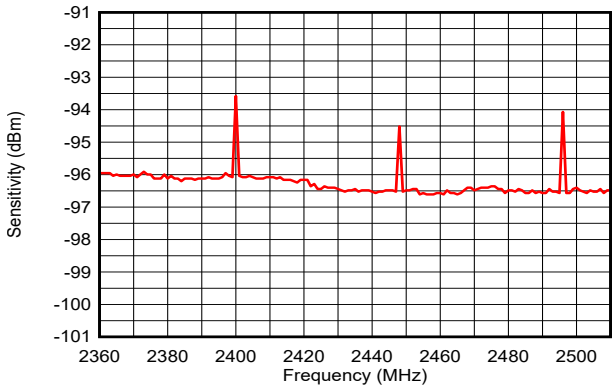

図 7-14. Sensitivity vs. Frequency (BLE 1 Mbps)

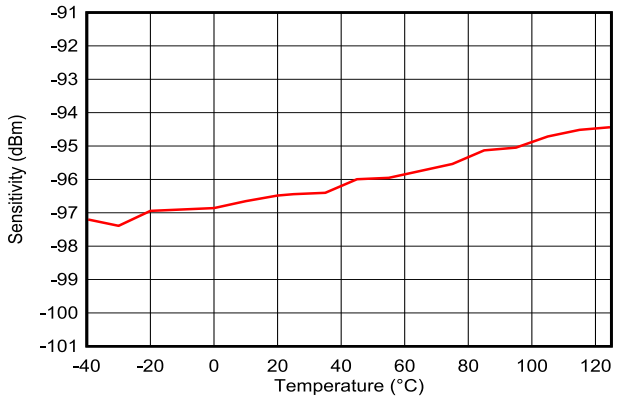

図 7-15. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)

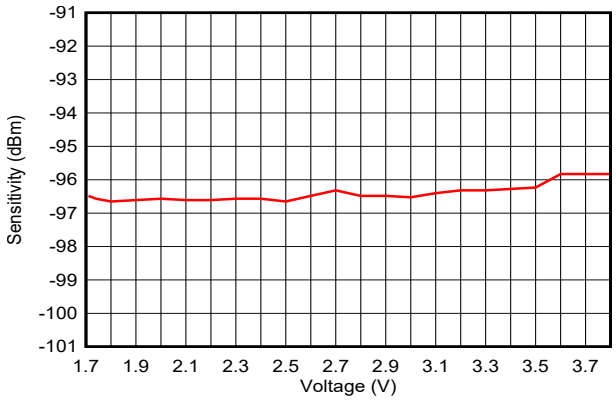

図 7-16. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

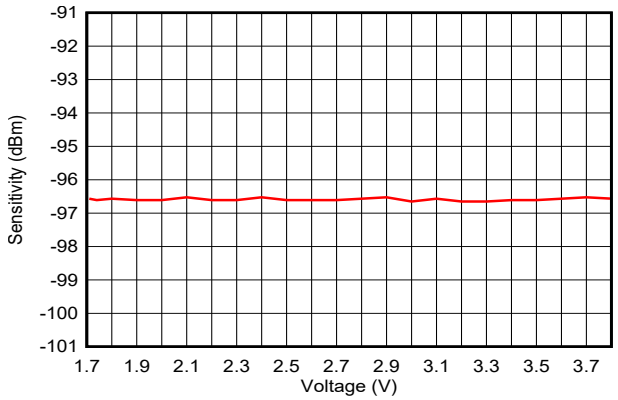

図 7-17. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)

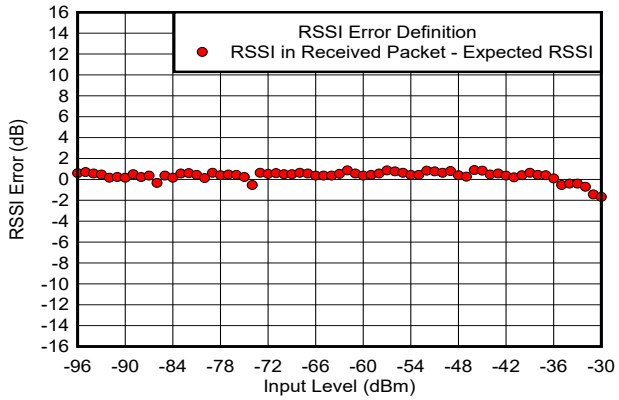

図 7-18. RSSI Error vs. Input Level (dBm)

7.20.5 TX Performance

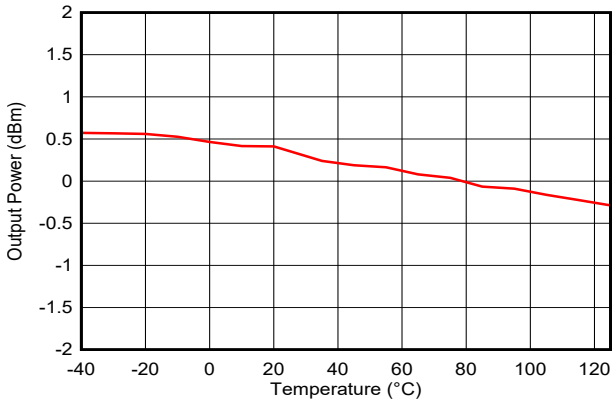

図 7-19. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

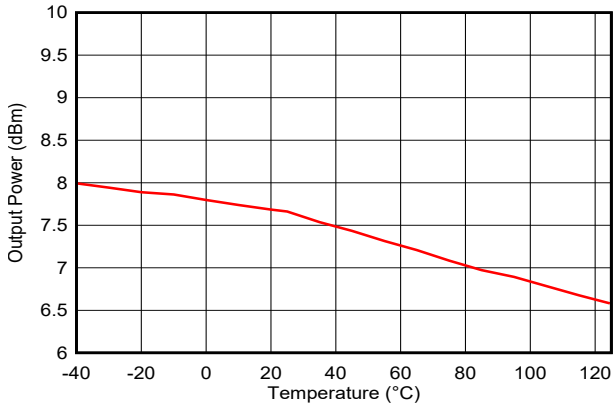

図 7-20. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +8 dBm)

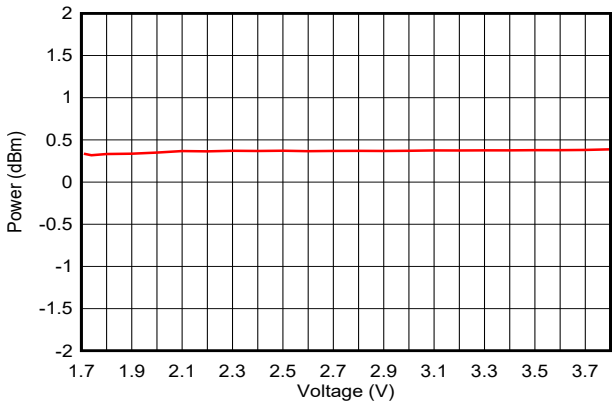

図 7-21. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)

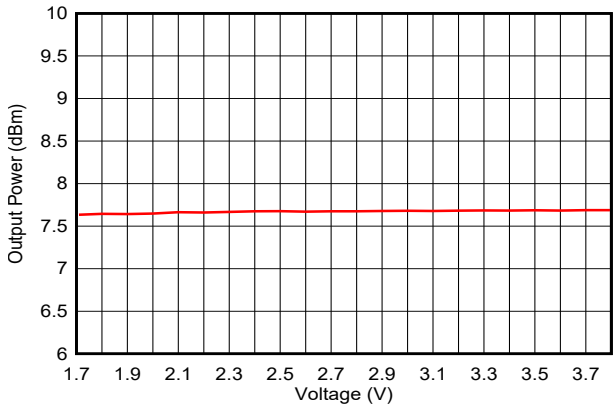

図 7-22. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +8 dBm)

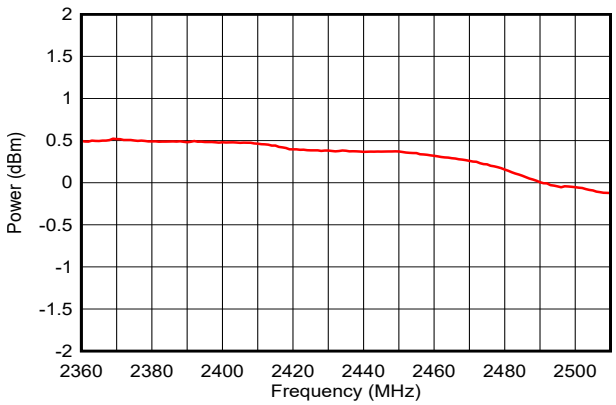

図 7-23. Output Power vs. Frequency (BLE 1 Mbps, 0 dBm)

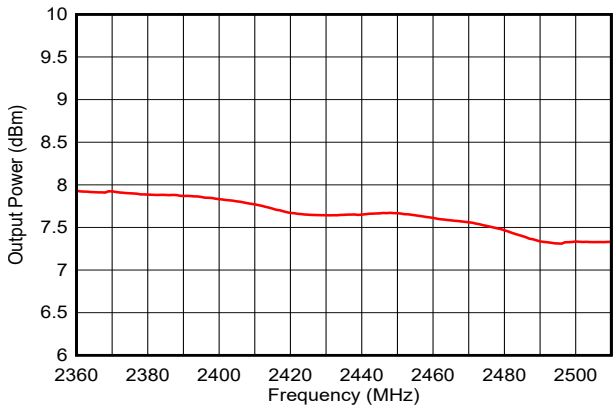

図 7-24. Output Power vs. Frequency (BLE 1 Mbps, +8 dBm)

7.20.6 ADC Performance

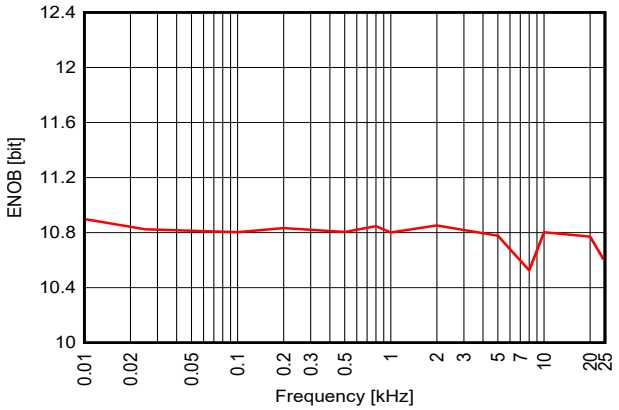

図 7-25. ENOB vs. Input Frequency (Internal Reference)

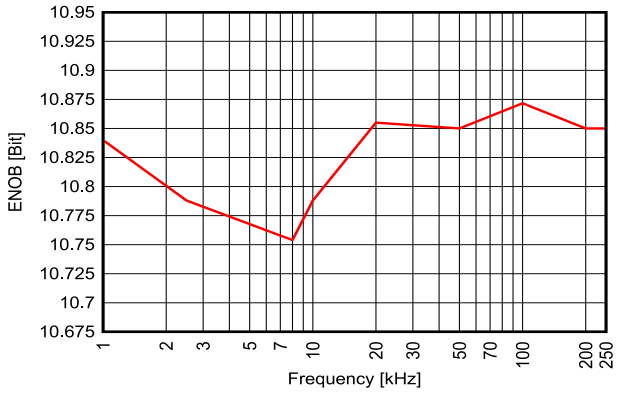

図 7-26. ENOB vs. Sampling Frequency (V_{in}= 3V Sine Wave, Internal Reference, F_{in}=F_s/10)

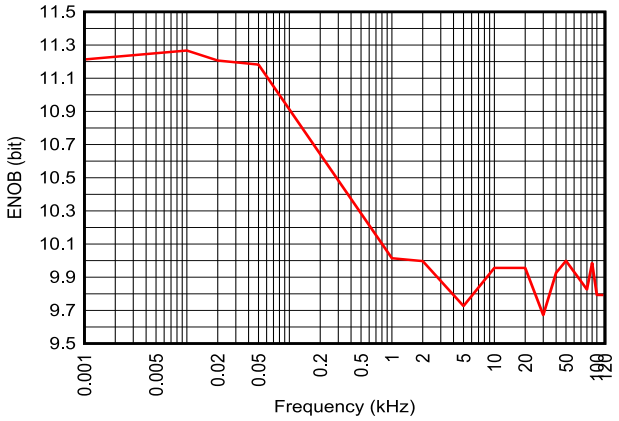

図 7-27. ENOB vs. Input Frequency (External Reference = 3.0 V)

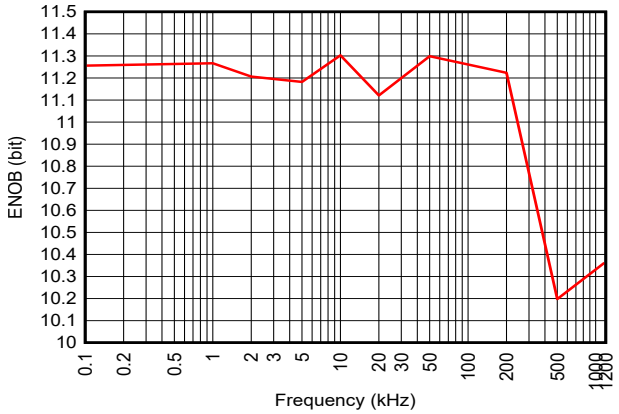

図 7-28. ENOB vs. Sampling Frequency (V_{in} = 3V Sine Wave, External Reference = 3.0 V, F_{in}=F_s/10

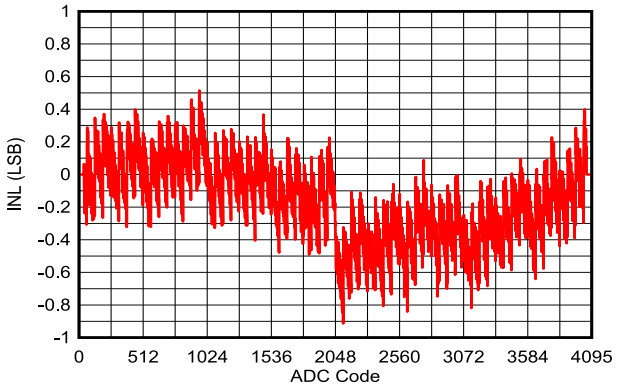

図 7-29. INL vs. ADC Code (V_{in}= 3V Sine Wave, Internal Reference, 200 ksps)

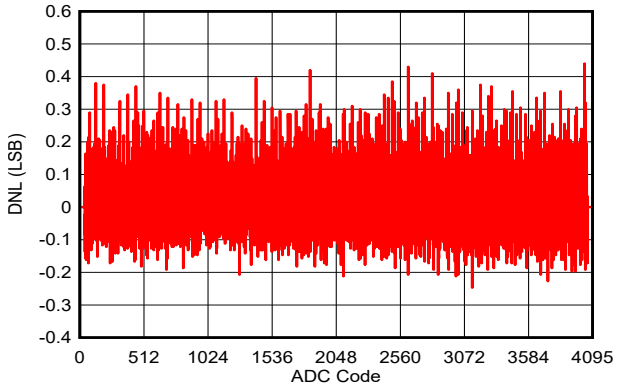

図 7-30. DNL vs. ADC Code (V_{in}= 3V Sine Wave, Internal Reference, 200 ksps)

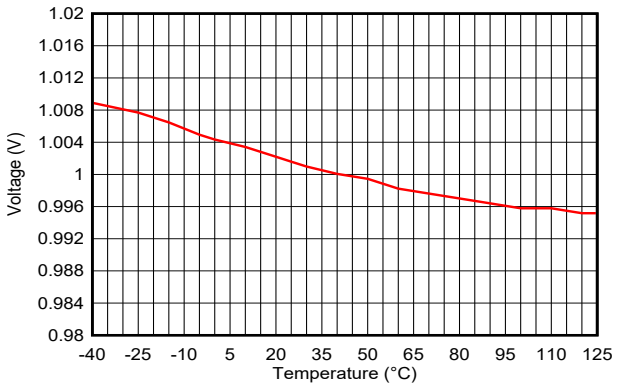

図 7-31. ADC Accuracy vs. Temperature (V_{in}= 1V, Internal Reference, 200 ksps)

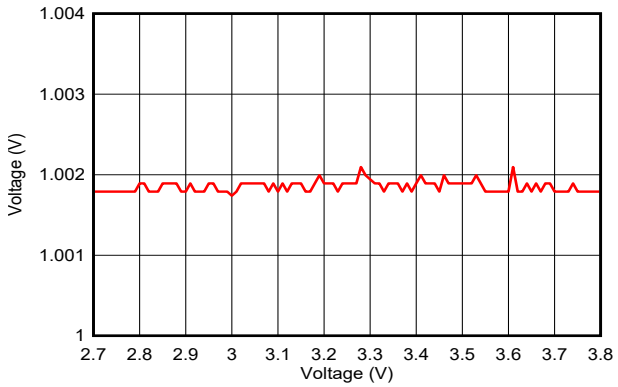

図 7-32. ADC Accuracy vs. Supply Voltage (V_{in}= 1V, Internal Reference, 200 ksps)

8 Detailed Description

8.1 Overview

セクション 4 shows the core modules of the CC2340R5-Q1 device.

8.2 System CPU

The CC2340R5-Q1 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M0+ system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The Cortex-M0+ processor offers multiple benefits to developers including:

- Ultra-low power, energy efficient operation
- Deterministic, high-performance interrupt handling for time-critical applications
- Upward compatibility with the Cortex-M processors family

The Cortex-M0+ processor provides the excellent performance expected of a modern 32- bit architecture core, with higher code density than other 8-bit and 16-bit microcontrollers. Its features include the following:

- ARMv6-M architecture optimized for small-footprint embedded applications
- Subset of Arm Thumb/Thumb-2 mixed 16- and 32-bit instructions delivers the high performance expected of a 32-bit Arm
- Single-cycle multiply instruction
- VTOR supporting offset of the vector table base address
- Serial Wire debug with HW break-point comparators
- Ultra-low-power consumption with integrated sleep modes
- SysTick timer
- 48 MHz operation
- 0.99 DMIPS/MHz

Additionally, the CC2340Rx devices are compatible with all ARM tools and software.

8.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high performance and highly flexible RF sub system containing RF and baseband circuitry in addition to a software defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The software-defined modem is not programmable by customers but is instead loaded with pre-compiled images provided in the radio driver in the SimpleLink™ Low Power F3 software development kit (SDK) for the CC23xx devices. This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory, thus image loading from NV memory only occurs once after boot and also, no patching is required when exiting power modes.

8.3.1 Bluetooth 5.3 Low Energy

The RF Core offers full support for Bluetooth 5.3 Low Energy, including the high-speed 2 Mbps physical layer and the 500 kbps and 125 kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.3 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.3 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.3 enables fast, reliable firmware updates.

8.4 Memory

The 512 KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. A special flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static 36 KB RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution during boot.

The ROM includes device bootcode firmware handling initial device trimming operations, security configurations and device lifecycle management. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

8.5 Cryptography

The CC2340R5-Q1 device comes with AES-128 cryptography hardware accelerator, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerators supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AES GCM
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

The AES hardware accelerator can be fed with plaintext/ciphertext from either CPU or using DMA. Sustained throughput of one 16 byte ECB block per 23 cycles is possible corresponding to > 30 Mbps.

The CC2340R5-Q1 device supports Random Number Generation (RNG) using on-chip analog noise as the non-deterministic noise source for the purpose of generating a seed for a cryptographically secure counter deterministic random bit generator (CTR-DRBG) that in turn is used to generate random numbers for keys, initialization vectors (IVs), and other random number requirements. Hardware acceleration of AES CTR-DRBG is supported.

The CC2340R5-Q1 device includes a complete SHA 256 library in ROM, reducing the code footprint of the application. Uses cases may include generating digests for use in digital signature algorithms, data integrity checks, and password storage.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform.

8.6 Timers

A large selection of timers are available as part of the CC2340R5-Q1 device. These timers are:

- **Real-Time Clock (RTC)**

  The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. When the device enters the RESET or SHUTDOWN state the RTC is reset.

  The RTC accumulates time elapsed since reset on each LFCLK. The RTC counter is incremented by LFINC at a rate of 32.768 kHz. LFINC indicates the period of LFCLK in µs, with an additional granularity of 16 fractional bits.

  The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

  There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multi-channel and higher resolution SYSTIM remain in synchronization with the RTC's time base.

  The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.
- **System Timer (SYSTIM)**

  The SYSTIM is a 34-bit, 5-channel wrap-around timer with a per-channel selectable 32b slice with either a 1 us resolution and 1h11m35s range or 250 ns resolution and 17m54s range. All channels support both capture and single-shot compare (posting an event) operation. One channel is reserved for system software, three channels are reserved for radio software and one channel is freely available to user applications.

For software convenience a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base (albeit with different resolutions/spans). Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately trigger if the submitted event is in the immediate past (4.294s with 1 us resolution and 1.049s with 250 ns resolution).

- **General Purpose Timers (LGPT)**

  The CC2340R5-Q1 device provides four LGPTs with 3 × 16 bit timers and 1× 24 bit timer, all running up to 48 MHz. The LGPTs support a wide range of features such as:

  – 3 capture/compare channels
  – One-shot or periodic counting
  – Pulse width modulation (PWM)
  – Time counting between edges and edge counting
  – Input filter implemented on each of the channels for all timers
  – IR generation feature available on Timer-0 and Timer-1
  – Dead band feature available on Timer-1

  The timer capture/compare and PWM signals are connected to IOs via IO controller module (IOC) and the internal timer event connections to CPU, DMA and other peripherals are via the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. Two LGPTs (2× 16 bit timers) supports quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

表 8-1. Timer Comparison

Feature	Timer 0	Timer 1	Timer 2	Timer 3
Counter Width	16-bit	16-bit	16-bit	24-bit
Quadrature Decoder	Yes	No	Yes	No
Park Mode on Fault	No	Yes	No	No
Programmable Dead-Band Insertion	No	Yes	No	No

- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32 kHz clock rate and operates in device active, idle, and standby modes and cannot be stopped once enabled.

8.7 Serial Peripherals and I/O

The CC2340R5-Q1 device provides 1xUART, 1xSPI and 1xI2C serial peripherals

The SPI module supports both SPI controller and peripheral up to 12 MHz with configurable phase and polarity.

The UART module implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps and IRDA SIR mode of operation.

The I2C module is used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both controller and target.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open source. Some GPIOs have high-drive capabilities, which are marked in **bold** in セクション 6.

For more information, see the CC23xx SimpleLink™ Wireless MCU Technical Reference Manual.

8.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2340R5-Q1 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

8.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 8 channels, with 6 channels having dedicated peripheral interface and 2 channels having ability to be triggered via configurable events.
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

8.10 Debug

On-chip debug is supported through the serial wire debug (SWD) interface, which is an ARM bi-directional 2-wire protocol that communicates with the JTAG Test Access Port (TAP) controller and allows for complete debug functionality. SWD is fully compatible with Texas Instruments' XDS family of debug probes.

8.11 Power Management

To minimize power consumption, the CC2340R5-Q1 supports a number of power modes and power management features (see 表 8-2).

表 8-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES (1)				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
48 MHz high-speed clock (HFCLK)	HFOSC (tracks HFXT)	HFOSC (tracks HFXT)	Off	Off	Off
32 kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IOC, BATMON, RTC, LPCOMP	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	On	On
Watchdog timer (WDT)	Available	Available	Available	Off	Off

(1) “Available” indicates that the specific IP or feature can be enabled by user application in the corresponding device operating modes. “On” indicates that the specific IP or feature is turned on irrespective of the user application configuration of the device in the corresponding device operating mode. “Off” indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode

In the **Active** mode, both of MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU..

In **Idle** mode the CPU is in sleep but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on state of the DMA and debug subsystem.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only state retained in this mode are the latched I/O state, 3V register bank, and the flash memory contents.

注

The power, RF and clock management for the CC2340R5-Q1 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2340R5-Q1 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

8.12 Clock Systems

The CC2340R5-Q1 device has the following internal system clocks.

The 48 MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 48 MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48 MHz crystal (HFXT). Radio operation requires an external 48 MHz crystal.

The 32.768 kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer before or after Standby power mode. LFCLK can be driven by the internal 32.8 kHz RC Oscillator (LFOSC), a 32.768 kHz watch-type crystal, or clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32 kHz LFCLK signal to other devices, thereby reducing the overall system cost.

8.13 Network Processor

Depending on the product configuration, the CC2340R5-Q1 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC - with the application and protocol stack running on the system CPU inside the device).

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

9 Application, Implementation, and Layout

注

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9.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2340R5-Q1 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

LP-EM-CC2340R5 Design Files	The CC2340R5 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2340R5-Q1 device.
Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

9.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are two recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \quad (2)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

Example:

In this example, we assume a simple use case where the radio is transmitting continuously at 0 dBm output power. Let us assume we want to maintain a junction temperature equal or less than 85 °C and the supply voltage is 3 V. Using Equation 1, the temperature difference between the top of the case and junction temperature is calculated. To calculate P, look up the current consumption for Tx at 85 °C. At 85 °C the current consumption is approximately 5.5 mA. This means that P is 5.5 mA × 3 V = 16.5 mW.

The maximum case temperature to maintain and junction temperature of 85 °C is then calculated as:

$$T_{\mathrm{case}} < T_j - 0.4^{\circ C}/_{W} \times 23.4mW = 84.99^{\circ}C \quad (3)$$

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, and so on. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in the Measuring CC13xx and CC26xx Current Consumption application report.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RHB*).

For orderable part numbers of devices in the RHB (5-mm x 5-mm) package type, see the *Package Option Addendum* of this document, the Device Information in セクション 3, the TI website (www.ti.com), or contact your TI sales representative.

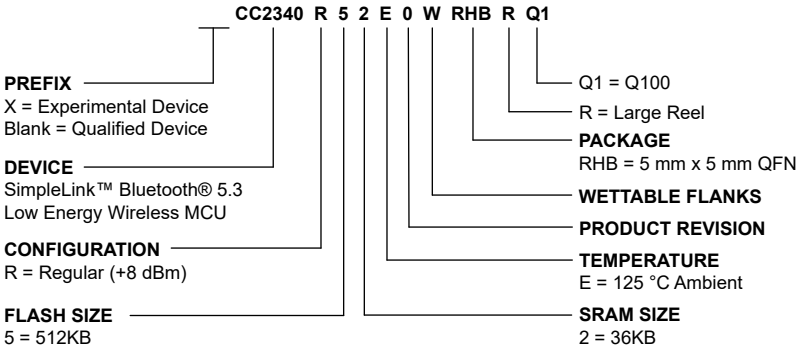

図 10-1. Device Nomenclature

10.2 Tools and Software

The CC2340R5-Q1 device is supported by a variety of software and hardware development tools.

Development Kit

CC2340R5 LaunchPad™ Development Kit

The CC2340R5 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2340R5 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and

Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ CC23xx software development kit (SDK)

The SimpleLink CC23xx software development kit (SDK) provides a complete package for the development of wireless applications on the CC23xx family of devices. The SDK includes a comprehensive software package for the CC2340R5-Q1 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.3

The SimpleLink CC23xx SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone

application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash — CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

10.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more at ti.com/simplelink.

10.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder (). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer — Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2340R5-Q1 Silicon Errata — The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2340R5-Q1 device are found on the device product folder ().

Technical Reference Manual (TRM)

CC23xx SimpleLink™ Wireless MCU TRM — The TRM provides a detailed description of all modules and peripherals available in the device family.

10.4 サポート・リソース

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Eclipse® is a registered trademark of Eclipse Foundation.
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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2340R52E0WRHBRQ1	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2340Q R52	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CC2340R5-Q1 :

- Catalog : CC2340R5

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

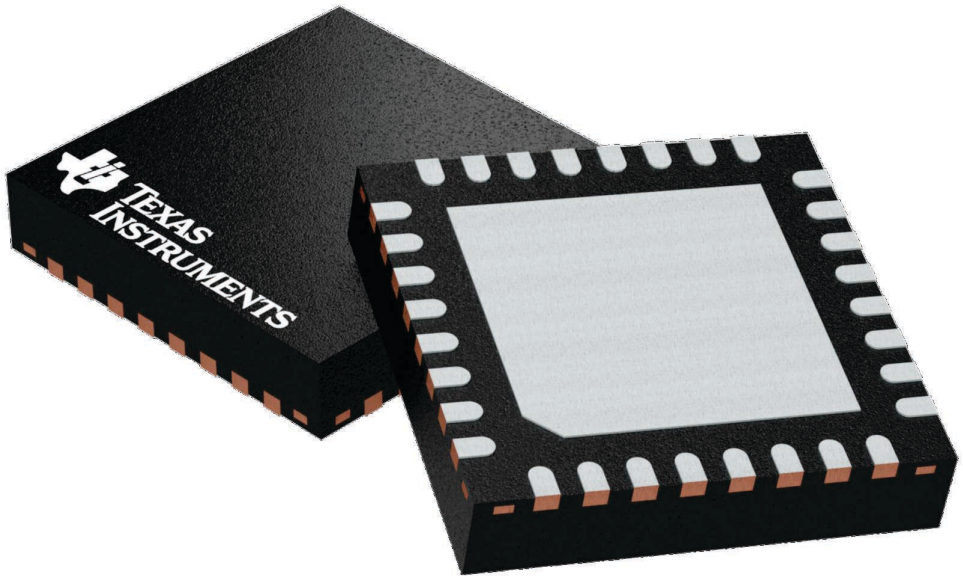
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

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