TEXAS INSTRUMENTS
CD54HCT125, CD74HCT125
JAJSMC5A – JUNE 2020 – REVISED AUGUST 2024

CDx4HCT125 クワッド バッファ、3 ステート出力

1 特長

- LSTTL 入力ロジック互換
  - $V_{IL(max)}$ = 0.8V、$V_{IH(min)}$ = 2V
- CMOS 入力ロジック互換
  - $I_I \leqq 1\mu A$ (V_{OL}、V_{OH})
- バッファ付き入力
- 4.5V～5.5V で動作
- 広い動作温度範囲：-55°C～+125°C
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

2 アプリケーション

- デジタル信号のイネーブル

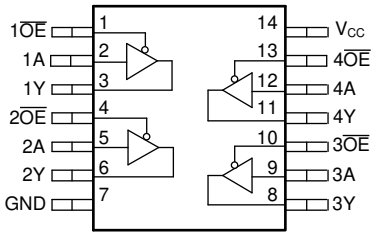
3 概要

このデバイスには、3 ステート出力を備えた 4 つの独立したバッファが内蔵されています。各ゲートはブール関数 Y = A を正論理で実行します。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (3)
CDx4HCT125	D (SOIC、14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP、14)	19.30mm × 9.4mm	19.30mm × 6.35mm
	J (CDIP、14)	19.56mm × 6.7mm	19.56mm × 4.57mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



機能的なピン配置

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4 Pin Configuration and Functions

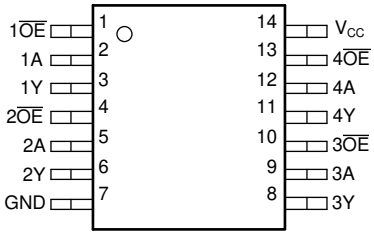


図 4-1. D, N, or J Package 14-Pin SOIC, PDIP, or CDIP Top View

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1 $\overline{OE}$	1	Input	Channel 1, Output Enable, Active Low
1A	2	Input	Channel 1, Input A
1Y	3	Output	Channel 1, Output Y
2 $\overline{OE}$	4	Input	Channel 2, Output Enable, Active Low
2A	5	Input	Channel 2, Input A
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3 $\overline{OE}$	10	Input	Channel 3, Output Enable, Active Low
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4 $\overline{OE}$	13	Input	Channel 4, Output Enable, Active Low
V_{CC}	14	—	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
	Lead temperature (soldering 10s)	SOIC - lead tips only		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition time	V_{CC} = 4.5 V			500	ns
		V_{CC} = 5.5 V			400	
T_A	Operating free-air temperature		–55		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		CD74HCT125		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.8	138.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	91.6	93.8	°C/W

THERMAL METRIC(1)		CD74HCT125		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	83.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.1	49.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.4	94.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4			4.4			4.4			V
			I_{OH} = –4 mA	4.5 V	3.98			3.84			3.7			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	4.5 V			0.1			0.1			0.1	V
			I_{OL} = 4 mA	4.5 V			0.26			0.33			0.4	
I_I	Input leakage current	V_I = V_{CC} and GND	I_O = 0	5.5 V			±0.1			±1			±1	µA
I_{OZ}	Three-state leakage current	V_I = V_{IH} or V_{IL}		5.5 V			±0.5			±5			±10	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	I_O = 0	5.5 V			8			80			160	µA
ΔI_{CC} (1)	Additional Quiescent Device Current Per Input Pin.	V_I = V_{CC} – 2.1		4.5 V to 5.5 V		100	360			450			490	µA
C_i	Input capacitance						10			10			10	pF
C_o	Three-state output capacitance						20			20			20	pF

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

PARAMETER		FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
						25°C			–40°C to 85°C			–55°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A	Y	C_L = 50 pF	4.5 V			25			31			38	ns
				C_L = 15 pF	5 V		10								
t_{en}	Enable delay	$\overline{OE}$	Y	C_L = 50 pF	4.5 V			25			31			38	ns
				C_L = 15 pF	5 V		10								
t_{dis}	Disable delay	$\overline{OE}$	Y	C_L = 50 pF	4.5 V			28			35			42	ns
				C_L = 15 pF	5 V		11								
t_t	Transition-time		Y	C_L = 50 pF	4.5 V			12			15			18	ns

5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	5 V		34		pF

5.8 Typical Characteristics

T_A = 25°C

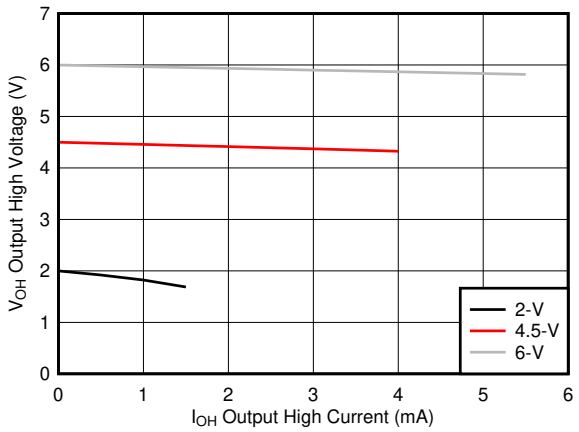


図 5-1. Typical output voltage in the high state (V_{OH})

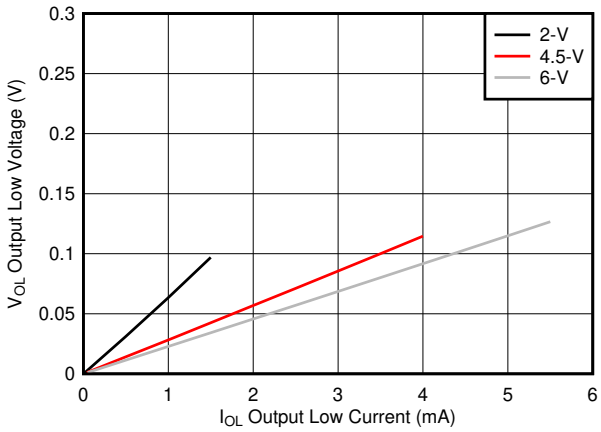
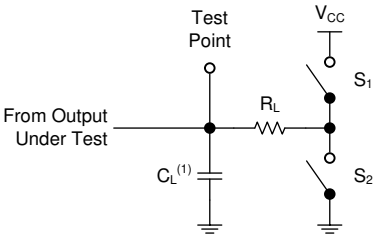


図 5-2. Typical output voltage in the low state (V_{OL})

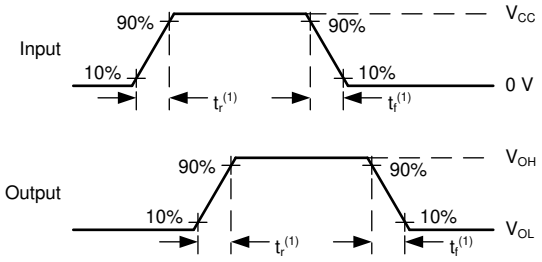
6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



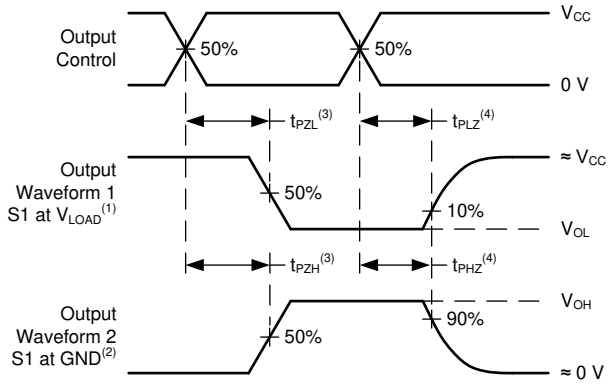
A. C_L = 50 pF and includes probe and jig capacitance.

図 6-1. Load Circuit



A. t_t is the greater of t_r and t_f.

図 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd}.

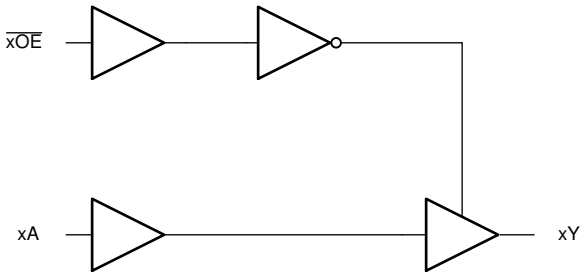
図 6-3. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function Y = A in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the セクション 5.1 must be followed at all times.

The CD74HCT125 can drive a load with a total capacitance less than or equal to the maximum load listed in the セクション 5.6 connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the セクション 5.1 .

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the I_{OZ} specification in the セクション 5.5 . A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

7.3.2 TTL-Compatible CMOS Inputs

TTL-Compatible CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the セクション 5.5 . The worst case resistance is calculated with the maximum input voltage, given in the セクション 5.1 , and the maximum input leakage current, given in the セクション 5.5 , using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the セクション 5.3 to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the TTL-compatible CMOS input.

TTL-Compatible CMOS inputs have a lower threshold voltage than standard CMOS inputs to allow for compatibility with older bipolar logic devices. See the セクション 5.3 for the valid input voltages for the CD74HCT125.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 図 7-1.

注意

Voltages beyond the values specified in the セクション 5.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

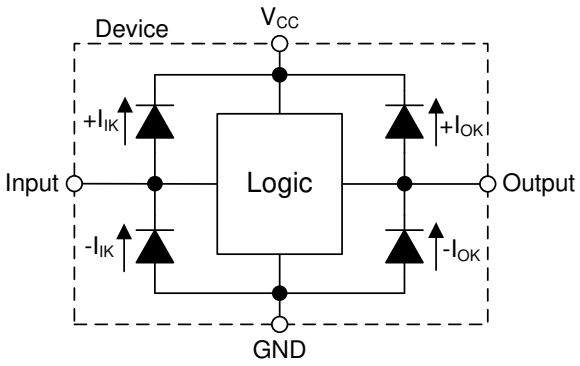


図 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS(1)		OUTPUT(2)
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

注

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8.1 Application Information

In this application, a 3-state buffer is used to enable or disable a data connection as shown in *図 8-1* . It is common to see all four channels of a device used together for controlling a 4-bit data bus, however each channel of the device can be used independently. Unused channels should have the inputs terminated at ground or V_{CC} and the output left unconnected.

When the output of the device is active, the data signal will be replicated at the output. When the output of the device is disabled, the output will be in a high-impedance state, and the output voltage will be determined by the circuit connected to the output pin. This circuit is most commonly used when a bus must be completely disabled. One example of this situation is when the circuitry connected to the output is to be powered off for an extended period of time to save system power, and the inputs to that circuitry cannot have a voltage present due to protective clamp diodes.

8.2 Typical Application

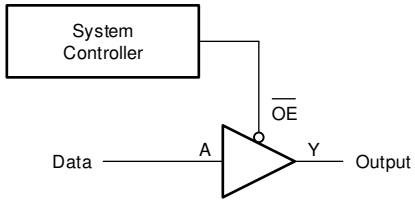

図 8-1. Typical application schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *セクション 5.3* . The supply voltage sets the device's electrical characteristics as described in the *セクション 5.5* .

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HCT125 plus the maximum supply current, I_{CC}, listed in the *セクション 5.5* . The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *セクション 5.1* .

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

注意

The maximum junction temperature, T_J(max) listed in the *セクション 5.1* , is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *セクション 5.1* . These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HCT125, as specified in the *セクション 5.5* , and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

Refer to the *セクション 7.3* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *セクション 5.5* . Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *セクション 5.5* .

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *セクション 7.3* for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *セクション 8.4* .
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HCT125 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω. This will ensure that the maximum output current from the *セクション 5.1* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

8.2.3 Application Curves

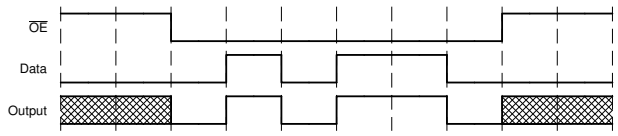

図 8-2. Typical application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *セクション 5.3* . Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *図 8-3* .

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a

triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

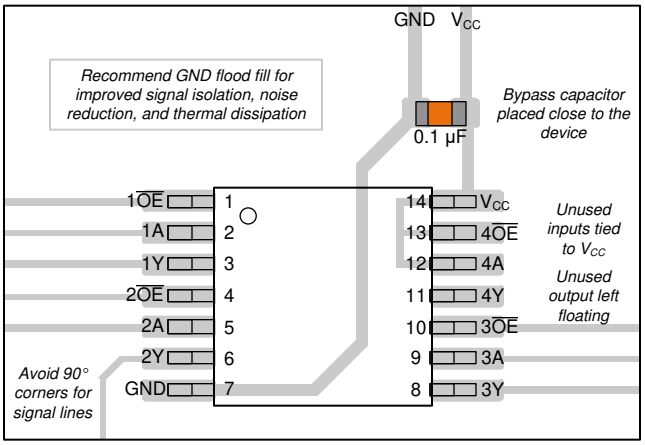

図 8-3. Example layout for the CD74HCT125

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision * (June 2020) to Revision A (August 2024)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1
• 「製品情報」の表にパッケージ サイズを追加	1
• Updated RθJA values: D = 96.7 to 138.7, N = 61.5 to 103.8; Updated D and N packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HCT125F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT125F3A	Samples
CD74HCT125E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT125E	Samples
CD74HCT125M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT125M	
CD74HCT125M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125M96E4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT125M	Samples
CD74HCT125MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT125M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HCT125, CD74HCT125 :

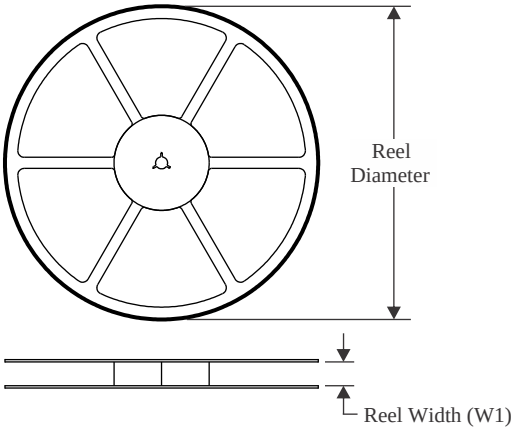
- Catalog : CD74HCT125
- Military : CD54HCT125

NOTE: Qualified Version Definitions:

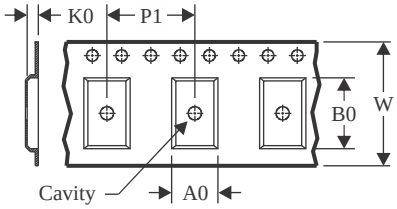
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

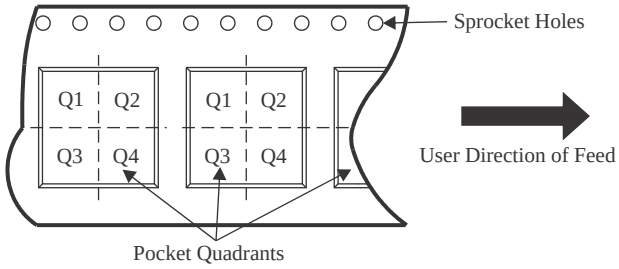


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

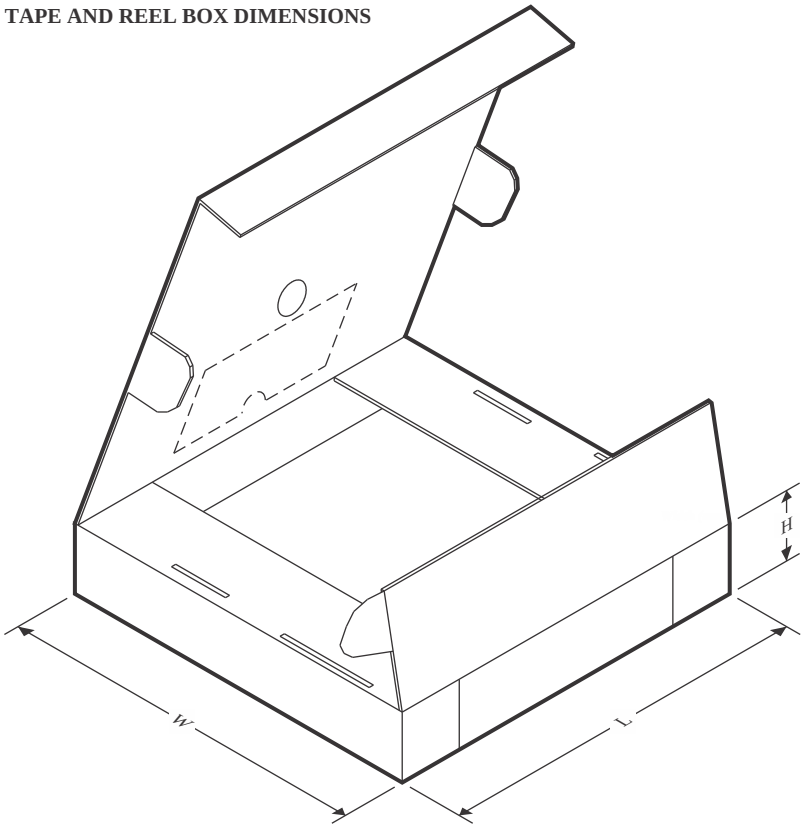
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96E4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT125M96E4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

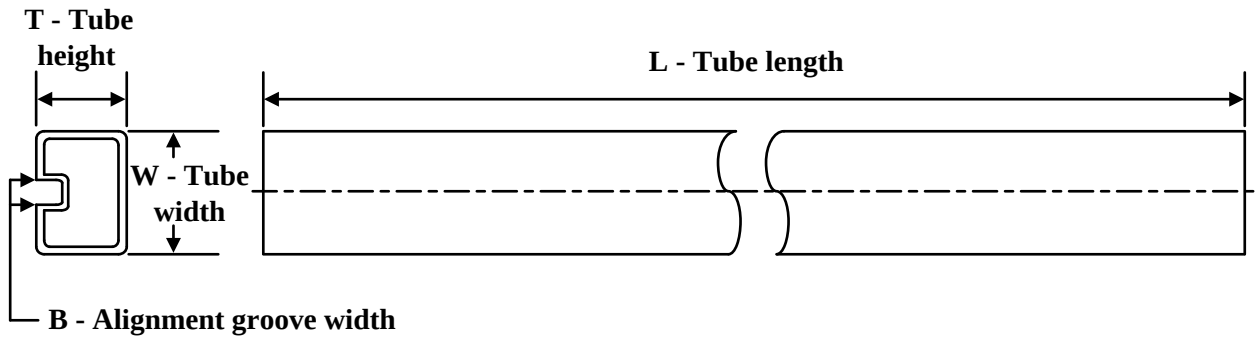
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT125M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96E4	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT125M96E4	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



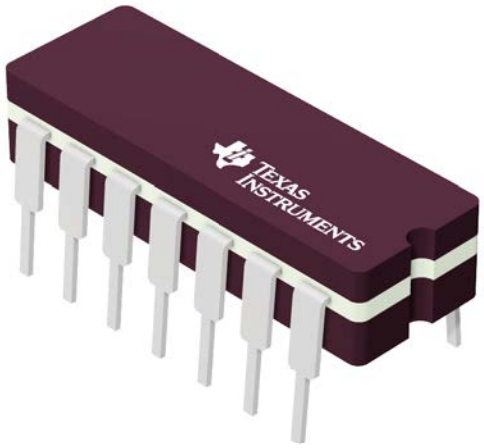
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HCT125E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT125E	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

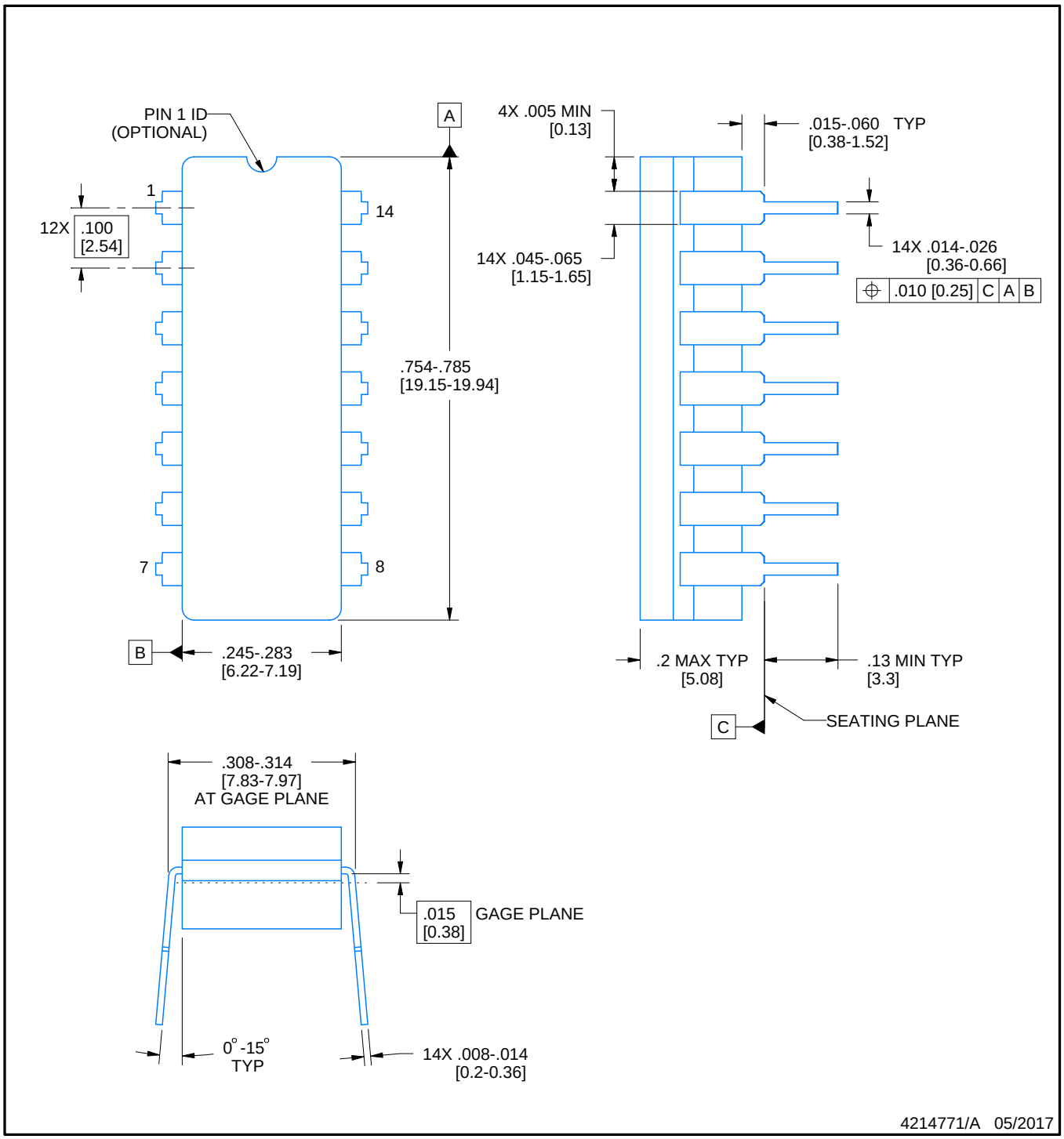
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

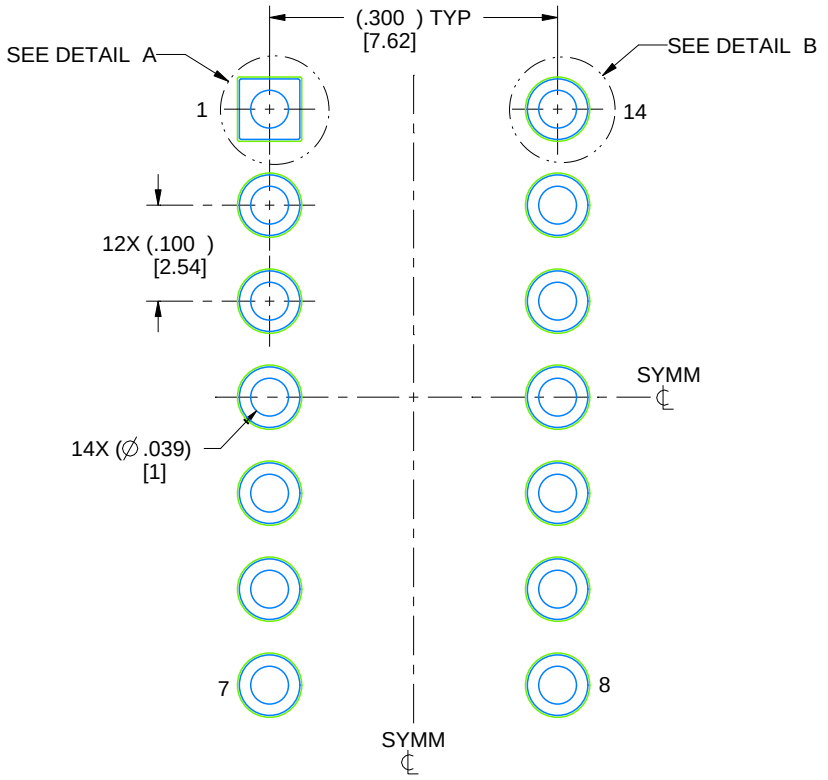
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

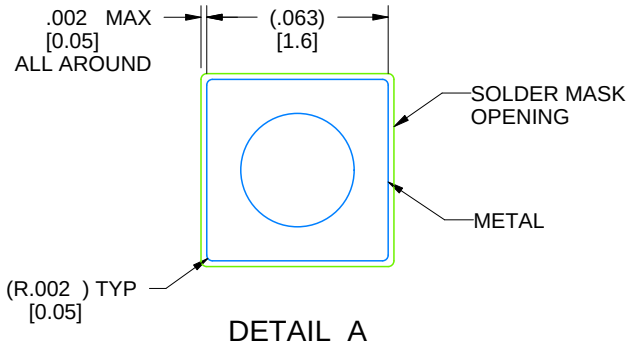
J0014A

CDIP - 5.08 mm max height

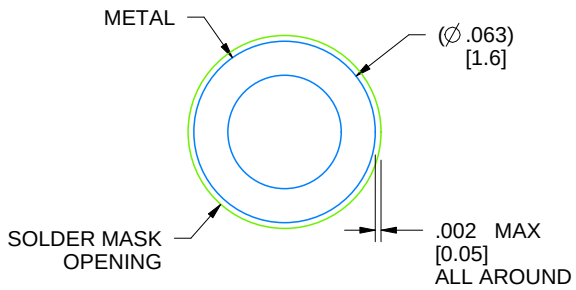
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



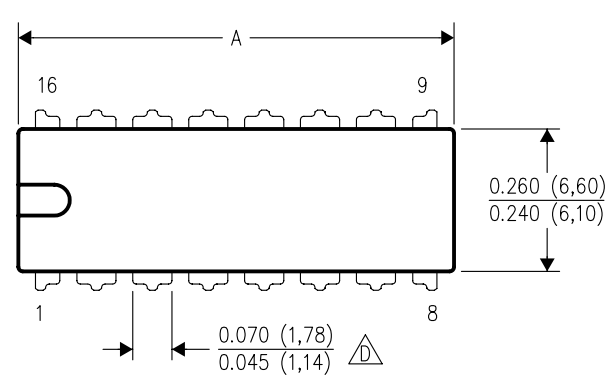
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

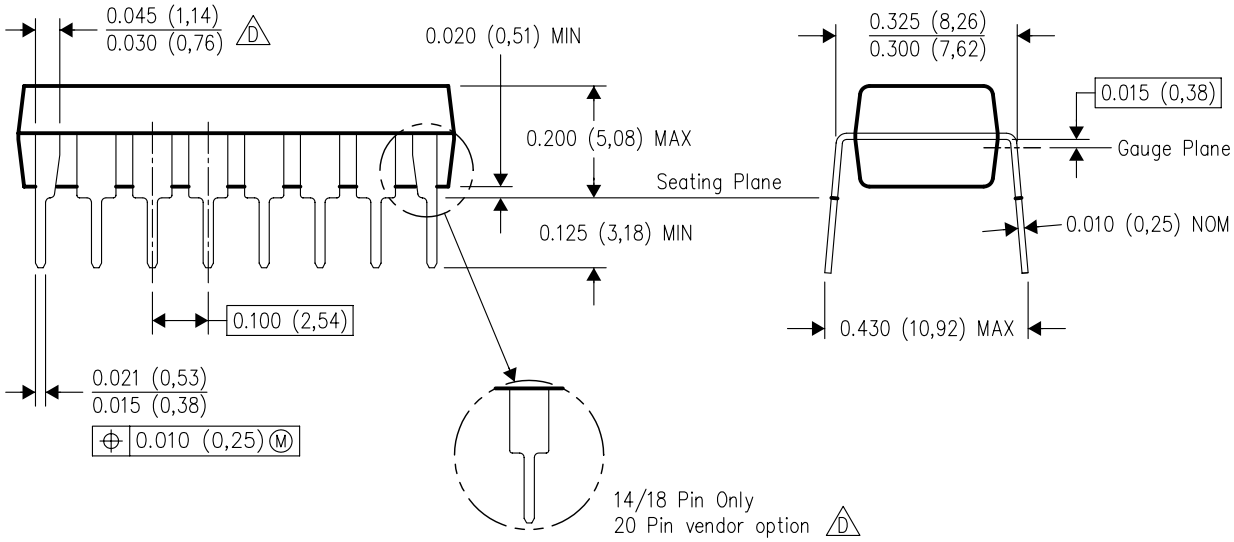
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

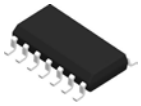


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

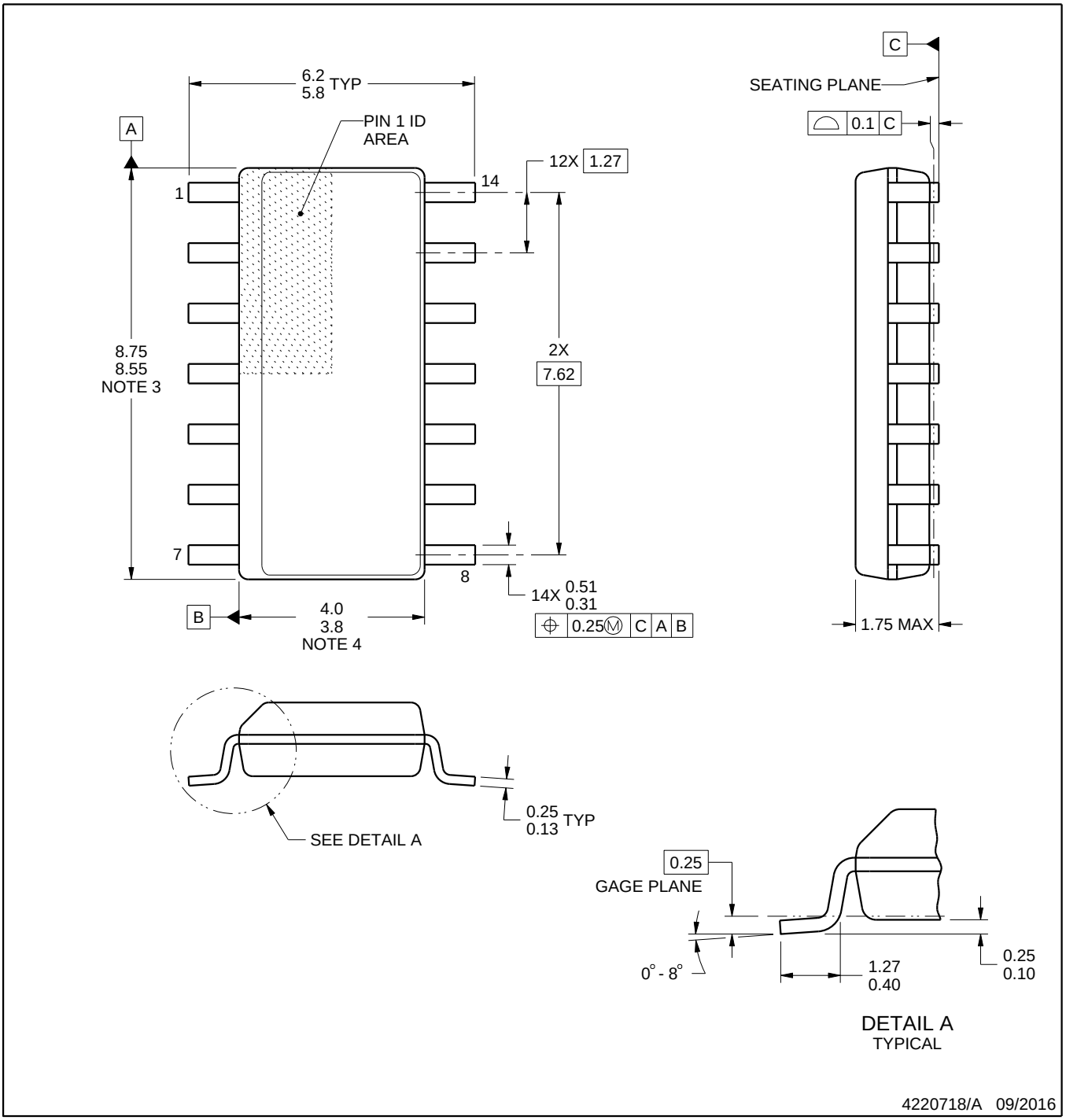


PACKAGE OUTLINE

D0014A

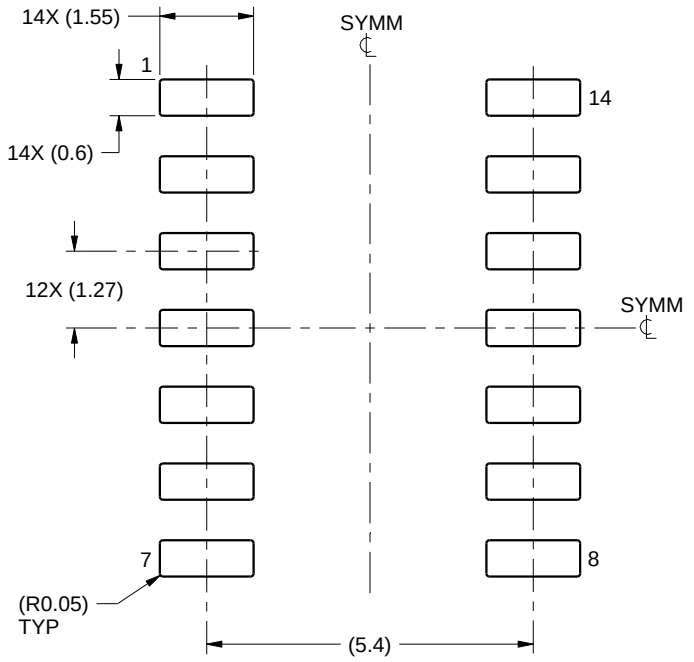
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

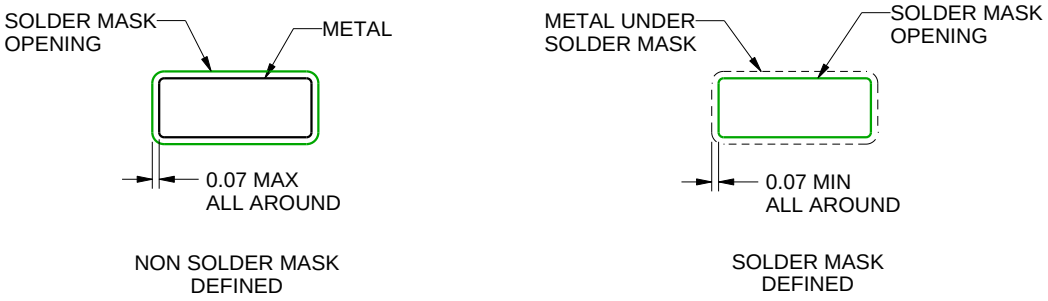


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

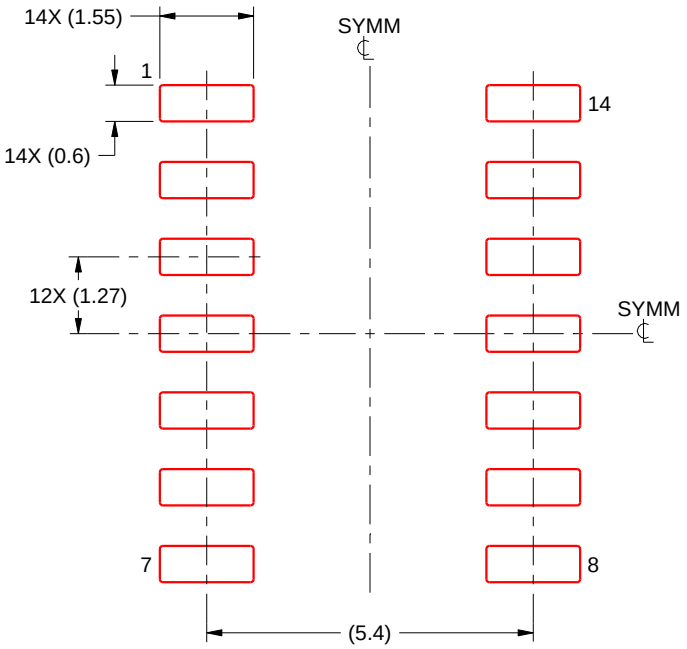
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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