CD54AC112, CD74AC112
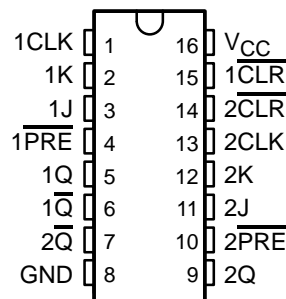## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC112 . . . F PACKAGE
CD74AC112 . . . E OR M PACKAGE
(TOP VIEW)

1CLK	1	16	V_{CC}
1K	2	15	1$\overline{CLR}$
1J	3	14	2$\overline{CLR}$
1$\overline{PRE}$	4	13	2CLK
1Q	5	12	2K
1$\overline{Q}$	6	11	2J
2$\overline{Q}$	7	10	2$\overline{PRE}$
GND	8	9	2Q

description/ordering information

The 'AC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse (CLK). Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP – E	Tube	CD74AC112E	CD74AC112E
	SOIC – M	Tube	CD74AC112M	AC112M
		Tape and reel	CD74AC112M96	
	CDIP – F	Tube	CD54AC112F3A	CD54AC112F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† Output states are unpredictable if $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ go high simultaneously after both being low at the same time.

logic diagram (positive logic)
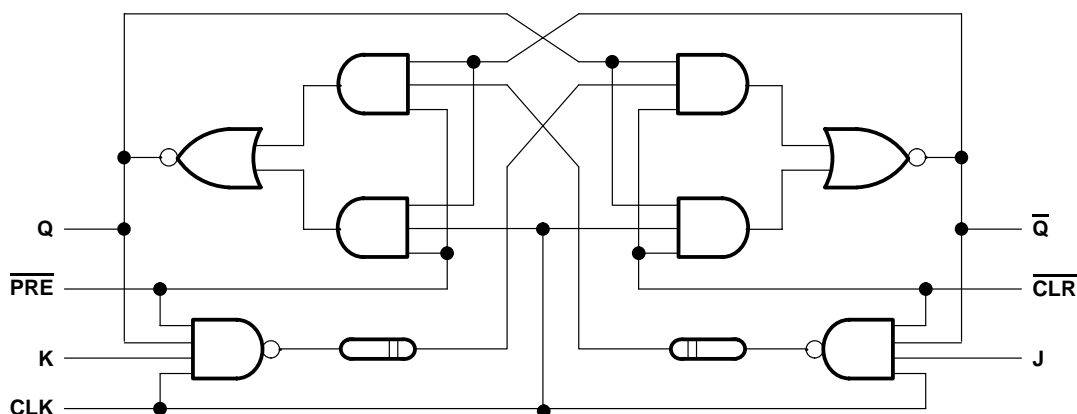
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1) . . . . ±50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package . . . . 67°C/W
                                                    M package . . . . 73°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
        2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			$T_A = 25°C$		$-55°C$ to $125°C$		$-40°C$ to $85°C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		-24		-24		-24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50		50		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20		20		20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$		$-55°C$ to $125°C$		$-40°C$ to $85°C$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50$ μA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		$I_{OH} = -4$ mA	3 V	2.58		2.4		2.48		
		$I_{OH} = -24$ mA	4.5 V	3.94		3.7		3.8		
		$I_{OH} = -50$ mA†	5.5 V			3.85				
		$I_{OH} = -75$ mA†	5.5 V					3.85		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		$I_{OL} = 12$ mA	3 V		0.36		0.5		0.44	
		$I_{OL} = 24$ mA	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50$ mA†	5.5 V				1.65			
		$I_{OL} = 75$ mA†	5.5 V						1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V		4		80		40	μA
C_i					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

timing requirements over recommended operating free-air temperature range, V_{CC} = 1.5 V (unless otherwise noted)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			8		9	MHz
t_w	Pulse duration	CLK high or low	63		55		ns
		$\overline{CLR}$ or $\overline{PRE}$ low	56		49		
t_{su}	Setup time, before CLK↓	J or K	50		44		ns
t_h	Hold time, after CLK↓	J or K	0		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{CLR}$↑ or $\overline{PRE}$↑	31		27		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			71		81	MHz
t_w	Pulse duration	CLK high or low	7		6		ns
		$\overline{CLR}$ or $\overline{PRE}$ low	6.3		5.5		
t_{su}	Setup time, before CLK↓	J or K	5.6		4.9		ns
t_h	Hold time, after CLK↓	J or K	0		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{CLR}$↑ or $\overline{PRE}$↑	3.5		3..1		ns

timing requirements over recommended operating free-air temperature₀ range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			100		114	MHz
t_w	Pulse duration	CLK high or low	5		4.4		ns
		$\overline{CLR}$ or $\overline{PRE}$ low	4.5		3.9		
t_{su}	Setup time, before CLK↓	J or K	4		3.5		ns
t_h	Hold time, after CLK↓	J or K	0		0		ns
t_{rec}	Recovery time, before CLK↓	$\overline{CLR}$↑ or $\overline{PRE}$↑	2.5		2.2		ns

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Q or $\overline{Q}$		129		117	ns
	$\overline{CLR}$ or $\overline{PRE}$			153		139	
t_{PHL}	CLK	Q or $\overline{Q}$		129		117	ns
	$\overline{CLR}$ or $\overline{PRE}$			153		139	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			71		81		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3.6	14.4	3.7	13.1	ns
	$\overline{CLR}$ or $\overline{PRE}$		4.3	17.1	4.4	15.5	
t_{PHL}	CLK	Q or $\overline{Q}$	3.6	14.4	3.7	13.1	ns
	$\overline{CLR}$ or $\overline{PRE}$		4.3	17.1	4.4	15.5	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100		114		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	2.6	10.3	2.7	9.4	ns
	$\overline{CLR}$ or $\overline{PRE}$		3.1	12.2	3.2	11.1	
t_{PHL}	CLK	Q or $\overline{Q}$	2.6	10.3	2.7	9.4	ns
	$\overline{CLR}$ or $\overline{PRE}$		3.1	12.2	3.2	11.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	56	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
RECOVERY TIME

VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC112F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC112F3A
CD54AC112F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC112F3A
CD74AC112E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC112E
CD74AC112E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC112E
CD74AC112M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	AC112M
CD74AC112M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC112M
CD74AC112M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC112M

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC112, CD74AC112 :

● Catalog : CD74AC112

● Military : CD54AC112

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Military - QML certified for Military and Defense Applications

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

K0 P1 B0 W Cavity A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 | Q2 Q1 | Q2
Q3 | Q4 Q3 | Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC112M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC112M96	SOIC	D	16	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC112E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC112E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC112E.A	N	PDIP	16	25	506	13.97	11230	4.32

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

C

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) D

0.045 (1,14) / 0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)   0.020 (0,51)
                      0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                                    0.004 (0,10)

0.010 (0,25)
0.005 (0,13)
                                              ⌒ | 0.004 (0,10)

Gauge Plane
                                                  Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0.006 (0,15) each side.
       ⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER