

CDx4AC153 デュアル、4 ライン入力 1 ライン出力、データ セレクタ / マルチプレクサ

1 特長

- AC タイプは 1.5V~5.5V で動作、電源の 30% での平衡ノイズ耐性を実現
- バイポーラ F、AS、S の速度と消費電力の大幅な低減
- 伝搬遅延時間の平衡化
- ±24mA 出力駆動電流
 - 15 F デバイスへのファンアウト
- SCR ラッチアップ耐性の高い CMOS プロセスと回路設計
- MIL-STD-883、Method 3015 に準拠した 2kV を超える ESD 保護

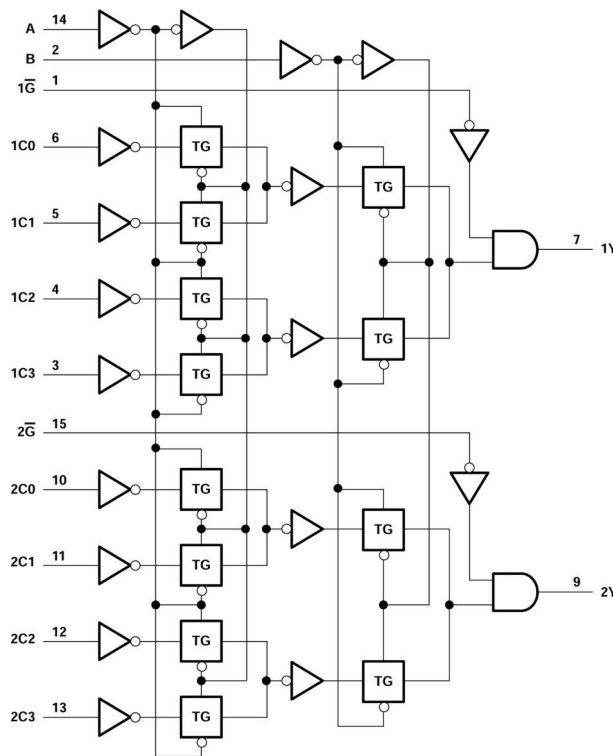
2 概要

これらの各データ セレクタ / マルチプレクサには、フル バイナリ デコード データ選択を AND-OR ゲートに供給するためのインバータとドライバが含まれています。2 つの 4 ライン選択のそれぞれに、独立したストロブ (\overline{G}) 入力が入用されています。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | パッケージ サイズ ⁽²⁾ | 本体サイズ ⁽³⁾ |
|-----------|----------------------|--------------------------|----------------------|
| CDx4AC153 | N (PDIP, 16) | 19.3mm × 9.4 mm | 19.3mm × 6.35 mm |
| | D (SOIC, 16) | 9.9mm × 6 mm | 9.9mm × 3.9 mm |

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれません。



論理図 (正論理)



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3 Pin Configuration and Functions

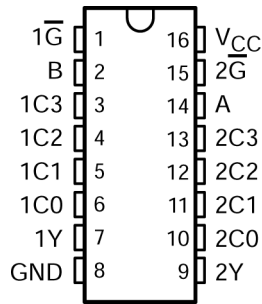


図 3-1. CD54AC153 J Package, 16-Pin CDIP; CD74AC153 N or D Package; 16-Pin PDIP or SOIC (Top View)

表 3-1. Pin Functions

| PIN | | TYPE ¹ | DESCRIPTION |
|--------------------|-----------------|-------------------|--------------------------------------|
| SOIC または TSSOP NO. | NAME | | |
| 1 | 1Ḡ | I | Channel 1, output strobe, active low |
| 2 | B | I | Address select B |
| 3 | 1C3 | I | Channel 1, data input 3 |
| 4 | 1C2 | I | Channel 1, data input 2 |
| 5 | 1C1 | I | Channel 1, data input 1 |
| 6 | 1C0 | I | Channel 1, data input 0 |
| 7 | 1Y | O | Channel 1, data output |
| 8 | GND | — | Ground |
| 9 | 2Y | I | Channel 2, data output |
| 10 | 2C0 | I | Channel 2, data input 0 |
| 11 | 2C1 | I | Channel 2, data input 1 |
| 12 | 2C2 | I | Channel 2, data input 2 |
| 13 | 2C3 | I | Channel 2, data input 3 |
| 14 | A | I | Address select A |
| 15 | 2Ḡ | I | Channel 2, output strobe, active low |
| 16 | V _{CC} | — | Positive supply |

1. I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------------------|---|---|-----|---------|
| V _{CC} | Supply voltage range | -0.5 | 6 | V |
| I _{IK} ⁽²⁾ | Input clamp current | (V _I < 0 or V _I > V _{CC}) | | ±20 mA |
| I _{OK} ⁽²⁾ | Output clamp current | (V _O < 0 or V _O > V _{CC}) | | ±50 mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | | ±50 mA |
| | Continuous current through V _{CC} or GND | | | ±100 mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|---------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾ | ±2000 V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | T _A = 25°C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------|----------------|-----------------|---------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 1.5 V | | 1.2 | | 1.2 | | V |
| | | V _{CC} = 3 V | | 2.1 | | 2.1 | | |
| | | V _{CC} = 5.5 V | | 3.85 | | 3.85 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.5 V | | 0.3 | | 0.3 | | V |
| | | V _{CC} = 3 V | | 0.9 | | 0.9 | | |
| | | V _{CC} = 5.5 V | | 1.65 | | 1.65 | | |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 4.5 V to 5.5 V | | -24 | | -24 | | mA |
| I _{OL} | Low-level output current | V _{CC} = 4.5 V to 5.5 V | | 24 | | 24 | | mA |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.5 V to 3 V | | 50 | | 50 | | ns/V |
| | | V _{CC} = 3.6 V to 5.5 V | | 20 | | 20 | | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D (SOIC) | N (PDIP) | UNIT |
|-------------------------------|--|----------|----------|------|
| | | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 119.9 | 67 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25 °C | | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|---|---|---|-----------------|------------------------|------|----------------|-----|---------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -50 μA | 1.5 V | 1.4 | 1.4 | 1.4 | 1.4 | V | | |
| | | | 3 V | 2.9 | 2.9 | 2.9 | | | | |
| | | | 4.5 V | 4.4 | 4.4 | 4.4 | | | | |
| | | I _{OH} = -4 mA | 3 V | 2.58 | 2.4 | 2.48 | | | | |
| | | I _{OH} = -24 mA | 4.5 V | 3.94 | 3.7 | 3.8 | | | | |
| | | I _{OH} = -50 mA ⁽¹⁾ | 5.5 V | | 3.85 | | | | | |
| I _{OH} = -75 mA ⁽¹⁾ | 5.5 V | | | 3.85 | | | | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 50 μA | 1.5 V | 0.1 | 0.1 | 0.1 | V | | | |
| | | | 3 V | 0.1 | 0.1 | 0.1 | | | | |
| | | | 4.5 V | 0.1 | 0.1 | 0.1 | | | | |
| | | I _{OL} = 12 mA | 3 V | 0.36 | 0.5 | 0.44 | | | | |
| | | I _{OL} = 24 mA | 4.5 V | 0.36 | 0.5 | 0.44 | | | | |
| | | I _{OL} = 50 mA ⁽¹⁾ | 5.5 V | | 1.65 | | | | | |
| I _{OL} = 75 mA ⁽¹⁾ | 5.5 V | | | 1.65 | | | | | | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | ±0.1 | ±1 | ±1 | μA | | | |
| I _{CC} | V _I = V _{CC} or GND, | I _O = 0 | 5.5 V | 8 | 160 | 80 | μA | | | |
| C _i | | | | 10 | 10 | 10 | pF | | | |

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

4.6 Switching Characteristics, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|------------------|--------------|-------------|----------------|-----|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | 250 | | 227 | | ns |
| t _{PHL} | | | 250 | | 227 | | |
| t _{PLH} | Any C | Y | 166 | | 151 | | ns |
| t _{PHL} | | | 166 | | 151 | | |
| t _{PLH} | \bar{G} | Y | 148 | | 134 | | ns |
| t _{PHL} | | | 148 | | 134 | | |

4.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, C_L = 50 pF (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|------------------|--------------|-------------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | 7 | 28 | 7.2 | 25.5 | ns |
| t _{PHL} | | | 7 | 28 | 7.2 | 25.5 | |
| t _{PLH} | Any C | Y | 4.7 | 18.6 | 4.8 | 16.9 | ns |
| t _{PHL} | | | 4.7 | 18.6 | 4.8 | 16.9 | |

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 over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|-----------|--------------|-------------|----------------|------|---------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | \bar{G} | Y | 4.1 | 16.5 | 4.3 | 15 | ns |
| t_{PHL} | | | 4.1 | 16.5 | 4.3 | 15 | |

4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

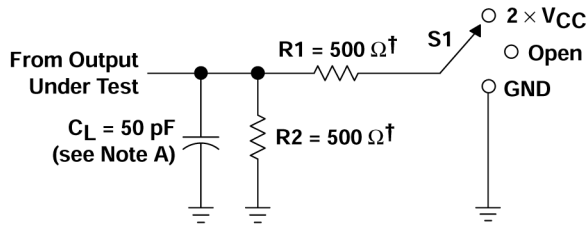
 over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -55°C to 125°C | | -40°C to 85°C | | UNIT |
|-----------|--------------|-------------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | Y | 5 | 20 | 5.2 | 18.2 | ns |
| t_{PHL} | | | 5 | 20 | 5.2 | 18.2 | |
| t_{PLH} | Any C | Y | 3.3 | 13.3 | 3.4 | 12.1 | ns |
| t_{PHL} | | | 3.3 | 13.3 | 3.4 | 12.1 | |
| t_{PLH} | \bar{G} | Y | 3 | 11.8 | 3.1 | 10.7 | ns |
| t_{PHL} | | | 3 | 11.8 | 3.1 | 10.7 | |

4.9 Operating Characteristics
 $T_A = 25^\circ\text{C}$

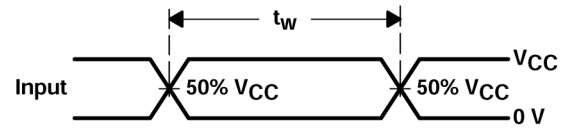
| PARAMETER | | TYP | UNIT |
|-----------|-------------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | 93 | pF |

5 Parameter Measurement Information

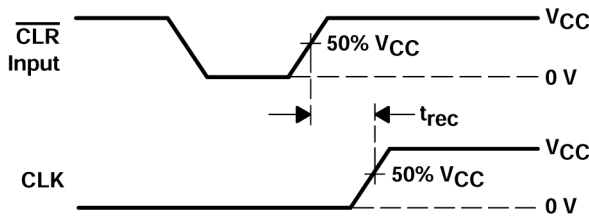


† When $V_{CC} = 1.5 \text{ V}$, $R_1 = R_2 = 1 \text{ k}\Omega$

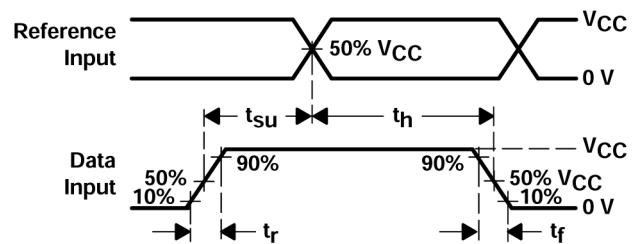
LOAD CIRCUIT



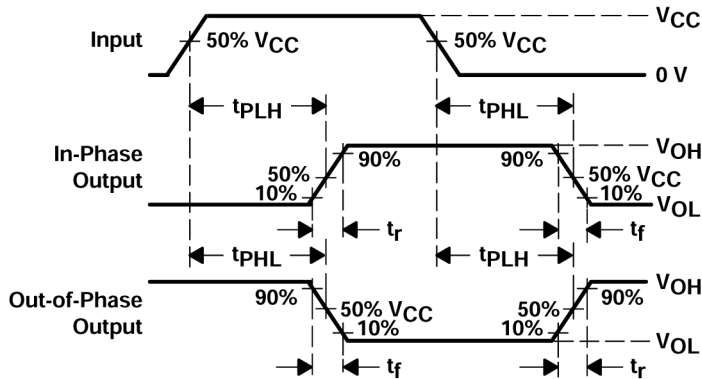
VOLTAGE WAVEFORMS
PULSE DURATION



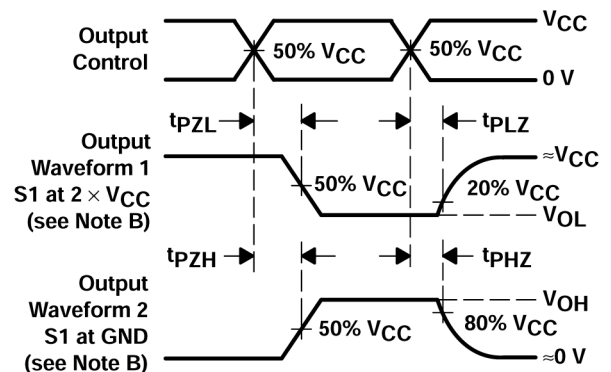
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
- For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- All parameters and waveforms are not applicable to all devices.

5-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

6 Detailed Description

6.1 Functional Block Diagram

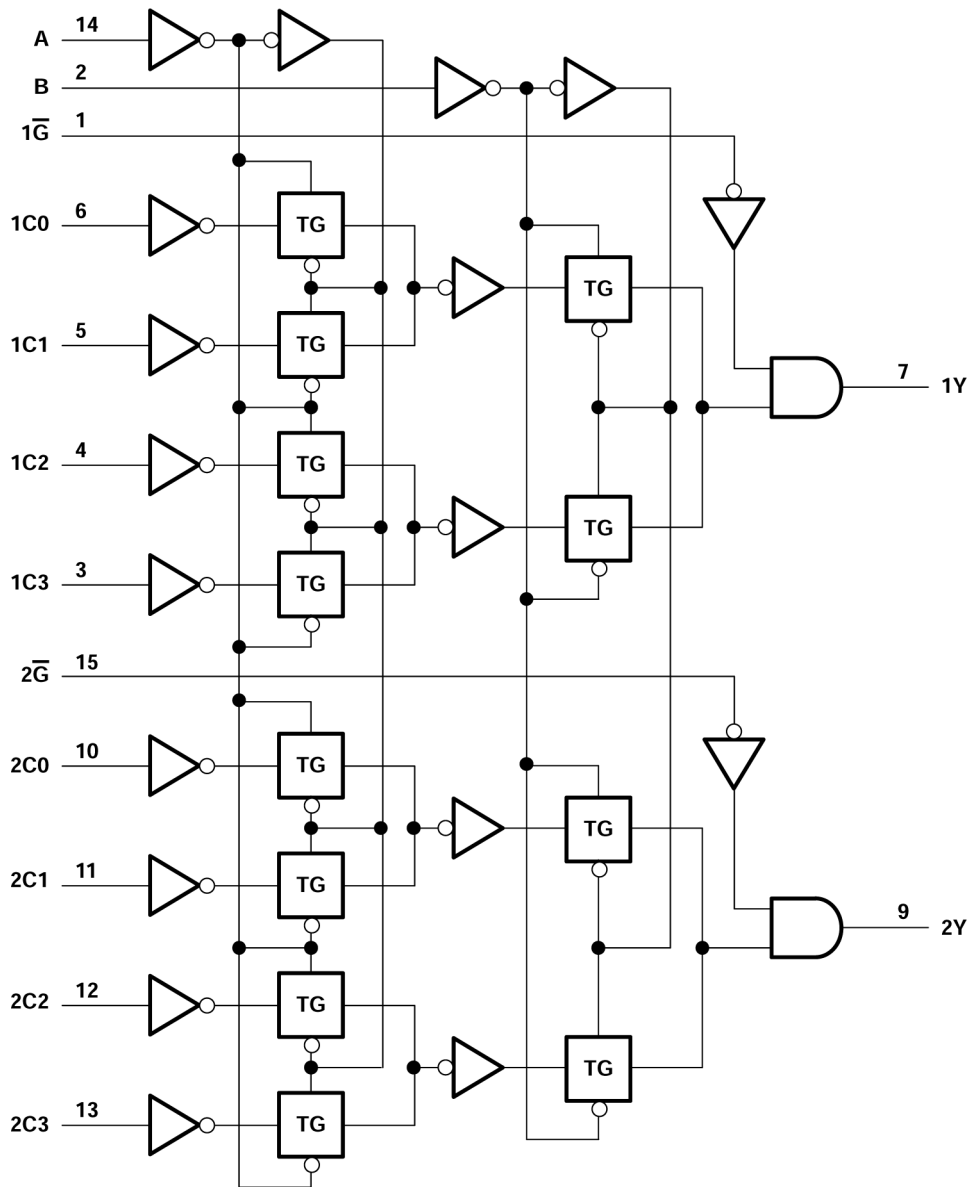


図 6-1. Logic Diagram (Positive Logic)

6.2 Device Functional Modes

表 6-1. Function Table

| INPUTS | | | | | | | G | OUTPUT Y |
|-----------------------|---|------|----|----|----|---|---|----------|
| SELECT ⁽¹⁾ | | DATA | | | | | | |
| B | A | C0 | C1 | C2 | C3 | | | |
| X | X | X | X | X | X | H | L | |
| L | L | L | X | X | X | L | L | |
| L | L | H | X | X | X | L | H | |
| L | H | X | L | X | X | L | L | |

表 6-1. Function Table (続き)

| INPUTS | | | | | | | OUTPUT Y |
|-----------------------|---|------|----|----|----|-----------|----------|
| SELECT ⁽¹⁾ | | DATA | | | | \bar{G} | |
| B | A | C0 | C1 | C2 | C3 | | |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

(1) Select inputs A and B are common to both sections.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [セクション 4.3](#).

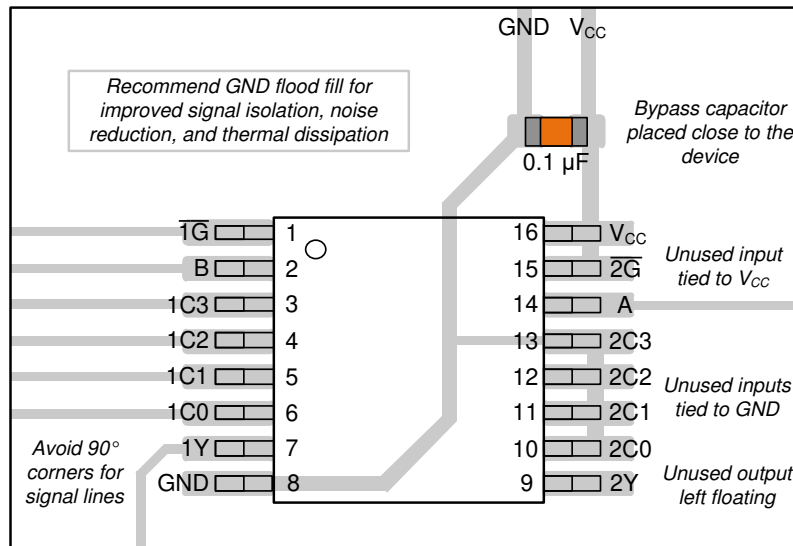
Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example



7-1. Example Layout for the CD74AC153

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CD54AC153 | Click here | Click here | Click here | Click here | Click here |
| CD74AC153 | Click here | Click here | Click here | Click here | Click here |

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision A (May 2003) to Revision B (July 2024) | Page |
|---|------|
| • 「製品情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加..... | 1 |
| • Updated RθJA values: D = 73 to 119.9, all values in °C/W..... | 4 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD54AC153F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54AC153F3A | Samples |
| CD74AC153E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC153E | Samples |
| CD74AC153M | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -55 to 125 | AC153M | |
| CD74AC153M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC153M | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54AC153, CD74AC153 :

- Catalog : [CD74AC153](#)
- Military : [CD54AC153](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC153M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74AC153M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC153M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74AC153M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74AC153E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC153E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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