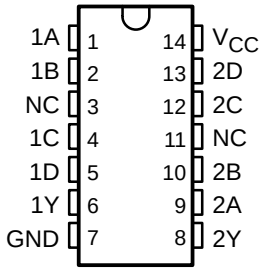
- **Inputs Are TTL-Voltage Compatible**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  - **Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

**CD54ACT20 . . . F PACKAGE**
**CD74ACT20 . . . E OR M PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’ACT20 devices contain two independent 4-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | PDIP – E | Tube | CD74ACT20E | CD74ACT20E |
| | SOIC – M | Tube | CD74ACT20M | ACT20M |
| | | Tape and reel | CD74ACT20M96 | |
| | CDIP – F | Tube | CD54ACT20F3A | CD54ACT20F3A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

## logic diagram (positive logic)


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package . . . . . 80°C/W
M package . . . . . 86°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | $T_A$ = 25°C | | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | | 10 | ns/V |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –50 μA | 4.5 V | 4.4 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | | | 3.85 | | | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | | | | | 3.85 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 4 | | 80 | | 40 | μA |
| $\Delta I_{CC}$‡ | $V_I = V_{CC}$ – 2.1 V | | 4.5 V to 5.5 V | | 2.4 | | 3 | | 2.8 | mA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.
‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

**ACT INPUT LOAD TABLE**

| INPUT | UNIT LOAD |
|---|---|
| All | 0.27 |

Unit Load is $\Delta I_{CC}$ limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

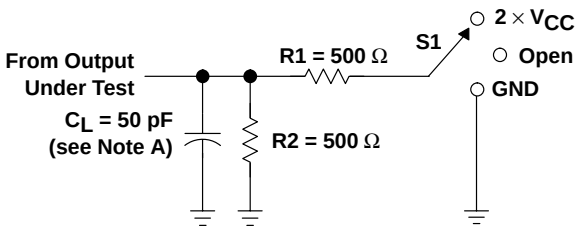
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A, B, C, or D | Y | 3.4 | 13.5 | 3.5 | 12.3 | ns |
| $t_{PHL}$ | | | 3.4 | 13.5 | 3.5 | 12.3 | |

## operating characteristics, $T_A$ = 25°C

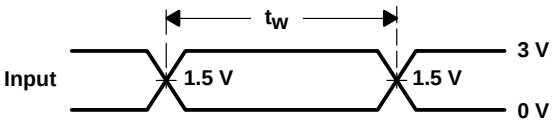
| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 48 | pF |

## PARAMETER MEASUREMENT INFORMATION

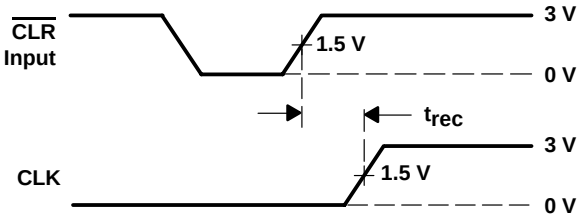



LOAD CIRCUIT

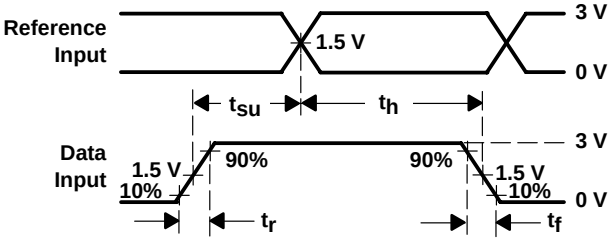
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



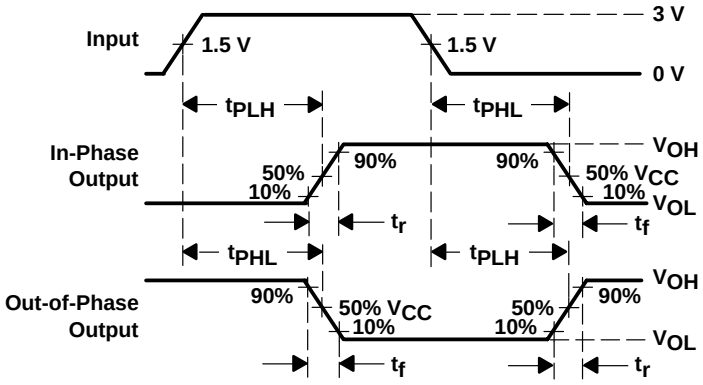

VOLTAGE WAVEFORMS
PULSE DURATION



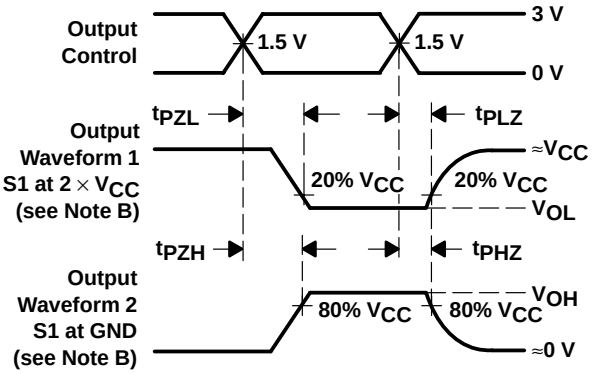

VOLTAGE WAVEFORMS
RECOVERY TIME




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-0051301QCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-0051301QCA CD54ACT20F3A |
| CD54ACT20F3A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-0051301QCA CD54ACT20F3A |
| CD54ACT20F3A.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-0051301QCA CD54ACT20F3A |
| CD74ACT20E | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT20E |
| CD74ACT20E.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74ACT20E |
| CD74ACT20M | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -55 to 125 | ACT20M |
| CD74ACT20M96 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT20M |
| CD74ACT20M96.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT20M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF CD54ACT20, CD74ACT20 :**

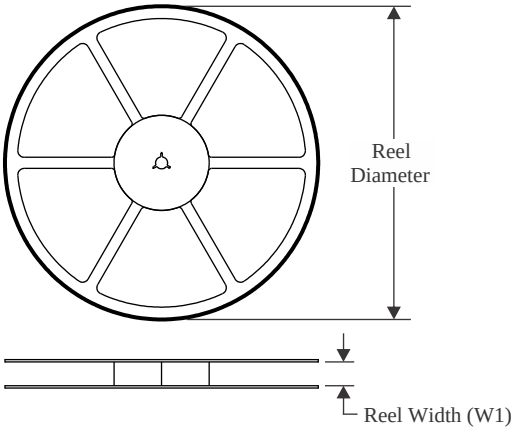
- Catalog : CD74ACT20
- Military : CD54ACT20

NOTE: Qualified Version Definitions:

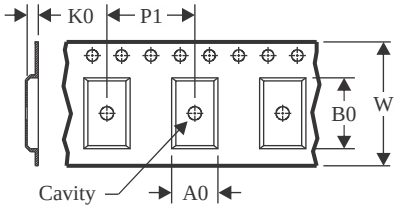
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

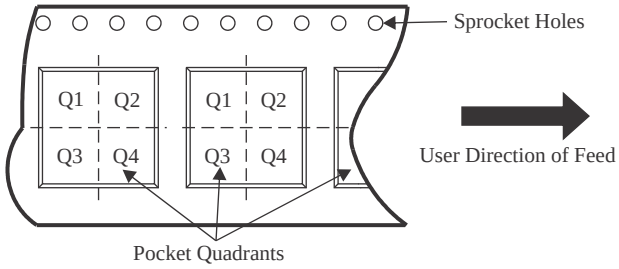



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

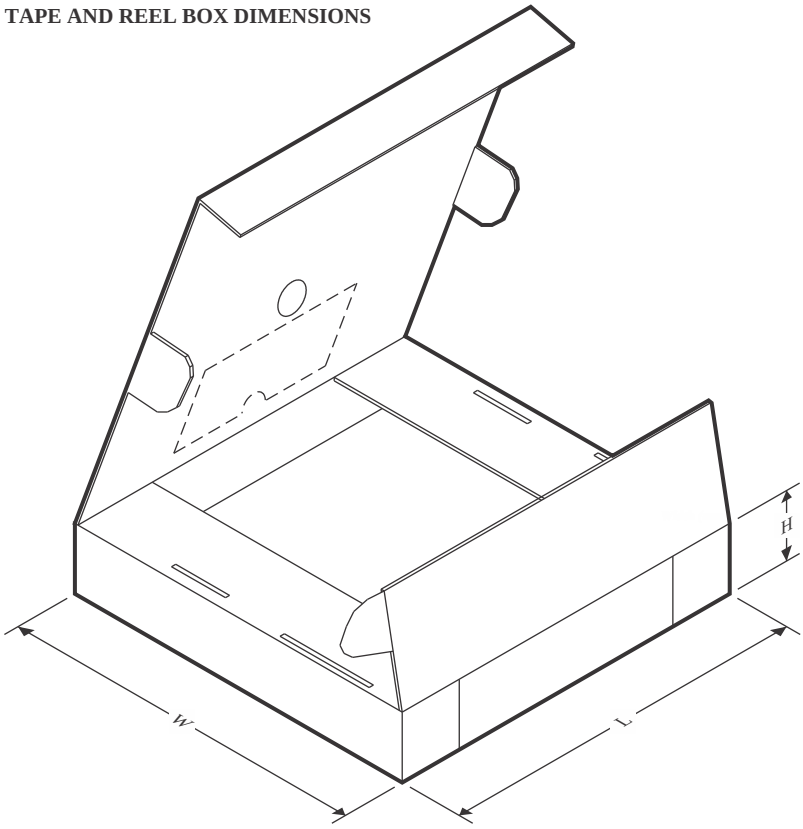
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74ACT20M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

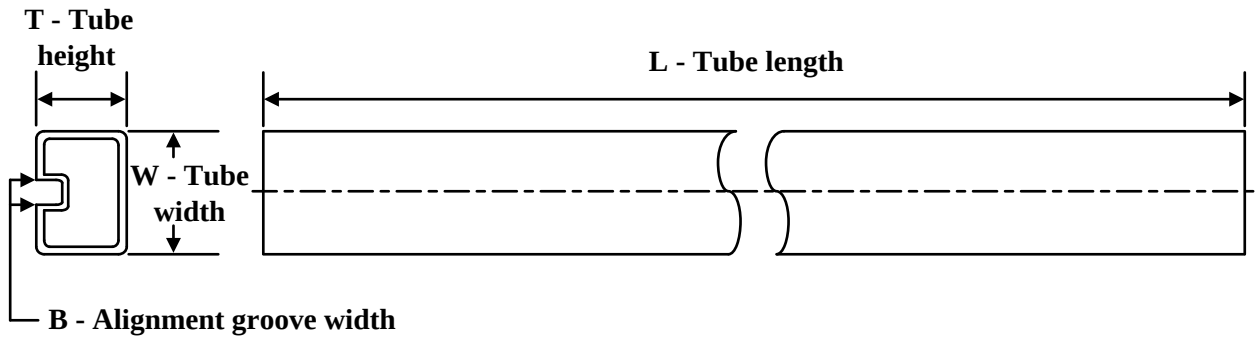
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

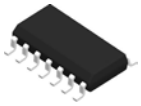
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74ACT20M96 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74ACT20E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT20E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT20E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT20E.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

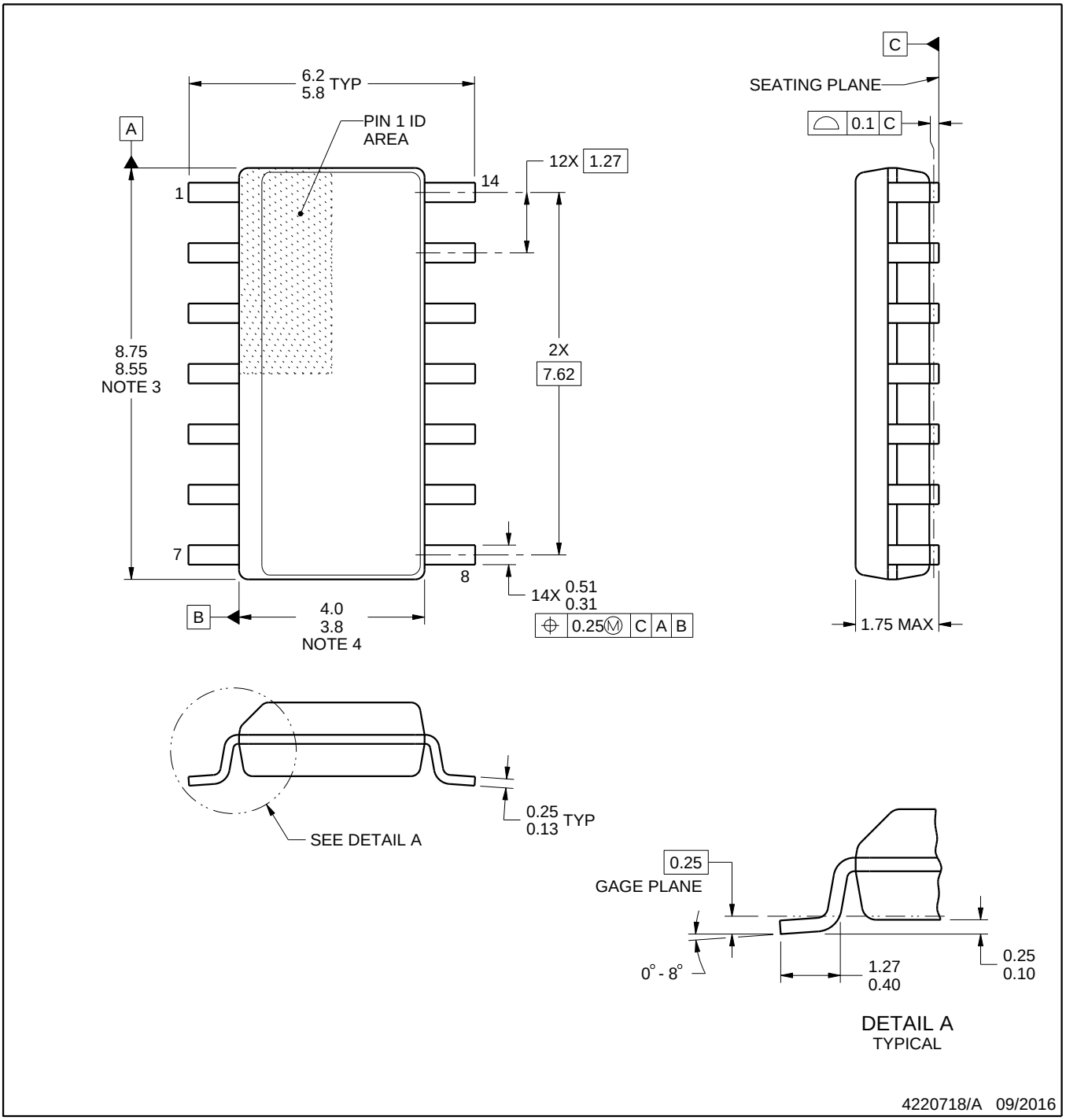


# PACKAGE OUTLINE

## D0014A

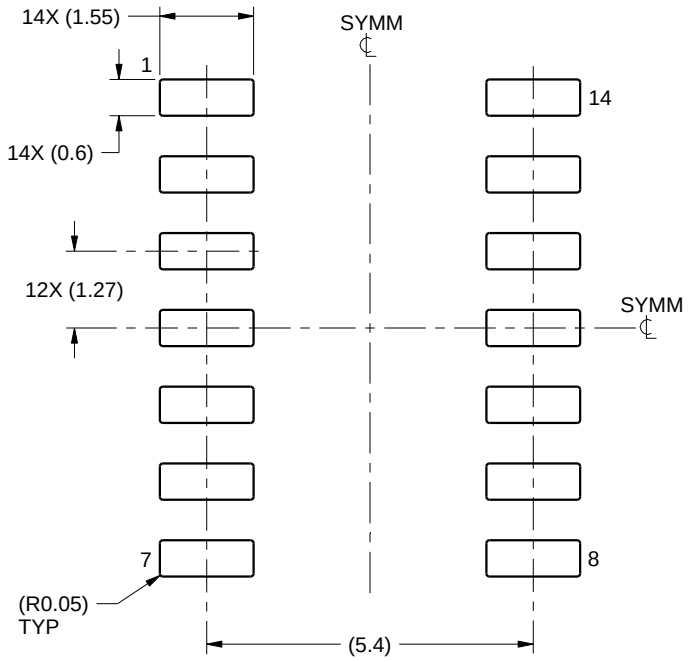
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

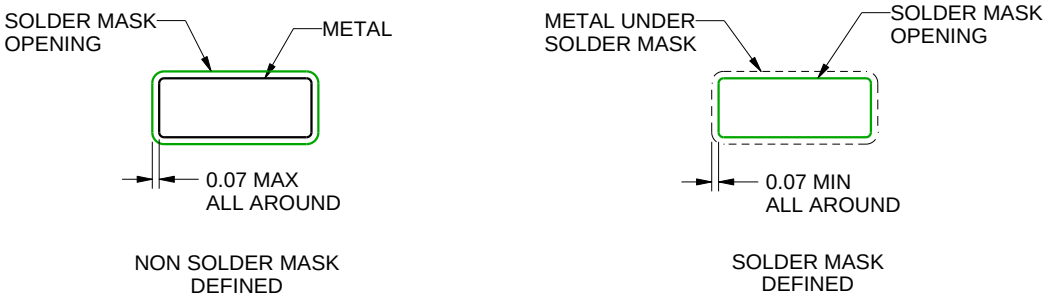



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

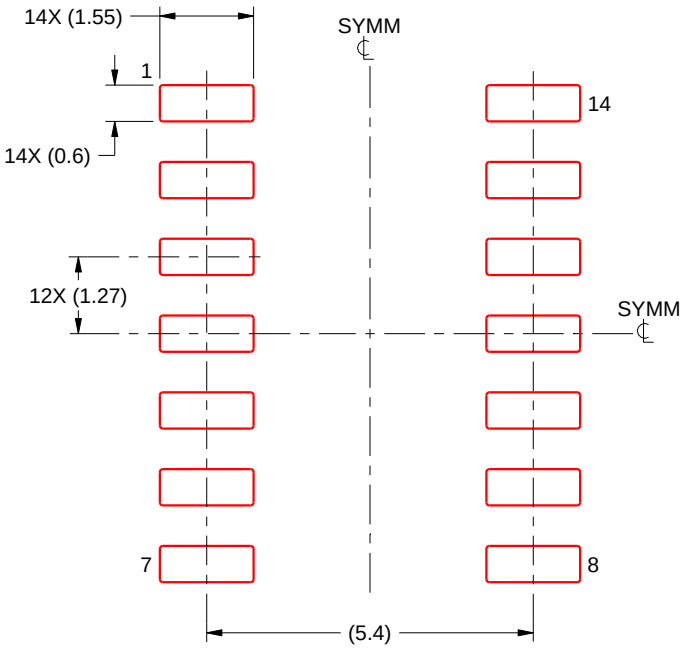
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

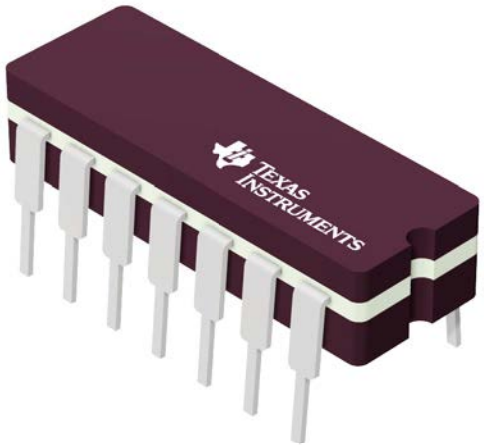
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

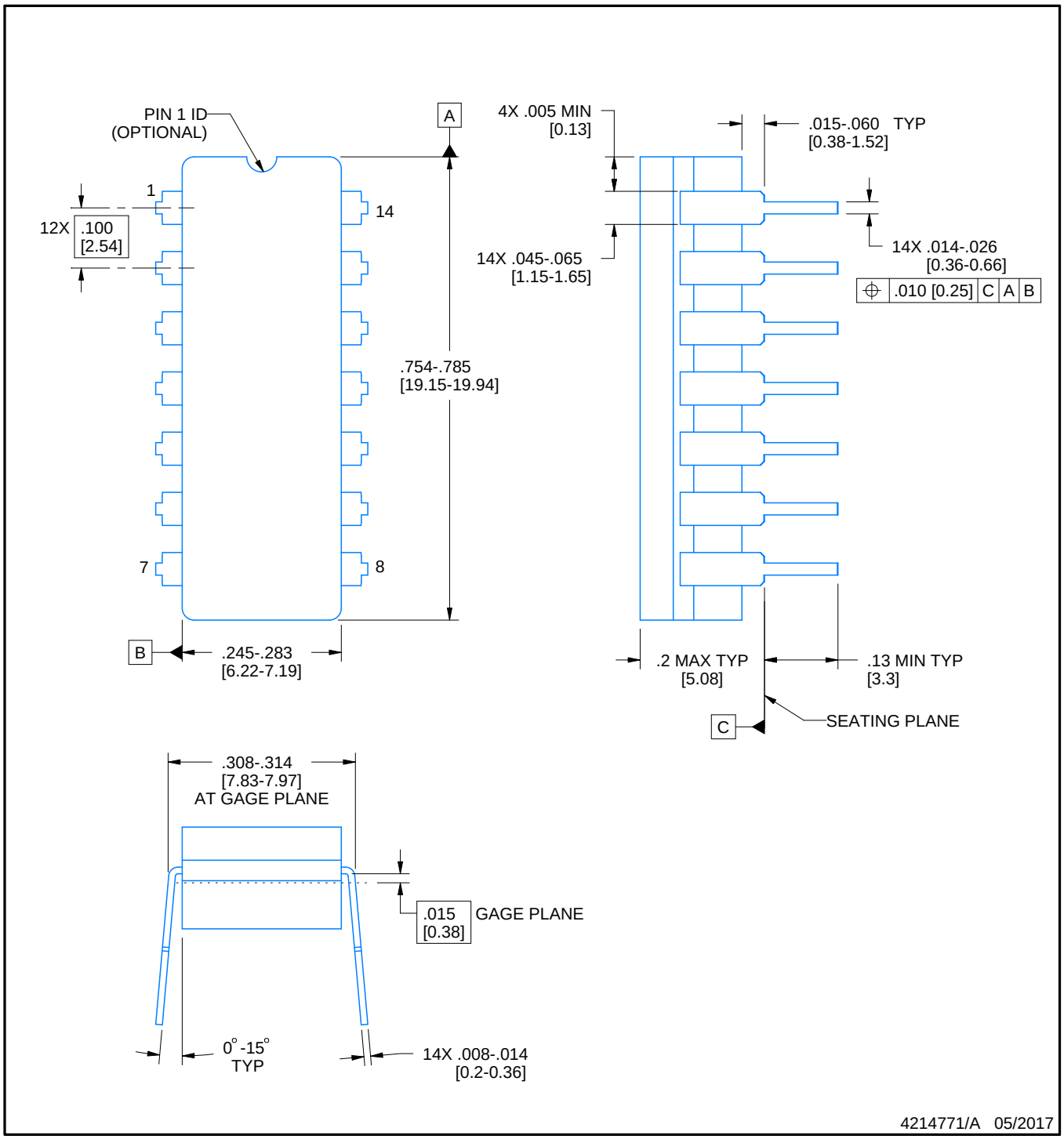
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

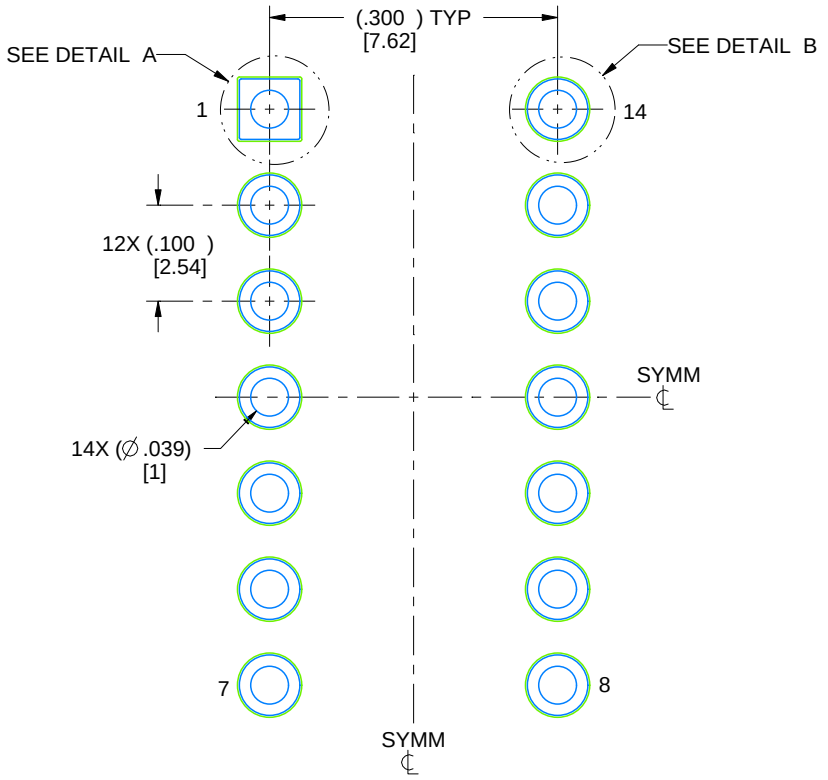
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

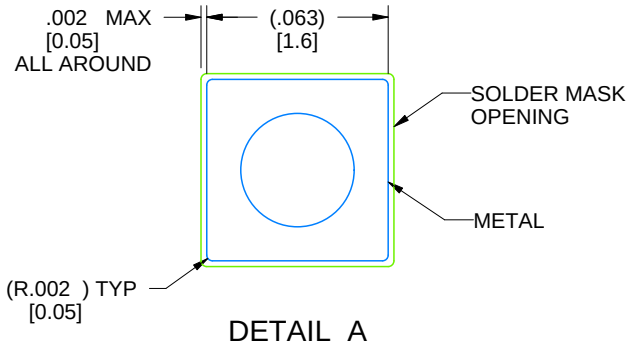
## J0014A

## CDIP - 5.08 mm max height

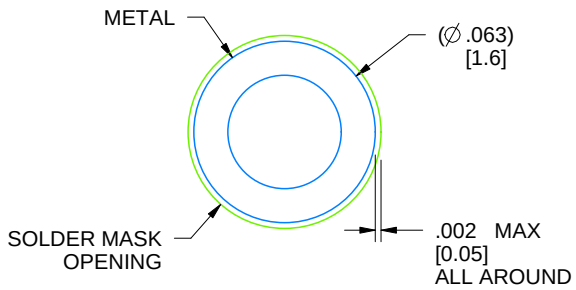
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



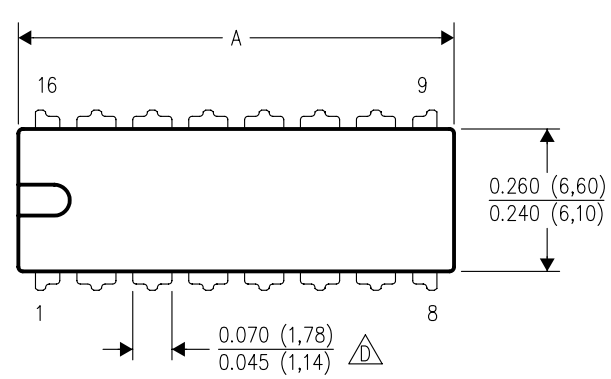

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

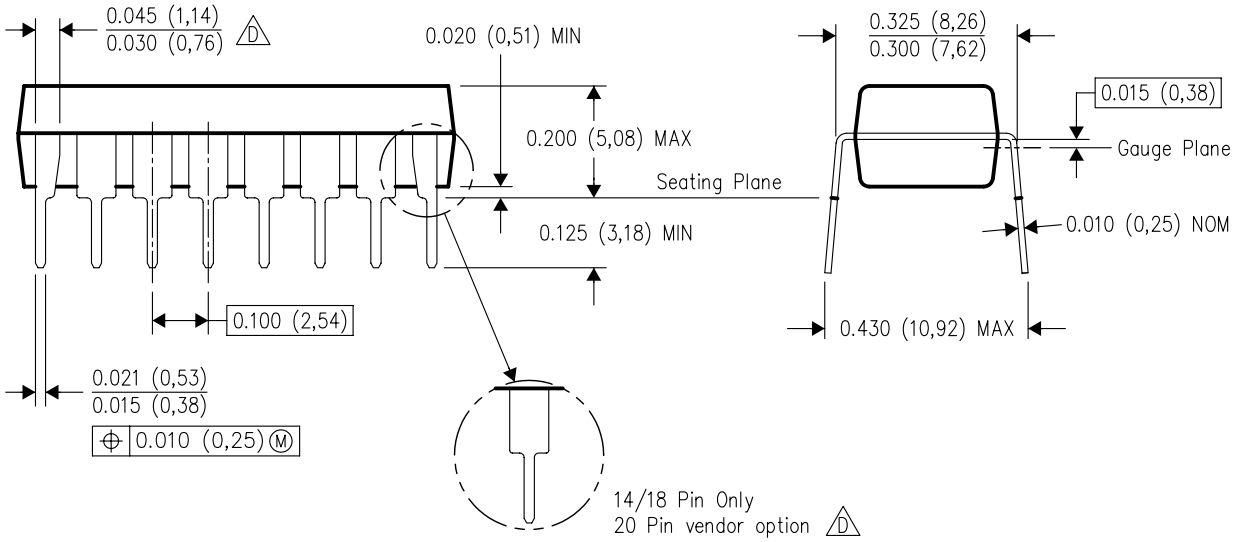
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265