CDCDB2000 PCIe Gen 1～Gen 5 用 DB2000QL 準拠 20 出力クロック バッファ

1 特長

- 85Ω の出力終端を内蔵した 20 の LP-HCSL 出力
- 8 つのハードウェア出力イネーブル (OE#) 制御
- DB2000QL フィルタ後の付加位相ジッタ:
  < 0.08ps rms
- PCIe Gen 4 および Gen 5 Common Clock (CC) および Individual Reference (IR) アーキテクチャをサポート
  – スペクトラム拡散対応
- サイクル間ジッタ:<50ps
- 出力間スキュー:<50ps
- 入出力間遅延:3ns 未満
- コアおよび入出力電源電圧:3.3V
- ハードウェア制御による低消費電力モード (PD#)
- PD# モードでの出力制御のためのサイドバンド インターフェイス (SBI)
- 9 つの選択可能な SMBus アドレス
- 消費電力:600mW 未満
- 6mm × 6mm、80 ピン TLGA/GQFN パッケージ

2 アプリケーション

- マイクロサーバー / タワー サーバー
- ストレージ エリア ネットワーク (SAN) およびホスト バス アダプタ (HBA) カード
- ネットワーク接続ストレージ
- ハードウェア アクセラレータ

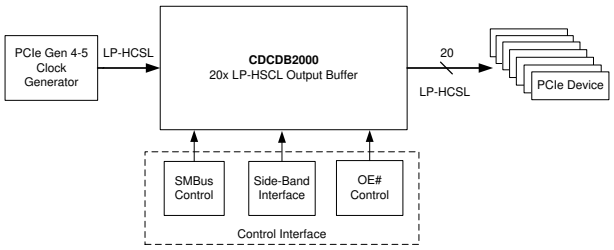
3 概要

CDCDB2000 は、PCIe Gen 1 ～ 5、QuickPath Interconnect (QPI)、UPI、SAS、SATA インターフェイス用のリファレンス クロックを分配できる 20 出力 LP-HCSL、DB2000QL 準拠クロック バッファです。SMBus、SBI、8 つの出力イネーブル ピンにより、20 の出力すべてを個別に設定および制御できます。CDCDB2000 は DB2000QL から派生したバッファであり、DB2000QL 仕様のシステム パラメータを満たし、または上回る性能を備えています。CDCDB2000 は 80 ピンの 6mm × 6mm TLGA/GQFN パッケージに封止されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
CDCDB2000	TLGA (80)	6.00mm × 6.00 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



CDCDB2000 のシステム図

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4 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	
A	CK17_P	CK16_N	CK16_P	CK15_N	CK15_P	CK14_N	CK14_P	CK13_N	CK13_P	CK12_N	CK12_P	CK11_N	A
B	CK17_N	VDD	NC	SADR0	NC	VDD	NC	SADR1	NC	OE12#	VDD	CK11_P	B
C	CK18_P	NC									OE11#	CK10_N	C
D	CK18_N	NC									NC	CK10_P	D
E	CK19_P	SBEN									OE10# SHFT_LD#	OE9#	E
F	CK19_N	NC				DAP = GND					NC	CK9_N	F
G	CLKIN_P	NC									NC	CK9_P	G
H	CLKIN_N	VDD_A									OE8#	CK8_N	H
J	CK0_P	NC									NC	CK8_P	J
K	CK0_N	NC									OE7#	CK7_N	K
L	CK1_P	VDD	NC	SMB DAT	SMB CLK	NC	NC	OE5# DATA	NC	OE6# CLK	VDD	CK7_P	L
M	CK1_N	CK2_P	CK2_N	CK3_P	CK3_N	CKPWRGD_PD#	CK4_P	CK4_N	CK5_P	CK5_N	CK6_P	CK6_N	M
	1	2	3	4	5	6	7	8	9	10	11	12	

図 4-1. CDCDB2000 NPP Package 80-Pin TLGA Top View

表 4-1. Pin Functions

PIN		I/O TYPE[2]	DESCRIPTION
NAME[1]	NO.		
INPUT CLOCK			
CLKIN_P	G1	I	LP-HCSL differential clock input. Typically connected directly to the differential output of clock source.
CLKIN_N	H1	I	
OUTPUT CLOCKS			
CK0_P	J1	O	LP-HCSL differential clock output of channel 0. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK0_N	K1	O	
CK1_P	L1	O	LP-HCSL differential clock output of channel 1. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK1_N	M1	O	
CK2_P	M2	O	LP-HCSL differential clock output of channel 2. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK2_N	M3	O	
CK3_P	M4	O	LP-HCSL differential clock output of channel 3. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK3_N	M5	O	
CK4_P	M7	O	LP-HCSL differential clock output of channel 4. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK4_N	M8	O	
CK5_P	M9	O	LP-HCSL differential clock output of channel 5. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin L8 (OE5# / DATA) is recommended to be either in DATA mode or pulled high.
CK5_N	M10	O	
CK6_P	M11	O	LP-HCSL differential clock output of channel 6. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin L10 (OE6# / CLK) is recommended to be either in CLK mode or pulled high.
CK6_N	M12	O	
CK7_P	L12	O	LP-HCSL differential clock output of channel 7. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin K11 (OE7#) is recommended to be pulled high to disable channel 7 output.
CK7_N	K12	O	
CK8_P	J12	O	LP-HCSL differential clock output of channel 8. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin H11 (OE8#) is recommended to be pulled high to disable channel 8 output.
CK8_N	H12	O	
CK9_P	G12	O	LP-HCSL differential clock output of channel 9. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin E12 (OE9#) is recommended to be pulled high to disable channel 9 output.
CK9_N	F12	O	
CK10_P	D12	O	LP-HCSL differential clock output of channel 10. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin E11 (OE10# / SHFT_LD#) is recommended to be either in SHFT_LD# mode or pulled high.
CK10_N	C12	O	
CK11_P	B12	O	LP-HCSL differential clock output of channel 11. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin C11 (OE11#) is recommended to be pulled high to disable channel 11 output.
CK11_N	A12	O	
CK12_P	A11	O	LP-HCSL differential clock output of channel 12. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect, and pin B10 (OE12#) is recommended to be pulled high to disable channel 12 output.
CK12_N	A10	O	
CK13_P	A9	O	LP-HCSL differential clock output of channel 13. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK13_N	A8	O	
CK14_P	A7	O	LP-HCSL differential clock output of channel 14. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK14_N	A6	O	
CK15_P	A5	O	LP-HCSL differential clock output of channel 15. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK15_N	A4	O	
CK16_P	A3	O	LP-HCSL differential clock output of channel 16. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK16_N	A2	O	
CK17_P	A1	O	LP-HCSL differential clock output of channel 17. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK17_N	B1	O	

表 4-1. Pin Functions (続き)

PIN		I/O TYPE[2]	DESCRIPTION
NAME[1]	NO.		
CK18_P	C1	O	LP-HCSL differential clock output of channel 18. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK18_N	D1	O	
CK19_P	E1	O	LP-HCSL differential clock output of channel 19. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK19_N	F1	O	
MANAGEMENT AND CONTROL			
CKPWRGD_PD#	M6	I, PD	Clock Power Good and Power Down multi-function input pin with internal 120-kΩ pulldown. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. On first high transition, PWRGD samples the latched SADR[1:0] inputs and starts up device. After PWRGD has been asserted high for the first time, the pin becomes a PD# pin and it controls power-down mode: LOW: Power-down mode, all output channels tri-stated. HIGH: Normal operation mode.
OE5# DATA	L8	I, PD	Output enable for channel 5 and Side-Band Interface data multi-function pin with internal 120-kΩ pulldown. Typically connected to GPIO of microcontroller. If both modes are unused, the pin can be left no connect. When pin E2 = LOW, OE5# mode. Output enable for channel 5, active low. LOW: enable output channel 5. HIGH: disable output channel 5. When pin E2 = HIGH, DATA mode. Side-Band Interface data pin.
OE6# CLK	L10	I, PD	Output enable for channel 6 and Side-Band Interface clock multi-function pin with internal 120-kΩ pulldown. Typically connected to GPIO of microcontroller. If both modes are unused, the pin can be left no connect. When pin E2 = LOW, OE6# mode. Output Enable for channel 6, active low. LOW: enable output channel 6. HIGH: disable output channel 6. When pin E2 = HIGH, CLK mode. Side-Band interface clock pin.
OE7#	K11	I, PD	Output Enable for channel 7 with internal 120-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 7. HIGH: disable output channel 7.
OE8#	H11	I, PD	Output Enable for channel 8, with internal 120-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 8. HIGH: disable output channel 8.
OE9#	E12	I, PD	Output Enable for channel 9, with internal 120-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 9. HIGH: disable output channel 9.
OE10# SHFT_LD#	E11	I, PD	Output enable for channel 10 and Side-Band Interface load shift registers multi-function pin with internal 120-kΩ pulldown. Typically connected to GPIO of microcontroller. If both modes are unused, the pin can be left no connect. When pin E2 = LOW, OE10# mode. Output Enable for channel 10, active low. LOW: enable output channel 10. HIGH: disable output channel 10. When pin E2 = HIGH, SHFT_LD# mode. Side-Band Interface load shift registers pin. LOW: disable Side-Band Interface shift register. HIGH: enable Side-Band Interface shift register. A falling edge transfers the Side-Band shift register contents to the output register.
OE11#	C11	I, PD	Output Enable for channel 11 with internal 120-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 11. HIGH: disable output channel 11.
OE12#	B10	I, PD	Output Enable for channel 12 with internal 120-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 12. HIGH: disable output channel 12.

表 4-1. Pin Functions (続き)

PIN		I/O TYPE[2]	DESCRIPTION
NAME[1]	NO.		
SBEN	E2	I, S, PD	Side-Band Interface enable input with internal 120-kΩ pulldown. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. This pin disables the Output Enable (OE#) pins when asserted. LOW: OE# pins and SMBus enable bits control outputs, Side-Band interface disabled. HIGH: Side-Band Interface controls outputs, OE# pins and SMBus enable bits are disabled.
SMBUS AND SMBUS ADDRESS			
SADR0	B4	I, S, PU / PD	SMBus address strap bit[0]. This is a 3-level input that is decoded in conjunction with pin B8 to set SMBus address. It has internal 120-kΩ pullup / pulldown network biasing to VDD/2 when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration input, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground.
SADR1	B8	I, S, PU / PD	SMBus address strap bit[1]. This is a 3-level input that is decoded in conjunction with pin B4 to set SMBus address. It has internal 120-kΩ pullup / pulldown network biasing to VDD/2 when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground.
SMBCLK	L5	I	Clock pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k.
SMBDAT	L4	I / O	Data pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k.
SUPPLY VOLTAGE AND GROUND			
GND	DAP	G	Ground. Connect ground pad to system ground.
VDD	B2, B6, B11, L2, L11	P	Power supply input for LP-HCSL clock output channels. Connect to 3.3-V power supply rail with decoupling capacitor to GND. Place a 0.1-µF capacitor close to each supply pin between power supply and ground.
VDD_A	H2	P	Power supply input for differential input clock. Connect to 3.3-V power supply rail with decoupling capacitor to GND. Place a 0.1-µF capacitor close to pin.
NO CONNECT			
NC	B3, B5, B7, B9, C2, D2, D11, F2, F11, G2, G11, J2, J11, K2, L3, L6, L7, L9,	—	Do not connect to GND or VDD.

(1) The “#” symbol at the end of a pin name indicates that the active state occurs when the signal is at a low voltage level. When “#” is not present, the signal is active high.

(2) The definitions below define the I/O type for each pin.

- I = Input
- O = Output
- I / O = Input / Output
- PU / PD = Internal 120-kΩ Pullup / Pulldown network biasing to VDD/2
- PD = Internal 120-kΩ Pulldown
- S = Hardware Configuration Pin
- P = Power Supply
- G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}, V_{DD_A}	Power supply voltage	–0.3	3.6	V
V_{IN}	IO input voltage	GND	V_{DD} + 0.5	V
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	IO supply voltage	3.135	3.3	3.465	V
V_{DD_A}	Core supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

THERMAL METRIC(1)		CDCDB2000 NPP (GQFN) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

VDD, VDD_A = 3.3 V ± 5 %, -40 °C < TA < 85 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION					

5.5 Electrical Characteristics (続き)

VDD, VDD_A = 3.3 V ± 5 %, -40 °C < TA < 85 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD_A}	Core supply current	Active mode. CKPWRGD_PD# = 1			12		mA
		Power down mode. CKPWRGD_PD# = 0			8		
I_{DD}	IO supply current per output	All-outputs disabled			20		mA
		All-outputs active, 100MHz			200		
		Power down mode. CKPWRGD_PD# = 0			8		
CLOCK INPUT							
f_{IN}	Input frequency			50	100	250	MHz
V_{IN}	Input voltage swing	Differential voltage between CLKIN_P and CLKIN_N(1)		200		2300	$mV_{Diff-peak}$
dV/dt	Input voltage edge rate	20% - 80% of input swing		0.7			V/ns
DV_{CROSS}	Total variation of V_{CROSS}	Total variation across V_{CROSS}			140		mV
DC_{IN}	Input duty cycle			40		60	%
C_{IN}	Input capacitance(2)	Differential capacitance between CLKIN_P and CLKIN_N pins			2.2		pF
CLOCK OUTPUT							
f_{OUT}	Output frequency			50	100	250	MHz
C_{OUT}	Output capacitance(1)	Differential capacitance between CKx_P and CKx_N pins			2.2		pF
V_{OH}	Output high voltage	Single-ended(2) (3)		225		270	mV
V_{OL}	Output low voltage			10		150	
V_{CROSS}	Crossing point voltage	Input V_{CROSS} varied by 140 mV. (3) (4)		130		200	
DV_{CROSS}	Total variation of V_{CROSS}	Input V_{CROSS} varied by 140 mV. Variation of V_{CROSS} (3) (4)				35	
V_{ovs}	Overshoot voltage	(3)				V_{OH}+75	
V_{uds}	Undershoot voltage	(3)				V_{OL}–75	
Z_{DIFF}	Differential impedance	Measured at V_{OL}/V_{OH}		81	85	89	ohm
Z_{DIFF_CROSS}	Differential impedance	Measured at V_{CROSS}		68	85	102	
t_{EDGE}	Edge rate	Measured at V_{CROSS}		2		20	V/ns
Dt_{EDGE}	Edge rate matching	Measured at V_{CROSS}				20	%
t_{STABLE}	Power good assertion to stable clock output	CKPWRGD_PD# pin transistions from 0 to 1, f_{IN} = 100 MHz	Measured when PWRGD reaches 0.2V			1.8	ms
$t_{DRIVE\_PD\#}$	Power good assertion to outputs driven high	CKPWRGD_PD# pin transistions from 0 to 1, f_{IN} = 100 MHz	Measured when PWRGD reaches 0.2V			300	µs
t_{OE}	Output enable assertion to stable clock output	OEx# pin transistions from 1 to 0				10	CLKIN Periods
t_{OD}	Output enable de-assertion to no clock output	OEx# pin transistions from 0 to 1				10	
t_{PD}	Power down assertion to no clock output	CKPWRGD_PD# pin transistions from 1 to 0				3	
t_{DCD}	Duty cycle distortion	Differential; f_{IN} = 100MHz, f_{in_DC} = 50%		–1.0		1.0	%
t_{DLY}	Propagation delay	(5)		0.5		3	ns

5.5 Electrical Characteristics (続き)

VDD, VDD_A = 3.3 V ± 5 %, -40 °C < TA < 85 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{SKEW}	Skew between outputs	(6)				50	ps
J_{CKx_PCIE}	Additive jitter	DB2000QL filter				0.08	ps, rms
	Additive jitter for PCIe5	PCIe5.0 filter				0.03	ps, rms
	Additive jitter for PCIe4	PLL BW = 2 - 5 MHz; CDR = 10 MHz	Input clock slew rate ≥ 1.8 V/ns			0.08	ps, rms
	Additive jitter for PCIe3		Input clock slew rate ≥ 0.6 V/ns			0.15	ps, rms
J_{CKx_PCIE}	Additive jitter for PCIe2	PCIe2 filter				0.2	ps, rms
J_{CKx_PCIE}	Additive jitter for PCIe1	PCIe1 filter				5	ps, rms
J_{CKx}	Additive jitter	f_{IN} = 100 MHz; slew rate ≥ 3 V/ns; 12 kHz to 20 MHz integration bandwidth.			155		fs, rms
SMBUS INTERFACE, SIDE-BAND INTERFACE, OEx#, CKPWRGD_PD#, SBEN							
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
I_{IL}	Input leakage current	With internal pull up/pull-down	GND < V_{IN} < V_{DD}	–30		30	uA
		Without internal pull up/pull-down		–5		5	uA
C_{IN}	Input capacitance				4.5		pF
C_{OUT}	Output capacitance				4.5		pF
3-LEVEL DIGITAL INTERFACE (SA_0, SA_1)							
V_{IHT}	High-level input voltage			2.4			V
V_{IMT}	Mid level input voltage			1.3	V_{DD}/2	1.8	V
V_{ILT}	Low-level input voltage					0.9	V
I_{INT}	Input high current	VIN = V_{DD}, VIN = GND		-10		10	uA
I_{Leak}	Input leakage current	With internal pull up/pull-down	GND < V_{IN} < V_{DD}	–30		30	uA

(1) Voltage swing includes overshoot.
(2) Not tested in production. Ensured by design and characterization.
(3) Measured into DC test load.
(4) V_{CROSS} is single-ended voltage when CKx_P = CKx_N with respect to system ground. Only valid on rising edge of CKx, when CKx_P is rising.
(5) Measured from rising edge of CLK_IN to any CKx output.
(6) Measured from rising edge of any CKx output to any other CKx output.

5.6 Timing Requirements

VDD, VDD_A = 3.3 V ± 5 %, -40 °C < TA < 85 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SMBUS-COMPATIBLE INTERFACE TIMING						
f_{SMB}	SMBus operating frequency		10		100	kHz
t_{BUF}	Bus free time between STOP and START		4.7			µs
t_{HD_STA}	START condition hold time		4			µs
t_{SU_STA}	START condition setup time		4.7			µs
t_{SU_STO}	STOP condition setup time		4			µs

VDD, VDD_A = 3.3 V ± 5 %, -40 °C < TA < 85 °C. Typical values are at VDD = VDD_A = 3.3 V, 25 °C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{HD_DAT}	SMBDAT hold time		300			ns
t_{SU_DAT}	SMBDAT setup time		250			
$t_{TIMEOUT}$	Detect SMBCLK low timeout		25		35	ms
t_{LOW}	SMBCLK low period		4.7			µs
t_{HIGH}	SMBCLK high period		4		50	
t_{LOW_SL}	Cumulative clock low extend time				25	ms
t_F	SMBCLK/SMBDAT fall time(1)				300	ns
t_R	SMBCLK/SMBDAT rise time(2)				1000	
SIDE-BAND INTERFACE TIMING						
t_{PERIOD}	Clock period		40			ns
t_{SETUP}	Setup time to clock		25			
t_{DSU}	Data set up time		10			
t_{DHOLD}	Data hold time		5			
t_{DELAY}	Delay time		25			
t_{PDLY}	Propagation delay		4		10	CLK periods
t_{SLEW}	Clock slew rate	20% - 80%	0.2		3	V/ns

(1) TF = (VIHMIN + 0.15) to (VILMAX - 0.15)
(2) TR = (VILMAX - 0.15) to (VIHMIN + 0.15)

5.7 Typical Characteristics

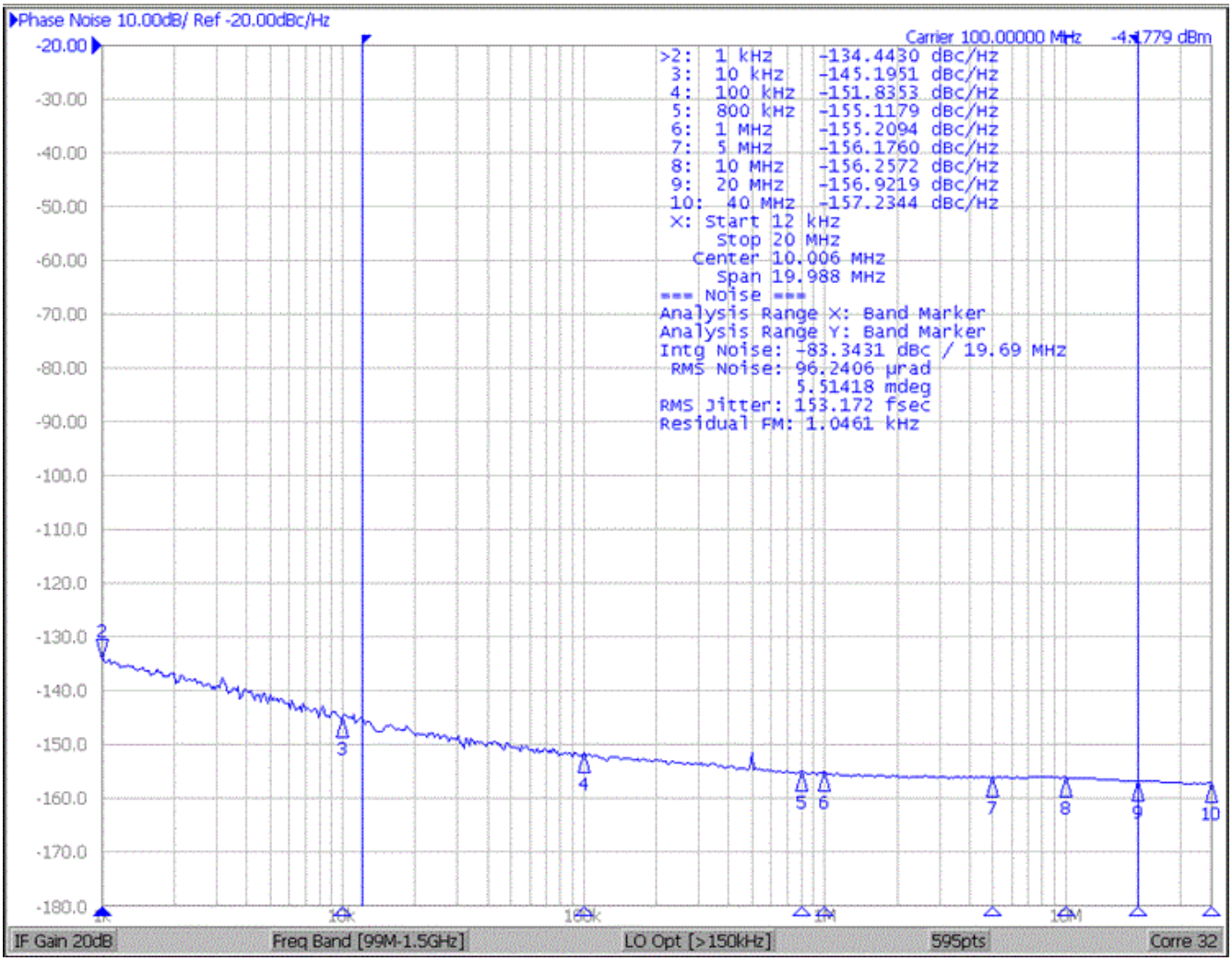


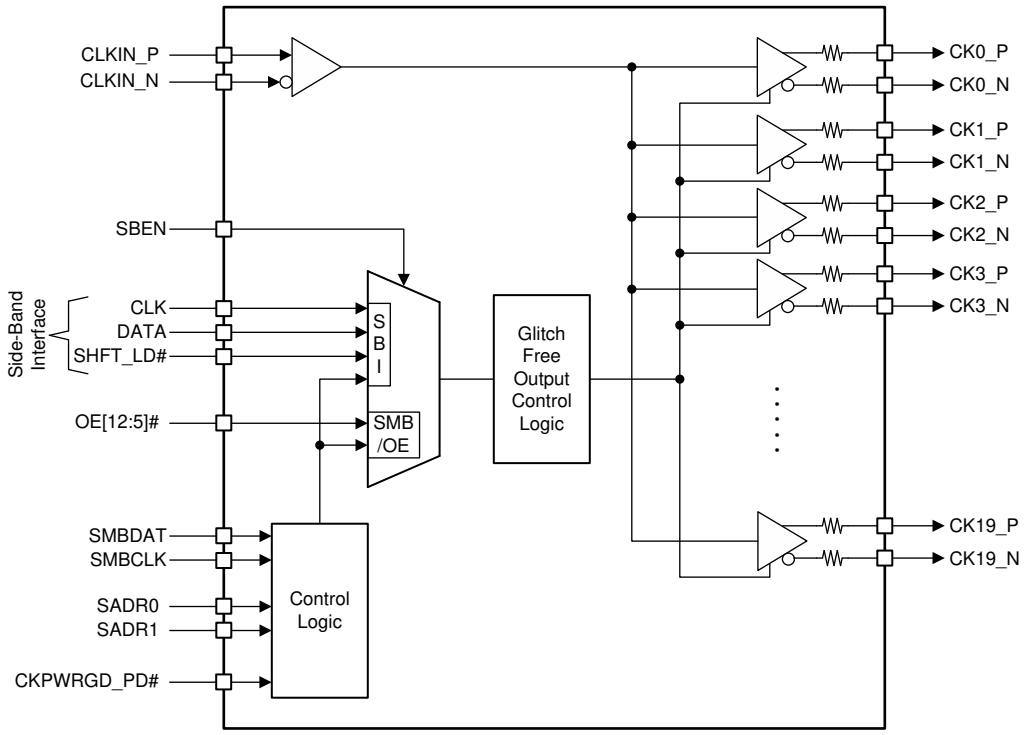
図 5-1. CDCDB2000 Clock Out (CK0:19) Phase Noise

6 Detailed Description

6.1 Overview

The CDCDB2000 is a low additive-jitter, low propagation delay clock buffer designed to meet the strict performance requirements for PCIe Gen 1-5, QPI and UPI reference clocks. The CDCDB2000 allows buffering and replication of a single clock source to up to 20 individual outputs in the LP-HCSL format. The outputs of the CDCDB2000 can be configured before they are enabled using the Side-Band control interface. The CDCDB2000 also includes status and control registers accessible by an SMBus version 2.0 compliant interface. The device integrates a large amount of external passive components to reduce overall system cost.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable Control

The CDCDB2000 allows two methods to control the state of the output channels: SMBus/OE#, and Side-Band Interface. Only one of the two methods can be active at any time, and the active interface is selected by the state of the SBEN pin. Both methods of output control can assign the state of each output individually.

When in SMBus/OE# control is selected, the OE# pins become active. The OE# pins control the state of the output with the same number. For example, the OE5# pin controls the state of the CK5 output driver. The SMBus registers may enable/disable the output regardless of the OE# pin state if desired.

6.3.2 SMBus

The CDCDB2000 has an SMBus interface that is active only when CKPWRGD_PD# = 1.The SMBus allows individual enable/disable of each output when the SMBus mode is selected using the SBEN pin.

When CKPWRGD_PD# = 0, the SMBus pins are placed in a Hi-Z state, but all register settings are retained. The SMBus register values are only retained while VDD_A remains inside of the recommended operating voltage.

6.3.2.1 SMBus Address Assignment

The SMBus address is assigned by configuration of two pins (SADR1 and SADR0) that each support three levels. This configuration allows the CDCDB2000 to assume 9 different SMBus addresses.

The SMBus address pins are sampled PWRGD is set to 1. See 表 6-1 for address pin configuration. The address cannot be changed until the PWRGD state is cleared by powering down the device.

表 6-1. SMBus Address Assignment

SADR1	SADR0	SMBUS ADDRESS
L	L	0xD8
L	M	0xDA
L	H	0xDE
M	L	0xC2
M	M	0xC4
M	H	0xC6
H	L	0xCA
H	M	0xCC
H	H	0xCE

6.3.3 Side-Band Interface

The Side-Band Interface(SBI) is a basic 3-wire interface that consists of the DATA, CLK and SHFT_LD# pins. The SBI is used to shift data into a 20-bit long shift register. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the SBI output register.

While SBI is enabled by the SBEN pin, OE[7:9, 11, 12]# pins are disabled and DATA, CLK and SHFT_LD# are enabled on the OE5#, OE6# and OE10# pins, respectively.

When power has been applied, and SBEN = 1, the SBI is active regardless of the CKPWRGD_PD# pin state. This characteristic allows loading the shift register and transferring the contents to the SBI output register before the first assertion of the CKPWRGD_PD# pin.

6.4 Device Functional Modes

6.4.1 CKPWRGD_PD# Function

The CKPWRGD_PD# pin is used to set 2 state variables inside of the device: PWRGD, and PD#. The PWRGD and PD# variables control which functions of the device are active at any time, as well as the state of the input and output pins.

The PWRGD and PD# states are multiplexed on the CKPWRGD_PD# pin. CKPWRGD_PD# must remain below VOL and not exceed VDD_A + 0.3 V until VDD, VDD_A, and CLKIN are present and within the recommended operating conditions.

The first rising edge of the CKPWRGD_PD# pin sets PWRGD = 1. After PWRGD is set to 1, the CKPWRGD_PD# pin is used to assert PD# mode only. PWRGD variable will only be cleared to 0 with the removal of VDD and VDD_A.

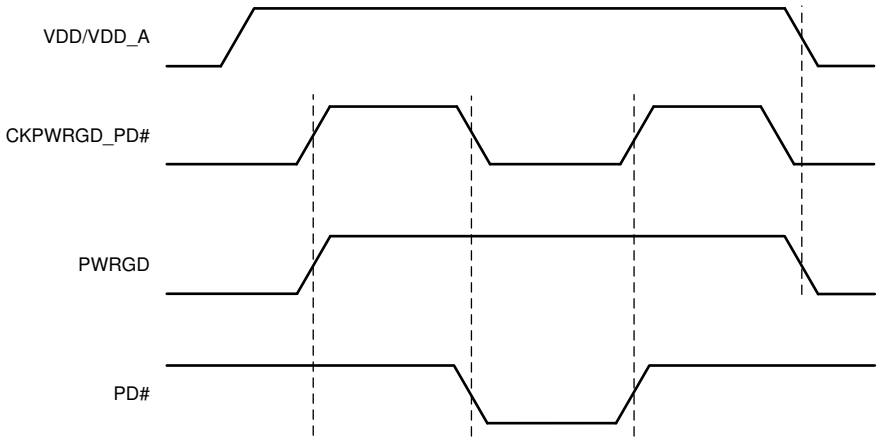


図 6-1. PWRGD and PD# State Changes

6.4.2 OE[12:5]# and SMBus Output Enables

Each output channel, 0 to 19, can be individually enabled or disabled by SMBus control register bits, called SMB enable bits. Additionally, each output channel from 12 to 5 has a dedicated, corresponding, OE[12:5]# hardware pin. The OE[12:5]# pins are asynchronously asserted-low signals that may enable or disable the output.

Refer to 表 6-2 for enabling and disabling outputs through the hardware and software. Note that both the SMB enable bit must be a '1' and the OEx# pin must be an input low voltage '0' for the output channel to be active.

表 6-2 is only valid when the SBEN signal is low (SBEN = 0).

表 6-2. OE[12:5]# Functionality When SBEN = 0

INPUTS			OE[12:5]# HARDWARE PINS AND SMBus CONTROL REGISTER BITS			
PWRGD	**PD#**	**CLKIN**	**SMBus ENABLE BIT (byte[2:0])**	**OE[12:5]#**	**CK[12:5]**	**CK[19:13, 4:0]**
0	X	X	X	X	LOW	LOW
1	0	X	X	X	Tristate	Tristate
1	1	Running	0	X	0	0
1	1	Running	1	0	Running	Running
1	1	Running	1	1	0	Running

6.5 Programming

The CDCDB2000 has two methods to program the states of its 20 output drivers: SMBus and SBI.

To select between SMBus and SBI interfaces, the SBEN pin is used. Pulling the SBEN to a high level enables the SBI. Pulling the SBEN pin to ground enables the SMBus interface. When SBI is enabled, the SMBus Mask registers are active. The SMBus Mask registers allow the function of the SBI shift registers to be disabled and set the each individual channel as enabled. See 図 6-2 for a diagram of how the SMBus Mask registers and SBI shift register interact to enable or disable each output.

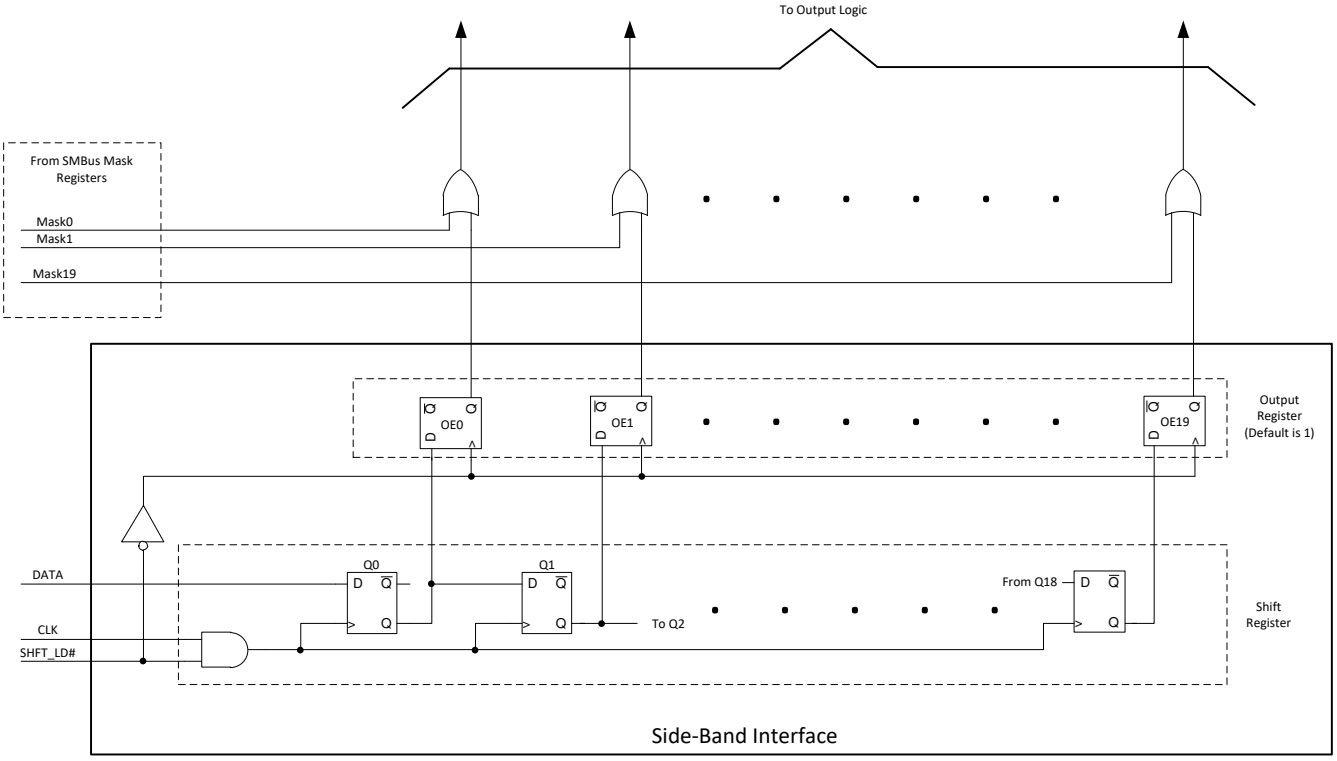


図 6-2. SMBus Mask Register and SBI Shift Register Logic

6.5.1 SMBus

SMBus programming is described in セクション 6.3.2, and the registers are described in セクション 7.

6.5.2 SBI

Side-Band Interface (SBI) is a simple 3-wire serial interface. This interface consists of DATA, CLK and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK clocks DATA into a shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents into the Output Register. Both the SBI and the traditional SMBus interface feed common output enable/disable synchronization logic, which ensures glitch-free enable and disable outputs regardless of the method used.

SBI can be configured at a system level in three ways: star topology, daisy chain topology, and directly. The star topology is shown in 図 6-3. The daisy chain topology is shown in 図 6-4.

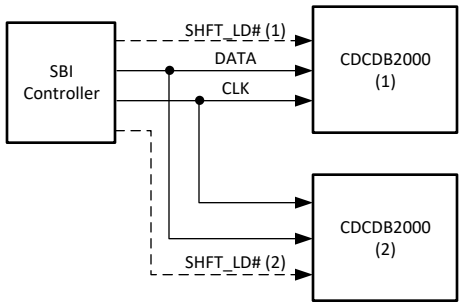


図 6-3. SBI Star Topology

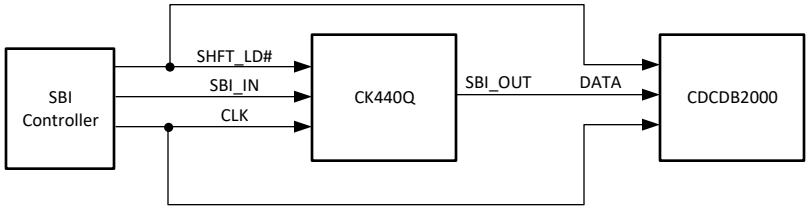


図 6-4. SBI Daisy Chain Topology

7 Register Maps

7.1 CDCDB2000 Registers

表 7-1 lists the CDCDB2000 registers. All register locations not listed in 表 7-1 should be considered as reserved locations and the register contents should not be modified.

表 7-1. CDCDB2000 Registers

Address	Acronym	Register Name	Section
0h	OECR1	Output Enable Control 1	Go
1h	OECR2	Output Enable Control 2	Go
2h	OECR3	Output Enable Control 3	Go
3h	OERDBK	Output Enable Read Back	Go
4h	SBRDBK	SBEN Read Back	Go
5h	VDRREVID	Vendor/Revision Identification	Go
6h	DEVID	Device Identification	Go
7h	BTRDCNT	Byte Read Count Control	Go
8h	SBIMSK1	Side-Band Interface Override Control 1	Go
9h	SBIMSK2	Side-Band Interface Override Control 2	Go
Ah	SBIMSK3	Side-Band Interface Override Control 3	Go

Complex bit access types are encoded to fit into small table cells. 表 7-2 shows the codes that are used for access types in this section.

表 7-2. CDCDB2000 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 OECR1 Register (Address = 0h) [reset = 78h]

OECR1 is shown in 表 7-3.

Return to the Summary Table.

The OECR1 register contains bits that enable or disable individual output clock channels [19:16]

表 7-3. OECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	Output Enable, CK19	R/W	1h	This bit controls the output enable signal for output channel CK19_P/CK19_N. 0h = Output Disabled 1h = Output Enabled
5	Output Enable, CK18	R/W	1h	This bit controls the output enable signal for output channel CK18_P/CK18_N. 0h = Output Disabled 1h = Output Enabled

表 7-3. OECR1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	Output Enable, CK17	R/W	1h	This bit controls the output enable signal for output channel CK17_P/CK17_N. 0h = Output Disabled 1h = Output Enabled
3	Output Enable, CK16	R/W	1h	This bit controls the output enable signal for output channel CK16_P/CK16_N. 0h = Output Disabled 1h = Output Enabled
2-0	RESERVED	R	0h	Reserved

7.1.2 OECR2 Register (Address = 1h) [reset = FFh]

OECR2 is shown in 表 7-4.

Return to the Summary Table.

The OECR2 register contains bits that enable or disable individual output clock channels [7:0]

表 7-4. OECR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Output Enable, CK7	R/W	1h	This bit controls the output enable signal for output channel CK7_P/CK7_N. 0h = Output Disabled 1h = Output Enabled
6	Output Enable, CK6	R/W	1h	This bit controls the output enable signal for output channel CK6_P/CK6_N. 0h = Output Disabled 1h = Output Enabled
5	Output Enable, CK5	R/W	1h	This bit controls the output enable signal for output channel CK5_P/CK5_N. 0h = Output Disabled 1h = Output Enabled
4	Output Enable, CK4	R/W	1h	This bit controls the output enable signal for output channel CK4_P/CK4_N. 0h = Output Disabled 1h = Output Enabled
3	Output Enable, CK3	R/W	1h	This bit controls the output enable signal for output channel CK3_P/CK3_N. 0h = Output Disabled 1h = Output Enabled
2	Output Enable, CK2	R/W	1h	This bit controls the output enable signal for output channel CK2_P/CK2_N. 0h = Output Disabled 1h = Output Enabled
1	Output Enable, CK1	R/W	1h	This bit controls the output enable signal for output channel CK1_P/CK1_N. 0h = Output Disabled 1h = Output Enabled
0	Output Enable, CK0	R/W	1h	This bit controls the output enable signal for output channel CK0_P/CK0_N. 0h = Output Disabled 1h = Output Enabled

7.1.3 OECR3 Register (Address = 2h) [reset = FFh]

OECR3 is shown in 表 7-5.

Return to the Summary Table.

The OECR3 register contains bits that enable or disable individual output clock channels [15:8]

表 7-5. OECR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Output Enable, CK15	R/W	1h	This bit controls the output enable signal for output channel CK15_P/CK15_N. 0h = Output Disabled 1h = Output Enabled
6	Output Enable, CK14	R/W	1h	This bit controls the output enable signal for output channel CK14_P/CK14_N. 0h = Output Disabled 1h = Output Enabled
5	Output Enable, CK13	R/W	1h	This bit controls the output enable signal for output channel CK13_P/CK13_N. 0h = Output Disabled 1h = Output Enabled
4	Output Enable, CK12	R/W	1h	This bit controls the output enable signal for output channel CK12_P/CK12_N. 0h = Output Disabled 1h = Output Enabled
3	Output Enable, CK11	R/W	1h	This bit controls the output enable signal for output channel CK11_P/CK11_N. 0h = Output Disabled 1h = Output Enabled
2	Output Enable, CK10	R/W	1h	This bit controls the output enable signal for output channel CK10_P/CK10_N. 0h = Output Disabled 1h = Output Enabled
1	Output Enable, CK9	R/W	1h	This bit controls the output enable signal for output channel CK9_P/CK9_N. 0h = Output Disabled 1h = Output Enabled
0	Output Enable, CK8	R/W	1h	This bit controls the output enable signal for output channel CK8_P/CK8_N. 0h = Output Disabled 1h = Output Enabled

7.1.4 OERDBK Register (Address = 3h) [reset = 0h]

OERDBK is shown in 表 7-6.

Return to the Summary Table.

The OERDBK register contains bits that report the current state of the OE[12:5]# input pins.

表 7-6. OERDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE12# State	R	0h	This bit reports the logic level present on the OE12# pin.
6	OE11# State	R	0h	This bit reports the logic level present on the OE11# pin.
5	OE10# State	R	0h	This bit reports the logic level present on the OE10# pin.

表 7-6. OERDBK Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	OE9# State	R	0h	This bit reports the logic level present on the OE9# pin.
3	OE8# State	R	0h	This bit reports the logic level present on the OE8# pin.
2	OE7# State	R	0h	This bit reports the logic level present on the OE7# pin.
1	OE6# State	R	0h	This bit reports the logic level present on the OE6# pin.
0	OE5# State	R	0h	This bit reports the logic level present on the OE5# pin.

7.1.5 SBRDBK Register (Address = 4h) [reset = 1h]

SBRDBK is shown in 表 7-7.

Return to the Summary Table.

The SBRDBK register contains a bit that report the current state of the SBEN input pin.

表 7-7. SBRDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	SBEN State	R/W	1h	This bit reports the logic level present on the SBEN pin.

7.1.6 VDRREVID Register (Address = 5h) [reset = X]

VDRREVID is shown in 表 7-8.

Return to the Summary Table.

The VDRREVID register contains a vendor identification code and silicon revision code.

表 7-8. VDRREVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Revision Code[3:0]	R	X	Silicon revision code. Silicon revision code bits [3:0] map to register bits [7:4] directly.
3-0	Vendor ID[3:0]	R	X	Vendor identification code. Vendor ID bits [3:0] map to register bits [3:0] directly.

7.1.7 DEVID Register (Address = 6h) [reset = X]

DEVID is shown in 表 7-9.

Return to the Summary Table.

The DEVID register contains a device identification code.

表 7-9. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Device ID[7:0]	R	X	Device ID code. Device ID bits[7:0] map to register bits[7:0] directly.

7.1.8 BTRDCNT Register (Address = 7h) [reset = 8h]

BTRDCNT is shown in 表 7-10.

Return to the Summary Table.

The BTRDCNT register allows configuration of the number of bytes that will be read back from the SMBus interface on an issued read command.

表 7-10. BTRDCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	Read Byte Count[5:0]	R/W	8h	Writing to this register configures how many bytes will be read back.

7.1.9 SBIMSK1 Register (Address = 8h) [reset = 0h]

SBIMSK1 is shown in 表 7-11.

Return to the Summary Table.

The SBIMSK1 register allows the SMBus to force enable each output channel individually when the CDCDB2000 is in Side-Band interface mode.

表 7-11. SBIMSK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI Output Mask, CK7	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK7 Enabled
6	SBI Output Mask, CK6	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK6 Enabled
5	SBI Output Mask, CK5	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK5 Enabled
4	SBI Output Mask, CK4	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK4 Enabled
3	SBI Output Mask, CK3	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK3 Enabled
2	SBI Output Mask, CK2	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK2 Enabled
1	SBI Output Mask, CK1	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK1 Enabled
0	SBI Output Mask, CK0	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK0 Enabled

7.1.10 SBIMSK2 Register (Address = 9h) [reset = 0h]

SBIMSK2 is shown in 表 7-12.

Return to the Summary Table.

The SBIMSK2 register allows the SMBus to force enable each output channel individually when the CDCDB2000 is in Side-Band interface mode.

表 7-12. SBIMSK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI Output Mask, CK15	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK15 Enabled
6	SBI Output Mask, CK14	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK14 Enabled
5	SBI Output Mask, CK13	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK13 Enabled
4	SBI Output Mask, CK12	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK12 Enabled
3	SBI Output Mask, CK11	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK11 Enabled
2	SBI Output Mask, CK10	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK10 Enabled
1	SBI Output Mask, CK9	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK9 Enabled
0	SBI Output Mask, CK8	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK8 Enabled

7.1.11 SBIMSK3 Register (Address = Ah) [reset = 0h]

SBIMSK3 is shown in 表 7-13.

Return to the Summary Table.

The SBIMSK3 register allows the SMBus to force enable each output channel individually when the CDCDB2000 is in Side-Band interface mode.

表 7-13. SBIMSK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	SBI Output Mask, CK19	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK19 Enabled
2	SBI Output Mask, CK18	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK18 Enabled
1	SBI Output Mask, CK17	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK17 Enabled

表 7-13. SBIMSK3 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	SBI Output Mask, CK16	R/W	0h	This bit overrides the the SBI output disable when set. 0h = SBI Controls Output 1h = Output CK16 Enabled

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The CDCDB2000 is a fanout buffer that supports PCIe generation 4 and PCIe generation 5 REFCLK distribution. It is used to create, and distribute, up to 20 copies of a typically 100-MHz clock.

8.2 Typical Application

図 8-1 shows a CDCDB2000 typical application. In this application, a clock generator provides a 100-MHz reference to the CDCDB2000 which then distributes that clock to PCIe endpoints. The clock generator may be a discrete clock generator like the LMK03328 or it may be integrated in a larger component such as a PCH or application processor.

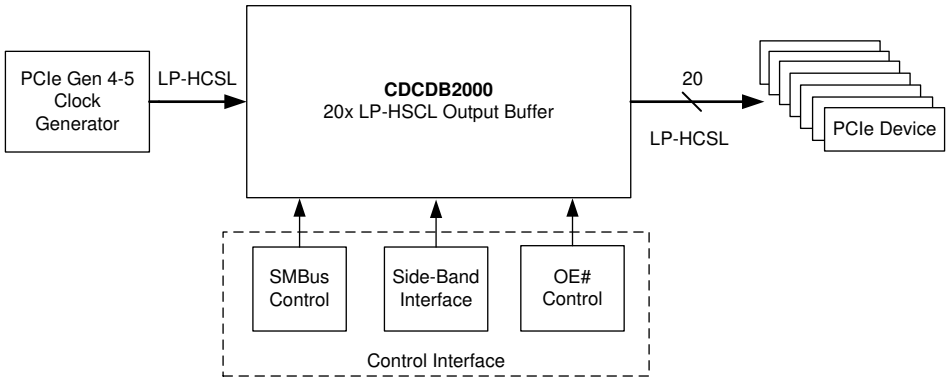


図 8-1. Typical Application

8.2.1 Design Requirements

Consider a typical server motherboard application which needs to distribute a 100-MHz PCIe reference clock from the PCH of a processor chipset to multiple endpoints. An example of clock input and output requirements is:

- Clock Input:
  - 100-MHz LP-HCSL
- Clock Output:
  - 2x 100-MHz to processors, LP-HCSL
  - 2x 100-MHz to riser/retimer, LP-HCSL
  - 2x 100-MHz to DDR memory controller, LP-HCSL

The section below describes the design procedure to configure the CDCDB2000 to output the frequencies for the above scenario.

8.2.2 Detailed Design Procedure

The following items must be determined before starting design of a CDCDB2000 socket:

- Output Enable Control Method

8.2.2.1 Output Enable Control Method

The device provides an option to either use SMBus programmed registers (software) to control the outputs or by using the hardware OE# pins. In case of using software to control the outputs, the hardware OE# pins can be left floating as each of these pins have a pulldown to ground. Refer to the *セクション 7* section for more information on programming the register.

When the user wants to control the outputs with the hardware OE# pins, they can do so for example by connecting these pins to a GPIO controller and follow the *セクション 4* section to set the outputs to HIGH/LOW. The bits OUT_EN_CLK7 to OUT_EN_CLK0 used to control the outputs are shown in registers OECR1 field descriptions. These register bits are set to 1 by default to ensure that the outputs are "software enabled" and their state is therefore set by hardware OE# pins.

8.2.2.2 SMBus Address

An SMBus address should be selected from the listed potential addresses in 表 8-1. The appropriate pullup or pulldown resistor should be placed on the SADRx pins as indicated in the table. Ensure the SMBus address is not already in use to avoid conflict.

表 8-1. SMBus Address Assignment

SADR1	SADR0	SMBus ADDRESS
L	L	0xD8
L	M	0xDA
L	H	0xDE
M	L	0xC2
M	M	0xC4
M	H	0xC6
H	L	0xCA
H	M	0xCC
H	H	0xCE

8.2.3 Application Curve

The graph listed in 表 8-2 is used as both an application curve and a typical characteristics plot (see the セクション 5.7 section).

表 8-2. Table of Graphs

TITLE	FIGURE
CDCDB2000 Clock Out (CK0:19) Phase Noise	図 5-1

8.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI

recommends to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer. These beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

図 8-2 shows the recommended power supply filtering and decoupling method.

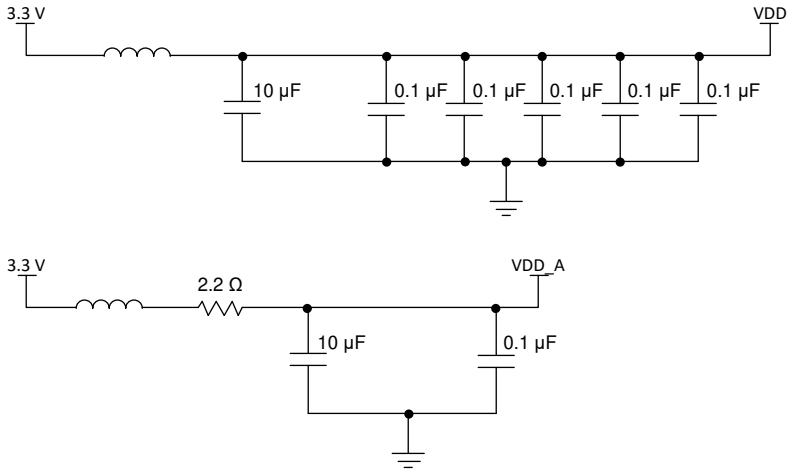


図 8-2. Power Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

The following section provides the layout guidelines to ensure good thermal performance and power supply connections for the CDCDB2000.

8.4.2 Layout Examples

図 8-3 and 図 8-4 are PCB layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

The CDCDB2000 has 85-Ω differential output impedance LP-HCSL format drivers. All transmission lines connected to CKx pins should be 85-Ω differential impedance, 42.5-Ω single-ended impedance to avoid reflections and increased radiated emissions. Take care to eliminate or reduce stubs on the transmission lines.

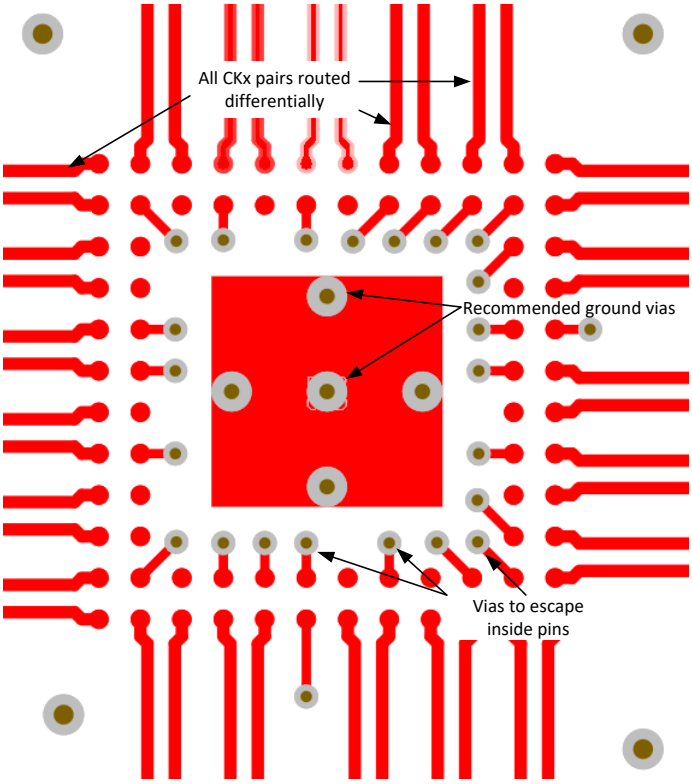


図 8-3. PCB Layout Example for CDCDB2000, Top Layer

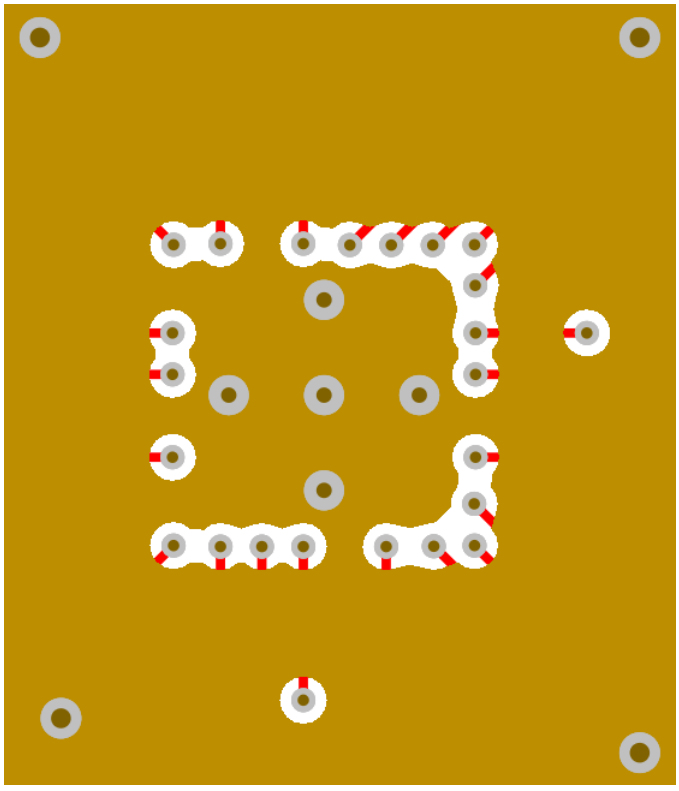


図 8-4. PCB Layout Example for CDCDB2000, GND Layer

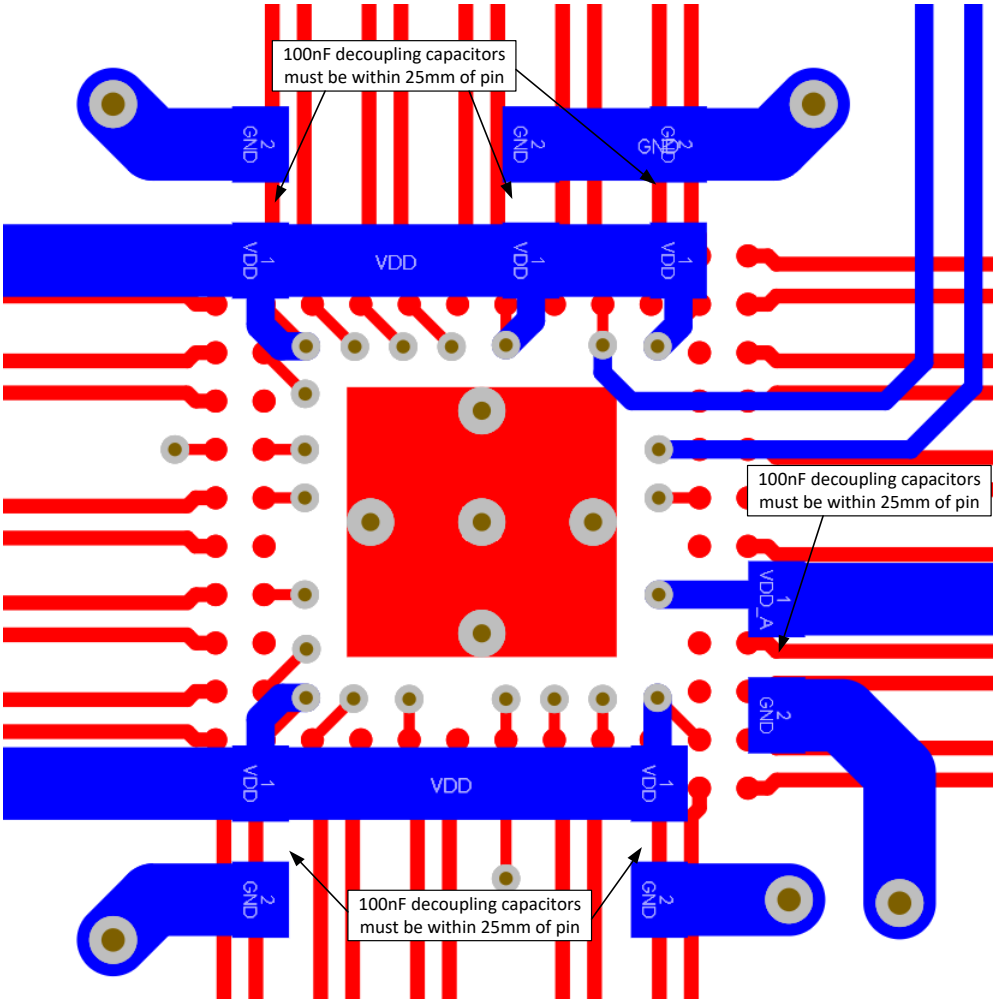


図 8-5. PCB Layout Example for CDCDB2000, Bottom Layer

9 Device and Documentation Support

9.1 Device Support

9.1.1 TICS Pro

TICS Pro is an offline software tool for EVM programming and also for register map generation to program a device configuration for a specific application. For TICS Pro, go to http://www.ti.com/tool/TICSPRO-SW.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (February 2020) to Revision B (October 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1

Changes from Revision * (November 2019) to Revision A (February 2020)	Page
• Changed maximum input voltage from:VDD+ 0.3 V to: VDD+ 0.5 V	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCDB2000ENPPR	ACTIVE	TLGA	NPP	80	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCDB 2000	Samples
CDCDB2000ENPPT	ACTIVE	TLGA	NPP	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCDB 2000	Samples
CDCDB2000NPPR	ACTIVE	TLGA	NPP	80	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCDB 2000	Samples
CDCDB2000NPPT	ACTIVE	TLGA	NPP	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCDB 2000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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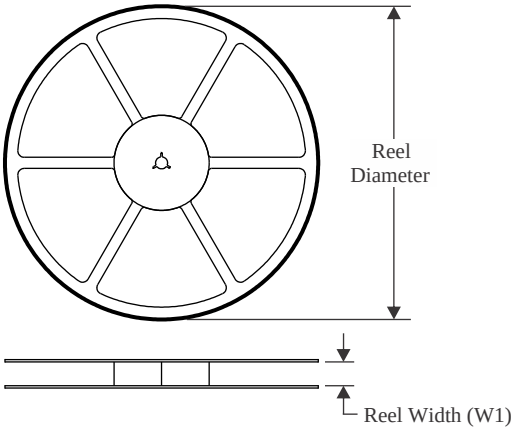
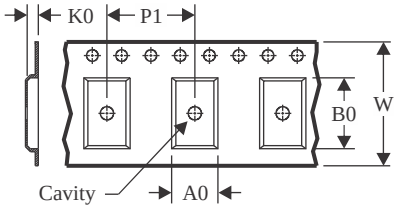
TAPE AND REEL INFORMATION

REEL DIMENSIONS

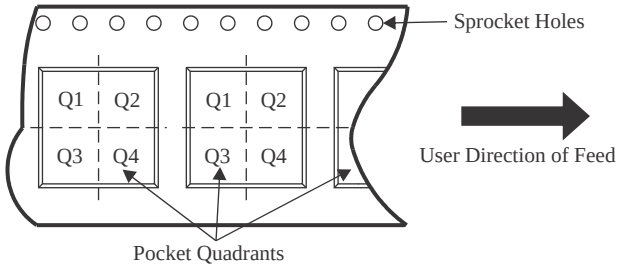


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

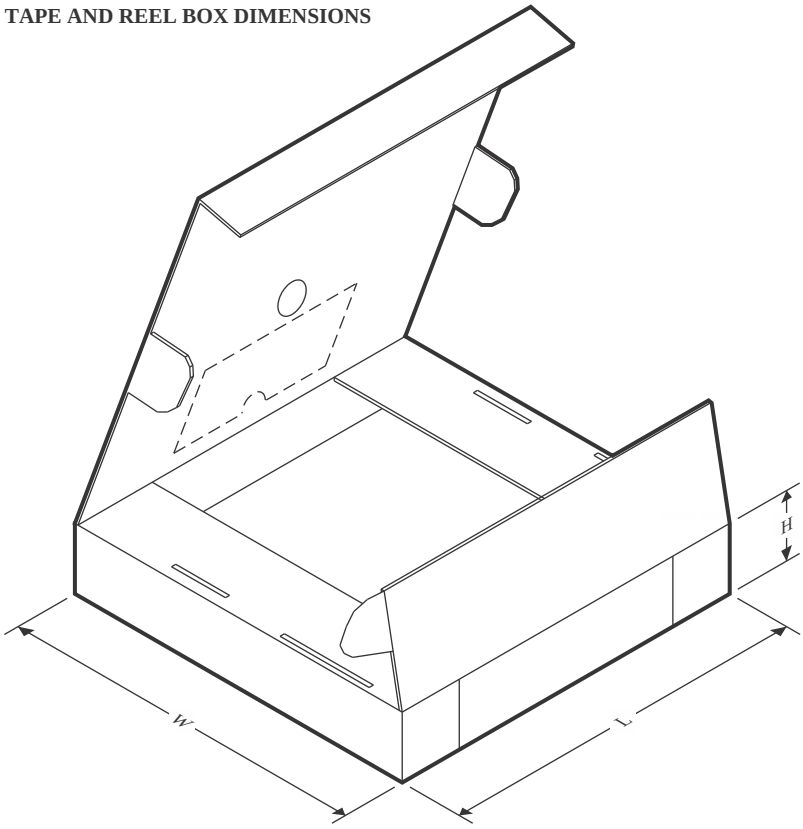
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCDB2000ENPPR	TLGA	NPP	80	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
CDCDB2000ENPPT	TLGA	NPP	80	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
CDCDB2000NPPR	TLGA	NPP	80	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCDB2000NPPT	TLGA	NPP	80	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

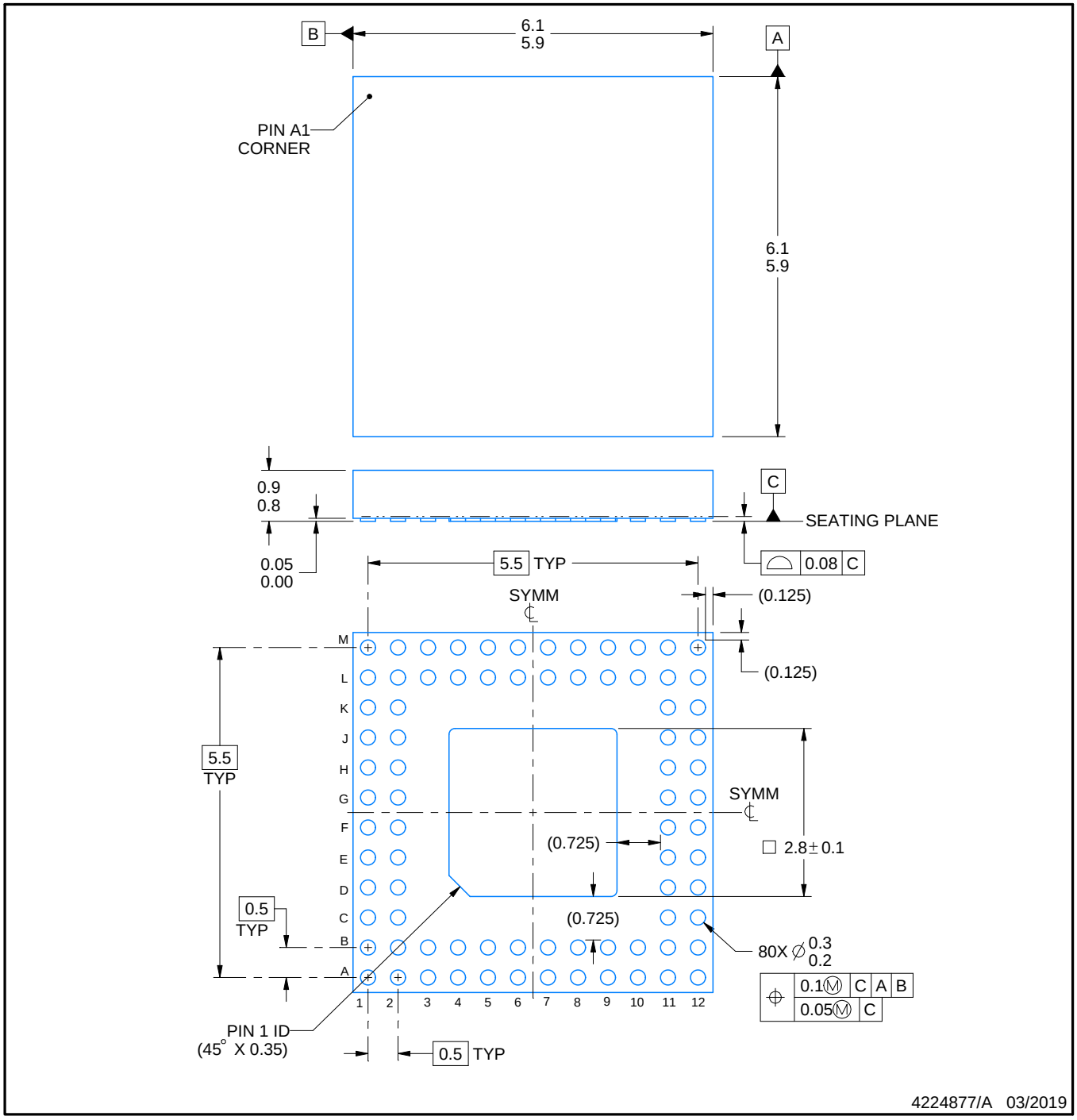
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCDB2000ENPPR	TLGA	NPP	80	4000	367.0	367.0	38.0
CDCDB2000ENPPT	TLGA	NPP	80	250	210.0	185.0	35.0
CDCDB2000NPPR	TLGA	NPP	80	3000	367.0	367.0	38.0
CDCDB2000NPPT	TLGA	NPP	80	250	210.0	185.0	35.0

PACKAGE OUTLINE

NPP0080A

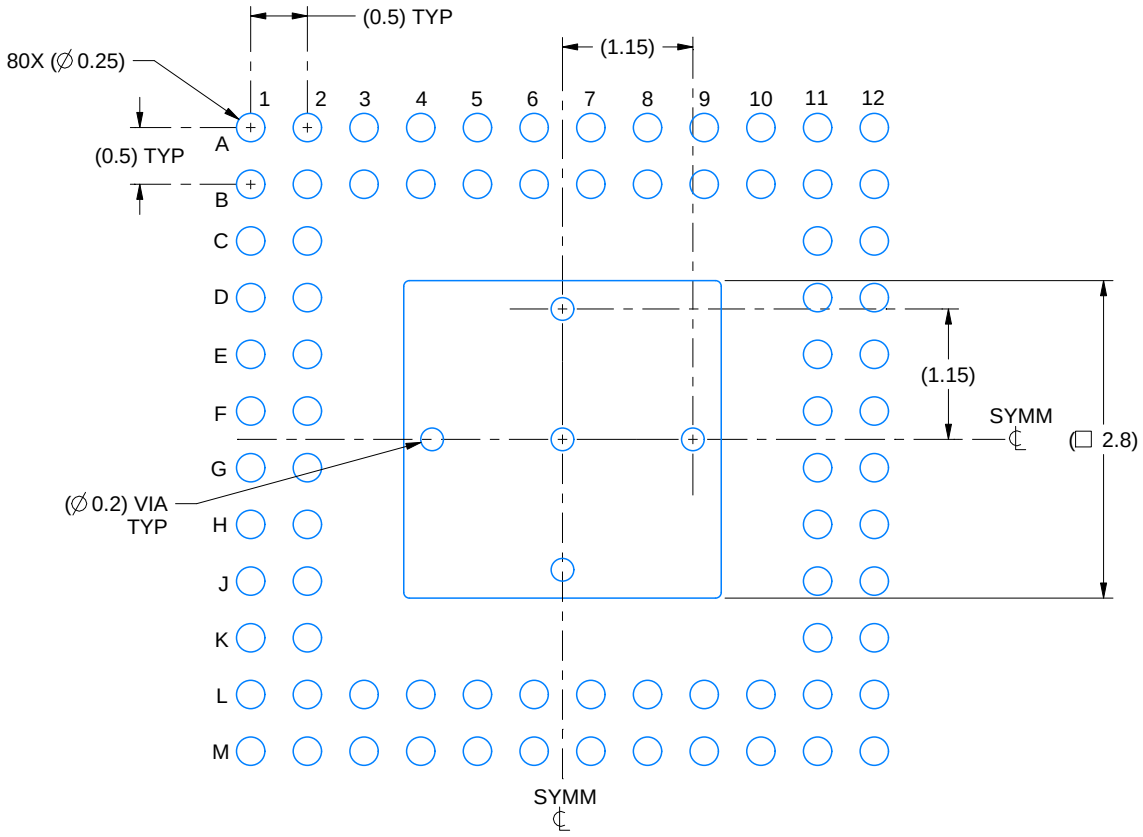
TLGA - 0.9 mm max height

THIN LAND GRID ARRAY

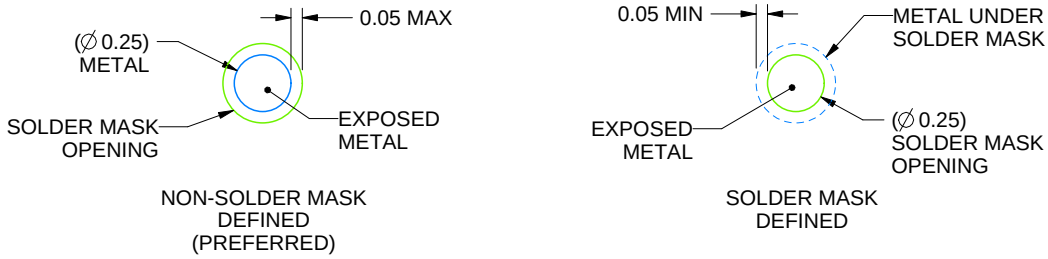


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

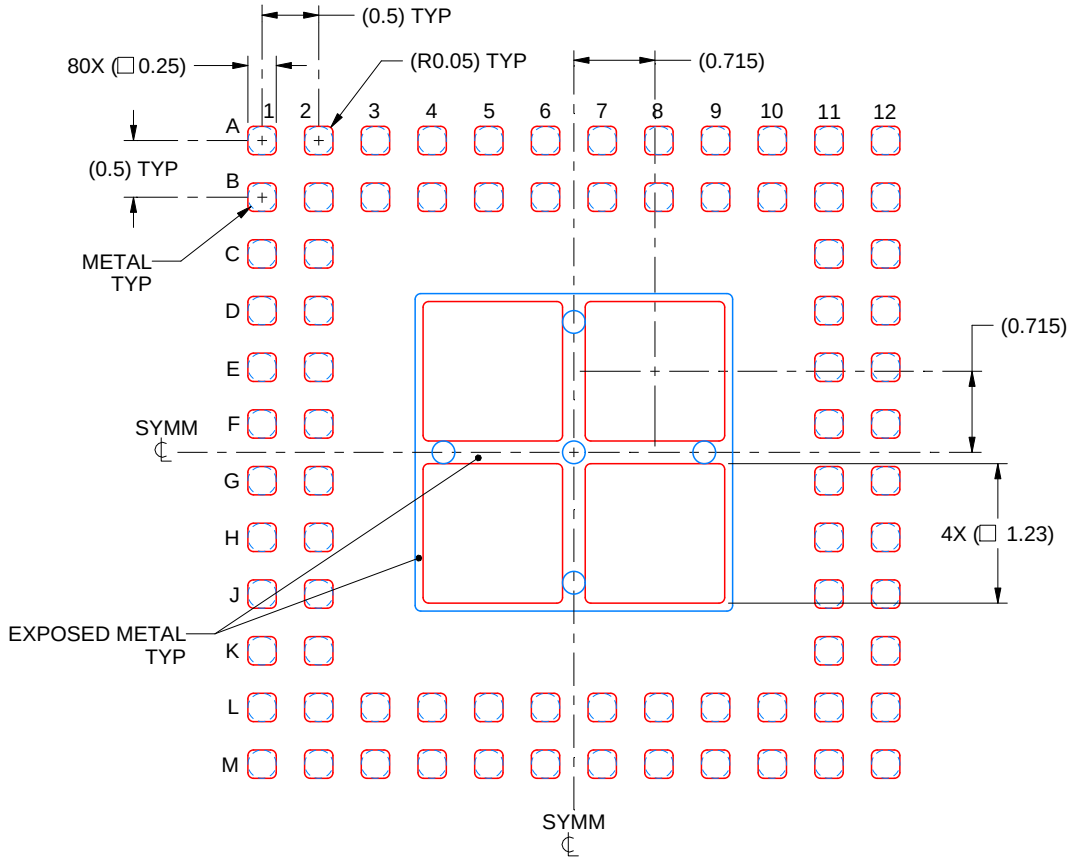


SOLDER MASK DETAILS
NOT TO SCALE

4224877/A 03/2019

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 15X

4224877/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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