CSD13201W10 N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Small Footprint (1 mm × 1 mm)
- Low Profile 0.62-mm Height
- Pb-Free
- RoHS Compliant
- Halogen-Free
- Gate-Source Voltage Clamp

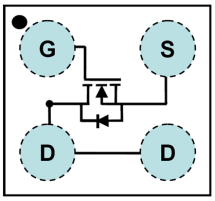
2 Applications

- Battery Management
- Load Switch
- Battery Protection

3 Description

This 12-V, 26-mΩ, N-Channel device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	2.3		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.3		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 1.8 V	38	mΩ
		V_{GS} = 2.5 V	29	
		V_{GS} = 4.5 V	26	mΩ
$V_{GS(th)}$	Threshold Voltage	0.8		V

Device Information(1)

PART NUMBER	PACKAGE	MEDIA	QTY	SHIP
CSD13201W10	1 mm × 1 mm Wafer Level Package	7-inch reel	3000	Tape and Reel

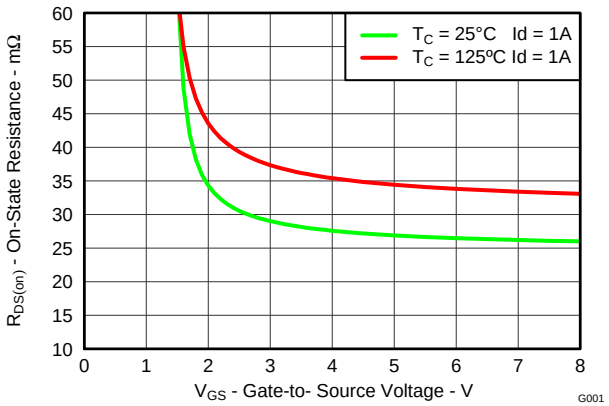
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±8	V
I_D	Continuous Drain Current, T_A = 25°C(1)	1.6	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	20.2	A
P_D	Power Dissipation(1)	1.2	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) $R_{\theta JA}$ = 105°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤ 300 µs, duty cycle ≤ 2%



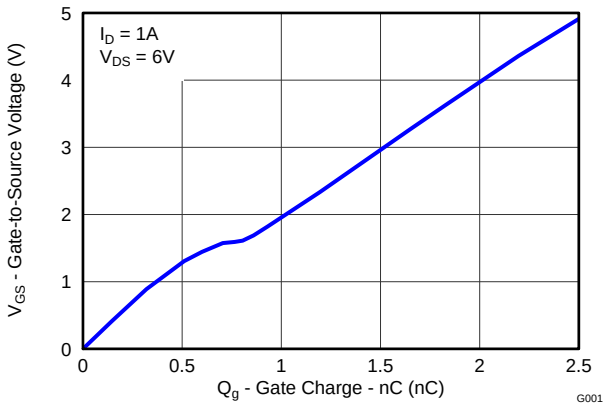


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2012) to Revision A	Page
• Added part number to title	1
• Enhanced *Description*	1
• Added *Device and Documentation Support* section.	7

5 Specifications

5.1 Electrical Characteristics

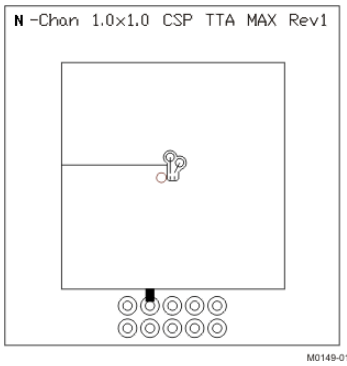
T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.65	0.8	1.1	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 1.8 V, I_D = 1 A		38	53	mΩ
		V_{GS} = 2.5 V, I_D = 1 A		29	39	
		V_{GS} = 4.5 V, I_D = 1 A		26	34	
g_{fs}	Transconductance	V_{DS} = 6 V, I_D = 1 A		23		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		385	462	pF
C_{OSS}	Output capacitance			245	294	pF
C_{RSS}	Reverse transfer capacitance			18.1	22.6	pF
R_g	Series gate resistance			3		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_D = 1 A		2.3	2.9	nC
Q_{gd}	Gate charge gate-to-drain			0.3		nC
Q_{gs}	Gate charge gate-to-source			0.5		nC
$Q_{g(th)}$	Gate charge at Vth			0.3		nC
Q_{OSS}	Output charge	V_{DS} = 6.0 V, V_{GS} = 0 V		1.8		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 1 A, R_G = 20 Ω		3.9		ns
t_r	Rise time			5.9		ns
$t_{d(off)}$	Turn off delay time			14.4		ns
t_f	Fall time			9.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = 1 A, V_{GS} = 0 V		0.7	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 6 V, I_S = 1 A, di/dt = 100 A/µs		2.4		nC
t_{rr}	Reverse recovery time			11.5		ns

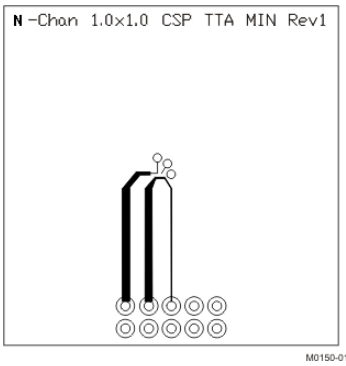
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient (minimum Cu area)			228.6	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (1 in^2 Cu area)			131.1	°C/W



Max $R_{\theta JA}$ = 131.1°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 228.6°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

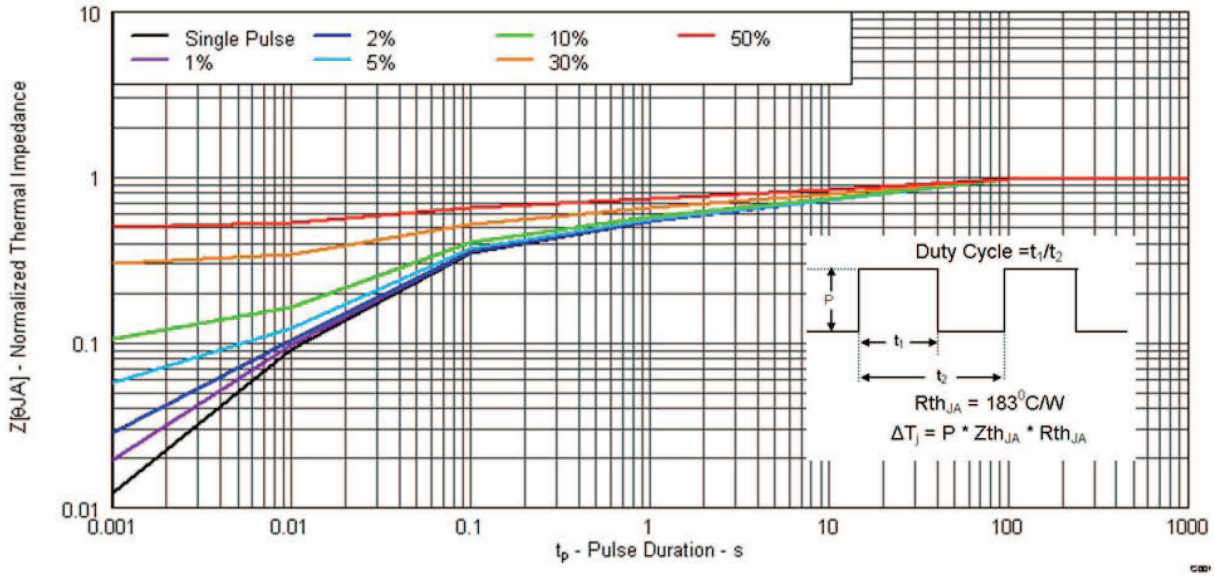


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

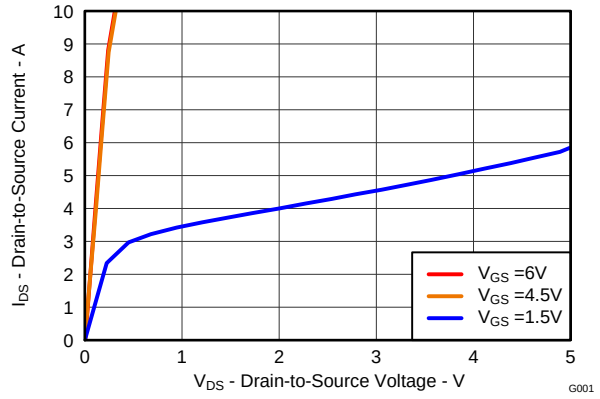


Figure 2. Saturation Characteristics

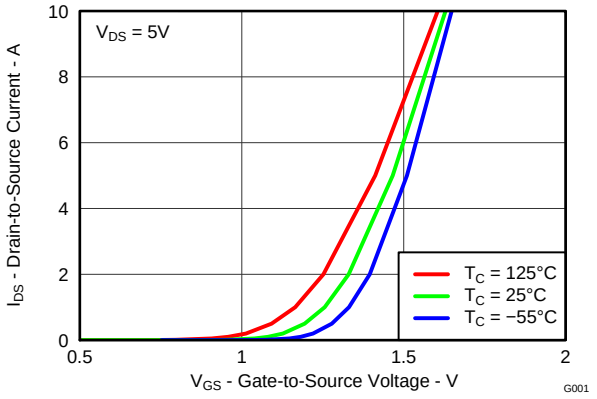


Figure 3. Transfer Characteristics

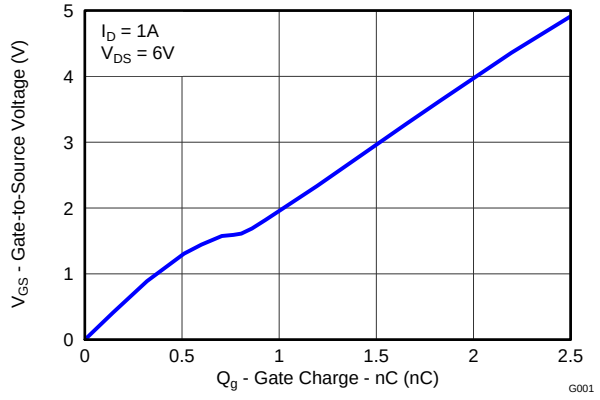


Figure 4. Gate Charge

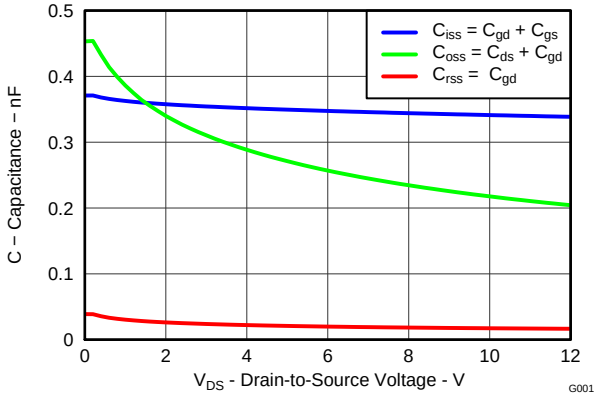


Figure 5. Capacitance

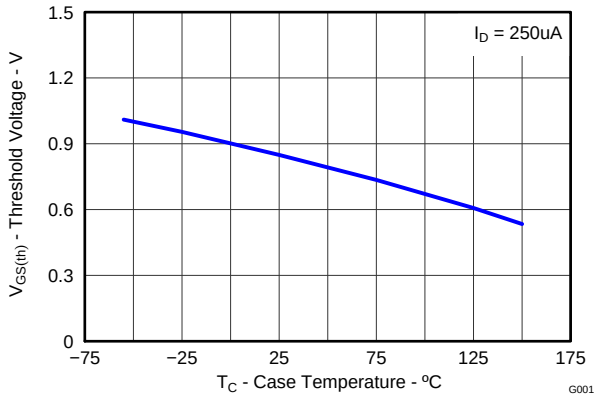


Figure 6. Threshold Voltage vs Temperature

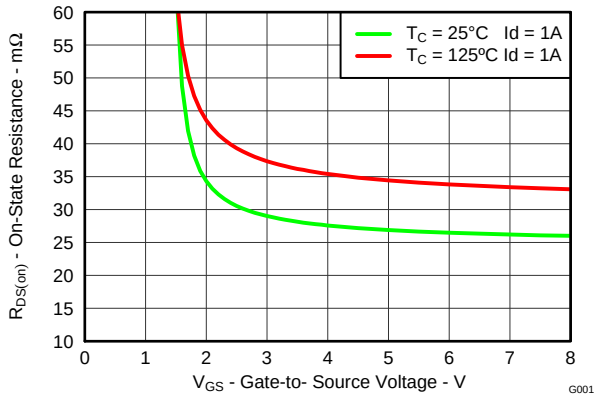


Figure 7. On Resistance vs Gate Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

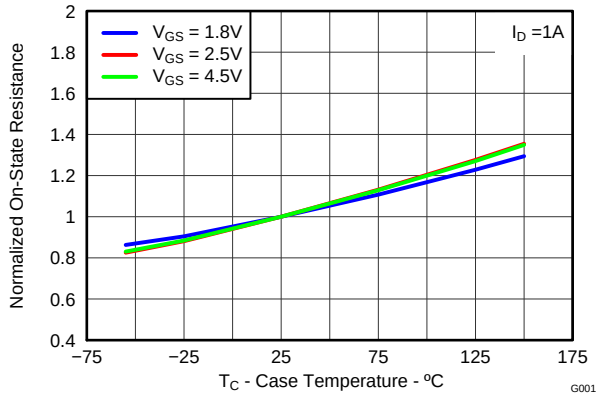


Figure 8. On Resistance vs Temperature

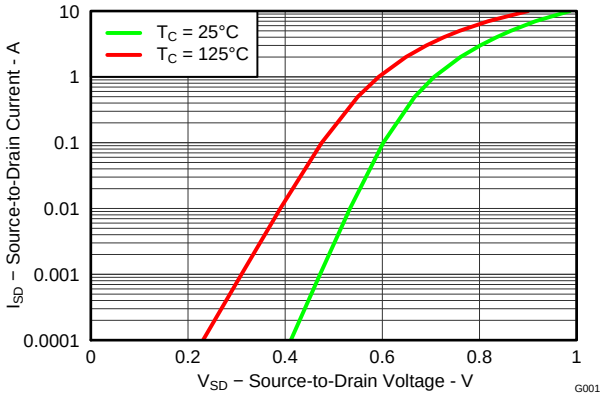


Figure 9. Typical Diode Forward Voltage

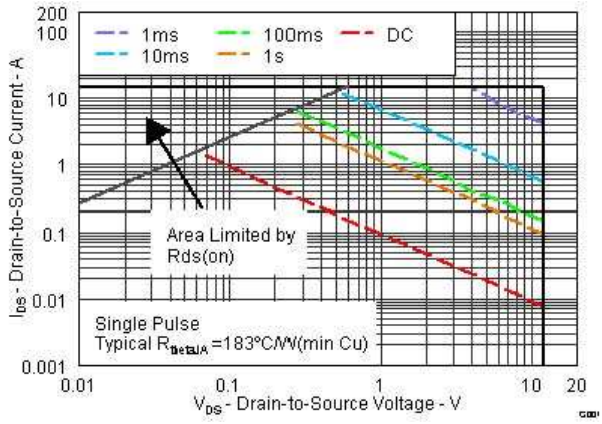


Figure 10. Maximum Safe Operating Area

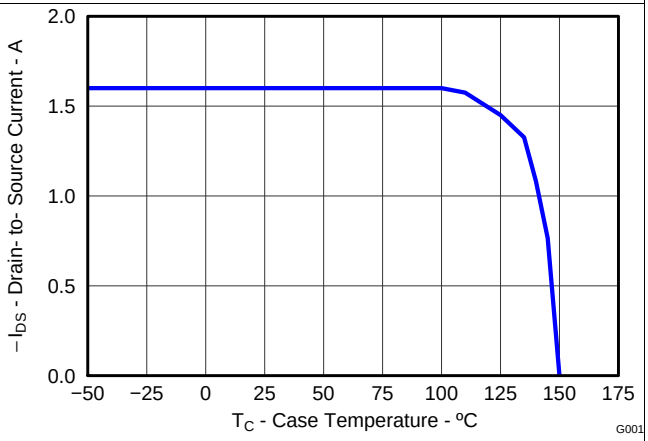


Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

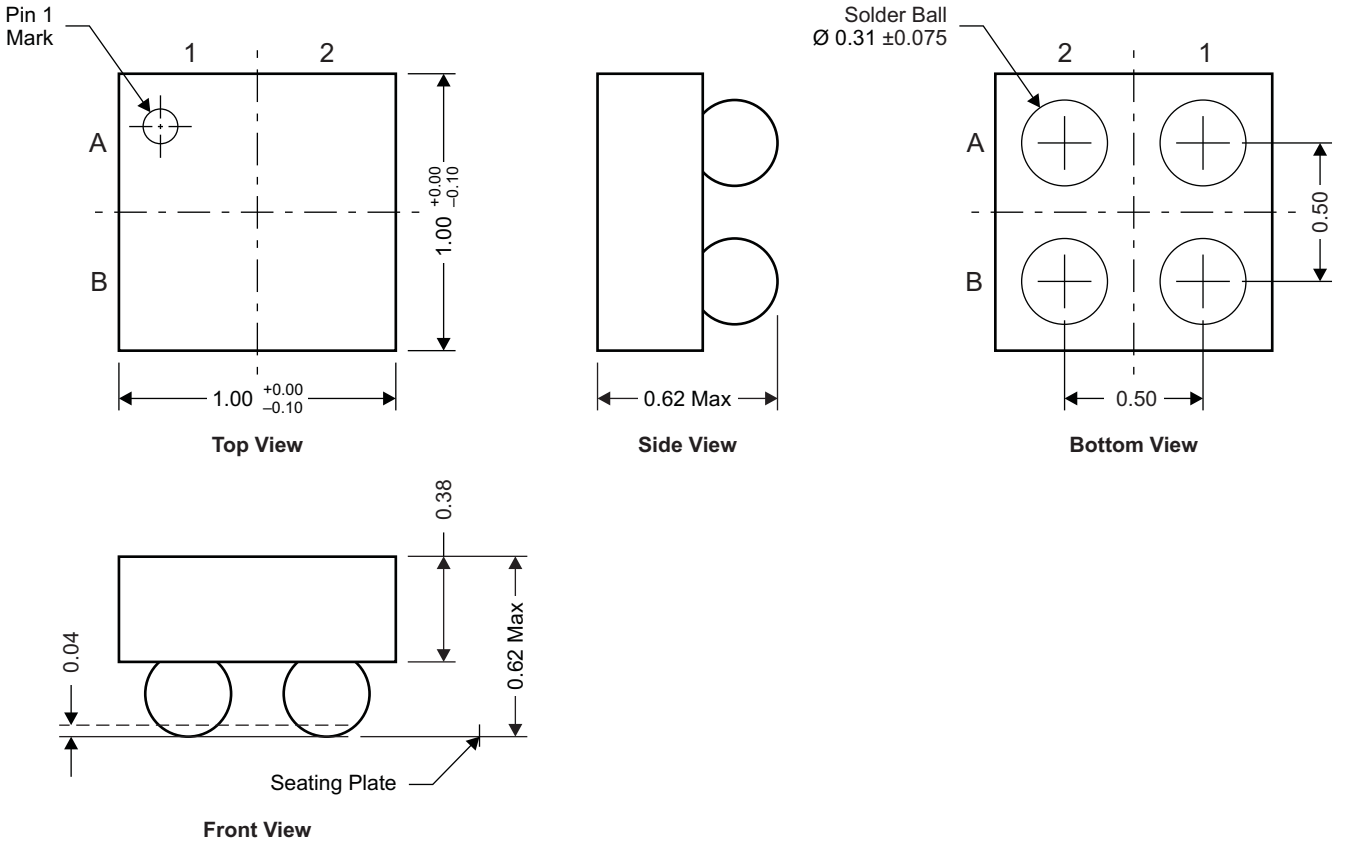
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD13201W10 Package Dimensions

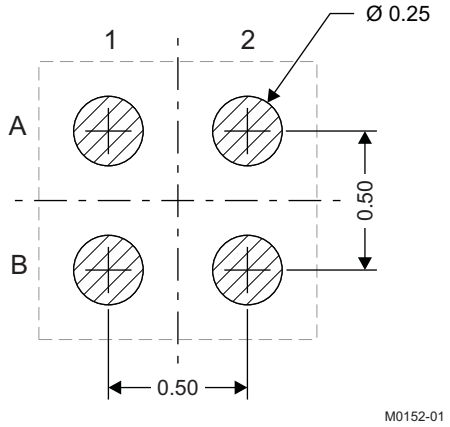


NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

7.2 Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD13201W10	Active	Production	DSBGA (YZB) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	201
CSD13201W10.B	Active	Production	DSBGA (YZB) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

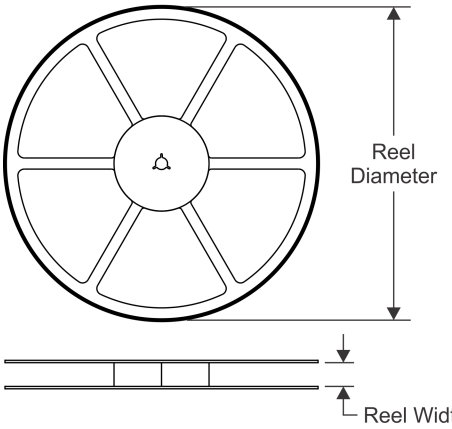
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

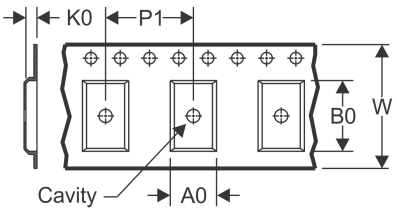
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

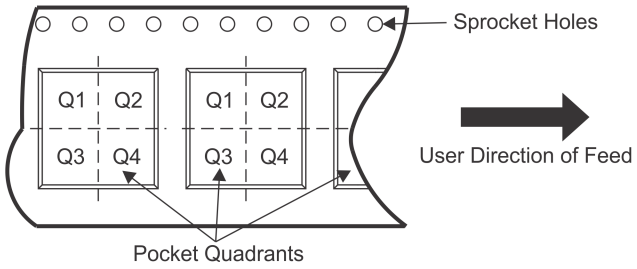


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

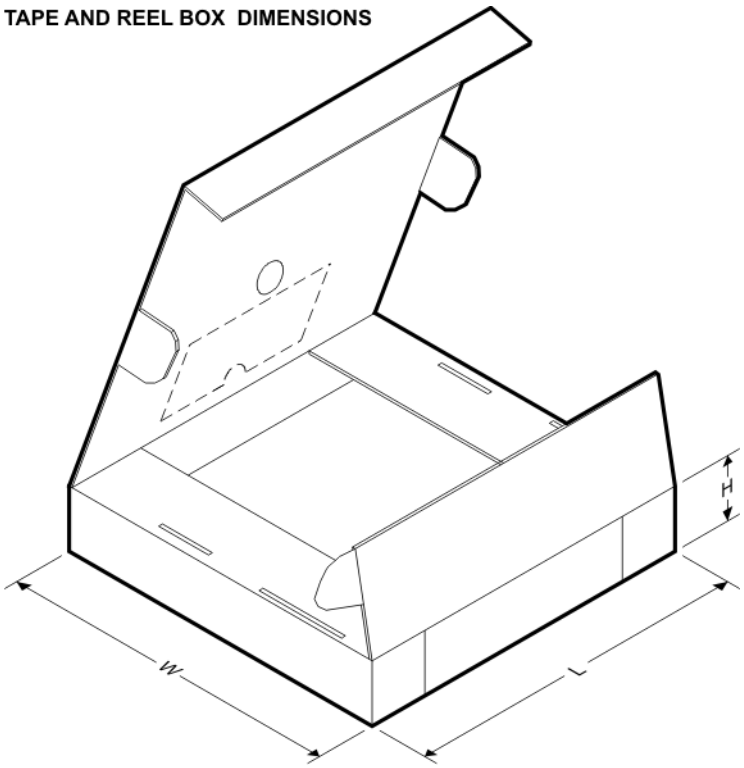
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13201W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	2.0	8.0	Q1

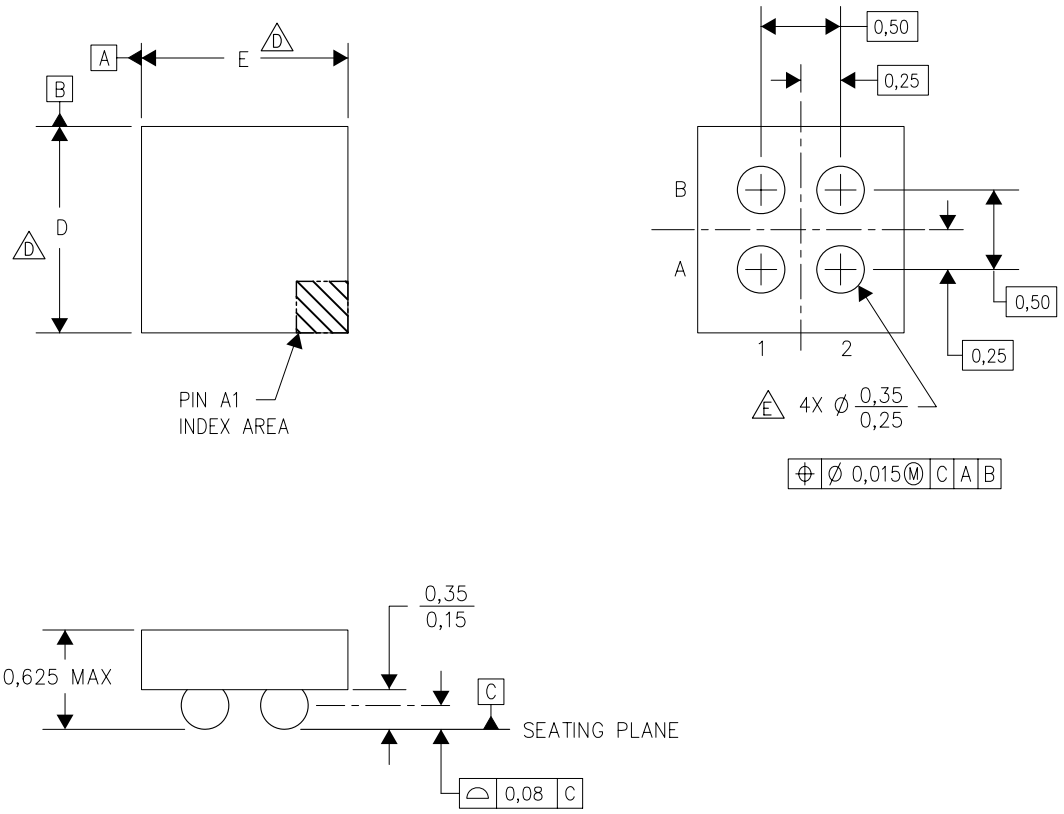
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13201W10	DSBGA	YZB	4	3000	182.0	182.0	20.0

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



4205055/D 07/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls.
Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

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Last updated 10/2025