

CSD75207W15 Dual P-Channel NexFET™ Power MOSFET

1 Features

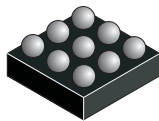
- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1.5-mm × 1.5-mm
- Gate-Source Voltage Clamp
- Gate ESD Protection >4 kV
 - HBM JEDEC standard JESD22-A114
- Pb and Halogen Free
- RoHS Compliant

2 Applications

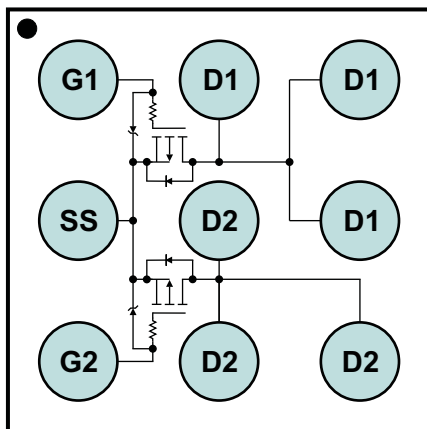
- Battery Management
- Battery Protection
- Load and Input Switching

3 Description

The CSD75207W15 device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery-operated space-constrained applications. The device has also been awarded with U.S. patents 7952145, 7420247, 7235845, and 6600182.



Top View



P0109-01

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{D1D2}	Drain-to-Drain Voltage	-20		V
Q_g	Gate Charge Total (-4.5 V)	2.9		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{D1D2(on)}$	Drain-to-Drain On Resistance	$V_{GS} = -1.8\text{ V}$	119	m Ω
		$V_{GS} = -2.5\text{ V}$	64	m Ω
		$V_{GS} = -4.5\text{ V}$	45	m Ω
$V_{GS(th)}$	Threshold Voltage	-0.8		V

Ordering Information⁽¹⁾

Device	Package	Media	Qty	Ship
CSD75207W15	1.5-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

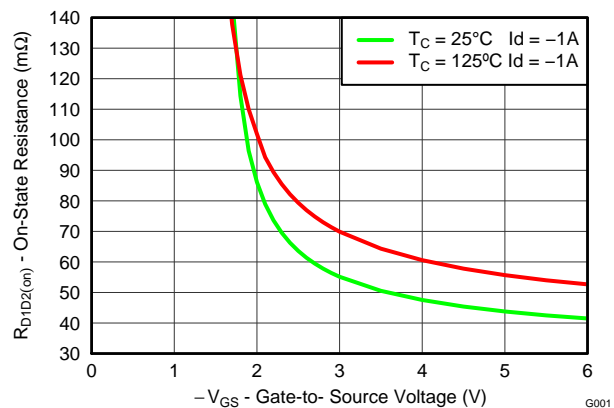
$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{D1D2}	Drain-to-Drain Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	-6.0	V
I_{D1D2}	Continuous Drain to Drain Current ^{(1) (2)}	-3.9	A
	Pulsed Drain to Drain Current, $T_C = 25^\circ\text{C}$ ⁽³⁾	-24	A
I_S	Continuous Source Pin Current	-1.2	A
	Pulsed Source Pin Current ⁽³⁾	-15	A
I_G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current ⁽³⁾	-7	A
P_D	Power Dissipation ⁽¹⁾	0.7	W
$T_{J, stg}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

(1) Per device, both sides in conduction

(2) Device operating at a temperature of 105 $^\circ\text{C}$

(3) Pulse duration 10 μs , duty cycle $\leq 2\%$

$R_{D1D2(on)}$ vs V_{GS}



G001



Table of Contents

1 Features	1	6 Device and Documentation Support	7
2 Applications	1	6.1 Trademarks	7
3 Description	1	6.2 Electrostatic Discharge Caution	7
4 Revision History	2	6.3 Glossary	7
5 Specifications	3	7 Mechanical, Packaging, and Orderable Information	8
5.1 Electrical Characteristics	3	7.1 CSD75207W15 Package Dimensions	8
5.2 Thermal Information	3	7.2 Recommended PCB Land Pattern	9
5.3 Typical MOSFET Characteristics	4	7.3 Tape and Reel Information	9

4 Revision History

Changes from Original (June 2013) to Revision A	Page
• Increased continuous drain to drain current to 3.9 A	1
• Updated the continuous drain to drain current conditions to specify a temperature of 105°C	1

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration).

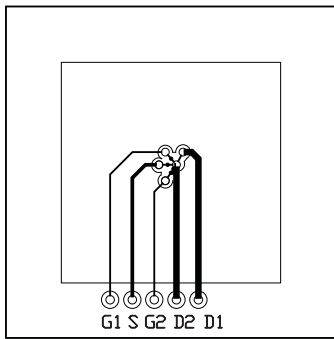
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{D1D2}	Drain-to-Drain Voltage	$V_{GS} = 0\text{ V}, I_{D1D2} = -250\ \mu\text{A}$	-20			V
BV_{GSS}	Gate-to-Source Voltage	$V_{D1D2} = 0\text{ V}, I_G = -250\ \mu\text{A}$	-6			V
I_{DDS}	Drain-to-Drain Leakage Current	$V_{GS} = 0\text{ V}, V_{D1D2} = -16\text{ V}$			-1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{D1D2} = 0\text{ V}, V_{GS} = -6\text{ V}$			-100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{D1D2} = V_{GS}, I_{DS} = -250\ \mu\text{A}$	-0.6	-0.8	-1.1	V
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	$V_{GS} = -1.8\text{ V}, I_{D1D2} = -1\text{ A}$		119	162	m Ω
		$V_{GS} = -2.5\text{ V}, I_{D1D2} = -1\text{ A}$		64	77	m Ω
		$V_{GS} = -4.5\text{ V}, I_{D1D2} = -1\text{ A}$		45	54	m Ω
g_{fs}	Transconductance	$V_{D1D2} = -10\text{ V}, I_{D1D2} = -1\text{ A}$		6.2		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{D1D2} = -10\text{ V}, f = 1\text{ MHz}$		458	595	pF
C_{OSS}	Output Capacitance			225	293	pF
C_{RSS}	Reverse Transfer Capacitance			10.4	13.5	pF
R_g	Series Gate Resistance			27		Ω
Q_g	Gate Charge Total (-4.5 V)	$V_{D1D2} = -10\text{ V}, I_{D1D2} = -1\text{ A}$		2.9	3.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.4		nC
Q_{gs}	Gate Charge – Gate to Source			0.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.4		nC
Q_{OSS}	Output Charge		$V_{D1D2} = -9.5\text{ V}, V_{GS} = 0\text{ V}$		3.1	
$t_{d(on)}$	Turn On Delay Time	$V_{D1D2} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_{D1D2} = -1\text{ A}, R_G = 30\ \Omega$		12.8		ns
t_r	Rise Time			8.6		ns
$t_{d(off)}$	Turn Off Delay Time			32.1		ns
t_f	Fall Time			16.0		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_{D1D2} = -1\text{ A}, V_{GS} = 0\text{ V}$	-0.8		-1	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -10\text{ V}, I_F = -1\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		10.5		nC
t_{rr}	Reverse Recovery Time	$V_{dd} = -10\text{ V}, I_F = -1\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		23		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

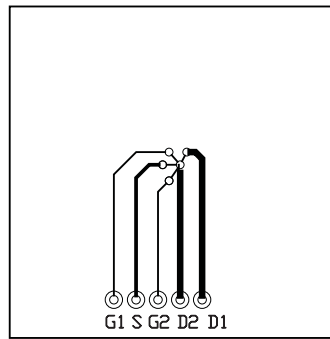
THERMAL METRIC		TYPICAL VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^{(1) (2)}	70	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ^{(3) (2)}	165	

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1-inch² of Cu (2 oz).



M0169-01

Typ $R_{\theta JA} = 70^{\circ}\text{C/W}$
when mounted on
1-inch² of 2 oz. Cu.

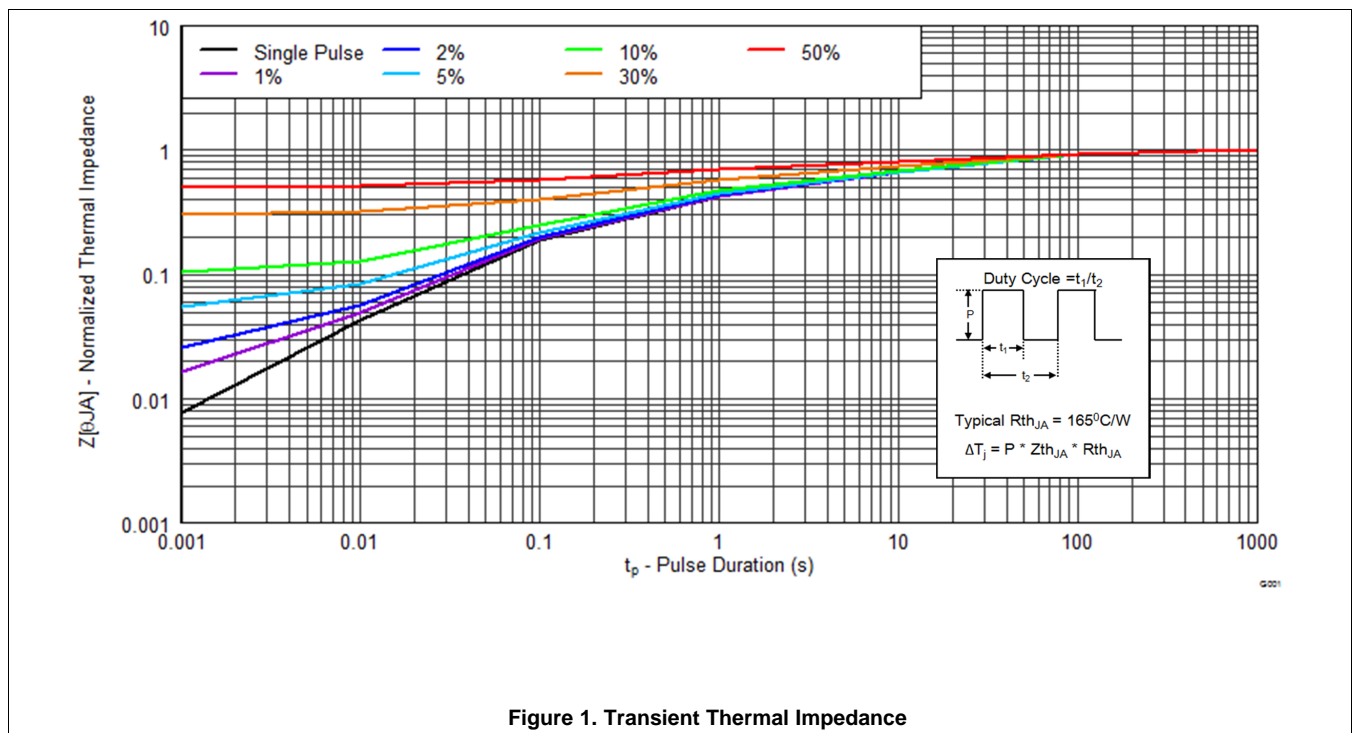


M0170-01

Typ $R_{\theta JA} = 165^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

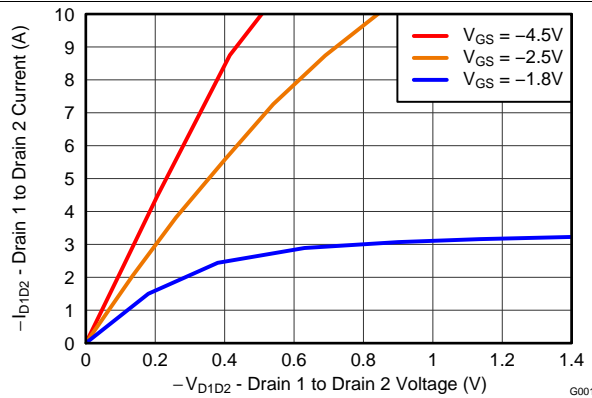


Figure 2. Saturation Characteristics

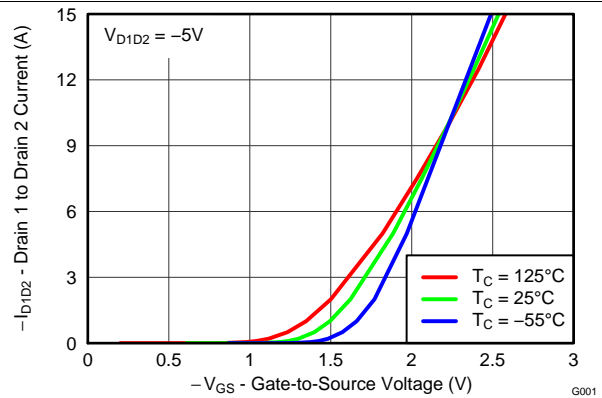


Figure 3. Transfer Characteristics

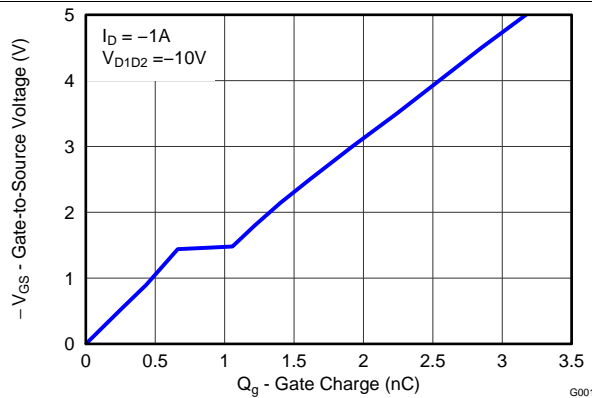


Figure 4. Gate Charge

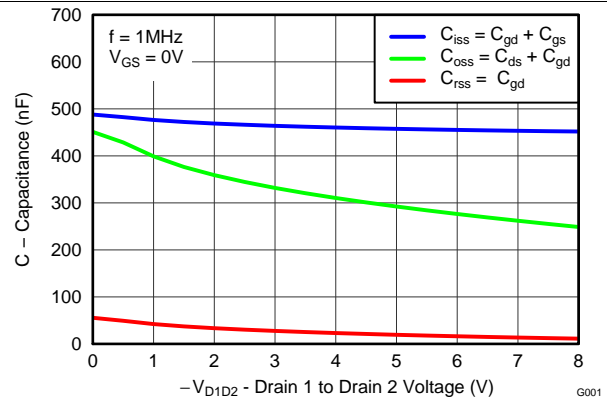


Figure 5. Capacitance

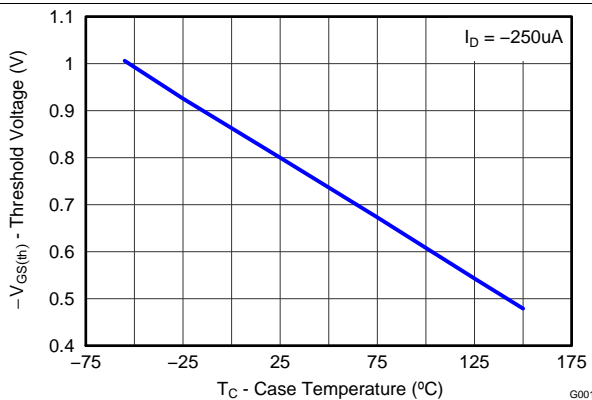


Figure 6. Threshold Voltage vs Temperature

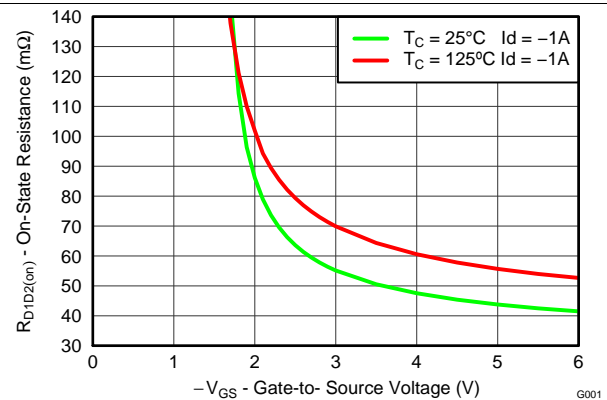


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

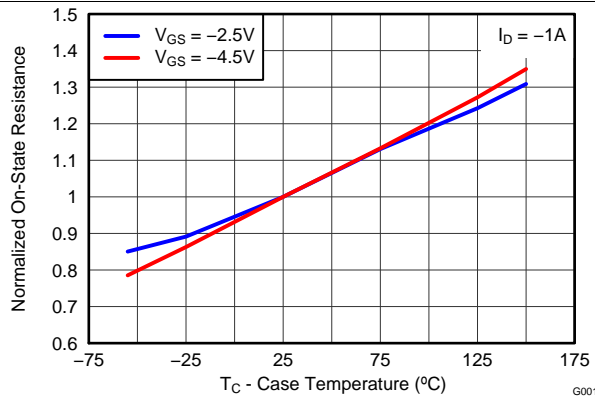


Figure 8. Normalized On-State Resistance vs Temperature

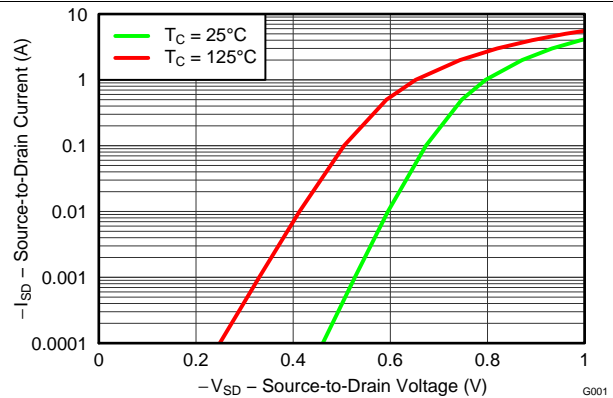


Figure 9. Typical Diode Forward Voltage

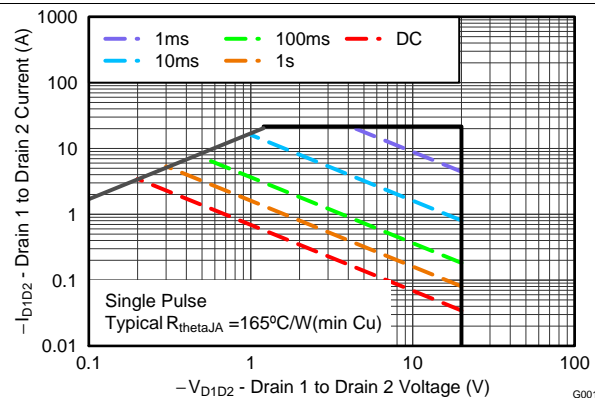


Figure 10. Maximum Safe Operating Area

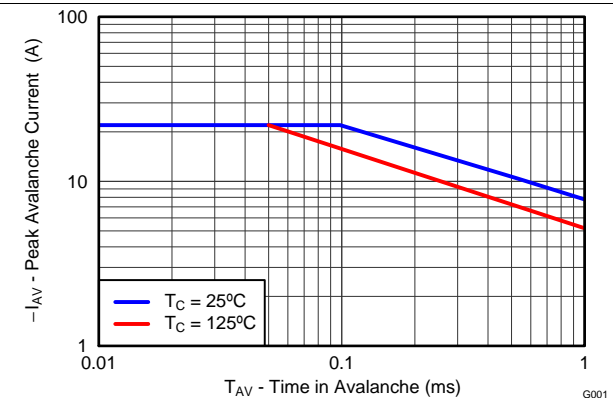


Figure 11. Single Pulse Unclamped Inductive Switching

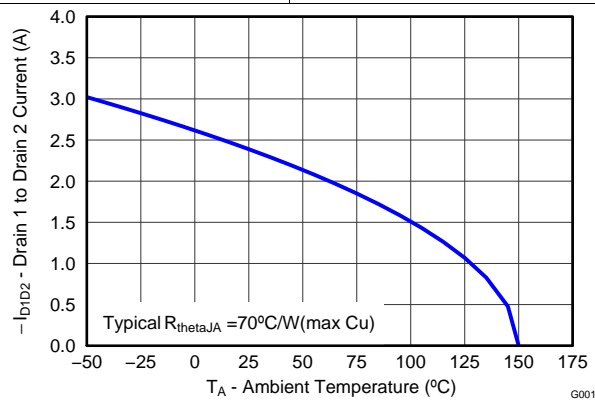


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

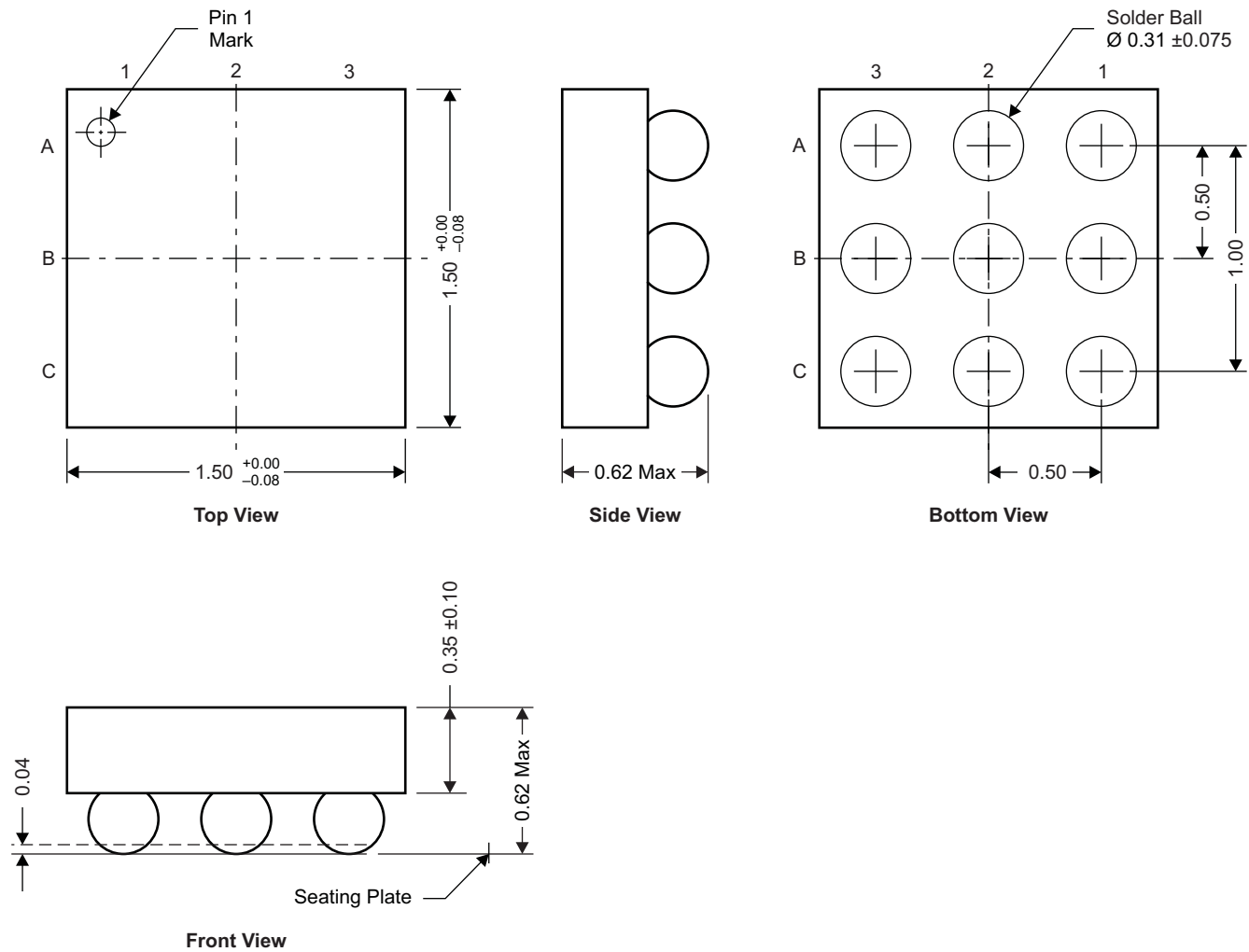
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD75207W15 Package Dimensions



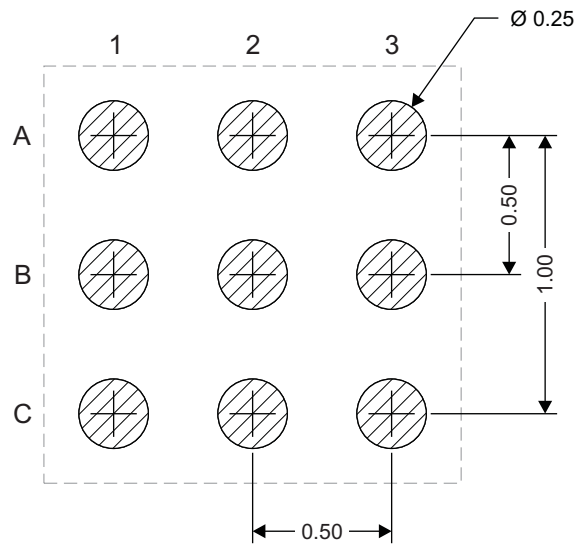
M0171-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

POSITION	DESIGNATION
A1	Gate1
A2, A3, B3	Drain1
C1	Gate2
C2, C3, B2	Drain2
B1	Source Sense

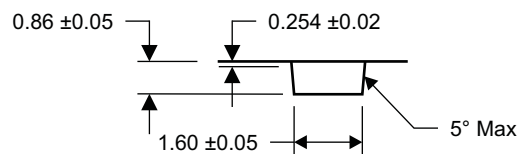
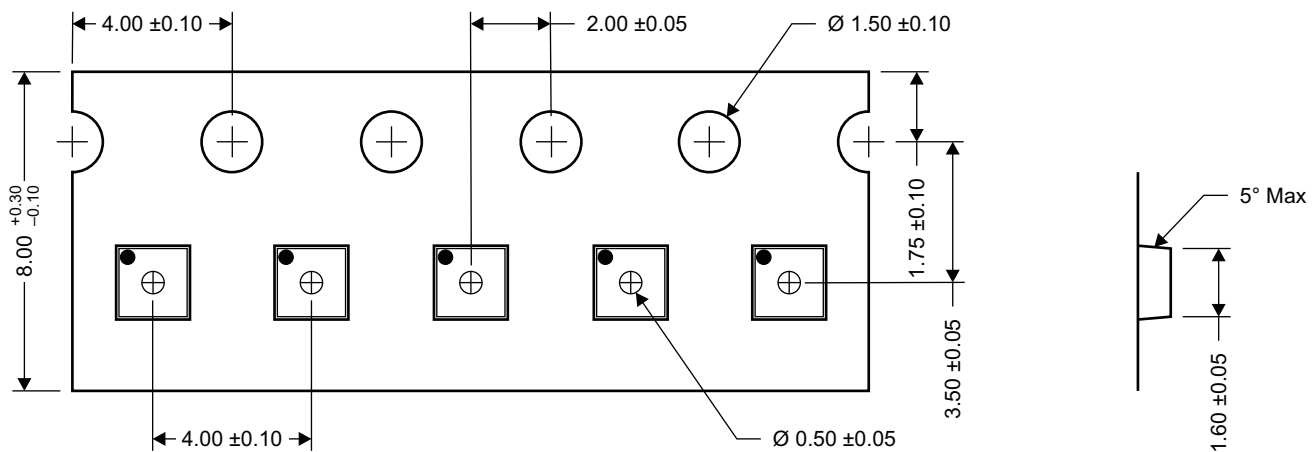
7.2 Recommended PCB Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



M0173-01

NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75207W15	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated