

# CY54FCT273T, CY74FCT273T 8-BIT REGISTERS

SCCS020A – MARCH 1995 – REVISED OCTOBER 2001

- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Fully Compatible With TTL Input and Output Logic Levels**
- **CY54FCT273T**
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- **CY74FCT273T**
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

## description

The 'FCT273T devices consist of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered-clock (CP) and master-reset ( $\overline{MR}$ ) inputs load and reset all flip-flops simultaneously. These devices are edge-triggered registers. The state of each D input (one setup time before the low-to-high clock transition) is transferred to the corresponding flip-flop's Q output. All outputs are forced low by a low logic level on the  $\overline{MR}$  input.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**CY54FCT273T . . . D PACKAGE  
CY74FCT273T . . . Q OR SO PACKAGE  
(TOP VIEW)**



**CY54FCT273T . . . L PACKAGE  
(TOP VIEW)**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# CY54FCT273T, CY74FCT273T 8-BIT REGISTERS

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## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	5.8	CY74FCT273CTQCT	FCT273C
	SOIC – SO	Tube	5.8	CY74FCT273CTSOC	FCT273C
		Tape and reel	5.8	CY74FCT273CTSOCT	
	QSOP – Q	Tape and reel	7.2	CY74FCT273ATQCT	FCT273A
		SOIC – SO	Tube	7.2	CY74FCT273ATSOC
	Tape and reel		7.2	CY74FCT273ATSOCT	
-55°C to 125°C	QSOP – Q	Tape and reel	13	CY74FCT273TQCT	FCT273
	SOIC – SO	Tube	13	CY74FCT273TSOC	FCT273
		Tape and reel	13	CY74FCT273TSOCT	
LCC – L	Tube	8.3	CY54FCT273ATLMB		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS			OUTPUT Q	OPERATING MODE
$\overline{MR}$	CP	D		
L	X	X	L	Reset (clear)
H	↑	h	H	Load '1'
H	↑	l	L	Load '0'

H = High logic level steady state, h = High logic level one setup time prior to low-to-high clock transition, L = Low logic level steady state, l = Low logic level one setup time prior to the low-to-high transition, X = Don't care, ↑ = Low-to-high clock transition

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	68°C/W
SO package .....	58°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{Stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	CY54FCT273T			CY74FCT273T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage	0.8			0.8			V
$I_{OH}$ High-level output current	–12			–32			mA
$I_{OL}$ Low-level output current	32			64			mA
$T_A$ Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

# CY54FCT273T, CY74FCT273T

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT273T			CY74FCT273T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	-0.7	-1.2					V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2			
		I <sub>OH</sub> = -15 mA			2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>			5				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>					5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V					±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V					±1		
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V			±1			±1	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1	0.2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open	0.5	2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open				0.5	2		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS		CY54FCT273T		CY74FCT273T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$I_{CCD}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ , Outputs open, One bit switching at 50% duty cycle, $\overline{MR} = V_{CC}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.06	0.12			mA/ MHz	
	$V_{CC} = 5.25\text{ V}$ , Outputs open, One bit switching at 50% duty cycle, $\overline{MR} = V_{CC}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$				0.06	0.12		
$I_C^{\#}$	$V_{CC} = 5.5\text{ V}$ , $f_0 = 10\text{ MHz}$ , Outputs open, $\overline{MR} = V_{CC}$	One bit switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4		mA	
			$V_{IN} = 3.4\text{ V}$ or GND	1.2	3.4			
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	1.6	3.2 $\parallel$			
			$V_{IN} = 3.4\text{ V}$ or GND	3.9	12.2 $\parallel$			
	$V_{CC} = 5.25\text{ V}$ , $f_0 = 10\text{ MHz}$ , Outputs open, $\overline{MR} = V_{CC}$	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.7		1.4
			$V_{IN} = 3.4\text{ V}$ or GND			1.2		3.4
		Eight bits switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			1.6		3.2 $\parallel$
			$V_{IN} = 3.4\text{ V}$ or GND			3.9		12.2 $\parallel$
$C_i$			5	10	5	10	pF	
$C_o$			9	12	9	12	pF	

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the  $I_{CC}$  formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

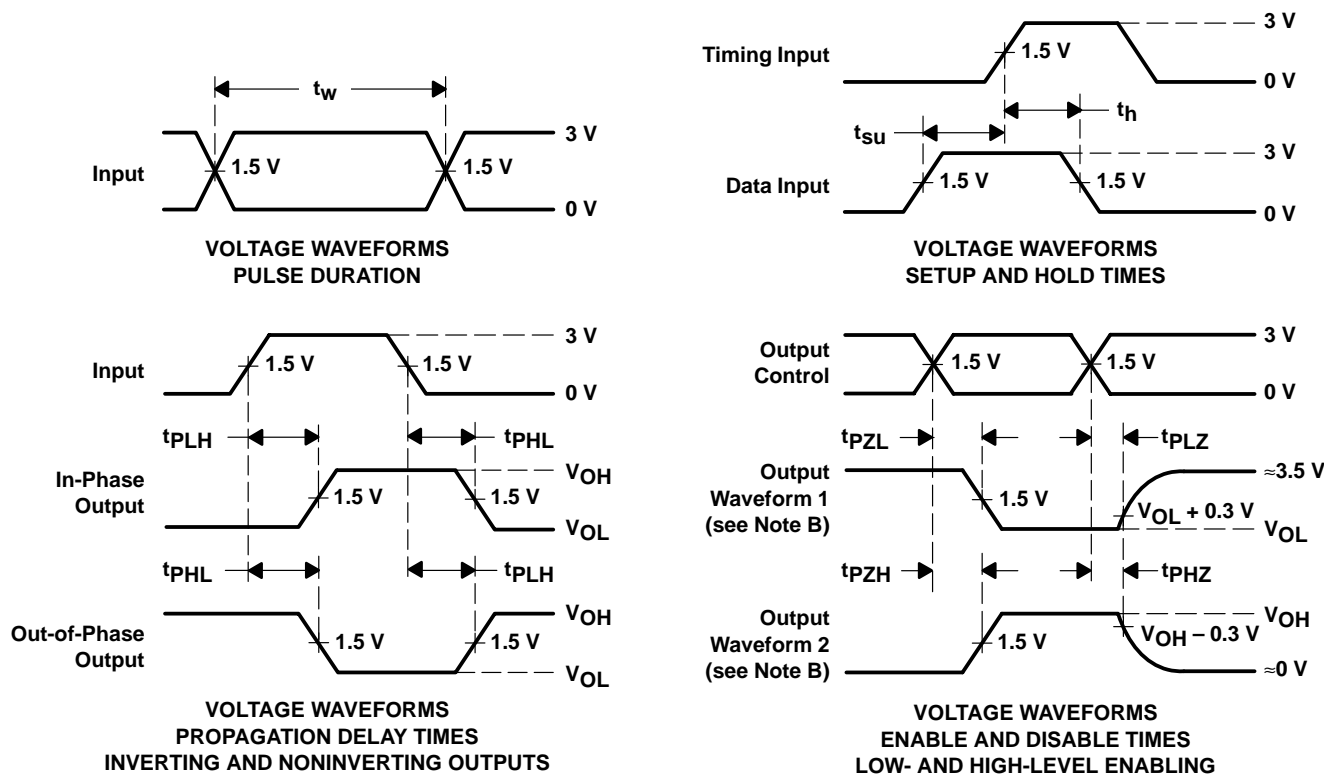
			CY74FCT273T		CY54FCT273AT		CY74FCT273AT		CY74FCT273CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, high or low	CP	6		6		6		6		ns
		$\overline{\text{MR}}$	6		6		6		6		
t <sub>su</sub>	Setup time, high or low	D before CP↑	2		2		2		2		ns
t <sub>h</sub>	Hold time, high or low	D after CP↑	1.5		1.5		1.5		1.5		ns
t <sub>rec</sub>	Recovery time	$\overline{\text{MR}}$ after CP↑	2		2.5		2		2		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT273T		CY54FCT273AT		CY74FCT273AT		CY74FCT273CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CP	Q	2	13	2	8.3	2	7.2	2	5.8	ns
t <sub>PHL</sub>			2	13	2	8.3	2	7.2	2	5.8	
t <sub>PLH</sub>	$\overline{\text{MR}}$	Q	2	13	2	8.3	2	7.2	2	6.1	ns
t <sub>PHL</sub>			2	13	2	8.3	2	7.2	2	6.1	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9221503M2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221503M2A CY54FCT 273ATLMB
<a href="#">5962-9221503MRA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221503MRA
<a href="#">CY54FCT273ATLMB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221503M2A CY54FCT 273ATLMB
<a href="#">CY74FCT273ATQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273A
<a href="#">CY74FCT273ATQCT.B</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273A
<a href="#">CY74FCT273ATQCTG4</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273A
<a href="#">CY74FCT273ATQCTG4.B</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273A
<a href="#">CY74FCT273ATSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A
<a href="#">CY74FCT273ATSOC.B</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A
<a href="#">CY74FCT273ATSOCT</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A
<a href="#">CY74FCT273ATSOCT.B</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273A
<a href="#">CY74FCT273CTQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273C
<a href="#">CY74FCT273CTQCT.B</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273C
<a href="#">CY74FCT273CTSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273C
<a href="#">CY74FCT273CTSOC.B</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273C
<a href="#">CY74FCT273TQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273
<a href="#">CY74FCT273TQCT.B</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT273
<a href="#">CY74FCT273TSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273
<a href="#">CY74FCT273TSOC.B</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273
<a href="#">CY74FCT273TSOCT</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273
<a href="#">CY74FCT273TSOCT.B</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT273

(1) **Status:** For more details on status, see our [product life cycle](#).



- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
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- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT273ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273ATQCTG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT273CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT273TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT273ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT273ATQCTG4	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT273ATSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT273CTQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT273TQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT273TSOCT	SOIC	DW	20	2000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9221503M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT273ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT273ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273CTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT273TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6

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