DAC60516 リファレンス内蔵、16 チャネル、12 ビット、電圧出力 DAC

1 特長

- 性能:
  - INL:12 ビット分解能で ±1LSB 以下
  - TUE (総合未調整誤差):FSR 最大値±0.15%
- 2.5V の高精度内部リファレンスを搭載
  - 初期精度:±2.5mV (最大値)
  - ドリフト:15ppm/°C (標準値)
- 高い駆動能力:電源レールからの供給で、0.5V 出力時に 50mA
- 柔軟な構成オプション
  - ユーザー選択可能なゲイン:2 ×、1 ×
  - ゼロ スケールへのリセット
  - クリア出力機能
- 広い動作範囲:
  - 電源:2.7V～5.5V
  - 温度範囲:-40°C ～ +125°C
- SPI および I²C インターフェイス:1.7V～5.5V で動作
  - SPI:4 線式インターフェイス
  - I²C:4 つのターゲット アドレス
- 小型パッケージ:
  - 4mm × 4mm、28 ピン WQFN

2 アプリケーション

- 光モジュール
- DC 間の相互接続
- アナログ出力モジュール

3 概要

12 ビット DAC60516 は、低消費電力、16 チャネル、バッファ付き、電圧出力の D/A コンバータ (DAC) です。DAC60516 には 2.5V、15ppm/°Cの内部基準電圧が搭載されているため、ほとんどのアプリケーションで外付けの高精度基準電圧を必要としません。ユーザーが選択可能なゲイン構成を使用して、2.5V または 5V のフルスケール出力電圧を供給できます。DAC60516 は、単一電源で動作します。

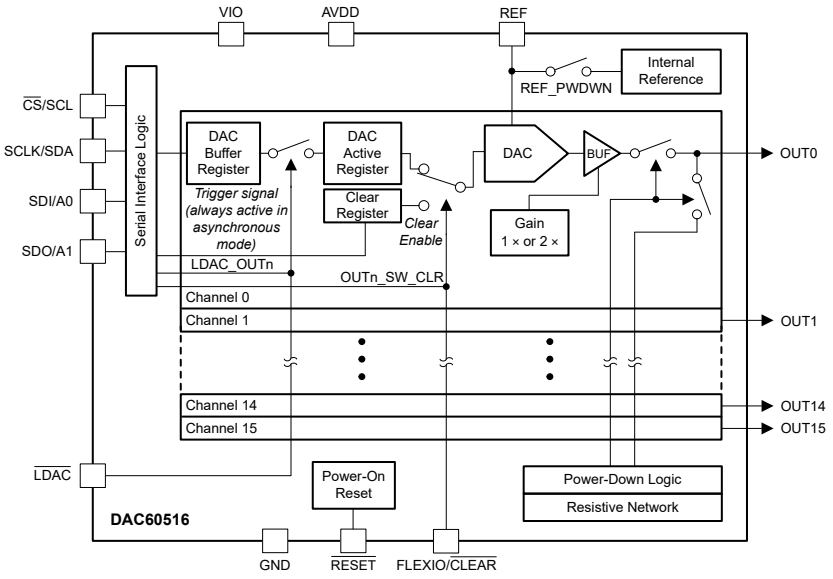
DAC60516 との通信は、SPI および I²C をサポートするシリアル インターフェイスで行われ、最大 50MHz のクロック速度で動作します (デバイスに対する SPI 書き込み中)。VIO ピンにより、1.7V～5.5V のシリアル インターフェイス動作が可能です。DAC60516 の柔軟なインターフェイスにより、業界標準の広範なマイクロプロセッサやマイクロコントローラとの動作が可能です。

DAC60516 は、-40°C～+125°Cの温度範囲で動作が規定されており、小型の WQFN パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
DAC60516	RUY (WQFN、28)	4mm × 4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Pin Configuration and Functions

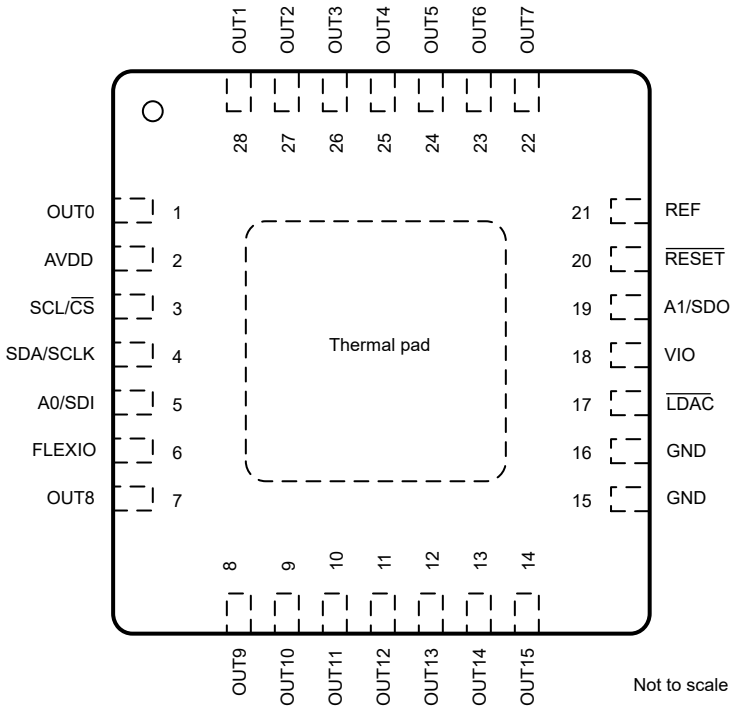


図 4-1. RUY Package, 28-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT0	Output	DAC output channel 0
2	AVDD	Power	Analog power supply
3	SCL/$\overline{CS}$	Input	I^2C: Clock input. SPI: Active-low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, this pin enables the serial interface input shift register.
4	SDA/SCLK	Input/ Output	I^2C: Bidirectional data line SPI: Clock input
5	A0/SDI	Input	I^2C: Target address selector SPI: Data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
6	FLEXIO	Input/ Output	FLEXIO pin, including GPIO and $\overline{CLEAR}$ pin functionality
7	OUT8	Output	DAC output channel 8
8	OUT9	Output	DAC output channel 9
9	OUT10	Output	DAC output channel 10
10	OUT11	Output	DAC output channel 11
11	OUT12	Output	DAC output channel 12
12	OUT13	Output	DAC output channel 13
13	OUT14	Output	DAC output channel 14
14	OUT15	Output	DAC output channel 15
15	GND	Power	Ground reference point for all circuitry on the device
16	GND	Power	Ground reference point for all circuitry on the device
17	$\overline{LDAC}$	Input	Active-low DAC synchronization signal. A high-to-low transition on the $\overline{LDAC}$ pin simultaneously updates the outputs configured in synchronous mode
18	VIO	Power	IO supply voltage. This pin sets the I/O operating voltage for the device.
19	A1/SDO	Input/ Output	I^2C: Target address selector. SPI: Data output. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit.
20	$\overline{RESET}$	Input	Active low reset input, logic low on this pin causes the device to initiate a reset event
21	REF	Input/ Output	DAC voltage reference input/output. This pin acts as input pin REFIN by default (with internal reference disabled). If internal reference is enabled, this pin acts as output pin REFOUT.
22	OUT7	Output	DAC output channel 7
23	OUT6	Output	DAC output channel 6
24	OUT5	Output	DAC output channel 5
25	OUT4	Output	DAC output channel 4
26	OUT3	Output	DAC output channel 3
27	OUT2	Output	DAC output channel 2
28	OUT1	Output	DAC output channel 1

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
AV_{DD}	Analog supply voltage, AV_{DD} to GND	–0.3	6	V
V_{IO}	Digital supply voltage, V_{IO} to GND	–0.3	AV_{DD}	V
	Analog output (OUT) pin voltage	–0.3	AV_{DD} + 0.3	V
	Reference pin voltage	–0.3	AV_{DD} + 0.3	V
	Serial interface pin voltage	–0.3	V_{IO} + 0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AV_{DD}	Analog supply voltage, AV_{DD} to GND	2.7		5.5	V
V_{IO}	IO supply voltage, V_{IO} to GND	1.7		AV_{DD}	V
	Serial interface input voltage to GND	0		V_{IO}	V
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		DAC60516 RUY (WQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, DAC outputs unloaded, and digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE (1)						
	Resolution		12			Bits
INL	Relative accuracy			±0.3	±1	LSB
DNL	Differential nonlinearity			±0.3	±1	LSB
TUE	Total unadjusted error	DAC output range = 0V to 5V		±0.04	±0.15	%FSR
	Offset error	Gain = 1 or 2		±0.75	±3	mV
	Zero-scale error	DAC register loaded with all zeroes	0	0.5	3	mV
	Full-scale error	DAC register loaded at full-scale code		±0.04	±0.15	%FSR
	Gain error	Gain = 1 or 2		±0.04	±0.15	%FSR
	Offset error drift			±3		µV/°C
	Zero-scale error drift			±2		µV/°C
	Full-scale error drift			±3		ppm FSR/°C
	Gain error drift			±2		ppm FSR/°C
	Output voltage drift over time	T_J = 25°C, DAC code = midscale, 1900 hours		20		ppm FSR
OUTPUT CHARACTERISTICS						
	Output voltage(2)	Gain = 2	0		2 × V_{REF}	V
		Gain = 1	0		V_{REF}	
	Output voltage headroom	To AV_{DD} (–50mA ≤ I_{OUT} ≤ 50mA), DAC code = full-scale	0.5			V
	Load current			50		mA
	Short-circuit current(3)	Full-scale output shorted to GND		75		mA
		Zero-scale output shorted to V_{DD}		75		
	Capacitive load(4)	R_{LOAD} = open	0		2	nF
	DC output impedance	DAC output at AV_{DD}/2		0.08		Ω
		DAC output at AV_{DD} or GND		10		
DYNAMIC PERFORMANCE						
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±1LSB, AV_{DD} = 5.5V, V_{REFIN} = 2.5V, gain = 2		6		µs
	Slew rate	AV_{DD} = 5.5V, V_{REFIN} = 2.5V		1.7		V/µs
	Power-on glitch magnitude	DAC code = zero scale		25		mV
	Output noise	At frequency = 0.1Hz to 10Hz, DAC code = midscale		12		µVpp
	Output noise density	At frequency = 1kHz, DAC code = midscale, AV_{DD} = 5.5V, V_{REFIN} = 2.5V		65		nV/Hz
	AC PSRR	DAC code = midscale, frequency = 60Hz, amplitude 200mVpp superimposed on AV_{DD}		80		dB
	DC PSRR	DAC code = midscale, AV_{DD} = 5V ±0.5V		0.02		mV/V
	Code change glitch impulse	1LSB change around major carrier		1		nV-s
	Channel-to-channel ac crosstalk	DAC code = zero scale, full-scale swing on adjacent channel		1		nV-s

5.5 Electrical Characteristics (続き)

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, DAC outputs unloaded, and digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Channel-to-channel dc crosstalk	Measured channel at zero scale, adjacent channel at full scale		12		µV
		Measured channel at zero scale, all other channels at full scale		12		
	Digital feedthrough	DAC code = midscale, f_{SCLK} = 1MHz		0.1		nV-s
	Power-up time(5)	Time for DAC channels to power on and output 0V after AV_{DD} ramps to 2.4V, V_{REFIN} = 2.5V.		120		µs
EXTERNAL REFERENCE INPUT						
V_{REFIN}	Reference input voltage range	Gain = 1	1		V_{DD}	V
		Gain = 2	1		AV_{DD}/2	
	Reference input current	V_{REFIN} = 2.5V		85		µA
	Reference input impedance			25	30	kΩ
	Reference input capacitance			5		pF
INTERNAL REFERENCE						
V_{REFOUT}	Reference output voltage range	T_J = 25°C	2.4975		2.5025	V
	Reference output drift			15	20	ppm/°C
	Reference output impedance			0.2		Ω
	Reference output noise	0.1Hz to 10Hz		10		µVpp
	Reference output noise density	10kHz, reference load = 10nF		125		nV/Hz
	Reference load current		-4		10	mA
	Reference load regulation	Source and sink		175		µV/mA
	Reference line regulation			500		µV/V
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	High-level input voltage, V_{IH}	AV_{DD} = 2.7V to 5.5V	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage, V_{IL}	AV_{DD} = 2.7V to 5.5V			0.3 × V_{IO}	V
	Input current			±2		µA
	Input pin capacitance			8		pF
V_{OH}	High-level output voltage, V_{OH}	I_{OH} = 0.2mA	V_{IO} - 0.2			V
V_{OL}	Low-level output voltage, V_{OL}	I_{OL} = 0.2mA			0.4	V
	Output pin capacitance			4		pF
POWER REQUIREMENTS						
I_{AVDD}	AV_{DD} supply current	Active mode, internal reference enabled, DAC code = full-scale, SPI static		8.5	13	mA
		Active mode, internal reference disabled, DAC code = full-scale, SPI static		8	12.5	
	AV_{DD} supply current	Power-down mode		10	20	µA
I_{VIO}	V_{IO} supply current			0.1	1	µA

(1) End point fit between codes 16 to 4080
(2) When using an external reference V_{REF} = V_{REFIN}. Otherwise, V_{REF} = 2.5V (internal reference voltage)
(3) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation at temperatures greater than the specified maximum junction temperature can impair device reliability.
(4) Specified by design and characterization, not production tested.
(5) For a further period of time equal to approximately 5ms, SPI or I2C communication to the device is blocked while the device loads internal calibration coefficients from memory. Any digital communication during this timeframe is ignored.

5.6 Timing Requirements - I²C Standard Mode

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, and digital inputs at V_{IO} or GND

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			100	kHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4000			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns
t_{VD_DAT}	Data valid time			3.45	µs
t_{VD_ACK}	Data valid acknowledge time			3.45	µs

5.7 Timing Requirements - I²C Fast Mode

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, and digital inputs at V_{IO} or GND

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			400	kHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns
t_{VD_DAT}	Data valid time			0.9	µs
t_{VD_ACK}	Data valid acknowledge time			0.9	µs

5.8 Timing Requirements - I²C Fast Mode Plus

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, and digital inputs at V_{IO} or GND

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns
t_{VD_DAT}	Data valid time			0.45	µs
t_{VD_ACK}	Data valid acknowledge time			0.45	µs

5.9 Timing Requirements - SPI

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, and digital inputs at V_{IO} or GND

		MIN	NOM	MAX	UNIT
SPI TIMING REQUIREMENTS, FSDO = 0					
$f_{(SCLK)}$	SCLK frequency			20	MHz
$t_{(SCLKH)}$	SCLK high time	20			ns
$t_{(SCLKL)}$	SCLK low time	23			ns
$t_{(SDIS)}$	SDI setup time	5			ns
$t_{(SDIH)}$	SDI hold time	8			ns
$t_{(SDOTOZ)}$	SDO active output to tri-state output delay	0		17	ns
$t_{(SDOEN)}$	SDO tri-state output to active output delay	0		21	ns
$t_{(SDOTOD)}$	SDO output delay	2		23	ns
$t_{(CSS)}$	$\overline{CS}$ setup time	15			ns
$t_{(CSH)}$	$\overline{CS}$ hold time	15			ns
$t_{(CSHIGH)}$	$\overline{CS}$ high time	15			ns
SPI TIMING REQUIREMENTS, FSDO = 1					
$f_{(SCLK)}$	SCLK frequency(1)			30	MHz
$t_{(SCLKH)}$	SCLK high time	14			ns
$t_{(SCLKL)}$	SCLK low time	16			ns
$t_{(SDIS)}$	SDI setup time	5			ns
$t_{(SDIH)}$	SDI hold time	8			ns
$t_{(SDOTOZ)}$	SDO active output to tri-state output delay	0		17	ns
$t_{(SDOEN)}$	SDO tri-state output to active output delay	0		21	ns
$t_{(SDOTOD)}$	SDO output delay	2.5		30	ns
$t_{(CSS)}$	$\overline{CS}$ setup time	15			ns
$t_{(CSH)}$	$\overline{CS}$ hold time	15			ns
$t_{(CSHIGH)}$	$\overline{CS}$ high time	15			ns

(1) Write operations to the device can be performed at frequencies up to 50MHz.

5.10 Switching Characteristics

at T_J = –40°C to +125°C, AV_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to AV_{DD}, V_{REFIN} = 2.4V to 5.5V, DAC outputs unloaded, and digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET CHARACTERISTICS						
t_{AMCRDY}	Device ready wait time	Time for valid serial interface access, measured from reset event			10	ms
t_{RESET}	$\overline{RESET}$ pulse duration		20			ns
DAC CHARACTERISTICS						
t_{DACCLR}	DAC clear response time	Time for DAC to begin code change after $\overline{CLEAR}$ trigger		50		ns
$t_{CLRWDTH}$	$\overline{CLEAR}$ pulse duration		100			ns
$t_{LDACWDTH}$	$\overline{LDAC}$ pulse duration		100			ns

5.11 Timing Diagrams

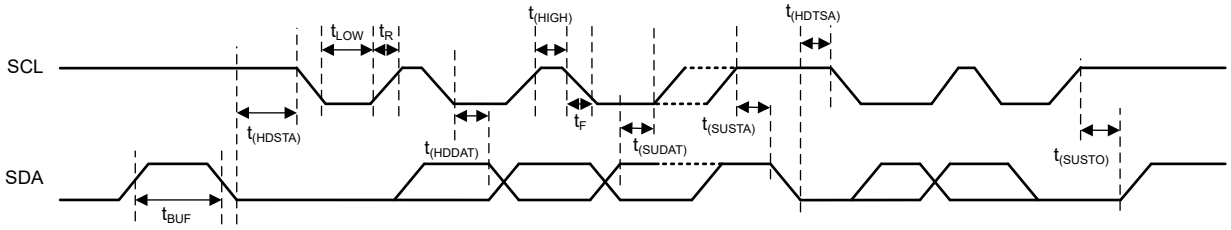


図 5-1. I²C Timing Diagram

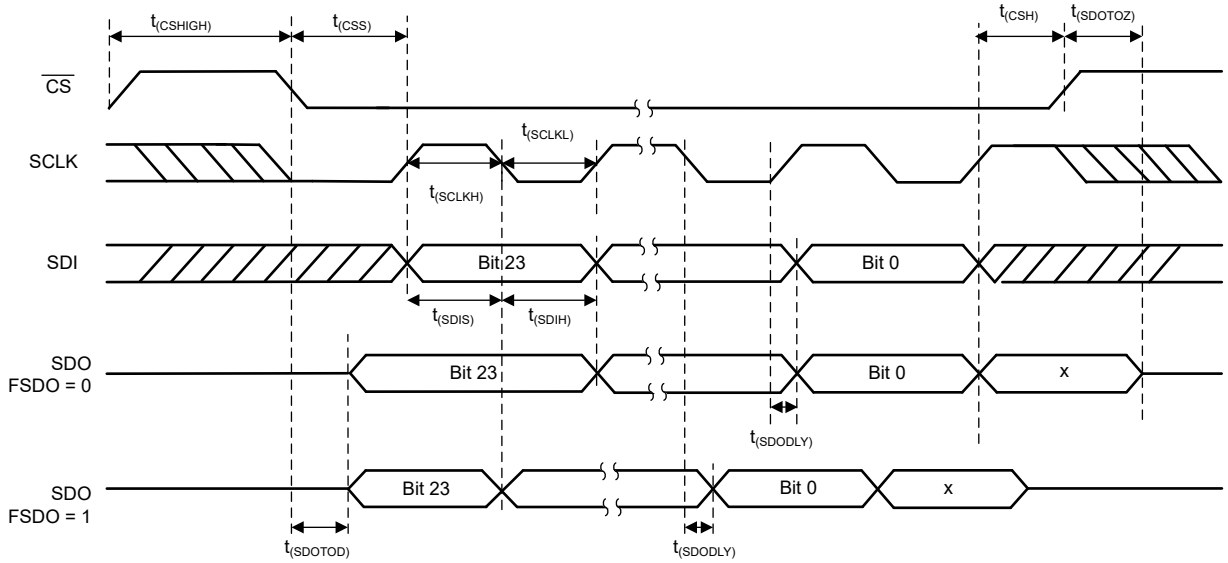


図 5-2. SPI Timing Diagram

5.12 Typical Characteristics

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)

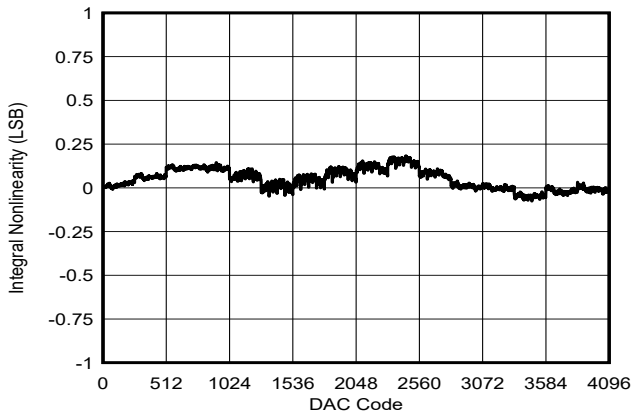


図 5-3. Integral Nonlinearity vs Digital Input Code

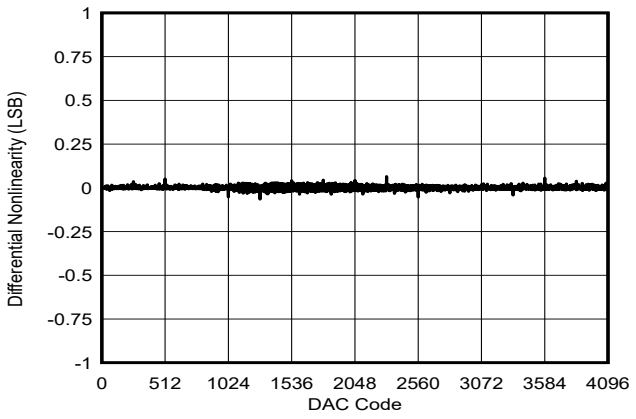


図 5-4. Differential Nonlinearity vs Digital Input Code

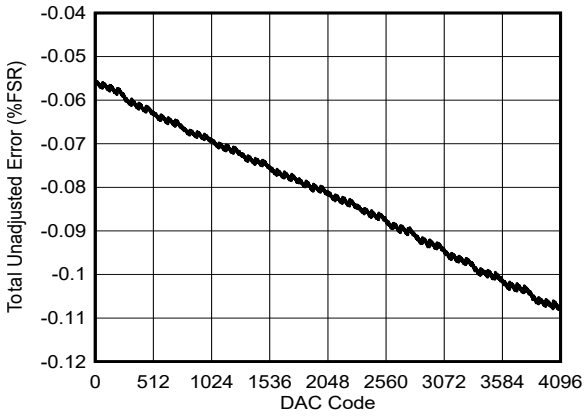


図 5-5. Total Unadjusted Error vs Digital Input Code

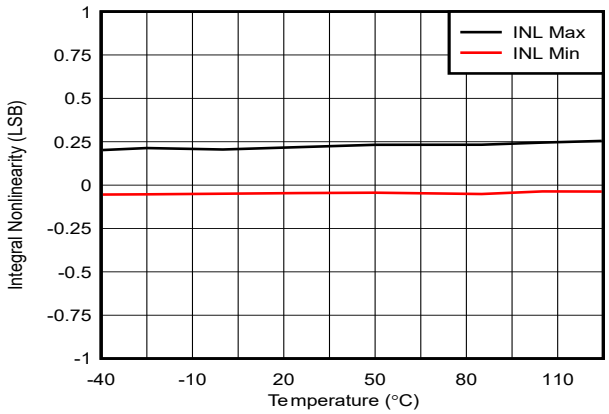


図 5-6. Integral Nonlinearity vs Temperature

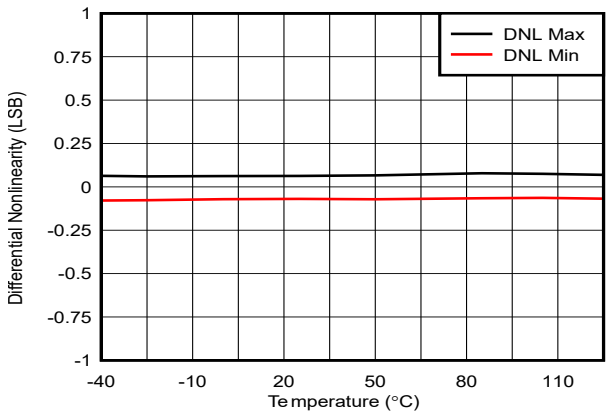


図 5-7. Differential Nonlinearity vs Temperature

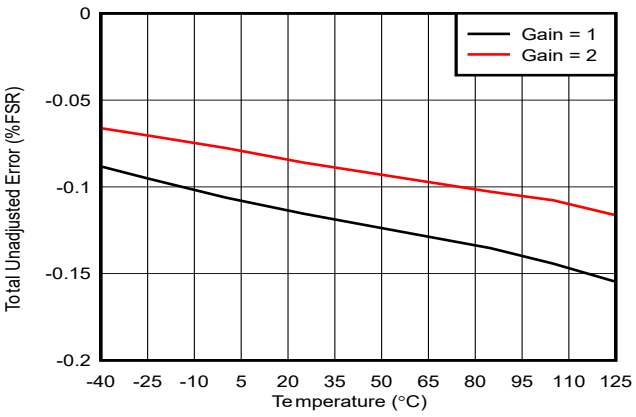


図 5-8. Total Unadjusted Error vs Temperature

5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)

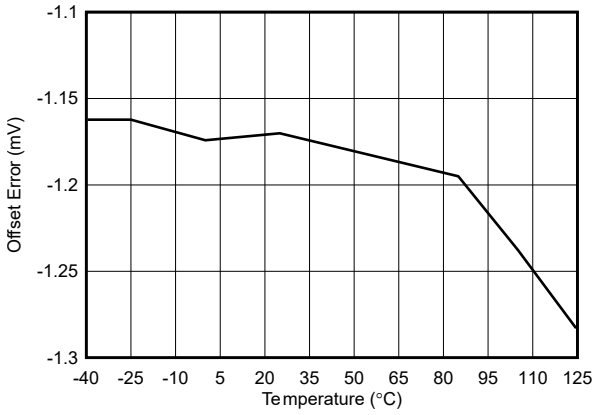


図 5-9. Offset Error vs Temperature

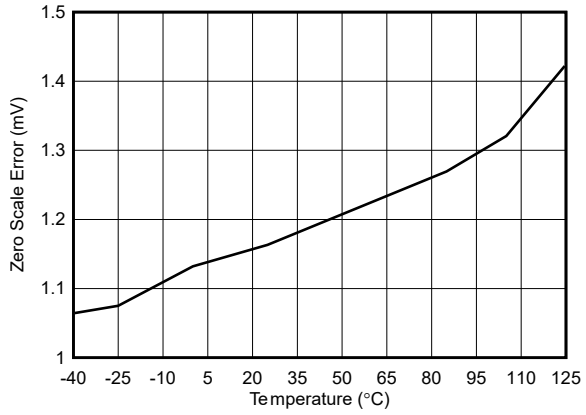


図 5-10. Zero-Scale Error vs Temperature

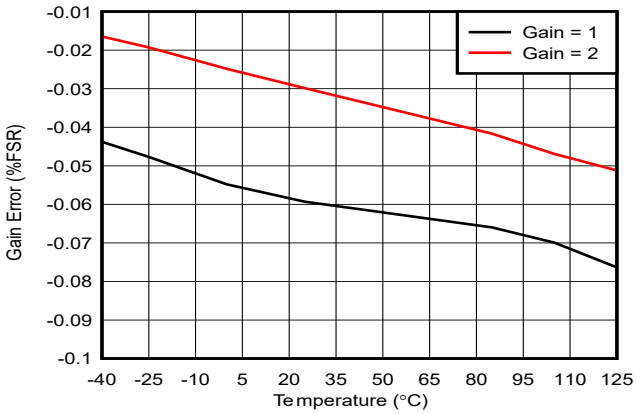


図 5-11. Gain Error vs Temperature

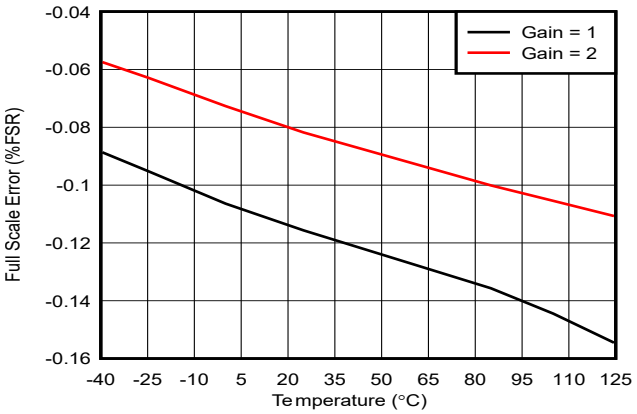


図 5-12. Full-Scale Error vs Temperature

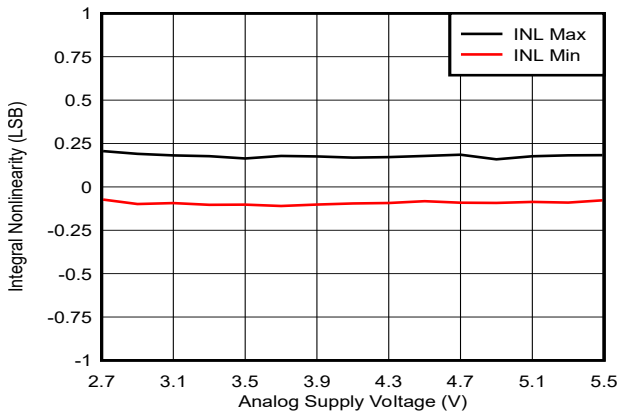


図 5-13. Integral Nonlinearity vs Supply Voltage

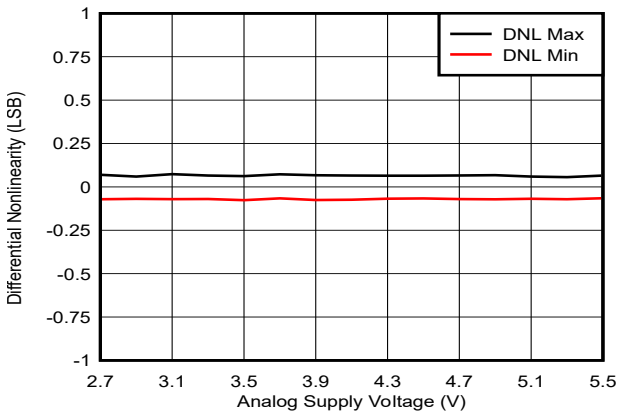


図 5-14. Differential Nonlinearity vs Supply Voltage

5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)

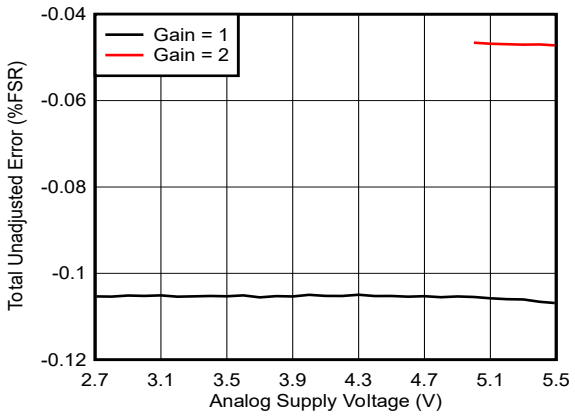


図 5-15. Total Unadjusted Error vs Supply Voltage

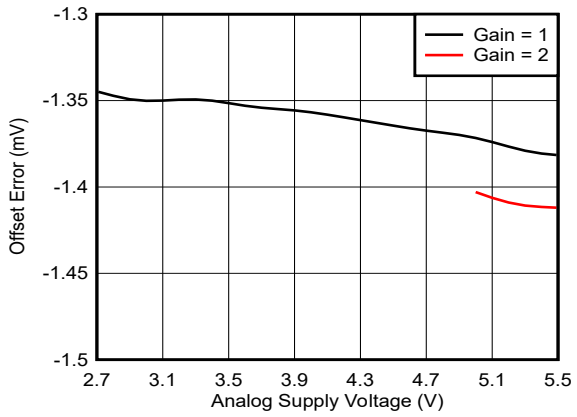


図 5-16. Offset Error vs Supply Voltage

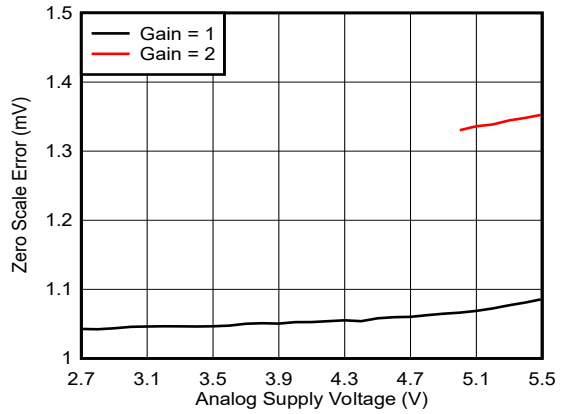


図 5-17. Zero-Scale Error vs Supply Voltage

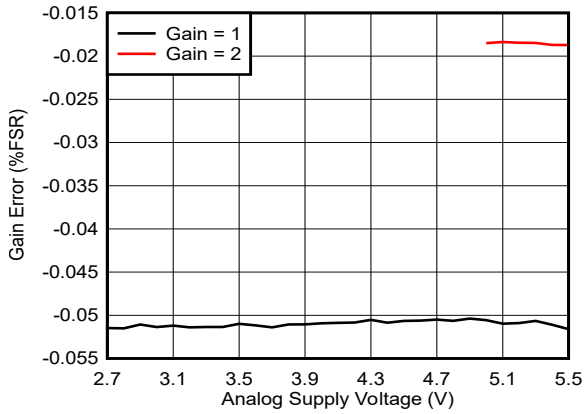


図 5-18. Gain Error vs Supply Voltage

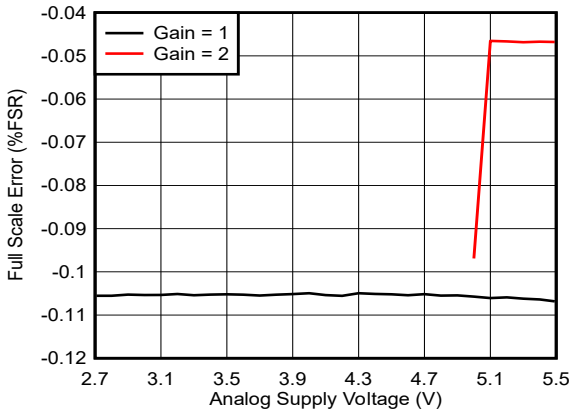


図 5-19. Full-Scale Error vs Supply Voltage

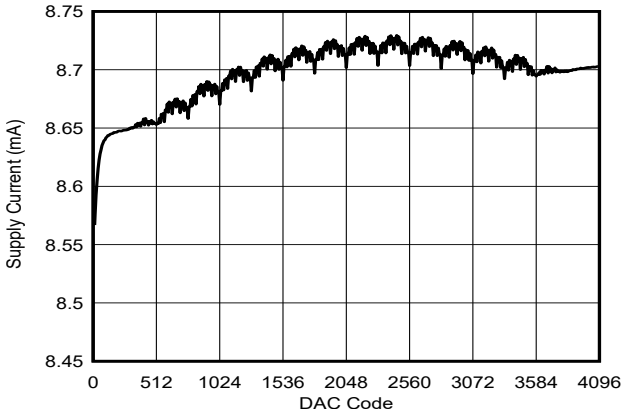
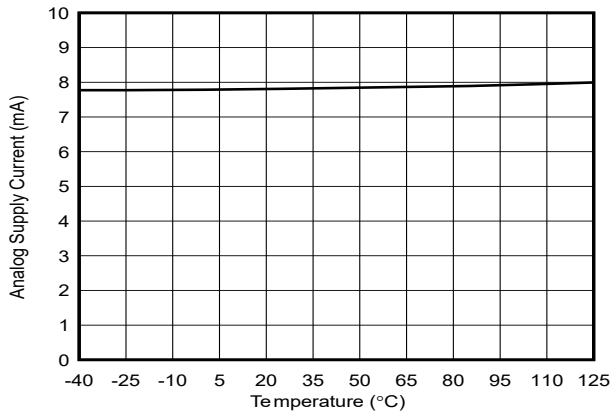


図 5-20. Supply Current With Internal Reference vs Digital Input Code

5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)



Gain = 2, external reference = 2.5V

図 5-21. Supply Current With External Reference vs Temperature

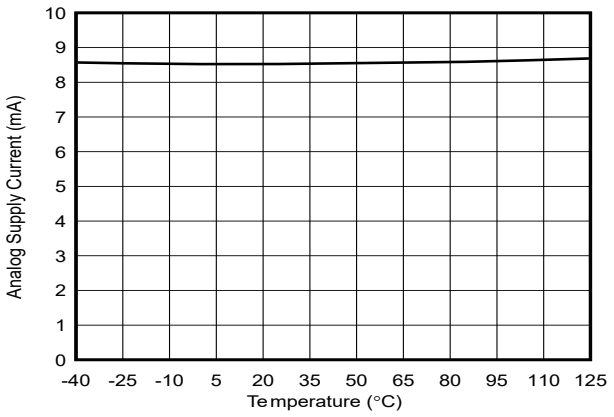
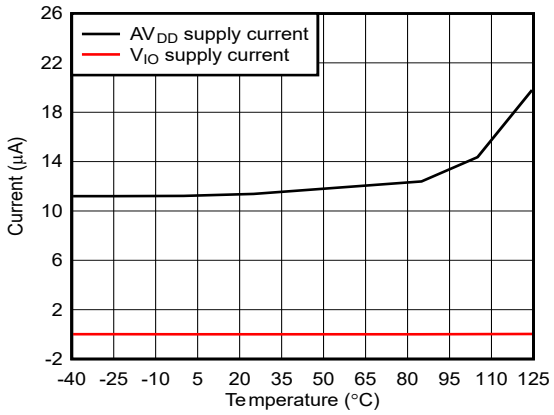
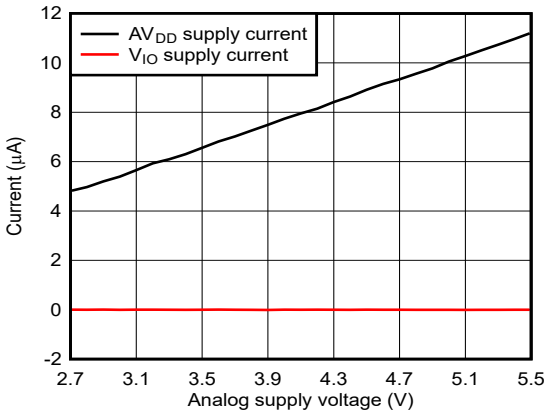


図 5-22. Supply Current With Internal Reference vs Temperature



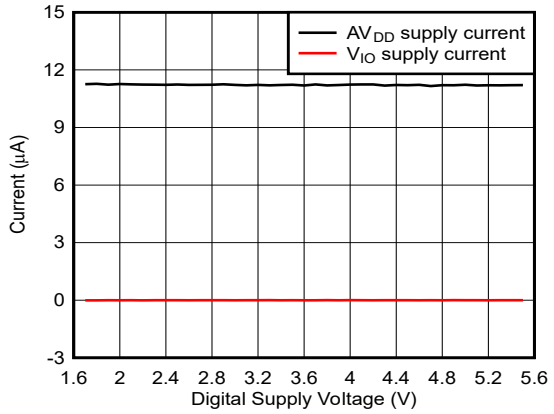
Gain = 1

図 5-23. Power-Down Current vs Temperature



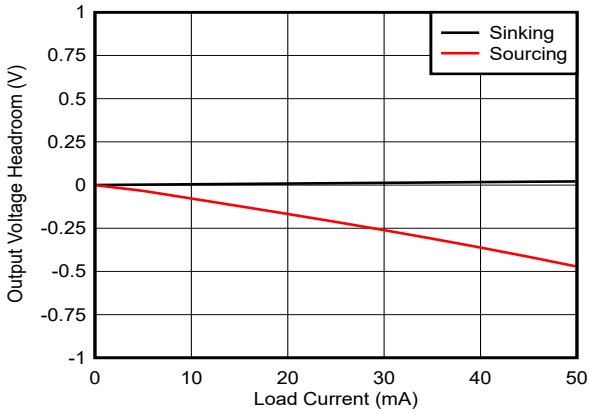
Gain = 1

図 5-24. Power-Down Current vs Supply Voltage



Gain = 1

図 5-25. Power-Down Current vs V_{IO}

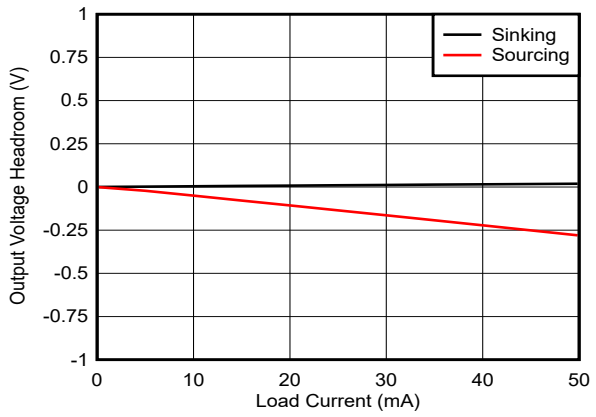


Gain = 1, AV_{DD} = 2.7V, measured DAC at full-scale

図 5-26. Headroom vs Load Current

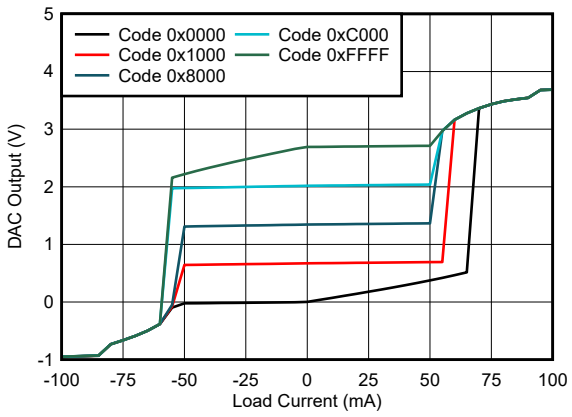
5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)



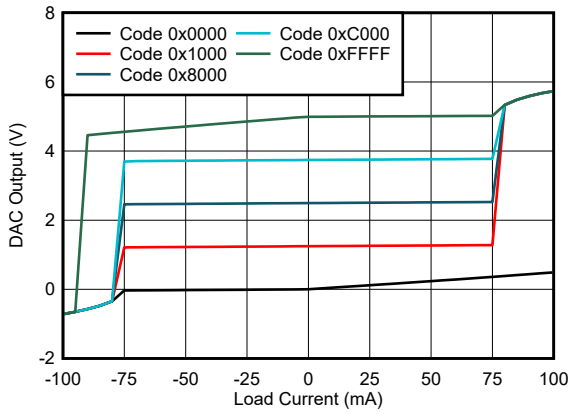
Gain = 2, AV_{DD} = 5V, measured DAC at full-scale

図 5-27. Headroom vs Load Current



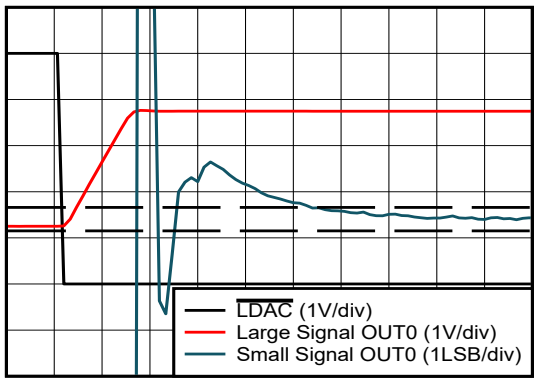
Gain = 1

図 5-28. Source and Sink Capability



Gain = 2

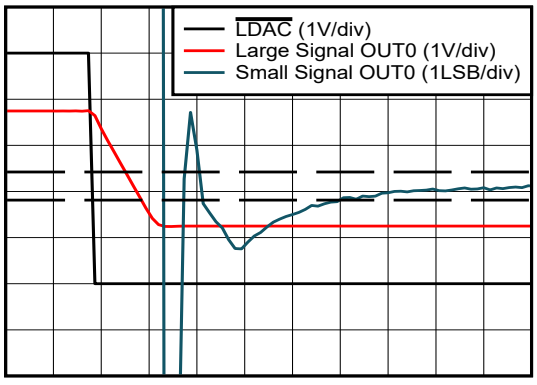
図 5-29. Source and Sink Capability



Time (1µs/div)

Dashed lines represent settling interval

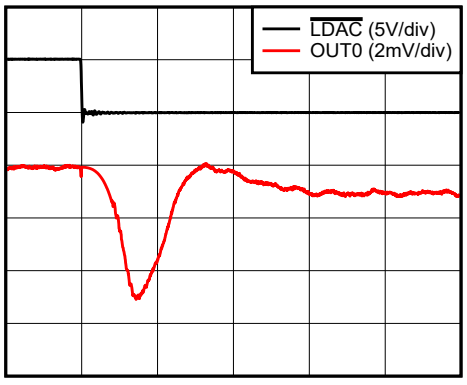
図 5-30. Full-Scale Settling Time, Rising Edge



Time (1µs/div)

Dashed lines represent settling interval

図 5-31. Full-Scale Settling Time, Falling Edge



Time (250ns/div)

1LSB step

図 5-32. Glitch Impulse, Falling Edge

5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)

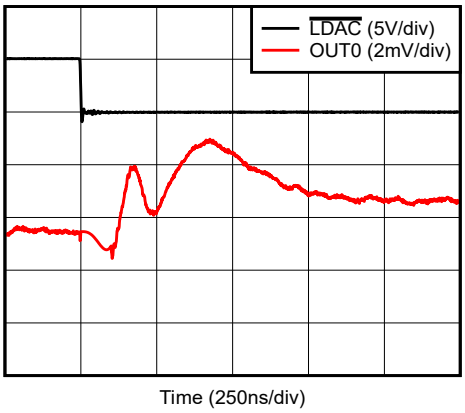


図 5-33. Glitch Impulse, Rising Edge

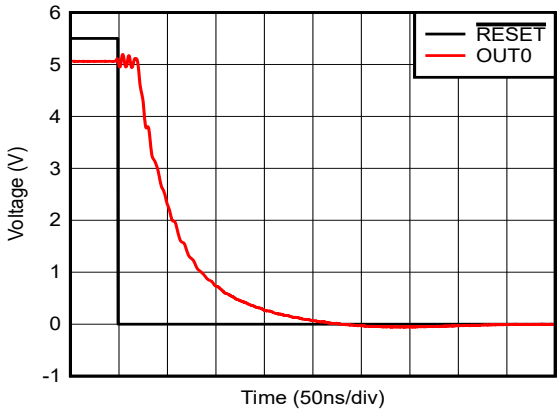


図 5-34. Power-On, Reset to Zero Scale

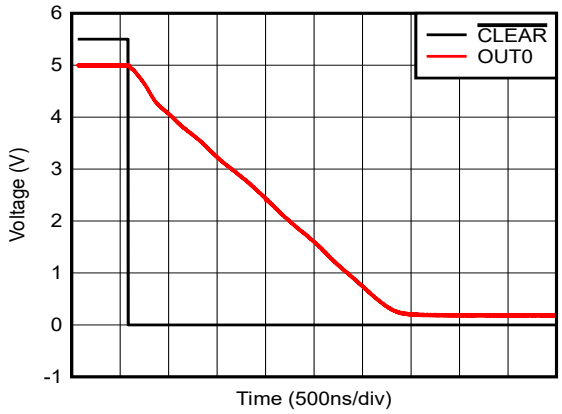


図 5-35. Clear to Zero Scale

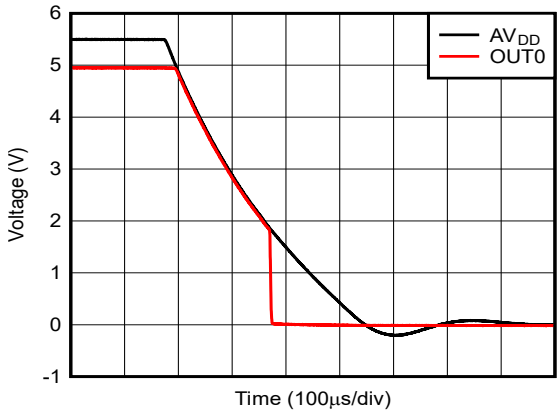


図 5-36. AV_{DD} Power Down Response

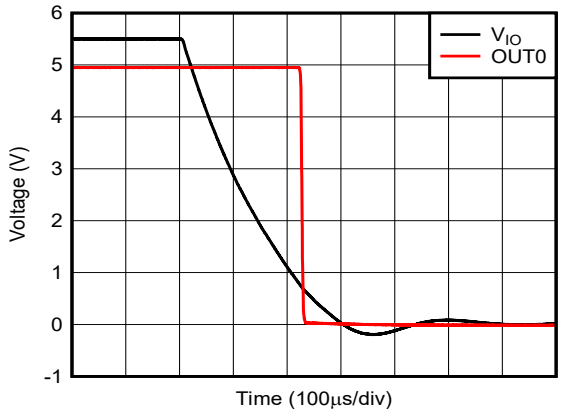


図 5-37. V_{IO} Power Down Response

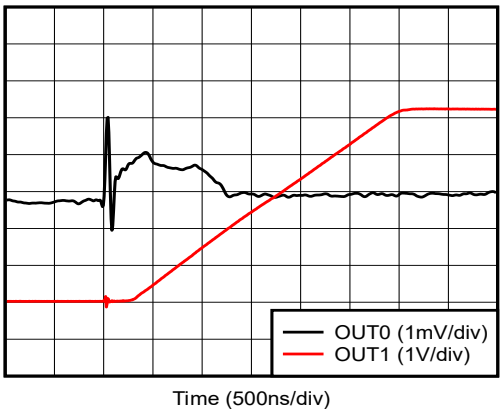
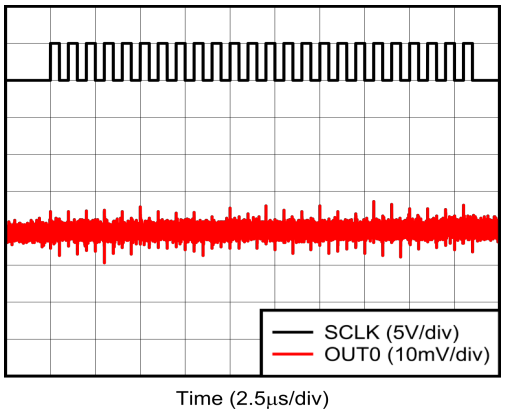


図 5-38. Channel-to-Channel DC Crosstalk

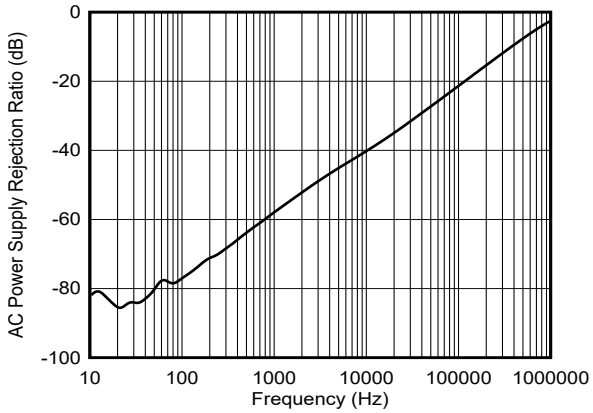
5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)



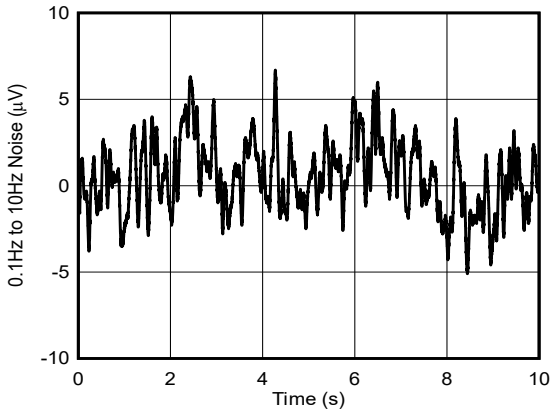
DAC code at midscale, SCLK = 1MHz

図 5-39. Clock Feedthrough



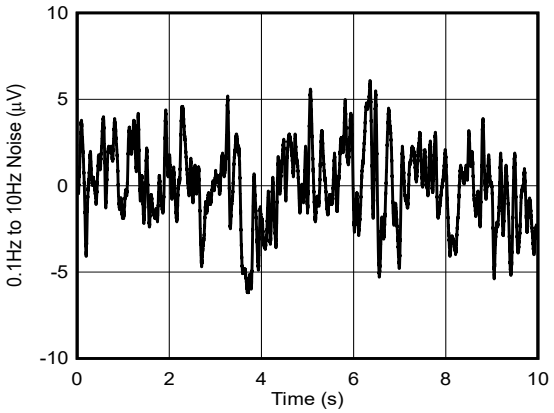
DAC code at full scale, V_{DD} = 5V + 200mV_{PP}

図 5-40. DAC Output AC PSRR vs Frequency



DAC code at midscale, gain = 2, external reference = 2.5V

図 5-41. DAC Output Noise With External Reference 0.1Hz to 10Hz



DAC code at midscale

図 5-42. DAC Output Noise With Internal Reference 0.1Hz to 10Hz

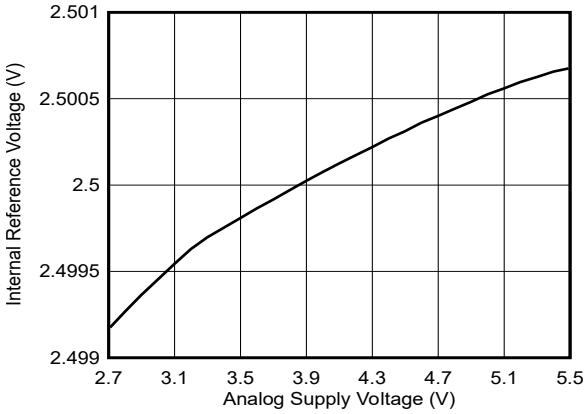


図 5-43. Internal Reference Voltage vs Supply Voltage

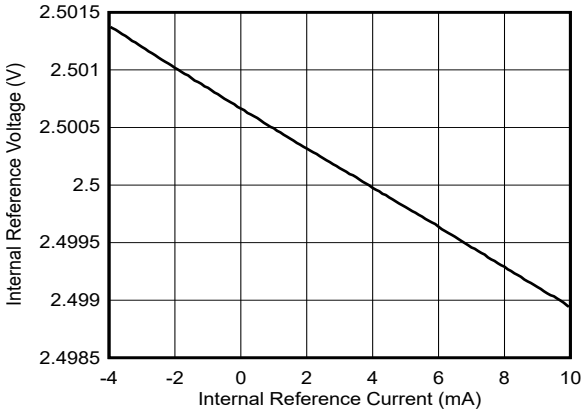


図 5-44. Internal Reference Voltage vs Internal Reference Current

5.12 Typical Characteristics (continued)

at T_J = 25°C, AV_{DD} = 5.5V, V_{IO} = 5.5V, internal reference = 2.5V, gain = 2, DAC outputs unloaded (unless otherwise noted)

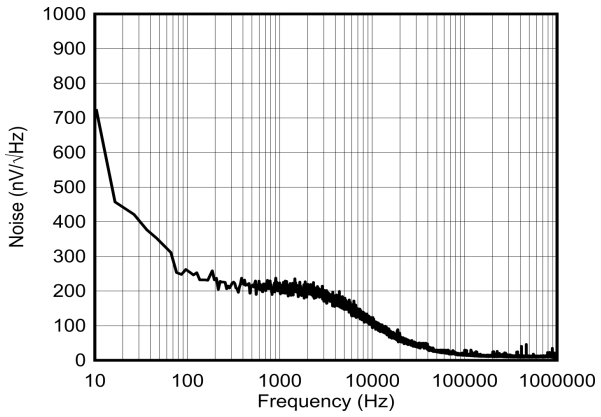


図 5-45. Internal Reference Noise Density vs Frequency

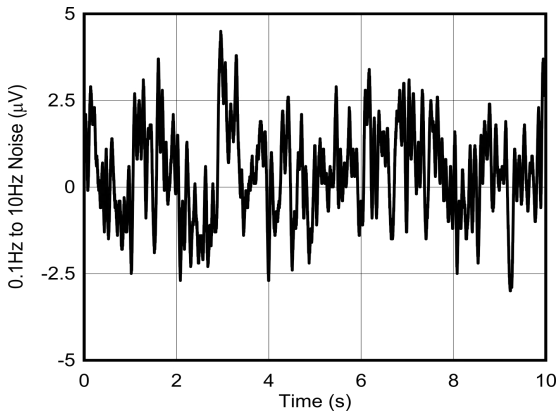


図 5-46. Internal Reference Noise

6 Detailed Description

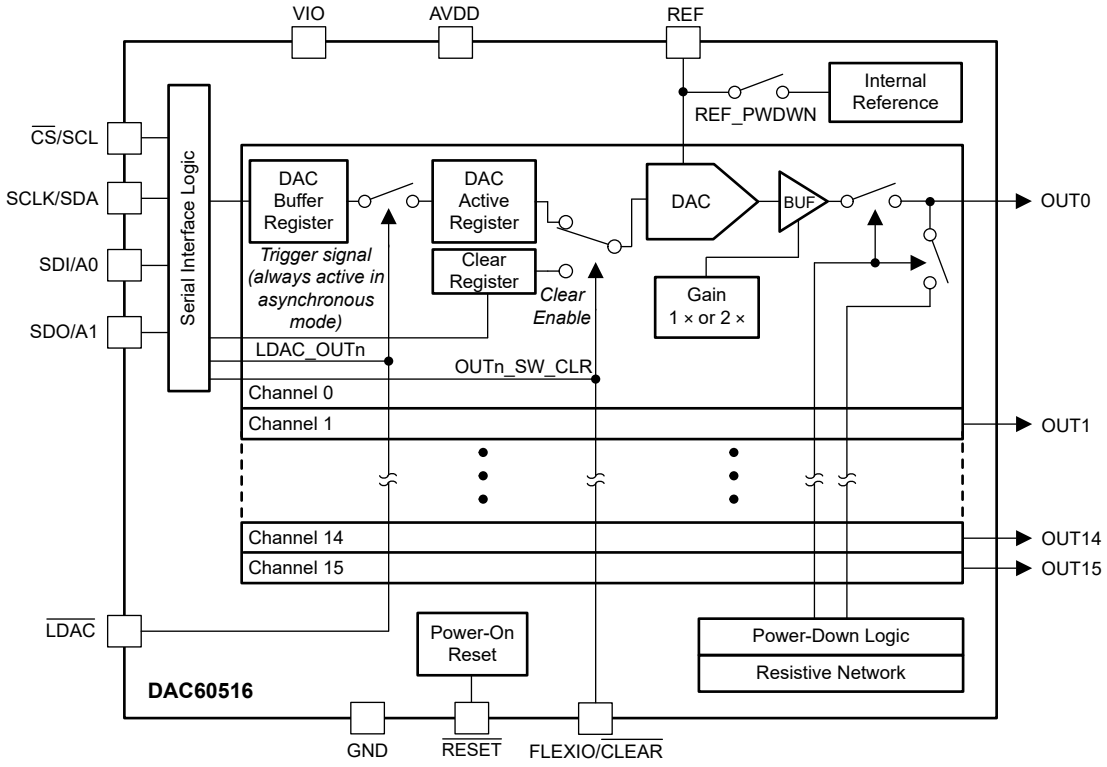
6.1 Overview

The DAC60516 is a low-power, sixteen-channel, buffered voltage-output digital-to-analog converter (DAC) with 12-bit resolution. The DAC60516 includes a 2.5V internal reference and provides user-selectable gain configuration through software, which can be used to set the full-scale output voltage range for groups of four DACs at a time (see also セクション 6.3.1.1). The device operates from a single 2.7V to 5.5V supply. Communication to the DAC60516 is performed through a serial interface that supports SPI and I^2C communication.

The DAC60516 incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at zero scale until a valid code is written to the device.

A clear pin enables a simultaneous update of multiple DAC channels to specified clear values.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DAC60516 consists of an R-2R ladder architecture followed by an output buffer amplifier. 図 6-1 shows a block diagram of the DAC architecture.

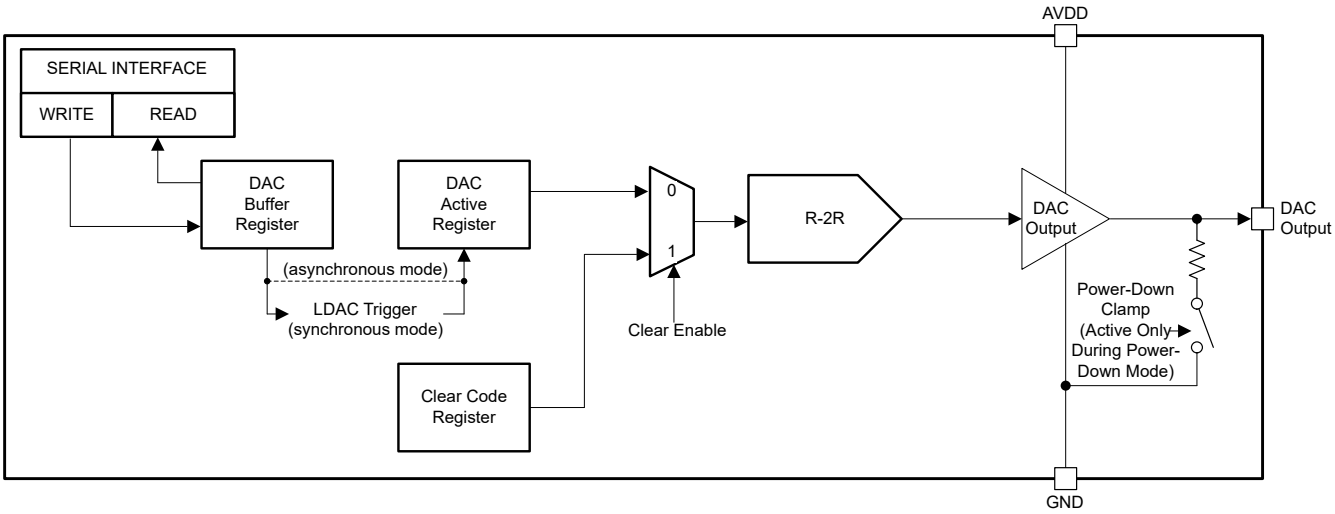


図 6-1. DAC60516 DAC Block Diagram

After a reset event, all the DAC registers are set to code 0x0000, the DAC output amplifiers are powered down, and the DAC outputs are clamped to GND. Each DAC output can be independently enabled or disabled through software by writing to the appropriate bit of the PWDWN register. When disabled, the DAC output is clamped to ground via a pull-down resistor.

6.3.1.1 DAC Register Structure

The DAC produces output voltages proportional to a 12-bit input data code. Input data are written to the DAC data register in straight binary format for all output ranges. By writing to the DAC_GAIN register, the user can configure the maximum full-scale DAC output voltage as either 1 × V_{REF} or 2 × V_{REF} (maximum of 5V), where V_{REF} is the internal or external reference input voltage. セクション 7.1.5 shows that the gain settings can be configured for QUAD0 (OUT0 through OUT3), QUAD1 (OUT4 through OUT7), QUAD2 (OUT8 through OUT11) and QUAD3 (OUT12 through OUT15); all DAC channels in a QUAD group share the same gain settings.

Data written to the DAC data registers are initially stored in the DAC buffer registers. The transfer of data from the DAC buffer registers to the DAC active registers can be configured to happen immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). When the DAC active registers are updated, the DAC output channels change to the new values.

By setting the corresponding BCAST_EN bits in the DAC_BCAST_EN register, each DAC can be configured to operate in broadcast mode. When a value is written to the BCAST_DAC_DATA register, this value is automatically stored in the buffer and active data registers of all DACs operating in broadcast mode.

Additionally, each DAC has a short circuit detection circuit. The DAC_STATUS register indicates which DAC channels are presently in short-circuit condition. A global status bit (GDAC_SC_STS, in the STATUS register) is the logical OR of all the DAC_STATUS bits, which can be used to determine if there is at least one channel in the short circuit condition.

6.3.1.1.1 DAC Synchronous Operation

The update mode for each DAC channel is determined by the DAC synchronous setting, configured for each DAC by writing to the SYNC_EN register. In asynchronous mode, a write to the DAC buffer data register results in an immediate update of the DAC active registers on a $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC buffer data register does not automatically update the DAC active register. Instead, the update occurs only after a DAC trigger signal is generated. A DAC trigger signal can be generated by pulling the $\overline{LDAC}$ pin low, which updates the active registers of all DAC output channels operating in synchronous mode simultaneously. The $\overline{LDAC}$ pin does not affect the active registers of channels already configured as asynchronous in the SYNC_EN register; however all other channels (configured as synchronous in the SYNC_EN register) operate in asynchronous mode as long as the $\overline{LDAC}$ pin is held at logic low. A DAC trigger can also be generated through software, by writing to the appropriate LDAC_OUTn bit in the TRIGGER register. A software trigger updates the active registers of two DAC channels at a time; each bit in the TRIGGER register corresponds to a pair of output channels, and setting a bit to 1 updates both corresponding channels simultaneously.

6.3.1.1.2 DAC Buffer Amplifier

The DAC output buffer amplifiers are capable of rail-to-rail operation, featuring low noise and low drift voltage output. The amplifier outputs are available at the DAC output pins. The maximum DAC output voltage range is limited by the AV_{DD} supply.

The high output current of the device provides good slewing characteristics even with large capacitive loads. To estimate the positive and negative slew rates for large capacitive loads, divide the source and sink short-circuit current value by the capacitor.

6.3.1.1.3 DAC Transfer Function

The DAC transfer function is given by 式 1.

$$V_{DAC} = \left(\frac{DACIN}{2^{12}}\right) \times FSR \quad (1)$$

where

- DACIN = decimal equivalent of the binary code loaded to the DAC register. DACIN range = 0 to $2^{12} – 1$.
- FSR = DAC full-scale output for the selected output range. FSR is 2.5V for the 0V to 2.5V range, and 5V for the 0V to 5V range.

The DAC output spans the voltage ranges shown in 表 6-1.

表 6-1. DAC Data Format

DAC DATA REGISTER		DAC OUTPUT VOLTAGE (V)	
BINARY	HEX	0V TO 5V RANGE	0V TO 2.5V RANGE
0000 0000 0000	000	0	0
0000 0000 0001	001	0.00122	0.00061
1000 0000 0000	800	2.5	1.25
1111 1111 1110	FFE	4.99877	2.49938
1111 1111 1111	FFF	5	2.5

6.3.2 Internal Reference

The DAC60516 includes a 2.5V precision band-gap reference enabled by default. Operation from an external reference is supported by disabling the internal reference, by writing to the REF_PWDWN bit in the GEN_CONFIG register. The internal reference is externally available at the REF pin.

A minimum 150nF capacitor is recommended between the reference output and GND for noise filtering.

6.3.3 Power-On Reset (POR)

The DAC60516 provides a power-on reset (POR) function. After start-up, when the AV_{DD} and V_{IO} supplies have been established, a POR is issued to so that the device initializes correctly (see also セクション 8.3). The DAC60516 requires 5ms to 10ms to initialize the serial interface after a POR; therefore, wait at least 10ms after start-up to communicate with the device.

During operation, the following three conditions can trigger a reset:

1. AV_{DD} or V_{IO} decrease to less than the recommended minimum operating value (by at least 200mV)
2. A value of 0xA (hexadecimal) is written to the SOFT_RST field in the TRIGGER register
3. The $\overline{\text{RESET}}$ pin of the device is pulled to logic 0, for at least 20ns. As long as the pin is held at logic 0, the device remains in a powered-down state until the pin is set to logic 1 (at which time, the device performs initialization of the serial interface again).

6.4 Device Functional Modes

6.4.1 Clear Mode

Each DAC can be set to enter a clear state using either hardware or software. When a DAC enters the clear state, the DAC is loaded with the data stored in the corresponding CLEAR_CODE register (code 0 by default) and the output is set to the corresponding voltage level.

The DAC buffer and active registers do not change when the DACs enter the clear state, which enables the DAC to return to the operating point prior to the clear event. The DAC buffer and active registers can also be updated while the DAC is in clear state, thus allowing the DAC to output a new value upon return to normal operation. When the DAC exits the clear state, the DAC is immediately loaded with the data in the active register, and the DAC output channel is set back to the corresponding level to restore operation.

By writing to the appropriate bits in the CLEAR register, each DAC can be programmed to enter or exit the clear state. Each DAC can also be forced to enter a clear state through the FLEXIO pin, when configured as an active-low $\overline{\text{CLEAR}}$ pin. This configuration is done by setting the FLEXIO_FUNC bit in the GEN_CONFIG register (by default, this bit is 0, and FLEXIO acts as a general purpose input-output pin). By default, each DAC output is automatically cleared when the $\overline{\text{CLEAR}}$ pin is asserted to a logic-low level, unless the appropriate bit in the CLEAR_PIN_MASK register is set. After the DAC leaves the clear state, the DAC is reloaded with the contents of the active register and the DAC output channel updates accordingly.

The device also allows user to set a common clear code for each DAC, which can be done by writing to the BCAST_CLR_DATA register. The value stored in this register is written to the CLEAR_CODE registers of all DACs operating in broadcast mode (determined by the appropriate bit setting in the BCAST_EN register), which can be used to clear multiple DACs channels to the same code simultaneously.

If a DAC channel is in a power-down state for any reason, any clear commands are ignored on the DAC until the channel exits the power-down state.

6.5 Programming

The device communicates with the system controller through a serial interface, which supports either an I^{2}C-compatible two-wire bus, or an SPI-compatible bus. The device includes a robust mechanism that detects between an SPI-compatible or I^{2}C-compatible controller, and automatically configures the interface accordingly. The interface detection mechanism operates at start-up, thus preventing protocol change during normal operation.

The register map addresses range from 0x00 to 0x32, enabling access of bits within each respective register (see セクション 7 for additional details).

6.5.1 I^{2}C Serial Interface

In I^{2}C mode, the device operates only as a target device on the two-wire bus. Connections to either bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast mode as well as fast mode plus. All data bytes are transmitted MSB first.

6.5.1.1 I^{2}C Bus Overview

The device is I^{2}C compatible. In I^{2}C protocol, the device that initiates the transfer is called a *controller*, and a device controlled by the controller is called a *target*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. A START condition is indicated by pulling the data line (SDA) from a high-to-low logic level while SCL is high. All targets on the bus receive the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a control signal.

After all data have been transferred, the controller generates a STOP condition. A STOP condition is indicated by pulling SDA from low to high, while SCL is high.

6.5.1.2 I²C Bus Definitions

The device is I²C-compatible and the bus definitions are listed in 表 6-2.

表 6-2. I²C Symbol Set

CONDITION	SYMBOL	SOURCE	DESCRIPTION
START	S	Controller	Begins all bus transactions. A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer initiates with a START condition
STOP	P	Controller	Terminates all transactions and resets bus. A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition.
IDLE	I	Controller	Bus idle. Both SDA and SCL lines remain high.
ACK (Acknowledge)	A	Controller/Target	Handshaking bit (low). Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Take setup and hold times into account.
NACK (Not Acknowledge)	$\overline{A}$	Controller/Target	Handshaking bit (high). On a controller receive, data transfer termination can be signaled by the controller generating a not-acknowledge on the last byte that has been transmitted by the target.
READ	R	Controller	Active-high bit that follows immediately after the target address sequence. Indicates that the controller is initiating the target-to-controller data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
WRITE	$\overline{W}$	Controller	Active-low bit that follows immediately after the target address sequence. Indicates that the controller is initiating the controller-to-target data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
REPEATED START	Sr	Controller	Generated by controller, same function as the START condition (highlights the fact that STOP condition is not strictly necessary.)
BLOCK ACCESS	B	Controller	Active-high bit that indicates the controller is initiating a block access data transfer.

6.5.1.3 I²C Target Address Selection

The I²C bus target address is selected by installing shunts from the A0 and A1 pins to the V_{IO} or GND rails. The state of the A0 and A1 pins is tested after every occurrence of START condition on the I²C bus. The device discerns between two possible options for each pin, shunt to V_{IO} (logic 1) and shunt to GND (logic 0), for a total of four possible target addresses, as shown in 表 6-3.

表 6-3. I²C Target Address Space

DEVICE PINS		I²C TARGET ADDRESS
A1	A0	[A6:A0]
0	0	101 0000
0	1	101 0001
1	0	101 0100
1	1	101 0101

6.5.1.4 I²C Read and Write Operations

When writing to the device, the value for the address register is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the address register, as shown in 図 6-2.

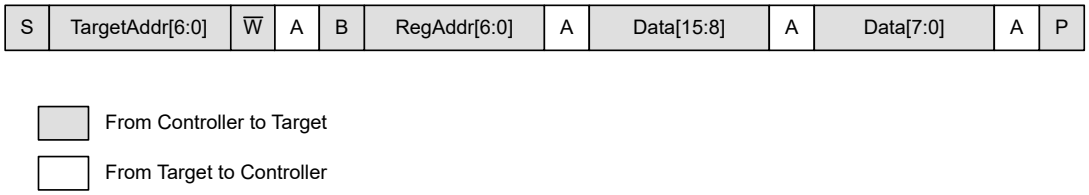


図 6-2. I²C Write Access Protocol

When reading from the device, the last value stored in the address register by a write operation is used to determine which register is read by a read operation. To change which register is read for a read operation, a new value must be written to the address register. This transaction is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the address register byte; no additional data are required. The controller can then generate a START condition and send the target address byte with the R/$\overline{W}$ bit high to initiate the read command.

If repeated reads from the same register are desired, there is no need to continually send the address register bytes because the device retains the address register value until the value is changed by the next write operation. The register bytes are big endian and left justified.

Terminate read operations by issuing a *not-acknowledge* command at the end of the last byte to be read. The controller must leave the SDA line high during the acknowledge time of the last byte that is read from the target, as shown in 図 6-3.

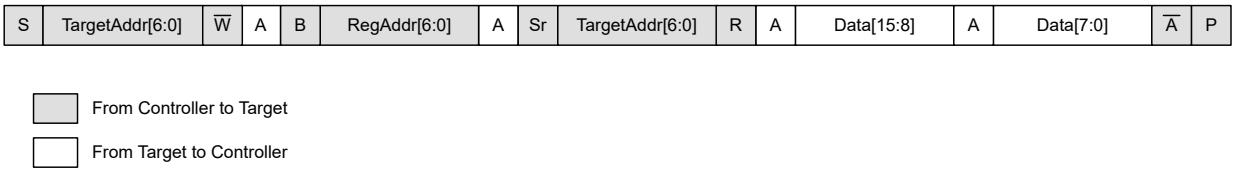


図 6-3. I²C Read Access Protocol

Block access functionality is provided to minimize the transfer overhead of large data sets. Block access enables multibyte transfers and is configured by setting the block access bit high. Until the transaction is terminated by the STOP condition, the device reads and writes the subsequent memory locations, as shown in 図 6-4 and 図 6-5. If the controller reaches address 0x7F in a page, the device continues reading and writing from this address until the transaction is terminated.

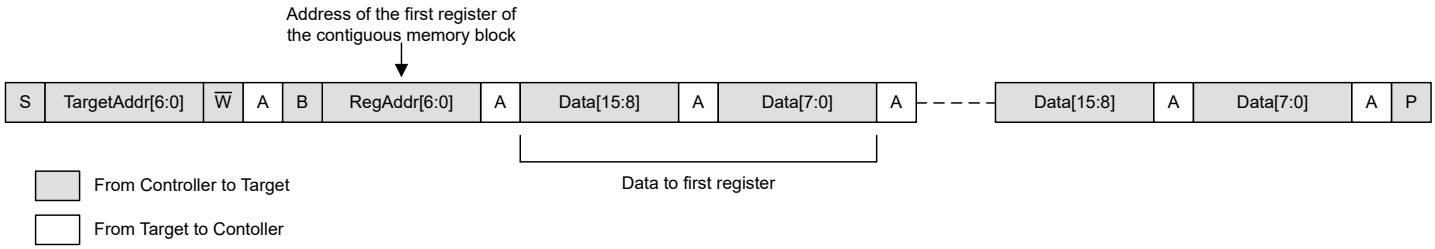


図 6-4. I²C Block Write Access

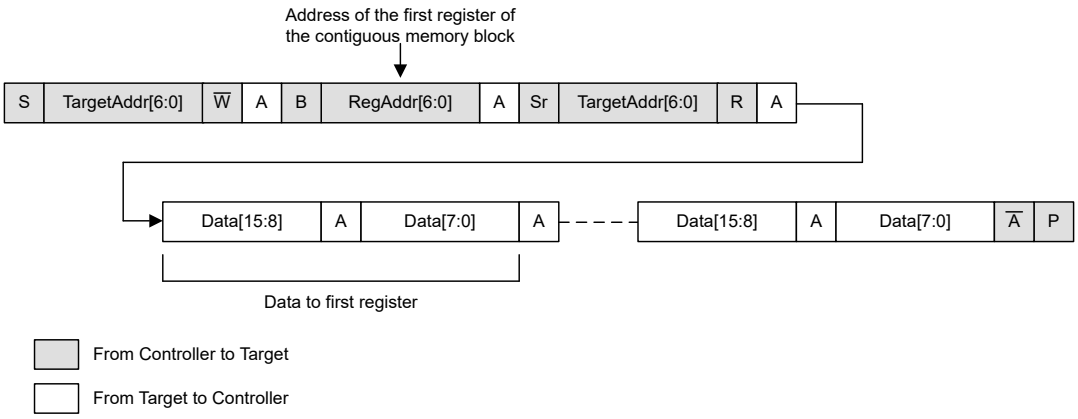


図 6-5. I²C Block Read Access

6.5.1.5 I²C General-Call Reset

The device supports reset using the two-wire general call address 00h (0000 0000b). The device acknowledges the general-call address, and responds to the second byte. If the second byte is 06h (0000 0110b), the device executes a software reset. This software reset initiates a reset event. The device takes no action in response to other values in the second byte.

6.5.2 Serial Peripheral Interface (SPI)

In SPI mode, the device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the device registers.

6.5.2.1 SPI Bus Overview

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long, thus the $\overline{CS}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the last 24 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

In a serial interface access cycle, the first byte input to SDI is the instruction cycle that identifies the request as a read or write command, and the 7-bit address to be accessed. The following bits in the cycle form the data cycle, as shown in 表 6-4.

表 6-4. SPI Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the addressed register. RW = 0 sets a write operation. RW = 1 sets a read operation.
22:16	A[6:0]	Register address. Specifies the register to be accessed during the read or write operation.
15:0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO_EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data, formatted as shown in 表 6-5. Data are clocked out on the SDO pin on SCLK rising or falling edges, according to the FSDO bit setting.

表 6-5. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW bit from previous access cycle.
22:16	STATUS[6:0]	Lower seven bits of the STATUS register.
15:0	DO[15:0]	Readback data requested on previous access cycle.

7 Register Map

表 7-1. Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	NOP	W	0000	NOP[15:0]															
01	DEVICE_ID	R	6516	CHIP_ID[15:0]															
02	VERSION_ID	R	0000	RESERVED													VERSION_ID[2:0]		
03	PWDWN	R/W	FFFF	OUT15_PWDWN	OUT14_PWDWN	OUT13_PWDWN	OUT12_PWDWN	OUT11_PWDWN	OUT10_PWDWN	OUT9_PWDWN	OUT8_PWDWN	OUT7_PWDWN	OUT6_PWDWN	OUT5_PWDWN	OUT4_PWDWN	OUT3_PWDWN	OUT2_PWDWN	OUT1_PWDWN	OUT0_PWDWN
04	DAC_GAIN	R/W	0000	RESERVED												OUT_QUAD3_GAIN	OUT_QUAD2_GAIN	OUT_QUAD1_GAIN	OUT_QUAD0_GAIN
05	TRIGGER	W	0000	LDAC_OUT15_OUT14	LDAC_OUT13_OUT12	LDAC_OUT11_OUT10	LDAC_OUT9_OUT8	LDAC_OUT7_OUT6	LDAC_OUT5_OUT4	LDAC_OUT3_OUT2	LDAC_OUT1_OUT0	RESERVED				SOFT_RST[3:0]			
06	BCAST_DAC_DATA	R/W	0000	DATA[11:0]												RESERVED			
07	STATUS	R	4008	RESERVED															GDAC_SC_STS
08	SDO_EN	R/W	0000	RESERVED														FSDO	SDO_EN
09	GEN_CONFIG	R/W	0014	RESERVED										FLEXIO_OUT_POL	FLEXIO_OUT_ODE	RESERVED	REF_PWDWN	RESERVED	FLEXIO_FUNC
0A	SYNC_EN	R/W	0000	OUT15_SYNC_EN	OUT14_SYNC_EN	OUT13_SYNC_EN	OUT12_SYNC_EN	OUT11_SYNC_EN	OUT10_SYNC_EN	OUT9_SYNC_EN	OUT8_SYNC_EN	OUT7_SYNC_EN	OUT6_SYNC_EN	OUT5_SYNC_EN	OUT4_SYNC_EN	OUT3_SYNC_EN	OUT2_SYNC_EN	OUT1_SYNC_EN	OUT0_SYNC_EN
0B	BCAST_EN	R/W	FFFF	OUT15_BCAST_EN	OUT14_BCAST_EN	OUT13_BCAST_EN	OUT12_BCAST_EN	OUT11_BCAST_EN	OUT10_BCAST_EN	OUT9_BCAST_EN	OUT8_BCAST_EN	OUT7_BCAST_EN	OUT6_BCAST_EN	OUT5_BCAST_EN	OUT4_BCAST_EN	OUT3_BCAST_EN	OUT2_BCAST_EN	OUT1_BCAST_EN	OUT0_BCAST_EN
0C	CLEAR	R/W	0000	OUT15_SW_CLR	OUT14_SW_CLR	OUT13_SW_CLR	OUT12_SW_CLR	OUT11_SW_CLR	OUT10_SW_CLR	OUT9_SW_CLR	OUT8_SW_CLR	OUT7_SW_CLR	OUT6_SW_CLR	OUT5_SW_CLR	OUT4_SW_CLR	OUT3_SW_CLR	OUT2_SW_CLR	OUT1_SW_CLR	OUT0_SW_CLR
0D	CLEAR_PIN_MASK	R/W	0000	OUT15_HW_CLR_MASK	OUT14_HW_CLR_MASK	OUT13_HW_CLR_MASK	OUT12_HW_CLR_MASK	OUT11_HW_CLR_MASK	OUT10_HW_CLR_MASK	OUT9_HW_CLR_MASK	OUT8_HW_CLR_MASK	OUT7_HW_CLR_MASK	OUT6_HW_CLR_MASK	OUT5_HW_CLR_MASK	OUT4_HW_CLR_MASK	OUT3_HW_CLR_MASK	OUT2_HW_CLR_MASK	OUT1_HW_CLR_MASK	OUT0_HW_CLR_MASK
0E	BCAST_CLR_DATA	R/W	0000	DATA[11:0]												RESERVED			
0F	RESET_FLAGS	W	000F	RESERVED												AVDD_COLLAPSE_FLAG	RSTPIN_FLAG	VIO_FLAG	PORBASE_FLAG
10	OUT0_BUFFER_CODE	R/W	0000	DATA[11:0]												RESERVED			
11	OUT1_BUFFER_CODE	R/W	0000	DATA[11:0]												RESERVED			

表 7-1. Register Map (続き)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12	OUT2_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
13	OUT3_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
14	OUT4_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
15	OUT5_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
16	OUT6_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
17	OUT7_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
18	OUT8_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
19	OUT9_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1A	OUT10_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1B	OUT11_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1C	OUT12_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1D	OUT13_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1E	OUT14_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
1F	OUT15_ BUFFER_ CODE	R/W	0000	DATA[11:0]												RESERVED			
20	OUT0_ CLEAR_ CODE	R/W	0000	DATA[11:0]												RESERVED			
21	OUT1_ CLEAR_ CODE	R/W	0000	DATA[11:0]												RESERVED			

表 7-1. Register Map (続き)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22	OUT2_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
23	OUT3_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
24	OUT4_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
25	OUT5_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
26	OUT6_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
27	OUT7_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
28	OUT8_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
29	OUT9_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2A	OUT10_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2B	OUT11_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2C	OUT12_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2D	OUT13_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2E	OUT14_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
2F	OUT15_CLEAR_CODE	R/W	0000	DATA[11:0]												RESERVED			
31	GPIO_DATA	R/W	0001	RESERVED															GPIO
32	DAC_STATUS	R	0000	OUT15_SC_STS	OUT14_SC_STS	OUT13_SC_STS	OUT12_SC_STS	OUT11_SC_STS	OUT10_SC_STS	OUT9_SC_STS	OUT8_SC_STS	OUT7_SC_STS	OUT6_SC_STS	OUT5_SC_STS	OUT4_SC_STS	OUT3_SC_STS	OUT2_SC_STS	OUT1_SC_STS	OUT0_SC_STS

7.1 DAC60516 Registers

7.1.1 NOP Register (Offset = 0h) [Reset = 0000h]

図 7-1. NOP Register

15	14	13	12	11	10	9	8
NOP[15:0]							
W-0h							
7	6	5	4	3	2	1	0
NOP[15:0]							
W-0h							

表 7-2. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NOP[15:0]	W	0h	No Operation (NOP).

7.1.2 DEVICE_ID Register (Offset = 1h) [Reset = 6516h]

図 7-2. DEVICE_ID Register

15	14	13	12	11	10	9	8
CHIP_ID[15:0]							
R-65h							
7	6	5	4	3	2	1	0
CHIP_ID[15:0]							
R-16h							

表 7-3. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CHIP_ID[15:0]	R	6516h	Device Chip ID. Device Chip ID loaded from OTP.

7.1.3 VERSION_ID Register (Offset = 2h) [Reset = 0000h]

図 7-3. VERSION_ID Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					VERSION_ID[2:0]		
R-0h					R-0h		

表 7-4. VERSION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0h	
2:0	VERSION_ID[2:0]	R	0h	Device Version ID. Device Version ID loaded from OTP.

7.1.4 PWDWN Register (Offset = 3h) [Reset = FFFFh]

図 7-4. PWDWN Register

15	14	13	12	11	10	9	8
OUT15_PWDWN	OUT14_PWDWN	OUT13_PWDWN	OUT12_PWDWN	OUT11_PWDWN	OUT10_PWDWN	OUT9_PWDWN	OUT8_PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
OUT7_PWDWN	OUT6_PWDWN	OUT5_PWDWN	OUT4_PWDWN	OUT3_PWDWN	OUT2_PWDWN	OUT1_PWDWN	OUT0_PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 7-5. PWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_PWDWN	R/W	1h	OUT15 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
14	OUT14_PWDWN	R/W	1h	OUT14 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
13	OUT13_PWDWN	R/W	1h	OUT13 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
12	OUT12_PWDWN	R/W	1h	OUT12 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
11	OUT11_PWDWN	R/W	1h	OUT11 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
10	OUT10_PWDWN	R/W	1h	OUT10 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
9	OUT9_PWDWN	R/W	1h	OUT9 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
8	OUT8_PWDWN	R/W	1h	OUT8 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
7	OUT7_PWDWN	R/W	1h	OUT7 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
6	OUT6_PWDWN	R/W	1h	OUT6 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
5	OUT5_PWDWN	R/W	1h	OUT5 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
4	OUT4_PWDWN	R/W	1h	OUT4 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
3	OUT3_PWDWN	R/W	1h	OUT3 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
2	OUT2_PWDWN	R/W	1h	OUT2 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
1	OUT1_PWDWN	R/W	1h	OUT1 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode
0	OUT0_PWDWN	R/W	1h	OUT0 power down bit. 0h = This DAC is enabled 1h = This DAC is disabled in a low-power mode

7.1.5 DAC_GAIN Register (Offset = 4h) [Reset = 0000h]

図 7-5. DAC_GAIN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				OUT_QUAD3_GAIN	OUT_QUAD2_GAIN	OUT_QUAD1_GAIN	OUT_QUAD0_GAIN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-6. DAC_GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R	0h	
3	OUT_QUAD3_GAIN	R/W	0h	QUAD-3 V_{REF} Gain. V_{REF} gain setting for OUT12, OUT13, OUT14, OUT15. 0h = This group of DACs is in 0V – 1 × V_{REF} output range 1h = This group of DACs is in 0V – 2 × V_{REF} output range
2	OUT_QUAD2_GAIN	R/W	0h	QUAD-2 V_{REF} Gain. V_{REF} gain setting for OUT8, OUT9, OUT10, OUT11. 0h = This group of DACs is in 0V – 1 × V_{REF} output range 1h = This group of DACs is in 0V – 2 × V_{REF} output range
1	OUT_QUAD1_GAIN	R/W	0h	QUAD-1 V_{REF} Gain. V_{REF} gain setting for OUT4, OUT5, OUT6, OUT7. 0h = This group of DACs is in 0V – 1 × V_{REF} output range 1h = This group of DACs is in 0V – 2 × V_{REF} output range
0	OUT_QUAD0_GAIN	R/W	0h	QUAD-0 V_{REF} Gain. V_{REF} gain setting for OUT0, OUT1, OUT2, OUT3. 0h = This group of DACs is in 0V – 1 × V_{REF} output range 1h = This group of DACs is in 0V – 2 × V_{REF} output range

7.1.6 TRIGGER Register (Offset = 5h) [Reset = 0000h]

図 7-6. TRIGGER Register

15	14	13	12	11	10	9	8
LDAC_ OUT15_OUT14	LDAC_ OUT13_OUT12	LDAC_ OUT11_OUT10	LDAC_ OUT9_OUT8	LDAC_ OUT7_OUT6	LDAC_ OUT5_OUT4	LDAC_ OUT3_OUT2	LDAC_ OUT1_OUT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RESERVED				SOFT_RST[3:0]			
R-0h				W-0h			

表 7-7. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LDAC_OUT15_OUT14	W	0h	Software DAC trigger. Transfers DAC data from OUT15 and OUT14 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
14	LDAC_OUT13_OUT12	W	0h	Software DAC trigger. Transfers DAC data from OUT13 and OUT12 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
13	LDAC_OUT11_OUT10	W	0h	Software DAC trigger. Transfers DAC data from OUT11 and OUT10 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
12	LDAC_OUT9_OUT8	W	0h	Software DAC trigger. Transfers DAC data from OUT9 and OUT8 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
11	LDAC_OUT7_OUT6	W	0h	Software DAC trigger. Transfers DAC data from OUT7 and OUT6 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
10	LDAC_OUT5_OUT4	W	0h	Software DAC trigger. Transfers DAC data from OUT5 and OUT4 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
9	LDAC_OUT3_OUT2	W	0h	Software DAC trigger. Transfers DAC data from OUT3 and OUT2 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
8	LDAC_OUT1_OUT0	W	0h	Software DAC trigger. Transfers DAC data from OUT1 and OUT0 buffer registers to active registers, if corresponding channels are configured in synchronous mode. This bit self-clears when action is completed. 0h = No action 1h = Transfer DAC data. This bit clears when action is completed.
7:4	RESERVED	R	0h	
3:0	SOFT_RST[3:0]	W	0h	Software device reset. Ah = Software Reset. Executes a full power-on-reset. Resets the device and all registers to the default power-on-reset state. Auto clears with execution.

7.1.7 BCAST_DAC_DATA Register (Offset = 6h) [Reset = 0000h]

図 7-7. BCAST_DAC_DATA Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-8. BCAST_DAC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	A write to this register sets all DAC buffer and active register values to the specified code, on output channels for which the broadcast enable bit is set.
3:0	RESERVED	R	0h	

7.1.8 STATUS Register (Offset = 7h) [Reset = 4008h]

図 7-8. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-40h							
7	6	5	4	3	2	1	0
RESERVED							GDAC_SC_STS
R-04h							R-0h

表 7-9. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	R	2004h	
0	GDAC_SC_STS	R	0h	Global DAC short circuit status. Global DAC short circuit status bit. This bit is the OR function of all DACn_SC_STS bits. DACn_SC_STS bits are located in DAC_STATUS register having one bit per DAC. 0h = No DAC output channels are in a short-circuit condition 1h = At least one DAC output channel is in a short-circuit condition

7.1.9 SDO_EN Register (Offset = 8h) [Reset = 0000h]

図 7-9. SDO_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						FSDO	SDO_EN
R-0h						R/W-0h	R/W-0h

表 7-10. SDO_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0h	
1	FSDO	R/W	0h	Fast SDO. Allows faster SPI bus speeds by sending the SDO data out one SCLK half-cycle earlier. SDI latching edge is always SCLK falling edge regardless of this setting. FSDO is ignored when SDO_EN is disabled. 0h = SDO drives MSB when chip select goes low and then updates on each SCLK rising edge (opposite edge of SDI latching edge). 1h = SDO drives MSB when chip select goes low and then updates on each SCLK falling edge (same edge as SDI latching edge)
0	SDO_EN	R/W	0h	SDO enable. Enable the SDO pin driver. When enabled, SDO is enabled for read and writes whenever SPI chip-select pin is low. SDO is always disabled in I^2C mode regardless of this bit setting. 0h = SDO disabled 1h = SDO enabled during read and write operations

7.1.10 GEN_CONFIG Register (Offset = 9h) [Reset = 0014h]

図 7-10. GEN_CONFIG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		FLEXIO_OUT_POL	FLEXIO_OUT_ODE	RESERVED	REF_PWDWN	RESERVED	FLEXIO_FUNC
R-0h		R/W-0h	R/W-1h	R-0h	R/W-1h	R-0h	R/W-0h

表 7-11. GEN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R	0h	
5	FLEXIO_OUT_POL	R/W	0h	FLEXIO pin polarity. Set the FLEXIO pin output active state (when pin is configured as GPIO). 0h = FLEXIO digital pin outputs 0V if GPIO_DATA is set to 0x00h, and V_{IO} (or high-impedance, when configured as open-drain) if GPIO_DATA is set to 0x01h 1h = FLEXIO digital pin outputs V_{IO} (or high-impedance, when configured as open-drain) if GPIO_DATA is set to 0x00h, and 0V if GPIO_DATA is set to 0x01h
4	FLEXIO_OUT_ODE	R/W	1h	FLEXIO open drain enable. Set the FLEXIO pin drive mode (when pin is configured as GPIO). Do not raise pin above the absolute maximum ratings with respect to VIO voltage. Bit is ignored if pin is not configured as a digital output. 0h = FLEXIO pin output is push-pull 1h = FLEXIO pin output is open-drain
3	RESERVED	R	0h	
2	REF_PWDWN	R/W	1h	Disable internal reference. Set to enable or disable the internal voltage reference. 0h = Internal reference enabled 1h = Internal reference disabled
1	RESERVED	R	0h	
0	FLEXIO_FUNC	R/W	0h	FLEXIO pin function. Sets the function of FLEXIO pin. 0h = GPIO. In this mode, the pin operates as a GPIO and the GPIO_DATA register is used to support GPIO functionality. 1h = $\overline{\text{CLEAR}}$ pin. In this mode, the pin operates as an active-low DAC Clear input pin.

7.1.11 SYNC_EN Register (Offset = Ah) [Reset = 0000h]

図 7-11. SYNC_EN Register

15	14	13	12	11	10	9	8
OUT15_ SYNC_EN	OUT14_ SYNC_EN	OUT13_ SYNC_EN	OUT12_ SYNC_EN	OUT11_ SYNC_EN	OUT10_ SYNC_EN	OUT9_ SYNC_EN	OUT8_ SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
OUT7_ SYNC_EN	OUT6_ SYNC_EN	OUT5_ SYNC_EN	OUT4_ SYNC_EN	OUT3_ SYNC_EN	OUT2_ SYNC_EN	OUT1_ SYNC_EN	OUT0_ SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-12. SYNC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
14	OUT14_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
13	OUT13_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
12	OUT12_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
11	OUT11_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
10	OUT10_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
9	OUT9_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)

表 7-12. SYNC_EN Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
8	OUT8_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
7	OUT7_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
6	OUT6_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
5	OUT5_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
4	OUT4_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
3	OUT3_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
2	OUT2_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
1	OUT1_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)
0	OUT0_SYNC_EN	R/W	0h	Synchronous mode enable. Enable or disable synchronous mode. 0h = Set this DAC into asynchronous mode (DAC active register updates when DAC buffer is updated) 1h = Set this DAC into synchronous mode (DAC active register updates with DAC trigger)

7.1.12 BCAST_EN Register (Offset = Bh) [Reset = FFFFh]

図 7-12. BCAST_EN Register

15	14	13	12	11	10	9	8
OUT15_ BCAST_EN	OUT14_ BCAST_EN	OUT13_ BCAST_EN	OUT12_ BCAST_EN	OUT11_ BCAST_EN	OUT10_ BCAST_EN	OUT9_ BCAST_EN	OUT8_ BCAST_EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
OUT7_ BCAST_EN	OUT6_ BCAST_EN	OUT5_ BCAST_EN	OUT4_ BCAST_EN	OUT3_ BCAST_EN	OUT2_ BCAST_EN	OUT1_ BCAST_EN	OUT0_ BCAST_EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 7-13. BCAST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
14	OUT14_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
13	OUT13_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
12	OUT12_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
11	OUT11_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
10	OUT10_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
9	OUT9_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
8	OUT8_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
7	OUT7_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
6	OUT6_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
5	OUT5_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
4	OUT4_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
3	OUT3_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
2	OUT2_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
1	OUT1_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC
0	OUT0_BCAST_EN	R/W	1h	Enable or disable broadcast mode. 0h = Ignore broadcast writes on this DAC 1h = Allow broadcast writes on this DAC

7.1.13 CLEAR Register (Offset = Ch) [Reset = 0000h]

図 7-13. CLEAR Register

15	14	13	12	11	10	9	8
OUT15_SW_CLR	OUT14_SW_CLR	OUT13_SW_CLR	OUT12_SW_CLR	OUT11_SW_CLR	OUT10_SW_CLR	OUT9_SW_CLR	OUT8_SW_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
OUT7_SW_CLR	OUT6_SW_CLR	OUT5_SW_CLR	OUT4_SW_CLR	OUT3_SW_CLR	OUT2_SW_CLR	OUT1_SW_CLR	OUT0_SW_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-14. CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
14	OUT14_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
13	OUT13_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
12	OUT12_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
11	OUT11_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
10	OUT10_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
9	OUT9_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
8	OUT8_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
7	OUT7_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state

表 7-14. CLEAR Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	OUT6_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
5	OUT5_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
4	OUT4_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
3	OUT3_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
2	OUT2_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
1	OUT1_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state
0	OUT0_SW_CLR	R/W	0h	Software clear enable bit. Forces DAC to enter clear state. DAC uses clear code that is specified in clear state. 0h = Restore this DAC to normal operation 1h = Force this DAC into clear state

7.1.14 CLEAR_PIN_MASK Register (Offset = Dh) [Reset = 0000h]

図 7-14. CLEAR_PIN_MASK Register

15	14	13	12	11	10	9	8
OUT15_ HW_CLR_MASK	OUT14_ HW_CLR_MASK	OUT13_ HW_CLR_MASK	OUT12_ HW_CLR_MASK	OUT11_ HW_CLR_MASK	OUT10_ HW_CLR_MASK	OUT9_ HW_CLR_MASK	OUT8_ HW_CLR_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
OUT7_ HW_CLR_MASK	OUT6_ HW_CLR_MASK	OUT5_ HW_CLR_MASK	OUT4_ HW_CLR_MASK	OUT3_ HW_CLR_MASK	OUT2_ HW_CLR_MASK	OUT1_ HW_CLR_MASK	OUT0_ HW_CLR_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 7-15. CLEAR_PIN_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
14	OUT14_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
13	OUT13_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
12	OUT12_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
11	OUT11_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
10	OUT10_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
9	OUT9_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
8	OUT8_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
7	OUT7_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
6	OUT6_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
5	OUT5_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
4	OUT4_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
3	OUT3_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
2	OUT2_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
1	OUT1_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel
0	OUT0_HW_CLR_MASK	R/W	0h	Mask bit for $\overline{\text{CLEAR}}$ (FLEXIO) pin. 0h = $\overline{\text{CLEAR}}$ pin affects this DAC channel 1h = $\overline{\text{CLEAR}}$ pin does not affect this DAC channel

7.1.15 BCAST_CLR_DATA Register (Offset = Eh) [Reset = 0000h]

図 7-15. BCAST_CLR_DATA Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-16. BCAST_CLR_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	A write to this register sets all DAC clear code register values to the specified code on output channels for which the broadcast enable bit is set.
3:0	RESERVED	R	0h	

7.1.16 RESET_FLAGS Register (Offset = Fh) [Reset = 000Fh]

図 7-16. RESET_FLAGS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				AVDD_COLLAPSE_FLAG	RSTPIN_FLAG	VIO_FLAG	PORBASE_FLAG
R-0h				W-1h	W-1h	W-1h	W-1h

表 7-17. RESET_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
4	AVDD_COLLAPSE_FLAG	W	1h	Write to 0 to detect a AVDD collapse event, at which time this flag is automatically set to 1. AVDD collapse occurs when AVDD pin voltage reaches to within 1V of the VREF voltage.
3	RSTPIN_FLAG	W	1h	Write to 0 to detect a RESET pin reset event, at which time this flag is automatically set to 1.
2	VIO_FLAG	W	1h	Write to 0 to detect a VIO reset event, at which time this flag is automatically set to 1. VIO reset event occurs as a result of VIO pin voltage dropping to less than the POR threshold voltage.
1	PORBASE_FLAG	W	1h	Write to 0 to detect a POR-base reset event, at which time this flag is automatically set to 1. A POR-base reset event occurs as a result of AVDD pin voltage dropping to less than the POR threshold voltage.

7.1.17 OUT0_BUFFER_CODE Register (Offset = 10h) [Reset = 0000h]

図 7-17. OUT0_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-18. OUT0_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT0 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.18 OUT1_BUFFER_CODE Register (Offset = 11h) [Reset = 0000h]

図 7-18. OUT1_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-19. OUT1_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT1 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.19 OUT2_BUFFER_CODE Register (Offset = 12h) [Reset = 0000h]

図 7-19. OUT2_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-20. OUT2_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT2 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.20 OUT3_BUFFER_CODE Register (Offset = 13h) [Reset = 0000h]

図 7-20. OUT3_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-21. OUT3_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT3 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.21 OUT4_BUFFER_CODE Register (Offset = 14h) [Reset = 0000h]

図 7-21. OUT4_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-22. OUT4_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT4 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.22 OUT5_BUFFER_CODE Register (Offset = 15h) [Reset = 0000h]

図 7-22. OUT5_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-23. OUT5_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT5 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.23 OUT6_BUFFER_CODE Register (Offset = 16h) [Reset = 0000h]

図 7-23. OUT6_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-24. OUT6_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT6 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.24 OUT7_BUFFER_CODE Register (Offset = 17h) [Reset = 0000h]

図 7-24. OUT7_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-25. OUT7_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT7 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.25 OUT8_BUFFER_CODE Register (Offset = 18h) [Reset = 0000h]

図 7-25. OUT8_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-26. OUT8_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT8 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.26 OUT9_BUFFER_CODE Register (Offset = 19h) [Reset = 0000h]

図 7-26. OUT9_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-27. OUT9_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT9 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.27 OUT10_BUFFER_CODE Register (Offset = 1Ah) [Reset = 0000h]

図 7-27. OUT10_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-28. OUT10_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT10 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.28 OUT11_BUFFER_CODE Register (Offset = 1Bh) [Reset = 0000h]

図 7-28. OUT11_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-29. OUT11_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT11 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.29 OUT12_BUFFER_CODE Register (Offset = 1Ch) [Reset = 0000h]

図 7-29. OUT12_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-30. OUT12_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT12 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.30 OUT13_BUFFER_CODE Register (Offset = 1Dh) [Reset = 0000h]

図 7-30. OUT13_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-31. OUT13_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT13 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.31 OUT14_BUFFER_CODE Register (Offset = 1Eh) [Reset = 0000h]

図 7-31. OUT14_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-32. OUT14_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT14 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.32 OUT15_BUFFER_CODE Register (Offset = 1Fh) [Reset = 0000h]

図 7-32. OUT15_BUFFER_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-33. OUT15_BUFFER_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT15 buffer register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.33 OUT0_CLEAR_CODE Register (Offset = 20h) [Reset = 0000h]

図 7-33. OUT0_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-34. OUT0_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT0 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.34 OUT1_CLEAR_CODE Register (Offset = 21h) [Reset = 0000h]

図 7-34. OUT1_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-35. OUT1_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT1 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.35 OUT2_CLEAR_CODE Register (Offset = 22h) [Reset = 0000h]

図 7-35. OUT2_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-36. OUT2_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT2 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.36 OUT3_CLEAR_CODE Register (Offset = 23h) [Reset = 0000h]

図 7-36. OUT3_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-37. OUT3_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT3 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.37 OUT4_CLEAR_CODE Register (Offset = 24h) [Reset = 0000h]

図 7-37. OUT4_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-38. OUT4_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT4 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.38 OUT5_CLEAR_CODE Register (Offset = 25h) [Reset = 0000h]

図 7-38. OUT5_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-39. OUT5_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT5 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.39 OUT6_CLEAR_CODE Register (Offset = 26h) [Reset = 0000h]

図 7-39. OUT6_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-40. OUT6_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT6 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.40 OUT7_CLEAR_CODE Register (Offset = 27h) [Reset = 0000h]

図 7-40. OUT7_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-41. OUT7_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT7 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.41 OUT8_CLEAR_CODE Register (Offset = 28h) [Reset = 0000h]

図 7-41. OUT8_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-42. OUT8_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT8 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.42 OUT9_CLEAR_CODE Register (Offset = 29h) [Reset = 0000h]

図 7-42. OUT9_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-43. OUT9_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT9 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.43 OUT10_CLEAR_CODE Register (Offset = 2Ah) [Reset = 0000h]

図 7-43. OUT10_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-44. OUT10_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT10 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.44 OUT11_CLEAR_CODE Register (Offset = 2Bh) [Reset = 0000h]

図 7-44. OUT11_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-45. OUT11_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT11 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.45 OUT12_CLEAR_CODE Register (Offset = 2Ch) [Reset = 0000h]

図 7-45. OUT12_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-46. OUT12_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT12 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.46 OUT13_CLEAR_CODE Register (Offset = 2Dh) [Reset = 0000h]

図 7-46. OUT13_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-47. OUT13_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT13 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.47 OUT14_CLEAR_CODE Register (Offset = 2Eh) [Reset = 0000h]

図 7-47. OUT14_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-48. OUT14_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT14 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.48 OUT15_CLEAR_CODE Register (Offset = 2Fh) [Reset = 0000h]

図 7-48. OUT15_CLEAR_CODE Register

15	14	13	12	11	10	9	8
DATA[11:4]							
R/W-0h							
7	6	5	4	3	2	1	0
DATA[3:0]				RESERVED			
R/W-0h				R-0h			

表 7-49. OUT15_CLEAR_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	DATA[11:0]	R/W	0h	Code for OUT15 clear register, unipolar straight binary format.
3:0	RESERVED	R	0h	

7.1.49 GPIO_DATA Register (Offset = 31h) [Reset = 0001h]

図 7-49. GPIO_DATA Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							GPIO
R-0h							R/W-1h

表 7-50. GPIO_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	R	0h	
0	GPIO	R/W	1h	GPIO bit. For write operation, the GPIO pin operates as an output. Write a 1 to set the corresponding GPIO pin to either high impedance (FLEXIO_OUT_ODE=1) or logic 1 (FLEXIO_OUT_ODE=0). Write a 0 to set the corresponding GPIO pin to logic low. For read operations the GPIO pin operates as an input. Read to receive the status of the corresponding GPIO pin, which is determined by the voltage at the pin; the bit reads as 0 at start-up if the voltage at this pin is less than V_{IH} (the register value, 1 by default, is not returned when a read command is issued in this circumstance). After a reset event, the GPIO pin is in a high-impedance state.

7.1.50 DAC_STATUS Register (Offset = 32h) [Reset = 0000h]

図 7-50. DAC_STATUS Register

15	14	13	12	11	10	9	8
OUT15_SC_STS	OUT14_SC_STS	OUT13_SC_STS	OUT12_SC_STS	OUT11_SC_STS	OUT10_SC_STS	OUT9_SC_STS	OUT8_SC_STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
OUT7_SC_STS	OUT6_SC_STS	OUT5_SC_STS	OUT4_SC_STS	OUT3_SC_STS	OUT2_SC_STS	OUT1_SC_STS	OUT0_SC_STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 7-51. DAC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OUT15_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
14	OUT14_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
13	OUT13_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
12	OUT12_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition

表 7-51. DAC_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11	OUT11_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
10	OUT10_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
9	OUT9_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
8	OUT8_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
7	OUT7_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
6	OUT6_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
5	OUT5_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
4	OUT4_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
3	OUT3_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
2	OUT2_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
1	OUT1_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition
0	OUT0_SC_STS	R	0h	DAC short circuit condition, indicating whether this DAC channel is shorted to ground. 0h = DAC channel is not in short circuit condition 1h = DAC channel is in short circuit condition

8 Application and Implementation

注

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8.1 Application Information

The high linearity, small package size, and wide temperature range make the DAC60516 an excellent choice in applications such as optical networking, wireless infrastructure, and analog output modules for industrial systems. The device incorporates a 2.5V internal reference with an internal reference divider circuit that enables full-scale DAC output voltages of 2.5V or 5V.

8.1.1 Bipolar Voltage Output

The DAC60516 is designed for single-supply operation, but 図 8-1 shows that bipolar output is also possible.

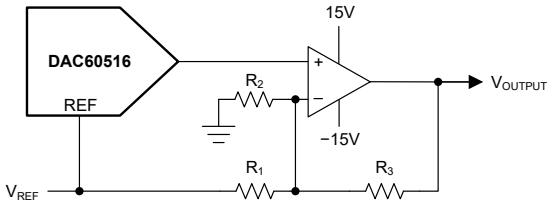

図 8-1. Bipolar Operation Using the DAC60516

The circuit in 図 8-1 gives a bipolar output voltage at V_{OUTPUT} and is calculated as follows (at gain = 1):

$$V_{OUTPUT}(CODE) = \left[\left(V_{REF} \times \frac{CODE}{2^{12}}\right)\left(1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right) - \left(V_{REF} \times \frac{R_3}{R_1}\right)\right] \quad (2)$$

where

- V_{OUTPUT}(CODE) = output voltage of circuit for a given code
- CODE = 0 to 4095. This is the digital code loaded to the DAC
- V_{REF} = reference voltage applied to the DAC60516

式 2 calculates the bipolar output span by defining a few parameters, the first being the value for the reference voltage. After choosing a reference voltage, set the gain resistors accordingly by determining the desired V_{OUTPUT} at code 0 and code 4096. For a V_{REF} of 2.5V, gain of 1, and a desired output voltage range of ±10V, the calculation is:

CODE = 0:

$$V_{OUTPUT}(0) = -\left(V_{REF} \times \frac{R_3}{R_1}\right) = -\left(2.5V \times \frac{R_3}{R_1}\right) \quad (3)$$

Setting the equation to minimum output span, $V_{OUTPUT}(0)$ = –10V, reduces the equation to: $R_3 / R_1 = 4$.

CODE = 4096:

Setting the equation to maximum output scan, $V_{OUTPUT}(4096)$ = 10V, and $R_3 / R_1 = 4$ reduces the equation to: $R_3 / R_2 = 3$

The maximum code of a 12-bit DAC is 4095; code 4096 is used to simplify 式 3. For practical use, the true output span uses a range of –10V to (10V – 1LSB); in this case, –10V to +9.9996V.

8.2 Typical Application

8.2.1 Programmable High-Current Voltage-Output Circuit

While the DAC60516 is capable of driving currents up to 50mA (with a short-circuit current rating of 75mA), the device can be integrated into the circuit in 図 8-2 to achieve a stable voltage output with even higher drive currents. In this application, the DAC programs the output voltage and gain of an amplifier. The amplifier maintains the output voltage using negative feedback. The high current to the load is provided by the transistor. This circuit is useful in applications where components must be tested with different voltage excitation levels at higher currents, including optical laser biasing applications (requiring over 50mA to 75mA of bias current) as well as semiconductor test equipment.

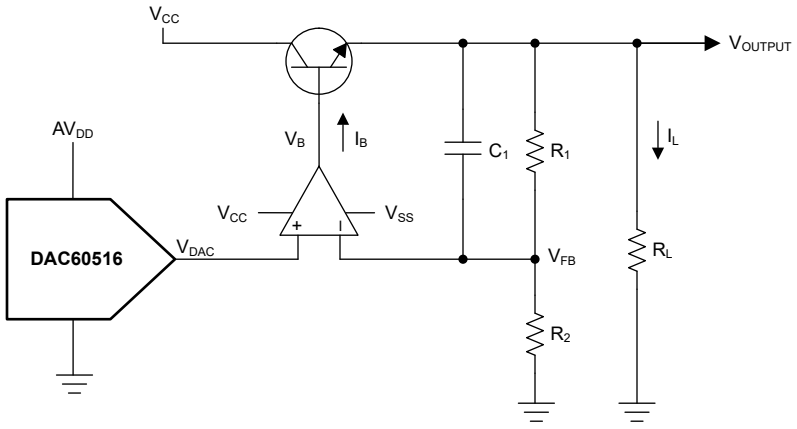

図 8-2. Programmable Voltage-Controlled Current Source Circuit

8.2.1.1 Design Requirements

An op amp with low offset and low drift (to minimize error) and sufficient gain bandwidth product (GBW) is recommended. R_1 and R_2 must have sufficient tolerance so that the desired output voltage (V_{OUTPUT}) accurately follows the DAC output voltage. Compensation capacitor C_1 must be larger than the input capacitance of the op-amp inputs. Choose a transistor that can provide the required load current and has a high H_{FE}, so that the base current is sufficiently smaller than the output current limit of the op amp. A bipolar-junction transistor (BJT) Darlington pair or a high-power metal-oxide semiconductor field-effect transistor (MOSFET) can be used.

表 8-1. Design Parameters

PARAMETER	VALUE
DAC output	0V to 2.5V
AV_{DD}	5V
V_{SS}	–5V
V_{CC}	24V
V_{REF}	2.5V
V_{OUTPUT}	0V to 5V
Current output	0A to 10A

8.2.1.2 Detailed Design Procedure

The transfer function of the output voltage is given by 式 4.

$$V_{OUTPUT} = V_{DAC}\left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

The resistance values can be chosen so that the quiescent current is negligible compared to the load current. For a desired load current of 10A at a desired V_{OUTPUT} of 5V (with V_{DAC} = 2.5V), choose R_1 and R_2 as 10kΩ each. This minimizes the quiescent current through the feedback network as 5V / 20kΩ = 250µA.

The base current, I_B, for the transistor for a given load current I_L is given by 式 5.

$$I_B = \frac{I_C}{H_{FE}} = \frac{1}{H_{FE}}\left(I_L + \left(\frac{V_{OUTPUT}}{R_1 + R_2}\right)\right) \quad (5)$$

Where:

- I_C = The collector current of the transistor
- H_{FE} = DC current gain of the transistor

V_{OUTPUT} / (R_1+R_2) is equal to the previously calculated quiescent current, which is negligible compared to the load current (particularly for load currents above 1A). This simplifies the equation to 式 6.

$$I_B = \frac{I_L}{H_{FE}} \quad (6)$$

To keep I_B less than 20mA, H_{FE} must be greater than I_L / 20mA. In general, compensation capacitor C_1 is not set by fixed equations, but rather by choosing values while observing the output small-signal step response.

8.2.1.3 Application Curve

図 8-3 shows the headroom curve for the DAC60516 when using the internal reference at gain = 2 (AV_{DD} = 5.5V). This curve illustrates how the DAC channels are able to maintain output voltage as load current increases.

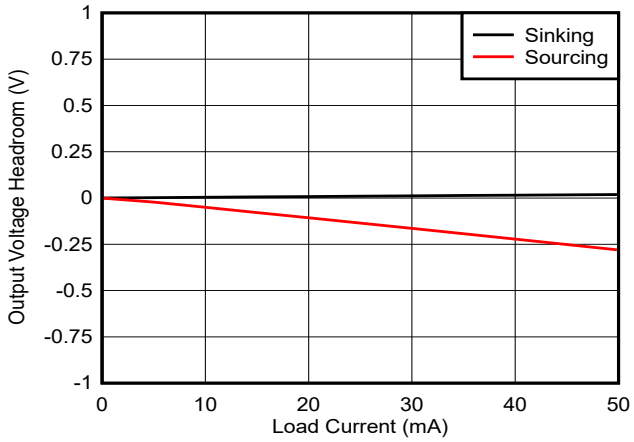

図 8-3. Headroom vs Load Current (DAC at Full-Scale Code)

8.3 Initialization Setup

Power on the device and ensure that the AV_{DD} and V_{IO} supplies are established. After the supplies have reached the minimum recommended operating value, a POR is issued so that the device initializes correctly. The DAC60516 requires 5ms to 10ms to initialize the serial interface after a POR; therefore, wait at least 10ms after start-up to communicate with the device.

8.4 Power Supply Recommendations

The DAC60516 operates within the specified AV_{DD} supply range of 2.7V to 5.5V and V_{IO} supply range of 1.7V to 5.5V. The DAC60516 does not require specific supply sequencing; however the serial interface requires 10ms to initialize and enable communication with the device.

The AV_{DD} supply must be well-regulated and low-noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To minimize noise from the power supply, include a 1µF to 10µF capacitor and 0.1µF bypass capacitor. The power supply must meet the input current requirements listed in *セクション 5*.

8.5 Layout

8.5.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- Bypass all power supply pins to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1µF to 0.22µF ceramic with a X7R or NP0 dielectric.
- Place power supplies and REF bypass capacitors close to the pins to minimize inductance and optimize performance.
- Use a high-quality, ceramic, type NP0 or X7R for optimized performance across temperature, and very low dissipation factor.
- The digital and analog sections must have proper placement with respect to the digital pins and analog pins of the DAC60516 device. The separation of analog and digital blocks minimizes coupling into neighboring blocks, as well as interaction between analog and digital return currents.

8.5.2 Layout Examples

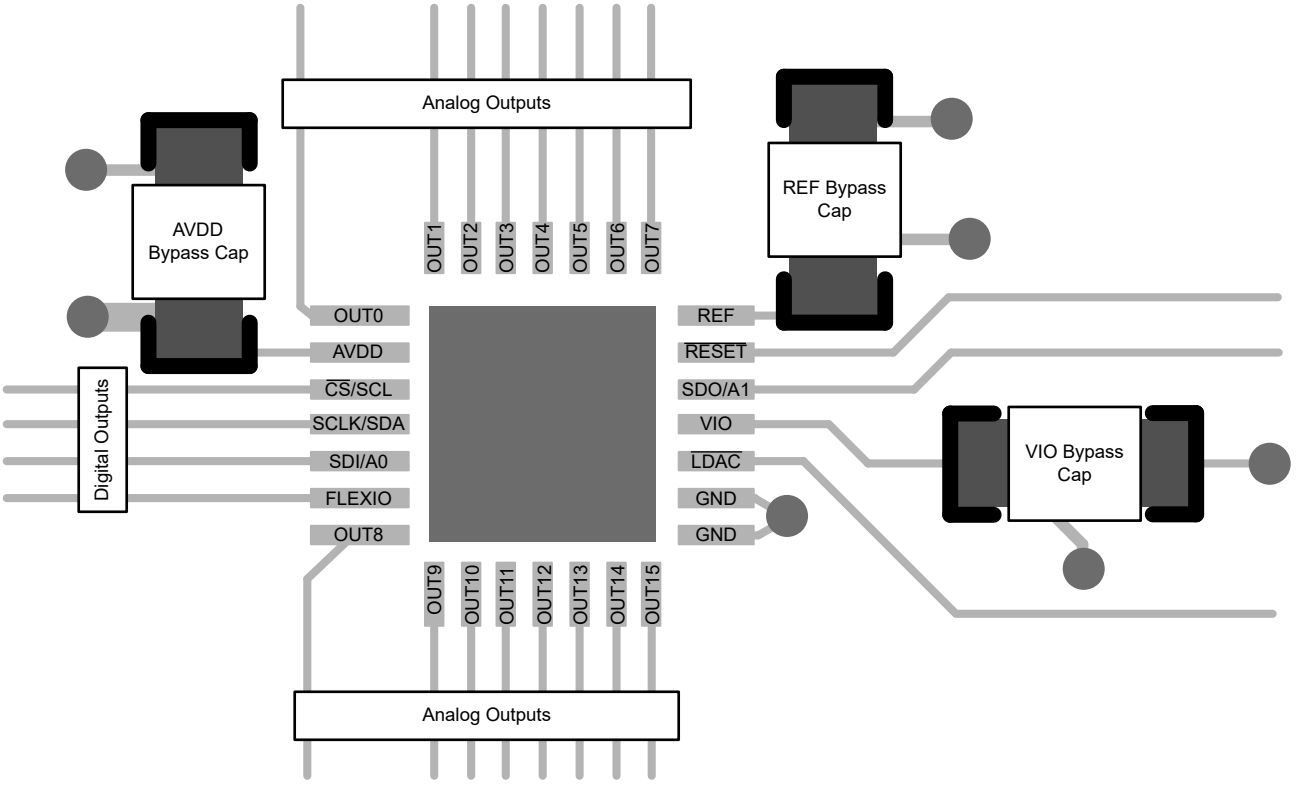

図 8-4. DAC60516 QFN Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC60516RUYR	Active	Production	WQFN (RUY) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	DAC 60516
DAC60516RUYR.A	Active	Production	WQFN (RUY) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See DAC60516RUYR	DAC 60516
DAC60516RUYT	Active	Production	WQFN (RUY) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	DAC 60516
DAC60516RUYT.A	Active	Production	WQFN (RUY) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See DAC60516RUYT	DAC 60516

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

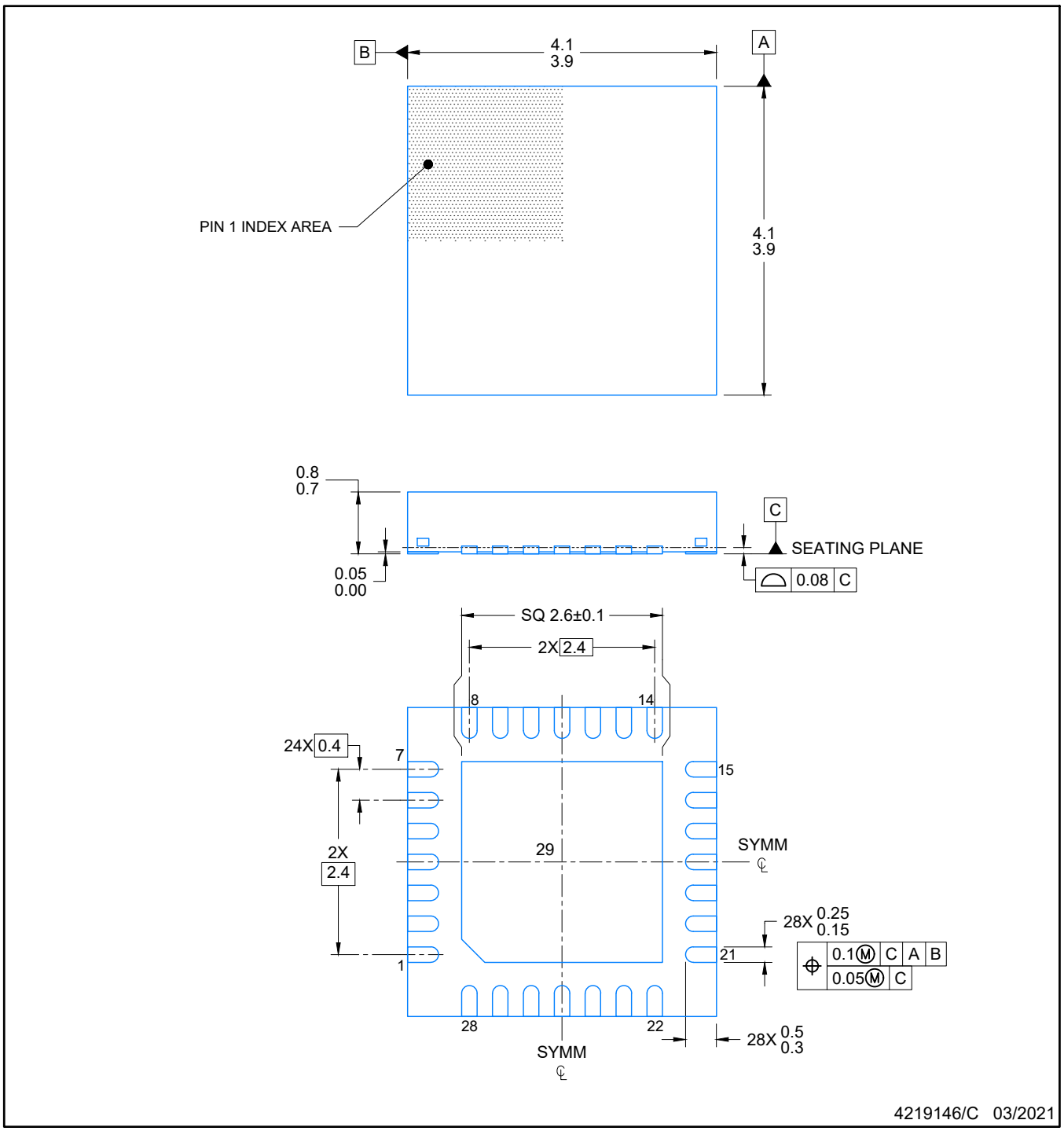
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RUY0028A

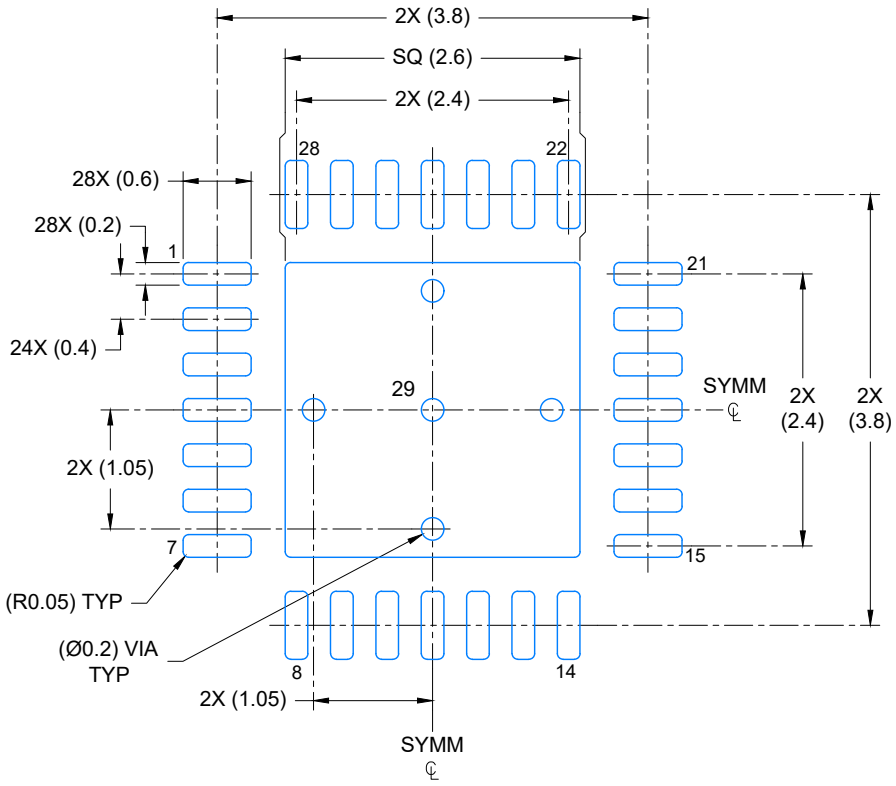
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

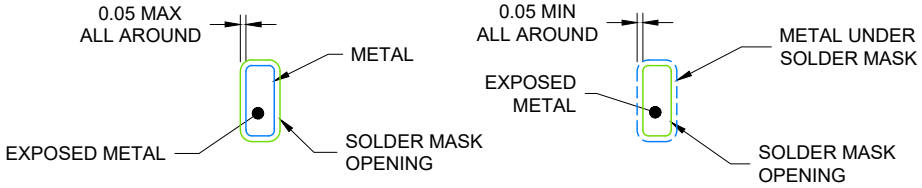


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

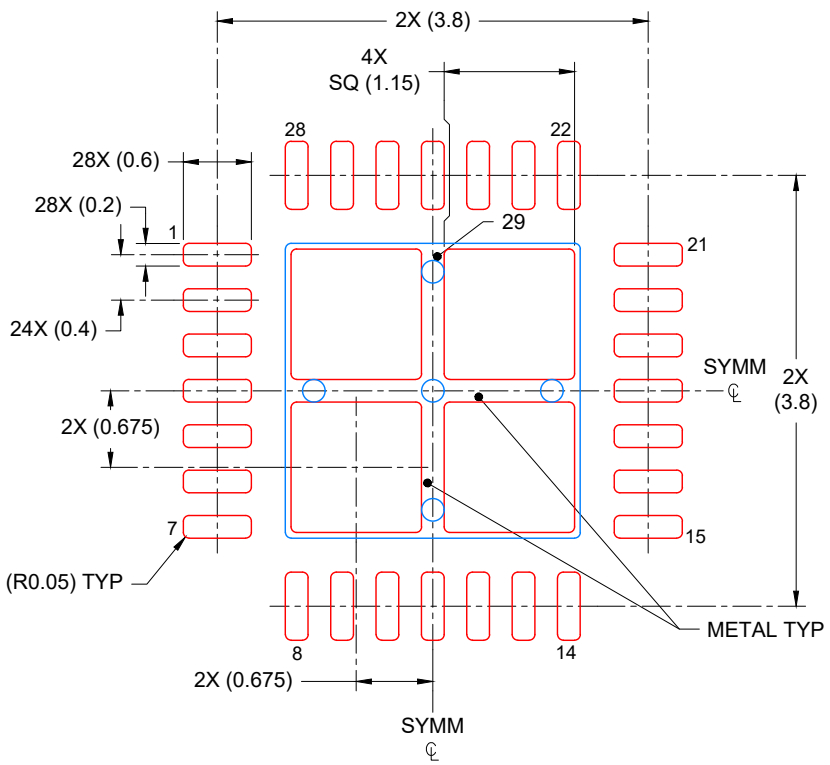
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219146/C 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

4219146/C 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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