参考資料

DLP160CP 0.16 HD および nHD デジタル マイクロミラー デバイス

1 特長

- 超小型 0.16 インチ (3.965mm) 対角マイクロミラー アレイ
  - nHD 構成 — 640 x 360 解像度を画面に表示
  - HD 構成 — 1280 x 720 解像度を画面に表示
  - 5.4μm のマイクロミラー ピッチ
  - マイクロミラー傾斜角 : 17° (平面に対して)
  - 側面照明による最適な効率と光学エンジン サイズ
  - 偏波無依存のアルミニウム製マイクロミラー表面
- 4 ビット SubLVDS 入力データ バス
- 専用の DLPC3421 ディスプレイ コントローラと DLPA2000、DLPA2005 または DLPA3000 PMIC/LED ドライバによる信頼性の高い動作

2 アプリケーション

- ディスプレイ:
  - ウルトラモバイルで超低消費電力の超小型プロジェクタ
  - スマートフォン、タブレット、ノート PC
  - スマート・ディスプレイ
  - スマート・ホーム
  - 拡張現実 (AR) メガネ
  - 情報ディスプレイ

3 概要

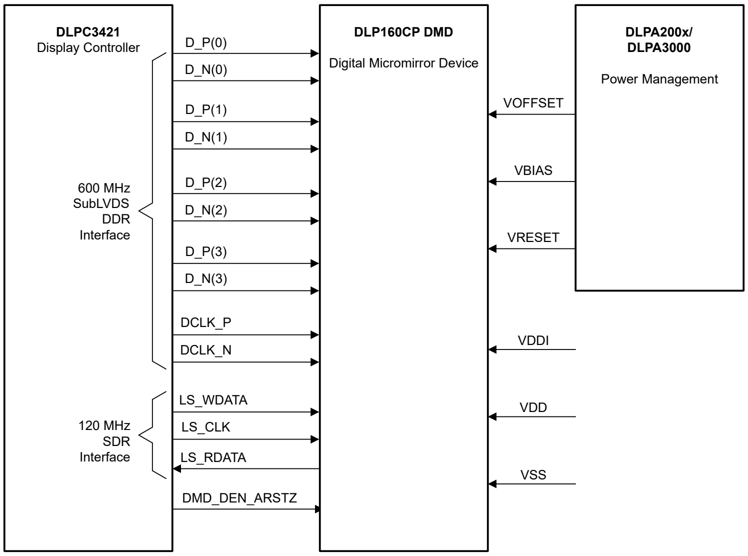
DLP160CP デジタル マイクロミラー デバイス (DMD) は、デジタル制御の MOEMS (micro-opto-electromechanical system) 空間光変調器 (SLM) です。適切な光学システムと組み合わせることで、DLP160CP DMD は鮮明で高品質の画像または映像を表示できます。DLP160CP は、DLP160CP DMD および DLPC3421 コントローラで構成されるチップセットの一部です。このチップセットは、DLPA2000、DLPA2005、DLPA3000 (HD 構成のみ) PMIC/LED ドライバでもサポートされています。DLP160CP は小型であるため、小さな外形と低消費電力が重視される携帯機器に最適です。コンパクトな DLP160CP DMD とコントローラおよび PMIC/LED ドライバとを組み合わせて使うことにより、完全なシステム ソリューションとして小型化、低消費電力化、表示画質向上を実現できます。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ
DLP160CP	FQT (35)	13.39mm × 4.97mm × 3.18mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

アプリケーション概略図



English Data Sheet: DLPS228

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4 Pin Configuration and Functions

図 4-1. FQT Package 35-Pin

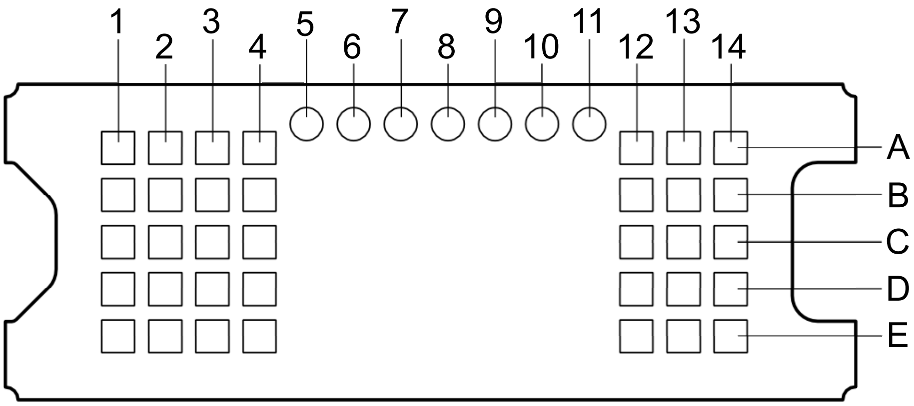


表 4-1. Connector Pins

PIN[(1)]						PACKAGE NET LENGTH (mm)[(2)]
NAME	**NO.**	**TYPE**	**SIGNAL**	**DATA RATE**	**DESCRIPTION**	
DATA INPUTS						
D_N(0)	A2	I	SubLVDS	Double	Data, negative	1.91
D_N(1)	A4	I	SubLVDS	Double	Data, negative	3.6
D_N(2)	D4	I	SubLVDS	Double	Data, negative	3.28
D_N(3)	E2	I	SubLVDS	Double	Data, negative	1.67
D_P(0)	A3	I	SubLVDS	Double	Data, positive	2.03
D_P(1)	B4	I	SubLVDS	Double	Data, positive	3.7
D_P(2)	E4	I	SubLVDS	Double	Data, positive	3.39
D_P(3)	E3	I	SubLVDS	Double	Data, positive	1.77
DCLK_N	C3	I	SubLVDS	Double	Clock, negative	2.29
DCLK_P	C4	I	SubLVDS	Double	Clock, positive	2.4
CONTROL INPUTS						
LS_WDATA	C12	I	LPSDR	Single	Write data for low-speed interface	1.55
LS_CLK	C13	I	LPSDR	Single	Clock for low-speed interface	1.65
DMD_DEN_ARSTZ	D12	I	LPSDR	Single	Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	1.57
LS_RDATA	D13	O	LPSDR	Single		1.43
POWER						
V_{BIAS} [(3)]	A13	Power			Supply voltage for positive bias level at micromirrors	
V_{OFFSET} [(3)]	E13	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	
V_{RESET} [(3)]	A14	Power			Supply voltage for negative reset level at micromirrors.	

表 4-1. Connector Pins (続き)

PIN[1]						PACKAGE NET LENGTH (mm)[2]
NAME	NO.	TYPE	SIGNAL	DATA RATE	DESCRIPTION	
V_{DD}	B12	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
V_{DD}	B14	Power				
V_{DD}	C1	Power				
V_{DD}	C14	Power				
V_{DD}	C2	Power				
V_{DD}	E14	Power				
V_{DDI}	B1	Power			Supply voltage for SubLVDS receivers.	
V_{DDI}	D1	Power				
V_{SS}	A1	Ground			Common return. Ground for all power.	
V_{SS}	A12	Ground				
V_{SS}	B13	Ground				
V_{SS}	B2	Ground				
V_{SS}	B3	Ground				
V_{SS}	D14	Ground				
V_{SS}	D2	Ground				
V_{SS}	D3	Ground				
V_{SS}	E1	Ground				
V_{SS}	E12	Ground				

(1) The low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)*. See JESD209B.

(2) Net trace lengths inside the package:
The relative dielectric constant for the FQP ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769in/ns.
Propagation delay = 0.265ns/inch = 265ps/in = 10.43ps/mm.

(3) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.

表 4-2. Test Pads

NUMBER	SYSTEM BOARD
A5	Do not connect
A6	Do not connect
A7	Do not connect
A8	Do not connect
A9	Do not connect
A10	Do not connect
A11	Do not connect

5 Specifications

5.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
Supply voltage	V_{DD}	Supply voltage for LVCMOS core logic(2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	V_{DDI}	Supply voltage for SubLVDS receivers(2)	–0.5	2.3	V
	V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2) (3)	–0.5	11	V
	V_{BIAS}	Supply voltage for micromirror electrode(2)	–0.5	19	V
	V_{RESET}	Supply voltage for micromirror electrode(2)	–15	0.5	V
	$\|V_{DDI}–V_{DD}\|$	Supply voltage delta (absolute value)(4)		0.3	V
	$\|V_{BIAS}–V_{OFFSET}\|$	Supply voltage delta (absolute value)(5)		11	V
	$\|V_{BIAS}–V_{RESET}\|$	Supply voltage delta (absolute value)(6)		34	V
Input voltage	Input voltage for other inputs LPSDR(2)		–0.5	V_{DD} + 0.5	V
	Input voltage for other inputs SubLVDS(2) (7)		–0.5	V_{DDI} + 0.5	V
Input pins	$\|V_{ID}\|$	SubLVDS input differential voltage (absolute value)(7)		810	mV
	I_{ID}	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational (8)	–20	90	°C
		Temperature – non-operational(8)	–40	90	°C
	$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(9)		30	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device lifetime.

(2) All voltage values are with respect to the ground terminals (V_{SS}). The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.

(3) V_{OFFSET} supply transients must fall within specified voltages.

(4) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw.

(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.

(6) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.

(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.

(8) The highest temperature of the active array (as calculated by the *セクション 6.6*) or of any point along the window edge is defined in 図 6-1. The location of thermal test point TP2 in 図 6-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.

(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 6-1. The window test point TP2 shown in 図 6-1 is intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP}	Average dew point temperature (non-condensing) (1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(3)					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(4)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for micromirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\lvert V_{DDI}–V_{DD} \rvert$	Supply voltage delta (absolute value)(5)			0.3	V
$\lvert V_{BIAS}–V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(6)			10.5	V
$\lvert V_{BIAS}–V_{RESET} \rvert$	Supply voltage delta (absolute value)(7)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(8)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(9)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(9)					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value). See 図 5-8, 図 5-9	150	250	350	mV
V_{CM}	Common mode voltage. See 図 5-8, 図 5-9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage. See 図 5-8, 図 5-9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance. See 図 5-10	80	100	120	Ω
	100Ω differential PCB trace	6.35		152.4	mm

5.4 Recommended Operating Conditions (続き)

Over-operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(10) (11) (12) (13)	0		40 to 70(12)	°C
	Array Temperature – short-term operational, 25 hr max(11) (14)	-20		–10	°C
	Array Temperature – short-term operational, 500 hr max(11) (14)	-10		0	°C
	Array Temperature – short-term operational, 500 hr max(11) (14)	70		75	°C
T_{WINDOW}	Window Temperature – operational(15) (16)			90	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(17)			15	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing) (18)			24	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing) (19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	months
ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410nm(10)			10	mW/cm^2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm(20)			26.1	W/cm^2
ILL_{IR}	Illumination power at wavelengths > 800nm			10	mW/cm^2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm(20)			8.3	W/cm^2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 445nm(20)			1.5	W/cm^2
ILL_{θ}	Illumination marginal ray angle(15)			55	deg

(1) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *セクション 5.4*. No level of performance is implied when operating the device above or below the *セクション 5.4* limits.
(2) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(3) All voltage values are with respect to the ground pins (V_{SS}).
(4) V_{OFFSET} supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(7) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(8) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(9) Refer to the SubLVDS timing requirements in *セクション 5.7*.
(10) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce the device's lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 6-1 and the package thermal resistance using *セクション 6.6*.
(12) Per 図 5-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *セクション 6.8* for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the usable life of the device.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including at the pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document and may negatively affect lifetime.
(16) Window temperature is the highest temperature on the window edge shown in 図 6-1. The location of thermal test point TP2 in 図 6-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 図 6-1. The window test point TP2 shown in 図 6-1 is intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(20) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).

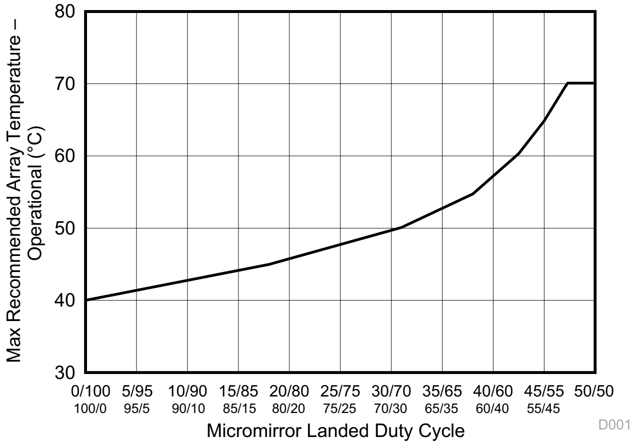


図 5-1. Maximum Recommended Array Temperature — Derating Curve

5.5 Thermal Information

THERMAL METRIC(1)		DLP160CP	UNIT
		FQT	
		35 PINS	
Thermal resistance	Active area to test point 1 (TP1)(1)	13	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *セクション 5.4*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipated by the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	V_{DD} = 1.95V			50	mA
		V_{DD} = 1.8V		38		
I_{DDI}	Supply current: V_{DDI} (3) (4)	V_{DDI} = 1.95V			12	mA
		V_{DDI} = 1.8V		8		
I_{OFFSET}	Supply current: V_{OFFSET} (5) (6)	V_{OFFSET} = 10.5V			1	mA
		V_{OFFSET} = 10V		0.9		
I_{BIAS}	Supply current: V_{BIAS} (5) (6)	V_{BIAS} = 18.5V			0.2	mA
		V_{BIAS} = 18V		0.18		
I_{RESET}	Supply current: V_{RESET} (6)	V_{RESET} = –14.5V			-0.9	mA
		V_{RESET} = –14V		-0.8		
POWER(7)						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	V_{DD} = 1.95V			97.5	mW
		V_{DD} = 1.8V		68.4		
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	V_{DDI} = 1.95V			23.4	mW
		V_{DD} = 1.8V		14.4		
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5) (6)	V_{OFFSET} = 10.5V			10.5	mW
		V_{OFFSET} = 10V		9		
P_{BIAS}	Supply power dissipation: V_{BIAS} (5) (6)	V_{BIAS} = 18.5V			3.7	mW
		V_{BIAS} = 18V		3.2		
P_{RESET}	Supply power dissipation: V_{RESET} (6)	V_{RESET} = –14.5V			13.1	mW
		V_{RESET} = –14V		11.2		
P_{TOTAL}	Supply power dissipation: Total			106	148	mW
LPSDR INPUT(8)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × V_{DD}	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(9)		–0.3		0.2 × V_{DD}	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	図 5-10	0.1 × V_{DD}		0.4 × V_{DD}	V
I_{IL}	Low–level input current	V_{DD} = 1.95V; V_I = 0V	–100			nA
I_{IH}	High–level input current	V_{DD} = 1.95V; V_I = 1.95V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2mA	0.8 × V_{DD}			V

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
V_{OL}	DC output low voltage	I_{OL} = 2mA			0.2 × V_{DD}	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1MHz			10	pF
	Input capacitance SubLVDS	f = 1MHz			10	pF
C_{OUT}	Output capacitance	f = 1MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1MHz; (360 × 160 micromirrors)	90		140	pF

(1) Device electrical characteristics are over *セクション 5.4* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) Supply power dissipation based on 3 global resets in 300µs.
(7) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) LPSDR specification is for pin LS_RDATA.

5.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

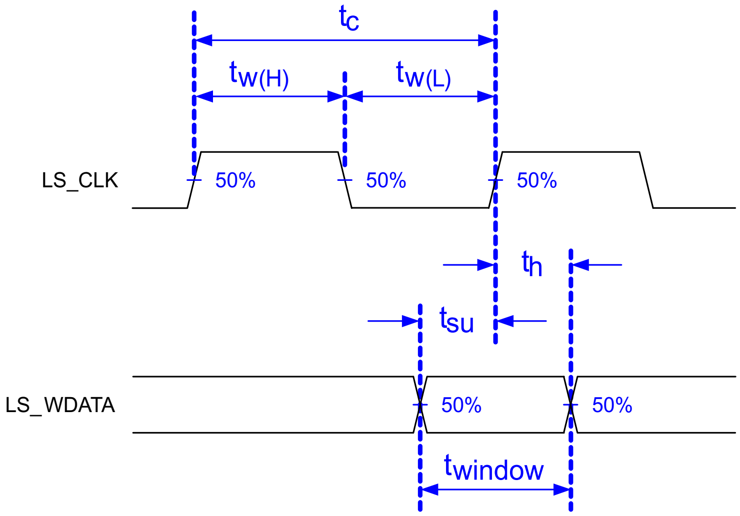
			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × V_{DD}, 図 5-3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × V_{DD}, 図 5-3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × V_{DD}, 図 5-3	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × V_{DD}, 図 5-3	0.25			V/ns
t_c	Cycle time LS_CLK	図 5-2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, 図 5-2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, 図 5-2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, 図 5-2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, 図 5-2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + hold time, 図 5-2	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25V/ns reduction in slew rate below 1V/ns, 図 5-5		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, 図 5-4	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, 図 5-4	0.7	1		V/ns
t_c	Cycle time DCLK	図 5-6	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, 図 5-6	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, 図 5-6	0.79			ns
t_{su}	Setup time	D(0:7) valid before DCLK ↑ or DCLK ↓, 図 5-6	Setup and Hold times are defined by t_{WINDOW}			
t_h	Hold time	D(0:7) valid after DCLK ↑ or DCLK ↓, 図 5-6	Setup and Hold times are defined by t_{WINDOW}			
t_{WINDOW}	Window time	Setup time + hold time, 図 5-6, 図 5-7	0.3			ns

5.7 Timing Requirements (続き)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in 図 5-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 図 5-3.
(3) Window time derating example: 0.5V/ns slew rate increases the window time by 0.7ns, from 3ns to 3.7ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to the *セクション 5.6* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

図 5-2. LPSDR Switching Parameters

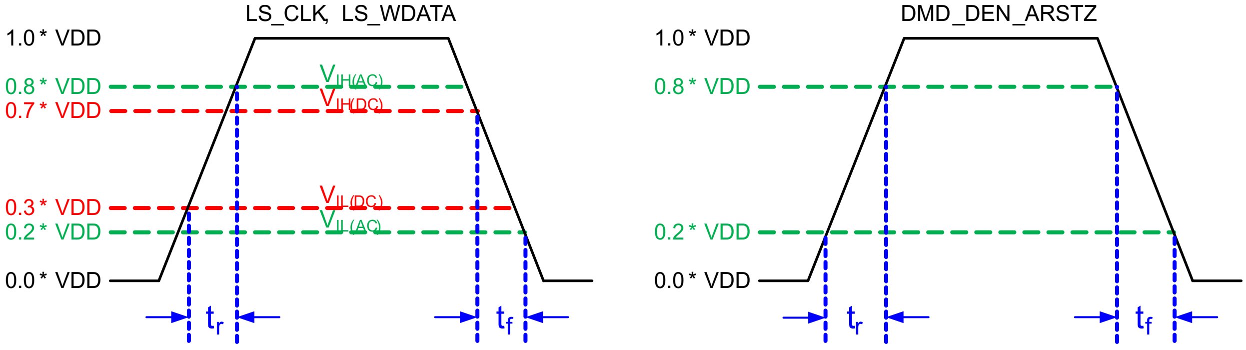


図 5-3. LPSDR Input Rise and Fall Slew Rate

Not to Scale

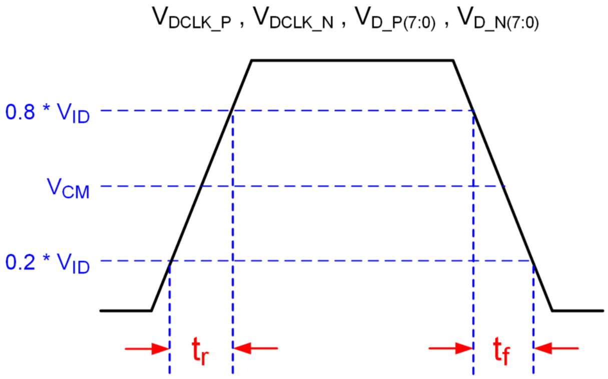
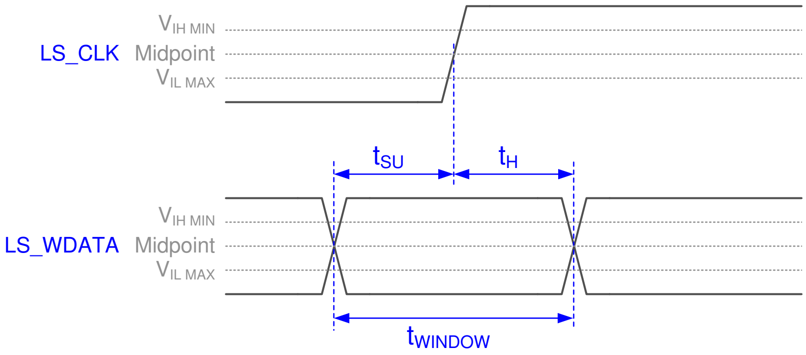


図 5-4. SubLVDS Input Rise and Fall Slew Rate



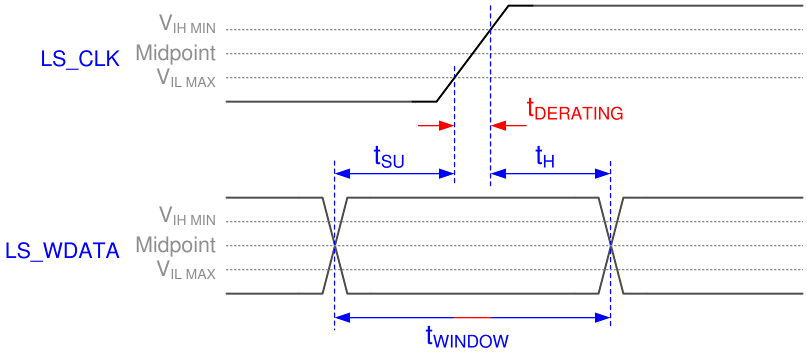


図 5-5. Window Time Derating Concept

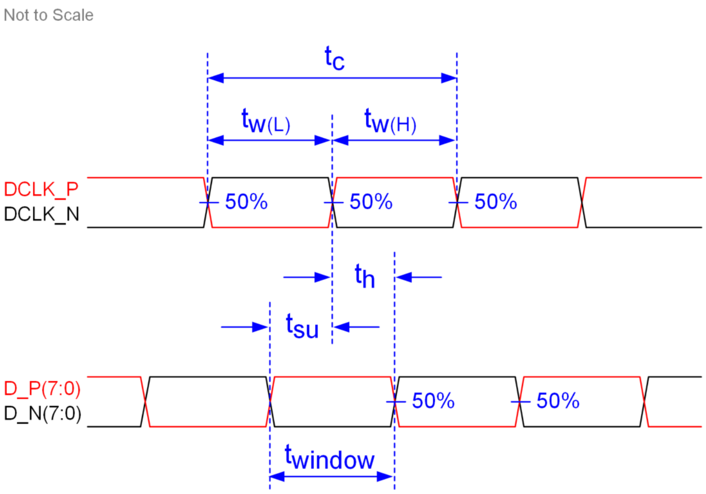
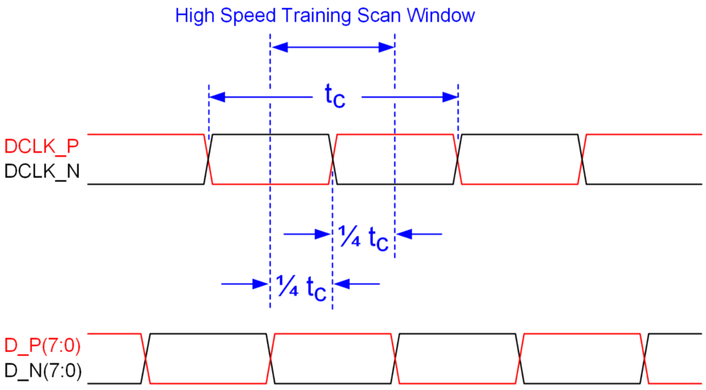


図 5-6. SubLVDS Switching Parameters



Note: Refer to *セクション 6.3.3* for details.

図 5-7. High-Speed Training Scan Window

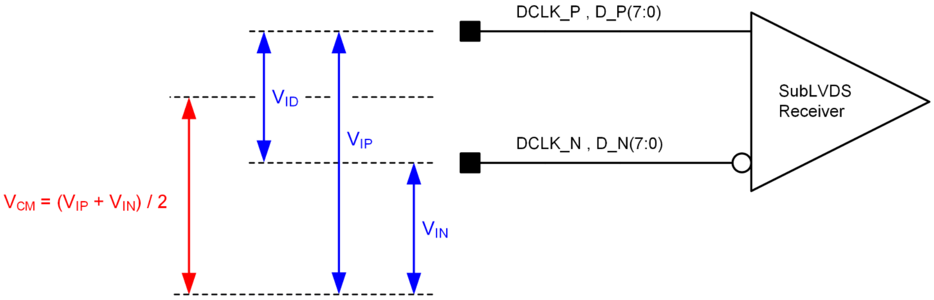


図 5-8. SubLVDS Voltage Parameters

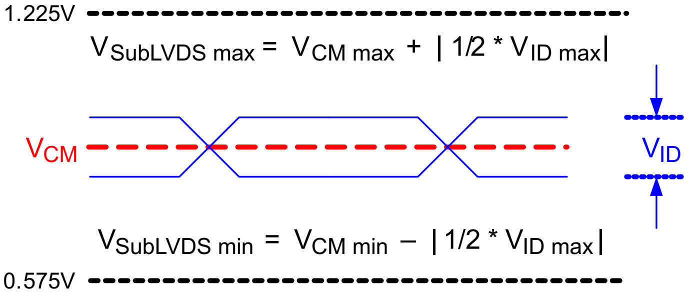


図 5-9. SubLVDS Waveform Parameters

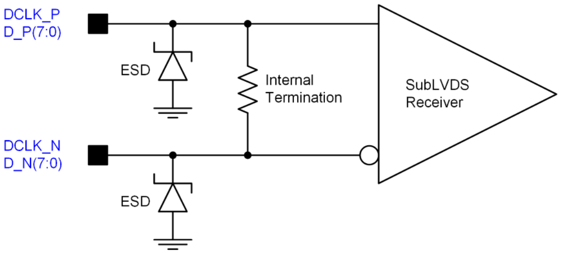


図 5-10. SubLVDS Equivalent Input Circuit

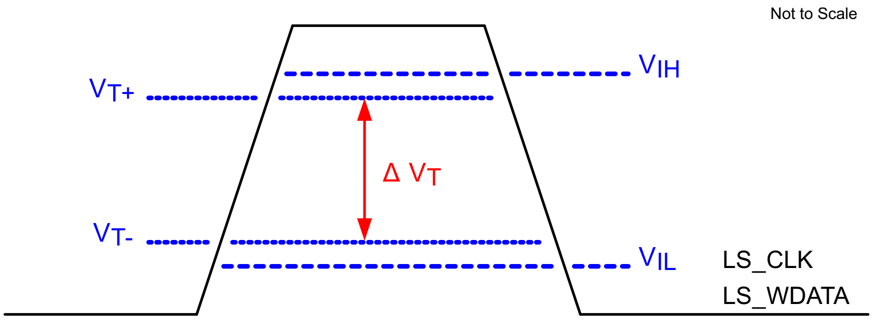


図 5-11. LPSDR Input Hysteresis

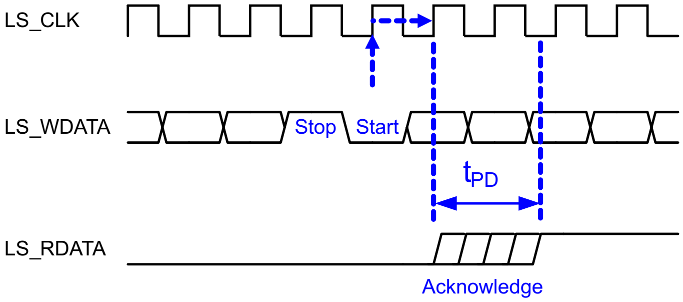
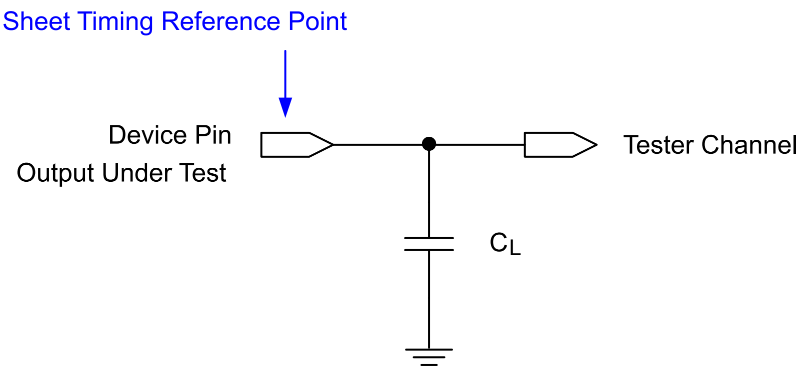


図 5-12. LPSDR Read Out



See セクション 6.3.4 for more information.

図 5-13. Test Load Circuit for Output Propagation Measurement

5.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output. See 図 5-12.	C_L = 45pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over セクション 5.4 unless otherwise noted.

5.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal interface area (1)			42	N
• Clamping and electrical interface area (1)			94	N

(1) Uniformly distributed within the area shown in 図 5-14.

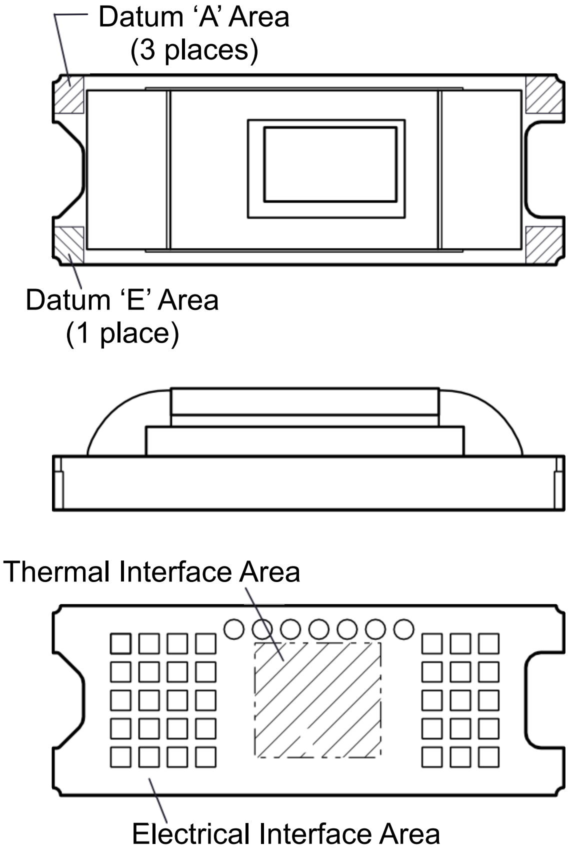


図 5-14. System Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER		VALUE	UNIT
Number of active columns [2]	See 図 5-15	640	micromirrors
Number of active rows [2]	See 図 5-15	360	micromirrors
Micromirror (pixel) pitch	See 図 5-16	5.4	µm
Micromirror active array width	Micromirror pitch × number of active columns; see 図 5-15	3.456	mm
Micromirror active array height	Micromirror pitch × number of active rows; see 図 5-15	1.944	mm
Micromirror active border	Pond of micromirror (POM)[1]	20	micromirrors/side

(1) The structure and qualities of the border around the active array include a band of partially functional micromirrors called the POM. These micromirrors are structurally or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

(2) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 1280x720 pixel image being displayed.

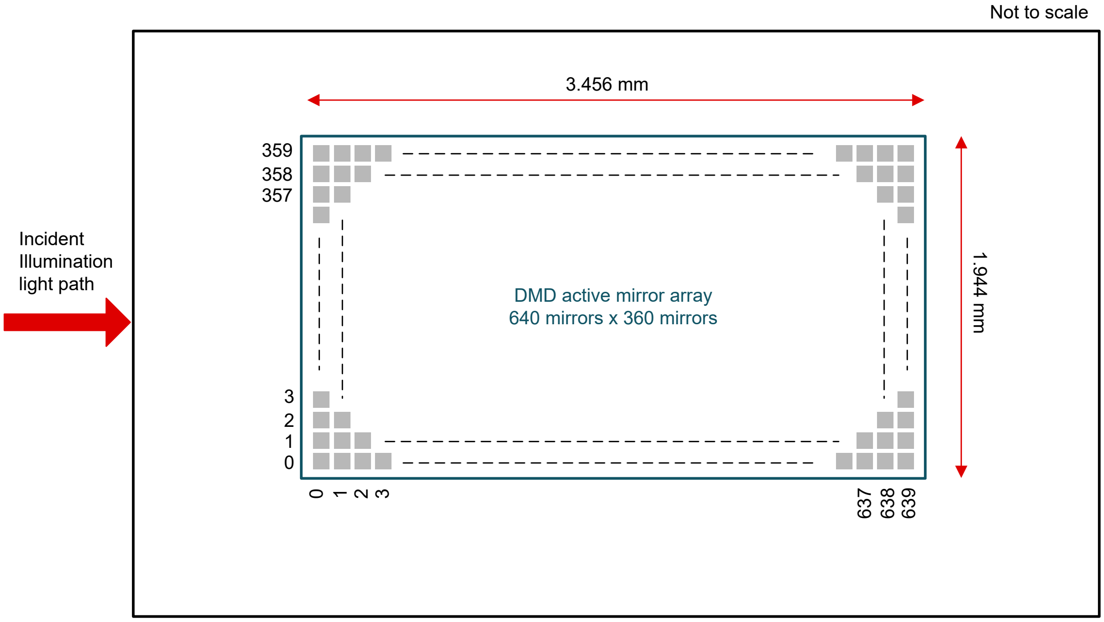


図 5-15. Micromirror Array Physical Characteristics

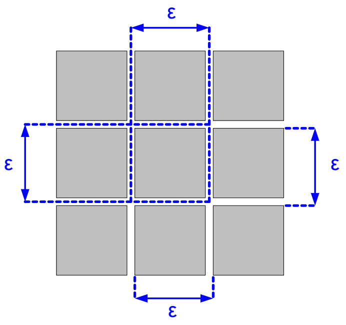


図 5-16. Mirror (Pixel) Pitch

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state(1)		17		degree
Micromirror tilt angle tolerance(2) (3) (4) (5)			–1.4		1.4	degree
Micromirror tilt direction (6) (7)		Landed ON state		180		degree
		Landed OFF state		270		
Micromirror crossover time(8)		Typical performance		1	3	µs
Micromirror switching time(9)		Typical performance	10			
Image performance (10)	Bright pixel(s) in active area (11)	Gray 10 Screen (12)			0	micromirrors
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
	Dark pixel(s) in the active area (14)	White Screen			4	
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See *Landed Pixel Orientation and Tilt*.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
    Test set degamma shall be linear
    Test set brightness and contrast shall be set to nominal
    The diagonal size of the projected image shall be a minimum of 20 inches
    The projections screen shall be 1X gain
    The projected image shall be inspected from a 38 inch minimum viewing distance
    The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
    Red = 10/255
    Green = 10/255
    Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

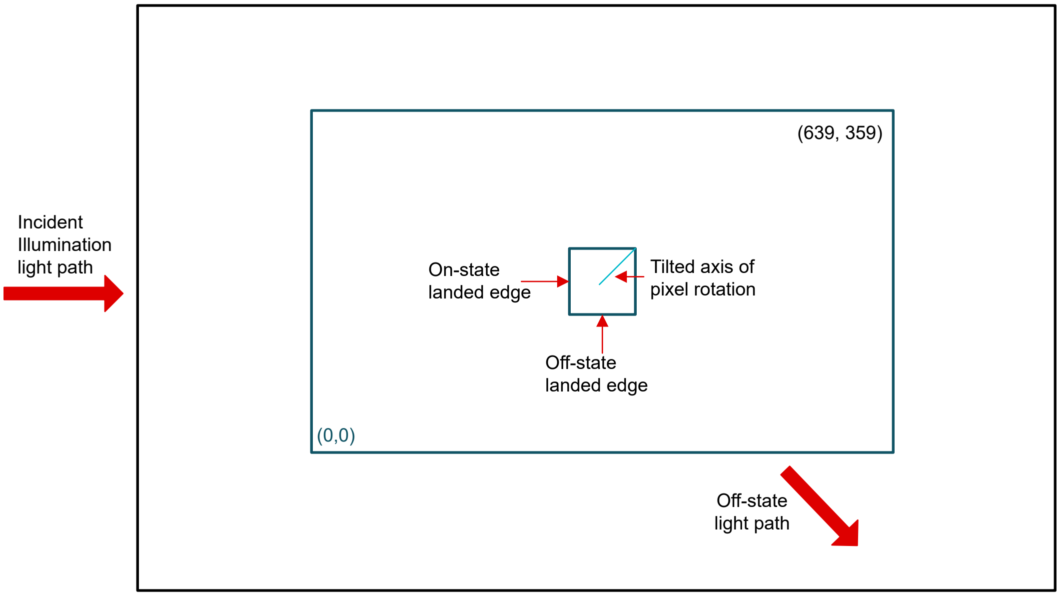


図 5-17. Landed Pixel Orientation and Tilt

5.12 Window Characteristics

PARAMETER[1]		MIN	NOM	MAX	UNIT
Window material			Corning Eagle XG		
Window refractive index	At wavelength 546.1nm		1.5119		
Window aperture				See [1]	
Illumination overfill				See [1]	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680nm. Applies to all angles 0° to 30° AOI	97%			
	Average over the wavelength range 420 to 680nm. Applies to all angles 30° to 45° AOI	97%			

(1) See *セクション 6.5* for more information.

5.13 Chipset Component Usage Specification

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP160CP is a component of one or more DLP chipsets. Reliable function and operation of the DLP160CP requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

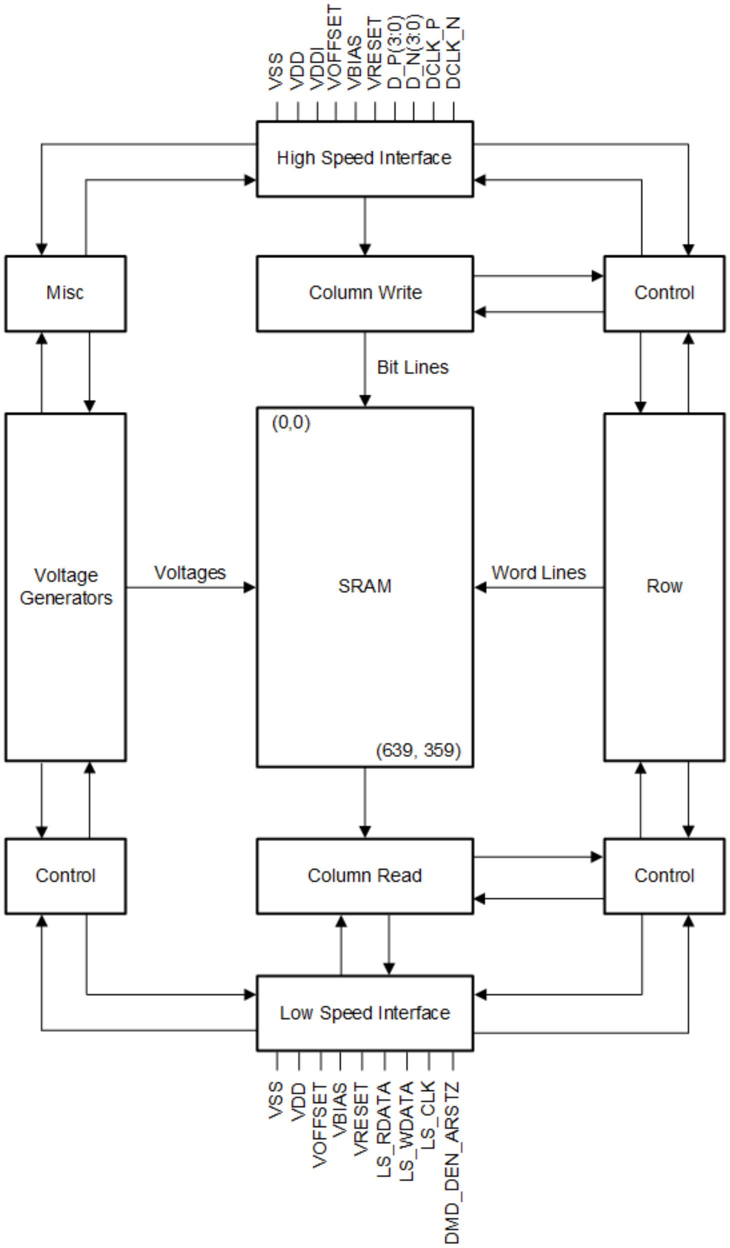
6 Detailed Description

6.1 Overview

The DLP160CP is a 0.16 インチ (対角) spatial light modulator of aluminum micromirrors. The pixel array size is 640 columns by 360 rows in a square grid pixel arrangement. The electrical interface is sub-low voltage differential signaling (SubLVDS) data.

The DLP160CP is part of the chipset comprised of the DLP160CP DMD, the DLPC3421ZVB display controller, and the DLPA200x/DLPA3000 PMIC/LED driver. To ensure reliable operation, the DLP160CP DMD must always be used with the DLPC3421ZVB display controller and the DLPA200x/DLPA3000 PMIC/LED drivers.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The power management IC DLPA200x/DLPA3000 contains three regulated DC supplies for the DMD reset circuitry: V_{BIAS}, V_{RESET} and V_{OFFSET}, as well as the two regulated DC supplies for the DLPC3421ZVB controller.

6.3.2 Low-Speed Interface

The low speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

6.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs with a dedicated clock.

6.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 5-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3421ZVB controller. See the DLPC3421ZVB controller data sheet or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display border and/or active area could occur.

6.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit the total light flux incident anywhere on the window aperture from exceeding approximately 10% of the total light flux in the active array. Depending on the particular optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

6.6 Micromirror Array Temperature Calculation

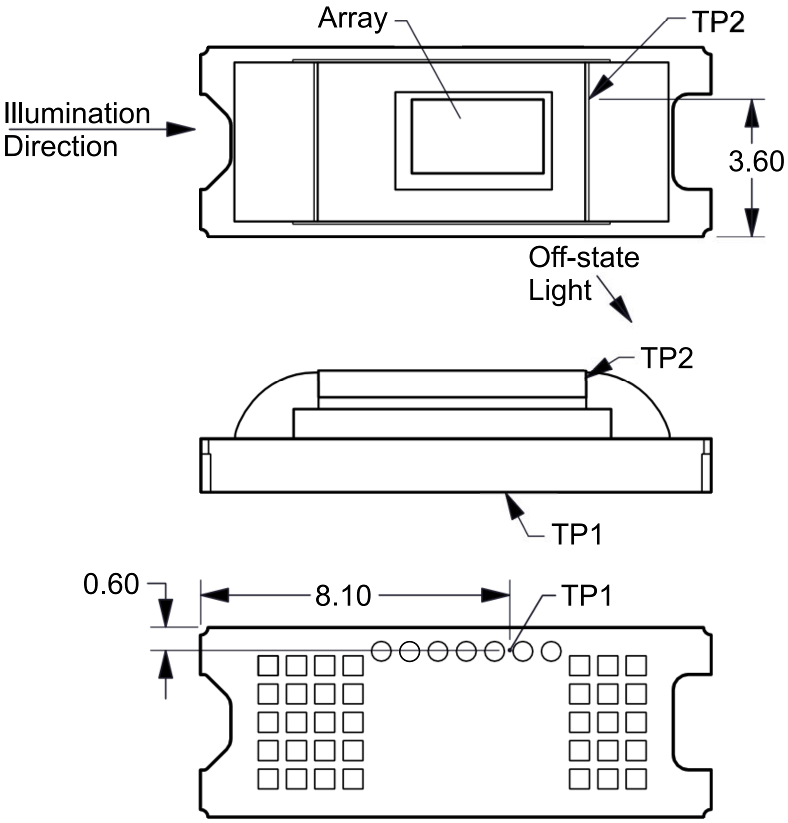


図 6-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test point TP1 in 図 6-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)

- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in セクション 5.5 from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.4

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.07W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$Q_{INCIDENT}$ = 1.4W (measured)

$T_{CERAMIC}$ = 55.0°C (measured)

$Q_{ELECTRICAL}$ = 0.07W

$Q_{ARRAY} = 0.07W + (0.40 \times 1.4W) = 0.63W$

$T_{ARRAY} = 55.0°C + (0.63W \times 13.0°C/W) = 63.2°C$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)

- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤445nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD outside the array (OV_{ILL}) and the percent of the total illumination on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 1.40W (measured)

$A_{ARRAY} = (0.3456 \times 0.1944) = 0.0672cm^2$ (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00021 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00002 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)

$A_{ILL} = 0.0672 \div (1 - 0.163) = 0.0803\ cm^2$

$ILL_{UV} = [0.00021 \times 1.40W] \times 1000 \div 0.0803cm^2 = 3.66mW/cm^2$

$ILL_{VIS} = [0.99977 \times 1.40W] \div 0.0803cm^2 = 17.4W/cm^2$

$ILL_{IR} = [0.00002 \times 1.40W] \times 1000 \div 0.0803cm^2 = 0.349\ mW/cm^2$

$ILL_{BLU} = [0.28100 \times 1.40W] \div 0.0803cm^2 = 4.90\ W/cm^2$

$ILL_{BLU1} = [0.03200 \times 1.40W] \div 0.0803\ cm^2 = 0.558\ W/cm^2$

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time), whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the usable life of the DMD.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the usable life of the DMD. The relationship between temperature and landed duty cycle is quantified in the derating curve shown in 図 5-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience close to a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Nominal Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (1)$$

where

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that red, green, and blue are displayed (respectively) to achieve the desired white point.

For example, assuming that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 6-2.

表 6-2. Example Nominal Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLP controller DLPC3421ZVB, the two functions which affect the landed duty cycle are gamma and IntelliBright ™.

Gamma is a power function of the form $Output\_Level = A \times Input\_Level^{Gamma}$, where A is a scaling factor that is typically set to 1.

In the DLPC3421ZVB controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 6-2.

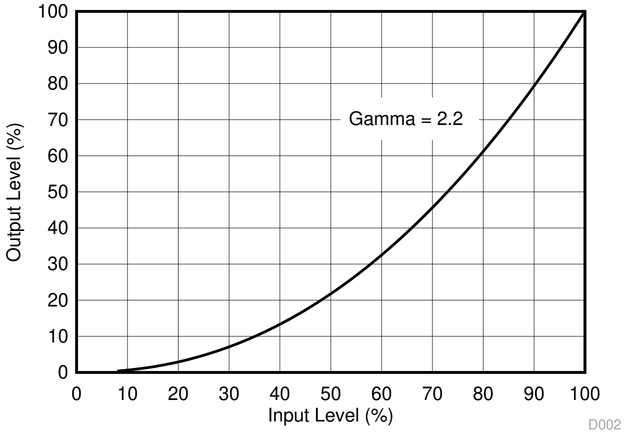


図 6-2. Example of Gamma = 2.2

From 図 6-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The content adaptive illumination control (CAIC) and local area brightness boost (LABB) of the IntelliBright algorithm also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma applied to every pixel of every frame is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3421ZVB controller.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The DMDs are spatial light modulators that reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3421 controller. The new high-tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Applications of interest include projection technology embedded in display devices like ultra low-power battery-operated mobile accessory projectors, phones, tablets, ultra-mobile low-end smart TVs, and virtual assistants.

DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA3000. Refer to *Power Supply Recommendations* for power-up and power-down specifications. To ensure reliable operation, the DLP160CP DMD must always be used with the DLPC3421 display controller and a DLPA200x/DLPA3000 PMIC/LED driver.

7.2 Typical Application

7.2.1 Typical Application—nHD Mode

A common application when using the DLPC34xx controller with the DLP160CP DMD and the DLPA200x PMIC/LED driver is to create a Pico projector embedded in a handheld product. For example, a Pico projector may be embedded in a smartphone, a tablet, or a camera. The controller in the Pico projector embedded module typically receives images from a host processor within the product.

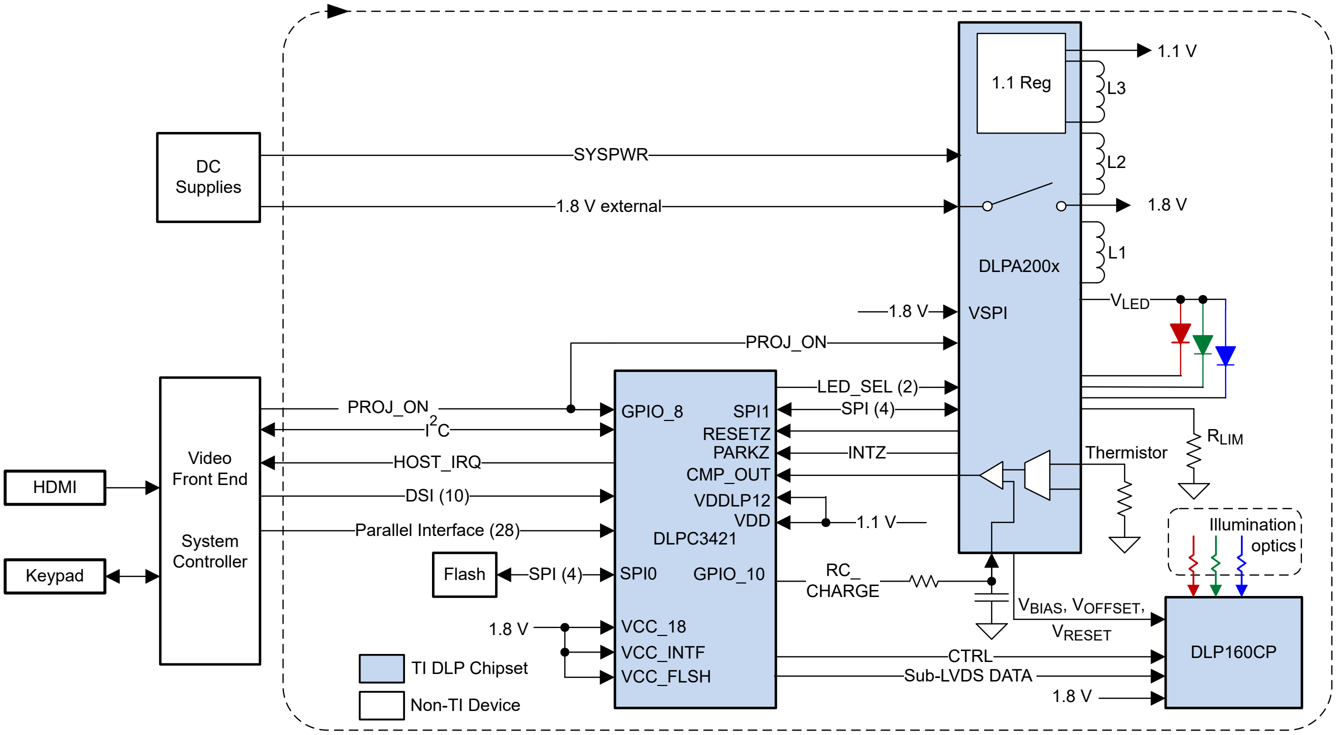


図 7-1. Typical Simplified Application Schematic—nHD Mode (Using DLPA200x)

7.2.2 Typical Application—HD Mode

The DLPC3421 controller when combined with the FPGA and supporting firmware is used to create a Pico projector capable of displaying an HD (1280 × 720) image on screen. The FPGA in the system receives images from the host processor over an FPD-link interface within the product.

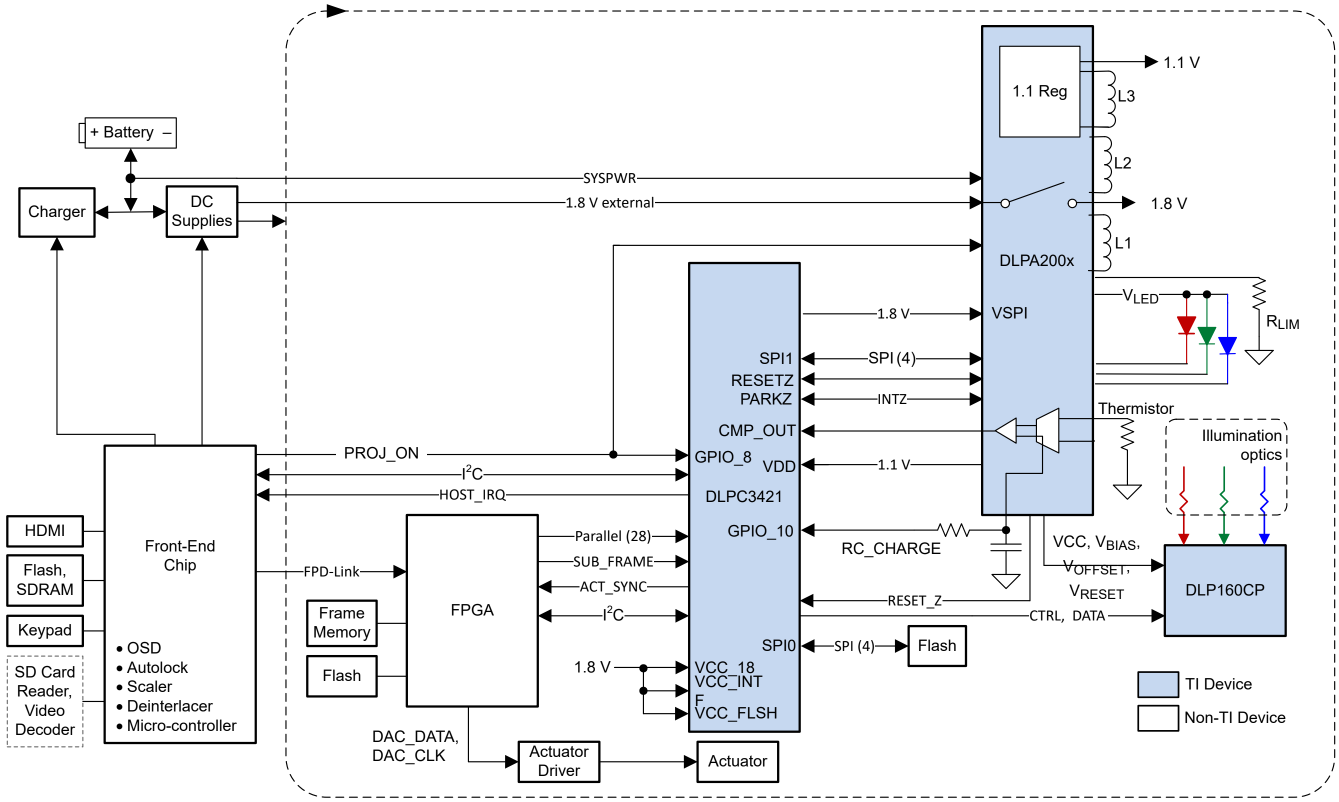


図 7-2. Typical Simplified Application Schematic—HD Mode (Using DLPA200x)

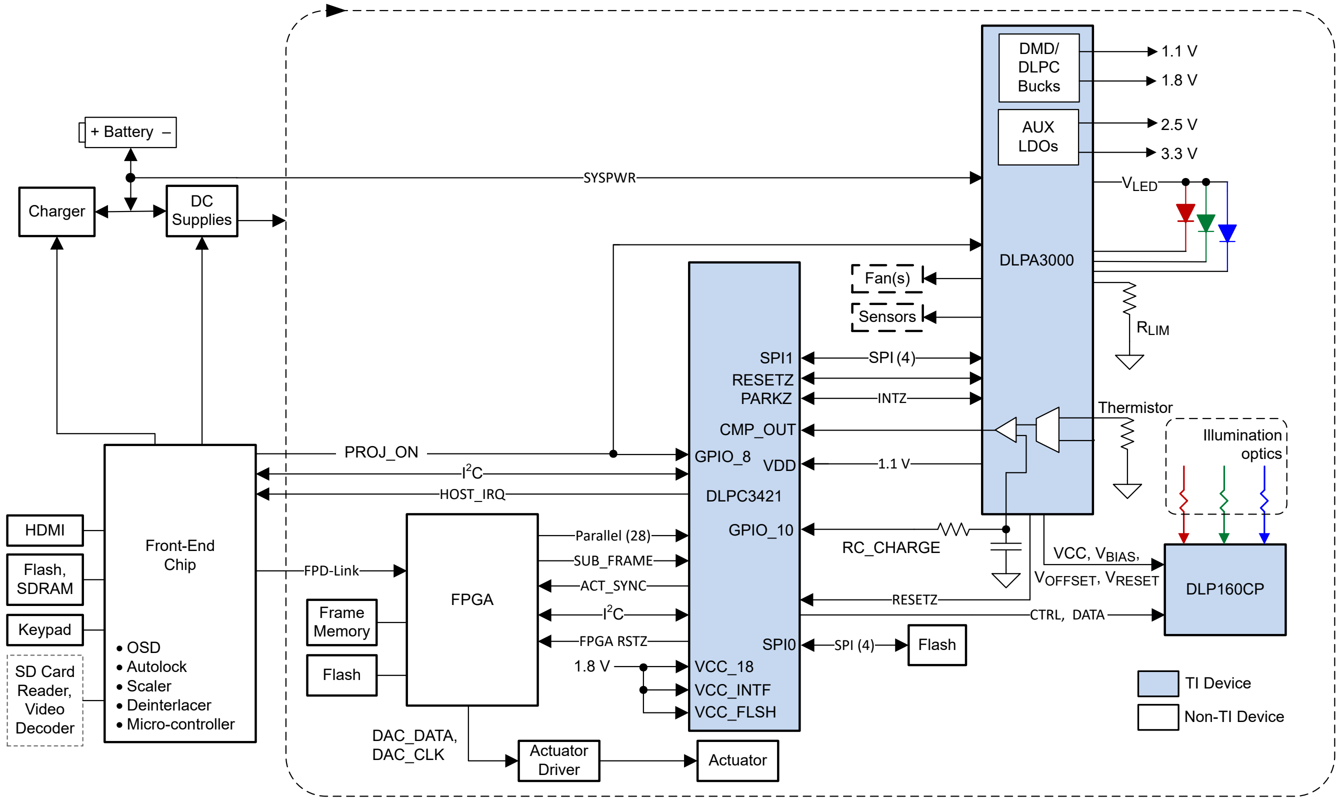


図 7-3. Typical Simplified Application Schematic—HD Mode (Using DLPA3000)

7.2.3 Design Requirements

A pico projector is created by using a DLP chipset comprised of a DLP160CP DMD, a DLPC3421 controller, and a DLPA200x/DLPA3000 PMIC/LED driver. The DLPC3421 controller performs the digital image processing, the DLPA200x/DLPA3000 provides the needed analog functions for the projector, and the DLP160CP DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips are needed. At a minimum, a flash part is needed to store the DLPC3421 controller software.

The illumination light applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico projector.

The DLPC3421 controller receives image data from the multimedia front end over a 24-bit parallel interface. An I^{2}C interface should be connected from the multimedia front end for sending commands to the DLPC3421 controller for configuring the chipset for different features.

7.2.4 Detailed Design Procedure

For instructions on how to connect the DLPC3421 controller, the DLPA200x/DLPA3000, and the DLP160CP DMD together, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

7.2.5 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in 図 7-4. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

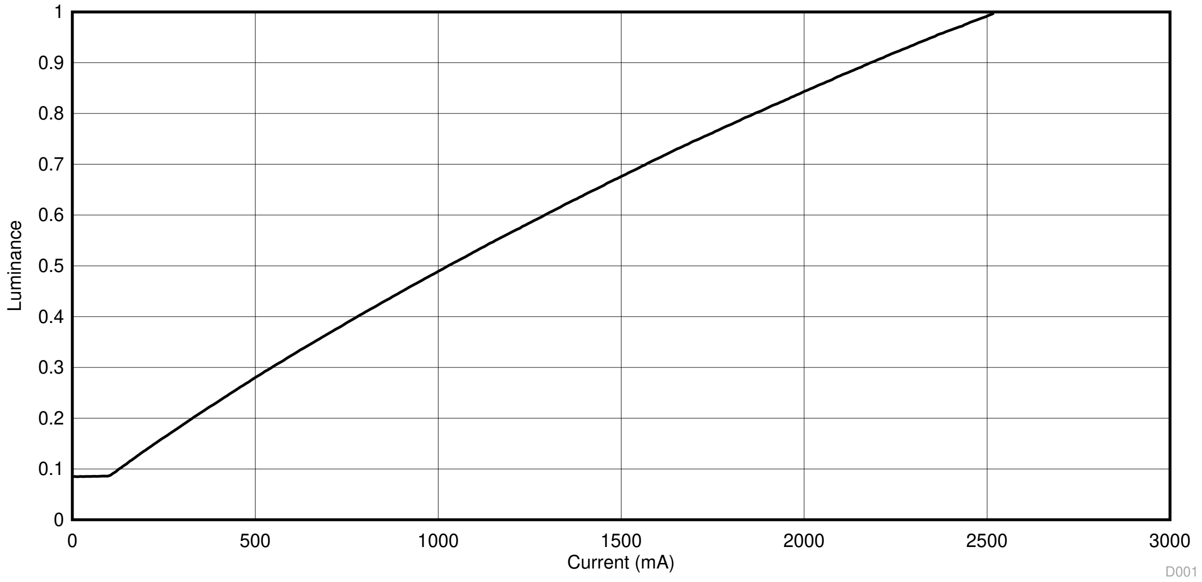


図 7-4. Luminance vs Current

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA3000 devices.

> 注意
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.
>
> V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the reliability and lifetime of the DMD. Refer to the *Power-Up Sequence Delay Requirement*. V_{SS} must also be connected.

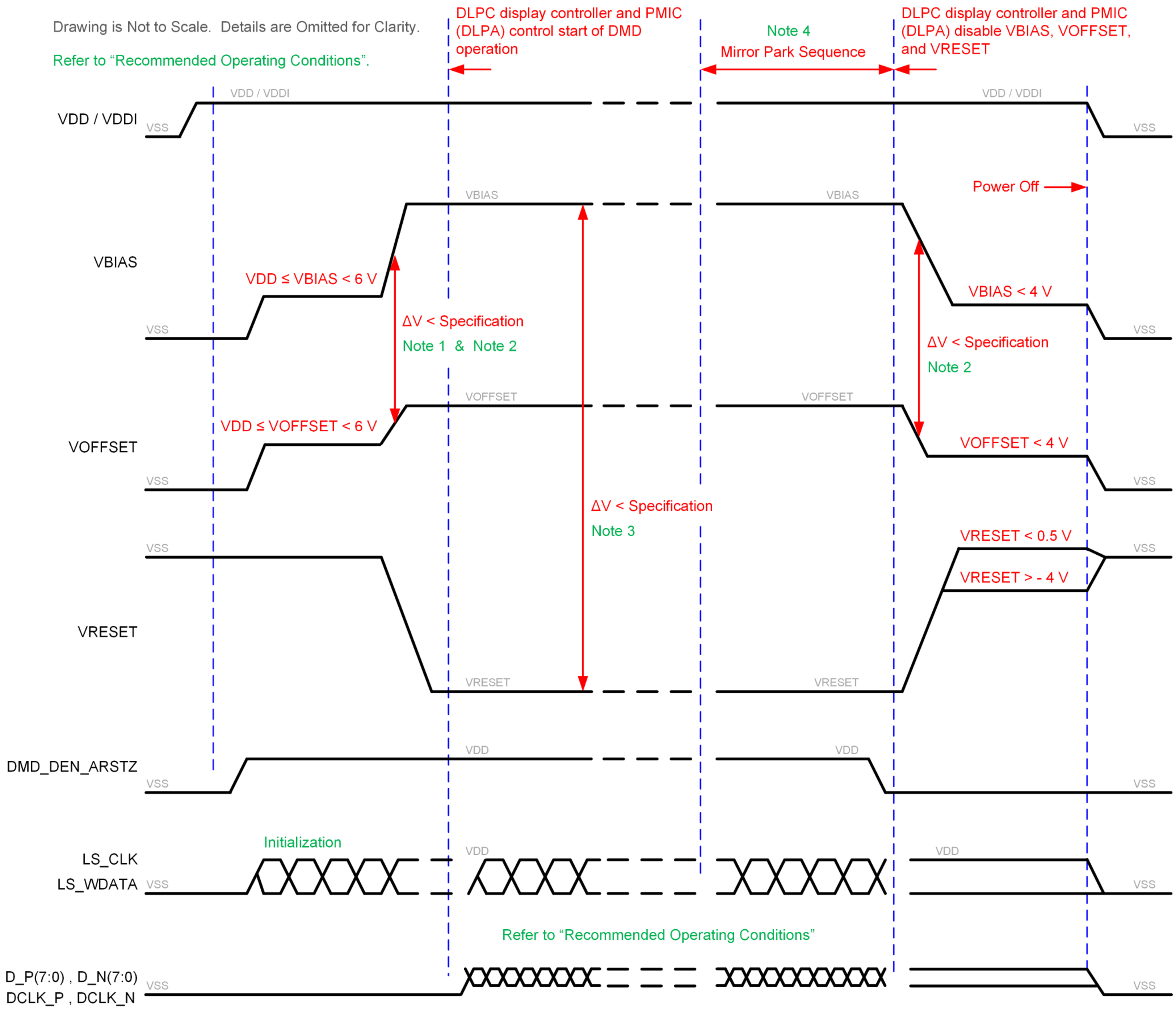
8.1 Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *セクション 5.4*. Refer to Power-Up Sequence Delay Requirement for power-up delay requirements.
- During power-up, the LPSDR input pins of the DMD shall not be driven high until after V_{DD} and V_{DDI} have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in *Power Supply Sequencing Requirements (Power Up and Power Down)*.

8.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4V of ground.
- During power-down, it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *セクション 5.4* (Refer to Note 2 for *Power Supply Sequencing Requirements (Power Up and Power Down)*.
- During power-down, the LPSDR input pins of the DMD must be less than V_{DDI}, the specified limit shown in *セクション 5.4*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in *Power Supply Sequencing Requirements (Power Up and Power Down)*.

8.3 Power Supply Sequencing Requirements



A. Refer to the *Power-Up Sequence Delay Requirement* for critical power-up sequence delay requirements.

B. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in セクション 5.4. OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down. Refer to *Power-Up Sequence Delay Requirement* for power-up delay requirements.

C. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit shown in セクション 5.4.

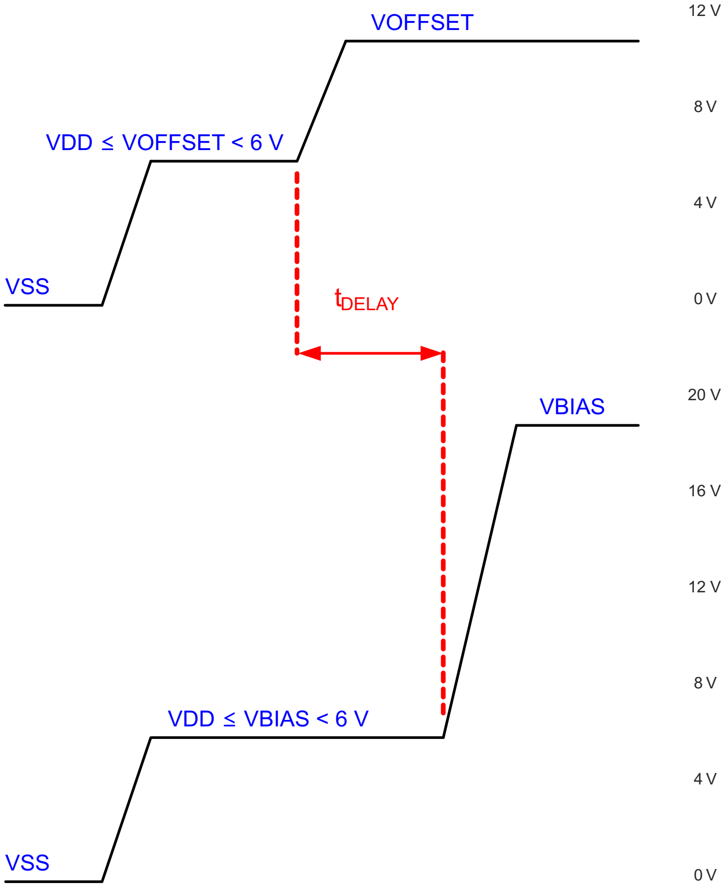
D. When system power is interrupted, the DLPA200x/DLPA3000 initiates hardware power-down that disables V_{BIAS}, V_{RESET}, and V_{OFFSET} after the micromirror park sequence.

E. The drawing is not to scale and details are omitted for clarity.

図 8-1. Power Supply Sequencing Requirements (Power Up and Power Down)

表 8-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from V_{OFFSET} power up to V_{BIAS} power up	2		ms
V_{OFFSET}	The supply voltage level at the beginning of power-up sequence delay		6	V
V_{BIAS}	The supply voltage level at end of power-up sequence delay		6	V



This requirement applies only to the DLPA200x.
Refer to *Power-Up Sequence Delay Requirement* for V_{OFFSET} and V_{BIAS} supply voltage levels during power-up sequence delay.

図 8-2. Power-Up Sequence Delay Requirement

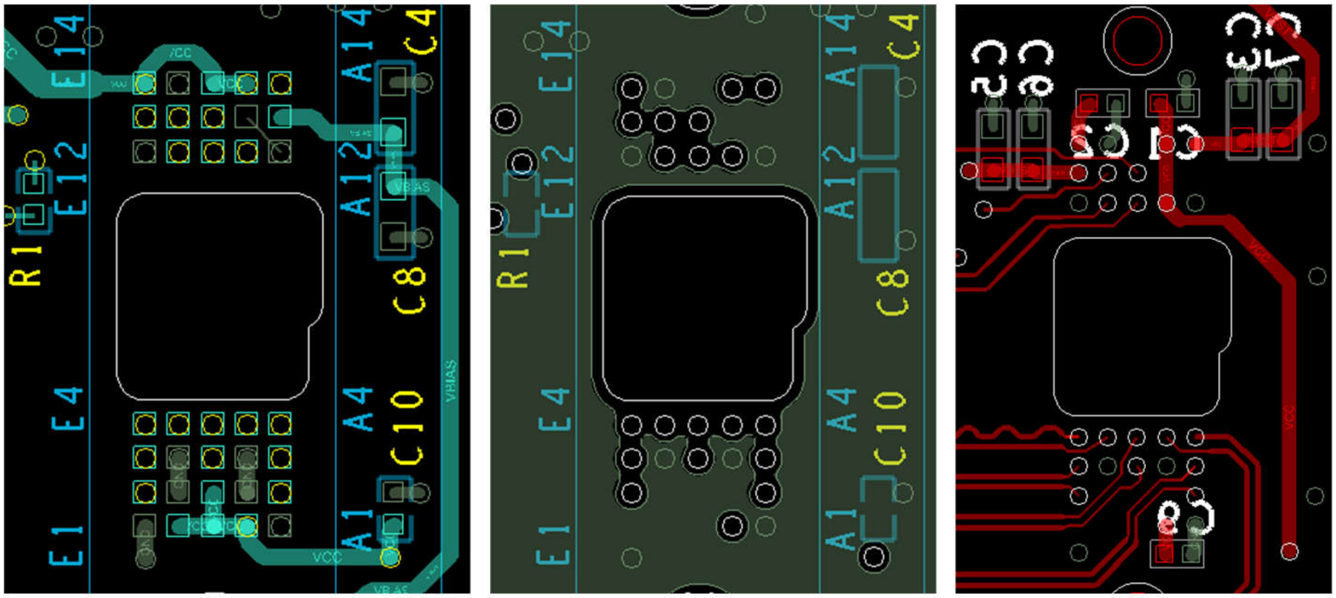
9 Layout

9.1 Layout Guidelines

The DMD is connected to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, and so on. see the DLPC3421 controller data sheet. For a detailed layout example refer to the layout design files. Some layout guidelines for routing to the DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 図 9-1.
- Minimum of two 100nF (25V) capacitors—one close to V_{BIAS} pin. Capacitors C4 and C8 in 図 9-1.
- Minimum of two 100nF (25V) capacitors—one close to each V_{RST} pin. Capacitors C3 and C7 in 図 9-1.
- Minimum of two 220nF (25V) capacitors—one close to each V_{OFS} pin. Capacitors C5 and C6 in 図 9-1.
- Minimum of four 100nF (6.3V) capacitors—two close to the VDD/VDDI pins on each side of the DMD. Capacitors C1, C2, C9, and C10 in the layout example.

9.2 Layout Example



Layer 1 (Top)　Layer 2 (GND)　Layer 3 (Bottom)

図 9-1. Power Supply Connections

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.1.2 Device Nomenclature

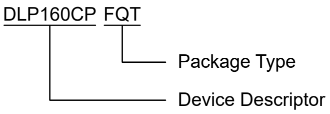
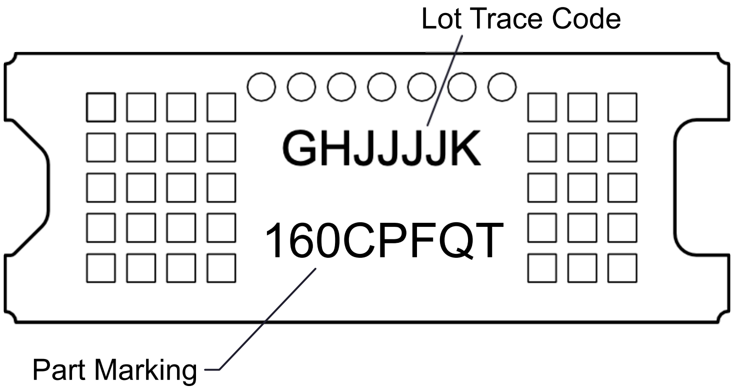


図 10-1. Part Number Description

10.1.3 Device Markings

The device marking includes the legible character string GHJJJJK 160CPFQT. GHJJJJK is the lot trace code. 160CPFQT is the abbreviated part number.

図 10-2. DMD Marking



10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2023) to Revision D (October 2024) **Page**

- 1280 × 720 の解像度の特長を追加 1
- DLP160CP DMD 向けの DLPA3000 サポートを追加 1
- Added a footnote to Micromirror Array Physical Characteristics describing the method of displaying HD resolution 17
- Added DLPA3000 as PMIC 21
- Added DLPA3000 as PMIC 22
- Added DLPA3000 as supported PMIC 30
- Added section to support HD Mode applications 31
- Added note to figure *Power-Up Sequencing Requirements* regarding changes between DLPA200x and DLPA3000 35

Changes from Revision B (May 2022) to Revision C (July 2023) **Page**

- Added section "ILLUMINATION" to *Recommended Operating Conditions* 6
- Updated *Micromirror Array Temperature Calculations* 23
- Added *Micromirror Power Density Calculation* 24

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP160CPFQT	ACTIVE	CLGA	FQT	42	180	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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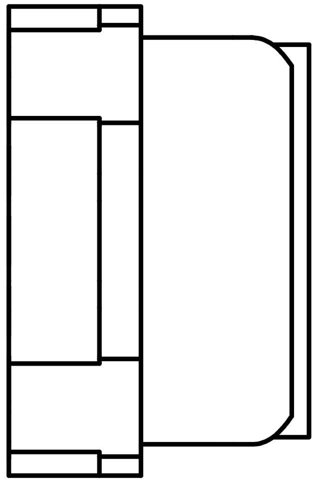
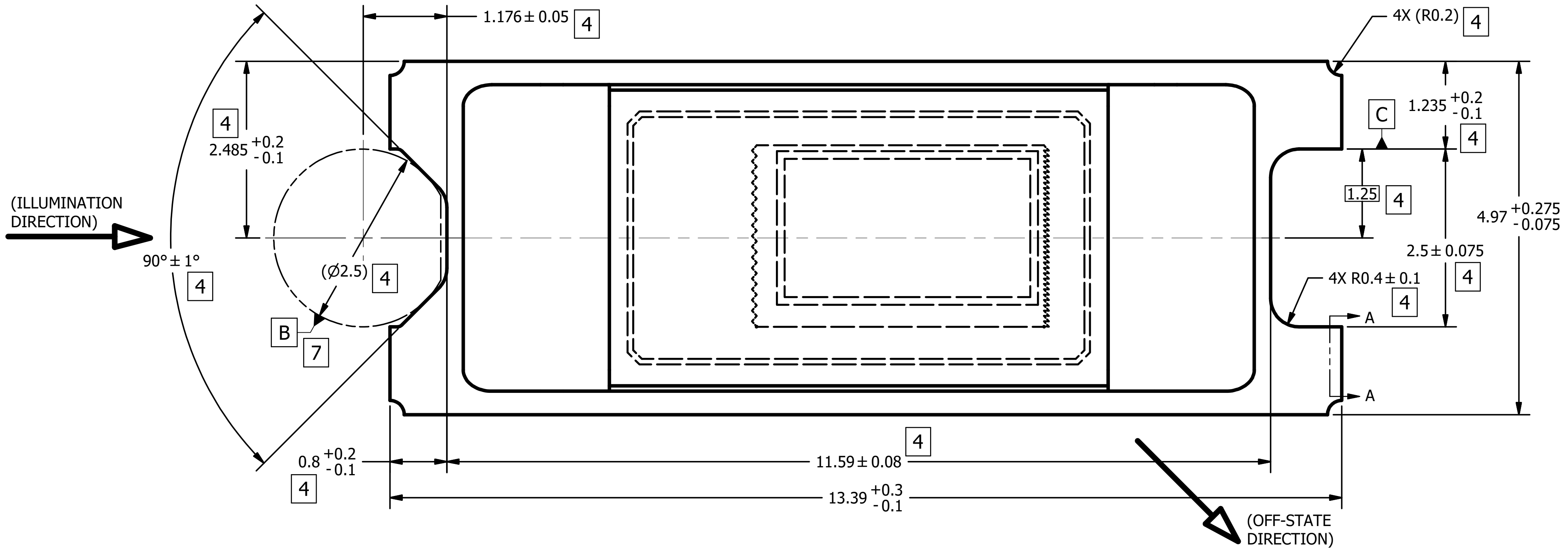
REVISIONS

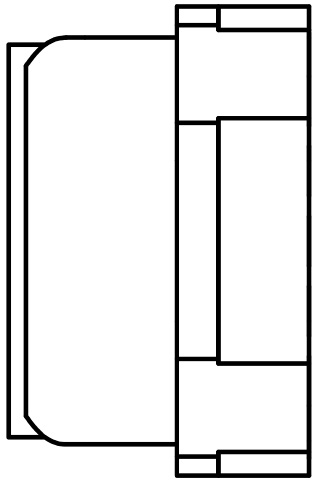
REV	DESCRIPTION	DATE	BY
A	ECO 2191771: INITIAL RELEASE	1/4/2021	BMH

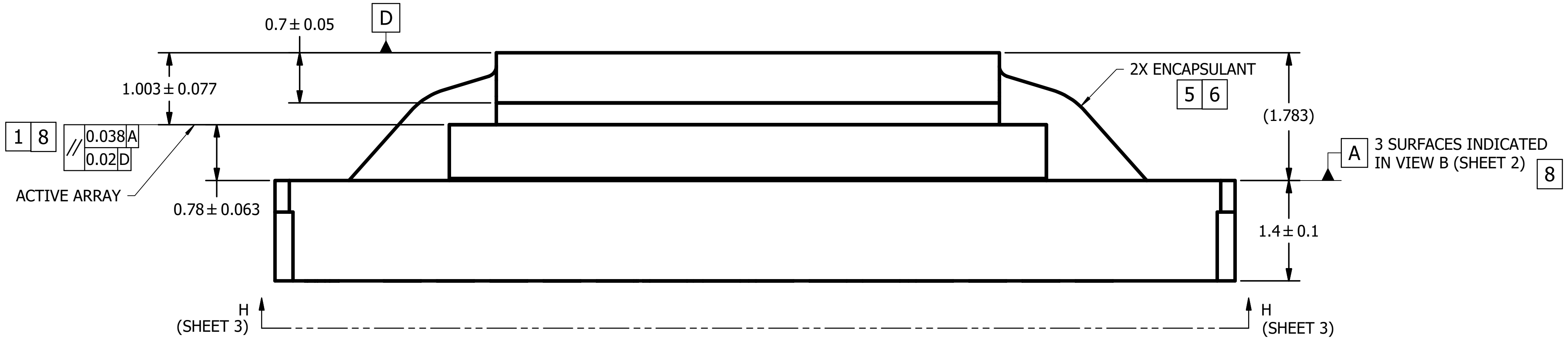
NOTES UNLESS OTHERWISE SPECIFIED:

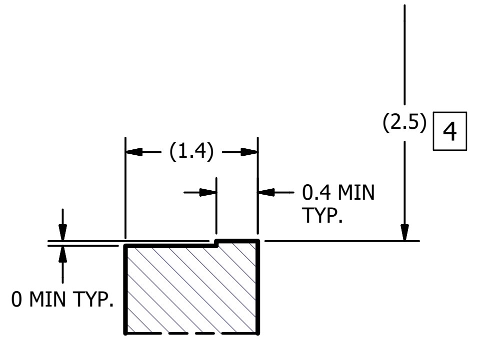
1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.











SECTION A-A
NOTCH OFFSETS

THIRD ANGLE PROJECTION

	0314DA
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	1/4/2021
ENGINEER	B. HASKETT	1/4/2021
QA/CE	C. HART	1/8/2021
CM	F. KHAN	1/4/2021
	G.HERMOSILLO	1/13/2021
APPROVED	J. GRIMMETT	1/11/2021

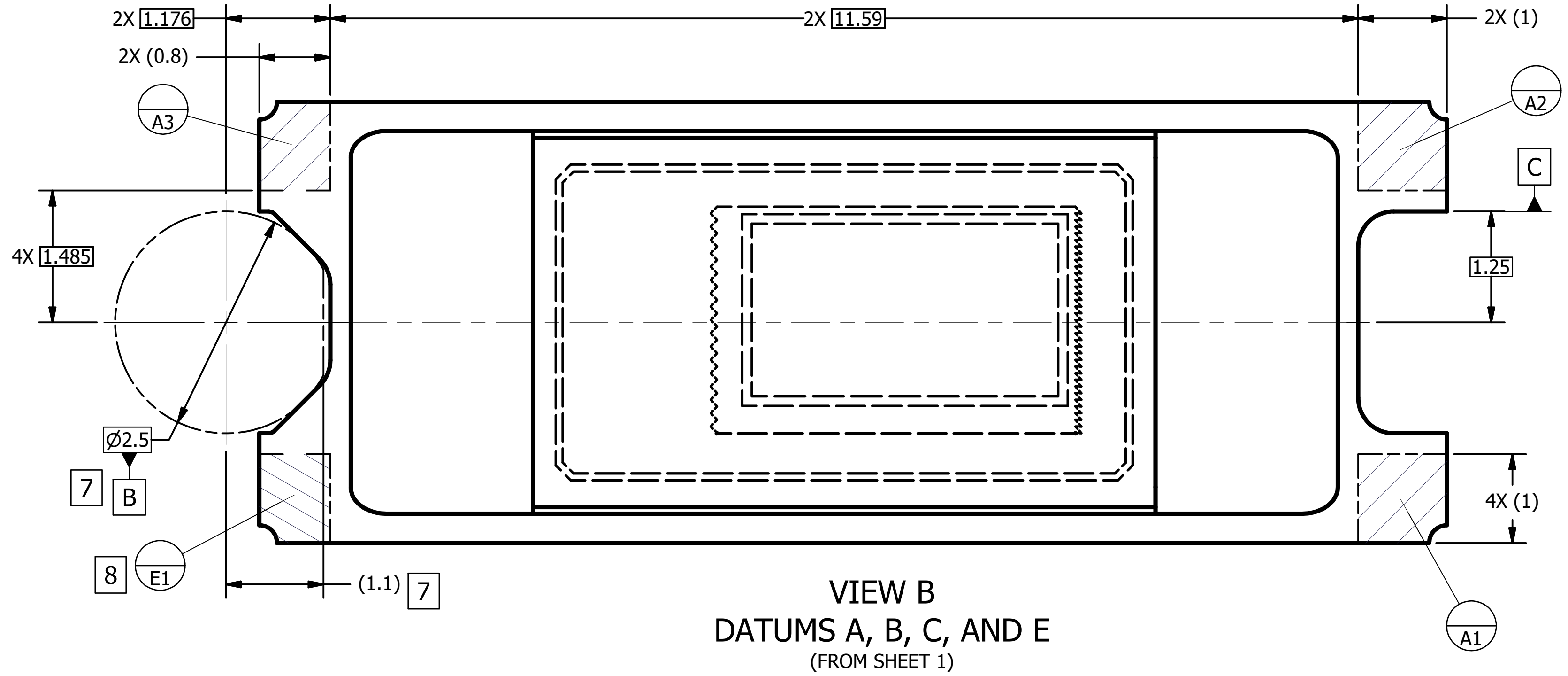
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.16 nHD SERIES 248
(FQT PACKAGE)

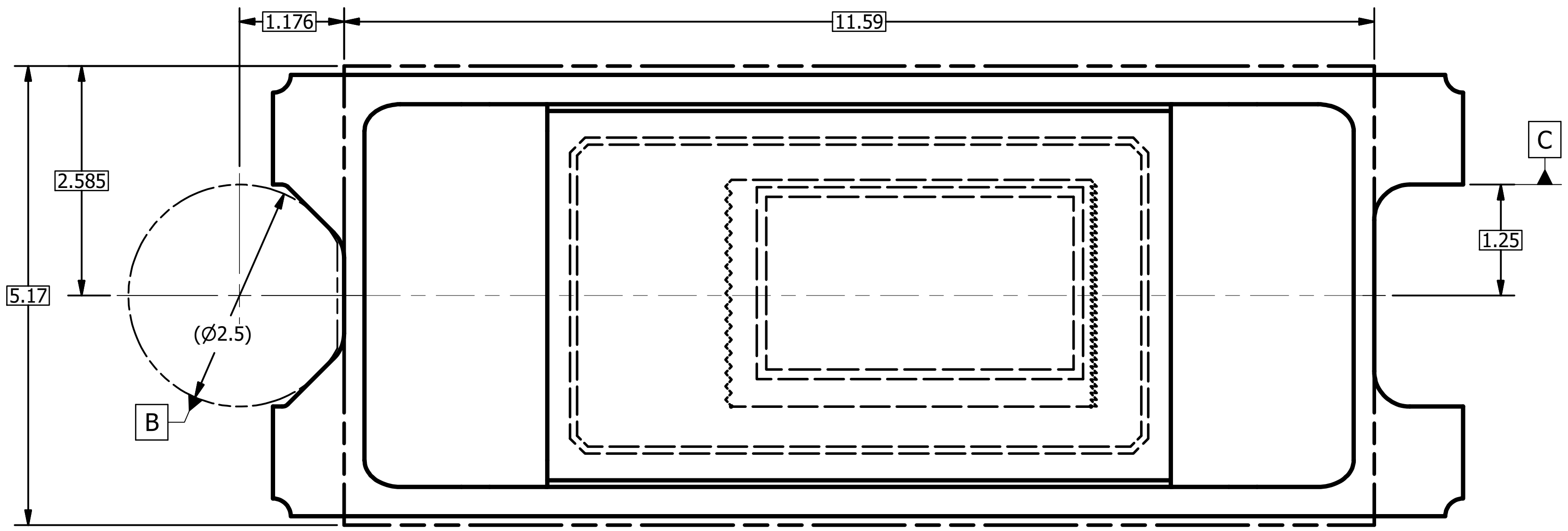
SIZE	DWG NO	REV
D	2517439	A

SCALE 25:1 SHEET 1 OF 3

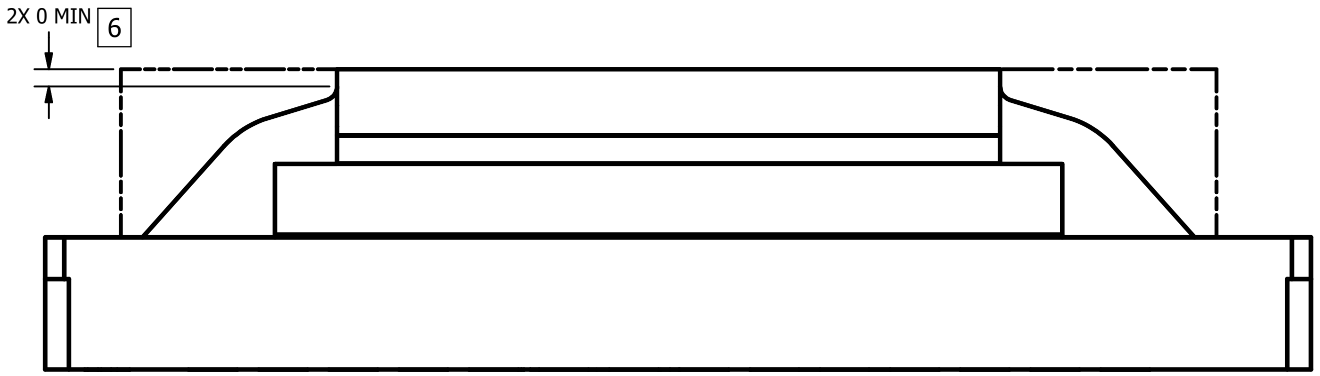
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)

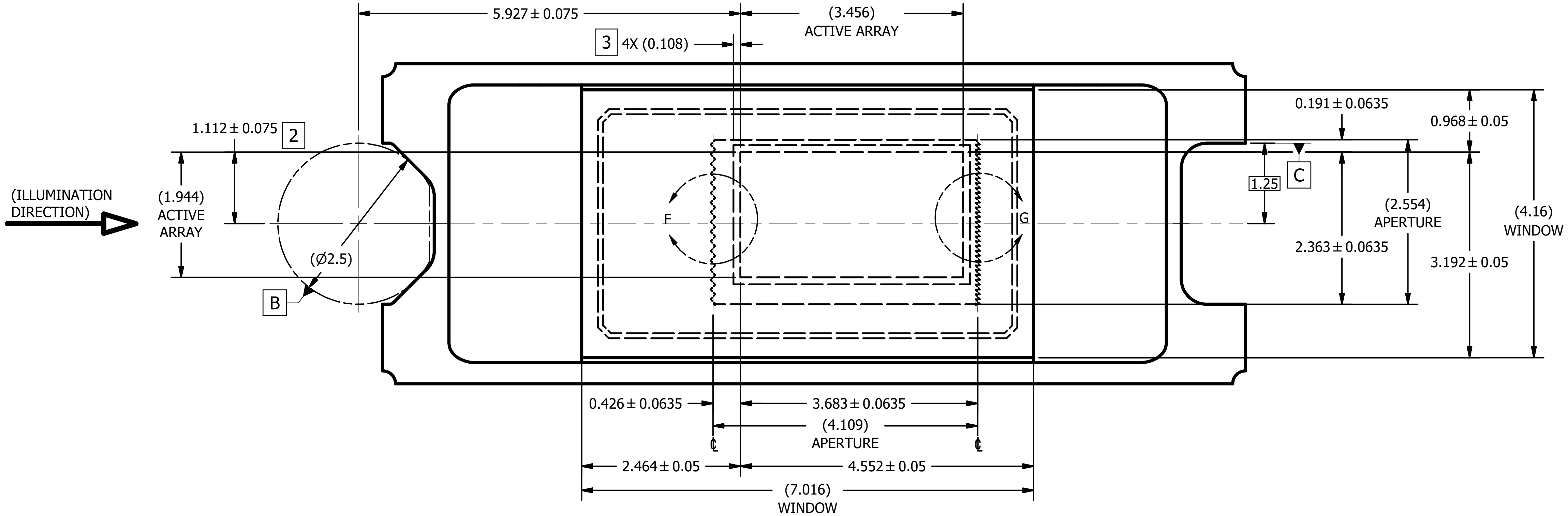


VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
(FROM SHEET 1)

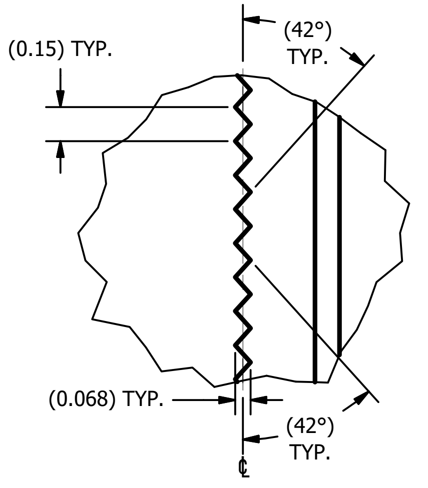


VIEW D
ENCAPSULANT MAXIMUM HEIGHT

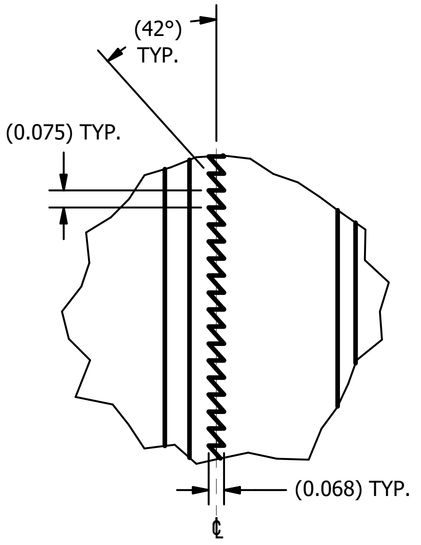
TEXAS INSTRUMENTS
Dallas Texas
DRAWN B. HASKETT
DATE 1/4/2021
SIZE D
DWG NO 2517439
REV A
SCALE
SHEET 2 OF 3



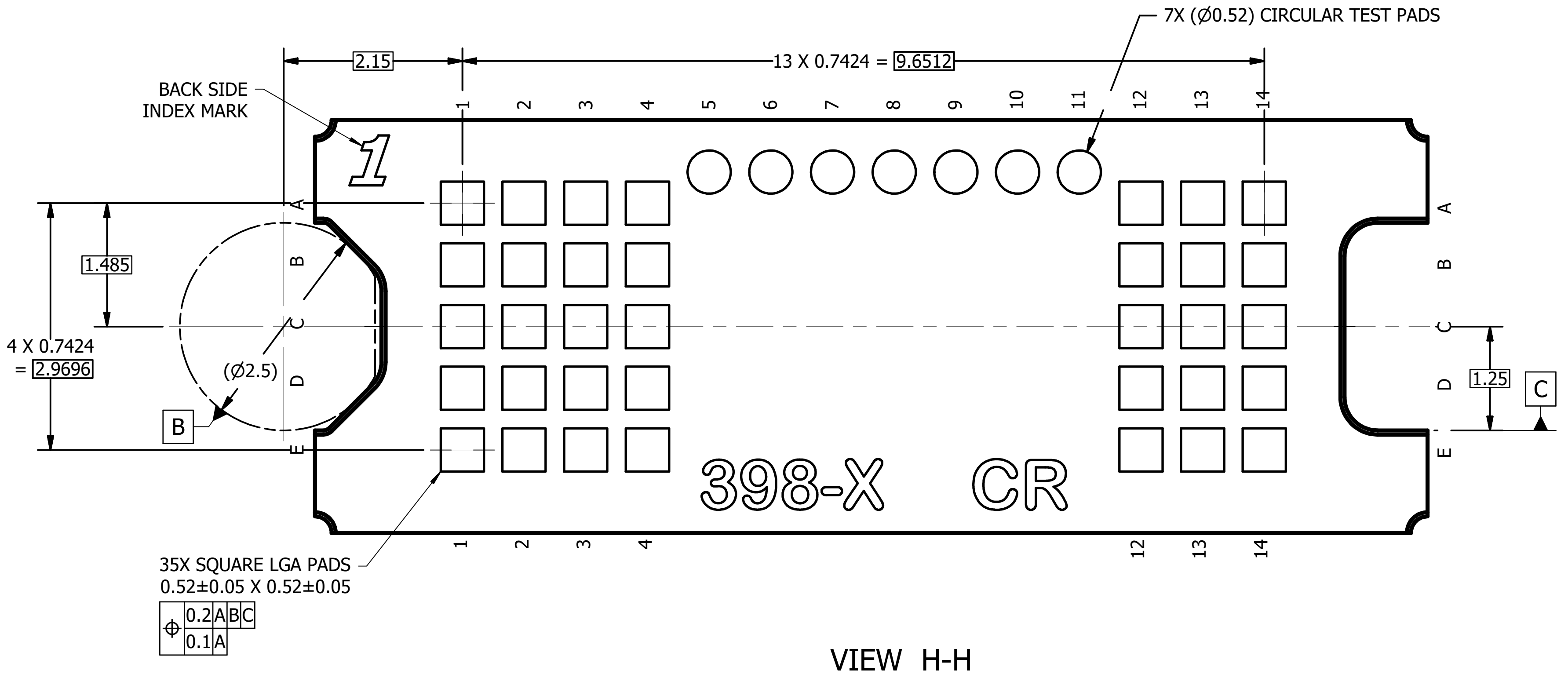
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
(WINDOW OMITTED FOR CLARITY)
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
(WINDOW OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS
Dallas Texas

DRAWN	DATE	SIZE	DWG NO	REV
B. HASKETT	1/4/2021	D	2517439	A
		SCALE	SHEET 3 OF 3	

INV11-2006a

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265