DLP2000 (.2 nHD) DMD

1 特長

- 超小型の 0.2 インチ (5.55mm) 対角マイクロミラー・アレイ
  - マイクロメートル・サイズのアルミ製ミラーを直交に配置した 640 × 360 アレイ
  - マイクロミラー・ピッチ:7.56 ミクロン
  - マイクロミラー傾斜角:12° (平面に対して)
  - コーナー照明による最適な効率と光学エンジン・サイズ
- 専用の DLPC2607 ディスプレイ・コントローラと DLPA1000 PMIC/LED ドライバによる信頼性の高い動作

2 アプリケーション

- 次のような IoT (Internet of Things) デバイス:
  - コントロール・パネル
  - セキュリティ・システム
  - サーモスタット
- ウェアラブル・ディスプレイ
- 次のような製品の組み込みディスプレイ:
  - タブレット
  - カメラ
  - 人工知能 (AI) アシスタント
- マイクロ・デジタル・サイネージ
- 超低消費電力のスマート・アクセサリ・プロジェクタ

3 概要

DLP2000 デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御の MOEMS (micro-opto-electromechanical system) 空間光変調器 (SLM) です。適切な光学システムと組み合わせることで、DLP2000 DMD は鮮明で高-品質の画像または映像を表示できます。DLP2000 は、DLP2000 DMD および DLPC2607 ディスプレイ・コントローラで構成される チップセットの一部です。このチップセットは、DLPA1000 PMIC/LED ドライバでもサポートされています。DLP2000 は小型であるため、a 小さな外形と低消費電力が重視される携帯機器に最適です。小型のパッケージと 小さなサイズの LED により、高効率で堅牢な光エンジンを実現できます。

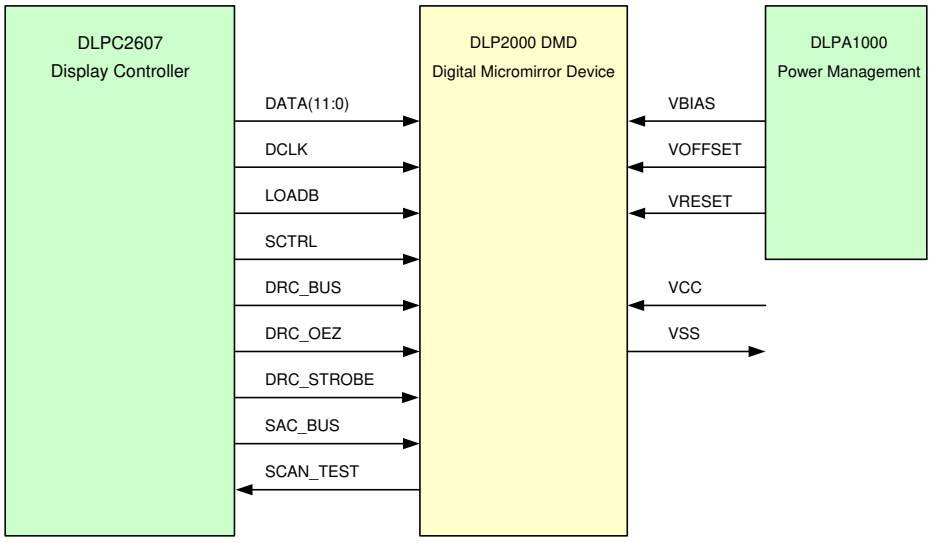
DLP2000 DMD を使用して設計を開始する方法については、「TI DLP®Pico™ ディスプレイ・テクノロジーを使用した設計の開始」ページを参照してください。

DLP2000 には、設計期間の短縮に役立つ定評あるリソースが用意されており、これには量産可能な光モジュール、光モジュール・メーカー、デザイン・ハウスが含まれます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
DLP2000	FQC (42)	14.12mm × 4.97mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2021) to Revision B (May 2022) — **Page**

- このドキュメントは、最新のテキサス・インスツルメンツおよび業界データシート標準に準拠して更新されています。 ... 1
- Updated *Micromirror Array Optical Characteristics* ... 14

Changes from Revision * (April 2019) to Revision A (November 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated $|T_{DELTA}|$ MAX from 30°C to 15°C ... 7

5 Pin Configuration and Functions

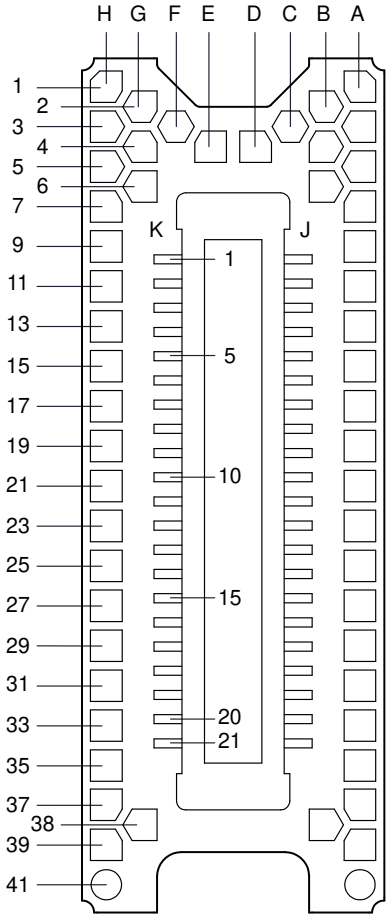


図 5-1. FQC Package 42-Pin LGA Bottom View

表 5-1. Pin Functions

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH (mm)
NAME	NO.					
DATA INPUTS						
DATA(0)	J13	Input	LVCMOS	DDR	Input data bus	8.83
DATA(1)	J2	Input	LVCMOS	DDR	Input data bus	7.53
DATA(2)	J4	Input	LVCMOS	DDR	Input data bus	6.96
DATA(3)	J6	Input	LVCMOS	DDR	Input data bus	7.05
DATA(4)	J7	Input	LVCMOS	DDR	Input data bus	7.56
DATA(5)	J8	Input	LVCMOS	DDR	Input data bus	7.07
DATA(6)	J12	Input	LVCMOS	DDR	Input data bus	7.61
DATA(7)	J10	Input	LVCMOS	DDR	Input data bus	7.68
DATA(8)	K4	Input	LVCMOS	DDR	Input data bus	7.31
DATA(9)	K2	Input	LVCMOS	DDR	Input data bus	6.76
DATA(10)	K7	Input	LVCMOS	DDR	Input data bus	8.18
DATA(11)	K6	Input	LVCMOS	DDR	Input data bus	7.81
DCLK	K9	Input	LVCMOS		Input data clock	7.78
CONTROL INPUTS						
LOADB	K10	Input	LVCMOS	DDR	Parallel latch load enable	7.64

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH (mm)
NAME	NO.					
SCTRL	K12	Input	LVCMOS	DDR	Serial control (sync)	8.62
DRC_BUS	K14	Input	LVCMOS		Reset control serial bus. synchronous to rising edge of DCLK. Bond pad does not connect to internal pull down.	7.28
DRC_OEZ	K18	Input	LVCMOS		Active low. Output enable signal for internal reset driver circuitry. Bond pads do not connect to internal pulldown.	4.69
DRC_STROBE	J15	Input	LVCMOS		Rising edge on DRC_STROBE latches in the control signals. Synchronous to rising edge of DCLK. Bond pad does not connect to internal pulldown.	7.61
SAC_BUS	K16	Input	LVCMOS		Stepped address control serial bus. Synchronous to rising edge of DCLK. Bond pad does not connect to internal pulldown.	8.17
SCAN_TEST	K20	Input	LVCMOS		MUX'ed output for scanned chip ID	1.18
POWER						
VBIAS	J16	Power			Power supply for positive bias level of mirror reset signal	
VOFFSET	K15	Power			Power supply for high voltage CMOS logic. Power supply for stepped high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal	
VRESET	J20	Power			Power supply for negative reset level of mirror reset signal	
VCC	J1	Power			Power supply for low voltage CMOS logic. Power supply for normal high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal during power down	
VCC	J11	Power				
VCC	J21	Power				
VCC	K1	Power				
VCC	K11	Power				
VCC	K21	Power				
VSS	J3	Power			Common return. Ground for all power	
VSS	J5	Power				
VSS	J9	Power				
VSS	J14	Power				
VSS	J17	Power				
VSS	J18	Power				
VSS	J19	Power				
VSS	K3	Power				
VSS	K5	Power				
VSS	K8	Power				
VSS	K13	Power				
VSS	K17	Power				
VSS	K19	Power				

Pin Functions—Test Pads

Electrical Test Pad	DLP® System Board
A1	Do not connect.
A3	Do not connect.
A5	Do not connect.
A7	Do not connect.
A9	Do not connect.
A11	Do not connect.
A13	Do not connect.
A15	Do not connect.
A17	Do not connect.
A19	Do not connect.
A21	Do not connect.
A23	Do not connect.
A25	Do not connect.
A27	Do not connect.
A29	Do not connect.
A31	Do not connect.
A33	Do not connect.
A35	Do not connect.
A37	Do not connect.
A39	Do not connect.
A41	Do not connect.
B2	Do not connect.
B4	Do not connect.
B6	Do not connect.
B38	Do not connect.
C3	Do not connect.
D4	Do not connect.
E4	Do not connect.
F3	Do not connect.
G2	Do not connect.
G4	Do not connect.
G6	Do not connect.
G38	Do not connect.
H1	Do not connect.
H3	Do not connect.
H5	Do not connect.
H7	Do not connect.
H9	Do not connect.
H11	Do not connect.
H13	Do not connect.
H15	Do not connect.
H17	Do not connect.
H19	Do not connect.
H21	Do not connect.
H23	Do not connect.

Pin Functions—Test Pads (continued)

Electrical Test Pad	DLP® System Board
H25	Do not connect.
H27	Do not connect.
H29	Do not connect.
H31	Do not connect.
H33	Do not connect.
H35	Do not connect.
H37	Do not connect.
H39	Do not connect.
H41	Do not connect.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply Voltage	V_{CC}	LVCMOS logic supply voltage(2)	–0.5	4	V
	V_{OFFSET}	Mirror electrode and HVCMOS voltage(2)	–0.5	8.75	V
	V_{BIAS}	Mirror electrode voltage	–0.5	17	V
	$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta(3)		8.75	V
	V_{RESET}	Mirror electrode voltage	–11	0.5	V
Input Voltage	Input voltage: other inputs	See (2).	–0.5	V_{CC} + 0.3	V
Clock Frequency	D_{CLK}	Clock frequency	60	80	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature—operational(4)	–20	90	°C
		Temperature—non-operational(4)	–40	90	°C
	T_{DP}	Dew point temperature—operating and non-operating (non-condensing)		See note(5).	°C
	$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(6)		30	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND (V_{SS}). V_{OFFSET}, V_{CC}, V_{BIAS}, V_{RESET} and V_{SS} power supplies are required for the normal DMD operating mode.
(3) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than 8.75 V.
(4) The highest temperature of the active array (as calculated in セクション 7.6) or of any point along the Window Edge as defined in 図 7-1.
(5) The DLP2000 DMD is intended for use in well controlled, low dew point environments. Please contact your local TI sales person or TI distributor representative to determine if this device is suitable for your application and operating environment compared to other DMD solutions. DLP® Products offers a broad portfolio of DMDs suitable for a wide variety of applications.
(6) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1.

6.2 Storage Conditions

Applicable before the DMD is installed in the final product

			MIN	MAX	UNIT
T_{DMD}	DMD Temperature		–40	85	°C

6.2 Storage Conditions (continued)

Applicable before the DMD is installed in the final product

			MIN	MAX	UNIT
T_{DP}	Dew Point Temperature	(non-condensing)		See Note(1)	°C

(1) The DLP2000 DMD is intended for use in well controlled, low dew point environments. Please contact your local TI sales person or TI distributor representative to determine if this device is suitable for your application and operating environment compared to other DMD solutions. DLP Products offers a broad portfolio of DMDs suitable for a wide variety of applications.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	LVCMOS logic power supply voltage(1)	1.65	1.8	1.95	V
	V_{OFFSET}	Mirror electrode and HVCMOS voltage(1)	8.25	8.5	8.75	V
	V_{BIAS}	Mirror electrode voltage	15.5	16	16.5	V
		Supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ (2)			8.75	V
	V_{RESET}	Mirror electrode voltage	–9.5	–10	–10.5	V
Input Voltage	V_P	Positive going threshold voltage	$0.4*V_{CC}$		$0.7*V_{CC}$	V
	V_N	Negative going threshold voltage	$0.3*V_{CC}$		$0.6*V_{CC}$	V
	V_H	Hysteresis voltage (Vp – Vn)	$0.1*V_{CC}$		$0.4*V_{CC}$	V
Environmental	T_{ARRAY}	Array temperature—long-term operational(3) (4) (5) (6)	0		40 to 70	°C
		Array Temperature – short-term operational(4) (7)	–20		75	°C
	$\lvert T_{DELTA} \rvert$	Absolute temperature difference between any point on the window edge and the ceramic test point TP1(8)			15	°C
	T_{WINDOW}	Window temperature—operational(3) (9)			90	°C
	T_{DP}	Dew point temperature (non-condensing)		See note(10) .		°C
	ILL_{UV}	Illumination wavelength < 400 nm(3)			0.68	mW/cm^2
	ILL_{VIS}	Illumination wavelengths between 400 nm and 700 nm			Thermally limited	
	ILL_{IR}	Illumination wavelength > 700 nm			10	mW/cm^2

(1) All voltage values are with respect to GND (V_{SS}). V_{OFFSET}, V_{CC}, V_{BIAS}, V_{RESET} , and V_{SS} power supplies are required for the normal DMD operating mode.
(2) To prevent excess current, the supply voltage delta $\lvert V_{BIAS} - V_{OFFSET} \rvert$ must be less than 8.75 V.
(3) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination reduces device lifetime.
(4) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-1 and the package thermal resistance in セクション 7.6.
(5) Per 図 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to セクション 7.7 for a definition of micromirror landed duty cycle.
(6) Long-term is defined as the usable life of the device
(7) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours for temperatures between the long-term maximum and 75°C, and less than 500 hours for temperatures between 0°C and –20°C.
(8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1.
(9) Window temperature is the highest temperature on the window edge shown in 図 7-1.
(10) The DLP2000 DMD is intended for use in well controlled, low dew point environments. Please contact your local TI sales person or TI distributor representative to determine if this device is suitable for your application and operating environment compared other DMD solutions. DLP Products offers a broad portfolio of DMDs suitable for a wide variety of applications.

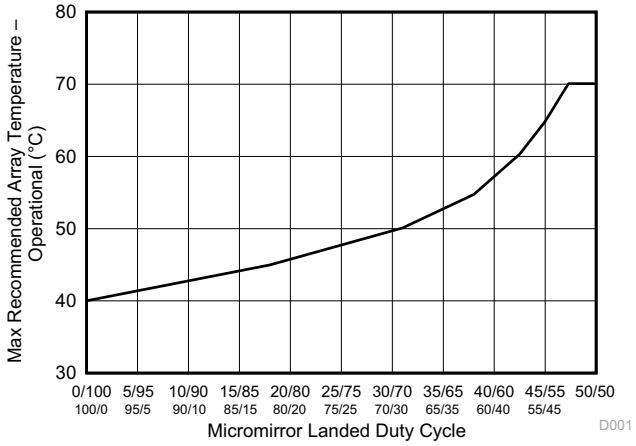


図 6-1. Max Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC(1)	DLP2000 FQC (LGA) 42 PINS	UNIT
Thermal resistance active area to test point 1 (TP1) (1)	8	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in セクション 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	V_{CC} = 1.65 V I_{OH} = –2 mA	1.20			V
V_{OL}	Low level output voltage	V_{CC} = 1.95 V I_{OL} = –2 mA			0.45	V
I_{IL}	Low level input current(1) (2)	V_{CC} = 1.95 V V_I = 0 V			52	nA
I_{IH}	High level input current(1) (2)	V_{CC} = 1.95 V V_I = 1.95 V	41			nA
CURRENT						
I_{CC}	Current at V_{CC} = 1.95 V	D_{CLK} Frequency = 77 MHz			30	mA
I_{OFFSET}	Current at V_{OFFSET} = 8.75 V(3)				1.5	mA
I_{BIAS}	Current at V_{BIAS} = 16.5 V(3) (4)	Three global resets within time period = 200 µs			1.3	mA
I_{RESET}	Current at V_{RESET} = –10.5 V	Three global resets within time period = 200 µs			1.2	mA
POWER						
P_{CC}	Power at V_{CC} = 1.95 V(5)	D_{CLK} Frequency = 77 MHz		26	59	mW
P_{OFFSET}	Power at V_{OFFSET} = 8.75 V(5)			5	13	mW
P_{BIAS}	Power at V_{BIAS} = 16.5 V(5)	Three global resets within time period = 200 µs		9	22	mW
P_{RESET}	Power at V_{RESET} = –10.5 V(5)	Three global resets within time period = 200 µs		4	13	mW
P_{TOTAL}	Supply power dissipation total			44	107	mW
CAPACITANCE						
C_{IN}	Input capacitance	f = 1 MHz			10	pF

6.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(1) Includes LVCMOS pins only
(2) LVCMOS input pins do not have pullup or pulldown configurations.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than 8.75 V.
(4) When DRC_OEZ = high, the internal reset drivers are tri-stated and I_{BIAS} standby current is 3.8 mA.
(5) Nominal values are measured with V_{CC} = 1.8 V, V_{OFFSET} = 8.5 V, V_{BIAS} = 16 V, and V_{RESET} = –10 V.

6.7 Timing Requirements

			MIN	NOM	MAX	UNIT
t_r	Rise time(1)	20% to 80% DCLK			2.5	ns
t_f	Fall time(1)	80% to 20% DCLK			2.5	ns
t_r	Rise time(2)	20% to 80% DATA(11:0), SCTRL, LOADB			2.5	ns
t_f	Fall time(2)	80% to 20% DATA(11:0), SCTRL, LOADB			2.5	ns
t_c	Cycle time(1)	50% to 50% DCLK	12.5		16.67	ns
t_w	Pulse duration(1)	50% to 50% DCLK	5			ns
t_w	Pulse duration low(1)	50% to 50% LOADB	7			ns
t_w	Pulse duration high(1)	50% to 50% DRC_STROBE	7			ns
t_{su}	Setup time(1)	DATA(11:0) before rising or falling edge of DCLK	1			ns
t_{su}	Setup time(1)	SCTRL before rising or falling edge of DCLK	1			ns
t_{su}	Setup time(1)	LOADB low before rising edge of DCLK	1			ns
t_{su}	Setup time(2)	SAC_BUS low before rising edge of DCLK	2			ns
t_{su}	Setup time(2)	DRC_BUS high before rising edge of DCLK	2			ns
t_{su}	Setup time(1)	DRC_STROBE high before rising edge of DCLK	2			ns
t_h	Hold time(1)	DATA(11:0) after rising or falling edge of DCLK	1			ns
t_h	Hold time(1)	SCTRL after rising or falling edge of DCLK	1			ns
t_h	Hold time(1)	LOADB low after falling edge of DCLK	1			ns
t_h	Hold time(2)	SAC_BUS low after rising edge of DCLK	2			ns
t_h	Hold time(2)	DRC_BUS after rising edge of DCLK	2			ns
t_h	Hold time(1)	DRC_STROBE after rising edge of DCLK	2			ns

(1) Refer to 図 6-2 and 図 6-3.
(2) Refer to 図 6-4 and 図 6-5.

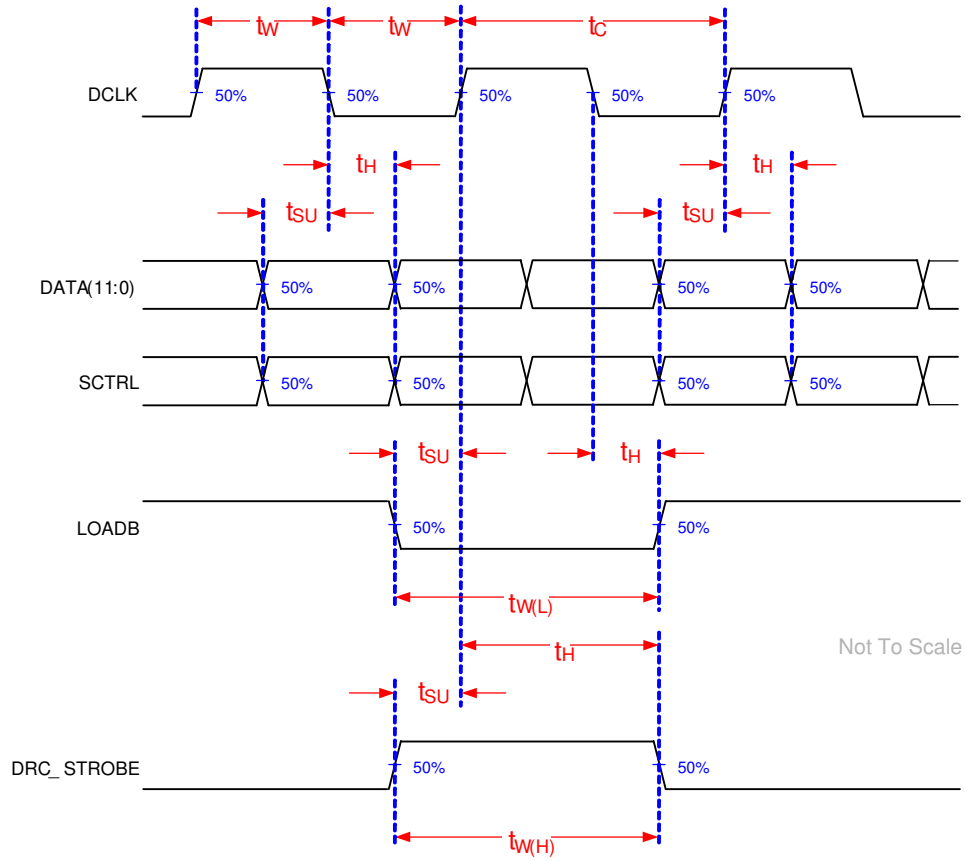


図 6-2. Switching Parameters 1

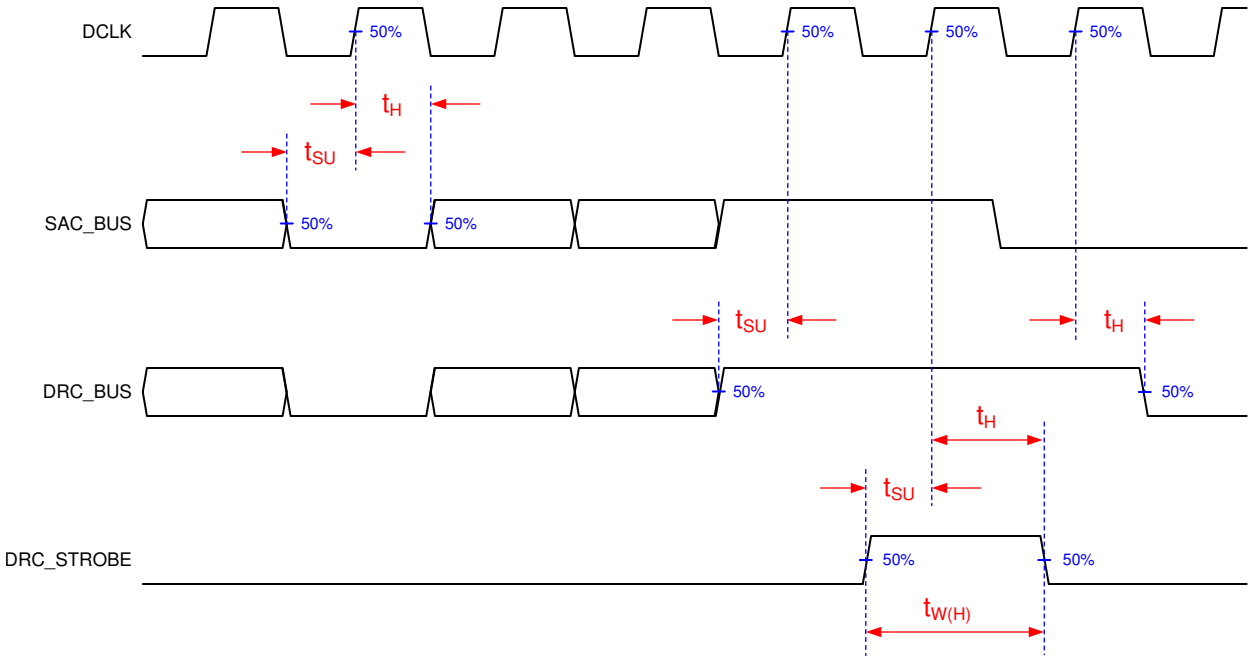


図 6-3. Switching Parameters 2

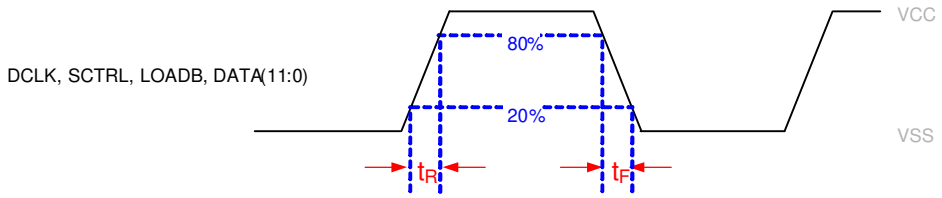


図 6-4. Rise and Fall Timing Parameters 1

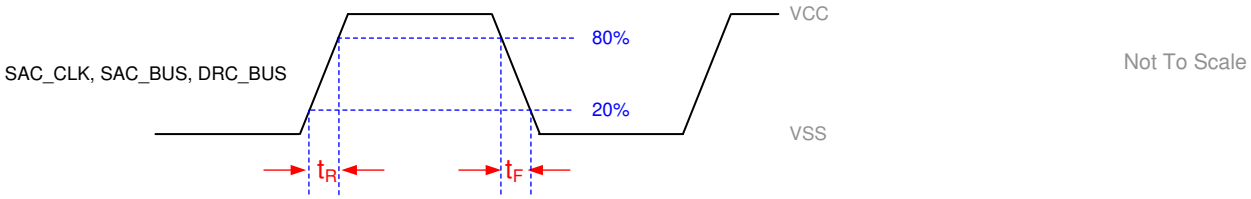


図 6-5. Rise and Fall Timing Parameters 2

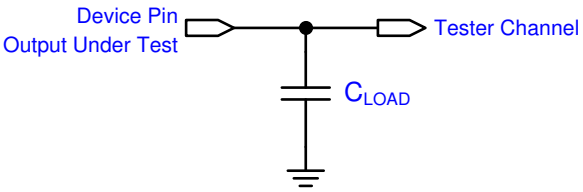


図 6-6. Test Load Circuit

See *セクション 7.3.4* for more information.

6.8 System Mounting Interface Loads

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Connector area (See 図 6-7.)			45	N
	DMD mounting area uniformly distributed over 4 areas (See 図 6-7.)			100	N

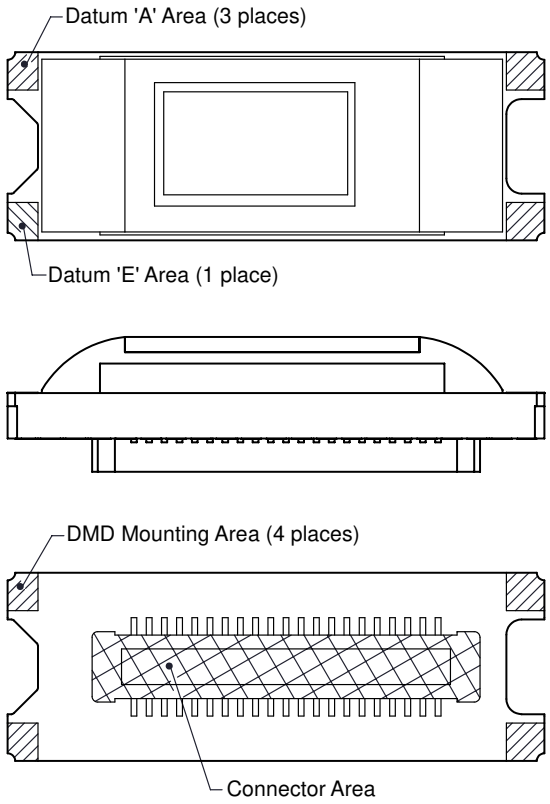
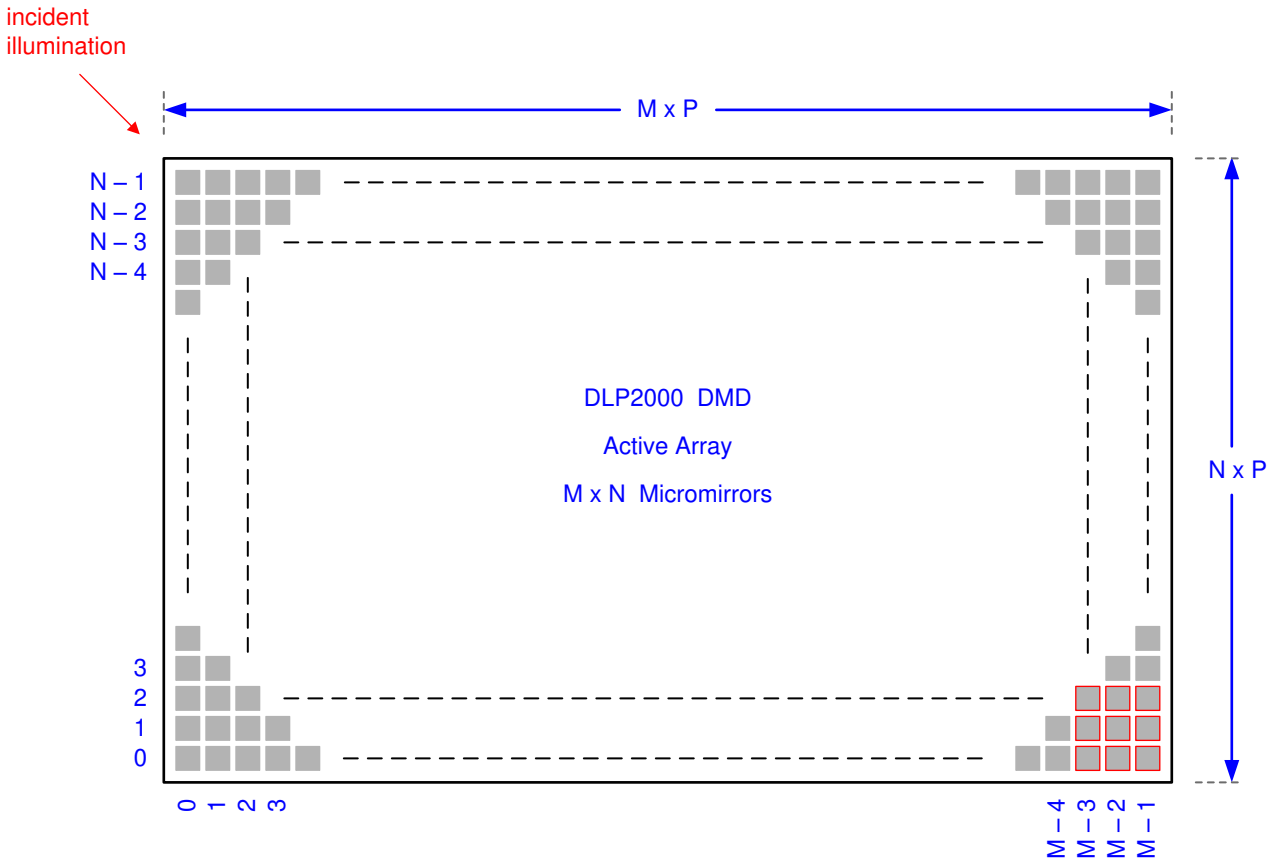


図 6-7. System Interface Loads

6.9 Physical Characteristics of the Micromirror Array

PARAMETER			VALUE	UNIT
M	Number of active columns(1)	See 図 6-8.	640	micromirrors
N	Number of active rows(1)	See 図 6-8.	360	micromirrors
P	Micromirror (pixel) pitch(1)	See 図 6-8.	7.56	µm
	Micromirror active array width(1)	M × P	4.8384	mm
	Micromirror active array height(1)	N × P	2.7216	mm
	Micromirror active border(2) (3)	Pond of micromirrors (POM)	8	micromirrors, side

(1) See 図 6-8.
(2) The structure and qualities of the border around the active array include a band of partially functional micromirrors called the “pond of micromirrors” (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”
(3) Out of the eight POM rows on the top and bottom, only the one POM row closest to the active array is electrically attached to that reset group. The other seven POM rows are attached to a dedicated POM internal reset driver circuit.



Pond Of Micromirrors (POM) omitted for clarity.

Details omitted for clarity.

Not to scale.

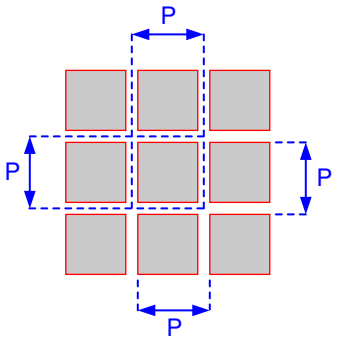


図 6-8. Micromirror Array Physical Characteristics

6.10 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt—half angle, variation device to device (1)			11	12	13	°
Axis of rotation with respect to system datums, variation device to device(2)			44	45	46	°
Image performance(3)	Bright pixel(s) in active area(4)	Gray 10 screen(5)			0	micromirrors
	Bright pixel(s) in the POM(6)	Gray 10 screen(5)			1	
	Dark pixel(s) in the active area(7)	White screen			4	
	Adjacent pixel(s)(8)	Any screen			0	
	Unstable pixel(s) in active area(9)	Any screen			0	

(1) Limits on variability of micromirror tilt half angle are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetry and system contrast variations. The specified limits represent the tolerances of the tilt angles within a device.
(2) See 図 6-9.
(3) Conditions of acceptance: All DMD image quality returns are evaluated using the following projected image test conditions:
Test set degamma should be linear.
Test set brightness and contrast should be set to nominal.
The diagonal size of the projected image should be a minimum of 20 inches.
The projections screen should be 1X gain.
The projected image should be inspected from a 38-inch minimum viewing distance.
The image should be in focus during all image quality tests.
(4) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(5) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(6) POM definition: Rectangular border of off-state mirrors surrounding the active area
(7) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(8) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(9) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

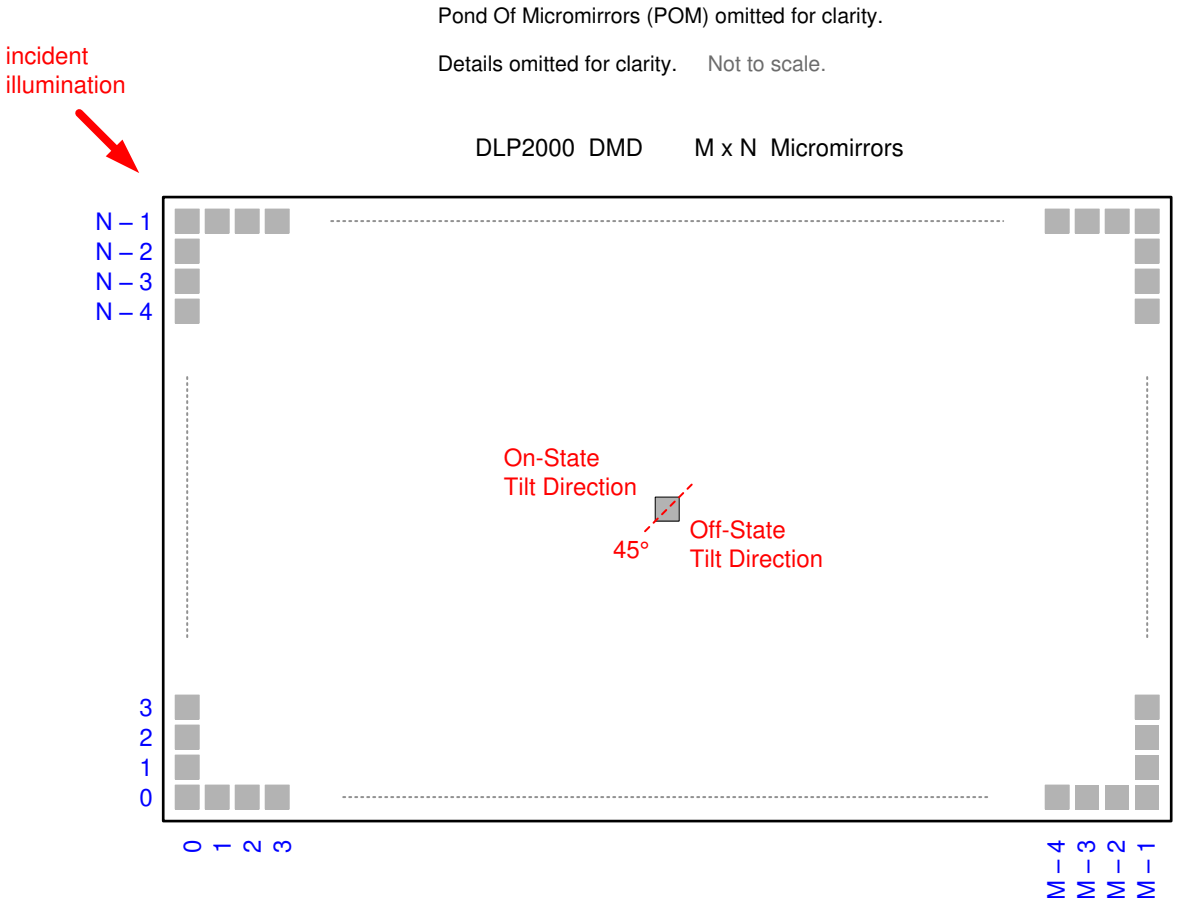


図 6-9. Landed Pixel Orientation and Tilt

See セクション 6.9 for M and N specifications.

6.11 Window Characteristics

表 6-1. DMD Window Characteristics

PARAMETER	VALUE	UNIT
Window Material	Corning Eagle XG	
Window Refractive Index at wavelength 546.1 nm	1.5119	
Window Transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0–30° AOI. (1) (2)	97%	
Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30–45° AOI. (1) (2)	97%	

(1) Single-pass through both surfaces and glass.
(2) AOI – Angle Of Incidence is the angle between an incident ray and the normal of a reflecting or refracting surface.

6.12 Chipset Component Usage Specification

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP2000 is a component of one or more DLP chipsets. Reliable function and operation of the DLP2000 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

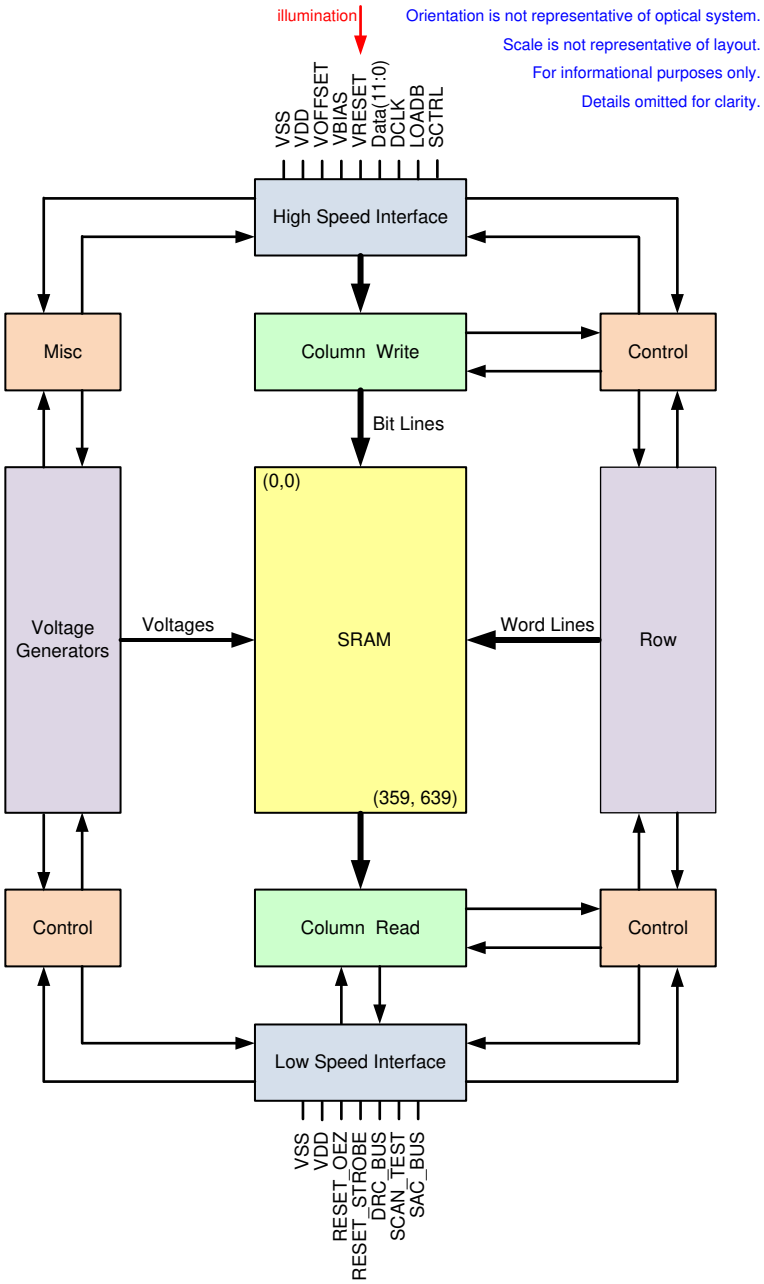
7 Detailed Description

7.1 Overview

The DLP2000 is a 0.2-inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 640 columns by 360 rows in a square grid pixel arrangement. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is a Double Data Rate (DDR) input data bus.

The DLP2000 is part of the chipset that includes the DLP2000 DMD, the DLPC2607 display controller, and the DLPA1000 PMIC/LED driver. To ensure optimal performance, the DLP2000 DMD should be used with the DLPC2607 display controller and the DLPA1000 PMIC/LED driver.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Interface

For the DLP2000 DMD, the power management IC is the DLPA1000. This driver contains three regulated DC supplies for the DMD reset circuitry: V_{BIAS}, V_{RESET}, and V_{OFFSET}.

7.3.2 Control Serial Interface

The control serial interface handles instructions that configure the DMD and control reset operation. DRC_BUS is the reset control serial bus, DRC_OEZ is the active low, output enable signal for internal reset driver circuitry, DRC_STROBE rising edge latches in the control signals, and SAC_BUS is the stepped address control serial bus.

7.3.3 High Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high speed interface is composed of LVCMOS signal receivers for inputs and a dedicated clock.

7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 6-6 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *セクション 8* section.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC2607 controller. See the DLPC2607 controller data sheet or contact a TI applications engineer.

7.5 Window Characteristics and Optics

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous components and system design parameters. Optimizing system optical performance and image quality strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance depends on compliance with the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.1.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border as well as the active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features surrounding the active array and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere outside more than 20 pixels from the edge of the active array on all sides. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the outside of the active array may still cause artifacts to still be visible.

7.6 Micromirror Array Temperature Calculation

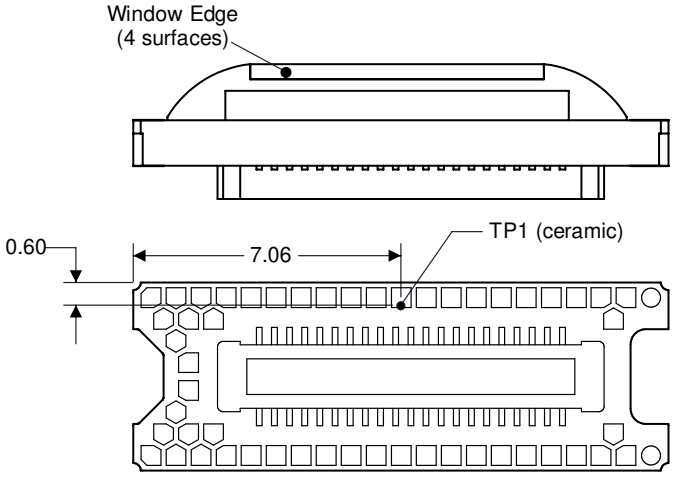


図 7-1. DMD Thermal Test Point

The micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in 図 7-1
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W), specified in *セクション 6.5*
- Q_{ARRAY} = Total DMD power; electrical plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm)
- SL = Measured ANSI screen lumens (lm)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.045 watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. The equations shown previously are valid for a 1-Chip DMD system with a total projection efficiency from DMD to screen of 87%.

The conversion constant C_{L2W} is based on DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light, and an illumination distribution of 83.7% on the DMD active

array and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00293 W/lm.

The following is a sample calculation for a typical projection application:

- SL = 20 lm
- $T_{Ceramic}$ = 55°C
- $Q_{Array} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$ = 0.045 W + (0.00293 W/lm × 20 lm) = 0.1036 W
- T_{Array} = 55°C + (0.1036 W × 8°C/W) = 55.8°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the On state 75% of the time (and in the Off state 25% of the time), whereas 25/75 would indicate that the pixel is in the On state 25% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (4)$$

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in 表 7-2.

表 7-2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

Note

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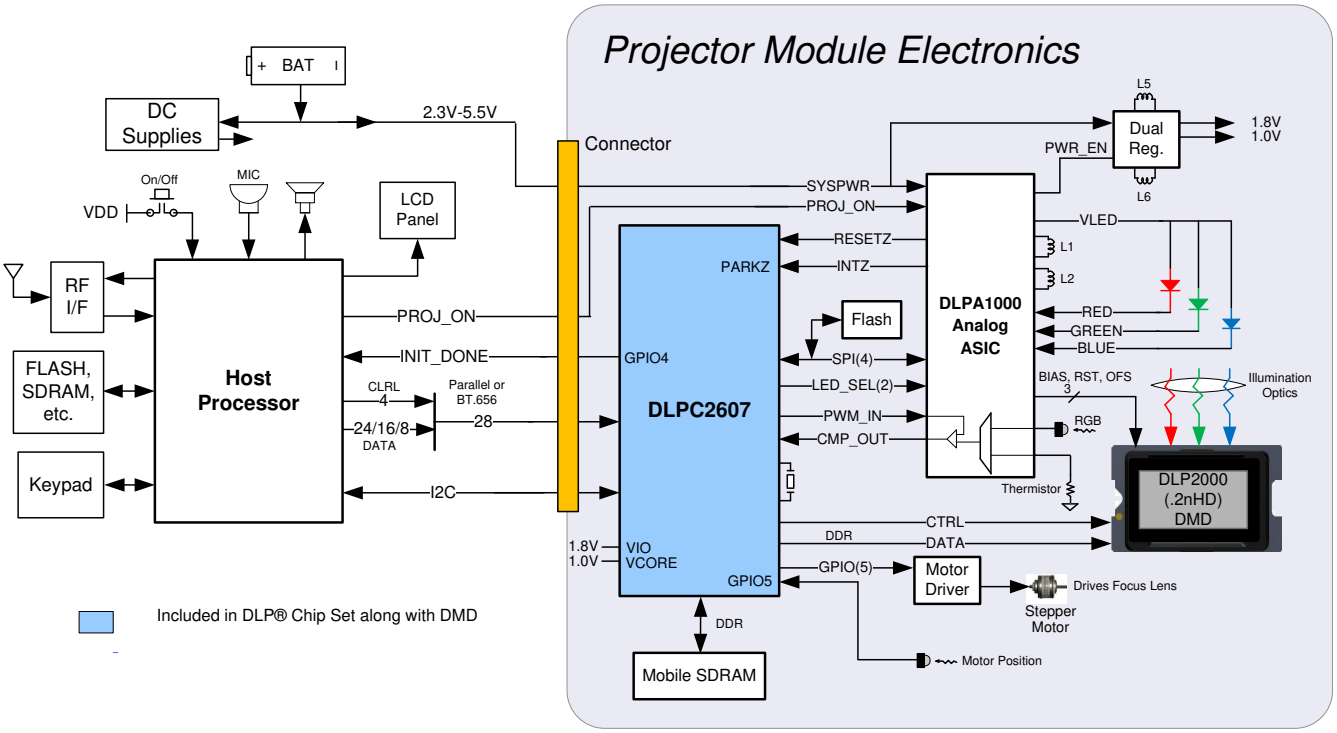
8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into projection or collection optics. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the the DLPC2607 controller. Applications of interest include internet of things (IoT) devices such as control panels, and security systems and thermostats, as well as projection embedded in display applications like smartphones, tablets, cameras, and artificial intelligence (AI) assistance. Other applications include wearable (near-eye) displays, micro digital signage, and ultra-low power smart accessory projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLPA1000. Refer to セクション 9 for power-up and power-down specifications. The DLP2000 DMD reliability is only specified when used with the DLPC2607 controller and the DLPA1000 PMIC/LED Driver.

8.2 Typical Application

A common application for the DLP2000 chipset is creating a pico-projector embedded in a handheld product. For example, a pico-projector embedded in a smart phone, camera, battery powered mobile accessory, micro digital signage or IoT application. The DLPC2607 controller in the pico-projector receives images from a multimedia front end within the product as shown below.



8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of the DLP2000 DMD, a DLPC2607 controller, and a DLPA1000 PMIC/LED driver. The DLPC2607 controller does the digital image processing, the DLPA1000

provides the needed analog functions for the projector, and the DLP2000 DMD is the display device producing the projected image.

In addition to the three DLP chips in the chipset, other chips may be needed. This includes a Flash part needed to store the software and firmware for controlling the DLPC2607 controller.

The illumination that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

When connecting the DLPC2607 controller to the multimedia front end to receive images, a parallel interface is used. When using the parallel interface, the I^2C should be connected to the multimedia front end to send commands to the DLPC2607 controller and configure the DLPC2607 controller for different features.

8.2.2 Detailed Design Procedure

To connect the DLPC2607 controller, the DLPA1000, and the DLP2000 DMD, see the reference design schematic. A small circuit board layout is possible when using this schematic. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector. An optical OEM who specializes in designing optics for DLP projectors typically supplies the optical engine that has the LED packages and the DMD mounted on it.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in 図 8-1. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

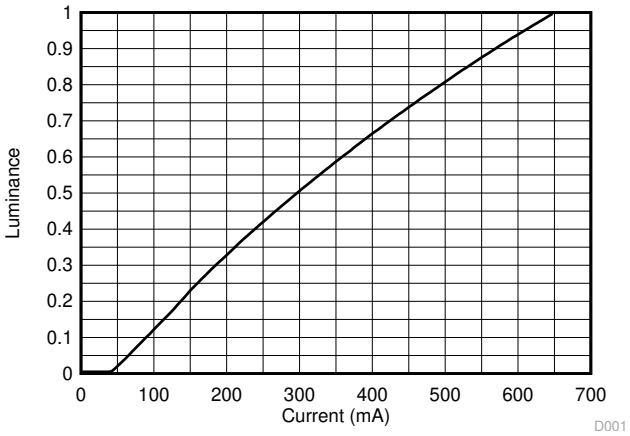


図 8-1. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{SS}, V_{CC}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. DMD power-up and power-down sequencing is strictly controlled by the DLPA1000 device.

V_{CC}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the following requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to 図 9-1.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

V_{CC}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the following requirements will result in a significant reduction in the DMD's reliability and lifetime.

9.1 Power Supply Power-Up Procedure

- During Power-Up, V_{CC} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During Power-Up, V_{BIAS} does not have to start after V_{OFFSET}. However, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (Note 1).
- During Power-Up, the DMD's LVCMOS input pins shall not be driven high until after V_{CC} has settled at operating voltage.
- During Power-Up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Slew Rates for Power-Up are flexible, as long as the transient voltage levels follow the requirements listed previously.

9.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. V_{CC} must be supplied until after V_{BIAS}, V_{RESET} and V_{OFFSET} are discharged to within 4 V of ground.
- During Power-Down, it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (Note 1).
- During power-down, the DMD's LVCMOS input pins must be less than V_{CC} + 0.3 V.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Slew rates for power-down are flexible, as long as the transient voltage levels follow the requirements listed previously.

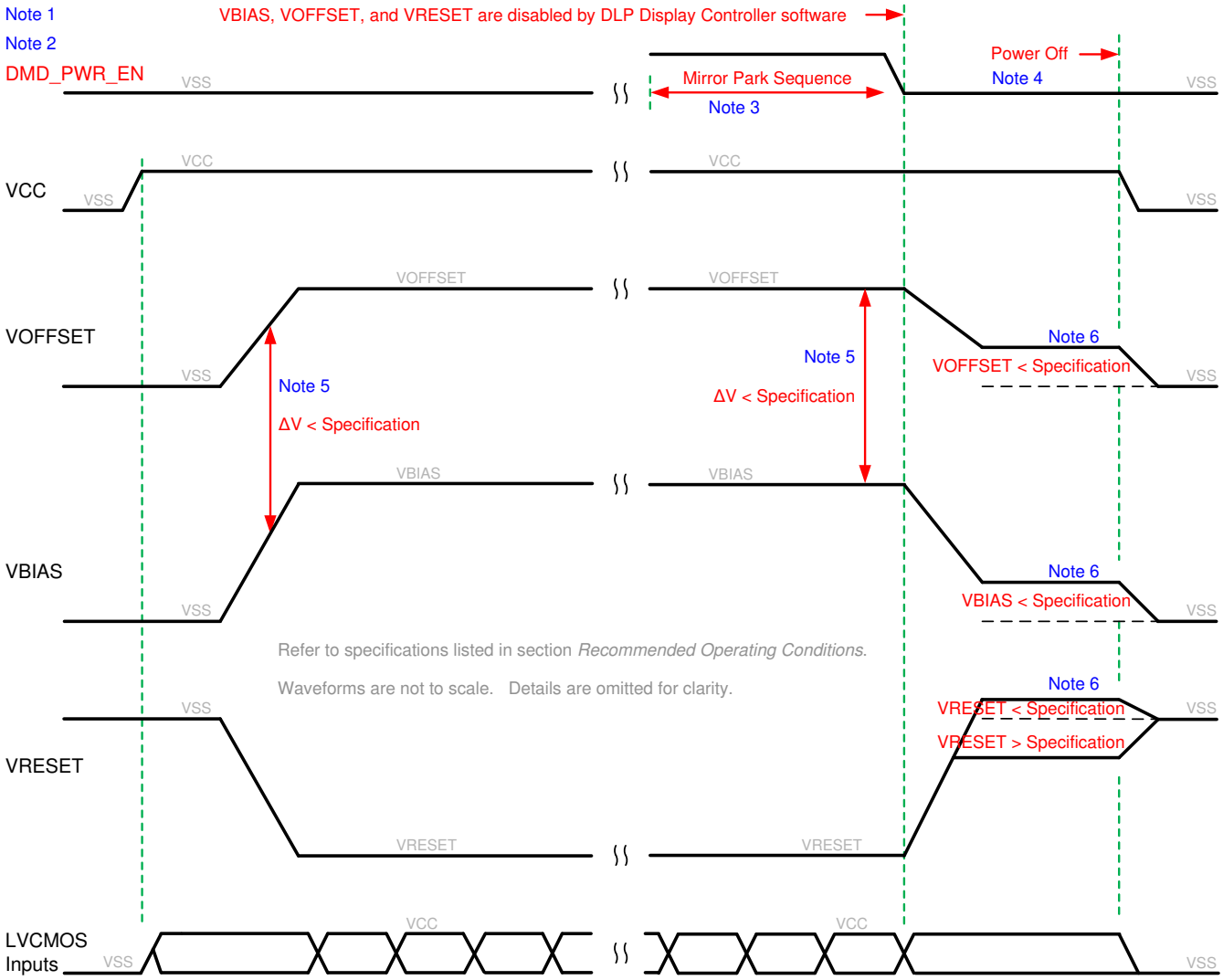


図 9-1. DMD Power Supply Sequencing Requirements

Note 1: Refer to specifications listed in セクション 6.4 . Waveforms are not to scale. Details are omitted for clarity.

Note 2: DMD_PWR_EN is not a package pin on the DMD. It is a signal from the DLP Display Controller (DLPC2607) that enables the V_{RESET}, V_{BIAS}, and V_{OFFSET} regulators on the system board.

Note 3: After the DMD micromirror park sequence is complete, the DLP display controller (DLPC2607) software initiates a hardware power-down that disables V_{BIAS}, V_{RESET} and V_{OFFSET}.

Note 4: During the micromirror parking process, V_{CC}, V_{BIAS}, V_{OFFSET}, and V_{RESET} power supplies are all required to be within the specification limits in セクション 6.4 . Once the micromirrors are parked, V_{BIAS}, V_{OFFSET}, and V_{RESET} power supplies can be turned off.

Note 5: To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in セクション 6.4 . It is critical to meet this requirement and that V_{BIAS} not reach full power level until after V_{OFFSET} is at almost full power level. OEMs may find that the most reliable way to ensure this is to delay powering V_{BIAS} until after V_{OFFSET} is fully powered on during power-up (and to remove V_{BIAS} prior to V_{OFFSET} during power down). In this case, V_{OFFSET} is run at its maximum allowable voltage level (8.75 V).

Note 6: Refer to specifications listed in 表 9-1.

表 9-1. DMD Power-Down Sequence Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{BIAS}	Supply voltage level during power-down sequence		4.0	V
V_{OFFSET}	Supply voltage level during power-down sequence		4.0	V
V_{RESET}	Supply voltage level during power-down sequence	–4.0	0.5	V

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD, however the DMD is typically connected using a board to board connector with a flex cable. The flex cable provides an interface for data and control signals between the DLPC2607 controller and the DLP2000 DMD. For detailed layout guidelines refer to the DLPC2607 controller layout guidelines under PCB design and DMD interface considerations.

Some layout guidelines for the flex cable interface with the DMD are:

- Minimize the number of layer changes for DMD data and control signals.
- DMD data and control lines are DDR, whereas DMD_SAC and DMD_DRC lines are single data rate. Matching the DDR lines is more critical and should take precedence over matching single data rate lines.
- 図 10-1 and 図 10-2 show the top and bottom layer of the DMD flex cable connections.

10.2 Layout Example

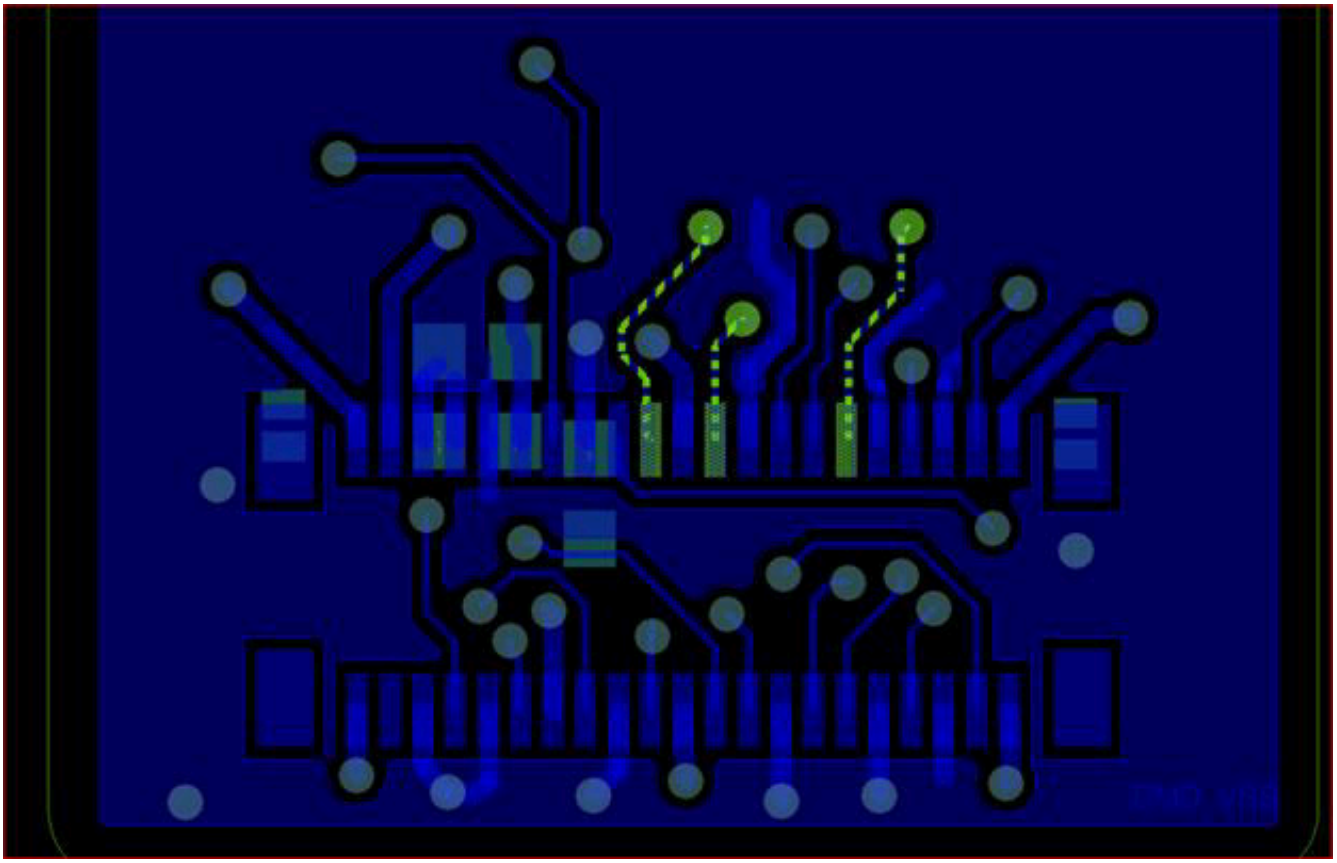


図 10-1. DMD Flex Cable—Top Layer

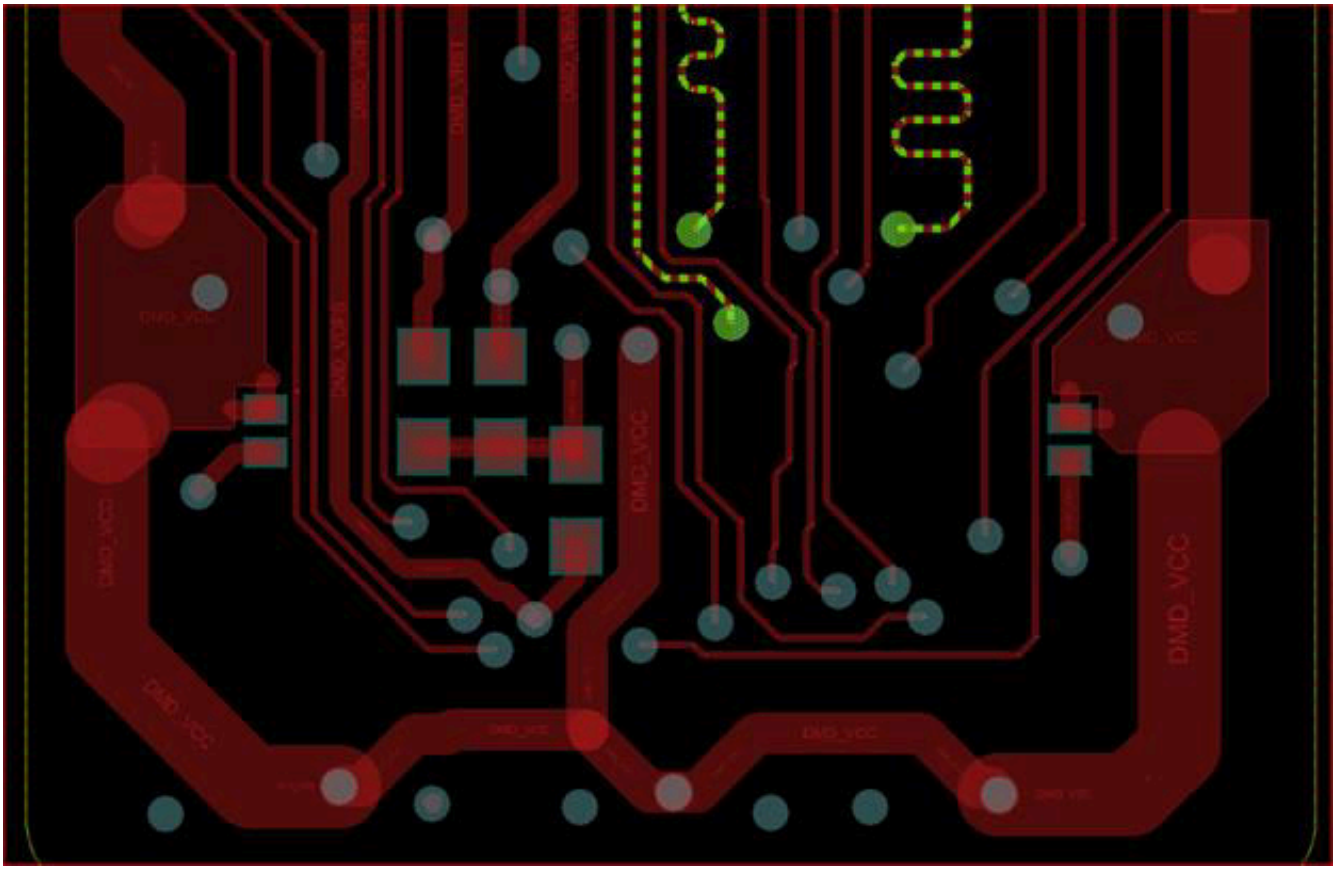


図 10-2. DMD Flex Cable—Bottom Layer

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

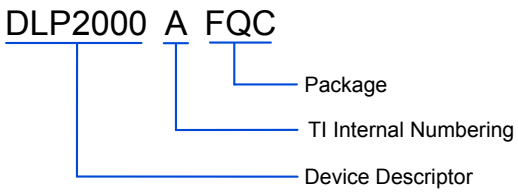

図 11-1. Part Number Description

11.2.2 Device Markings

- Device Marking includes the Human-Readable character string GHJJJJK VVVV
- GHJJJJK is the Lot Trace Code
- VVVV is a 4 character Encoded Device Part Number

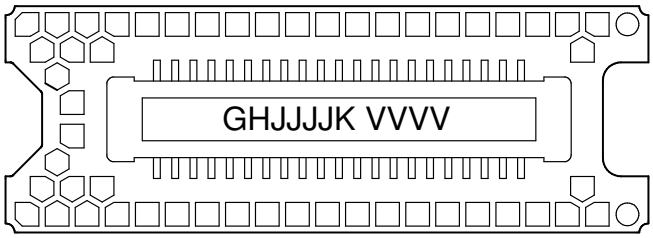

図 11-2. DMD Marking Location

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPC2607	Click here	Click here	Click here	Click here	Click here
DLPA1000	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.6 Trademarks

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP2000AFQC	ACTIVE	CLGA	FQC	42	180	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

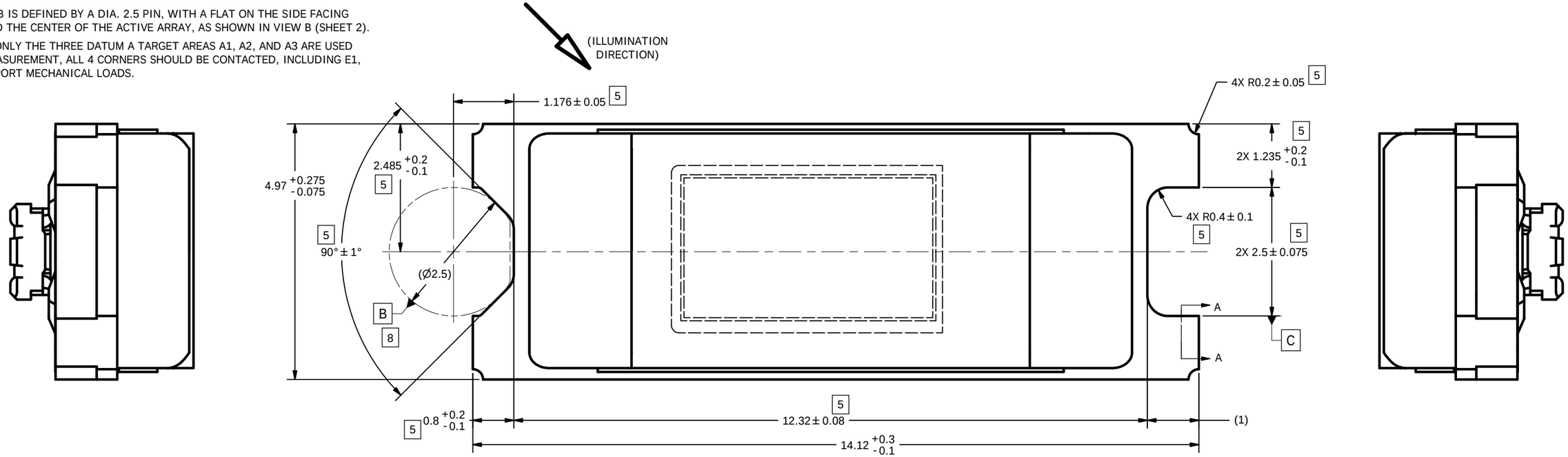
DWG NO. 2510560 SH 1

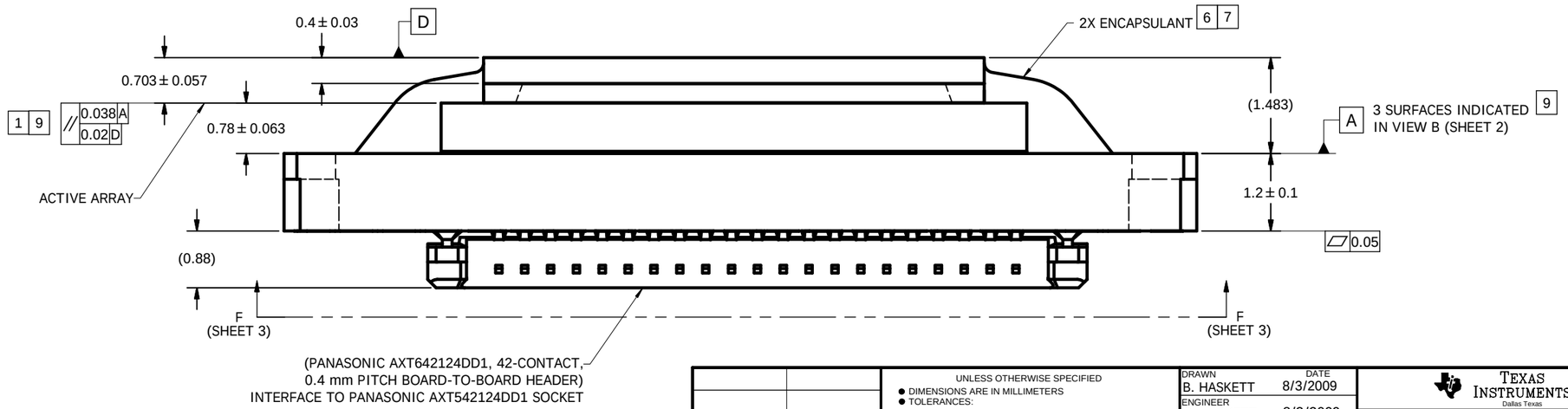
REVISIONS

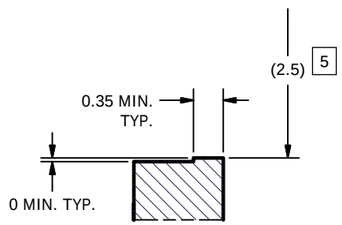
REV	DESCRIPTION	DATE	BY
A	ECO 2100735 INITIAL RELEASE	8/3/09	BMH
B	ECO 2102356 ADD DATUM E AND NOTE 9; UPDATE SOLDER APPEARANCE; TIGHTEN NOTCH X-AXIS TOL'S	10/22/09	BMH
C	ECO 2104056 CHG ENCAP MAX HEIGHT FROM TBD TO ZERO	1/4/10	BMH
D	ECO 2166625 ADD "FQC PACKAGE" TO DRAWING TITLE; SHOW APERTURE CORNER RADII PICTORIALLY	5/30/17	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR IN CONNECTOR RECESS.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
7. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
8. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
9. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.







SECTION A-A
NOTCH OFFSETS

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ±1°
  - 2 PLACE DECIMALS ±0.25
  - 1 PLACE DECIMALS ±0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	8/3/2009
ENGINEER	B. HASKETT	8/3/2009
QA/CE	P. KONRAD	8/3/2009
CM	F. ARMSTRONG	8/3/2009
	J. GRIMMETT	8/3/2009
APPROVED		

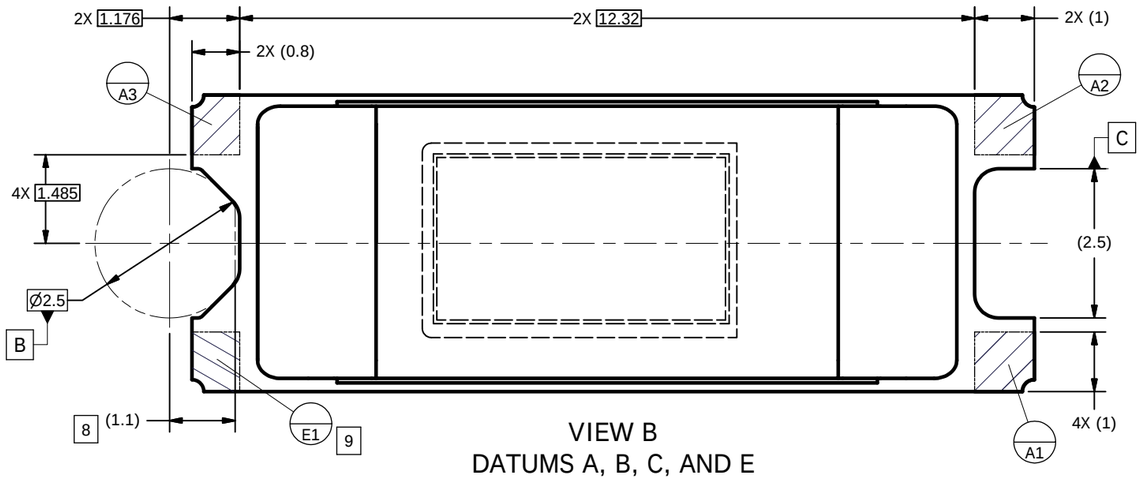
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .2 nHD DDR SERIES 230 (FQC PACKAGE)

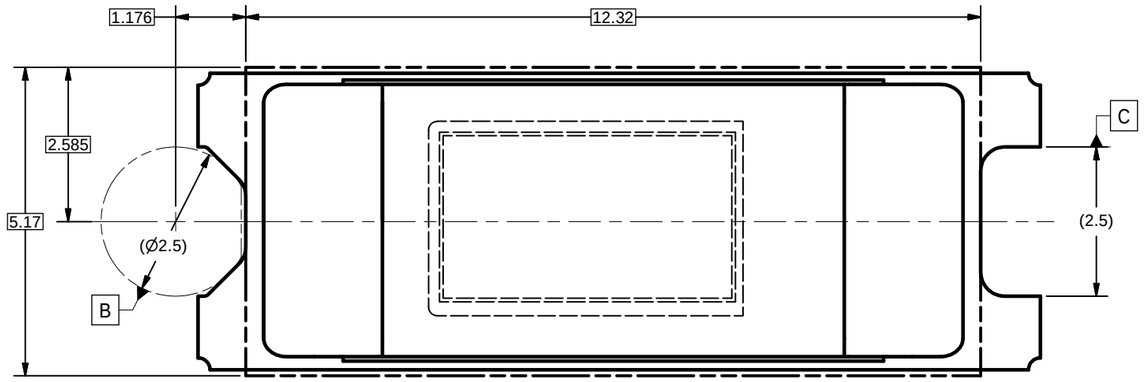
SIZE	DWG NO	REV
D	2510560	D

SCALE 25:1 SHEET 1 OF 3

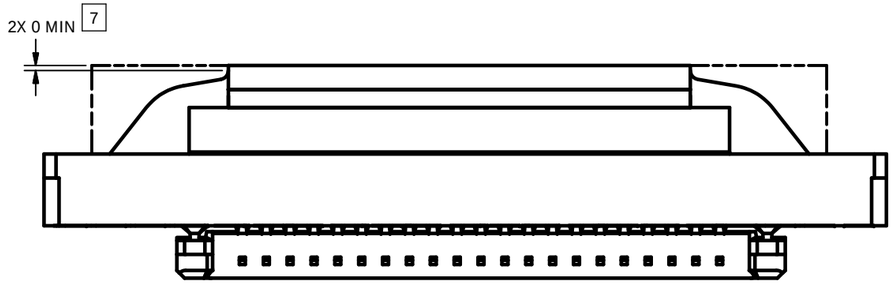
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
SCALE 20 : 1
(FROM SHEET 1)



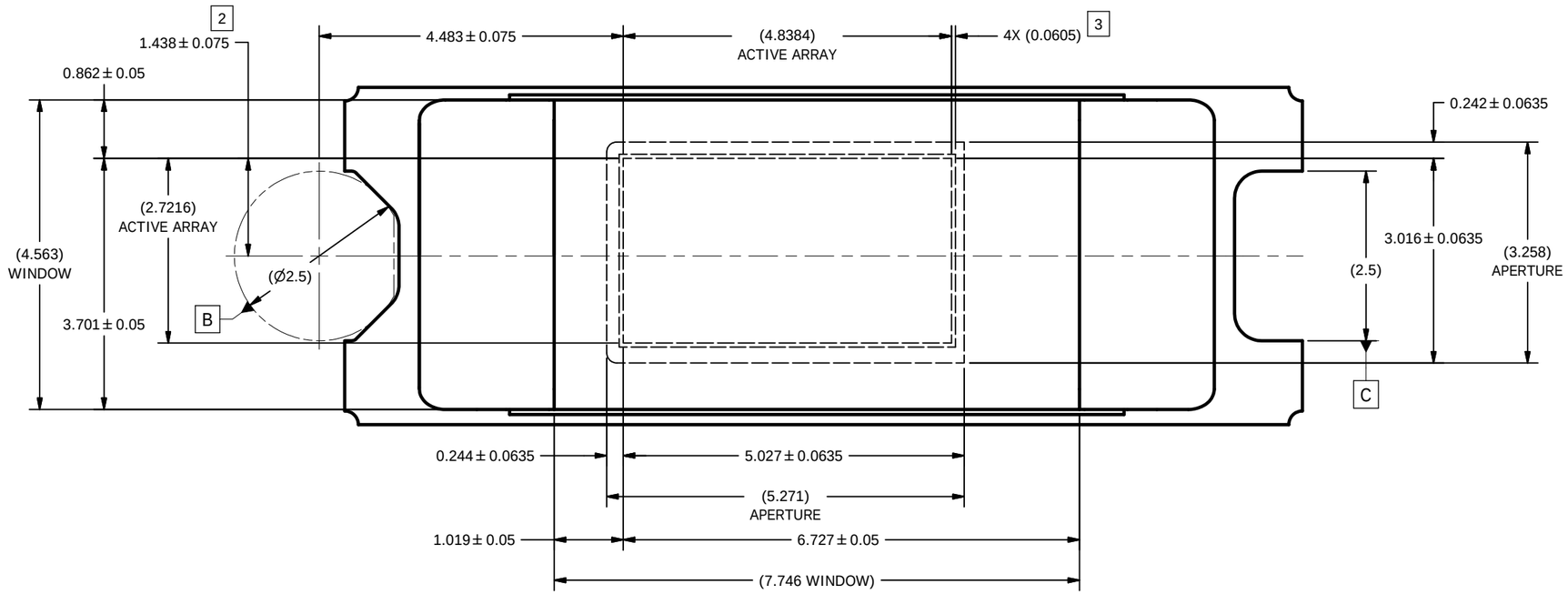
VIEW C 6
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
SCALE 20 : 1
(FROM SHEET 1)



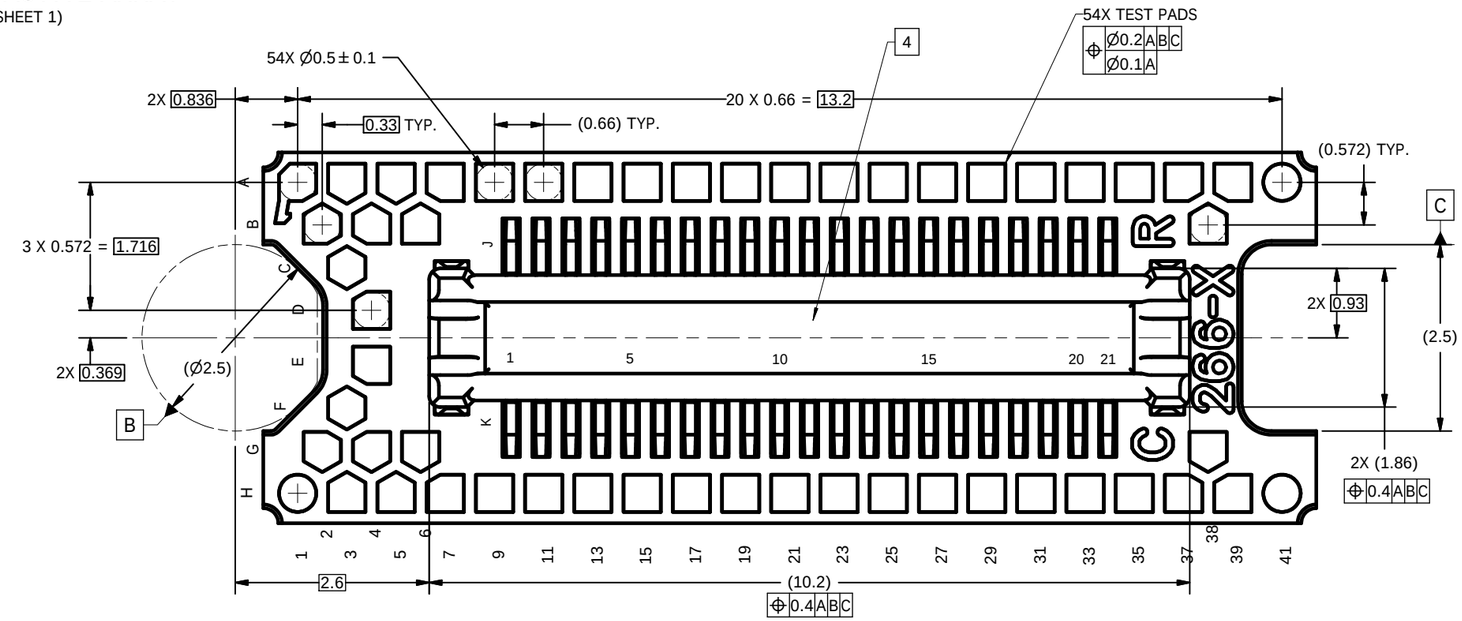
VIEW D
ENCAPSULANT MAXIMUM HEIGHT
SCALE 20 : 1

Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 8/3/2009	SIZE D	DWG NO 2510560	REV D
			SCALE	SHEET 2 OF 3	

INV11-2006a



VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



VIEW F-F
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 8/3/2009	SIZE D	DWG NO 2510560	REV D
			SCALE	SHEET 3 OF 3	

INV11-2006a

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