TEXAS INSTRUMENTS
DLP4620S-Q1
JAJSPG6C – DECEMBER 2022 – REVISED AUGUST 2024

DLP4620S-Q1 車載対応ディスプレイ・アプリケーション向け、DLP デジタル・マイクロミラー・デバイス (DMD)

1 特長

- 車載アプリケーション認定済み
  - DMD アレイの動作温度範囲:-40℃～105℃
- 機能安全品質管理
  - ASIL-B までの ISO 26262 機能安全システム設計に役立つ資料を入手可能
- DLP4620S-Q1 車載用チップセットには以下のものが含まれます。
  - DLP4620S-Q1 DMD
  - DLPC231S-Q1 DMD コントローラ
  - TPS99000S-Q1 システム管理および照明コントローラ
- 0.46 インチの対角のマイクロミラー アレイ
  - 7.6µm のマイクロミラーピッチ
  - ±12° のマイクロミラー傾斜角
  - 下位 照明による高効率と小型エンジン サイズの実現
  - 最大 1920 × 960 の解像度、外部 GPU を使った 5 点型前処理付き
  - 1358 × 566 または 1220 × 610 の解像度モード
  - LED またはレーザー照明に対応可能
- 600MHz SubLVDS DMD インターフェイスによる低い消費電力と放射妨害
- 上限や下限の温度でも 10kHz の DMD リフレッシュ レートを維持
- DMD メモリ セルの内蔵セルフ テスト (BIST)

2 アプリケーション

- 広視野の拡張現実ヘッドアップ ディスプレイ (HUD)
- デジタル クラスタ、ナビゲーション、インフォテインメント用のフロントガラス ディスプレイ

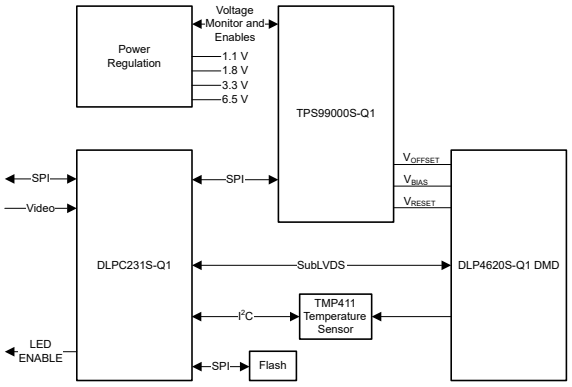
3 概要

DLP® DLP4620S-Q1 車載用デジタル マイクロミラー デバイス (DMD) は、DLPC231S-Q1 DMD コントローラや TPS99000S-Q1 システム管理および照明コントローラとの組み合わせにより、高性能の高解像度拡張現実ヘッドアップ ディスプレイ (HUD) を実現します。2:1 のアスペクト比によって非常に大きいアスペクト比の設計に対応可能であり、また、0.9 メガピクセルの解像度により HUD アプリケーションで網膜に匹敵する解像度のディスプレイを実現します。DLP4620S-Q1 は、光学スループットと解像度のバランスが優れているため、広い視野角と大きなドライバー アイ ボックスを実現し、ユーザー体験を向上させることができます。このチップセットを LED またはレーザーおよび光学システムと組み合わせることで、125% NTSC の深い飽和色、15,000cd/m2 を超える非常に高い輝度、5000:1 を超える高いダイナミック調光比、太陽光負荷に対する高い耐性を実現できます。DLP4620S-Q1 車載用 DMD マイクロミラー アレイは、左 / 右ハンドル構成に対応するため、高効率でより小型の光学エンジン設計が可能な底面照明用に構成されています。システム コストを最適化するため、DLP4620S-Q1 デバイスはパネル パッケージで供給されます。このパッケージは、DMD アレイへの熱抵抗が小さいため、効率的なサーマル ソリューションを実現できます。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ
DLP4620S-Q1	FQX	25.2mm × 11.0 mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」セクションを参照してください。



DLP4620S-Q1DLP チップセットのシステム ブロック図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 8
5.1 Absolute Maximum Ratings ... 8
5.2 Storage Conditions ... 8
5.3 ESD Ratings ... 9
5.4 Recommended Operating Conditions ... 9
5.5 Thermal Information ... 10
5.6 Electrical Characteristics ... 10
5.7 Timing Requirements ... 11
5.8 Switching Characteristics ... 14
5.9 System Mounting Interface Loads ... 15
5.10 Micromirror Array Physical Characteristics ... 15
5.11 Micromirror Array Optical Characteristics ... 17
5.12 Window Characteristics ... 17
5.13 Chipset Component Usage Specification ... 17
6 Detailed Description ... 18
6.1 Overview ... 18
6.2 Functional Block Diagram ... 19
6.3 Feature Description ... 19
6.4 System Optical Considerations ... 21
6.5 DMD Image Performance Specification ... 22
6.6 Micromirror Array Temperature Calculation ... 23
6.7 Micromirror Landed-On/Landed-Off Duty Cycle ... 25
7 Application and Implementation ... 26
7.1 Application Information ... 26
7.2 Typical Application ... 26
7.3 Power Supply Recommendations ... 28
7.4 Layout Guidelines ... 30
7.5 Layout Example ... 30
8 Device and Documentation Support ... 33
8.1 Device Support ... 33
8.2 サード・パーティ製品に関する免責事項 ... 33
8.3 ドキュメントの更新通知を受け取る方法 ... 33
8.4 サポート・リソース ... 34
8.5 Trademarks ... 34
8.6 静電気放電に関する注意事項 ... 34
8.7 DMD Handling ... 34
8.8 用語集 ... 34
9 Revision History ... 34
10 Mechanical, Packaging, and Orderable Information ... 34

4 Pin Configuration and Functions

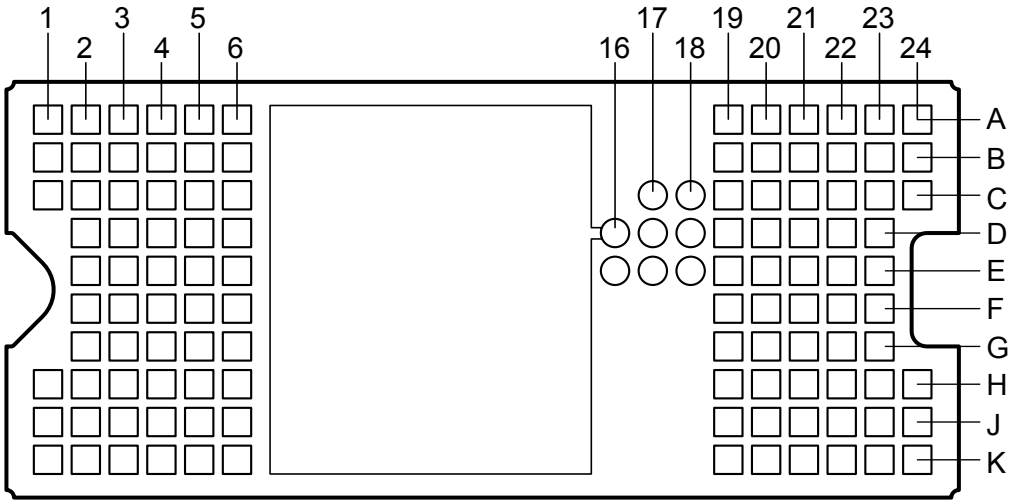


図 4-1. FQX Package 120-Pin LGA Bottom View

表 4-1. Pin Functions—Connector Pins

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	A3	I	SubLVDS	Double	Data, Negative
D_AN(1)	B1	I	SubLVDS	Double	Data, Negative
D_AN(2)	C2	I	SubLVDS	Double	Data, Negative
D_AN(3)	F2	I	SubLVDS	Double	Data, Negative
D_AN(4)	H2	I	SubLVDS	Double	Data, Negative
D_AN(5)	K1	I	SubLVDS	Double	Data, Negative
D_AN(6)	K4	I	SubLVDS	Double	Data, Negative
D_AN(7)	K6	I	SubLVDS	Double	Data, Negative
D_AP(0)	A2	I	SubLVDS	Double	Data, Positive
D_AP(1)	C1	I	SubLVDS	Double	Data, Positive
D_AP(2)	D2	I	SubLVDS	Double	Data, Positive
D_AP(3)	E2	I	SubLVDS	Double	Data, Positive
D_AP(4)	G2	I	SubLVDS	Double	Data, Positive
D_AP(5)	K2	I	SubLVDS	Double	Data, Positive
D_AP(6)	K3	I	SubLVDS	Double	Data, Positive
D_AP(7)	K5	I	SubLVDS	Double	Data, Positive
D_BN(0)	A22	I	SubLVDS	Double	Data, Negative
D_BN(1)	B24	I	SubLVDS	Double	Data, Negative
D_BN(2)	D23	I	SubLVDS	Double	Data, Negative
D_BN(3)	F23	I	SubLVDS	Double	Data, Negative

表 4-1. Pin Functions—Connector Pins (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BN(4)	H23	I	SubLVDS	Double	Data, Negative
D_BN(5)	K24	I	SubLVDS	Double	Data, Negative
D_BN(6)	K21	I	SubLVDS	Double	Data, Negative
D_BN(7)	K19	I	SubLVDS	Double	Data, Negative
D_BP(0)	A23	I	SubLVDS	Double	Data, Positive
D_BP(1)	C24	I	SubLVDS	Double	Data, Positive
D_BP(2)	C23	I	SubLVDS	Double	Data, Positive
D_BP(3)	E23	I	SubLVDS	Double	Data, Positive
D_BP(4)	G23	I	SubLVDS	Double	Data, Positive
D_BP(5)	K23	I	SubLVDS	Double	Data, Positive
D_BP(6)	K22	I	SubLVDS	Double	Data, Positive
D_BP(7)	K20	I	SubLVDS	Double	Data, Positive
DCLK_AN	J1	I	SubLVDS	Double	Clock, Negative
DCLK_AP	H1	I	SubLVDS	Double	Clock, Positive
DCLK_BN	J24	I	SubLVDS	Double	Clock, Negative
DCLK_BP	H24	I	SubLVDS	Double	Clock, Positive
LS_CLKN	C3	I	SubLVDS	Single	Clock for Low Speed Interface, Negative
LS_CLKP	C4	I	SubLVDS	Single	Clock for Low Speed Interface, Positive
LS_WDATAN	C5	I	SubLVDS	Single	Write Data for Low Speed Interface, Negative
LS_WDATAP	C6	I	SubLVDS	Single	Write Data for Low Speed Interface, Positive
CONTROL INPUTS					
DMD_DEN_ARSTZ	E6	I	LPSDR		Asynchronous Reset Active Low. Logic High Enables DMD
LS_RDATA_A	E19	O	LPSDR	Single	Read Data for Low Speed Interface
LS_RDATA_B	F19	O	LPSDR	Single	Read Data for Low Speed Interface
TEMPERATURE SENSE DIODE					
TEMP_N	F6	O			Calibrated temperature diode used to assist accurate temperature measurements of DMD die
TEMP_P	G6	I			

表 4-1. Pin Functions—Connector Pins (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
POWER					
VBIAS	A4	Power			Supply voltage for positive bias level at micromirrors
VBIAS	A21	Power			
VOFFSET	B3	Power			Supply voltage for high-voltage CMOS core logic. Supply voltage for offset level at micromirrors
VOFFSET	B4	Power			
VOFFSET	B21	Power			
VOFFSET	B22	Power			
VOFFSET	J4	Power			
VOFFSET	J21	Power			
VRESET	B6	Power			Supply voltage for negative reset level at micromirrors
VRESET	B19	Power			
VDD	A5	Power			Supply voltage for Low Voltage CMOS core logic; for LPSDR inputs; for normal high level at micromirror address electrodes
VDD	A20	Power			
VDD	C20	Power			
VDD	D4	Power			
VDD	D19	Power			
VDD	D21	Power			
VDD	E3	Power			
VDD	E22	Power			
VDD	F4	Power			
VDD	G3	Power			
VDD	G21	Power			
VDD	H22	Power			
VDD	J3	Power			
VDD	J6	Power			
VDD	J19	Power			
VDDI	E5	Power			Supply voltage for SubLVDS receivers
VDDI	E20	Power			
VDDI	F5	Power			
VDDI	F20	Power			
VDDI	G5	Power			
VDDI	G20	Power			
VDDI	H5	Power			
VDDI	H20	Power			

表 4-1. Pin Functions—Connector Pins (続き)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
VSS	A1	Ground			Common return. Ground for all power
VSS	A6	Ground			
VSS	A19	Ground			
VSS	A24	Ground			
VSS	B2	Ground			
VSS	B5	Ground			
VSS	B20	Ground			
VSS	B23	Ground			
VSS	C19	Ground			
VSS	C21	Ground			
VSS	C22	Ground			
VSS	D3	Ground			
VSS	D5	Ground			
VSS	D6	Ground			
VSS	D20	Ground			
VSS	D22	Ground			
VSS	E4	Ground			
VSS	E21	Ground			
VSS	F3	Ground			
VSS	F21	Ground			
VSS	F22	Ground			
VSS	G4	Ground			
VSS	G19	Ground			
VSS	G22	Ground			
VSS	H3	Ground			
VSS	H4	Ground			
VSS	H6	Ground			
VSS	H19	Ground			
VSS	H21	Ground			
VSS	J2	Ground			
VSS	J5	Ground			
VSS	J20	Ground			
VSS	J22	Ground			
VSS	J23	Ground			

表 4-2. Pin Functions—Test Pads

Pin Number	SYSTEM BOARD
C17	Do not connect.
C18	Do not connect.
D16	Do not connect. Internally connected to VSS
D17	Do not connect.
D18	Do not connect.
E16	Do not connect.
E17	Do not connect.
E18	Do not connect.

5 Specifications

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure above or below the Recommended Operating Conditions for extended periods may affect device reliability.

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{DD}	Supply voltage for LVCMOS core logic(1) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
V_{DDI}	Supply voltage for SubLVDS receivers(1)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (1) (2)	–0.5	8.75	V
V_{BIAS}	Supply voltage for micromirror electrode (1)	–0.5	17	V
V_{RESET}	Supply voltage for micromirror electrode (1)	–11	0.5	V
$\lvert V_{DDI} - V_{DD} \rvert$	Supply voltage delta (absolute value) (3)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value) (4)		8.75	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value) (5)		28	V
INPUT VOLTAGE				
Input voltage for LVCMOS Inputs (1)		–0.5	V_{DD} + 0.5	V
Input voltage for other inputs SubLVDS (1) (6)		–0.5	V_{DDI} + 0.5	V
INPUT PINS				
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) (6)		810	mV
$\lvert I_{ID} \rvert$	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
F_{max_LS}	Clock frequency for low speed interface LS_CLK	100	130	MHz
TEMPERATURE DIODE				
I_{TEMP_DIODE}	Max current source into temperature diode		120	µA
ENVIRONMENTAL				
T_{ARRAY}	Operating DMD array temperature	–40	105	°C

(1) All voltage values are with respect to the ground terminals (V_{SS}). The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw and permanent damage to the device.
(4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw and permanent damage to the device.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw and permanent damage to the device.
(6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage to the internal termination resistors may result.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	–40	125	°C

5.3 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (3)	8.25	8.5	8.75	V
V_{BIAS}	Supply voltage for mirror electrode	15.5	16	16.5	V
V_{RESET}	Supply voltage for micromirror electrode	–9.5	–10	–10.5	V
$\lvert V_{DDI} - V_{DD}\rvert$	Supply voltage delta (absolute value) (4)			0.3	V
$\lvert V_{BIAS} - V_{OFFSET}\rvert$	Supply voltage delta (absolute value) (5)			8.75	V
$\lvert V_{BIAS} - V_{RESET}\rvert$	Supply voltage delta (absolute value) (6)			28	V
LOW-SPEED LPDSR INTERFACE					
f_{clock_LS}	Clock frequency for low speed interface LS_CLK	108		120	MHz
DCD_{IN}	LSIF duty cycle distortion (LS_CLK)	44%		56%	
SUBLVDS INTERFACE					
f_{clock_HS}	Clock frequency for high-speed interface DCLK			600	MHz
DCD_{IN}	LVDS duty cycle distortion (DCLK)	44%		56%	
$\lvert V_{ID}\rvert$	LVDS differential input voltage magnitude (7)	150	250	350	mV
V_{CM}	Common mode voltage (7)	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage (7)	525		1275	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance (8)	80	100	120	Ω
	100Ω differential PCD trace	6.35		152.4	mm
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature (9) (11)	-40		105	°C
Illumination					
ILL_{UV}	Illumination, wavelength < 395 nm (10)			2	mW/cm^2
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in the Illumination Overfill Diagram			90	mW/mm^2

(1) Recommended Operating Conditions are applicable after the DMD is installed in the final product.
(2) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(3) V_{OFFSET} supply transients must fall within specified min/max voltages.
(4) To prevent excess current, the supply voltage delta $|V_{DDI} - V_{DD}|$ must be less than the specified limit.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit.
(7) See Figure 5-6 and Figure 5-7.
(8) See Figure 5-8.
(9) DMD Active Array temperature can be calculated as shown in the Micromirror Array Temperature Calculation section.
(10) The maximum operation conditions for operating temperature and UV illumination shall not be implemented simultaneously.
(11) Operating profile information for device micromirror landed duty-cycle and temperature may be provided if requested.

5.4.1 Illumination Overfill Diagram

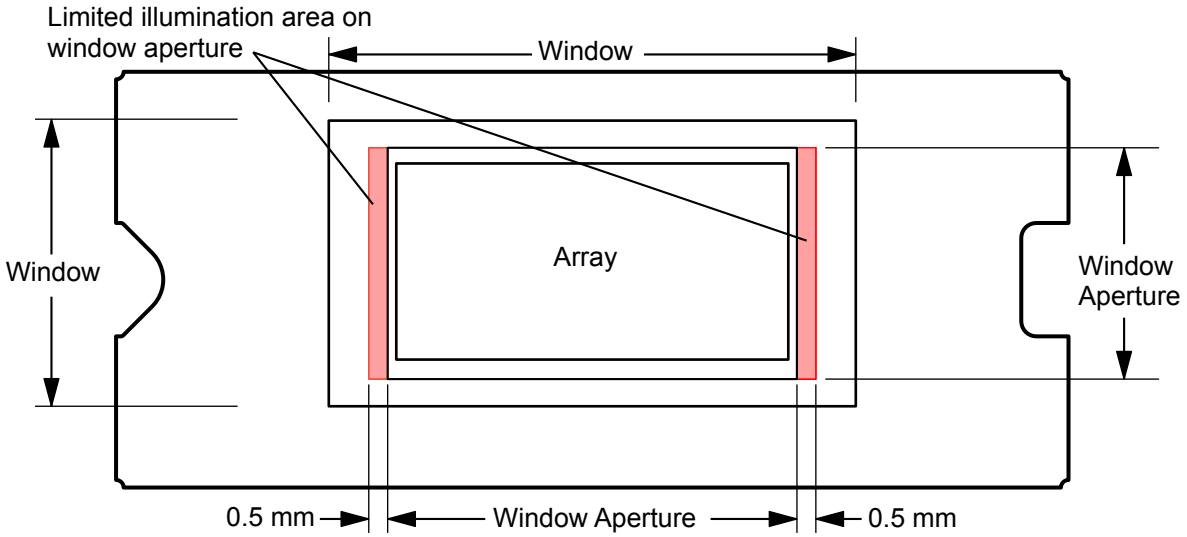


図 5-1. Illumination Overfill Diagram

5.5 Thermal Information

THERMAL METRIC		DLP4620S-Q1 FQX	UNIT
Thermal resistance	Active area-to-test point 1 (TP1)(1)	1.3	°C/W
Thermal resistance	Active area-to-temperature sense diode(1)	0.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions* section. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Design optical systems to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD(2)	VDD = 1.95V			220	mA
I_{DDI}	Supply current: VDDI(2)	VDDI = 1.95V			62	mA
I_{OFFSET}	Supply current: VOFFSET	VOFFSET = 8.75V			35	mA
I_{BIAS}	Supply current: VBIAS	VBIAS = 16.5V			1.5	mA
I_{RESET}	Supply current: VRESET	VRESET = –10.5V	–16			mA
POWER						
P_{DD}	Supply power dissipation: VDD (2)	VDD = 1.95V			430	mW
P_{DDI}	Supply power dissipation: VDDI (2)	VDDI = 1.95V			121	mW
P_{OFFSET}	Supply power dissipation: VOFFSET	VOFFSET = 8.75V			307	mW
P_{BIAS}	Supply power dissipation: VBIAS	VBIAS = 16.5V			25	mW
P_{RESET}	Supply power dissipation: VRESET	VRESET = –10.5V			168	mW
P_{TOTAL}	Supply power dissipation: Total				1045	mW
LVCMOS INPUT						

5.6 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage(3)		0.7 × V_{DD}		VDD + 0.3	V
V_{IL}	Low-level input voltage(3)		–0.3		0.3 × V_{DD}	V
$V_{IH(AC)}$	AC input high voltage(3)		0.8 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(3)		–0.3		0.2 × V_{DD}	V
V_{Hyst}	Input Hysteresis(3)	See Figure 5-9.	0.1 × V_{DD}		0.4 × V_{DD}	V
I_{IL}	Low–level input current(3)	VDD = 1.95V; V_I = 0V	–100			nA
I_{IH}	High–level input current(3)	VDD = 1.95V; V_I = 1.95V			135	µA
LVCMOS OUTPUT						
V_{OH}	DC output high voltage(4)	I_{OH} = –2mA	0.8 × V_{DD}			V
V_{OL}	DC output low voltage(4)	I_{OL} = 2mA			0.2 × V_{DD}	V
I_{OZ}	High impedance output current	VDD = 1.95V			10	µA
CAPACITANCE						
C_{IN}	Input capacitance LVCMOS	F = 1MHz			10	pF
	Input capacitance SubLVDS	F = 1MHz			20	pF
C_{OUT}	Output capacitance	F = 1MHz			13	pF
C_{TEMP}	Temperature sense diode capacitance	F = 1MHz			20	pF

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) Supply power dissipation based on non-compressed commands and data.
(3) LPSDR input specification are for pin DMD_DEN_ARSTZ.
(4) LPSDR output specification is for pins LS_RDATA_A and LS_RDATA_B.

5.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
Low-Speed Interface						
t_r	Rise slew rate (1) (2)	(20% to 80%) × VDD	0.25			V/ns
t_f	Fall slew rate (1) (2)	(80% to 20%) × VDD	0.25			V/ns
t_c	Cycle time LS_CLK		7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high(3)	50% to 50% reference points	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low(3)	50% to 50% reference points	3.1			ns
t_{su}	Setup time(3)	LS_WDATA valid before LS_CLK ↑ or LS_CLK ↓	1.5			ns
t_h	Hold time(3)	LS_WDATA valid after LS_CLK ↑ or LS_CLK ↓	1.5			ns
t_{WINDOW}	Window time	Setup time + hold time	3			ns
$t_{DERATING}$	Window time derating	For each 0.25 V/ns reduction in slew rate below 1 V/ns		0.35		ns
High-Speed Interface						
t_r	Rise slew rate(2)	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate(2)	80% to 20% reference points	0.7	1		V/ns
t_c	Cycle time DCLK (3)		1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high(3)	50% to 50% reference points	0.75			ns

5.7 Timing Requirements (続き)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
$t_{W(L)}$	Pulse duration DCLK low(3)	50% to 50% reference points	0.75			ns
t_{WINDOW}	Window time(3) (4)	Setup time + Hold time	0.3			ns
$t_{LVDS-EN+REFGEN}$	Power-up receiver (5)				2000	ns

(1) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 6-2.
(2) See Figure 5-3.
(3) See Figure 5-4.
(4) See Figure 5-5.
(5) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

Electrical and Timing Diagrams

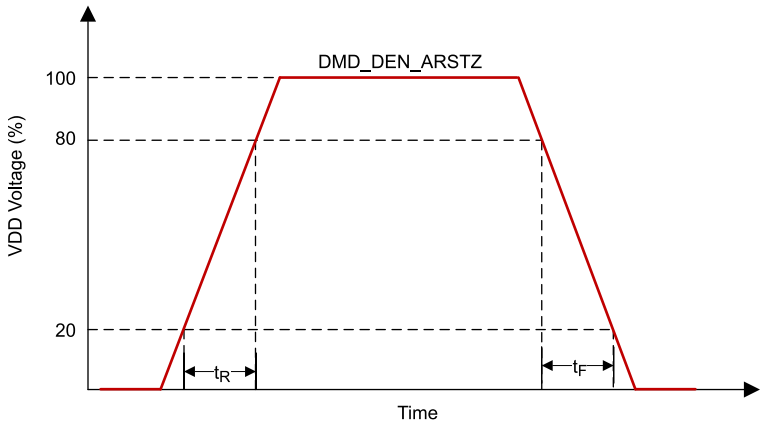


図 5-2. LPSDR Input Rise and Fall Slew Rate

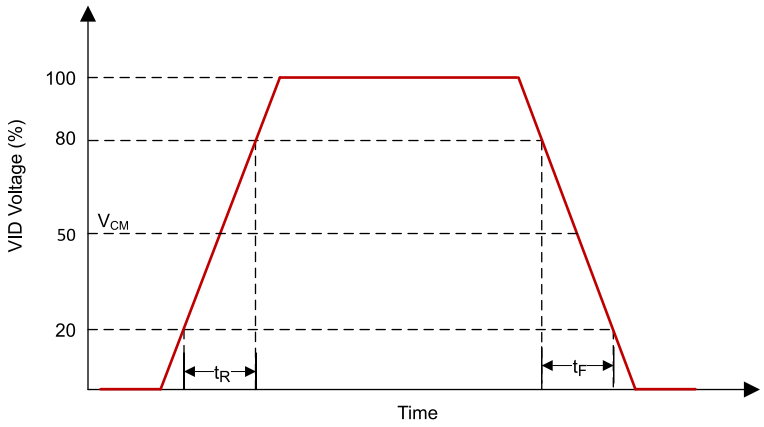


図 5-3. SubLVDS Input Rise and Fall Slew Rate

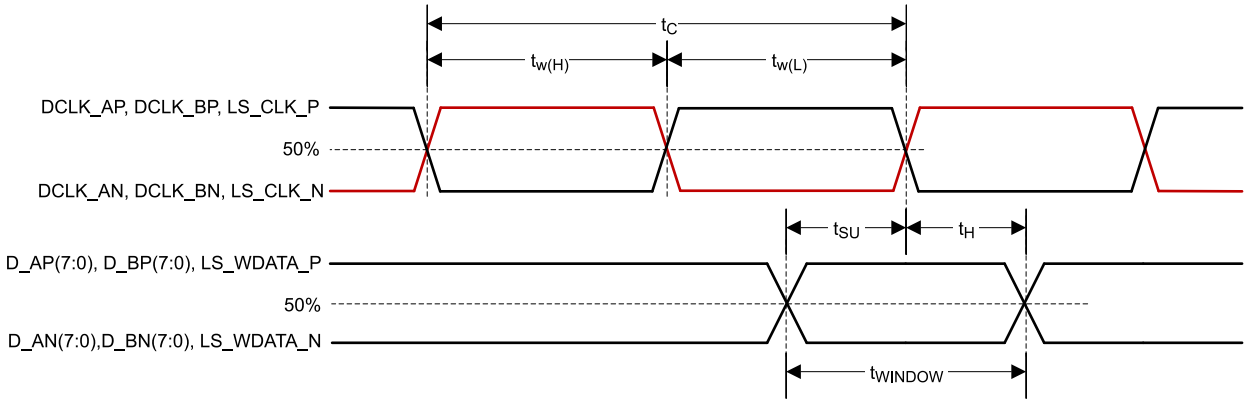
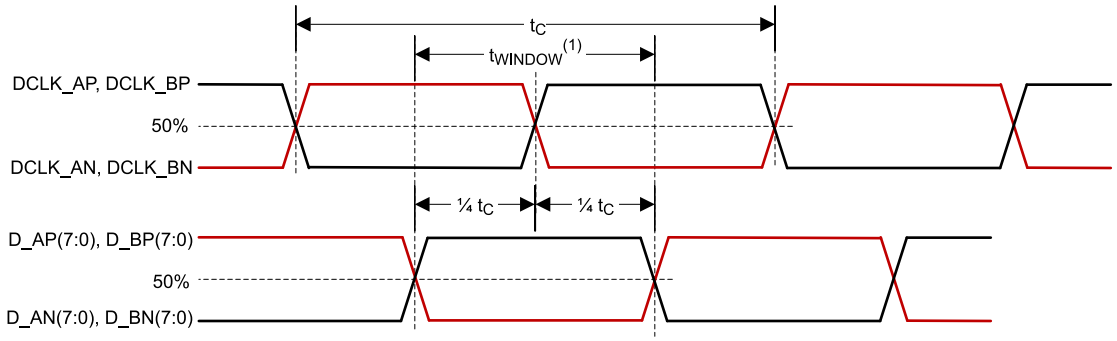


図 5-4. SubLVDS Switching Parameters



(1) High-speed training scan window

図 5-5. High-Speed Training Scan Window

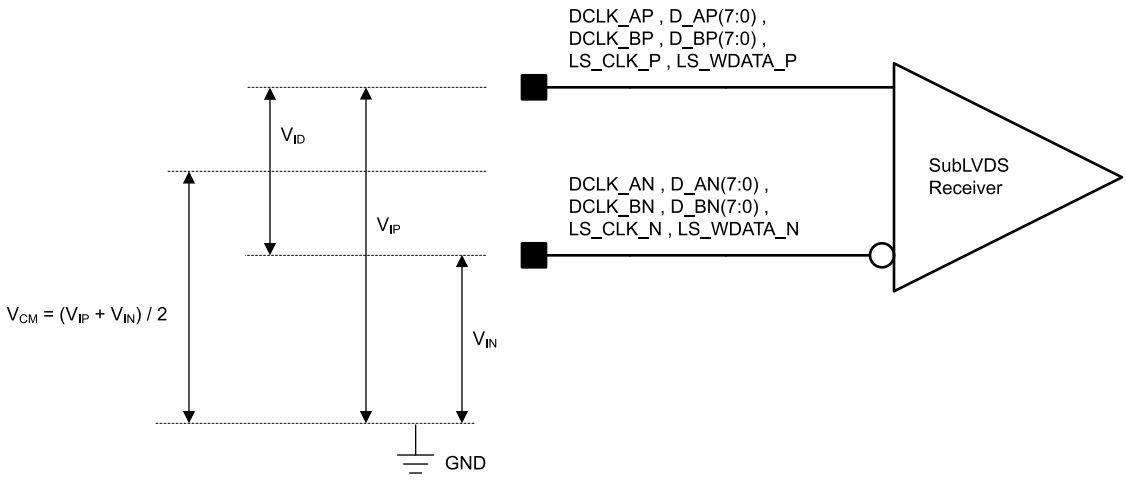


図 5-6. SubLVDS Voltage Parameters

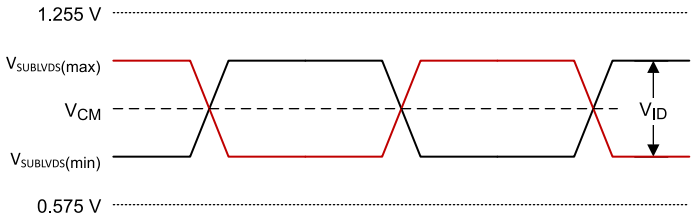


図 5-7. SubLVDS Waveform Parameters

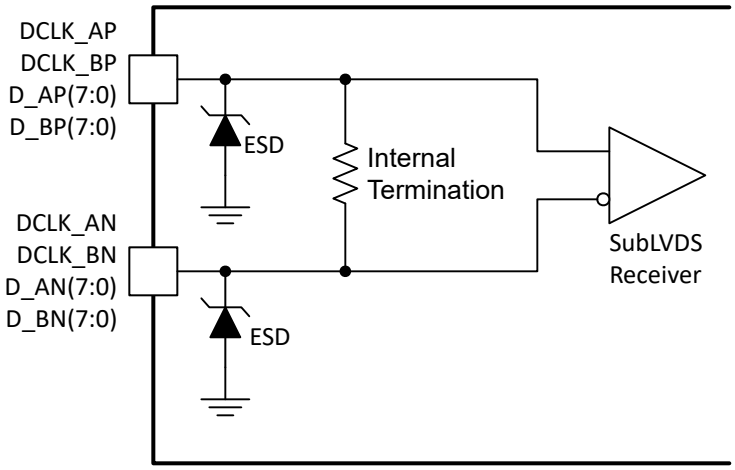


図 5-8. SubLVDS Equivalent Input Circuit

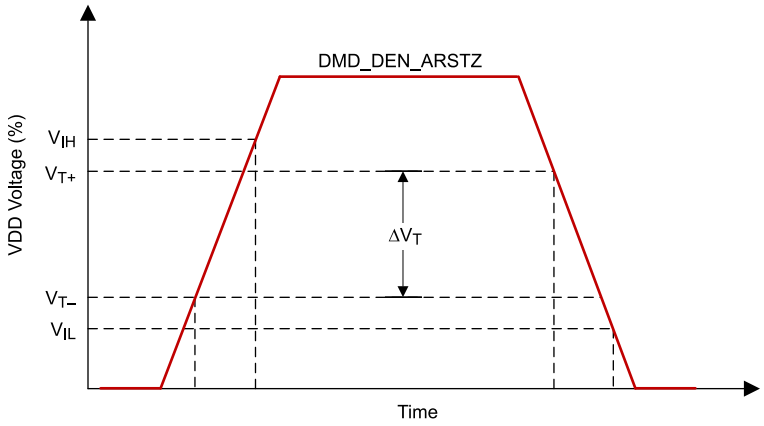


図 5-9. LPSDR Input Hysteresis

5.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output(2)	C_L = 45pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) See 図 5-10 and 図 5-11.

5.8.1 LPSDR and Test Load Circuit Diagrams

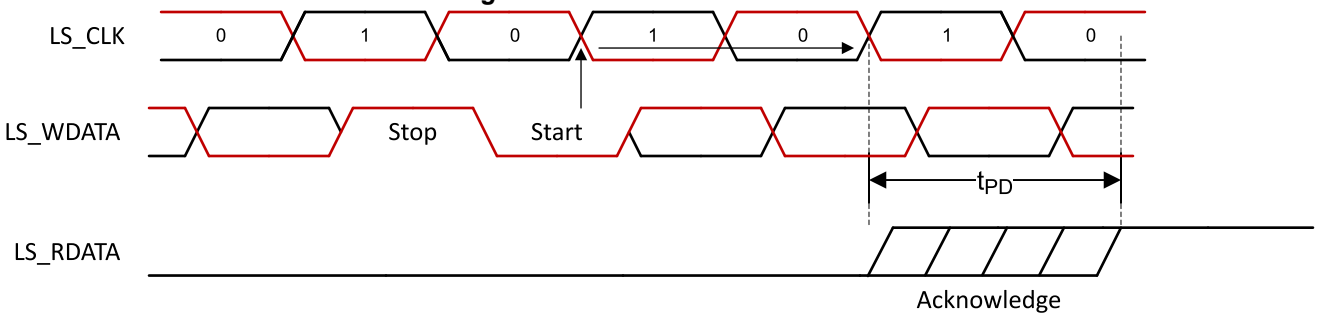


図 5-10. LPSDR Read Out

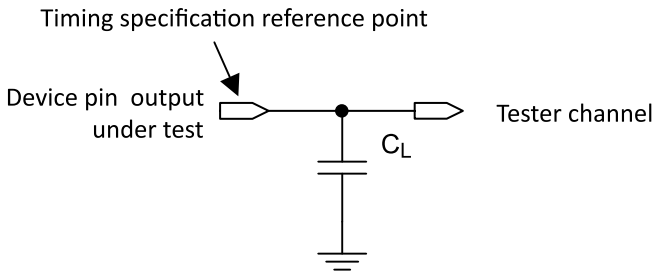


図 5-11. Test Load Circuit for Output Propagation Measurement

5.9 System Mounting Interface Loads

PARAMETER	Condition	MIN	NOM	MAX	UNIT
Thermal interface area	Maximum load uniformly distributed within each area (1)			90	N
Electrical interface area	Maximum load uniformly distributed within each area (1)			135	

(1) See Figure 5-12.

System Interface Loads Diagram

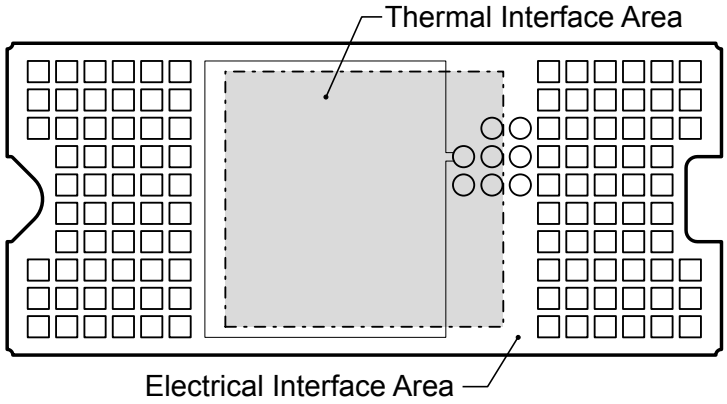


図 5-12. System Interface Loads

5.10 Micromirror Array Physical Characteristics

PARAMETER			VALUE	UNIT
M	Number of active columns(1)		960	micromirrors
N	Number of active rows(1)		960	micromirrors
ε	Micromirror (pixel) pitch—diagonal(1)		7.6	µm
P	Micromirror (pixel) pitch—horizontal and vertical(1)		10.8	µm

5.10 Micromirror Array Physical Characteristics (続き)

PARAMETER			VALUE	UNIT
	Micromirror active array width	(P × M) + (P / 2)	10.373	mm
	Micromirror active array height	(P x N) / 2 + (P / 2)	5.189	mm
	Micromirror active border	Pond of micromirrors (POM) (2)	10	micromirrors/side

(1) See 図 5-13.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

5.10.1 Micromirror Array Physical Characteristics Diagram

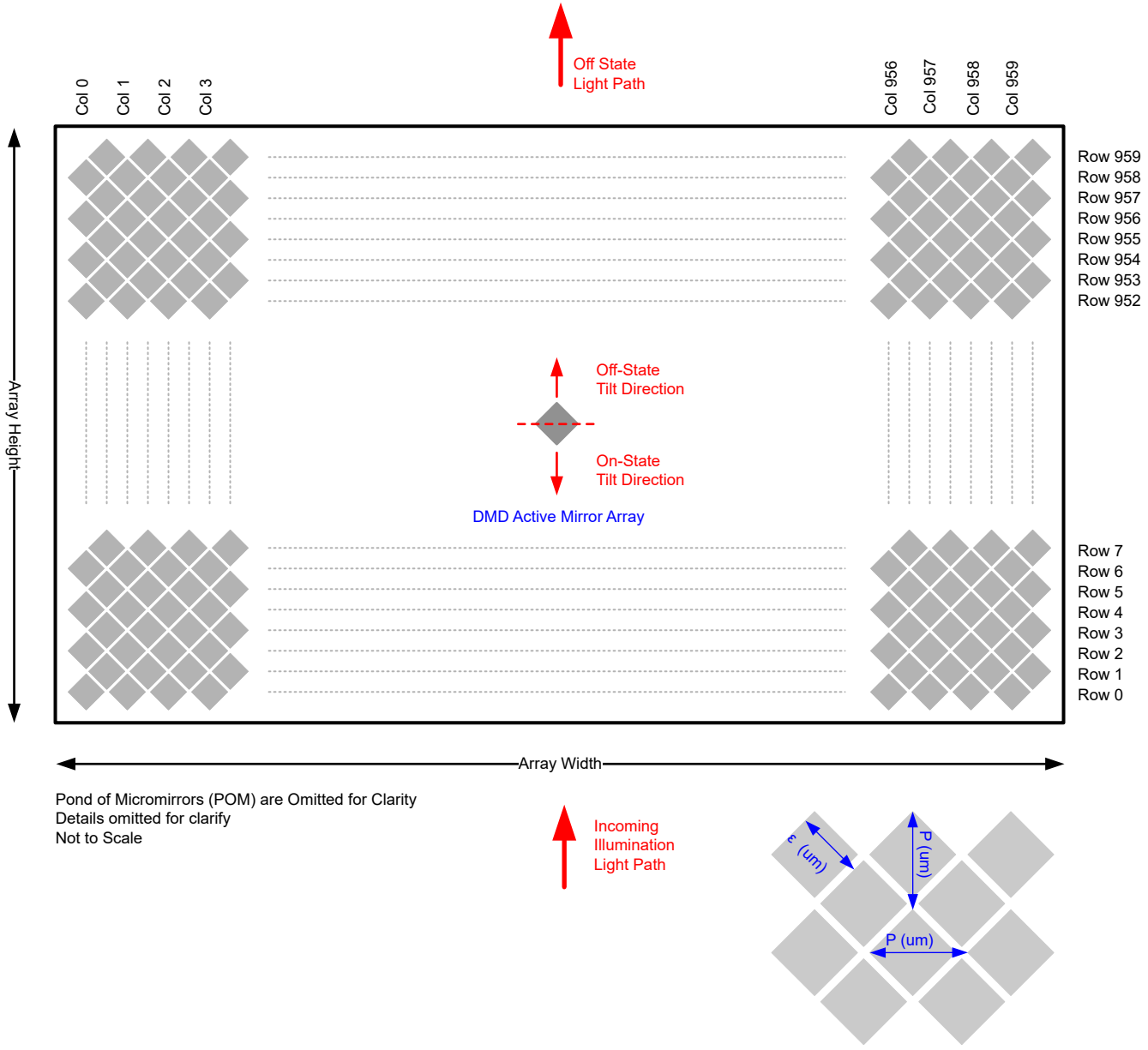


図 5-13. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		12		degree
Micromirror tilt angle tolerance(2)		–1		1	degree
DMD efficiency(3)	420nm – 700nm		66%		

(1) Measured relative to the plane formed by the overall micromirror array at 25°C.
(2) For some applications, it is critical to account for the micromirror tilt angle variation in the overall optical system design. With some optical system designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some optical system designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic micromirror landed duty-cycle and do not include system optical efficiency or overfill loss. This number is measured under conditions described above and deviations from these specified conditions can result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in *DMD Optical Efficiency for Visible Wavelengths Application Note*.

5.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546. nm		1.5119		
Window aperture (1)				See (1)	
Illumination overfill				See (1)	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

5.13 Chipset Component Usage Specification

The DLP4620S-Q1 is a component of a chipset. Reliable function and operation of the DLP4620S-Q1 requires that it be used in conjunction with the TPS99000S-Q1 and DLPC231S-Q1, and includes components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6 Detailed Description

6.1 Overview

The DLP4620S-Q1 automotive DMD consists of 921,600 highly reflective, digitally switchable, micrometer-sized mirrors organized in a two-dimensional array. As shown in Figure 6-13, the micromirror array consists of 960 micromirror columns × 960 micromirror rows in a diamond pixel configuration with a 2:1 aspect ratio.

Around the perimeter of the 960 × 960 array of micromirrors is a uniform band of border micromirrors called the Pond of Micromirrors (POM). The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 960 × 960 active array.

Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row. Each mirror is switchable between two discrete angular positions: –12° and +12°. The mirrors are illuminated from the bottom, which allows for compact and efficient system optical design.

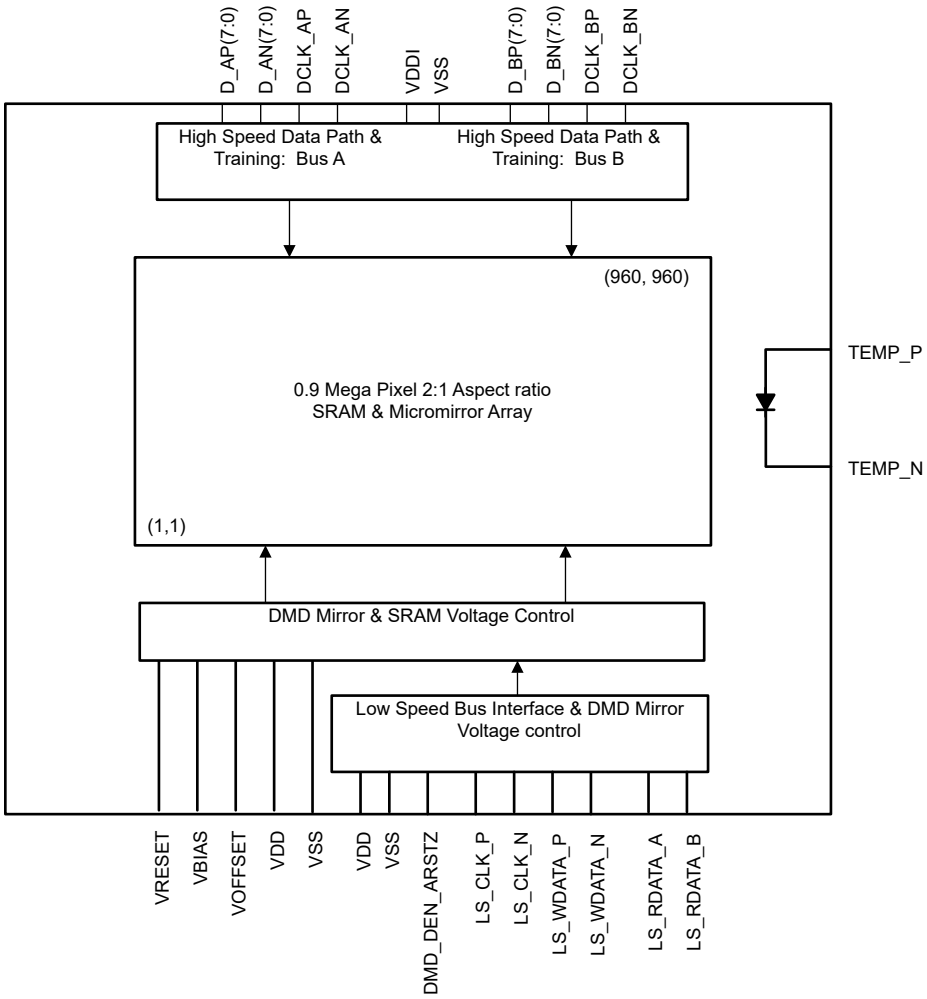
Although the native resolution of the DLP4620S-Q1 is 960 × 960 with an aspect ratio of 2:1, when paired with the DLPC231S-Q1 controller, the DLP4620S-Q1 can be driven with different resolutions. For example, a Head-Up Display system can use a resolution of 960 × 480 or 1920 × 960 with external quincunx processing before the DLPC231S-Q1. The DLPC231S-Q1 can also support resolutions of 1220 × 610 and 1358 × 566, which are displayed as 864 × 864 and 960 × 800 subimages on the 960 × 960 DLP4620S-Q1, respectively.

For more information on supported resolutions and associated processing with DLPC231S-Q1, refer to *DLPU041-DLPC230-Q1, DLPC230S-Q1 Programmer's Guide for Display Applications*. The table below summarizes the resolution options.

表 6-1. DLP4620S-Q1 Resolution Options

INPUT MANHATTAN RESOLUTION	EXTERNAL VIDEO PROCESSING REQUIRED	DMD DIAMOND MIRRORS USED
960 × 480	No	960 × 960
1220 × 610	No	864 × 864 (subimage)
1358 × 566	No	960 × 800 (subimage)
1920 × 960	Yes: Quincunx	960 × 960

6.2 Functional Block Diagram



6.3 Feature Description

The DLP4620S-Q1 consists of a two-dimensional array of 1-bit CMOS memory cells driven by a SubLVDS bus from the DLPC231S-Q1 and powered by the TPS99000S-Q1. The temperature sensing diode is used to continuously monitor the DMD array temperature.

To ensure reliable operation, the DLP4620S-Q1 must be used with the DLPC231S-Q1 DMD display controller and the TPS99000S-Q1 system management and illumination controller.

6.3.1 SubLVDS Data Interface

The SubLVDS signaling protocol was designed to enable very fast DMD data refresh rates while simultaneously maintaining low power and low emission.

Data is loaded into the SRAM under each micromirror using the SubLVDS interface from the DLPC231S-Q1. This interface consists of 16 pairs of differential data signals plus two clock pairs into two separate buses A and B loading the left and right half of the SRAM array. The data is latched on both transitions creating a double data rate (DDR) interface. The SubLVDS interface also implements a continuous training algorithm to optimize the data and clock timing to allow for a more robust interface.

The entire DMD array of 0.9 million pixels can be updated at a rate of less than 100µs as a result of the high-speed SubLVDS interface.

6.3.2 Low Speed Interface for Control

The purpose of the low speed interface is to configure the DMD at power up and power down and to control the micromirror reset voltage levels that are synchronized with the data loading. The micromirror reset voltage controls the time when the mirrors are mechanically switched. The low speed differential interface includes two pairs of signals for write data and clock, and two single-ended signals for output (A and B).

6.3.3 DMD Voltage Supplies

The micromirrors require unique voltage levels to control the mechanical switching from –12° to +12°. These voltage levels are nominally 16V, 8.5V, and –10V (VBIAS, VOFFSET, and VRESET), and are generated by the TPS99000S-Q1.

6.3.4 Asynchronous Reset

Reset of the DMD is required and controlled by the DLPC231S-Q1 through the signal DMD_DEN_ARSTZ.

6.3.5 Temperature Sensing Diode

The DMD includes a temperature-sensing diode designed to be used with the TMP411-Q1 temperature monitoring device. The DLPC231S-Q1 monitors the temperature sense diode through the TMP411-Q1. The DLPC231S-Q1 operation of the DMD timing can be adjusted based on the DMD array temperature, therefore this connection is essential to ensure reliable operation of the DMD.

図 6-1 shows the typical connection between the DLPC231S-Q1, TMP411-Q1, and the DMD.

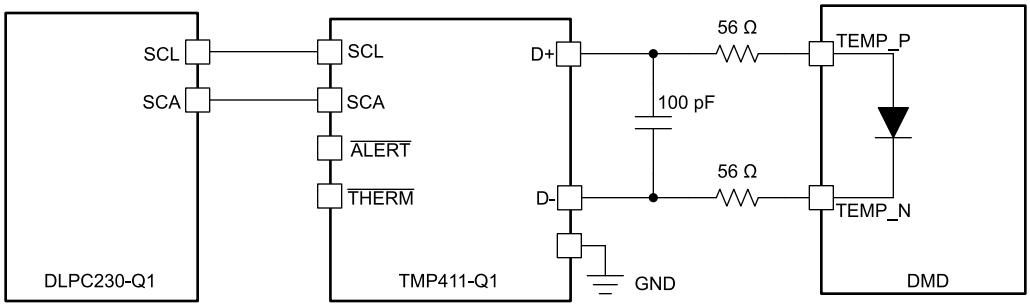


図 6-1. Temperature Sense Diode Typical Circuit Configuration

6.3.5.1 Temperature Sense Diode Theory

A temperature-sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Three different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411-Q1 data sheet for detailed information about temperature diode theory and measurement. 図 6-2 and 図 6-3 illustrate the relationships between the current and voltage through the diode.

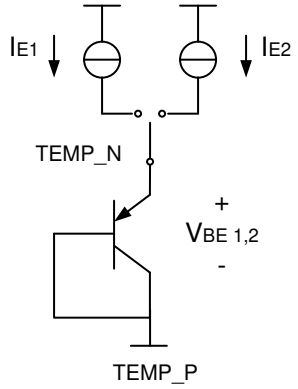


図 6-2. Temperature Measurement Theory

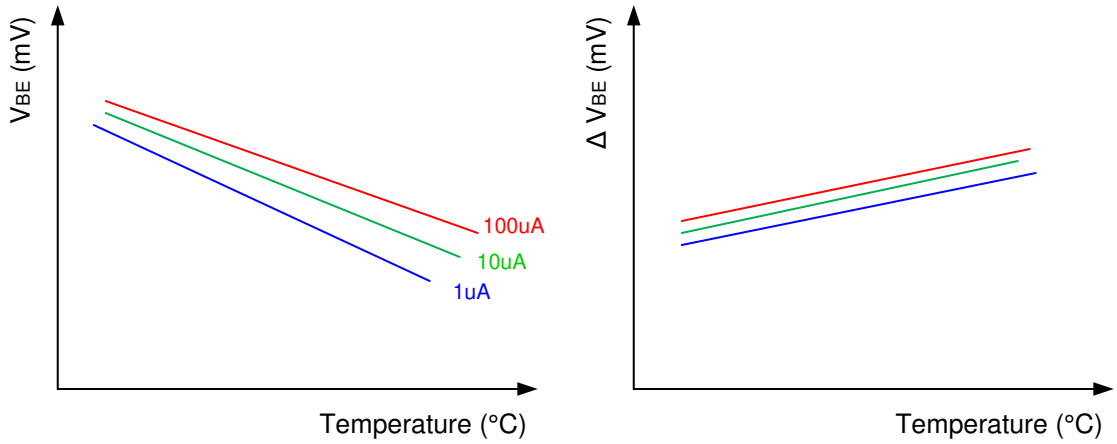


図 6-3. Example of Delta VBE Versus Temperature

6.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.4.1 Numerical Aperture and Stray Light Control

The numerical aperture of the illumination and projection optics at the DMD optical area must be the same. This cone angle defined by the numerical aperture must not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines the DMD's capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces.

6.4.2 Pupil Match

TI's optical and image performance specifications assume that the exit pupil of the illumination optics is nominally centered and located at the entrance pupil position of the projection optics. Misalignment of pupils between the illumination and projection optics can degrade screen image uniformity and cause objectionable artifacts in the display's border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.4.3 Illumination Overfill

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. Design the illumination optical system to minimize a light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible.

Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Heat load on the aperture in the areas shown in 図 5-1 must not exceed the values listed in the recommended operating conditions. This area is a 0.5mm wide area and length of the aperture opening. The values listed in *Recommended Operating Conditions* assume a uniform distribution. For a non-uniform distribution please contact TI for additional information.

注

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED PREVIOUSLY.

6.5 DMD Image Performance Specification

表 6-2. DMD Image Performance

PARAMETER(1) (2)	MIN	NOM	MAX	UNIT
Dark Blemishes—Viewed on a linear blue 60 screen(3)			4	
Light Blemishes—Viewed on a linear gray 10 screen			4	
Bright Pixels—Viewed on a linear gray 10 screen			0	micromirrors
Dark Pixels—Viewed on a white screen			4	micromirrors

(1) See the *System Optical Considerations* section.
(2) Blemish counts do not include reflections or shadows of the same artifact. Any artifact that is not specifically called out in this table is acceptable. Viewing distance must be > 60 inches. Screen size must be similar to application image size. All values referenced are in linear gamma. Non-linear gamma curves may be running by default, and are assured by a TI applications engineer that the equivalent linear gamma value as specified is used to judge artifacts.
(3) Linear gray 5 may be substituted in monochrome applications.

6.6 Micromirror Array Temperature Calculation

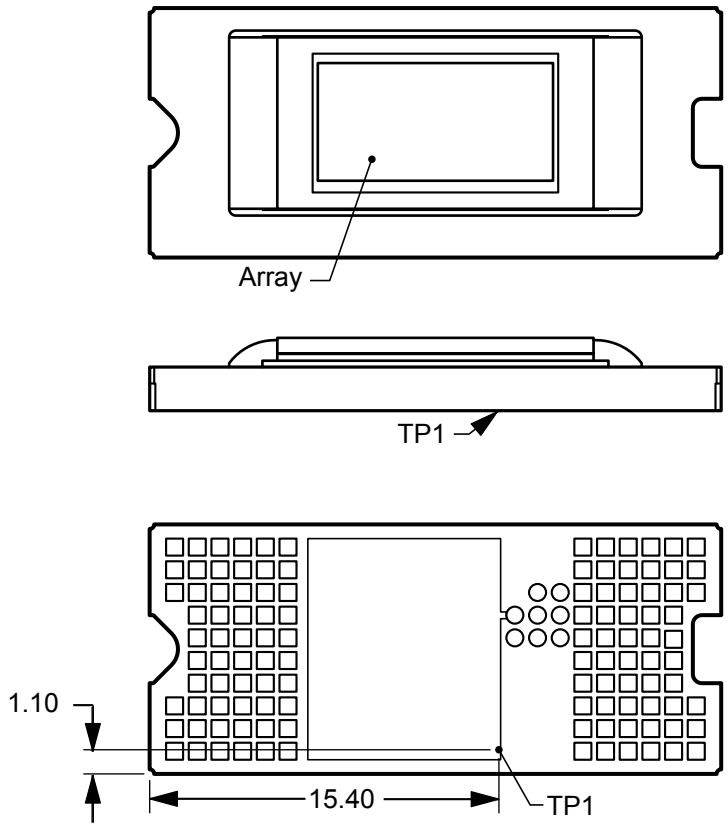


図 6-4. DMD Thermal Test Points

The active array temperature can be computed analytically from the thermal measurement point on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations provide the relationship between the array temperature and the reference ceramic temperature (TP1) in 図 6-4:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ILLUMINATION} = (Q_{INCIDENT} \times \text{DMD Absorption Constant}) \quad (2)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (3)$$

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature at the TP1 location in 図 6-4 (°C)
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to thermal test point TP1 (°C/W),
- Q_{ARRAY} = total power (electrical plus absorbed) on the DMD array (W)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The DMD absorption constant is a function of illumination distribution on the active array and the array border, angle of incidence (AOI), f number of the system, and operating state of the mirrors. The absorption constant is

higher in the OFF state than in the ON state. Equations to calculate the absorption constant are provided for both ON and OFF mirror states. They assume an AOI of 34 degrees, an f/1.7 system, and they account for the distribution of light on the active array, POM, and array border.

$$\text{DMD Absorption Constant (OFF state)} = 0.895 - 0.004783 \times (\%\text{ of light on ActiveArray + POM}) \quad (4)$$

$$\text{DMD Absorption Constant (ON state)} = 0.895 - 0.007208 \times (\%\text{ of light on ActiveArray + POM}) \quad (5)$$

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. $T_{CERAMIC}$ = 50°C (measured)
2. $Q_{INCIDENT}$ = 10W (measured)
3. DMD Absorption Constant = 0.895 – 0.004783 × 90 = 0.46
4. $Q_{ELECTRICAL}$ = 0.4W
5. $R_{ARRAY–TO–CERAMIC}$ = 1.3°C/W
6. Q_{ARRAY} = 0.4W + (0.46 x 10 W) = 5W
7. T_{ARRAY} = 50°C × (5W × 1.3°C/W) = 56.5°C

When designing the DMD heatsink solution, the package thermal resistance from array to reference ceramic temperature (thermocouple location TP1 can be used to determine the temperature rise through the package as given by the following equations:

$$T_{ARRAY\text{-}TO\text{-}CERAMIC} = Q_{ARRAY} \times R_{ARRAY–TO–CERAMIC} \quad (6)$$

6.6.1 Monitoring Array Temperature Using the Temperature Sense Diode

The active array temperature can be computed analytically from the temperature sense diode measurement, the thermal resistance from array to diode, the electrical power, and the illumination heat load. The relationship between array temperature and the temperature sense diode is provided by the following equations:

$$T_{ARRAY} = T_{DIODE} + (Q_{ARRAY} \times R_{ARRAY–TO–DIODE}) \quad (7)$$

$$Q_{ILLUMINATION} = (Q_{INCIDENT} \times \text{DMD Absorption Constant}) \quad (8)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (9)$$

where

- T_{ARRAY} = computed array temperature (°C)
- T_{DIODE} = measured temperature sense diode temperature (°C)
- $R_{ARRAY–TO–DIODE}$ = package thermal resistance from array to diode (°C/W)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (W)
  Refer to Section 7.6 for details.
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION}$ = absorbed illumination heat load (W)
- $Q_{INCIDENT}$ = incident power on the DMD (W)

The temperature sense diode to array thermal resistance ($R_{ARRAY–TO–DIODE}$) assumes a uniform illumination distribution on the DMD.

The following sample calculations assume 10% of the total incident light falls outside of the active array and POM, and the mirrors are in the OFF state.

1. T_{DIODE} = 55°C
2. $Q_{INCIDENT}$ = 10W (measured)

3. DMD Absorption Constant = 0.895 – 0.004783 × 90 = 0.46
4. $Q_{ELECTRICAL}$ = 0.4W
5. $R_{ARRAY–TO–DIODE}$ = 0.1°C/W
6. Q_{ARRAY} = 0.4W + (0.46 × 10W) = 5W
7. T_{ARRAY} = 55°C + (5 W × 0.1°C/W) = 55.5°C

6.7 Micromirror Landed-On/Landed-Off Duty Cycle

6.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DLP4620S-Q1 chipset is designed to support projection-based automotive applications such as head-up display systems.

7.2 Typical Application

The chipset consists of three components—the DLP4620S-Q1 automotive DMD, the DLPC231S-Q1, and the TPS99000S-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC231S-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99000S-Q1 is a high-performance voltage regulator for the DMD, a controller for the illumination sources (for example, LEDs or lasers), and a management IC for the entire chipset. In conjunction, the DLPC231S-Q1 and the TPS99000S-Q1 can be used for system-level monitoring, diagnostics, and failure detection features. 図 7-1 is a system-level block diagram with these devices in the DLP head-up display configuration and displays the primary features and functions of each device.

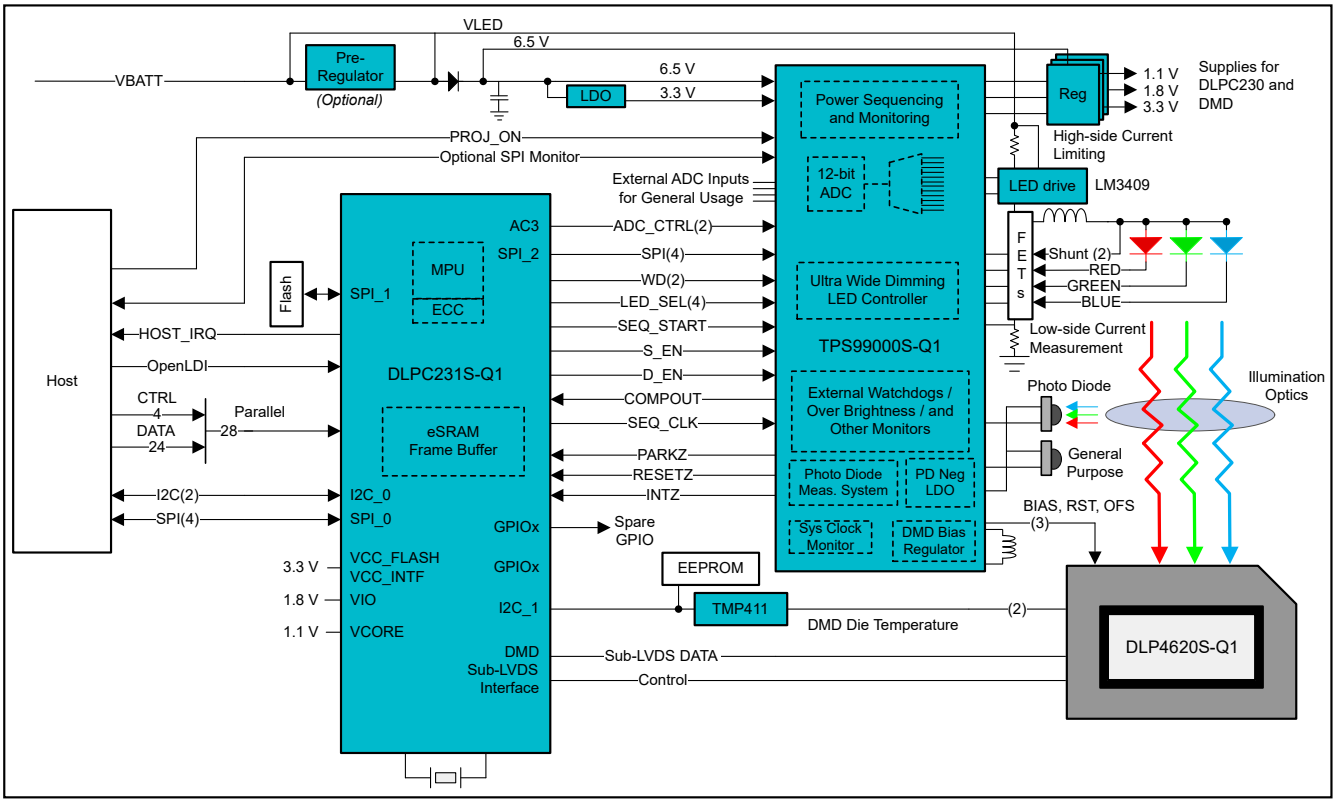


図 7-1. HUD System Block Diagram

7.2.1 Application Overview

図 7-1 shows the system block diagram for a DLP HUD module. The system uses the DLPC231S-Q1, TPS99000S-Q1, and the DLP4620S-Q1 automotive DMD to enable a head-up display with high brightness, high efficiency, and a large virtual image distance. The combination of the DLPC231S-Q1 and TPS99000S-Q1 removes the need for external SDRAM and a dedicated microprocessor. The chipset manages the illumination control of LED sources, power sequencing functions, and system management functions. Additionally, the chipset supports numerous system diagnostic and built-in self-test (BIST) features. The following paragraphs describe the functionality of the chipset used for a HUD system in more detail.

The DLPC231S-Q1 is a controller for the DMD and the light sources in the DLP Headlight, HUD, or Projector module. It receives input video from the host and synchronizes DMD and light source timing to achieve the desired video. The DLPC231S-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing to create a video with grayscale shading and multiple colors, if applicable.

The DLPC231S-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Host commands can be sent using either the I^2C bus or the SPI bus. The bus that is not being used for host commands can be used as a read-only bus for diagnostic purposes. The input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits or 16-bits of data for single light source or dual light source systems depending on the system design. The SPI flash memory provides the embedded software for the DLPC231S-Q1's ARM core, any calibration data, and default settings. The TPS99000S-Q1 provides diagnostic and monitoring information to the DLPC231S-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^2C interface to provide the DMD array temperature to the DLPC231S-Q1.

The outputs of the DLPC231S-Q1 are configuration and monitoring commands to the TPS99000S-Q1, timing controls to the LED or laser driver, control and data signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC231S-Q1 communicates with the TPS99000S-Q1 over an SPI bus. It uses this to configure the TPS99000S-Q1 and to read monitoring and diagnostics information from the TPS99000S-Q1. The DLPC231S-Q1 sends drive-enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a SubLVDS interface.

The TPS99000S-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the DLP HUD system. The power sequencing and monitoring blocks of the TPS99000S-Q1 properly power up the DMD and provide accurate DMD voltage rails (–16V, 8.5V, and 10V), and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000S-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000S-Q1 has several general-purpose ADCs that designers can use for system-level monitoring, such as over-brightness detection.

The TPS99000S-Q1 receives inputs from the DLPC231S-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC231S-Q1 sends configuration and control commands to the TPS99000S-Q1 over an SPI bus and several other control signals. The DLPC231S-Q1's clocks are also monitored by the watchdogs in the TPS99000S-Q1 to detect any errors. The power rails are monitored by the TPS99000S-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000S-Q1 using a dedicated SPI bus, which enables independent monitoring. Additionally, the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000S-Q1 has several general-purpose ADCs that can be used to implement system-level monitoring functions.

The outputs of the TPS99000S-Q1 are diagnostic information and error alerts to the DLPC231S-Q1, and control signals to the LED or laser driver. The TPS99000S-Q1 can output diagnostic information to the host and the DLPC231S-Q1 over two SPI buses. In case of critical system errors, such as power loss, it outputs signals to the DLPC231S-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a SubLVDS interface with the DLPC231S-Q1. The mechanical output is the state of more than 0.9 million mirrors in the DMD array that can be tilted ±12°. In a projection system, the mirrors are used as pixels to display an image.

7.2.2 Input Image Resolution

The DLP4620S-Q1 together with the DLPC231S-Q1 supports different display resolutions, some include diamond down sampling (DDS). For information on how the input image is displayed onto the DLP4620S-Q1 and DDS function, refer to the *DLPC230-Q1, DLPC230S-Q1 Programmer's Guide for Display Applications.*

7.2.3 Reference Design

For information about connecting together the DLP4620S-Q1 DMD, DLPC231S-Q1 controller, and TPS99000S-Q1, contact the TI Application Team for additional information about the DLP4620S-Q1 evaluation module (EVM). TI has optical-mechanical reference designs available; contact the TI Application team for more information.

7.2.4 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles or number of operating hours at different temperatures. To assist in evaluation an Application Report may be provided in the future. Contact the TI Application team for more information.

7.3 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the TPS99000S-Q1 device.

> **注意**
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.
>
> VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. VSS must also be connected.

7.3.1 Power Supply Power-Up Procedure

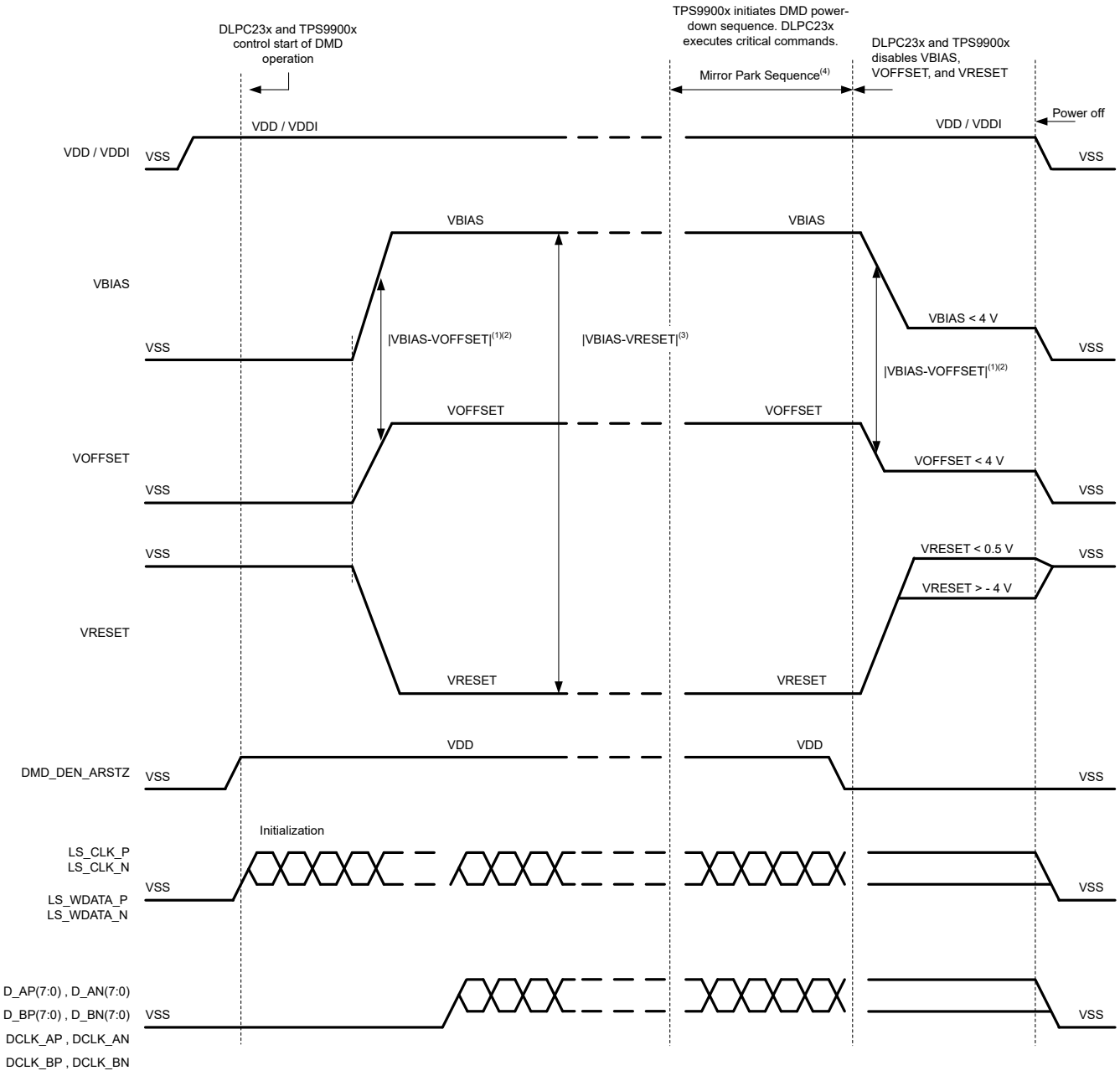
- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the *Recommended Operating Conditions* specified limit.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in 図 7-2.

7.3.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the *Recommended Operating Conditions* specified limit.

- During power-down, the DMD's LPSDR input pins must be less than VDDI, the *Recommended Operating Conditions* specified limit.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in the *Power Supply Sequencing Requirements (Power Up and Power Down)* graphic.

7.3.3 Power Supply Sequencing Requirements



1. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the *Recommended Operating Conditions* specified. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Also, the TPS99000S-Q1 is capable of managing the timing between VBIAS and VOFFSET.

2. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified than the *Recommended Operating Conditions* limit shown.
3. When system power is interrupted, the TPS99000S-Q1 initiates hardware power-down that disables VBIAS, VRESET, and VOFFSET after the Micromirror Park Sequence.
4. LS_CLK and LS_WDATA signals are ignored until DMD_DEN_ARSTZ is released.
5. The drawing is not to scale and details are omitted for clarity. For example, the DLPC231S-Q1 will read information from DLP4620S-Q1 during initialization and activity on LS_CLK, LSWDATA, and DMD_DEN_ARSTZ may toggle multiple times prior to displaying information on DLP4620S-Q1.

図 7-2. Power Supply Sequencing Requirements (Power Up and Power Down)

7.4 Layout Guidelines

Refer to the DLPC231S-Q1 and TPS99000S-Q1 data sheets for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- Match lengths for the LS_WDATA and LS_CLK signals
- Minimize vias, layer changes, and turns for the HS bus signals
- Minimum of two 220nF decoupling capacitors close to VBIAS
- Minimum of two 220nF decoupling capacitors close to VRESET
- Minimum of three 4.7µF decoupling capacitors close to VOFFSET
- Minimum of four 100nF decoupling capacitors close to VDDI and VDD
- Temperature diode pins

  The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411 are sensitive to noise. See the *TMP411 ±1°C Remote and Local Temperature Sensor with N-Factor and Series Resistance Correction Data Sheet* for specific routing recommendations.

7.5 Layout Example

The DLP4620S-Q1 example layouts are shown for high-speed SubLVDS pairs and the micromirror voltage supplies (VBIAS, VOFFSET, and VRESET). The 1.8V power supplies must have a dedicated power plane.

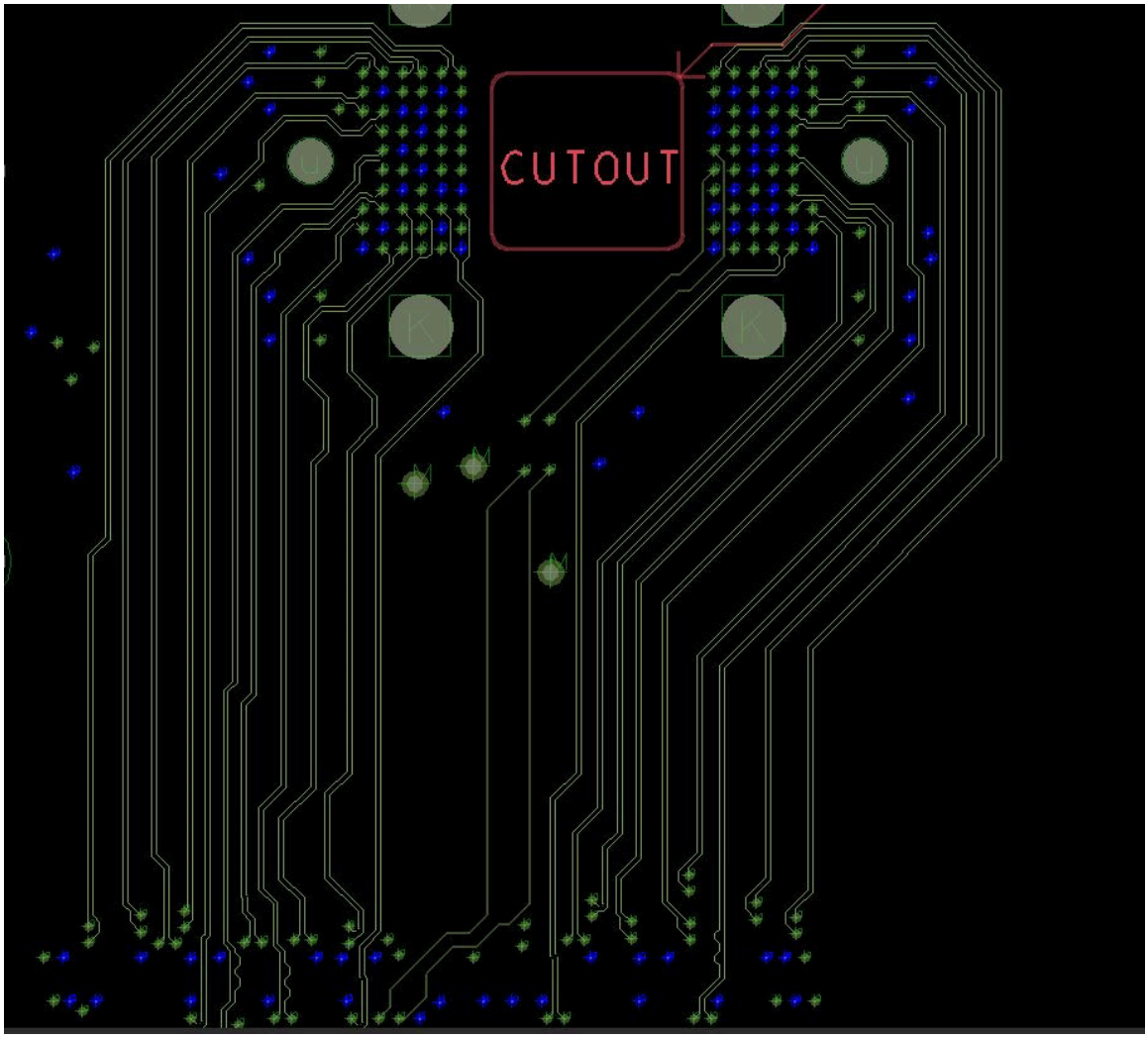


図 7-3. High-Speed SubLVDS Pairs

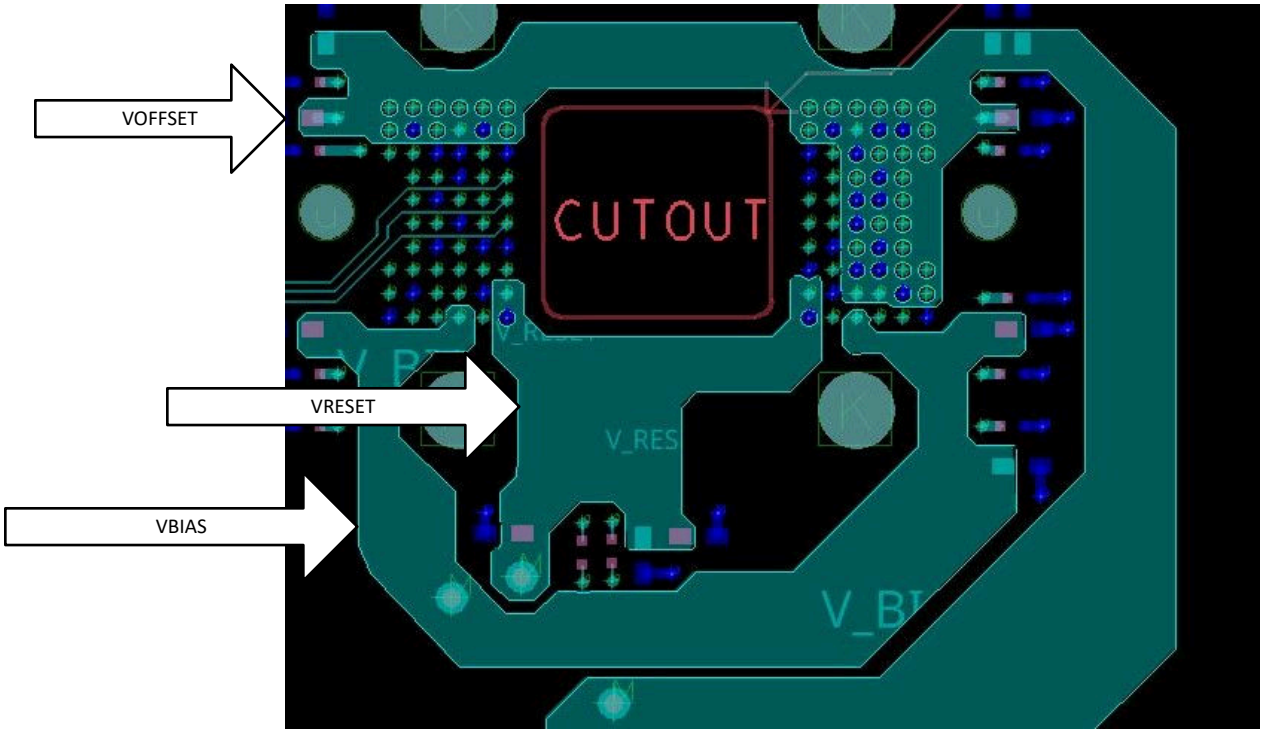


図 7-4. DMD Micromirror Supply Voltages (VBIAS, VOFFSET, and VRESET)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

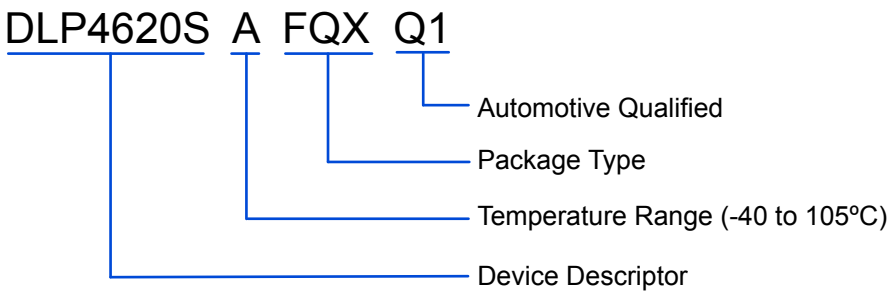


図 8-1. Part Number Description

8.1.2 Device Markings

The device marking includes the legible character string GHJJJJK DLP4620SAFQXQ1. GHJJJJK is the lot trace code. DLP4620SAFQXQ1 is the part number.

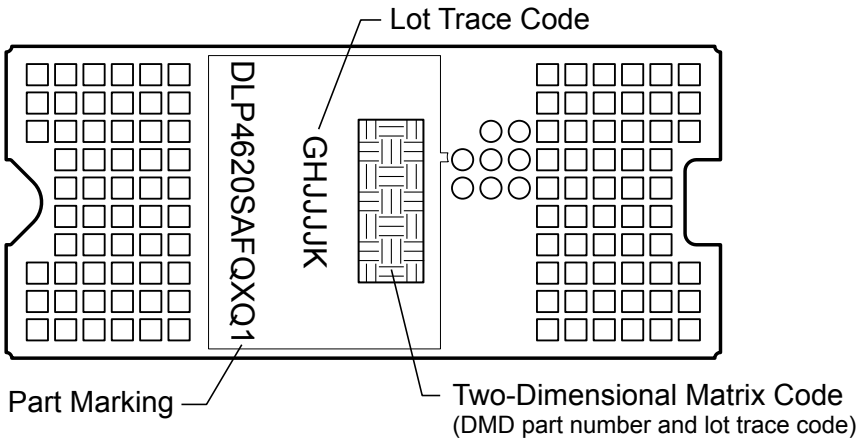


図 8-2. DMD Marking

8.2 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 DMD Handling

The DMD is an optical device so take precautions to avoid damaging the glass window. See the application note DLPA019 DMD Handling for instructions on how to properly handle the DMD.

8.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2024) to Revision C (August 2024)	Page
• Updated the clock frequency, DCLK, for the high-speed interface in Recommended Operating Conditions	9
• Updated the clock frequency, DCLK, for the high-speed interface in Timing Requirements	11

Changes from Revision A (February 2023) to Revision B (February 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」	1
• Clarified test pad functions in 表 4-2	3
• Updated ESD Ratings; Updated Current and Power Consumption in *Electrical Characteristics*	8

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP4620SAFQXQ1	Active	Production	CLGA (FQX) | 120	72 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	
DLP4620SAFQXQ1.A	Active	Production	CLGA (FQX) | 120	72 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

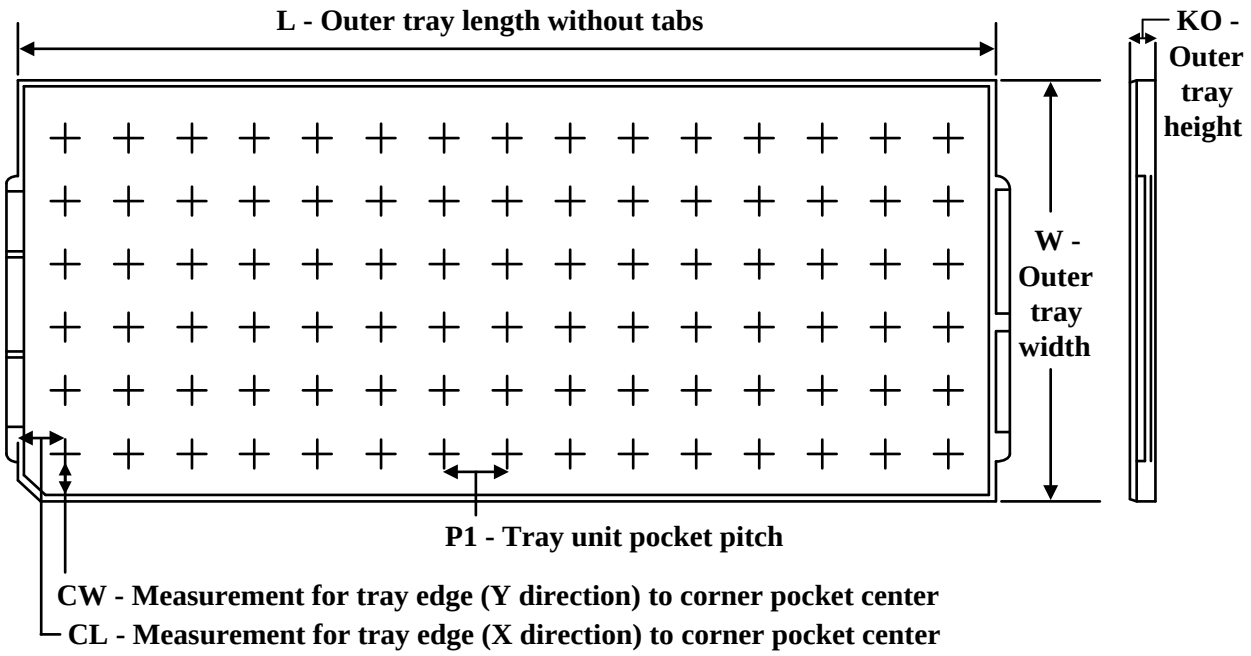
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP4620SAFQXQ1	FQX	CLGA	120	72	8 x 7	150	315	135.9	12190	21.9	15.15	16.95
DLP4620SAFQXQ1.A	FQX	CLGA	120	72	8 x 7	150	315	135.9	12190	21.9	15.15	16.95

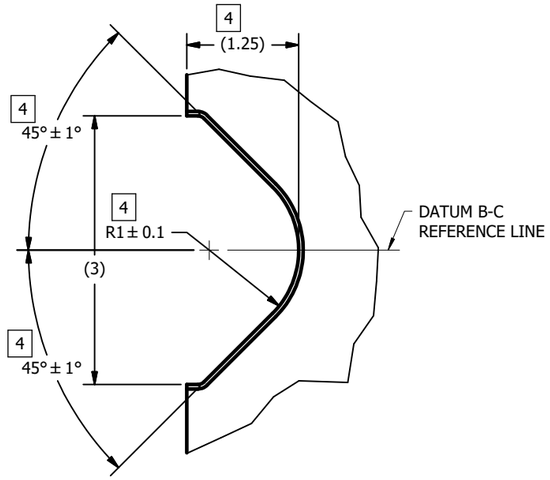
DWG NO. 2518197 SH 1

REVISIONS

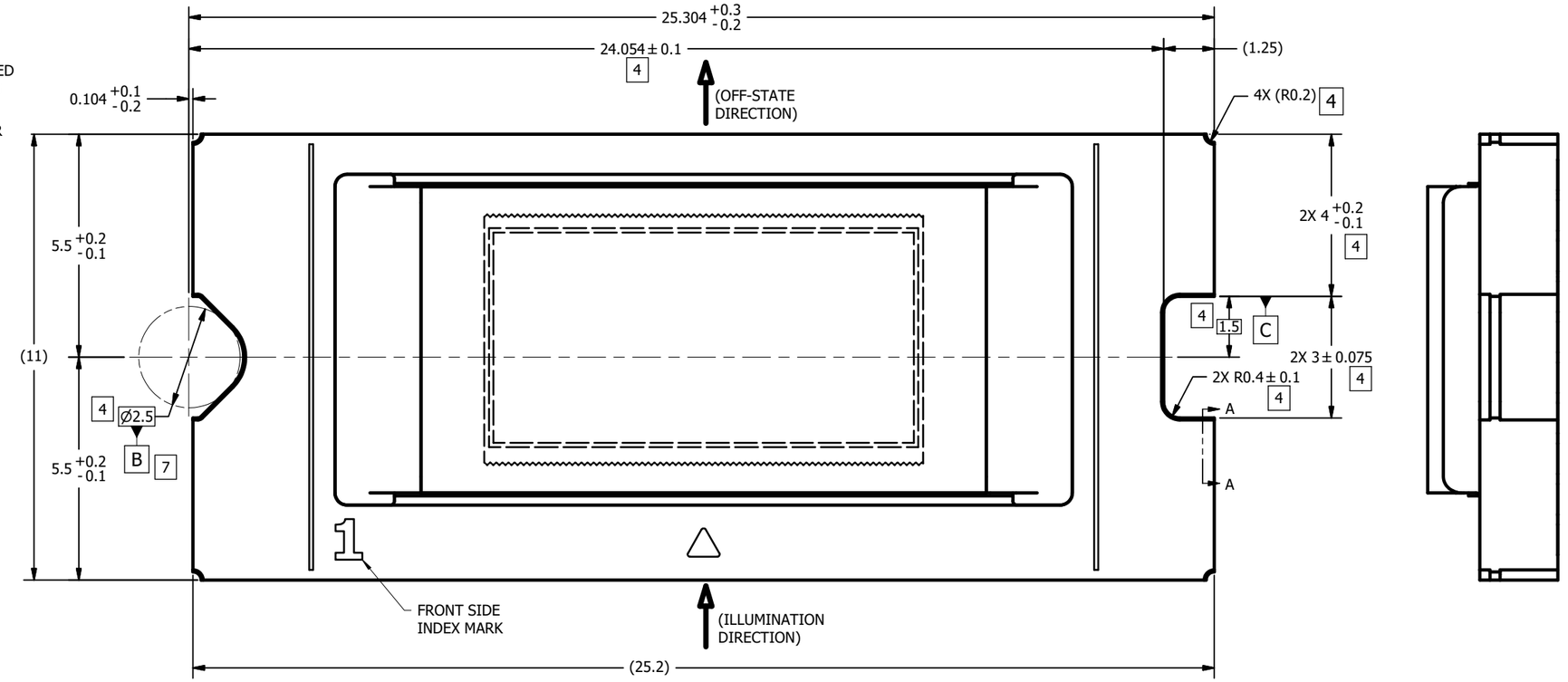
REV	DESCRIPTION	DATE	BY
A	ECO 2199615: INITIAL RELEASE	4/19/2022	BMH
B	ECO 2200854: TOLERANCE RIGHT & BOTTOM EDGES FROM DATUMS B/C, INSTEAD OF FROM LEFT & TOP EDGES	8/1/2022	BMH

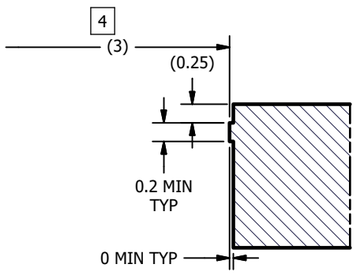
NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY SECOND LAYER OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 3). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
9. SHORTING TEST PADS AND SYMBOLIZATION PAD TO EACH OTHER AND/OR TO VSS IS ACCEPTABLE.

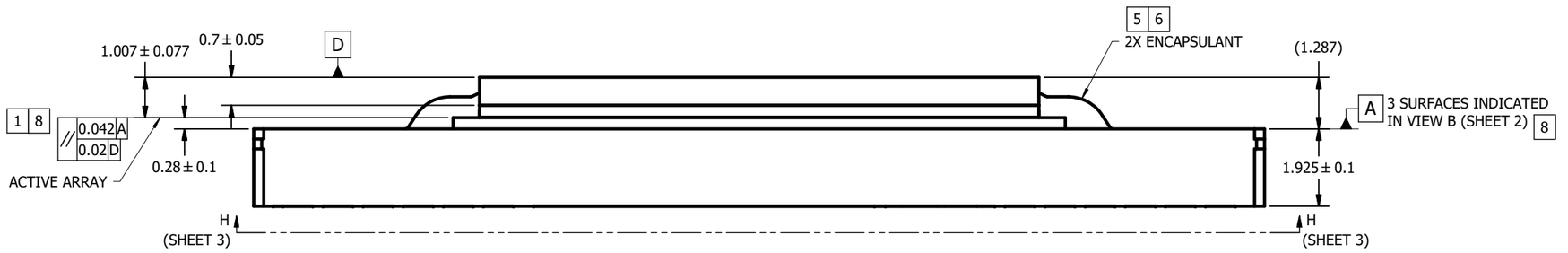


DETAIL B
V-NOTCH
SCALE 30 : 1





SECTION A-A
NOTCH OFFSETS
SCALE 25 : 1
(ROTATED 90°)



	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	4/19/2022
ENGINEER	B. HASKETT	4/19/2022
QA/CE	P. KONRAD	4/20/2022
CM	B. HASKETT	4/27/2022
	J. McKINLEY	4/27/2022
APPROVED	B. RAY	4/21/2022

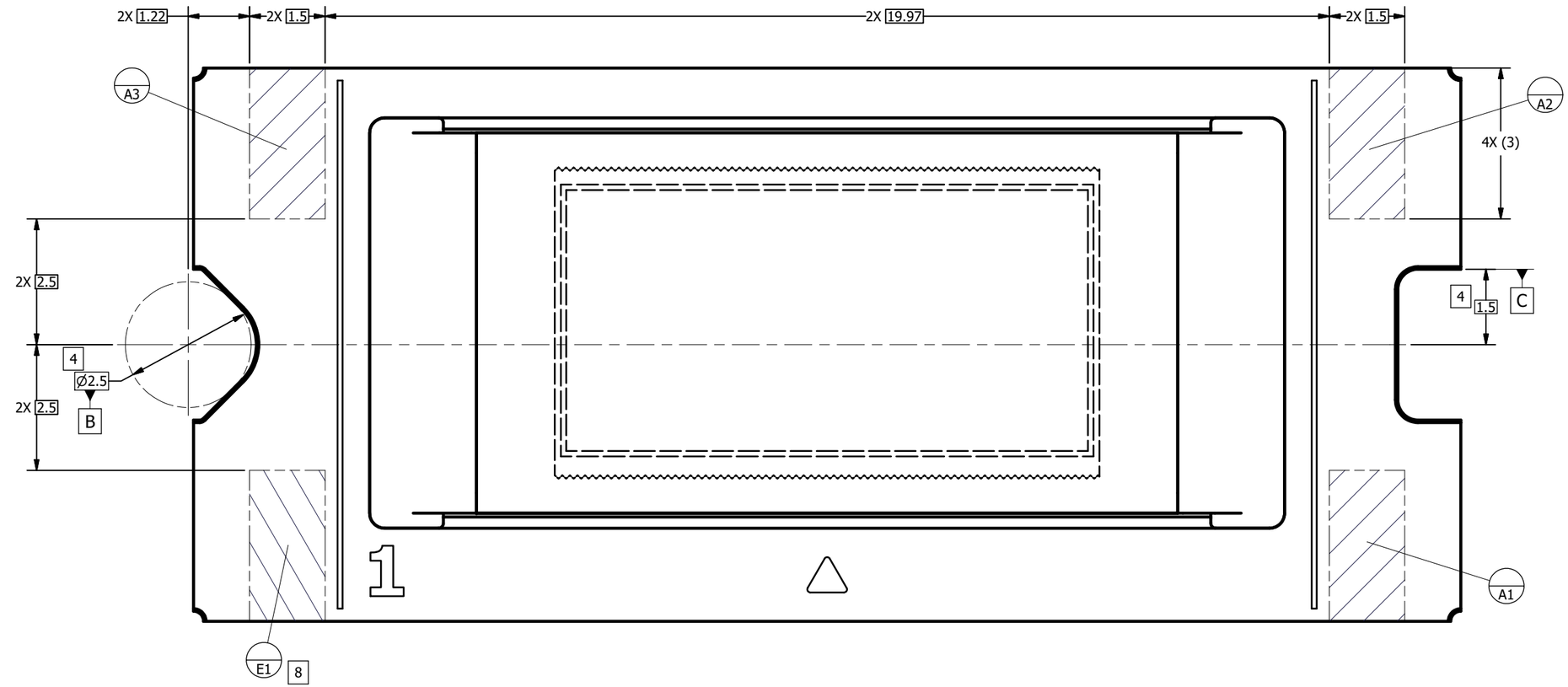
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .46 AUTO SERIES 320 (FQX PACKAGE)

SIZE	DWG NO	REV
D	2518197	B

SCALE 15:1 SHEET 1 OF 5

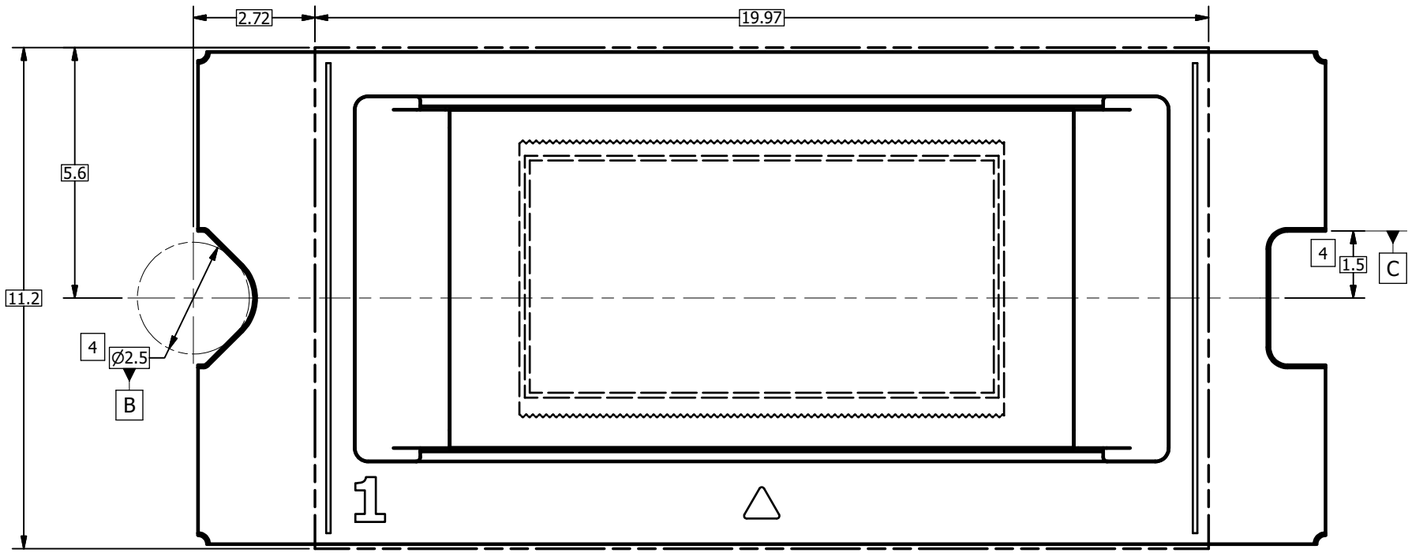
INV11-2006a



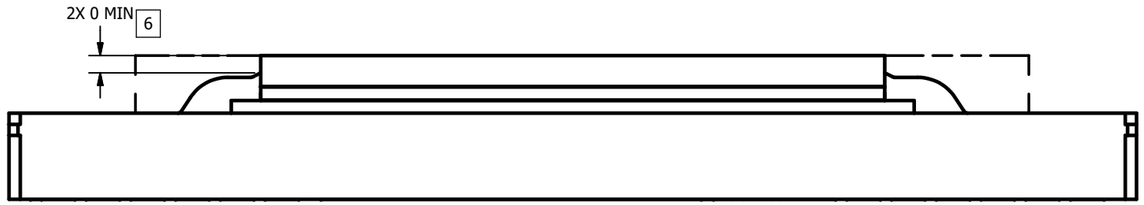
VIEW C
DATUMS A AND E
SCALE 20 : 1
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 4/19/2022	SIZE D	DWG NO 2518197	REV B
			SCALE	SHEET 2 OF 5	

INV11-2006a



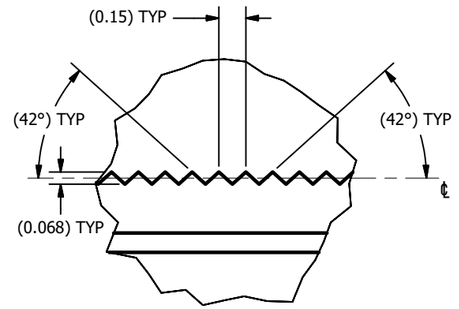
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS [5]
(FROM SHEET 1)



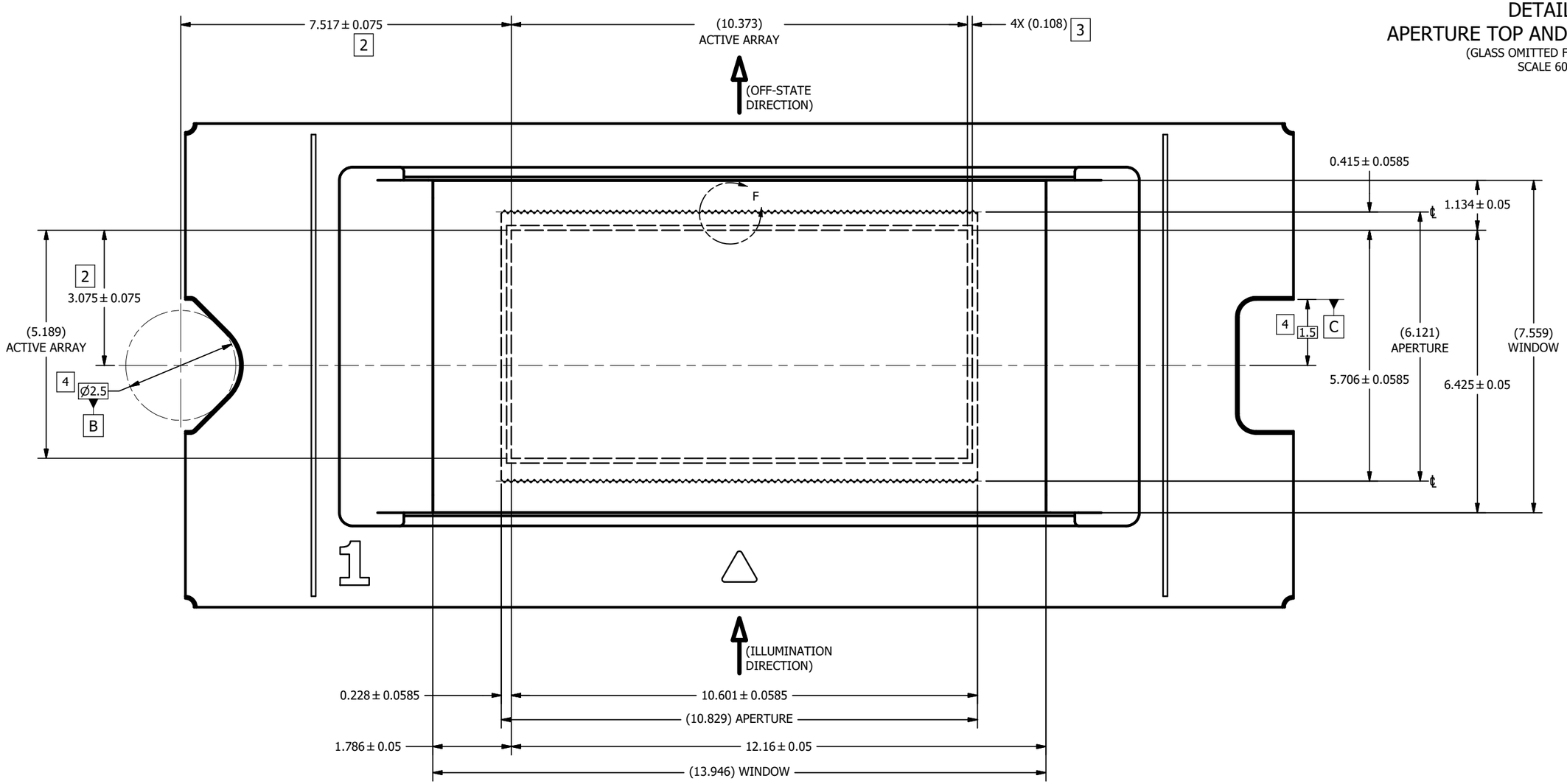
VIEW E
ENCAPSULANT MAXIMUM HEIGHT

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 4/19/2022	SIZE D	DWG NO 2518197 REV B
			SCALE	SHEET 3 OF 5

INV11-2006a



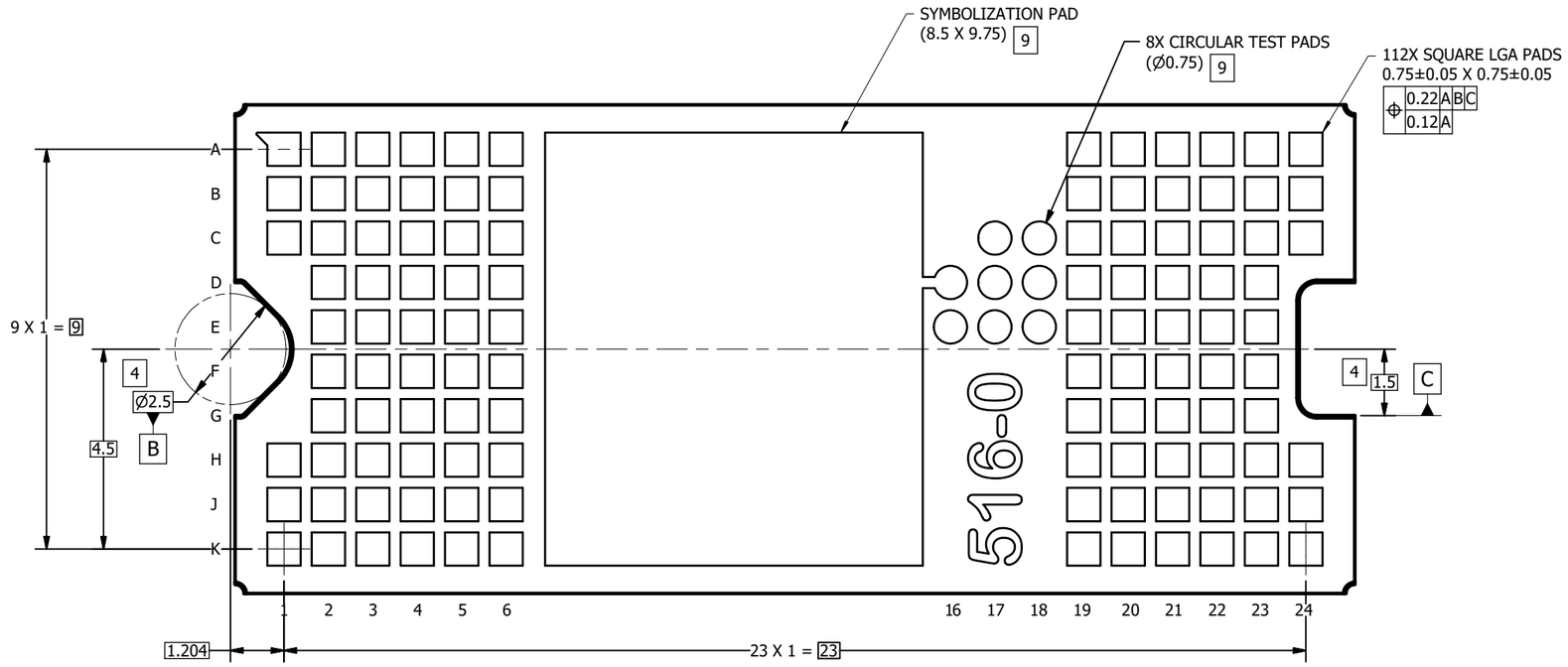
DETAIL F
APERTURE TOP AND BOTTOM EDGES
(GLASS OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW E
WINDOW AND ACTIVE ARRAY
SCALE 20 : 1
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 4/19/2022	SIZE D		DWG NO 2518197	REV B
			SCALE		SHEET 4 OF 5	

INV11-2006a



VIEW H-H
BACK SIDE METALLIZATION
SCALE 15 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 4/19/2022	SIZE D	DWG NO 2518197	REV B
			SCALE	SHEET 5 OF 5	

INV11-2006a

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月