DLP500YX 0.50 2048 x 1200 DMD

1 特長

- 高解像度の 2048 × 1200 アレイ
  - 2.4M 超のミラー
  - 対角 0.50 インチ (16.5mm) のマイクロミラー・アレイ
  - マイクロミラー・ピッチ:5.4 ミクロン
  - マイクロミラー傾斜角:±17.5° (平面に対して)
  - 下部光源向けの設計
  - マイクロミラー・ドライバ回路を内蔵
- 広帯域の可視光 (420nm～700nm) で使用するよう設計
  - ウィンドウ透過率 97% (シングル・パス、ウィンドウ表面を 2 回通過)
  - マイクロミラーの反射率 88%
  - アレイ回折効率 84% (f/2.4)
  - アレイの充填率 93%
- 4 つの 16 ビット、低電圧差動信号 (LVDS) のダブル・データ・レート (DDR) 入力データ・バス
- デュアル DLPC900 デジタル・コントローラで駆動
  - 最大 16.1kHz、1 ビット・パターン/秒
  - 保存済みパターン・モードで 39.6 ギガビット/秒のピクセル・データ・レートに相当
  - 最大 2016Hz 8 ビット・グレー・パターン・レート (照明変調による保存済みパターン)
  - 最大 1008Hz 16 ビット・グレー・パターン・レート (照明変調による保存済みパターン)
  - 最大 247Hz 8 ビット・パターン・レート (外部ビデオ・パターン入力)

2 アプリケーション

- 産業用
  - マシン・ビジョン用の 3D スキャナ
  - 3D タッチレス計測および品質管理
  - 3D プリンティング
- 医療用
  - 眼科用
  - 四肢および皮膚測定用の 3D スキャナ
  - ハイパー・スペクトル・スキャンおよび画像処理
- ディスプレイ
  - 3D 画像処理顕微鏡
  - インテリジェントおよび適応型照明

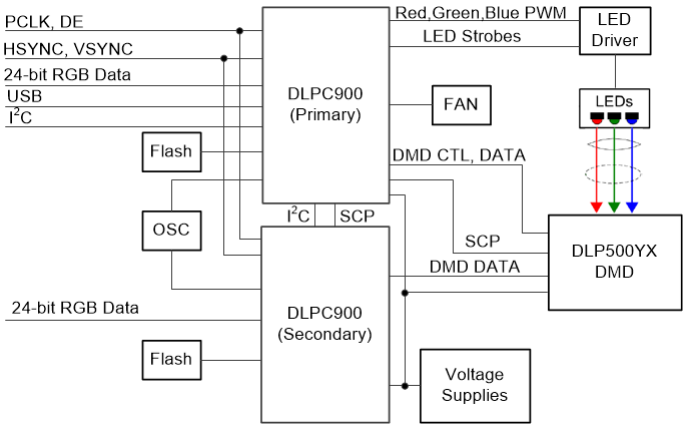
3 概要

DLP500YX デジタル ・マイクロミラー ・デバイス (DMD) は、入射光の振幅、方向、位相を変調する空間光変調器 (SLM) です。この DMD を 4 つの 2xLVDS 入力データ・バスと組み合わせると、非常に高いパターン更新レートで高解像度パターンを表示できます。DLP500YX は、高分解能で高速なパターン・レートを実現しており、さまざまな産業用、医療用、および高度な画像処理アプリケーションのサポートに最適です。DLP500YX の信頼性の高い機能と動作は、デュアル DLPC900 デジタル・コントローラと組み合わせて使用することで実現できます。この専用チップセットは、さまざまな最終製品ソリューションの要件を満たすために必要な高いパターン・レートで、プログラムが容易でフレキシブルなパターン・ストリームを提供します。

表 3-1. 製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DLP500YX	FXK (257)	32.2mm × 22.3mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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4 Revision History

Changes from Revision * (November 2020) to Revision A (July 2022)	Page
• This document is updated per the latest Texas Instruments and industry data sheet standards	11
• Updated Timing Requirements	16

5 Pin Configuration and Functions

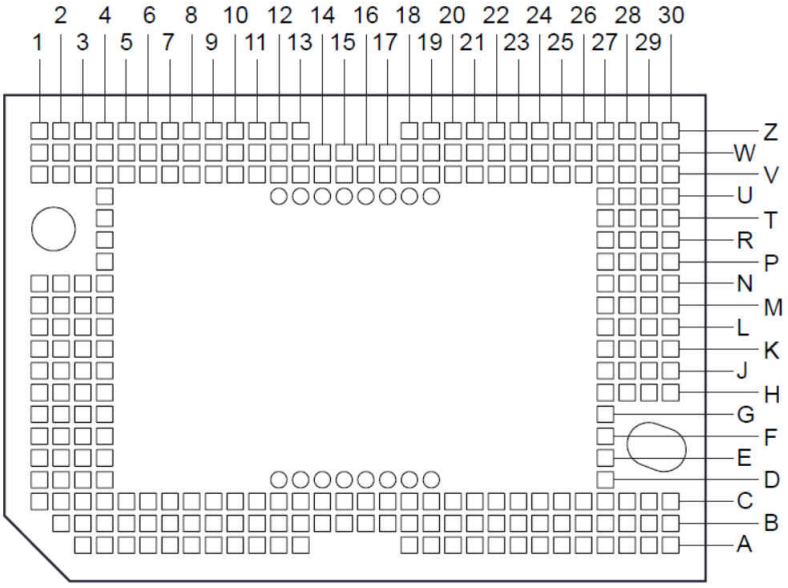


図 5-1. FXK Package 257-Pin CLGA Bottom View

> **注意**
>
> To ensure reliable, long-term operation of the DLP500YX DMD, it is critical to properly manage the layout and operation of the signals identified in Pin Functions . For specific details and guidelines, refer to セクション 10.1 section before designing the board.

表 5-1. Pin Functions

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
D_AN(0)	C6	Input	LVDS	DDR	Differential	Data negative	805
D_AN(1)	C3						
D_AN(2)	E1						
D_AN(3)	C4						
D_AN(4)	D1						
D_AN(5)	B8						
D_AN(6)	F4						
D_AN(7)	E3						
D_AN(8)	C11						
D_AN(9)	F3						
D_AN(10)	K4						
D_AN(11)	H3						
D_AN(12)	J3						
D_AN(13)	C13						
D_AN(14)	A5						
D_AN(15)	A3						

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
D_AP(0)	C7	Input	LVDS	DDR	Differential	Data positive	805
D_AP(1)	C2						
D_AP(2)	E2						
D_AP(3)	B4						
D_AP(4)	C1						
D_AP(5)	B7						
D_AP(6)	E4						
D_AP(7)	D3						
D_AP(8)	C12						
D_AP(9)	F2						
D_AP(10)	J4						
D_AP(11)	G3						
D_AP(12)	J2						
D_AP(13)	C14						
D_AP(14)	A6						
D_AP(15)	A4						
D_BN(0)	N4	Input	LVDS	DDR	Differential	Data negative	805
D_BN(1)	Z11						
D_BN(2)	W4						
D_BN(3)	W10						
D_BN(4)	L1						
D_BN(5)	V8						
D_BN(6)	W6						
D_BN(7)	M1						
D_BN(8)	R4						
D_BN(9)	W1						
D_BN(10)	U4						
D_BN(11)	V2						
D_BN(12)	Z5						
D_BN(13)	N3						
D_BN(14)	Z2						
D_BN(15)	L4						

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
D_BP(0)	M4	Input	LVDS	DDR	Differential	Data positive	805
D_BP(1)	Z12						
D_BP(2)	Z4						
D_BP(3)	Z10						
D_BP(4)	L2						
D_BP(5)	V9						
D_BP(6)	W7						
D_BP(7)	N1						
D_BP(8)	P4						
D_BP(9)	V1						
D_BP(10)	T4						
D_BP(11)	V3						
D_BP(12)	Z6						
D_BP(13)	N2						
D_BP(14)	Z3						
D_BP(15)	L3						
D_CN(0)	H27	Input	LVDS	DDR	Differential	Data negative	805
D_CN(1)	A20						
D_CN(2)	H28						
D_CN(3)	K28						
D_CN(4)	K30						
D_CN(5)	C23						
D_CN(6)	G27						
D_CN(7)	J30						
D_CN(8)	B24						
D_CN(9)	A21						
D_CN(10)	A27						
D_CN(11)	C29						
D_CN(12)	A26						
D_CN(13)	C25						
D_CN(14)	A29						
D_CN(15)	C30						

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
D_CP(0)	J27	Input	LVDS	DDR	Differential	Data positive	805
D_CP(1)	A19						
D_CP(2)	H29						
D_CP(3)	K27						
D_CP(4)	K29						
D_CP(5)	C22						
D_CP(6)	F27						
D_CP(7)	H30						
D_CP(8)	B25						
D_CP(9)	B21						
D_CP(10)	B27						
D_CP(11)	C28						
D_CP(12)	A25						
D_CP(13)	C24						
D_CP(14)	A28						
D_CP(15)	B30						
D_DN(0)	V25	Input	LVDS	DDR	Differential	Data negative	805
D_DN(1)	V28						
D_DN(2)	T30						
D_DN(3)	V27						
D_DN(4)	U30						
D_DN(5)	W23						
D_DN(6)	R27						
D_DN(7)	T28						
D_DN(8)	V20						
D_DN(9)	R28						
D_DN(10)	L27						
D_DN(11)	N28						
D_DN(12)	M28						
D_DN(13)	V18						
D_DN(14)	Z26						
D_DN(15)	Z28						

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
D_DP(0)	V24	Input	LVDS	DDR	Differential	Data positive	805
D_DP(1)	V29						
D_DP(2)	T29						
D_DP(3)	W27						
D_DP(4)	V30						
D_DP(5)	W24						
D_DP(6)	T27						
D_DP(7)	U28						
D_DP(8)	V19						
D_DP(9)	R29						
D_DP(10)	M27						
D_DP(11)	P28						
D_DP(12)	M29						
D_DP(13)	V17						
D_DP(14)	Z25						
D_DP(15)	Z27						
SCTRL_AN	G1	Input	LVDS	DDR	Differential	Serial control negative[3]	805
SCTRL_AP	F1	Input	LVDS	DDR	Differential	Serial control positive[3]	805
SCTRL_BN	V5	Input	LVDS	DDR	Differential	Serial control negative[3]	805
SCTRL_BP	V4	Input	LVDS	DDR	Differential	Serial control positive[3]	805
SCTRL_CN	C26	Input	LVDS	DDR	Differential	Serial control negative[3]	805
SCTRL_CP	C27	Input	LVDS	DDR	Differential	Serial control positive[3]	805
SCTRL_DN	P30	Input	LVDS	DDR	Differential	Serial control negative[3]	805
SCTRL_DP	R30	Input	LVDS	DDR	Differential	Serial control positive[3]	805
DCLK_AN	H2	Input	LVDS		Differential	Clock negative[3]	805
DCLK_AP	H1	Input	LVDS		Differential	Clock positive[3]	805
DCLK_BN	V6	Input	LVDS		Differential	Clock negative[3]	805
DCLK_BP	V7	Input	LVDS		Differential	Clock positive[3]	805
DCLK_CN	D27	Input	LVDS		Differential	Clock negative[3]	805
DCLK_CP	E27	Input	LVDS		Differential	Clock positive[3]	805
DCLK_DN	N29	Input	LVDS		Differential	Clock negative[3]	805
DCLK_DP	N30	Input	LVDS		Differential	Clock positive[3]	805
SCPCLK	A10	Input	LVCMOS		Pull down	Serial communications port clock. Active only when SCPENZ is logic low[3]	
SCPDI	A12	Input	LVCMOS	SDR	Pull down	Serial communications port data input. Synchronous to SCPCLK rising edge[3]	
SCPENZ	C10	Input	LVCMOS		Pull down	Serial communications port enable active low[3]	
SCPDO	A11	Output	LVCMOS	SDR		Serial communications port output	

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
RESET_ADDR(0)	Z13	Input	LVCMOS		Pull down	Reset driver address select[3]	
RESET_ADDR(1)	W13						
RESET_ADDR(2)	V10						
RESET_ADDR(3)	W14						
RESET_MODE(0)	W9	Input	LVCMOS		Pull down	Reset driver mode select[3]	
RESET_SEL(0)	V14					Reset driver level select[3]	
RESET_SEL(1)	Z8					Reset driver level select.[3]	
RESET_STROBE	Z9	Input	LVCMOS		Pull down	Rising edge latches in RESET_ADDR, RESET_MODE, & RESET_SEL.[3]	
PWRDNZ	A8	Input	LVCMOS		Pull down	Active low device reset.[3]	
RESET_OEZ	W15	Input	LVCMOS		Pull up	Active low output enable for internal reset driver circuits.[3]	
RESET_IRQZ	V16	Output	LVCMOS			Active low output interrupt to DLP controller	
EN_OFFSET	C9	Output	LVCMOS			Active high enable for external V_{OFFSET} regulator	
PG_OFFSET	A9	Input	LVCMOS		Pull up	Active low fault from external V_{OFFSET} regulator[3]	
TEMP_N	B18	Input	Analog			Temperature sensor diode cathode	
TEMP_P	B17	Input	Analog			Temperature sensor diode anode	
RESERVED **MUST VERIFY WITH SRC DATA SHEET	D12, D13, D14, D15, D16, D17, D18, D19, U12, U13, U14, U15	NC	Analog		Pull Down	Do not connect on DLP system board. No connect. No electrical connections from CMOS bond pad to package pin.	
No Connect	U16, U17, U18, U19	NC				No connect. No electrical connection from CMOS bond pad to package pin	
RESERVED_BA	W11	Output	LVCMOS			Do not connect on DLP system board.	
RESERVED_BB	B11						
RESERVED_BC	Z20						
RESERVED_BD	C18						
RESERVED_PFE	A18	Input	LVCMOS		Pull down	Do not connect on DLP system board.	
RESERVED_TM	C8						

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
RESERVED_TP0	Z19	Input	Analog			Do not connect on DLP system board.	
RESERVED_TP1	W20						
RESERVED_TP2	W19						
V_{BIAS} [4]	C15, C16, V11, V12	Power	Analog			Supply voltage for positive bias level of micromirror reset signal	
V_{RESET} [4]	G4, H4, J1, K1	Power	Analog			Supply voltage for negative reset level of micromirror reset signal	
V_{OFFSET} [4]	A30, B2, M30, Z1, Z30	Power	Analog			Supply voltage for HVCMOS logic. Supply voltage for positive offset level of micromirror reset signal. Supply voltage for stepped high voltage at micromirror address electrodes	
V_{CC} [4]	A24, A7, B10, B13, B16, B19, B22, B28, B5, C17, C20, D4, J29, K2, L29, M2, N27, U27, V13, V15, V22, W17, W21, W26, W29, W3, Z18, Z23, Z29, Z7	Power	Analog			Supply voltage for LVCMOS core. Supply voltage for positive offset level of micromirror reset signal during power down. Supply voltage for normal high level at micromirror address electrodes	

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	SIGNAL	DATA RATE[6]	INTERNAL TERMINATION[7]	DESCRIPTION[1]	TRACE LENGTH (mil[8])
NAME	NO.						
V_{SS} [5]	A13, A22, A23, B12, B14, B15, B20, B23, B26, B29, B3, B6, B9, C19, C21, C5, D2, G2, J28, K3, L28, L30, M3, P27, P29, U29, V21, V23, V26, W12, W16, W18, W2, W22, W25, W28, W30, W5, W8, Z21, Z22, Z24	Ground				Device ground. Common return for all power.	

(1) The DLP500YX DMD is a component of a DLP chipset. Reliable function and operation of the DLP500YX DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.
(2) I = Input, O = Output, P = Power, G = Ground, NC = No connect
(3) These signals are very sensitive to noise or intermittent power connections, which can cause irreversible DMD micromirror array damage or, to a lesser extent, image disruption. Consider this precaution during DMD board design and manufacturer handling of the DMD sub-assemblies.
(4) The following power supplies are required to operate the DMD: V_{CC}, V_{OFFSET}, V_{BIAS}, and V_{RESET}.
(5) V_{SS} must be connected for proper DMD operation.
(6) DDR = Double Data Rate, SDR = Single Data Rate. Refer to the Timing Requirements for specifications and relationships.
(7) Internal term = CMOS level internal termination. Refer to Recommended Operating Conditions for differential termination specification.
(8) Dielectric Constant for the DMD FXK (S410) ceramic package is approximately 9.6. For the package trace lengths shown: Propagation Speed = 11.8 sqrt (9.60 = 3.808 in/ns. Propagation Delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2) (3)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(2)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(2)	–15	–0.3	V
$\lvert V_{BIAS} – V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(4)		11	V
$\lvert V_{BIAS} – V_{RESET} \rvert$	Supply voltage difference (absolute value)(5)		34	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins(2)	–0.5	V_{CC} + 0.5	V
	Input voltage for all other LVDS input pins (2) (6)	–0.5	V_{CC} + 0.5	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(7)		500	mV
I_{ID}	Input differential current(6)		6.3	mA
CLOCKS				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A, DCLK_B, DCLK_C, DCLK_D		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Array temperature: operational(8)	0	90	°C
	Array temperature: non–operational(8)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (non-condensing)		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(5) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(6) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(8) The highest temperature of the active array (as calculated using *セクション 7.6*) or of any location along the window edge as defined in 図 7-2. The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 7-2 are intended to measure the highest window edge temperature. If a particular application causes another location on the window edge to be at a higher temperature, use that location.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-2. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-2 are intended to result in the worst case delta. If a particular application causes another location on the window edge to result in a larger delta temperature, use that location.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Limit the exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	–14.5	–14	–13.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(3)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value)(4)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage(5)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(5)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(5)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(5)	–0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse duration(6)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(7)			500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO(8)	0		900	ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			µs
$t_{SCP\_POS\_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling edge)(8)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling edge)(8)	900			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse duration (high level)	2			µs
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(9)			400	MHz

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
$\|V_{ID}\|$	Input differential voltage (absolute value)(10)	150	300	440	mV
V_{CM}	Common mode voltage(10)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(10)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long–term operational(11) (12) (13) (14)	10		40 to 70(13)	°C
	Array temperature, short–term operational(12) (15)	0		10	°C
T_{WINDOW}	Window temperature – operational(16)			85	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(16) (17)			14	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(18)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{θ}	Illumination marginal ray angle(20)			55	deg
For Illumination Source Between 420 nm and 700 nm					
ILL_{VIS}	Illumination power density on array(21)			31	W/cm^2
ILL_{VISTP}	Illumination total power on array			22	W
For Illumination Source <420 nm and >700 nm					
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{UV}	Illumination wavelengths < 420 nm(11)			10	mW/cm^2

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit. See セクション 9 , 図 9-1, and 表 9-1.
(4) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit. See セクション 9 , 図 9-1, and 表 9-1.
(5) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, “Low-Power Double Data Rate (LPDDR)” JESD209B. Tester conditions for V_{IH} and V_{IL}.
- Frequency = 60 MHz. Maximum rise time = 2.5 ns at 20/80
- Frequency = 60 MHz. Maximum fall time = 2.5 ns at 80/20

(6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(7) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(8) See 図 6-2.
(9) See LVDS timing requirements in セクション 6.8 and 図 6-6.
(10) See LVDS waveform requirements in 図 6-5.
(11) Simultaneous exposure of the DMD to the maximum セクション 6.4 for temperature and UV illumination reduces device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-2 and the package thermal resistance セクション 7.6 .
(13) Per 図 6-1, the maximum operational array temperature must be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See セクション 7.7 for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the usable life of the device.
(15) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as the cumulative time over the usable life of the device and is less than 500 hours.
(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-2. The window test points TP2, TP3, TP4, and TP5 shown in 図 7-2 are intended to result in the worst case delta temperature. If a particular application causes another location on the window edge to result in a larger delta in temperature, use that location.

(17) DMD is qualified at the maximum temperature specified. Operation of the DMD outside of these limits has not been tested.
(18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(19) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.
(20) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including the pond of micromirrors (POM), cannot exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) contributes to thermal limitations described in this document, and may negatively affect lifetime.
(21) The maximum optical power that can be incident on the DMD is limited by the maximum optical power density and the micromirror array temperature.

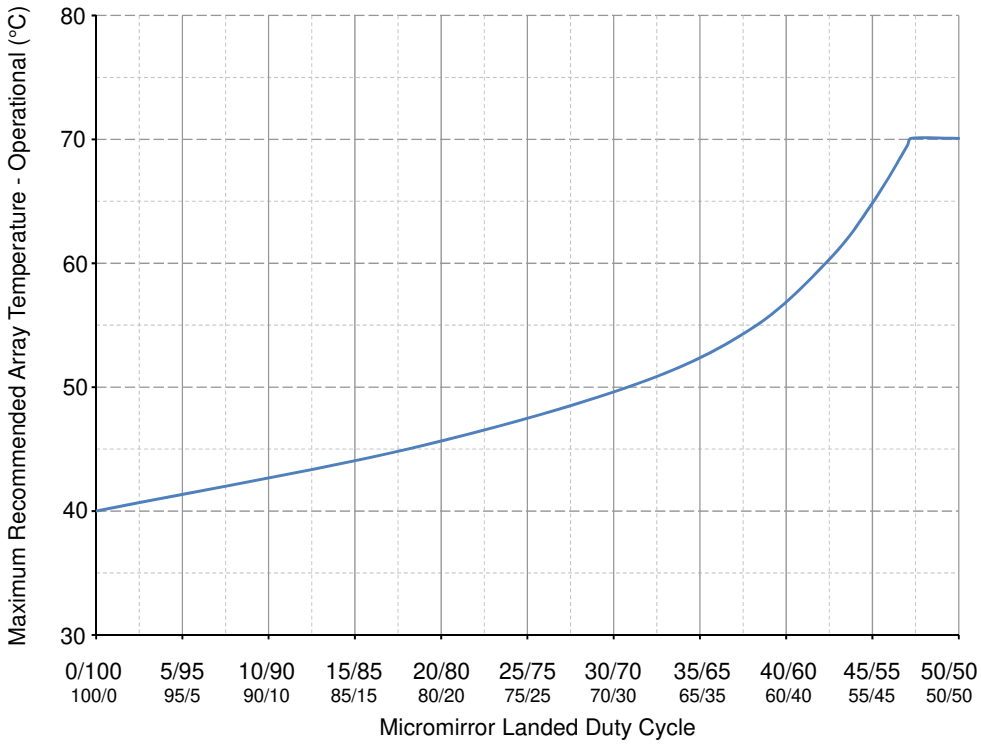


図 6-1. Maximum Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP500YX FXK Package 257 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.90	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the セクション 6.4 .
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems must be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGES						
V_{OH}	High level output voltage	V_{CC} = 1.8 V, I_{OH} = –2 mA	0.8 x V_{CC}			V
V_{OL}	Low level output voltage	V_{CC} = 1.95 V, I_{OL} = 2 mA			0.2 x V_{CC}	V
CURRENTS						
I_{OZ}	High impedance output current	V_{CC} = 1.95 V	–40		25	µA
I_{IL}	Low level input current	V_{CC} = 1.95 V, V_I = 0	–1			µA
I_{IH}	High level input current (1)	V_{CC} = 1.95 V, V_I = V_{CC}			110	µA
I_{CC}	Supply current V_{CC}	V_{CC} = 1.95 V			1500	mA
I_{OFFSET}	Supply current V_{OFFSET} (2)	V_{OFFSET} = 10.5 V			13	mA
I_{BIAS}	Supply current V_{BIAS} (2) (3)	V_{BIAS} = 18.5 V			4	mA
I_{RESET}	Supply current V_{RESET} (3)	V_{RESET} = –14.5 V			–9	mA
SUPPLY POWER						
P_{CC}	Supply power dissipation V_{CC}	V_{CC} = 1.95 V			2925	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (2)	V_{OFFSET} = 10.5 V			139	mW
P_{BIAS}	Supply power dissipation V_{BIAS} (2) (3)	V_{BIAS} = 18.5 V			67	mW
P_{RESET}	Supply power dissipation V_{RESET} (3)	V_{RESET} = –14.5 V			131	mW
P_{TOTAL}	Supply power dissipation V_{TOTAL}				3261	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and MBRST (15:0) pins.
(2) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limits listed in the *セクション 6.4* table.
(3) To prevent excess current, the supply voltage difference $|V_{BIAS} – V_{RESET}|$ must be less than specified limit in *セクション 6.4*.

6.7 Capacitance at Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{I_lvds}	LVDS input capacitance 2xLVDS	f = 1 MHz			20	pF
$C_{I\_nonlvds}$	Non-LVDS input capacitance	f = 1 MHz			20	pF
C_{I_tdiode}	Temperature diode input capacitance	f = 1 MHz			30	pF
C_O	Output capacitance	f = 1 MHz			20	pF

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP INTERFACE(1)						
t_r	Rise time	20% to 80% reference points	1		3	V/ns
t_f	Fall time	80% to 20% reference points	1		3	V/ns
LVDS INTERFACE(2)						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock cycle	DCLK_A, LVDS pair	2.5			ns
		DCLK_B, LVDS pair	2.5			ns
		DCLK_C, LVDS pair	2.5			ns
		DCLK_D, LVDS pair	2.5			ns
t_W	Pulse duration	DCLK_A, LVDS pair	1.19	1.25		ns
		DCLK_B, LVDS pair	1.19	1.25		ns
		DCLK_C, LVDS pair	1.19	1.25		ns
		DCLK_D, LVDS pair	1.19	1.25		ns
t_{Su}	Setup time	D_A(15:0) before DCLK_A, LVDS pair	0.275			ns
		D_B(15:0) before DCLK_B, LVDS pair	0.275			ns
		D_C(15:0) before DCLK_C, LVDS pair	0.275			ns
		D_D(15:0) before DCLK_D, LVDS pair	0.275			ns
		SCTRL_A before DCLK_A, LVDS pair	0.275			ns
		SCTRL_B before DCLK_B, LVDS pair	0.275			ns
		SCTRL_C before DCLK_C, LVDS pair	0.275			ns
		SCTRL_D before DCLK_D, LVDS pair	0.275			ns
t_h	Hold time	D_A(15:0) after DCLK_A, LVDS pair	0.195			ns
		D_B(15:0) after DCLK_B, LVDS pair	0.195			ns
		D_C(15:0) after DCLK_C, LVDS pair	0.195			ns
		D_D(15:0) after DCLK_D, LVDS pair	0.195			ns
		SCTRL_A after DCLK_A, LVDS pair	0.195			ns
		SCTRL_B after DCLK_B, LVDS pair	0.195			ns
		SCTRL_C after DCLK_C, LVDS pair	0.195			ns
		SCTRL_D after DCLK_D, LVDS pair	0.195			ns
t_{SKEW}	Skew time	Channel B relative to channel A (3) (4)	–1.25		1.25	ns
t_{SKEW}	Skew time	Channel D relative to channel C(5) (6), LVDS pair	–1.25		1.25	ns

(1) See 図 6-3 for rise time and fall time for SCP.
(2) See 図 6-5 for timing requirements for LVDS.
(3) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(4) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).
(5) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0) and D_CP(15:0).
(6) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0) and D_DP(15:0).

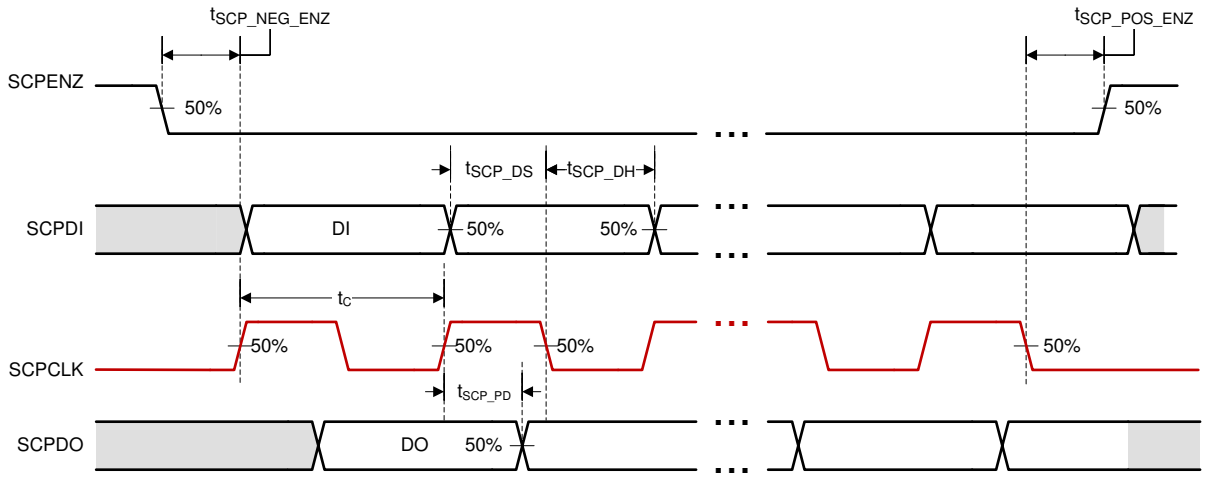


図 6-2. SCP Timing Requirements

A. See セクション 6.4 for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH} and t_{SCP_PD} specifications.
B. SCPCLK falling–edge capture for SCPDI.
C. SCPCLK rising–edge launch for SCPDO.
D. See 式 1

$$f_{SCPCLK} = \frac{1}{t_C} \quad (1)$$

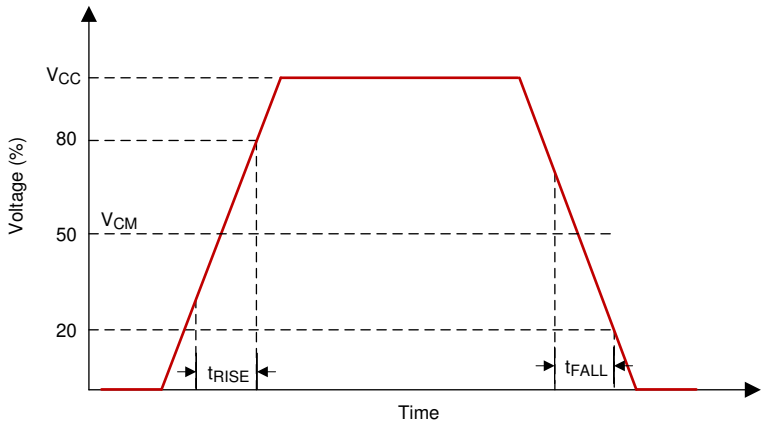


図 6-3. SCP Requirements for Rise and Fall

See セクション 6.8 for t_r and t_f specifications and conditions.

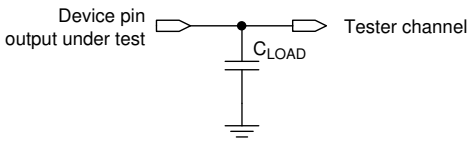
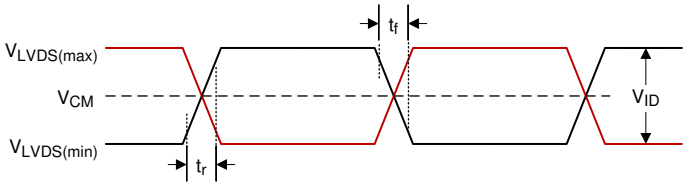


図 6-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers must use IBIS or other simulation tools to correlate the timing reference load to a system environment.



A. See 式 2 and 式 3

図 6-5. LVDS Waveform Requirements

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \tag{2}$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \tag{3}$$

See セクション 6.4 for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

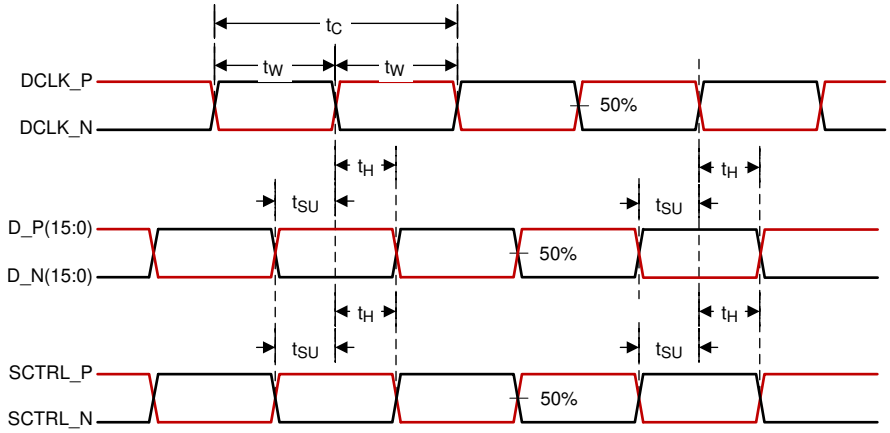


図 6-6. Timing Requirements

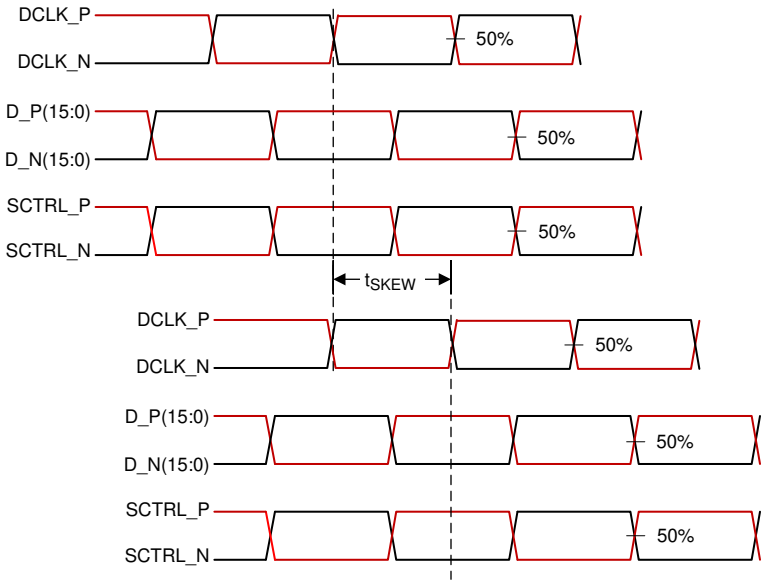


図 6-7. LVDS Interface Channel Skew Definition

See セクション 6.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(15:0) and D_N(15:0).

6.9 Typical Characteristics

When the DMD is controlled by the DLPC900, the digital controller has four modes of operation:

A. Video mode

B. Video pattern mode

C. Pre-stored pattern mode

D. Pattern on-the-fly mode

In video mode (A), the 24-bit frames displayed on the DMD are the same as the input 24-bit video frame rates. In video pattern mode (B), the V_{SYNC} rates displayed on the DMD are linked to the incoming video source V_{SYNC} rates but the overall pattern rates depend upon the configured bit depth. In modes B, C, and D, the pattern rates depend on the bit depth as shown in 表 6-1.

表 6-1. DLP500YX Pattern Rate versus Bit Depth using DLPC900

BIT DEPTH	VIDEO PATTERN MODE (Hz)	PRE-STORED or PATTERN ON-THE-FLY MODE (Hz)
1	2880	16129
2	1440	5434
3	960	3717
4	720	2183
5	480	1466
6	480	1239
7	360	923
8	247	441
10		96
12		24
14		6
16		1

6.10 System Mounting Interface Loads

表 6-2. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
When loads are applied to the electrical and thermal interface areas				
Maximum load to be applied to the electrical interface area(1)			111	N
Maximum load to be applied to the thermal interface area(1)			111	N
When loads are applied to only the electrical interface area				
Maximum load to be applied to the electrical interface area(1)			222	N
Maximum load to be applied to the thermal interface area(1)			0	N

(1) Apply the load uniformly in the corresponding areas shown in 図 6-8.

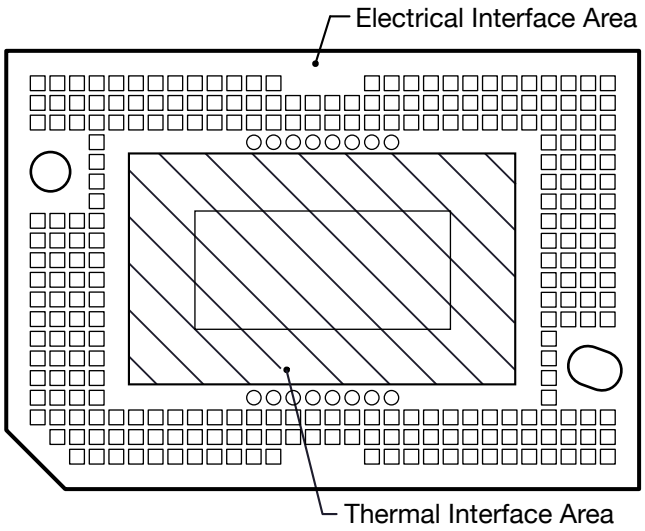


図 6-8. System Mounting Interface Loads

6.11 Micromirror Array Physical Characteristics

表 6-3. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns(1)	M	2048	micromirrors
Number of active rows(1)	N	1200	micromirrors
Micromirror (pixel) pitch(1)	P	5.4	µm
Micromirror active array width(1)	Micromirror Pitch × number of active columns	11.0592	mm
Micromirror active array height(1)	Micromirror Pitch × number of active rows	6.4800	mm
Micromirror active border (All four sides) (2)	Pond of micromirrors (POM)	20	micromirrors/side

(1) See 図 6-9
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

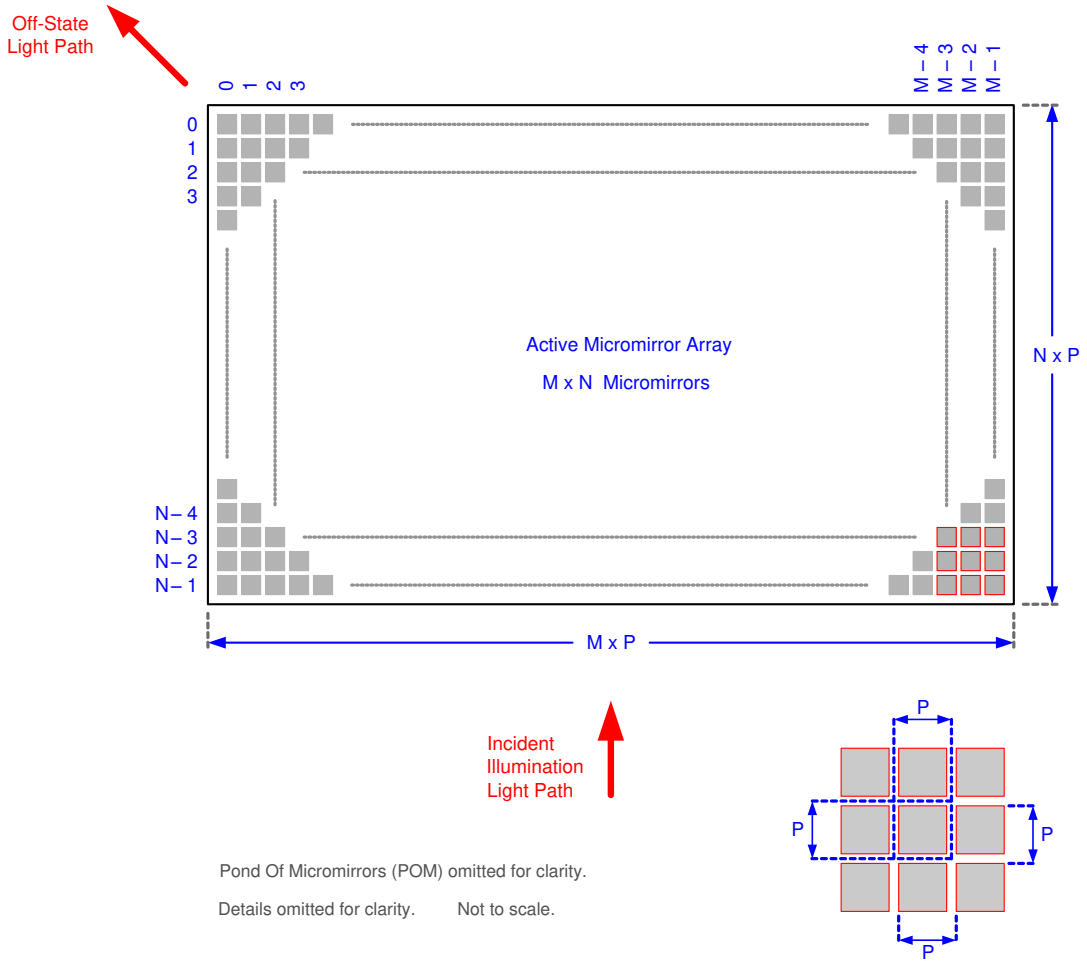


図 6-9. Micromirror Array Physical Characteristics

Refer to セクション 6.11 table for M, N, and P specifications.

6.12 Micromirror Array Optical Characteristics

表 6-4. Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
Mirror tilt angle (1) (2) (3) (4)	Landed State	15.6	17.5	18.4	degrees
Micromirror crossover time(5)	Typical Performance		1	3	µs
Micromirror switching time(6)	Typical Performance	6			
Number of out-of-specification micromirrors(7)	Adjacent micromirrors			0	micromirrors
	Non-Adjacent micromirrors			10	
DMD Photopic Efficiency(8)	420 - 700 nm		65%		

(1) Measured relative to the plane formed by the overall micromirror array
(2) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(3) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(4) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction. See 図 6-10.
(5) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(6) The minimum time between successive transitions of a micromirror.
(7) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified MICROMIRROR SWITCHING Time.
(8) Efficiency numbers assume 35-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination.

- Window Transmission 94% (double Pass, Through Two Window Surfaces)
- Micromirror Reflectivity 88%
- Array Diffraction Efficiency 84% (@f/2.4)
- Array Fill Factor 93%

Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.

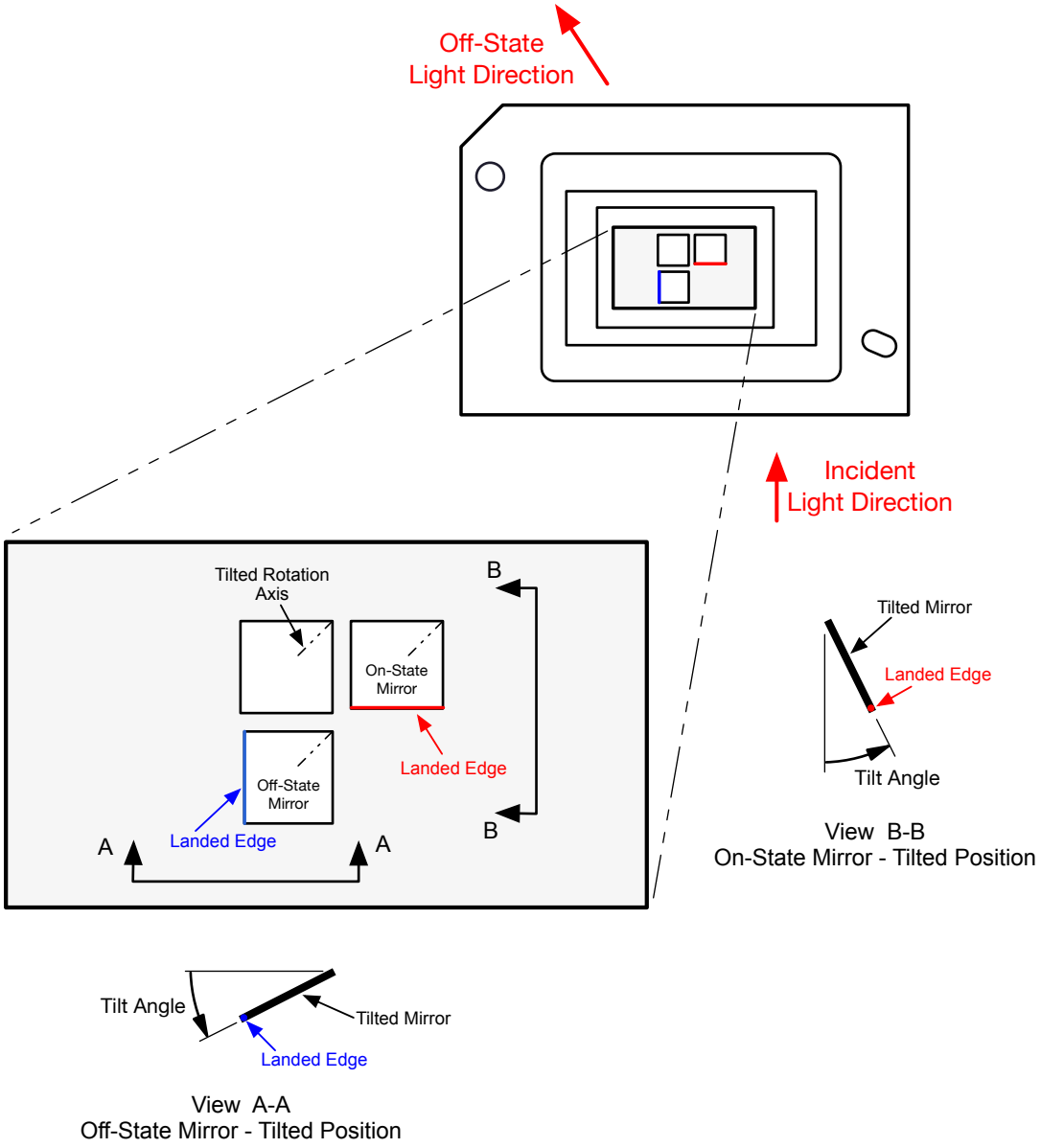


図 6-10. Micromirror Landed Orientation and Tilt

6.13 Window Characteristics

表 6-5. DMD Window Characteristics

PARAMETER(1)	CONDITIONS	MIN	NOM	MAX	UNIT
Window material	Corning Eagle XG				
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture	See Note (2)				
Illumination overfill	Refer to *セクション 7.5.3*				
Window transmittance, single–pass through both surfaces and glass (3)	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *セクション 7.5* for more information.
(2) For details on the size and location of the window aperture, see the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section of this data sheet.
(3) See the TI application report DLPA031, *Wavelength Transmittance Considerations for DLP® DMD Window*.

6.14 Chipset Component Usage Specification

Reliable function and operation of the DLP500YX DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

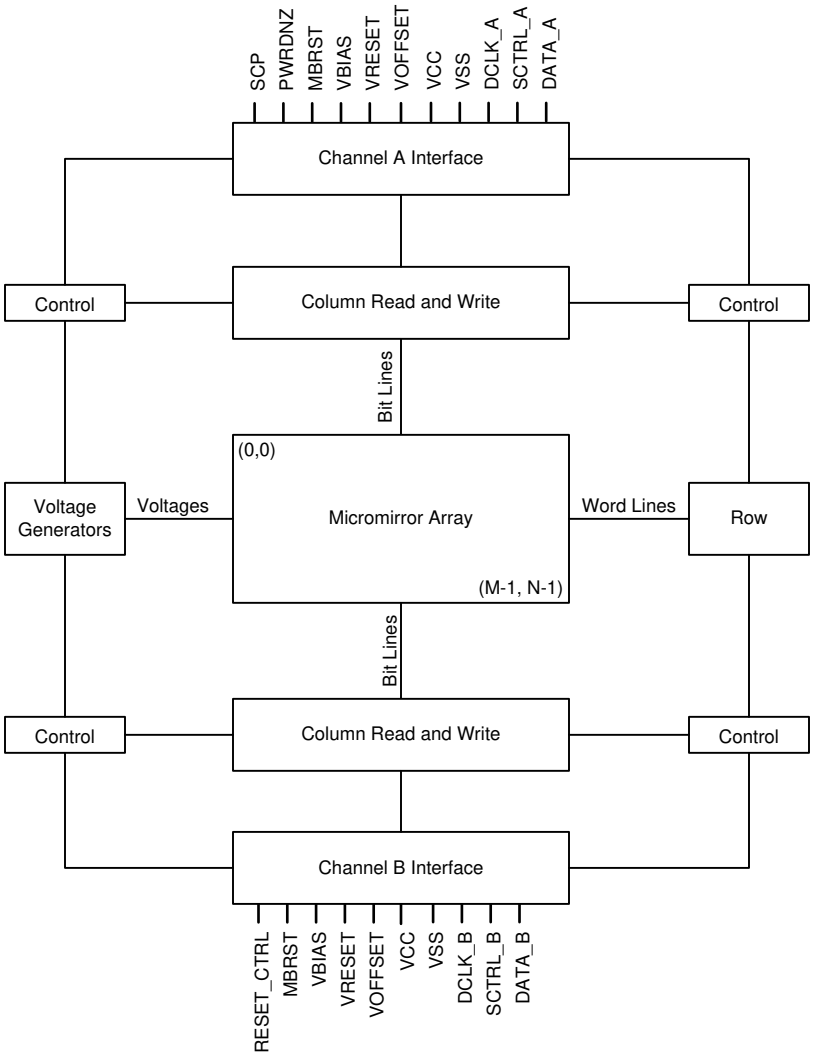
7 Detailed Description

7.1 Overview

The DLP500YX DMD is a 0.50-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to セクション 7.2 . The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DMD is one part of a chipset comprising of the DLP500YX DMD and the DLPC900 Controller. To ensure reliable operation, the DLPC900 Controller must always be used to control the DLP500YX DMD.

7.2 Functional Block Diagram



Channels C and D not shown. For pin details on channels A, B, C, and D, refer to the *Pin Configurations and Functions* table and the LVDS interface section of セクション 6.8.

図 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Interface

The DMD requires 5 DC voltages: DMD_P3P3V, DMD_P1P8V, VOFFSET, VRESET, and VBIAS. DMD_P3P3V is a filtered version of the 3.3VDS supply received over the flex cables from the DLPC910 Controller Board. DMD_P3P3V is used on the DMD Board to create the other DMD voltages (DMD_P1P8V, VOFFSET, VRESET, and VBIAS) required for proper DMD operation. TI provides a DMD board reference design on TI.com to enable customers to see how these voltages are created as well and how the DMD board design is accomplished.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers need to use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC900 controller. See the DLPC900 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, the projected image quality and the optical performance are contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area needs to be the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation, and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating

conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

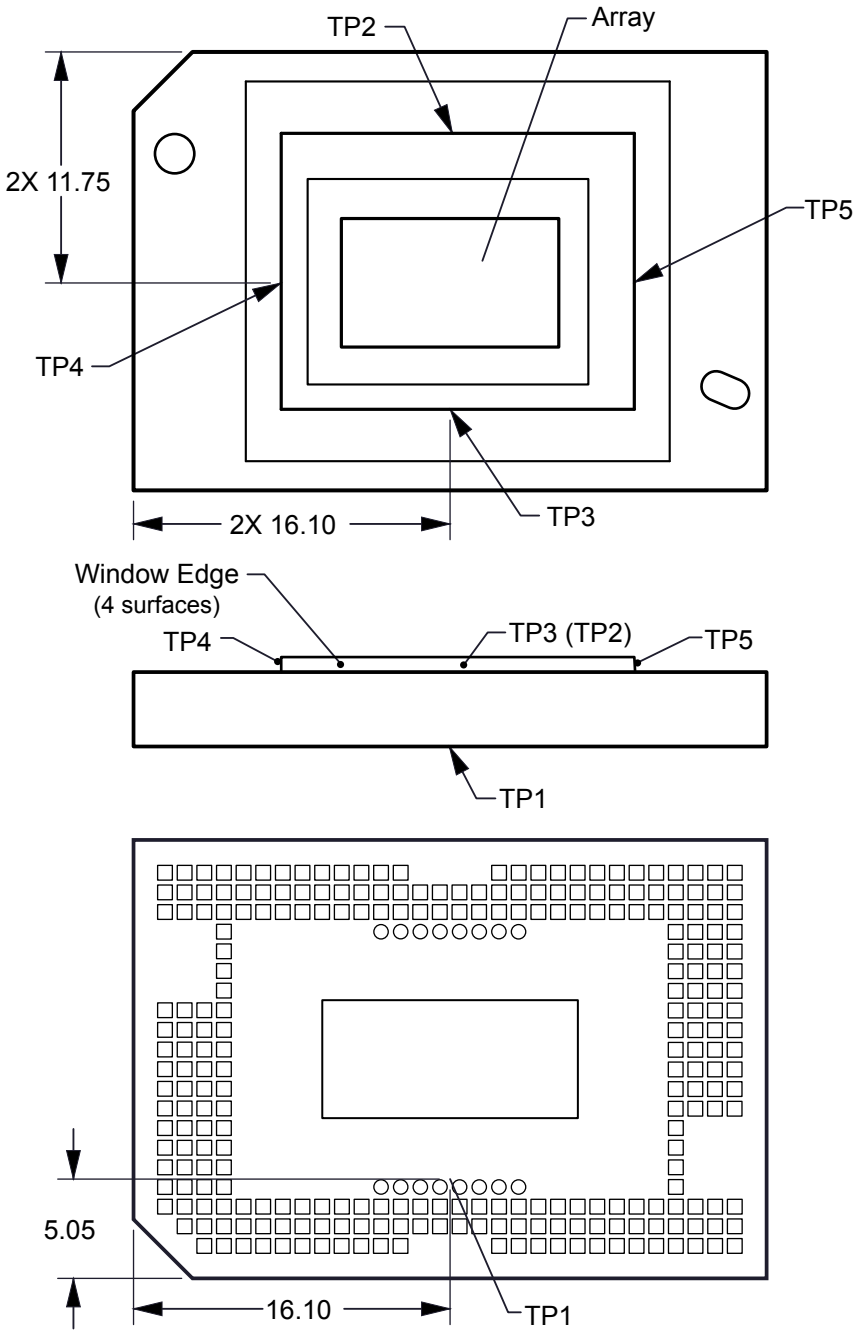


図 7-2. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (measured at TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in Thermal Information from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{ILLUMINATION}$ = Illumination power absorbed (W)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.26 W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The factors used in determining the illumination power absorbed is shown in each of the examples below. Examples are included where the optical power has been determined by measuring the illumination power density, total illumination power, and screen lumens. The examples assume illumination distribution is 83.7% on the active array and 16.3% on the area outside the array.

7.6.1 Micromirror Array Temperature Calculation using Illumination Power Density

The equations below are valid for each DMD in a single chip or multi-chip DMD system.

- $Q_{ILLUMINATION}$ = ($Q_{INCIDENT}$ × DMD average thermal absorptivity) (W)
- $Q_{INCIDENT}$ = $ILL_{DENSITY}$ × ILL_{AREA} (W)
- $ILL_{DENSITY}$ = measured illumination optical power density at DMD (W/cm^2)
- ILL_{AREA} = illumination area on DMD (cm^2)
- DMD average thermal absorptivity = 0.40

$Q_{ELECTRICAL}$ = 3.26 W

Array size = 11.0592 mm × 6.4800 mm = 0.72 cm^2

$ILL_{DENSITY}$ = 31 W/cm^2 (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

ILL_{AREA} = 0.72 cm^2 / (83.7%) = 0.86 cm^2

$Q_{INCIDENT}$ = 31 W/cm^2 × 0.86 cm^2 =26.66 W

Q_{ARRAY} = 3.26 W + (0.40 × 26.66 W) = 13.92 W

T_{ARRAY} = 50.0 °C + (13.92 W × 0.90 °C/W) = 62.53 °C

7.6.2 Micromirror Array Temperature Calculation using Total Illumination Power

The equations below are valid for each DMD in a single chip or multi-chip DMD system.

- $Q_{ILLUMINATION}$ = ($Q_{INCIDENT}$ × DMD average thermal absorptivity) (W)
- $Q_{INCIDENT}$ = measured total illumination optical power at DMD (W)

- DMD average thermal absorptivity = 0.40

$Q_{ELECTRICAL}$ = 3.26 W

$Q_{INCIDENT}$ =26.66 W (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

Q_{ARRAY} = 3.26 W + (0.40 × 26.66 W) = 13.92 W

T_{ARRAY} = 50.0 °C + (13.92 W × 0.90 °C/W) = 62.53 °C

7.6.3 Micromirror Array Temperature Calculation using Screen Lumens

The equations below are valid for a single chip DMD system with spectral efficiency of 300 lumens/Watt.

- $Q_{ILLUMINATION}$ = SL × C_{L2W} (W)
- SL = measured ANSI screen lumens (lm)
- C_{L2W} = Conversion constant for screen lumens to power absorbed on DMD (Watts/Lumen)

$Q_{ELECTRICAL}$ = 3.26 W

C_{L2W} = 0.00266 W/lm

SL = 4000 lm (measured)

$T_{CERAMIC}$ = 50.0 °C (measured)

Q_{ARRAY} = 3.26 W + (0.00266 W/lm × 4000 lm) = 13.9 W

T_{ARRAY} = 50.0 °C + (13.9 W × 0.90 °C/W) = 62.51 °C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time), whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD usable life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature at a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

If the use case involves inputting Grayscale input images, between the two extremes (ignoring for the moment color), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use the following equation to calculate the landed duty cycle of a given pixel during a specified time period

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_% represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_% represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, and blue color intensities would be as shown in 表 7-2 and 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
50%	20%	30%

表 7-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data being used.

The DLP500YX DMD is controlled by two DLPC900 controllers. The DMD itself receives bit planes through a 2xLVDS input data bus and, when input control commands dictate, activates the controls which update the mechanical state of the DMD mirrors. In combination with the DLPC900 Controllers, the chipset enables four unique modes of system level operation:

- Video Mode - 24 bit video signals presented to inputs of the DLPC900 Controllers appear on the DMD. The DMD mirrors are updated in a PWM fashion to construct the 24 bit video data. This mode is similar to standard DLP Display projector use cases.
- Video Pattern Mode - the user can define periods of time for specific patterns to be displayed on the DMD. Those patterns are provided via the input video interface and are constrained to input video timing parameters. This mode is optimal for when the data to be presented is not known in advance of operation, or input data needs to be streamed or updated based on real-time processing conditions.
- Pre-stored Pattern Mode - the user can define the patterns in advance and build the pattern data into an on-board flash memory. Upon power up, the DLPC900 controllers immediately start reading and displaying those patterns. This mode is typically used in applications where the patterns to be used are known in advance and the patterns can all fit in the external flash memory. This mode typically provides the fastest pattern update rates.
- Pattern-on-the-Fly Pattern Mode - the user can download and update pattern data over the DLPC900 input USB data interface. This allows an external processor to modify and update patterns based on external processing decisions. This mode also provides streaming capability similar to the Video Pattern Mode except that the user would need to take into account delays involved with USB transmission of pattern data and control information.

The DLP500YX provides solutions for many varied applications including structured light (3-D machine vision), 3-D printing, information projection, and lithography.

The DLP500YX contains the most recent breakthrough micromirror technology called the TRP pixel. With a smaller pixel pitch of 5.4 µm and increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor while maintaining high optical efficiency. DLP chipsets are a great fit for any system that requires high resolution and high output projection imaging.

8.2 Typical Application

3D machine vision is a typical embedded system application for the DLP500YX DMD. In this application, two DLPC900 devices control the pattern data being imaged from a DLP500YX DMD onto the object being measured while an external camera system monitors the projected patterns as they appear on the object. An external microprocessor can then geometrically determine all 3D points of the object using the knowledge of the projected pattern provided to the object, the actual distorted pattern as captured by the camera, and the angle between the projector line-of-sight and the camera line-of-sight. This type of application diagram is shown in 図 8-1. In this configuration, the DLPC900 controller supports a 24-bit parallel RGB video input from an external source computer or processor. The video input FPGA splits each 2048 x 1200 image frame into a left half and a right half with the left half feeding the Primary DLPC900 and the right half feeding the Secondary DLPC900. Each half consists of 1024 columns by 1200 rows plus any horizontal and vertical blanking at half the pixel clock rate. This system configuration supports still and motion video as well as sequential pattern modes. For more

information, refer to the DLPC900 digital controller data sheet, found on the DLPC900 Product Folder listed under セクション 11.3.1.

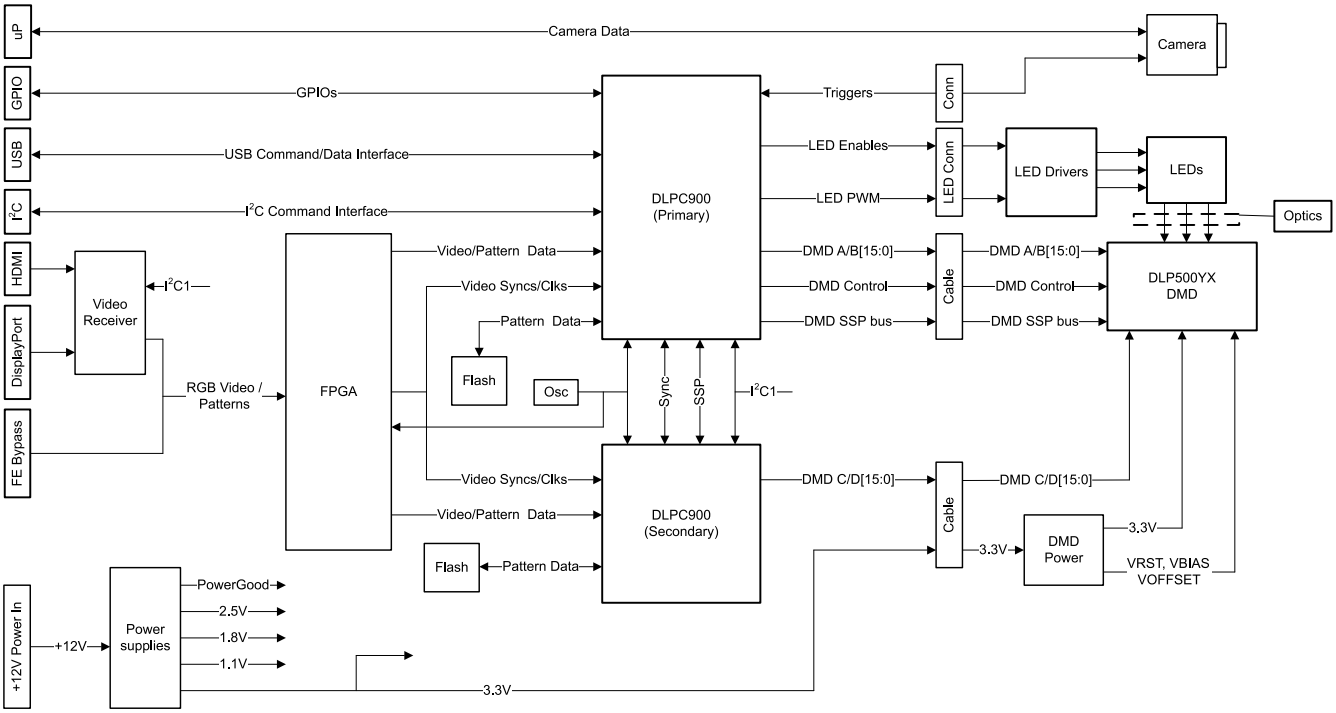


図 8-1. Typical DLP500YX Application Diagram

8.2.1 Design Requirements

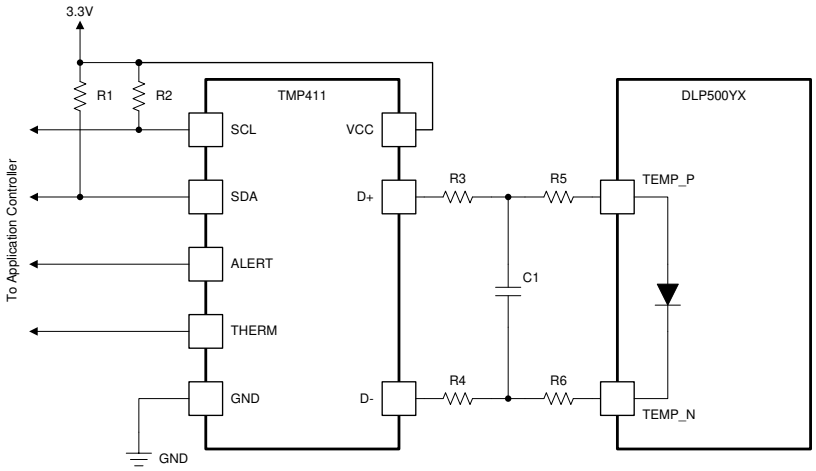
At the high level, typical DLP500YX DMD systems include an illumination source (Lamp, LED, or Laser), an optical light engine containing both illumination and projection optics, mechanics, electronic components, power supplies, cooling systems, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the optical relationship from the illumination source to the DMD, and from the DMD to the location of the projected image. The designer must then understand the electronic components of a DLP500YX DMD system, part of which includes one or more PCBs which contain the DMD and Controllers. In the TI DLP500YX based evaluation module design, the DLPC900 Controller board provides power, bit plane data, and control information to the DMD mounted on the DLP500YX DMD board. The DLPC900 Controller board also interfaces to the user system, accepting image data based on user provided timing (software or hardware triggered) and providing that data in bit plane format to the DMD to be projected on the imaging target.

8.2.2 Detailed Design Procedure

A TI evaluation module design exists which shows how to connect the DLPC900 controller to the DMD. In creating a new board specific to a customer application, layout guidelines need to be followed to achieve a functional and reliable projection system. To complete the system, an optical module or light engine is required that contains the DLP500YX DMD, associated illumination sources, optical elements, and necessary mechanical components. Care must be taken to understand and implement wise design decisions regarding the engineering aspects of illumination and projection optics, digital and analog electronics, software, and mechanical and thermal design principles.

8.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The DMD thermal diode pins B17 and B18 can be connected to the TMP411 temperature sensor as shown in 図 8-2, and an external processor can interface with the TMP411 temperature sensor over I^2C bus to allow monitoring of the DMD temperature. This temperature data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth, all with the idea of maintaining appropriate temperature control of the DMD.



A. Details omitted for clarity, see the DLPLCR500YXEVM evaluation module design for connections.
B. See the TMP411 datasheet for system board layout recommendation.
C. See the TMP411 datasheet and the DLPLCR500YXEVM evaluation module design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. Zero ohm resistors need to be located close to the DMD package pins.

図 8-2. TMP411 Sample Schematic

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{CC}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP® controller.

> **注意**
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 図 9-1.
>
> V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, V_{CC} must always start and settle before V_{OFFSET} plus Delay1 specified in 表 9-1, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 6.4.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-up, LVCMOS input pins must not be driven high until after V_{CC} have settled at operating voltages listed in セクション 6.4.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, V_{CC} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within the specified limit of ground. See 表 9-1.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in セクション 6.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in セクション 6.1, in セクション 6.4, and in 図 9-1.
- During power-down, LVCMOS input pins must be less than specified in セクション 6.4.

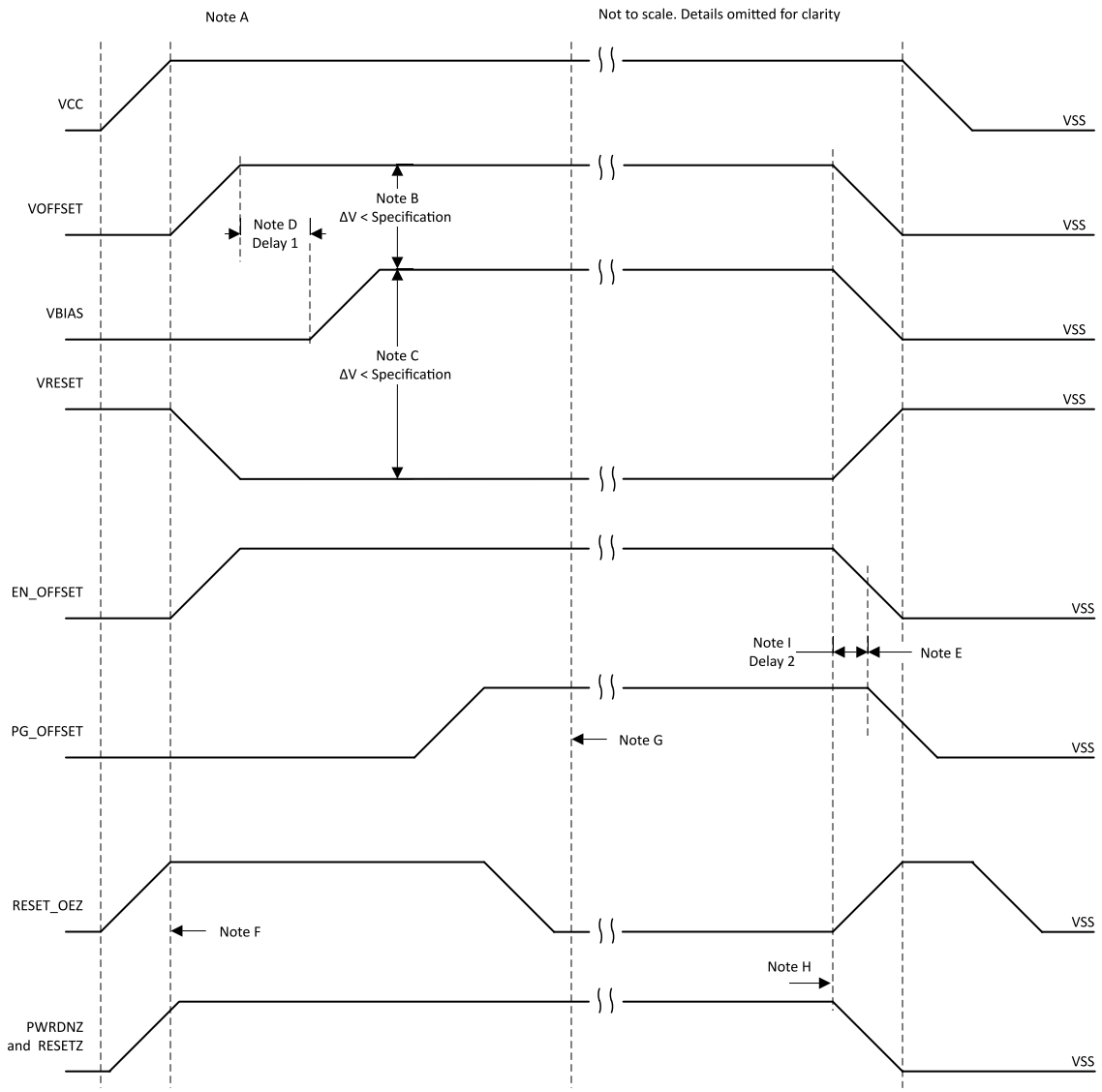


図 9-1. DMD Power Supply Requirements

A. See セクション 6.4, and the Pin Functions 表 5-1.
B. To prevent excess current, the supply voltage difference |VOFFSET – VBIAS| must be less than the specified limit in the セクション 6.4
C. To prevent excess current, the supply difference |VBIAS – VRESET| must be less than the specified limit in the セクション 6.4.
D. VBIAS must power up after VOFFSET has powered up, per the Delay1 specification in 表 9-1.
E. PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in 表 9-1.
F. DLP® controller software enables the DMD power supplies VBIAS, VRESET, VOFFSET with VCC active after RESET_OEZ is at logic high.
G. DLP® controller software initiates the global VBIAS command.
H. After the DMD micromirror park sequence is complete, the DLP® controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET, and VOFFSET.
I. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP® controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal goes high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

表 9-1. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from VOFFSET settled at recommended operating voltage to VBIAS power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

9.3 Restrictions on Hot Plugging and Hot Swapping

The DLP500YX uses a state of the art pixel node which enables smaller optics, higher resolution, and overall great performance and reliability as long as certain design-for-assembly methods are used. To maximize DMD reliability, Hot Plugging and/or Hot Swapping DMDs **voids the DMD warranty conditions and must be avoided at all times**.

9.3.1 No Hot Plugging

Avoid hot plugging, the act of connecting the DMD to power supplies and/or data inputs which are already energized, to ensure maximum reliability of the DMD. Do not add or remove the DMD from a DMD socket unless all input power supplies of the DMD are at a potential equal to the local ground potential (VSS). This applies to a DMD incoming test station, a partially assembled product, a completed product under test, and a product in the field. This also applies to any cables, flex cables, or PCB connections which provide power to the DMD. Provide power as defined in the power-up scenario detailed in セクション 9.1. Perform power down as defined in セクション 9.2.

9.3.2 No Hot Swapping

Avoid hot swapping, the act of removing and replacing the DMD with DMD power supplies and/or data inputs which are already energized, to ensure maximum reliability of the DMD. Never add or remove the DMD from a DMD socket unless all input power supplies of the DMD are at a potential equal to the local ground potential (VSS). This applies to a DMD incoming test station, a partially assembled product, a completed product under test, and a product in the field. This also applies to any cables, flex cables, or PCB connections which provide power to the DMD. Provide power as defined in the power-up scenario detailed in セクション 9.1. Perform power down as defined in セクション 9.2

9.3.3 Intermittent or Voltage Power Spike Avoidance

When DMD power and/or data and clock inputs are energized, twisting of the DMD, DMD socket, or DMD board must be avoided when trying to align the DMD within an optical engine. This twisting motion can create power intermittences and/or voltage spikes exceeding input power and data specifications of the DMD which may ultimately affect the DMD reliability. PCB power/data/clock/control circuits must be de-energized before making or removing connections, including cables, connectors, probes and bed-of-nails connections.

PCB and System design considerations must take into account ways to prevent external influence of DMD input power clock, data and control signals. Robust connectors must be used which are resistant to intermittent connections or noise spikes if jostled or vibrated. Connectors must be used which are rated to exceed the number of insertion/removal cycles expected in the application. External electromagnetic emitters must not be placed nearby these sensitive circuits unless adequate EMI shielding is properly used. Sufficient bulk decoupling and component decoupling capacitance as well as appropriate PCB layout techniques must be available for all electrical components within the DMD based "system" such that ground bounce does not occur. See the section on セクション 10.1 for more layout information.

10 Layout

10.1 Layout Guidelines

10.1.1 Critical Signal Guidelines

The DLP500YX DMD is one device in a chipset controlled by the DLPC900 Controller. The following guidelines are targeted at designing a functioning PCB using this DLP500YX DMD chipset. The DLP500YX DMD board must be a high-speed multi-layer PCB containing high-speed digital logic utilizing dual edge (DDR) LVDS signals at 400 MHz clock rates. 図 10-1 shows the DLP500YX signals and the recommendations needed from/to the

DLPC900 Controller devices. The DLPC900 device provides the data and control to the DMD. The TPS65145 and LP38513 devices supply power to the DMD.

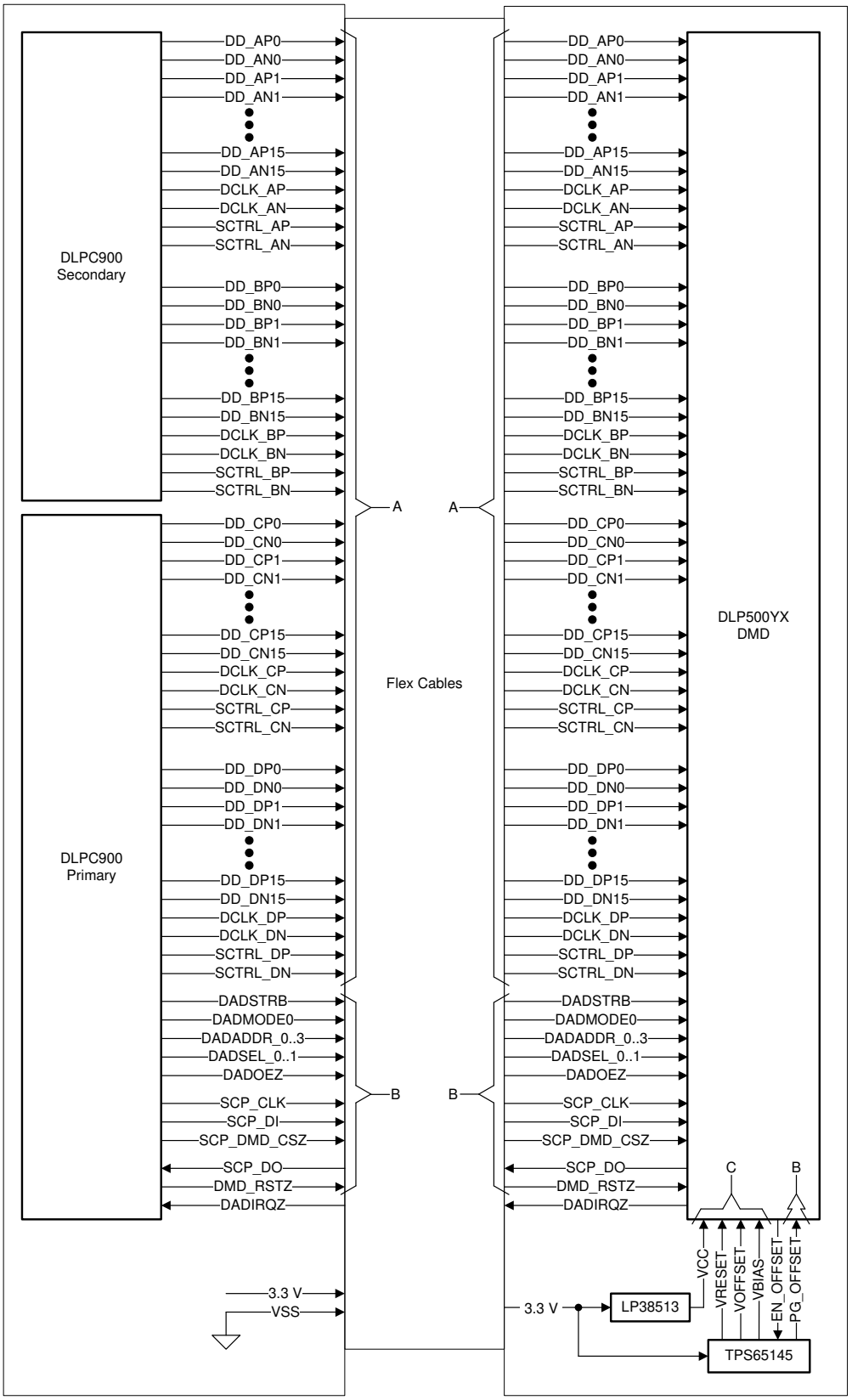


図 10-1. DLP500YX DMD System Connections and Layout Restrictions

表 10-1. Layout Restriction Notes for 図 10-1

Note	Signal Type	Guideline
A	Differential	Prevent signal noise
		Route 100 ±10-Ω resistor
		Intra-pair (P-to-N) length tolerance is ±12-mils
		DD and SCTRL must be matched to the DCLK within ±150-mils
		DCLK_C must be matched to DCLK_D within ±1.25-ns
		DCLK_A must be matched to DCLK_B within ±1.25-ns
		Do not switch routing layers except at the beginning and end of trace
		Signal routing length must not exceed 375-mm
B	Single-ended	Prevent signal noise
		Route single-ended signals 50 ±5-Ω
		No length match requirement
C	Power	VRESET, VOFFSET, VBIAS, and VCC at the DMD must be kept within the operating limits specified in the data sheet
		Provide proper amount of decoupling capacitance for each voltage at the DMD

10.1.2 Power Connection Guidelines

The following are recommendations for the power connections to the DMD or DMD PCB:

- Solid planes are **required** for DMD_P3P3V(3.3V), DMD_P1P8V and Ground.
- TI strongly recommends partial power planes are used for VOFFSET, VRESET, and VBIAS.
- VOFFSET, VBIAS, VRESET, VCC, and VCCI power rails must be kept within the specified operating range. *This includes effects from ripple and DC error.*
- To accommodate power supply transient current requirements, adequate decoupling capacitance must be placed as near the DMD VOFFSET, VBIAS, VRESET, VCC, and VCCI pins as possible.
- Do not swap DMDs while the DMD is still powered on (this is called hot swapping). All DMD power supply rails and signals must be 0 volts (not driven) before connecting or disconnecting the DMD physical interface.
- Do not allow power to be applied to the DMD when one or more signal pins are not being driven.
- Decoupling capacitor locations for the DMD must be as close as possible to the DMD. The pads of the capacitors must be connected to at least two or three vias to get a very low impedance to ground as shown in 図 10-3. Furthermore, the capacitor must be in the flow of the power trace as it goes to the input of the DMD.
- It is extremely important to adhere to the セクション 9.1 and セクション 9.2 and do not allow the DMD power-supply levels to be outside of the recommended operating conditions specified in the DMD data sheet.

These figures show examples of bypass decoupling capacitor layout.

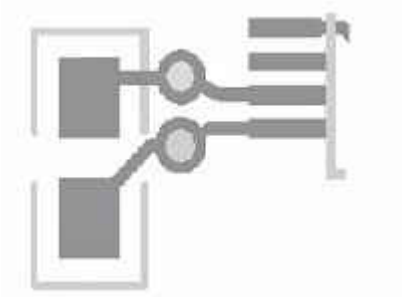


図 10-2. Poor Layout

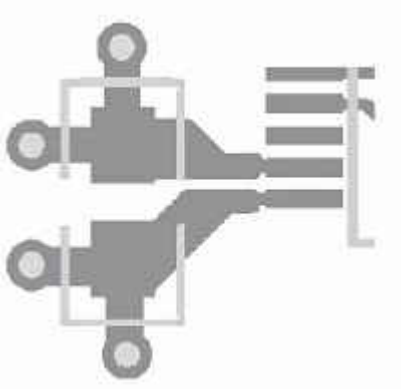


図 10-3. Good Layout

10.1.3 Noise Coupling Avoidance

During operation, it is critical to prevent the coupling of noise or intermittent power connections onto the following signals because *irreversible DMD micromirror array damage* or lesser effects of image disruption can occur:

- SCTRL_DN, STRL_DP
- DCLK_DN, DCLK_DP
- SCPCLK
- SCPDI
- SCP_DMD_CSZ
- DADADDR_0, DADADDR1_1, DADADDR_2, DADADDR_3
- DADMODE0
- DADSEL_0, DADSEL_1, DADSEL_2, DADSEL_3
- DADSTRB
- DMD_RSTZ
- DADOEZ
- PG_OFFSET

In this context, the following conditions are considered noise:

- Shorting to another signal
- Shorting to power
- Shorting to ground
- Intermittent connection (includes hot swapping)
- An electrical open condition
- An electrical floating condition
- Inducing electromagnetic interference that is strong enough to affect the integrity of the signals
- Unstable inputs (conditions outside of the specified operating range) to any of the device power rails
- Voltage fluctuations on the device ground pins

10.2 Layout Example

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in 表 10-2. Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top/bottom layers if necessary.

表 10-2. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes.
2	Ground	1	Solid ground plane (net GND).
3	Signal	0.5	50 Ω and 100 Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5	50 Ω and 100 Ω differential signals
7	Ground	1	Solid ground plane (net GND).
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

10.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50 Ω ±10% for all signals. The exceptions are listed in 図 10-1 and repeated for convenience in 表 10-3.

表 10-3. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 ±10% differential across each pair
	DCLK_AP, DCLK_AN	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 ±10% differential across each pair
	DCLK_BP, DCLK_BN	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	D_CP(0:15), D_CN(0:15)	100 ±10% differential across each pair
	DCLK_CP, DCLK_CN	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	D_DP(0:15), D_DN(0:15)	100 ±10% differential across each pair
	DCLK_DP, DCLK_DN	
	SCTRL_DP, SCTRL_DN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005”/0.005” design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1” minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

10.2.3.1 Voltage Signals

Below are additional voltage supply layout examples from the power planes to the individual DMD pins. In general, power supply trace widths must be as wide as possible to reduce impedances.

表 10-4. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from the power generation to the DMD input
VRESET	15	Create mini plane from the power generation to the DMD input
VBIAS	15	Create mini plane from the power generation to the DMD input
All DMD control input/ output connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Device Support

11.2.1 Device Nomenclature

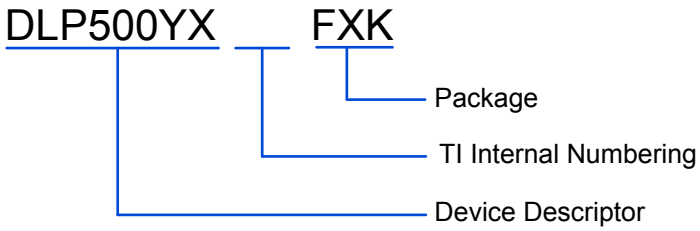

図 11-1. Part Number Description

11.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of the serial number, and part 2 of the serial number. The first character of the DMD serial number (part 1) is the manufacturing year. The second character of the DMD serial number (part 1) is the manufacturing month.

Example: DLP500YXFXK GHXXXXX LLLLLLM

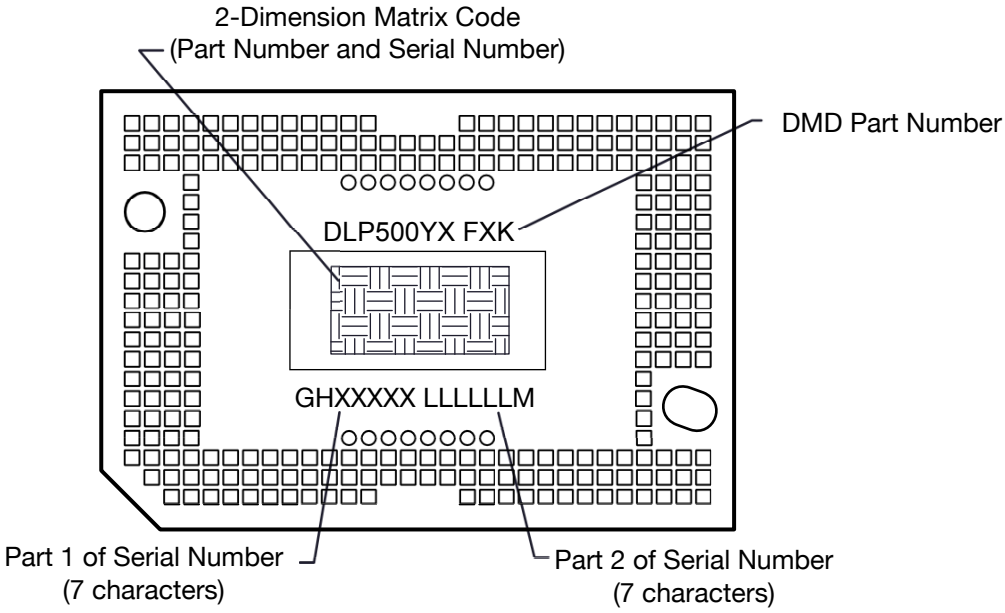

図 11-2. DMD Marking Locations

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP500YX.

- *DLP500YX Product Folder*
- *DLPC900 Product Folder*
- *DLPC900 Programmers Guide*

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 サポート・リソース

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP500YXFXK	Last Time Buy	Production	CLGA (FXK) | 257	33 | JEDEC TRAY (5+1)	Yes	NIPDAU	N/A for Pkg Type	0 to 70	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

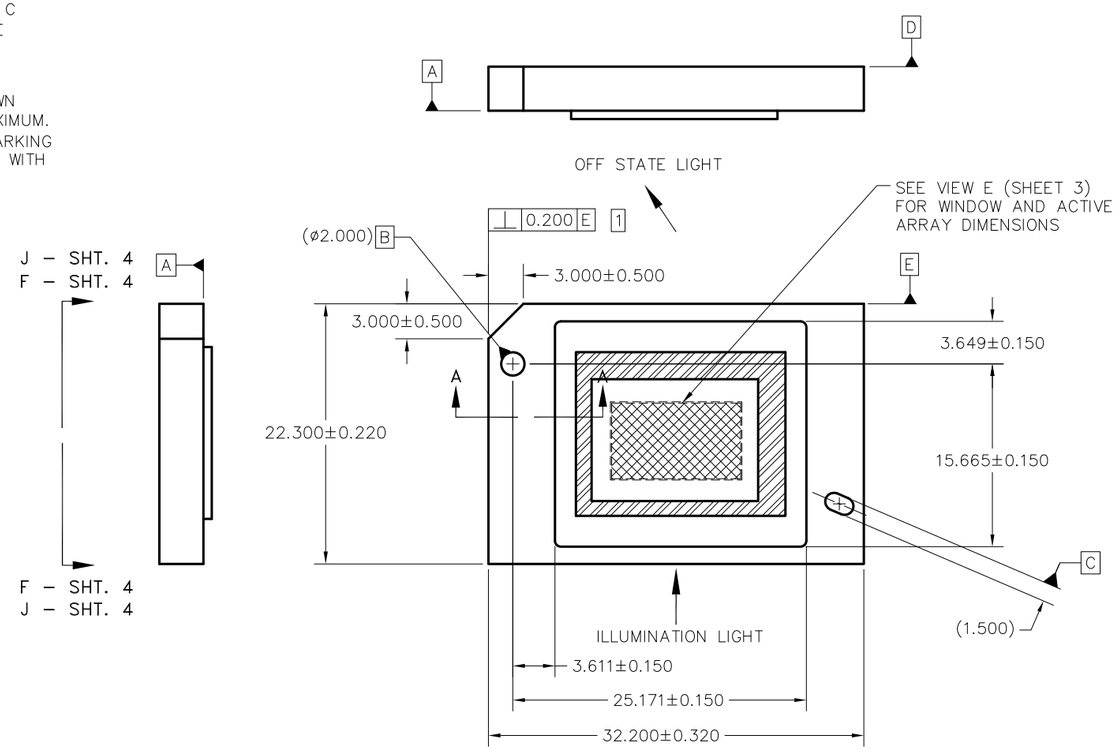
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

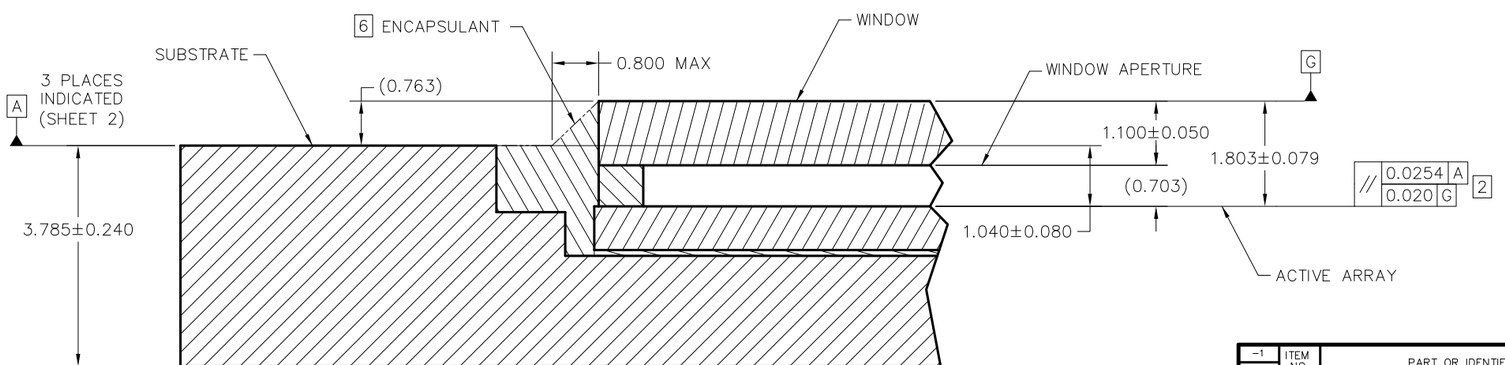
DWG NO 2516659 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2181188, INITIAL RELEASE	05/07/2019	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA TO THE LEFT OF THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA TO THE RIGHT OF THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

−1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG	DATE 05/07/19
ENGR	F. ARMSTRONG	05/07/19
QA	F. KONRAD	05/14/19
CQE	M. DORAK	05/14/19

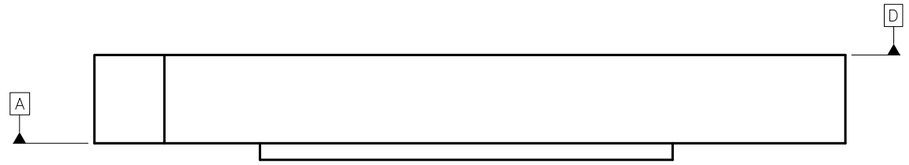
TEXAS INSTRUMENTS
Dallas, Texas

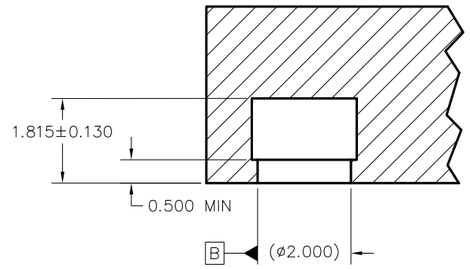
ICD, MECHANICAL, DMD
.50" MTRP 2xLVDS HB
SERIES 410 (FXK PACKAGE)

THIRD ANGLE PROJECTION		
NONE	0314DA	
NEXT ASSY	USED ON	
APPLICATION		

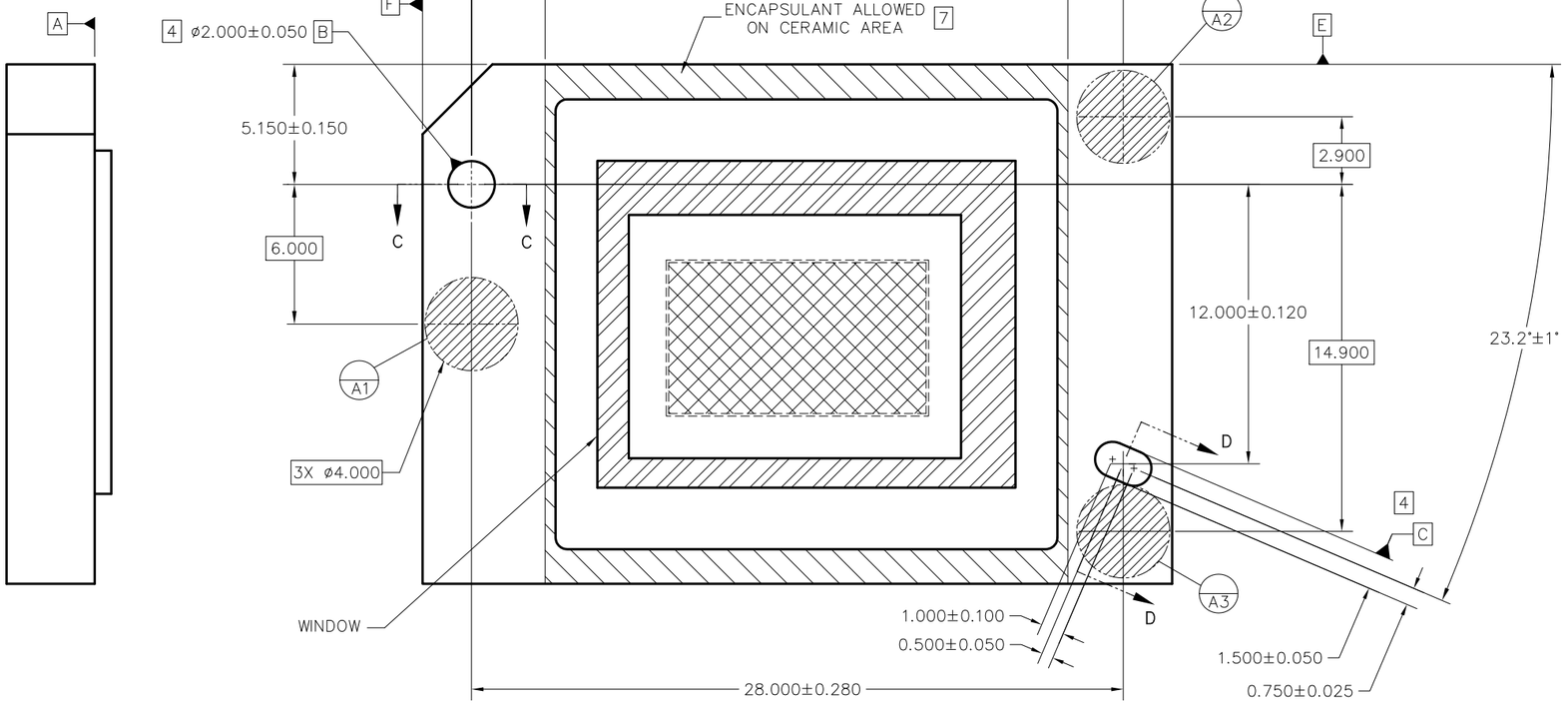
SIZE B | DRAWING NO 2516659 | REV A
SCALE 4/1 | SHEET 1 OF 4

ACED1g

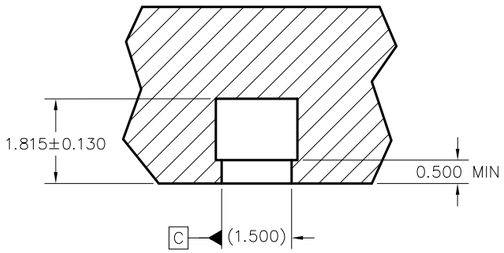




SECTION C–C
DATUM B
SCALE 16/1



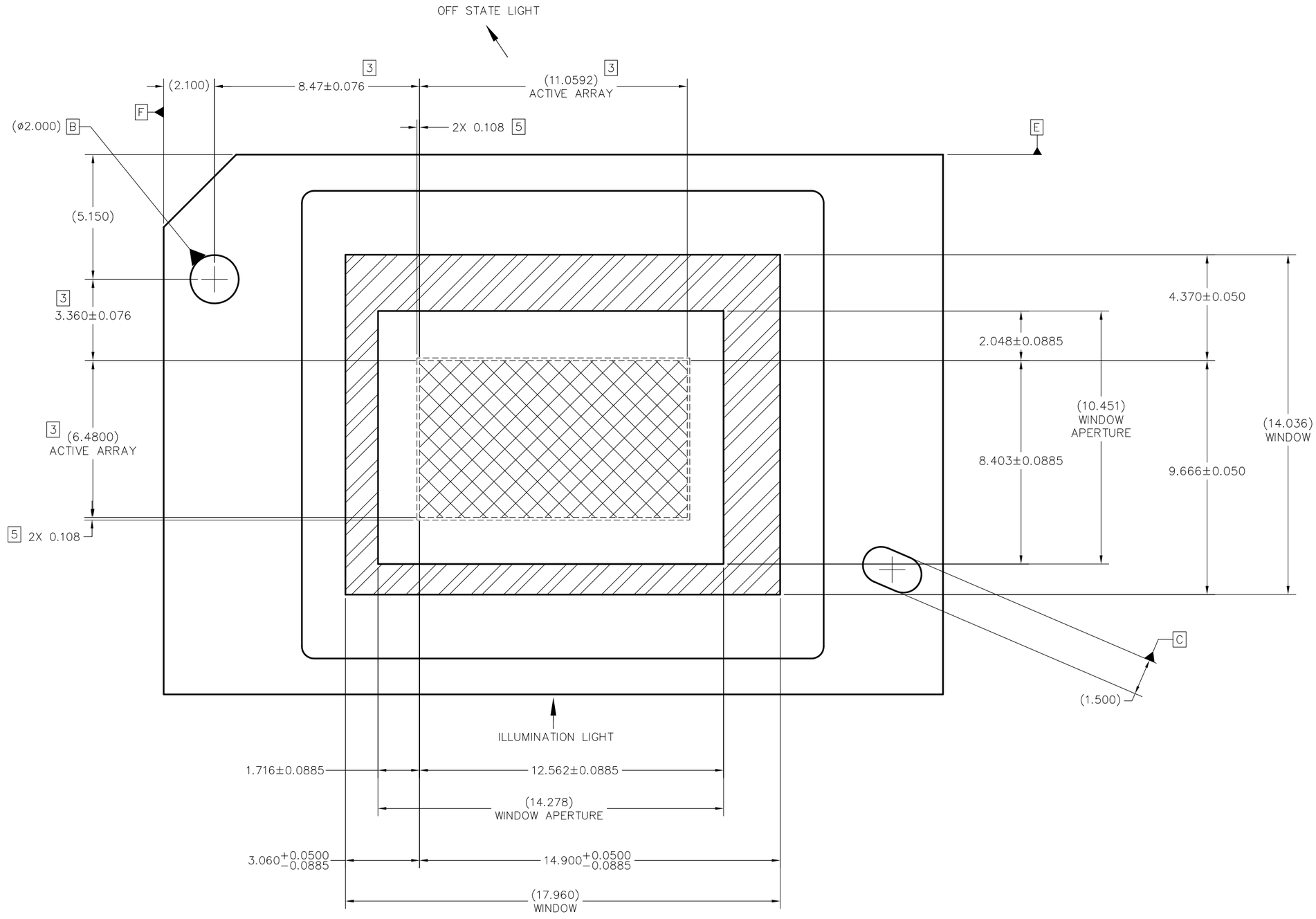
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2516659	REV A
		SCALE 4/1	SHEET 2	

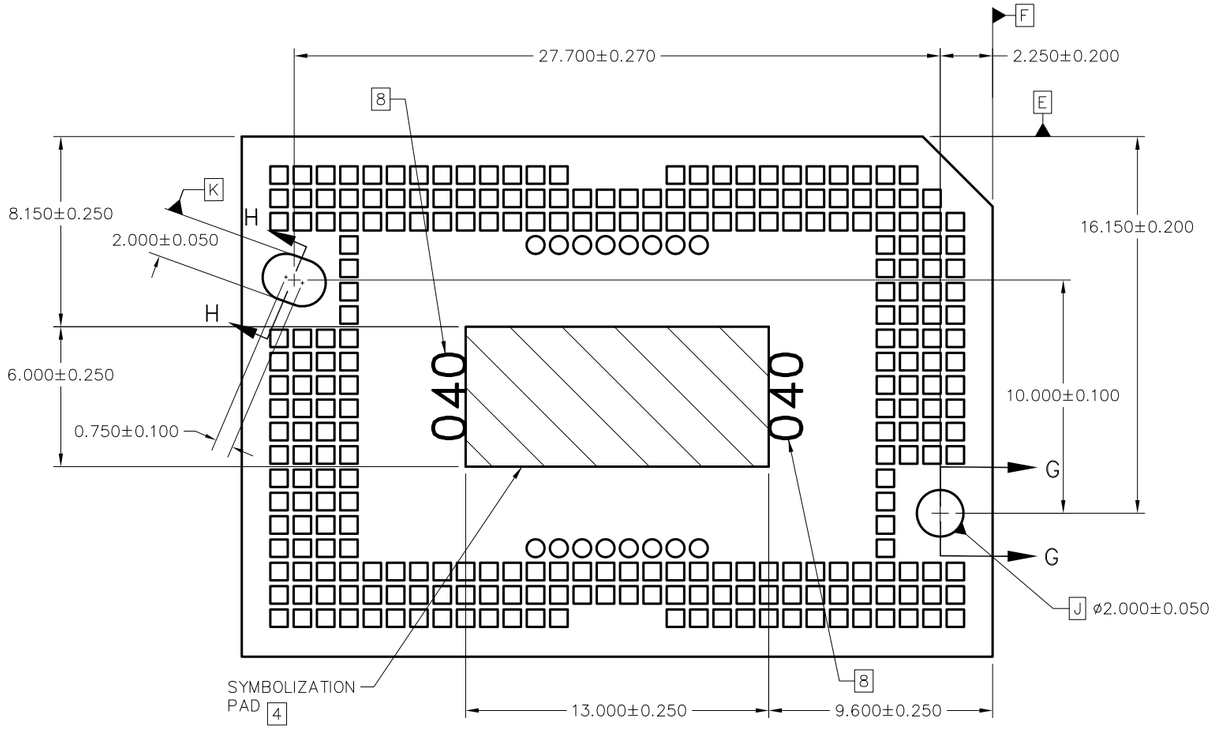
ACED2c



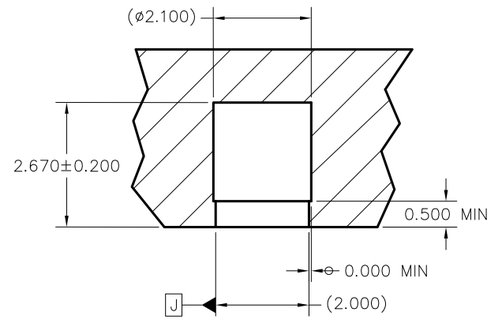
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2516659	REV A
		SCALE 4/1	SHEET 3	

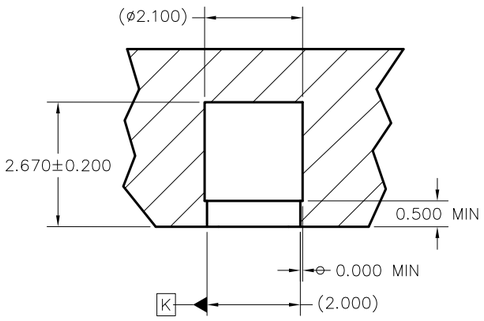
ACED2c



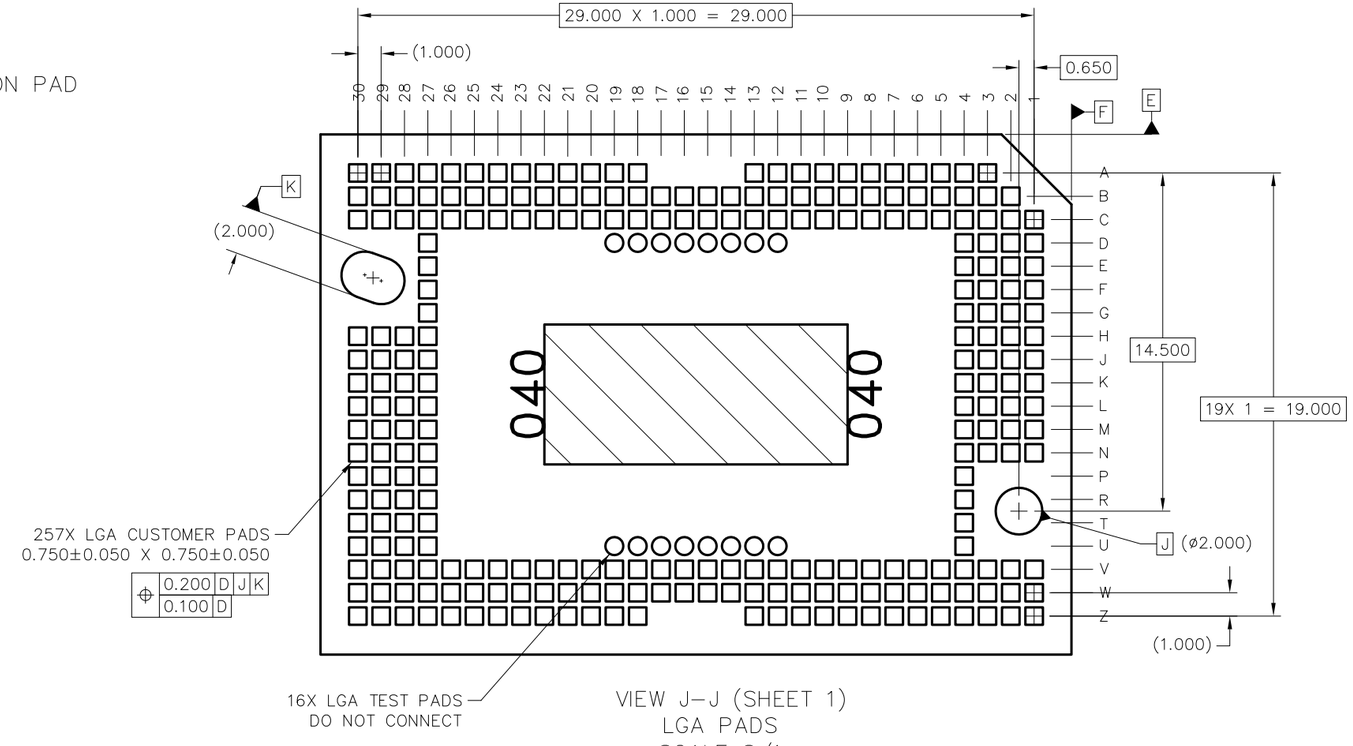
VIEW F–F (SHEET 1)
DATUMS J AND K, SYMBOLIZATION PAD
SCALE 8/1



SECTION G–G
DATUM J
SCALE 16/1



SECTION H–H
DATUM K
SCALE 16/1



VIEW J–J (SHEET 1)
LGA PADS
SCALE 8/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE B	DRAWING NO 2516659	REV A
	ISSUE DATE	SCALE 4/1	SHEET 4	

ACED2c

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最終更新日：2025 年 10 月