TEXAS INSTRUMENTS
DLP5530S-Q1
JAJSJA0B – JULY 2020 – REVISED APRIL 2021

DLP5530S-Q1 車載用車内ディスプレイ用の 0.55 インチ、1.3 メガピクセル DMD

1 特長

- 車載アプリケーションに対応
  - DMD アレイの動作温度範囲:-40℃～105℃
- 機能安全品質管理
  - ASIL-B までの ISO 26262 機能安全システム設計に役立つ資料を入手可能
- DLP5530S-Q1 車載用チップセットには以下のものが含まれます。
  - DLP5530S-Q1 DMD
  - DLPC230S-Q1
  - TPS99000S-Q1 システム管理および照明コントローラ
- 対角 0.55 インチのマイクロミラー・アレイ
  - 7.6µm のマイクロミラー・ピッチ
  - マイクロミラー傾斜角:±12° (フラット状態に対して)
  - 底面照明による最良の効率と光学エンジン・サイズ
  - 1152 × 576 の入力解像度をサポート
  - 外部 GPU ベースのダイヤモンド型前処理により、最大 2304 x 1152 の解像度
  - LED またはレーザー照明に対応可能
- 600MHz の Sub-LVDS DMD インターフェイスによる低い消費電力と放射妨害
- 上限や下限の温度でも 10kHz の DMD リフレッシュ・レートを維持
- DMD メモリ・セルのセルフ・テストを内蔵

2 アプリケーション

- 広視野の拡張現実ヘッドアップ・ディスプレイ (HUD)
- デジタル・クラスタ、ナビゲーション、インフォテインメントのフロント・ガラス・ディスプレイ

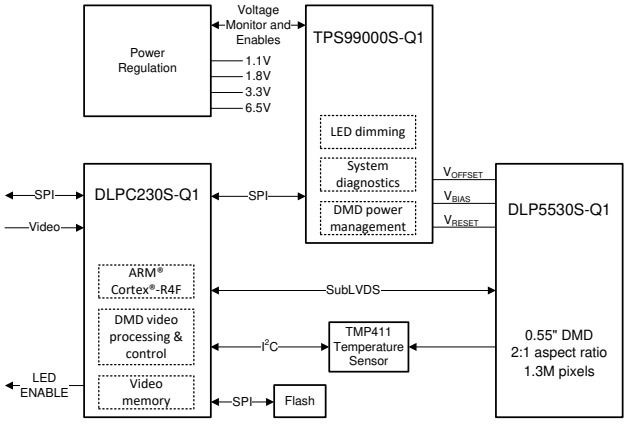
3 概要

DLP5530S-Q1 車載用 DMD を DLPC230S-Q1 DMD コントローラ、TPS99000S-Q1 システム管理および照明コントローラと組み合わせることで、高性能の拡張現実 HUD を実現できます。2:1 の縦横比は超広縦横比設計に対応し、1.3 メガピクセルの解像度は HUD アプリケーションで網膜に匹敵する解像度のディスプレイの実現を可能にします。DLP5530S-Q1 の光学スループットは前世代の DLP3030-Q1 車載用 DMD の 3 倍以上であるため、より大きな視野角と大きなドライバー・アイ・ボックスにより、優れたユーザー体験を実現できます。このチップセットを LED および光学システムと組み合わせることで、125% NTSC の深い飽和色、15,000cd/m^2 を超える非常に高い輝度、5000:1 を超える高いダイナミック調光比、太陽光負荷に対する高い耐性を実現できます。DLP5530S-Q1 車載用 DMD マイクロミラー・アレイは、高効率でより小型の光学エンジン設計が可能な底面照明用に構成されています。S450 パッケージは、DMD アレイへの熱抵抗が小さいため、より効率的なサーマル・ソリューションを実現できます。

製品情報

部品番号	パッケージ(1) (2)	本体サイズ (公称)
DLP5530S-Q1	FYS (149)	22.30mm × 32.20mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) このデータシートは、ヘッドアップ・ディスプレイ・アプリケーションにおけるこの DMD の仕様とアプリケーションに関連しています。ヘッドライトの仕様とアプリケーション情報については、DLP5531A-Q1 データシート (DLPS075) を参照してください。



DLP5530S-Q1 DLP® チップセットのシステム・ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2020) to Revision B (April 2021)	Page
• Updated Current and Power Consumption in *Electrical Characteristics* section	8

Changes from Revision * (August 2020) to Revision A (October 2020)	Page
• デバイス・ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

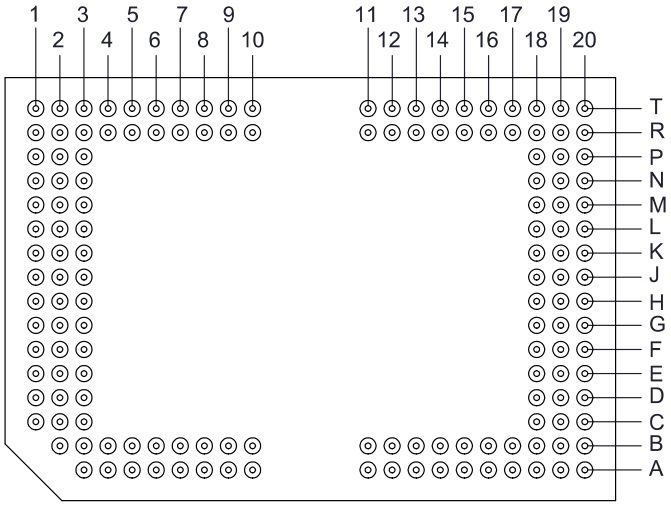


図 5-1. FYS Package
149-Pin CPGA
Bottom View

Pin Functions - Connector Pins

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	L2	I	SubLVDS	Double	Data, Negative
D_AN(1)	K2	I	SubLVDS	Double	Data, Negative
D_AN(2)	J2	I	SubLVDS	Double	Data, Negative
D_AN(3)	H2	I	SubLVDS	Double	Data, Negative
D_AN(4)	F2	I	SubLVDS	Double	Data, Negative
D_AN(5)	E2	I	SubLVDS	Double	Data, Negative
D_AN(6)	D2	I	SubLVDS	Double	Data, Negative
D_AN(7)	C2	I	SubLVDS	Double	Data, Negative
D_AP(0)	L1	I	SubLVDS	Double	Data, Positive
D_AP(1)	K1	I	SubLVDS	Double	Data, Positive
D_AP(2)	J1	I	SubLVDS	Double	Data, Positive
D_AP(3)	H1	I	SubLVDS	Double	Data, Positive
D_AP(4)	F1	I	SubLVDS	Double	Data, Positive
D_AP(5)	E1	I	SubLVDS	Double	Data, Positive
D_AP(6)	D1	I	SubLVDS	Double	Data, Positive
D_AP(7)	C1	I	SubLVDS	Double	Data, Positive
D_BN(0)	K19	I	SubLVDS	Double	Data, Negative
D_BN(1)	J19	I	SubLVDS	Double	Data, Negative
D_BN(2)	H19	I	SubLVDS	Double	Data, Negative
D_BN(3)	G19	I	SubLVDS	Double	Data, Negative
D_BN(4)	E19	I	SubLVDS	Double	Data, Negative
D_BN(5)	D19	I	SubLVDS	Double	Data, Negative
D_BN(6)	C19	I	SubLVDS	Double	Data, Negative
D_BN(7)	B19	I	SubLVDS	Double	Data, Negative

Pin Functions - Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BP(0)	K20	I	SubLVDS	Double	Data, Positive
D_BP(1)	J20	I	SubLVDS	Double	Data, Positive
D_BP(2)	H20	I	SubLVDS	Double	Data, Positive
D_BP(3)	G20	I	SubLVDS	Double	Data, Positive
D_BP(4)	E20	I	SubLVDS	Double	Data, Positive
D_BP(5)	D20	I	SubLVDS	Double	Data, Positive
D_BP(6)	C20	I	SubLVDS	Double	Data, Positive
D_BP(7)	B20	I	SubLVDS	Double	Data, Positive
DCLK_AN	G2	I	SubLVDS	Double	Clock, Negative
DCLK_AP	G1	I	SubLVDS	Double	Clock, Positive
DCLK_BN	F19	I	SubLVDS	Double	Clock, Negative
DCLK_BP	F20	I	SubLVDS	Double	Clock, Positive
LS_CLKN	R3	I	SubLVDS	Single	Clock for Low Speed Interface, Negative
LS_CLKP	T3	I	SubLVDS	Single	Clock for Low Speed Interface, Positive
LS_WDATAN	R2	I	SubLVDS	Single	Write Data for Low Speed Interface, Negative
LS_WDATAP	T2	I	SubLVDS	Single	Write Data for Low Speed Interface, Positive
CONTROL INPUTS					
DMD_DEN_ARSTZ	T10	I	LPSDR		Asynchronous Reset Active Low. Logic High Enables DMD.
LS_RDATA_A	T5	O	LPSDR	Single	Read Data for Low Speed Interface
LS_RDATA_B	T6	O	LPSDR	Single	Read Data for Low Speed Interface
TEMPERATURE SENSE DIODE					
TEMP_N	P1	O			Calibrated temperature diode used to assist accurate temperature measurements of DMD die.
TEMP_P	N1	I			
RESERVED PINS					
VCCH	A8	Ground			Reserved Pin. Connect to Ground.
VCCH	A9	Ground			
VCCH	A10	Ground			
VCCH	B8	Ground			
VCCH	B9	Ground			
VCCH	B10	Ground			
VSSH	A11	Ground			Reserved Pin. Connect to Ground.
VSSH	A12	Ground			
VSSH	A13	Ground			
VSSH	B11	Ground			
VSSH	B12	Ground			
VSSH	B13	Ground			

Pin Functions - Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
POWER					
VBIAS	T7	Power			Supply voltage for positive bias level at micromirrors.
VBIAS	T15	Power			
VOFFSET	T9	Power			Supply voltage for High Voltage CMOS core logic. Supply voltage for offset level at micromirrors.
VOFFSET	T13	Power			
VOFFSET	A5	Power			
VOFFSET	B5	Power			
VOFFSET	A16	Power			
VOFFSET	B16	Power			
VRESET	T8	Power			Supply voltage for negative reset level at micromirrors.
VRESET	T14	Power			
VDD	R4	Power			Supply voltage for Low Voltage CMOS core logic; for LPSDR inputs; for normal high level at micromirror address electrodes.
VDD	R10	Power			
VDD	R11	Power			
VDD	R20	Power			
VDD	N2	Power			
VDD	M20	Power			
VDD	L3	Power			
VDD	K18	Power			
VDD	H3	Power			
VDD	G18	Power			
VDD	E3	Power			
VDD	D18	Power			
VDD	C3	Power			
VDD	A6	Power			
VDD	A18	Power			
VDDI	T4	Power			Supply voltage for SubLVDS receivers.
VDDI	R1	Power			
VDDI	M3	Power			
VDDI	L18	Power			
VDDI	J3	Power			
VDDI	H18	Power			
VDDI	F3	Power			
VDDI	E18	Power			
VDDI	B3	Power			
VDDI	B18	Power			

Pin Functions - Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
VSS	T1	Ground			Common return. Ground for all power.
VSS	T16	Ground			
VSS	T19	Ground			
VSS	T20	Ground			
VSS	R5	Ground			
VSS	R6	Ground			
VSS	R7	Ground			
VSS	R8	Ground			
VSS	R9	Ground			
VSS	R13	Ground			
VSS	R14	Ground			
VSS	R15	Ground			
VSS	P2	Ground			
VSS	P3	Ground			
VSS	P20	Ground			
VSS	N19	Ground			
VSS	N20	Ground			
VSS	M1	Ground			
VSS	M2	Ground			
VSS	L19	Ground			
VSS	L20	Ground			
VSS	K3	Ground			
VSS	J18	Ground			
VSS	G3	Ground			
VSS	F18	Ground			
VSS	D3	Ground			
VSS	C18	Ground			
VSS	B2	Ground			
VSS	B4	Ground			
VSS	B15	Ground			
VSS	B17	Ground			
VSS	A3	Ground			
VSS	A4	Ground			
VSS	A7	Ground			
VSS	A15	Ground			
VSS	A17	Ground			
VSS	A19	Ground			
VSS	A20	Ground			

Pin Functions - Test Pads

NUMBER	SYSTEM BOARD
T11	Do not connect
T12	Do not connect
T17	Do not connect
T18	Do not connect
R12	Do not connect
R16	Do not connect
R17	Do not connect
R18	Do not connect
R19	Do not connect
P18	Do not connect
P19	Do not connect
N3	Do not connect
N18	Do not connect
M18	Do not connect
M19	Do not connect
B6	Do not connect
B7	Do not connect
B14	Do not connect
A14	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low speed interface	–0.5		2.3	V
VDDI	Supply voltage for SubLVDS receivers	–0.5		2.3	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode	–0.5		8.75	V
VBIAS	Supply voltage for micromirror electrode	–0.5		17	V
VRESET	Supply voltage for micromirror electrode	–11		0.5	V
| VDDI–VDD |	Supply voltage delta (absolute value)			0.3	V
| VBIAS–VOFFSET |	Supply voltage delta (absolute value)			8.75	V
| VBIAS–VRESET |	Supply voltage delta (absolute value)			28	V
INPUT VOLTAGE					
Input voltage for other inputs LPSDR		–0.5		VDD + 0.5	V
Input voltage for other inputs SubLVDS		–0.5		VDDI + 0.5	V
INPUT PINS					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value)			810	mV
I_{ID}	SubLVDS input differential current			10	mA
TEMPERATURE DIODE					
I_{TEMP_DIODE}	Max current source into temperature diode			120	µA
ENVIRONMENTAL					
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in 図 6-1			37	mW/mm^2
T_{ARRAY}	Operating DMD array temperature	–40		105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	–40	125	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.7	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.7	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode	8.25	8.5	8.75	V
VBIAS	Supply voltage for mirror electrode	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrode	–9.5	–10	–10.5	V
| VDDI–VDD |	Supply voltage delta (absolute value)			0.3	V
| VBIAS–VOFFSET |	Supply voltage delta (absolute value)			8.75	V
CLOCK FREQUENCY					
f_{max}	Clock frequency for low speed interface LS_CLK			120	MHz
f_{max}	Clock frequency for high speed interface DCLK			600	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value)(2)	150	250	350	mV
V_{CM}	Common mode voltage (2)	700	900	1100	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance(3)	80	100	120	Ω
ENVIRONMENTAL					
T_{ARRAY}	Operating DMD array temperature(5)	–40		105	°C
ILL_{UV}	Illumination, wavelength < 395 nm (4)			2	mW/cm ^{2}
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in area shown in 図 6-1			28	mW/mm ^{2}

(1) *Recommended Operating Conditions* are applicable after the DMD is installed in the final product.
(2) See 図 6-6 and 図 6-7
(3) See 図 6-8
(4) The maximum operation conditions for operating temperature and UV illumination shall not be implemented simultaneously.
(5) Operating profile information for device micromirror landed duty-cycle and temperature may be provided if requested.

Illumination Overfill Diagram

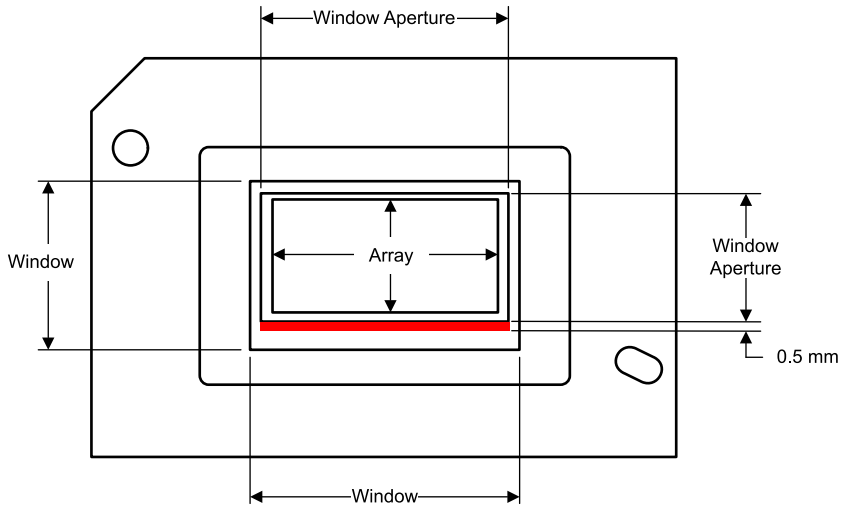


図 6-1. Illumination Overfill Diagram

6.5 Thermal Information

THERMAL METRIC		DLP5530A-Q1 FYS (CPGA) 149 PINS	UNIT
Thermal resistance	Active area-to-test point 1 (TP1) (1)	1.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD(2)	VDD = 1.95 V			310	mA
I_{DDI}	Supply current: VDDI(2)	VDDI = 1.95 V			55	mA
I_{OFFSET}	Supply current: VOFFSET	VOFFSET = 8.75 V			6	mA
I_{BIAS}	Supply current: VBIAS	VBIAS = 16.5 V			1	mA
I_{RESET}	Supply current: VRESET	VRESET = -10.5 V			-4.5	mA
POWER						
P_{DD}	Supply power dissipation: VDD(2)	VDD = 1.95 V			604.5	mW
P_{DDI}	Supply power dissipation: VDDI(2)	VDDI = 1.95 V			107.25	mW
P_{OFFSET}	Supply power dissipation: VOFFSET	VOFFSET = 8.75 V			52.5	mW
P_{BIAS}	Supply power dissipation: VBIAS	VBIAS = 16.5 V			16.5	mW
P_{RESET}	Supply power dissipation: VRESET	VRESET = -10.5 V			47.25	mW
P_{TOTAL}	Supply power dissipation: Total				828	mW
LPSDR INPUT (3)						
$V_{IH(DC)}$	DC input high voltage		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	See 図 6-9	0.1 × VDD		0.4 × VDD	V
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			300	nA
LPSDR OUTPUT (4)						
V_{OH}	DC output high voltage	I_{OH} = -2mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz (1152 X 144 micromirrors)	350	400	450	pF
C_{TEMP}	Temperature sense diode capacitance	f = 1 MHz			20	pF

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) Supply power dissipation based on non–compressed commands and data.
(3) LPSDR input specifications are for pin DMD_DEN_ARSTZ.
(4) LPSDR output specification is for pins LS_RDATA_A and LS_RDATA_B.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate (1)	(20% to 80%) × VDD	0.25			V/ns
t_f	Fall slew rate (1)	(80% to 20%) × VDD	0.25			V/ns
$t_{W(H)}$	Pulse duration LS_CLK high(3)	50% to 50% reference points	0.75			ns
$t_{W(L)}$	Pulse duration LS_CLK low(3)	50% to 50% reference points	0.75			ns
t_{su}	Setup time(3)	LS_WDATA valid before LS_CLK ↑ or LS_CLK ↓	1.5			ns
t_h	Hold time(3)	LS_WDATA valid after LS_CLK ↑ or LS_CLK ↓	1.5			ns
SubLVDS						
t_r	Rise slew rate(2)	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate(2)	80% to 20% reference points	0.7	1		V/ns
t_c	Cycle time DCLK(3)		1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high(3)	50% to 50% reference points	0.75			ns
$t_{W(L)}$	Pulse duration DCLK low(3)	50% to 50% reference points	0.75			ns
t_{WINDOW}	Window time(3) (4)	Setup time + Hold time	0.3			ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(5)				2000	ns

(1) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 図 6-2
(2) See 図 6-3
(3) See 図 6-4
(4) See 図 6-5
(5) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

Electrical and Timing Diagrams

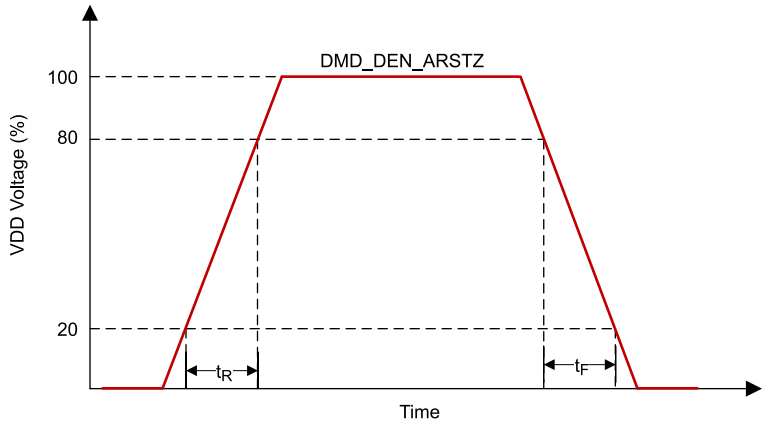


図 6-2. LPSDR Input Rise and Fall Slew Rate

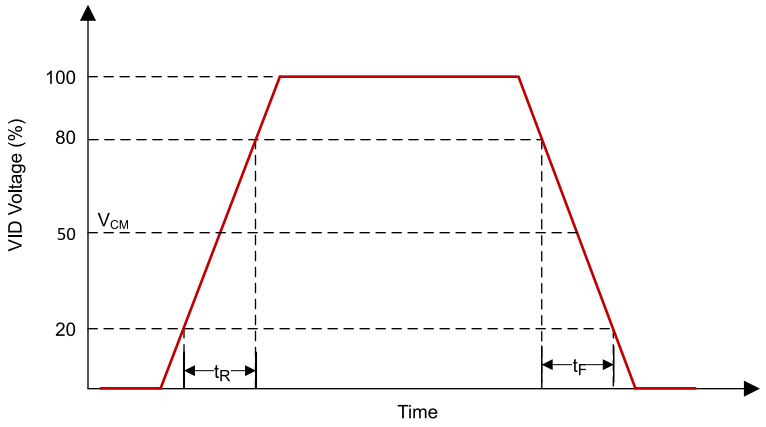


図 6-3. SubLVDS Input Rise and Fall Slew Rate

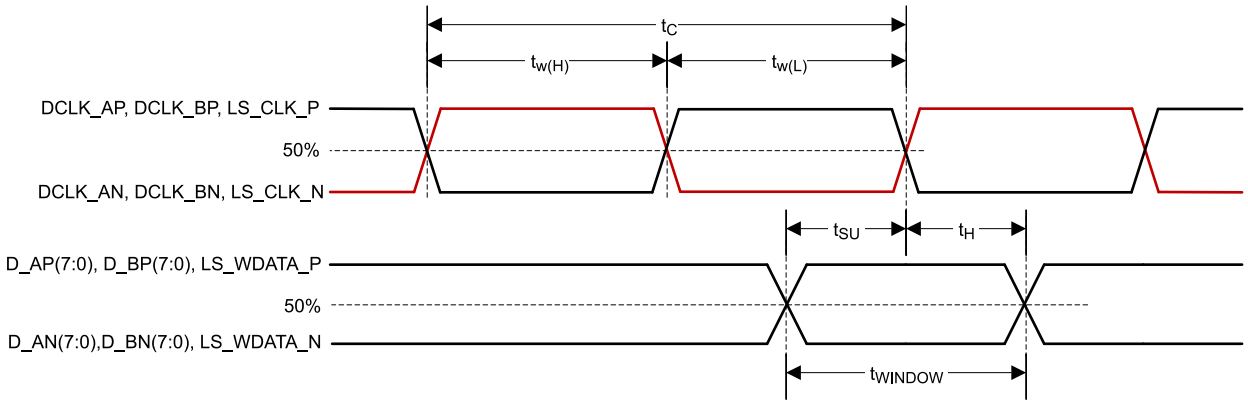
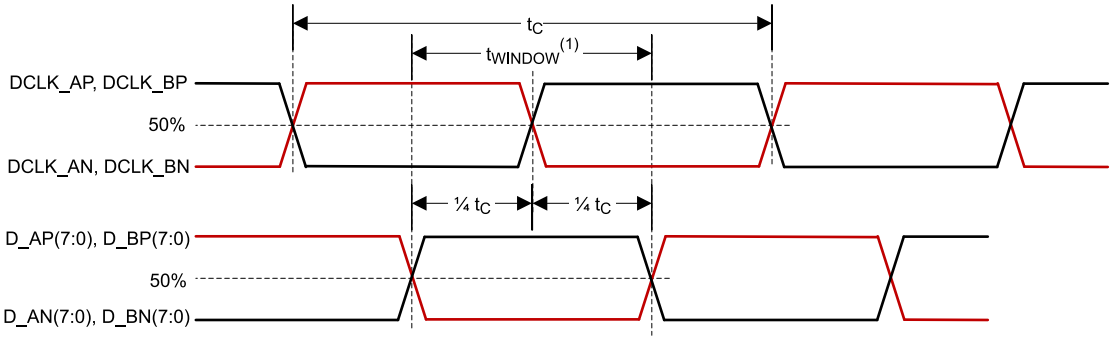


図 6-4. SubLVDS Switching Parameters



(1) High-speed training scan window

図 6-5. High-Speed Training Scan Window

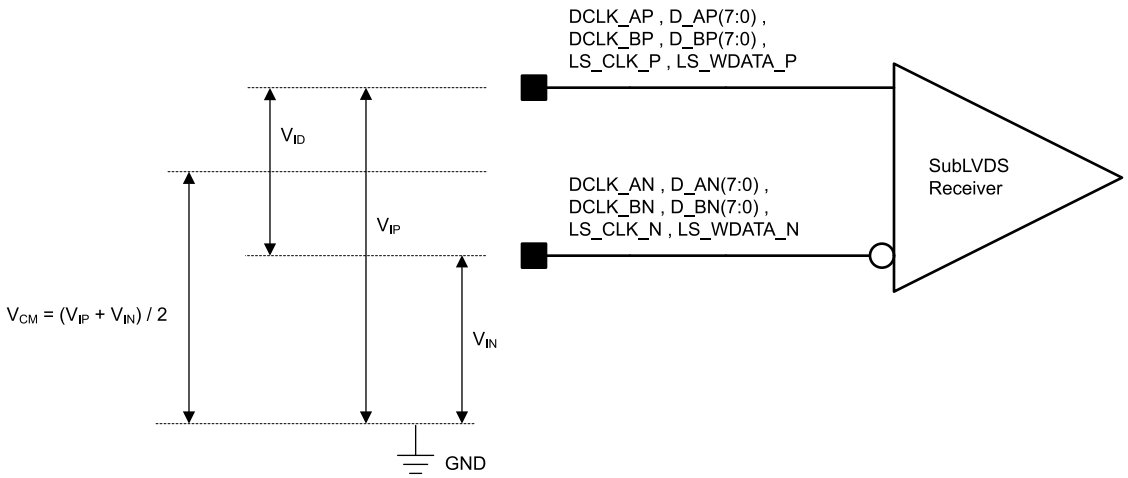


図 6-6. SubLVDS Voltage Parameters

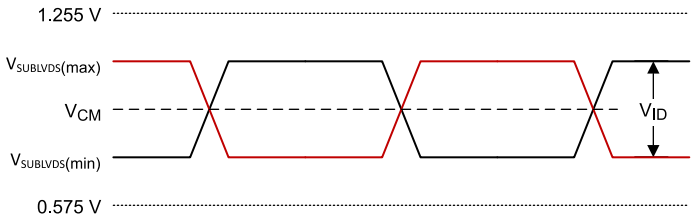


図 6-7. SubLVDS Waveform Parameters

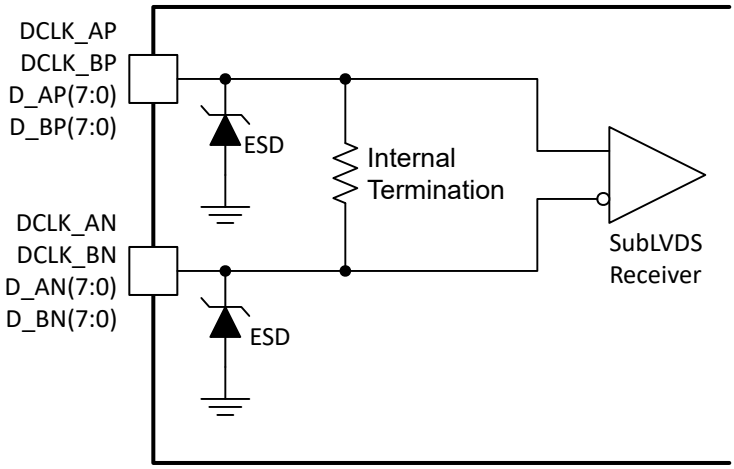


図 6-8. SubLVDS Equivalent Input Circuit

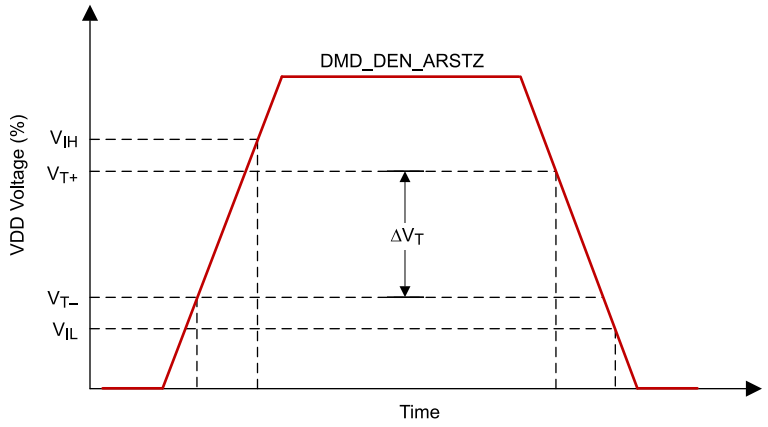


図 6-9. LPSDR Input Hysteresis

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output.(2)	C_L = 45 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

(1) Device electrical characteristics are over Recommended Operating Conditions unless otherwise noted.
(2) See 図 6-10 and 図 6-11

LPSDR and Test Load Circuit Diagrams

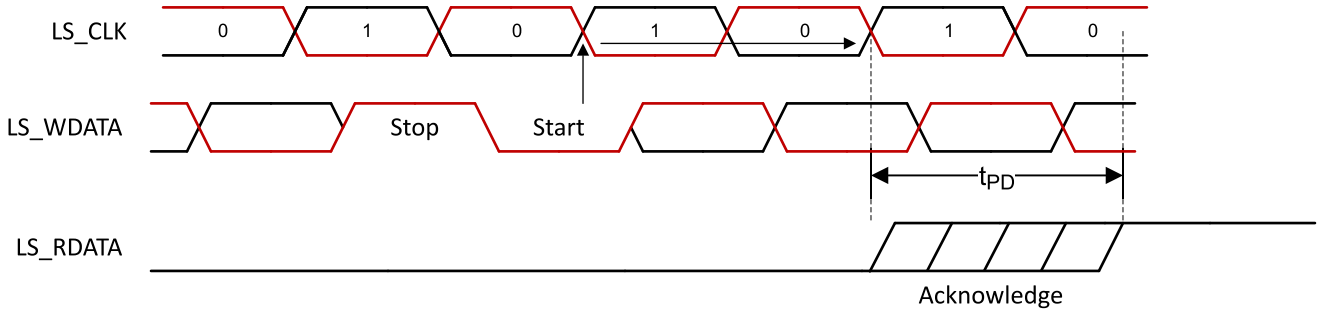


図 6-10. LPSDR Read Out

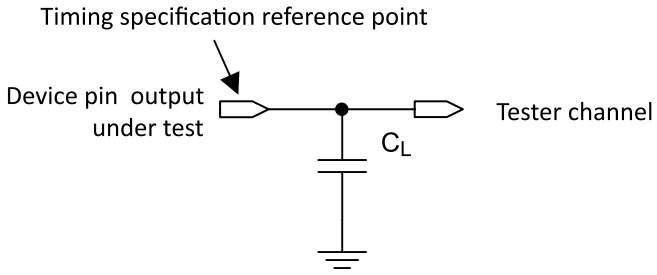


図 6-11. Test Load Circuit for Output Propagation Measurement

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Condition 1: Maximum load evenly distributed within each area (1)					
	Thermal Interface Area			110.8	N
	Electrical Interface Area			111.3	
Condition 2: Maximum load evenly distributed within each area (1)					
	Thermal Interface Area			0	N
	Electrical Interface Area			222.1	

(1) See 図 6-12

System Interface Loads Diagram

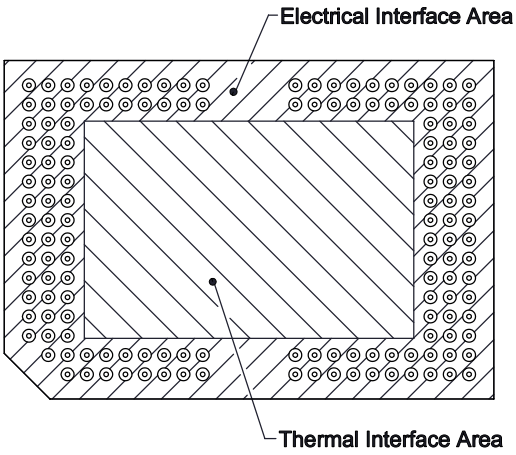


図 6-12. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

PARAMETER			VALUE	UNIT
M	Number of active columns(1)		1152	micromirrors
N	Number of active rows(1)		1152	micromirrors
ε	Micromirror (pixel) pitch - diagonal(1)		7.6	µm
P	Micromirror (pixel) pitch - horizontal and vertical(1)		10.8	µm
	Micromirror active array width	(P × M) + (P / 2)	12.447	mm
	Micromirror active array height	(P x N) / 2 + (P / 2)	6.226	mm
	Micromirror active border	Pond of micromirrors (POM) (2)	10	micromirrors/side

(1) See 図 6-13
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

Array Physical Characteristics Diagram

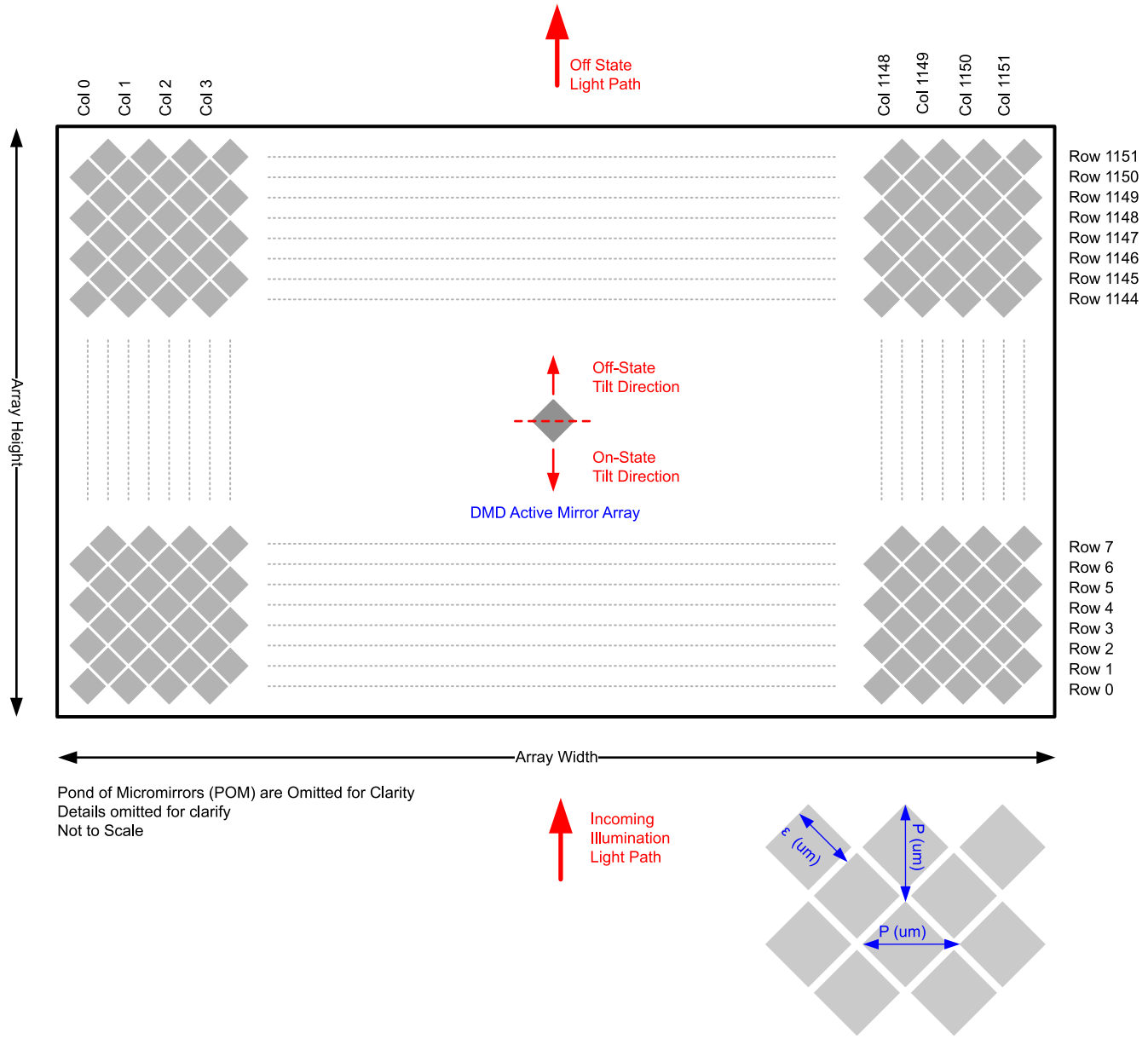


図 6-13. Micromirror Array Physical Characteristics

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		12		degree
Micromirror tilt angle tolerance(2)		–1		1	degree
DMD efficiency(3)	420 nm - 700 nm		66%		

(1) Measured relative to the plane formed by the overall micromirror array at 25°C.
(2) For some applications, it is critical to account for the micromirror tilt angle variation in the overall optical system design. With some optical system designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some optical system designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic micromirror landed duty-cycle and do not include system optical efficiency or overfill loss. This number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in DLPA083A

6.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture (1)				See (1)	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

6.13 Chipset Component Usage Specification

The DLP5530S-Q1 is a component of a chipset. Reliable function and operation of the DLP5530S-Q1 requires that it be used in conjunction with the TPS99000S-Q1 and DLPC230S-Q1, and includes components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7 Detailed Description

7.1 Overview

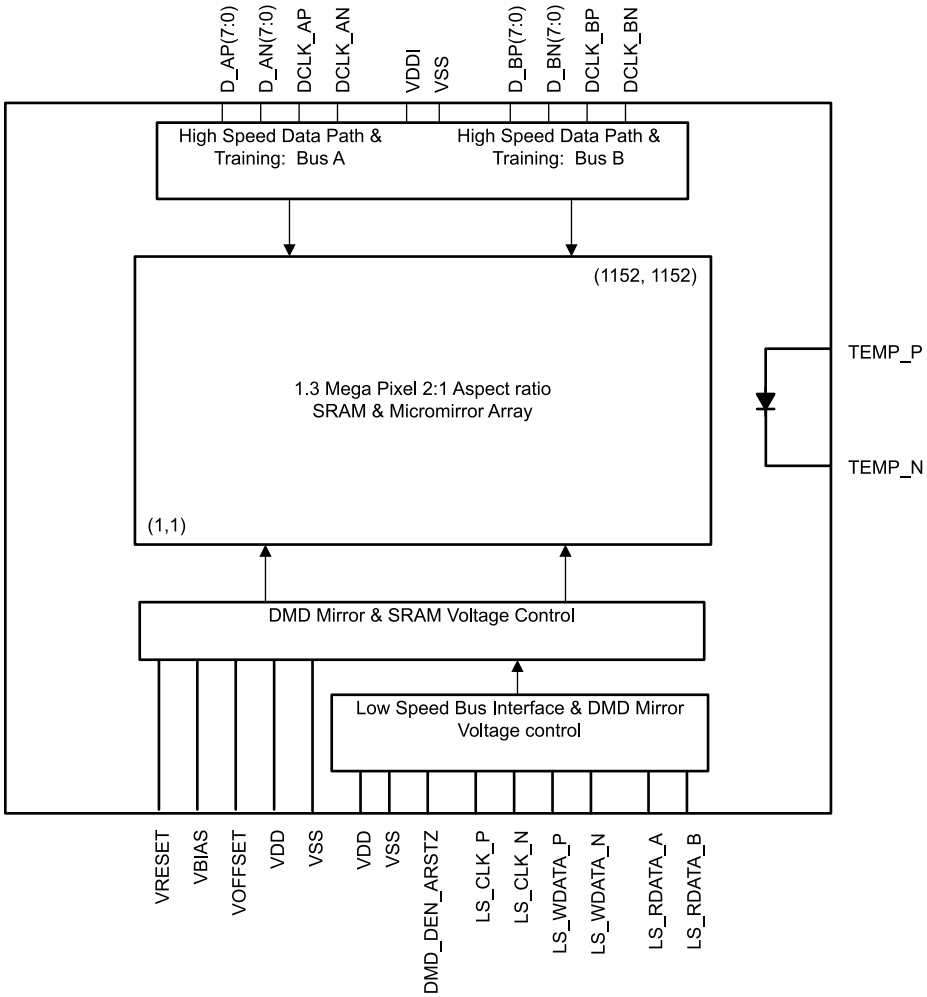
The DLP5530S-Q1 Automotive DMD consists of 1,327,104 highly reflective, digitally switchable, micrometer-sized mirrors organized in a two-dimensional array. As shown in Figure 6-13, the micromirror array consists of 1152 micromirror columns × 1152 micromirror rows in a diamond pixel configuration with a 2:1 aspect ratio.

Around the perimeter of the 1152 × 1152 array of micromirrors is a uniform band of border micromirrors called the Pond of Micromirrors (POM). The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1152 × 1152 active array.

Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row. Each mirror is switchable between two discrete angular positions: –12° and +12°. The mirrors are illuminated from the bottom which allows for compact and efficient system optical design.

Although the native resolution of the DLP5530S-Q1 is 1152 × 1152, when paired with the DLPC230S-Q1 controller, the DLP5530S-Q1 can be driven with different resolutions to utilize the 2:1 aspect ratio. For example, Head-Up Display applications typically use a resolution of 1152 × 576. Please see the DLPC230S-Q1 automotive DMD controller data sheet (DLPS054) for a list of supported resolutions. Diamond pixel arrays also have the capability to increase display resolution beyond native resolution. Future controllers or video formatters may take advantage of this enhanced resolution.

7.2 Functional Block Diagram



7.3 Feature Description

The DLP5530S-Q1 consists of a two-dimensional array of 1-bit CMOS memory cells driven by a sub-LVDS bus from the DLPC230S-Q1 and powered by the TPS99000S-Q1. The temperature sensing diode is used to continuously monitor the DMD array temperature.

To ensure reliable operation the DLP5530S-Q1 must be used with the DLPC230S-Q1 DMD display controller and the TPS99000S-Q1 system management and illumination controller.

7.3.1 Sub-LVDS Data Interface

The Sub-LVDS signaling protocol was designed to enable very fast DMD data refresh rates while simultaneously maintaining low power and low emission.

Data is loaded into the SRAM under each micromirror using the sub-LVDS interface from the DLPC230S-Q1. This interface consists of 16 pairs of differential data signals plus two clock pairs into two separate buses A and B loading the left and right half of the SRAM array. The data is latched on both transitions creating a double data rate (DDR) interface. The sub-LVDS interface also implements a continuous training algorithm to optimize the data and clock timing to allow for a more robust interface.

The entire DMD array of 1.3 million pixels can be updated at a rate of less than 100 µs as a result of the high speed sub-LVDS interface.

7.3.2 Low Speed Interface for Control

The purpose of the low speed interface is to configure the DMD at power up and power down and to control the micromirror reset voltage levels that are synchronized with the data loading. The micromirror reset voltage controls the time when the mirrors are mechanically switched. The low speed differential interface includes 2 pairs of signals for write data and clock, and 2 single-ended signals for output (A and B).

7.3.3 DMD Voltage Supplies

The micromirrors require unique voltage levels to control the mechanical switching from –12° to +12°. These voltage levels are nominally 16 V, 8.5 V, and –10 V (VBIAS, VOFFSET, and VRESET), and are generated by the TPS99000S-Q1.

7.3.4 Asynchronous Reset

Reset of the DMD is required and controlled by the DLPC230S-Q1 via the signal DMD_DEN_ARSTZ.

7.3.5 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411 temperature monitoring device. The DLPC230S-Q1 monitors the temperature sense diode via the TMP411. The DLPC230S-Q1 operation of the DMD timing can be adjusted based on the DMD array temperature, therefore this connection is essential to ensure reliable operation of the DMD.

図 7-1 shows the typical connection between the DLPC230S-Q1, TMP411, and the DMD.

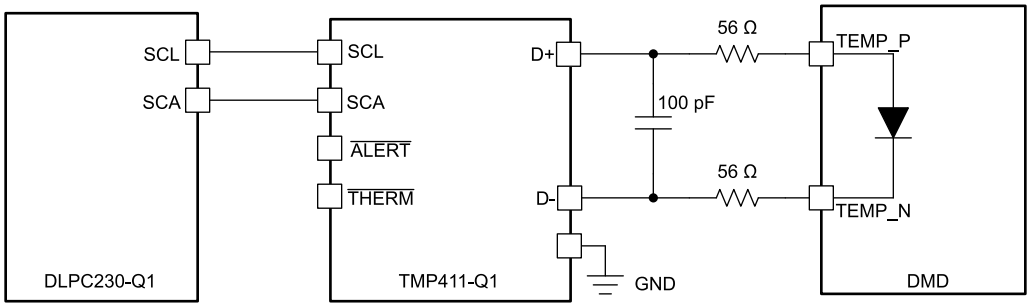


図 7-1. Temperature Sense Diode Typical Circuit Configuration

7.3.5.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Three different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base–emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411-Q1 data sheet for detailed information about temperature diode theory and measurement. 図 7-2 and 図 7-3 illustrate the relationships between the current and voltage through the diode.

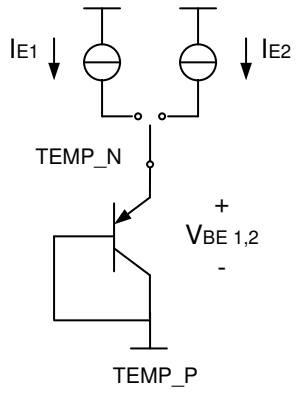


図 7-2. Temperature Measurement Theory

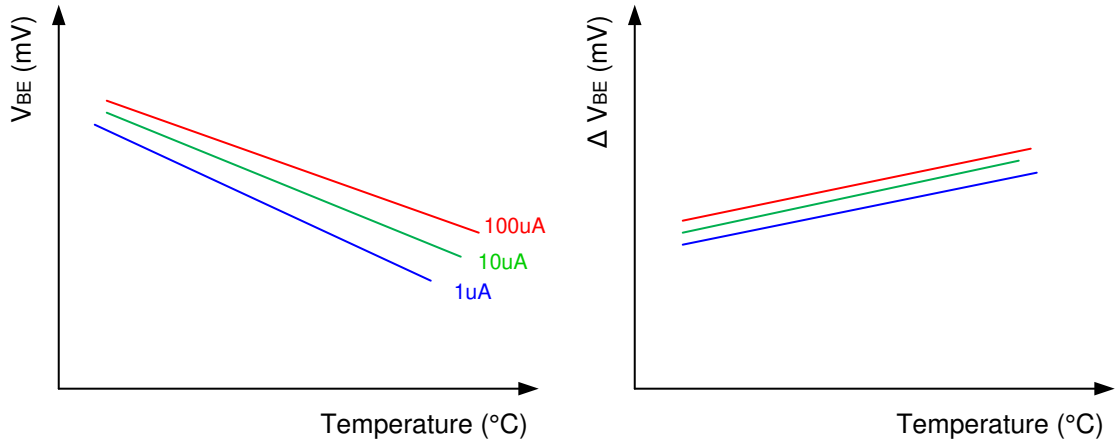


図 7-3. Example of Delta VBE Versus Temperature

7.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This cone angle defined by the numerical aperture should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines the DMD's capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces.

7.4.2 Pupil Match

TI's optical and image performance specifications assume that the exit pupil of the illumination optics is nominally centered and located at the entrance pupil position of the projection optics. Misalignment of pupils between the illumination and projection optics can degrade screen image uniformity and cause objectionable artifacts in the display's border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible.

Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Heat load on the aperture in the areas shown in 図 6-1 should not exceed the values listed in *Recommended Operating Conditions*. This area is a 0.5-mm wide area the length of the aperture opening. The values listed in *Recommended Operating Conditions* assume a uniform distribution. For a non-uniform distribution please contact TI for additional information.

Note

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED PREVIOUSLY.

7.5 DMD Image Performance Specification

表 7-1. DMD Image Performance

PARAMETER(1) (2)	MIN	NOM	MAX	UNIT
Dark Blemishes - Viewed on a linear blue 60 screen.(3)			4	
Light Blemishes - Viewed on a linear gray 10 screen.			4	
Bright Pixels - Viewed on a linear gray 10 screen.			0	micromirrors
Dark Pixels - Viewed on a white screen.			4	micromirrors

(1) See *セクション 7.4*
(2) Blemish counts do not include reflections or shadows of the same artifact. Any artifact that is not specifically called out in this table is acceptable. Viewing distance must be > 60 in. Screen size should be similar to application image size. All values referenced are in linear gamma. Non-linear gamma curves may be running by default, and it should be ensured with a TI applications engineer that the equivalent linear gamma value as specified is used to judge artifacts.
(3) Linear gray 5 may be substituted in monochrome applications.

7.6 Micromirror Array Temperature Calculation

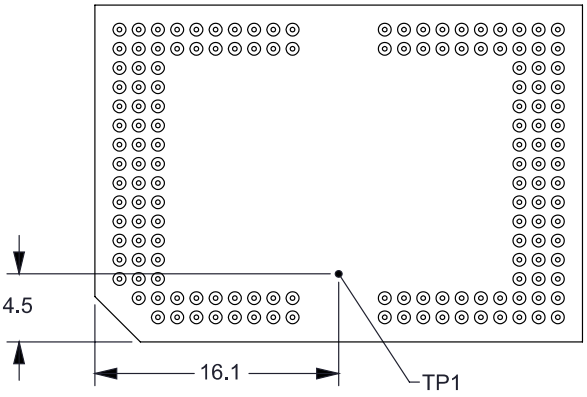


図 7-4. DMD Thermal Test Points

The active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in 図 7-4) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

where

- T_{ARRAY} = computed DMD array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature, TP1 location in 図 7-4 (°C)
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to thermal test point TP1 (°C/W), see *Thermal Information*
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (W)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{ILLUMINATION} = (C_{L2W} \times SL)$
- C_{L2W} = conversion constant for screen lumens to power on the DMD (W/lm)
- SL = measured screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown above are valid for a 1–chip DMD system with a total projection efficiency from DMD to the screen of 87%.

The constant C_{L2W} is based on the DMD array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The following is a sample calculation for a typical projection application:

1. SL = 50 lm
2. C_{L2W} = 0.00293 W/lm
3. $Q_{ELECTRICAL}$ = 0.4 W (This number does not represent an actual DMD electrical power; for illustration purposes only)
4. $R_{ARRAY–TO–CERAMIC}$ = 1.1°C/W
5. $T_{CERAMIC}$ = 55°C
6. Q_{ARRAY} = 0.4 W + (0.00293 W/lm × 50 lm) = 0.5465 W
7. T_{ARRAY} = 55°C + (0.5465 W × 1.1°C/W) = 55.6°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DLP5530S-Q1 chipset is designed to support projection-based automotive applications such as head-up display systems.

8.2 Typical Application

The chipset consists of three components—the DLP5530S-Q1 automotive DMD, the DLPC230S-Q1, and the TPS99000S-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC230S-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99000S-Q1 is a controller for the illumination sources (e.g. LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC230S-Q1 and the TPS99000S-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features. 図 8-1 is a system level block diagram with these devices in the DLP head-up display configuration and shows the primary features and functions of each device.

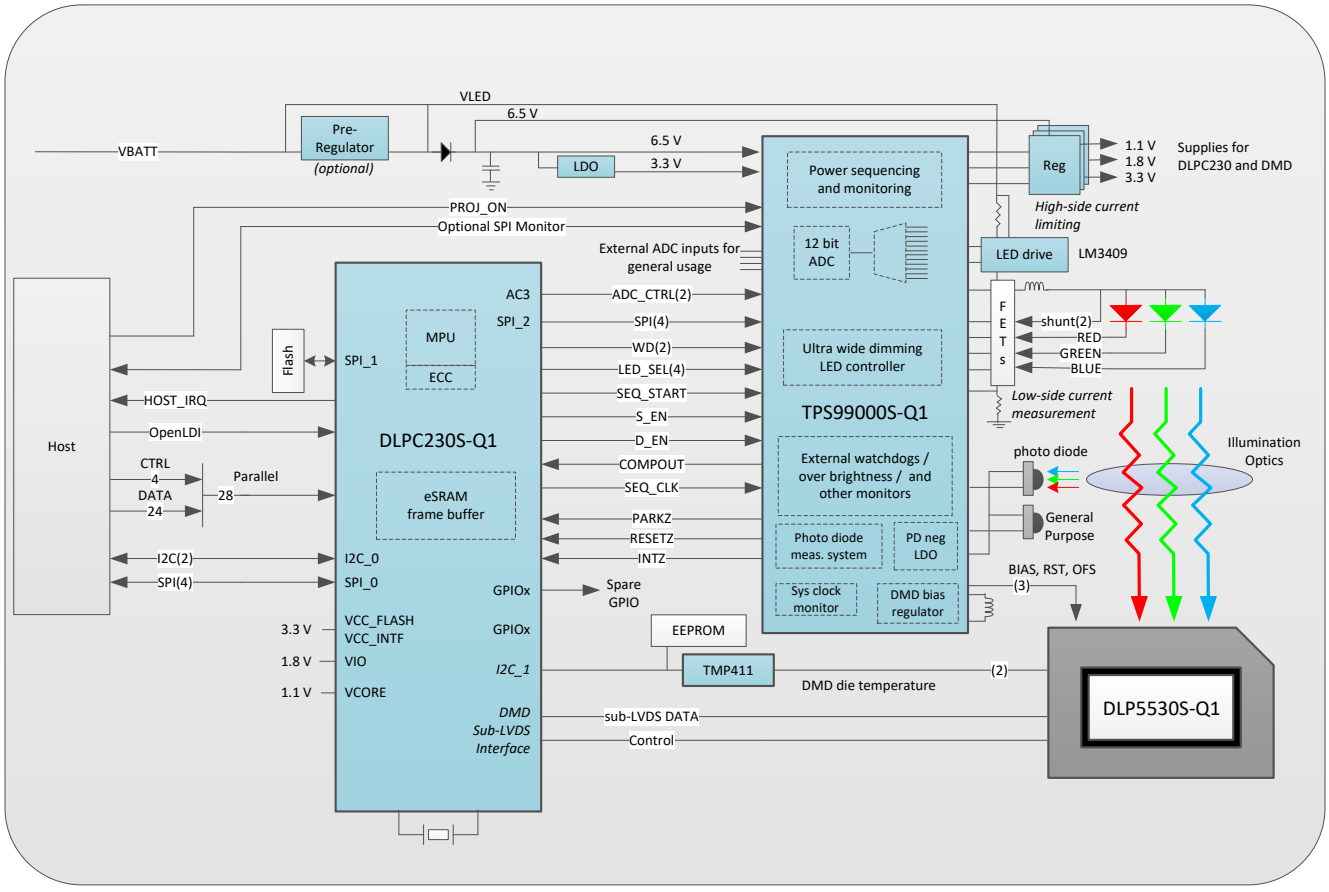


図 8-1. Head-Up Display System Block Diagram

8.2.1 Application Overview

図 8-1 shows the system block diagram for a DLP HUD system. The system uses the DLPC230S-Q1, TPS99000S-Q1, and the DLP5530S-Q1 automotive DMD to enable a head-up display with high brightness, high efficiency, and a large virtual image distance. The combination of the DLPC230S-Q1 and TPS99000S-Q1 removes the need for external SDRAM and a dedicated microprocessor. The chipset manages the illumination control of LED sources, power sequencing functions, and system management functions. Additionally, the chipset supports numerous system diagnostic and built-in self test (BIST) features. The following paragraphs describe the functionality of the chipset used for a HUD system in more detail.

The DLPC230S-Q1 is a controller for the DMD and the light sources in the DLP HUD module. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video. The DLPC230S-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create a video with a multi-colored display.

The DLPC230S-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Host commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for host commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The SPI flash memory provides the embedded software for the DLPC230S-Q1's ARM core and default settings. The TPS99000S-Q1 provides diagnostic and monitoring information to the DLPC230S-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^2C interface to provide the DMD array temperature to the DLPC230S-Q1.

The outputs of the DLPC230S-Q1 are configuration and monitoring commands to the TPS99000S-Q1, timing controls to the LED or laser driver, control and data signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC230S-Q1 communicates with the TPS99000S-Q1 over an SPI bus. It uses this to configure the TPS99000S-Q1 and to read monitoring and diagnostics information from the TPS99000S-Q1. The DLPC230S-Q1 sends drive enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a sub-LVDS interface.

The TPS99000S-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the DLP HUD system. The power sequencing and monitoring blocks of the TPS99000S-Q1 properly power up the DMD and provide accurate DMD voltage rails (–16 V, 8.5 V, and 10 V), and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000S-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000S-Q1 has several general-purpose ADCs that designers can use for system level monitoring, such as over-brightness detection.

The TPS99000S-Q1 receives inputs from the DLPC230S-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC230S-Q1 sends configuration and control commands to the TPS99000S-Q1 over an SPI bus and several other control signals. The DLPC230S-Q1's clocks are also monitored by the watchdogs in the TPS99000S-Q1 to detect any errors. The power rails are monitored by the TPS99000S-Q1 in order to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000S-Q1 using a dedicated SPI bus, which enables independent monitoring. Additionally the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000S-Q1 has several general-purpose ADCs that can be used to implement system level monitoring functions.

The outputs of the TPS99000S-Q1 are diagnostic information and error alerts to the DLPC230S-Q1, and control signals to the LED or laser driver. The TPS99000S-Q1 can output diagnostic information to the host and the DLPC230S-Q1 over two SPI buses. In case of critical system errors, such as power loss, it outputs signals to the DLPC230S-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data), and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface with the DLPC230S-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system the mirrors are used as pixels in order to display an image.

8.2.2 Reference Design

For information about connecting together the DLP5530S-Q1 DMD, DLPC230S-Q1 controller, and TPS99000S-Q1, please contact the TI Application Team for additional information about the DLP5530S-Q1 evaluation module (EVM). TI has optical-mechanical reference designs available, see the TI Application team for more information.

8.2.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation the Application Report *Reliability Lifetime Estimates for DLP3030-Q1 and DLP553x-Q1 DMDs in Automotive Applications* may be provided. See the TI Application team for more information.

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the TPS99000S-Q1 device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. VSS must also be connected.

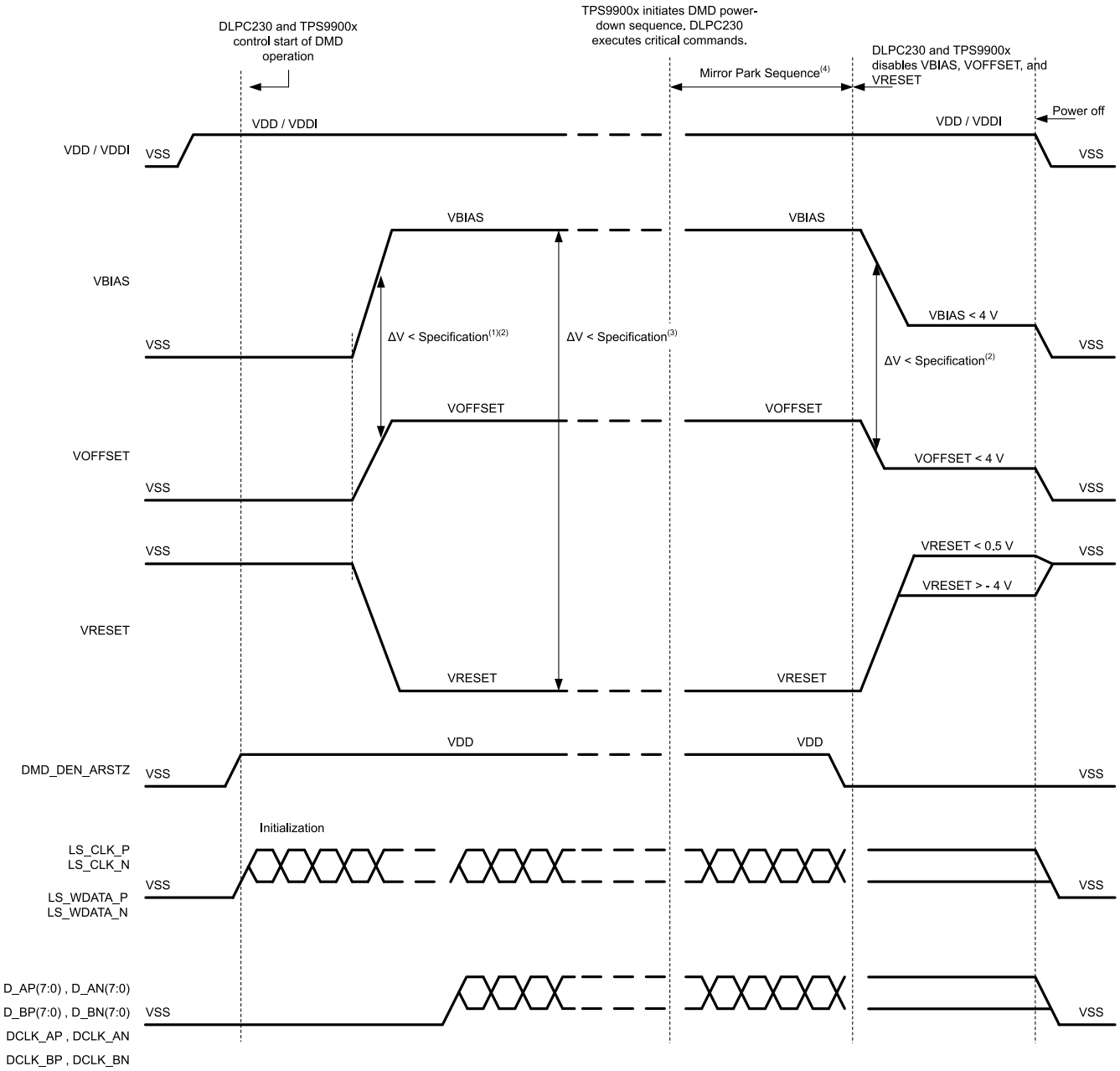
9.1 Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in 図 9-1.

9.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions* (Refer to Note 2 in セクション 9.3).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in セクション 9.3.

9.3 Power Supply Sequencing Requirements



A. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in the Recommended Operating Conditions. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Also, the TPS99000S-Q1 is capable of managing the timing between VBIAS and VOFFSET.

B. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified than the limit shown in the Recommended Operating Conditions.

C. When system power is interrupted, the TPS99000S-Q1 initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the Micromirror Park Sequence.

D. Drawing is not to scale and details are omitted for clarity.

図 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

10 Layout

10.1 Layout Guidelines

Please refer to the DLPC230S-Q1 and TPS99000S-Q1 data sheets for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals.
- Minimum of two 220-nF decoupling capacitors close to VBIAS.
- Minimum of two 220-nF decoupling capacitors close to VRESET.
- Minimum of two 220-nF decoupling capacitors close to VOFFSET.
- Minimum of four 100-nF decoupling capacitors close to VDDI and VDD.
- Temperature diode pins

  The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411 are sensitive to noise. Please see the TMP411 data sheet for specific routing recommendations.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

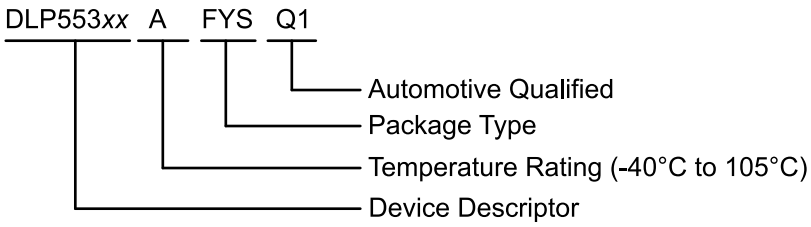


図 11-1. Part Number Description

11.1.2 Device Markings

The device marking includes the legible character string GHJJJJK DLP553xxAFYSQ1. GHJJJJK is the lot trace code. DLP553*xx*AFYSQ1 is the part number.

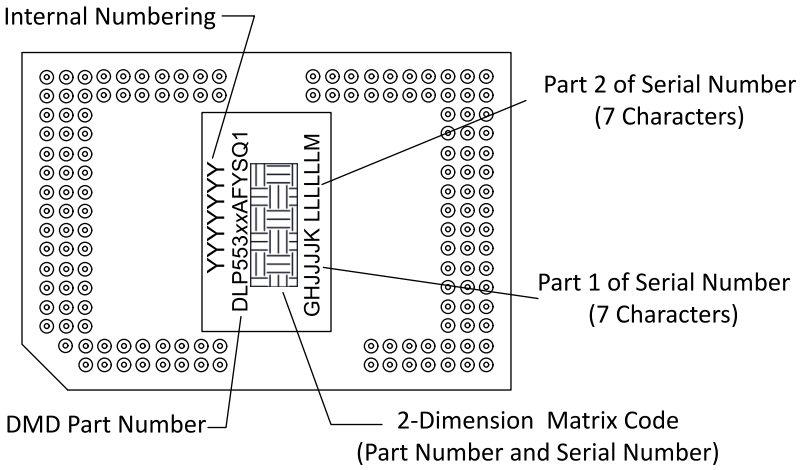


図 11-2. DMD Marking

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.6 DMD Handling

The DMD is an optical device so precautions should be taken to avoid damaging the glass window. Please see the application note DLPA019 DMD Handling for instructions on how to properly handle the DMD.

11.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP5530SAFYSQ1	ACTIVE	CPGA	FYS	149	33	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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