# DLPA300 ドライバ、DLP デジタル・マイクロミラー・デバイス用

## 1 特長

- DLP® 9µm ピクセルのデジタル・マイクロミラー・デバイス (DMD) 向けに設計
  - DLP780NE
  - DLP780TE
  - DLP800RE
  - DLP781NE
  - DLP781TE
  - DLP801RE
  - DLP801XE
- 9µm ピクセルの DMD が必要とするマイクロミラーのクロック・パルスを生成
- マイクロミラーのクロック・パルスに必要とされる専用の電圧レベルを生成

## 2 アプリケーション

- 企業向けプロジェクタ
- スマート・プロジェクタ
- レーザー TV
- デジタル・サイネージ
- 大会場向けプロジェクタ
- ProAV プロジェクト

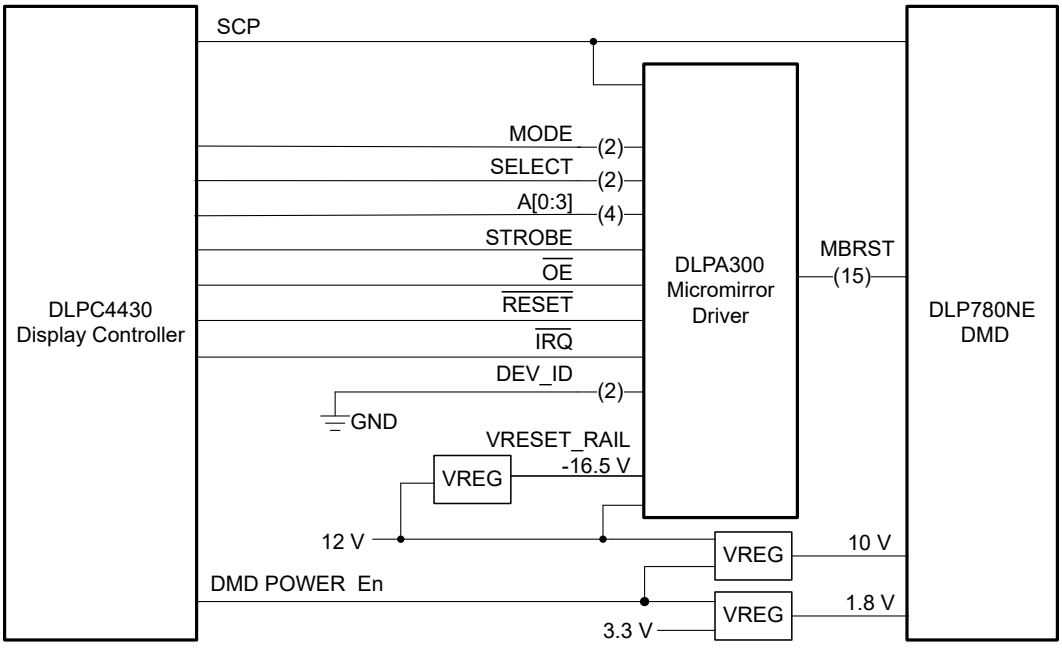
## 3 概要

DLPA300 デバイスは、DLP780NE、DLP780TE、DLP800RE、DLP781NE、DLP781TE、DLP801RE、DLP801XE DMD などの DLP 9µm ピクセル、高効率 デジタル・マイクロミラー・デバイス (DMD) のマイクロミラー・ドライバです。これらの DMD チップセットの一部である DLPA300 マイクロミラー・ドライバは、$V_{OFFSET}$ および $V_{BIAS}$ 電圧を生成します。また、$V_{OFFSET}$、$V_{BIAS}$、および外部で生成された $V_{RESET}$ を切り替えて、DLP DMD のマイクロミラー・クロック・パルスを作成します。この波形のタイミングは、TI DLPC4420 または DLPC4430 ディスプレイ・コントローラで管理します。

**製品情報**

| 部品番号 (1) | パッケージ | 本体サイズ |
|---|---|---|
| DLPA300 | HTQFP (80) | 14.00mm × 14.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**簡素化されたアプリケーション**

# Table of Contents



## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (October 2021) to Revision A (June 2023) | Page |
|---|---|
| • 新しい DMD 向けに 特長 を更新 | 1 |
| • アプリケーション を更新 | 1 |
| • 新しい DMD 向けに 概要 を更新 | 1 |
| • Added minimum value to $V_{IN}$ in Absolute Maximum Ratings | 6 |
| • Updated $F_{SW}$ in Bias Voltage Boost Converter | 8 |
| • Deleted Discharge time constant in $V_{OFFSET}$ Regulator | 9 |
| • Added Discharge current sink in $V_{OFFSET}$ Regulator | 9 |
| • Updated Overview | 12 |
| • Updated drawing for proper logic polarity in Functional Block Diagram | 13 |
| • Updated switching frequency in Bias Voltage Boost Converter | 14 |
| • Updated Bias Voltage Boost Converter for new DMDs | 14 |
| • Updated $V_{OFFSET}$ Regulator for new DMDs | 15 |
| • Updated Application Information | 17 |
| • Updated Typical Application | 17 |
| • Updated Design Requirements | 18 |
| • Corrected minor typos in Detailed Design Procedure | 19 |

## 5 Pin Configuration and Functions

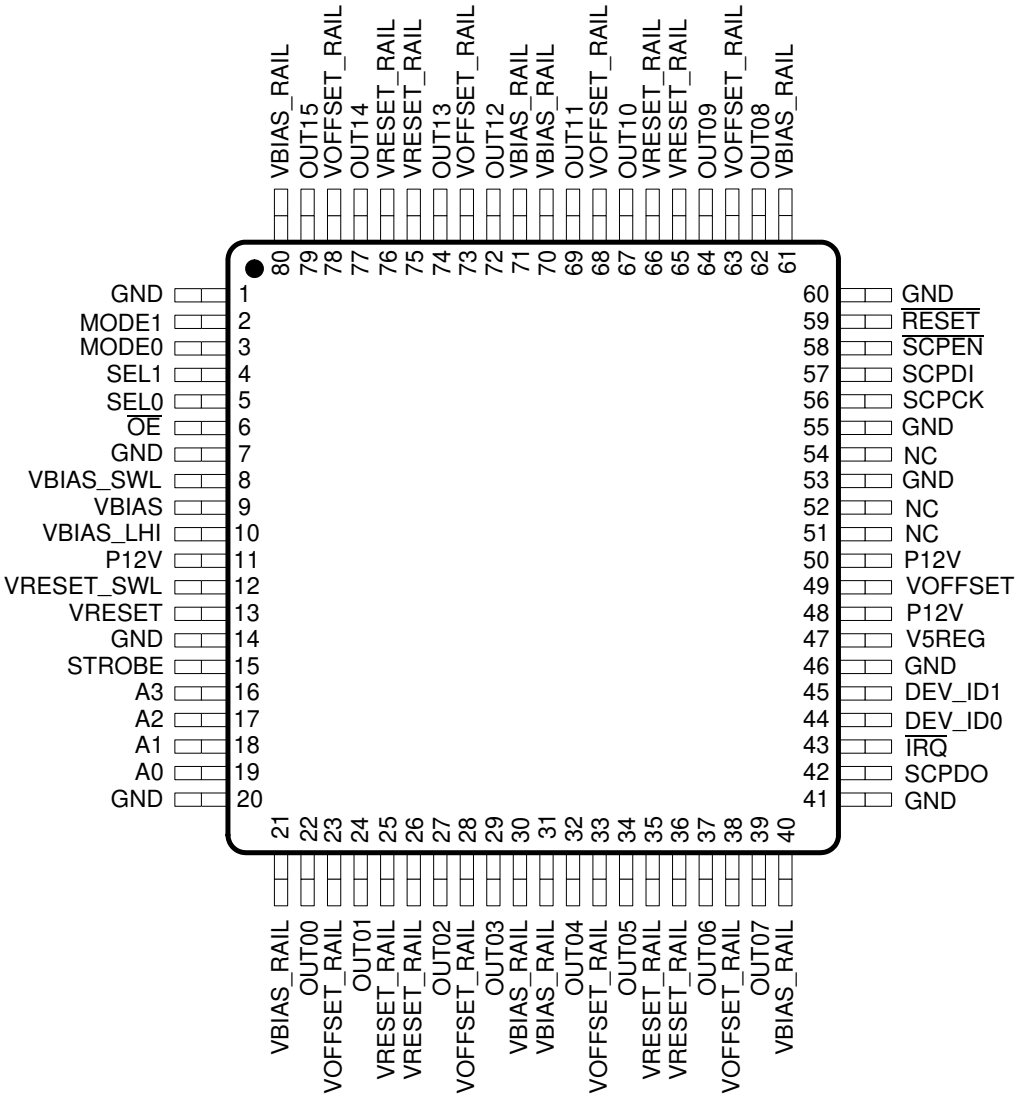



**図 5-1. PFP Package 80-Pin HTQFP Top View**

**表 5-1. Package Pinout**

| PIN | | I/O (INPUT DEFAULT) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT00 | 22 | Output | 16 micromirror clocking waveform outputs (enabled by $\overline{OE}$ = 0) |
| OUT01 | 24 | Output | |
| OUT02 | 27 | Output | |
| OUT03 | 29 | Output | |
| OUT04 | 32 | Output | |
| OUT05 | 34 | Output | |
| OUT06 | 37 | Output | |
| OUT07 | 39 | Output | |
| OUT08 | 62 | Output | |
| OUT09 | 64 | Output | |
| OUT10 | 67 | Output | |
| OUT11 | 69 | Output | |
| OUT12 | 72 | Output | |
| OUT13 | 74 | Output | |
| OUT14 | 77 | Output | |
| OUT15 | 79 | Output | |
| A0 | 19 | Input (pulldown) | Output Address. Used to select which OUTxx pin is active at a given time |
| A1 | 18 | Input (pulldown) | |
| A2 | 17 | Input (pulldown) | |
| A3 | 16 | Input (pulldown) | |
| MODE0 | 3 | Input (pulldown) | Mode Select. Used to determine the operating mode of the DLPA300 |
| MODE1 | 2 | Input (pulldown) | |
| SEL0 | 5 | Input (pulldown) | Output Voltage Select. Used to switch the voltage applied to the addressed OUTxx pin |
| SEL1 | 4 | Input (pulldown) | |
| STROBE | 15 | Input (pulldown) | A rising edge on STROBE latches in the control signals after a tristate delay |
| $\overline{OE}$ | 6 | Input (pullup) | Asynchronous input controls whether the 16 OUTxx pins are active or are in a in high-impedance state.<br>$\overline{OE}$ = 0 : Enabled. $\overline{OE}$ = 1 : High Z |
| $\overline{RESET}$ | 59 | Input (pullup) | Resets the DLPA300 internal logic. Active low. Asynchronous |
| $\overline{SCPEN}$ | 58 | Input (pullup) | Enables serial bus data transfers. Active low |
| SCPDI | 57 | Input (pull down) | Serial bus data input. Clocked in on the falling edge of SCPCK |
| SCPCK | 56 | Input (pull down) | Serial bus clock. Provided by chipset controller |
| SCPDO | 42 | Output | Serial bus data output (open drain). Clocked out on the rising edge of SCPCK.<br>A 1-kΩ pullup resistor to the chip-set controller $V_{DD}$ supply is recommended. |
| $\overline{IRQ}$ | 43 | Output | Interrupt request output to the chipset Controller. Active low.<br>A 1-kΩ pullup resistor to the chip-set controller $V_{DD}$ supply is recommended. |
| DEV_ID1 | 45 | Input (pullup) | Serial bus device address:<br>00 = all; 01 = device 1; 10 = device 2; 11 = device 3 |
| DEV_ID0 | 44 | Input (pullup) | |
| VBIAS | 9 | Output | One of three specialized voltages the DLPA300 generates |
| VBIAS_LHI | 10 | Input | Current limiter output for VBIAS supply (also the VBIAS switching inductor input) |
| VBIAS_SWL | 8 | Input | Connection point for VBIAS supply switching inductor |
| VBIAS_RAIL | 21, 30, 31, 40, 61, 70, 71, 80 | Input | The internally used VBIAS supply rail. Internally isolated from VBIAS |
| VRESET | 13 | No Connect | This pin is unused by the DLPA300. |

**表 5-1. Package Pinout (continued)**

| PIN | | I/O (INPUT DEFAULT) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VRESET_SWL | 12 | No Connect | This pin is unused by the DLPA300. |
| VRESET_RAIL(1) | 25, 26, 35,36, 65, 66, 75, 76 | Input | The internally-used VRESET supply rail. Internally isolated from VRESET. The external VRESET supply is connected to this pin. The package thermal pad is tied to this voltage level.(1) |
| VOFFSET | 49 | Output | One of three specialized voltages the DLPA300 generates |
| VOFFSET_RAIL | 23, 28, 33, 38, 63, 68, 73, 78 | Input | The internally-used VOFFSET supply rail. Internally isolated from VOFFSET |
| GND | 1, 7, 14, 20, 41, 46, 53, 55, 60 | GND | Common ground |
| V5REG | 47 | Output | The 5-V logic supply output |
| P12V | 11, 48, 50 | Input | The main power input to the DLPA300 |
| NC | 51, 52, 54 | No Connect | No connect |

(1) Exposed thermal pad is internally connected to VRESET_RAIL.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **ELECTRICAL** | | | | | |
| P12V | Load supply voltage | | | 14 | V |
| VRESET_SWL | Reset supply switching inductor connection point | (VRESET_SWL-VRESET_RAIL ) | | –1 | V |
| VBIAS_RAIL | Internally-used $V_{BIAS}$ supply rail | (VBIAS_RAIL-VRESET_RAIL) | | 60 | V |
| VOFFSET_RAIL | Internally-used $V_{OFFSET}$ supply rail | (VOFFSET_RAIL-VRESET_RAIL) | | 40.5 | V |
| $V_{IN}$ | Logic inputs | | –0.3 | 7 | V |
| $V_{OUT}$ | Open drain logic outputs | | | 7 | V |
| **ENVIRONMENTAL** | | | | | |
| $T_{J(max)}$ | Maximum junction temperature | | | 125 | °C |
| $T_A$ | Operating temperature | | 0 | 75 | °C |
| $T_{stg}$ | Storage temperature | | –55 | 150 | °C |

(1) Stresses beyond those listed under *セクション 6.1* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM)(1) | ±2000 | V |
| | | Charged device model (CDM)(2) | 800 | |

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

at $T_A$ = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)(2)

| POWER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{P12V1}$ | P12V supply current(1) | Global shadow at 50 kHz, OUT load = 39 Ω and 410 pF, V5REG = 30 mA, $V_{BIAS}$ = 21 V at 5 mA, $V_{OFFSET}$ = 10V at 30 mA | | 200 | | mA |
| $I_{P12V2}$ | | Outputs disabled and no external loads, $V_{BIAS}$ = 21 V, $V_{OFFSET}$ = 4.5 V | | | 22 | mA |
| $T_{JTSDR}$ | Thermal shutdown temperature | With device temperature rising | 145 | 160 | 175 | °C |
| | | Hysteresis | 5 | 10 | 15 | °C |
| | Delta between thermal shutdown and thermal warning | | 5 | 10 | 15 | °C |
| $T_{JTWR}$ | Thermal warning temperature | With device temperature rising | 125 | 140 | 155 | °C |
| | | Hysteresis | 5 | 10 | 15 | °C |

(1) During power up the inrush power supply current can be as high as 1 A for a momentary period of time.
(2) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DLPA300 PFP (HTQFP) 80 PINS | UNIT |
|---|---|---|---|
| $R_{c-j}$ | Thermal resistance | 3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics Control Logic

$T_A$ = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level logic input voltage | | | | 0.8 | V |
| $V_{IH}$ | High-level logic input voltage | | 1.97 | | | V |
| $I_{IH}$ | High-level logic input current | $V_{IN}$ = 5 V, input with pulldown. See terminal functions table. | | 40 | 50 | µA |
| $I_{IL}$ | Low-level logic input current | $V_{IN}$ = 0 V, input with pullup. See terminal functions table. | –50 | –40 | | µA |
| $I_{IH}$ | High-level logic input leakage current | $V_{IN}$ = 0 V, input with pulldown | –1 | | 1 | µA |
| $I_{IL}$ | Low-level logic input leakage current | $V_{IN}$ = 5 V, input with pullup | –1 | | 1 | µA |
| $V_{OL}$ | Open drain logic outputs | I = 4 mA | | | 0.4 | V |
| $I_{OL}$ | Logic output leakage current | V = 3.3 V | | | 1 | µA |

## 6.6 5-V Linear Regulator

$T_A$ = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{5REG}$ | Output voltage | Average voltage, $I_{OUT}$ = 4 mA to 50 mA | | 4.75 | 5 | 5.25 | V |
| $I_{IL}$ | Output current: internal logic | | | 4 | | 20 | mA |
| $I_{IE}$ | Output current: external circuitry | | | 0 | | 30 | mA |
| $I_{CL5}$ | Current limit | | | 80 | | | mA |
| $V_{UV5}$ | Undervoltage threshold | $I_{OUT}$ = 50 mA | V5REG voltage increasing, P12V = 5.4 V | | 4.1 | | V |
| | | | V5REG voltage falling, P12V = 5.2 V | | 3.9 | | |
| $V_{RIP}$ | Output ripple voltage(1) | | | | | 200 | mVpk-pk |
| $V_{OS5}$ | Voltage overshoot at start up | | | | | 2 | %V5REG |
| $t_{ss}$ | Power up | Measured between 10 to 90% of V5REG | | | | 1 | ms |

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

## 6.7 Bias Voltage Boost Converter

$T_A$ = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{RL}$ | Output current: reset outputs | Load = 400pF, 39 Ω, repetition frequency = 50 kHz | 0 | | 18 | mA |
| $I_{QL}$ | Output current: quiescent / drivers | Load = 400 pF, 39 Ω, repetition frequency = 50 kHz | | | 3 | mA |
| $I_{DL}$ | Output current: DMD load | | 0 | | 5 | mA |
| $I_{CLFB}$ | Current limit flag | Corresponding current on output at P12V = 10.8 V | 30 | | | mA |
| $I_{CLB}$ | Current limit | Measured on input | 330 | 376 | 460 | mA |
| $V_{BIAS}$ | Output voltage | | 20.5 | 21 | 21.5 | V |
| $V_{UVB}$ | $V_{BIAS}$ undervoltage threshold | Bias voltage falling | 50 | | 92 | %VBIAS |
| $V_{UVLHI}$ | VBIAS_LHI undervoltage threshold | VBIAS_LHI voltage increasing | | 8 | | V |
| | | VBIAS_LHI voltage falling | | 6.5 | | V |
| $R_{DS}$ | Boost switch $R_{DS(on)}$ | $T_J$ = 25°C | | 2 | | Ω |
| $V_{RIP}$ | Output ripple voltage(1) | | | | 200 | mVpk-pk |
| $F_{SW}$ | Switching frequency | | 1.1 | 1.3 | 1.5 | MHz |
| $V_{OSB}$ | Voltage overshoot at start up | | | | 2 | %VBIAS |
| $t_{ss}$ | Power up | $C_{OUT}$ = 3.3 µF, Measured between 10 to 90% of target $V_{BIAS}$ | | | 1 | ms |
| $t_{dis}$ | Discharge current sink | | 400 | | | mA |

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

## 6.8 Reset Voltage Buck-Boost Converter

This is feature is not used in the DLPA300.

## 6.9 $V_{OFFSET}$ Regulator

$T_A$ = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{RL}$ | Output current: reset outputs | Load = 400 pF, 39 Ω, repetition frequency = 50 kHz | 0 | | 12.2 | mA |
| $I_{QL}$ | Output current: quiescent / drivers | Load = 400 pF, 39 Ω, repetition frequency = 50 kHz | | | 3 | mA |
| $I_{DL}$ | Output current | | 0 | | 30 | mA |
| $I_{CLO}$ | Current limit | | 100 | | | mA |
| $V_{OFFSET}$ | Output Voltage | | 9.75 | 10 | 10.25 | V |
| $V_{UVO}$ | Undervoltage threshold | $V_{OFFSET}$ voltage falling | 50 | | 92 | %VOFFSET |
| $V_{RIP}$ | Output ripple voltage(1) | | | | 100 | mVpk-pk |
| $V_{OSO}$ | Voltage overshoot at start-up | | | | 2 | %VOFFSET |
| $t_{ss}$ | Power up | $C_{OUT}$ = 4.7 µF, Measured between 10 to 90% of target $V_{OFFSET}$ | | | 1 | ms |
| $I_{dis}$ | Discharge current sink | | 400 | | | mA |

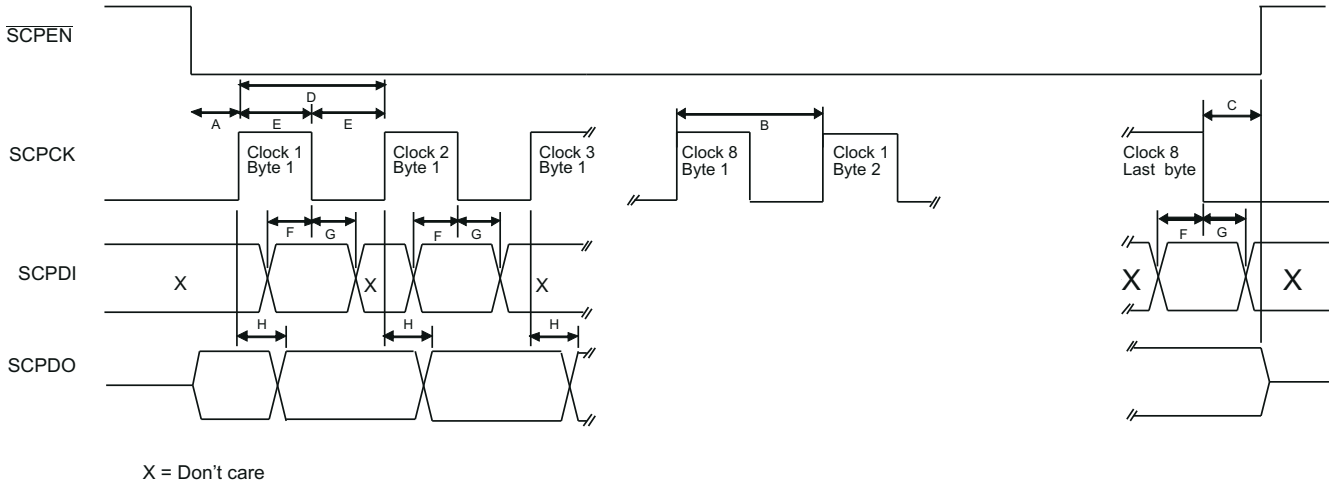
(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

## 6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SERIAL COMMUNICATION PORT INTERFACE | | | | | | |
| A(1) | Setup $\overline{SCPEN}$ low to SCPCK | Reference to rising edge of SCPCK | 360 | | | ns |
| B(1) | Byte to byte delay | Nominally 1 SCPCK cycle, rising edge to rising edge | 1.9 | | | µs |
| C(1) | Setup SCPDI to $\overline{SCPEN}$ high | Last byte to secondary disable | 360 | | | ns |
| D(1) | SCPCK frequency(2) | | 0 | | 526 | kHz |
| | SCPCK period | | 1.9 | 2 | | µs |
| E(1) | SCPCK high or low time | | 300 | | | ns |
| F(1) | SCPDI set-up time | Reference to falling edge of SCPCK | 300 | | | ns |
| G(1) | SCPDI hold time | Reference from falling edge of SCPCK | 300 | | | ns |
| H(1) | SCPDO propagation delay | Reference from rising edge of SCPCK | | | 300 | ns |
| | $\overline{SCPEN}$, SCPCK, SCPDI, $\overline{RESET}$ filter (pulse reject) | | 150 | | | ns |
| **OUTPUT MICROMIRROR CLOCKING PULSES** | | | | | | |
| $F_{PREP}$ | Phased reset repetition frequency each output pin (non-overlapping) | | | | 50 | kHz |
| $F_{GREP}$ | Global reset repetition frequency all output pins | | | | 50 | kHz |
| $I_{RLK}$ | $V_{RESET}$ output leakage current | $\overline{OE}$ = 1, VRESET_RAIL = -28.5V | | -1 | -10 | µA |
| $I_{BLK}$ | $V_{BIAS}$ output leakage current | $\overline{OE}$ = 1, VBIAS_RAIL = 28.5V | | 1 | 10 | µA |
| $I_{OLK}$ | $V_{OFFSET}$ output leakage current | $\overline{OE}$ = 1, VOFFSET_RAIL = 10.25V | | 1 | 10 | µA |
| **OUTPUT MICROMIRROR CLOCKING PULSE CONTROLS** | | | | | | |
| $t_{SPW}$ | STROBE pulse width | | 10 | | | ns |
| $t_{SP}$ | STROBE period | | 20 | | | ns |
| $t_{OHZ}$ | Output time to high impedance | $\overline{OE}$ Pin = High | | | 100 | ns |
| $t_{OEN}$ | Output enable time from high impedance | $\overline{OE}$ Pin = Low | | | 100 | ns |
| $t_{SUS}$ | Set-up time | From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge | 8 | | | ns |
| $t_{HOS}$ | Hold time | From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge | 8 | | | ns |
| $t_{PBR}$ | Propagation time | From STROBE to $V_{BIAS}/V_{RESET}$ edge 50% point. | 80 | | 200 | ns |
| $t_{PRO}$ | | From STROBE to $V_{RESET}/V_{OFFSET}$ edge 50% point. | 80 | | 200 | ns |
| $t_{POB}$ | | From STROBE to $V_{OFFSET}/V_{BIAS}$ edge 50% point. | 80 | | 200 | ns |
| $t_{DEL}$ | Edge-to-edge propagation delta | Maximum difference between the slowest and fastest propagation times for any given reset output. | | | 40 | ns |
| $t_{CHCH}$ | Output channel-to-channel propagation delta | Maximum difference between the slowest and fastest propagation times for any two outputs for any given edge. | | | 20 | ns |

(1) See 図 6-1
(2) There is no minimum speed for the serial port. It can be written to statically for diagnostic purposes.




X = Don't care

**図 6-1. Serial Interface Timing**

# 7 Detailed Description

## 7.1 Overview

The DLPA300 is a micromirror driver for the 9-µm pixel family of DMDs. These include the DLP780NE, DLP800RE. DLP780TE, DLP781NE, DLP781TE, DLP801RE and DLP801XE DMDs. The DLPA300 micromirror driver generates $V_{OFFSET}$ and $V_{BIAS}$ voltages required by the DMD. $V_{RESET}$ for the DMDs is generated by an external voltage regulator. Under the control of the DLPC4430 (or DLPC4420) display controller, the DLPA300 micromirror driver switches these three voltage supplies to control the micromirror reset waveform via the MBRST pins on the DMD.

Reliable function and operation of the DLPA300 micromirror driver require that it is used as part of the family of 9-µm pixel DMD chipsets. For LED and RGB direct laser illumination, the DLPA100 can be replaced by discrete power supply ICs and a power supply sequencer.

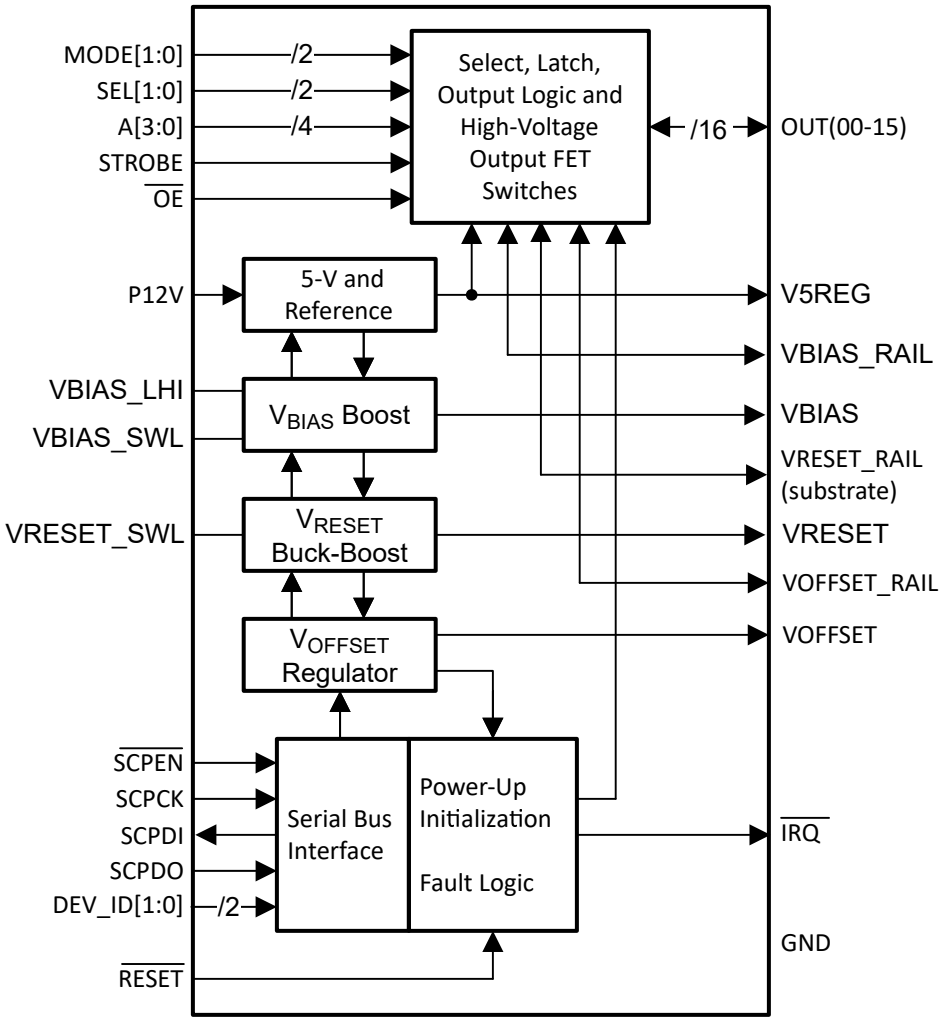
The DLPA300 consists of three functional blocks: a high-voltage power supply function, a DMD micromirror clock generation function, and a serial communication (SCP) function.

The high-voltage power supply function generates two specialized voltage levels: $V_{BIAS}$ (21-V) and $V_{OFFSET}$ (10-V). The exact values are controlled by the DLPC4430 or DLPC4420 display controller. $V_{RESET}$ is generated by external voltage regulator.

The micromirror clock generation function uses the two voltages generated by the high-voltage power supply function and the one generated by the external voltage regulator to create the fifteen micromirror clock pluses (output the OUT[0:14] pins of the DLPA300). OUT15 is unused.

The serial communication function allows the display controller to control the generation of $V_{BIAS}$, $V_{RESET}$, and $V_{OFFSET}$; control the generation of the micromirror clock pulses; and control the general operation of the DLPA300 micromirror driver.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 5-V Linear Regulator

The 5-V linear regulator supplies the 5-V needed for the internal logic of the DLPA300 micromirror driver. It can also provide 5-V, up to 30 mA, for external peripherals.

図 7-1 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA300 modules. See セクション 8.2.2.1 for recommended component values.

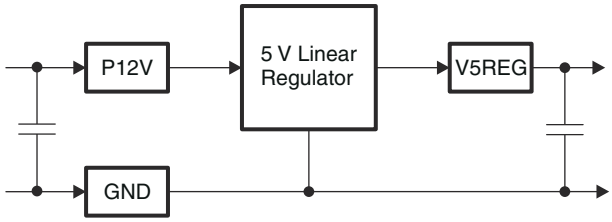



**図 7-1. 5-Volt Linear Regulator Block Diagram**

### 7.3.2 Bias Voltage Boost Converter

The bias voltage converter is a switching supply that operates at 1.3 MHz. The converter supplies the internal bias voltage for the high voltage FET switches. The $V_{BIAS}$ voltage level for the 9-µm pixel family of DMDs is 21V. The $V_{BIAS}$ voltage level is configured by the DLP display controller chip over the serial communication port (SCP). Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage ($V_{UV}$) and current-limit ($C_L$) conditions.

図 7-2 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA300 modules. See セクション 8.2.2.1 for recommended component values.

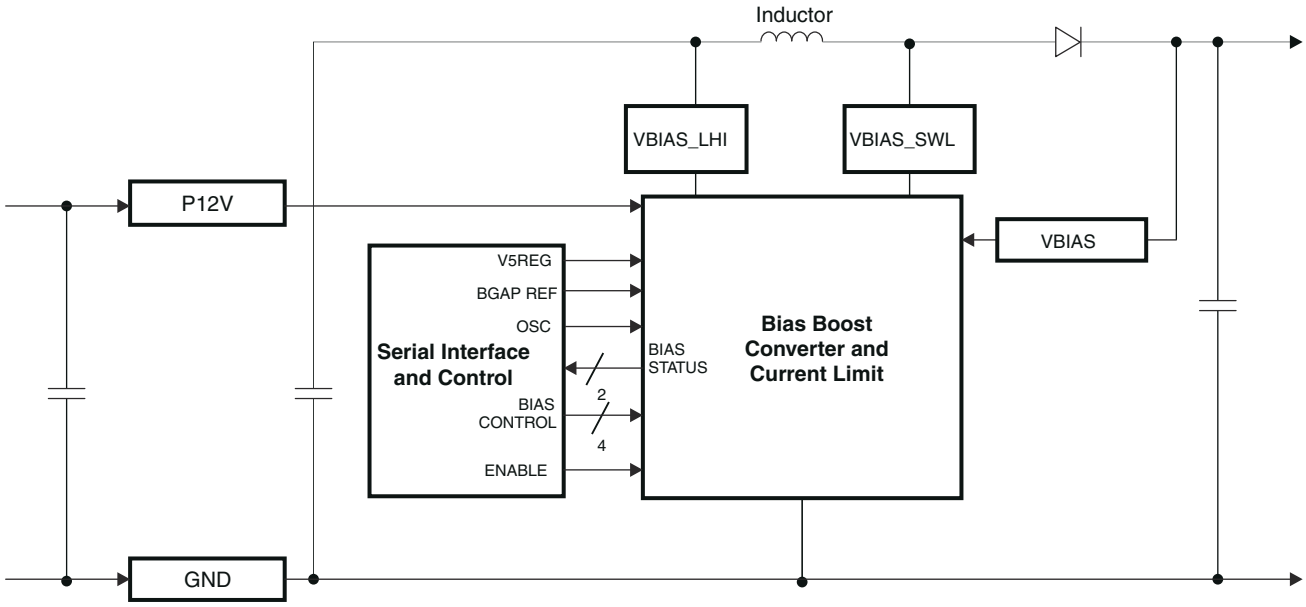



**図 7-2. Bias Voltage Boost Converter Block Diagram**

### 7.3.3 Reset Voltage Buck-Boost Converter

The internal reset voltage buck-boost converter in the DLPA300 is unused. An external voltage regulator is used to generate the –16.5-V for $V_{RESET}$. The output of this regulator is connected to the $V_{RESET\_RAIL}$ pin on the DLPA300 micromirror driver.

The external voltage regulator provide reset voltage level for the high voltage FET switches. The internal reset voltage buck-boost converter is disabled by the DLP display controller over the serial communication port.

### 7.3.4 $V_{OFFSET}$ Regulator

The $V_{OFFSET}$ regulator supplies the internal $V_{OFFSET}$ voltage for the high voltage FET switches. The $V_{OFFSET}$ voltage level for the 9-µm pixel family of DMDs is 10-V during normal operation and 4.5-V during power down. The $V_{OFFSET}$ voltage level is configured by the DLP controller chip over the serial communication port. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for undervoltage ($V_{UV}$) and current-limit ($C_L$) conditions.

図 7-3 shows the block diagram of this module. The input decoupling capacitors are shared with other DLPA300 modules. See セクション 8.2.2.1 for recommended component values.

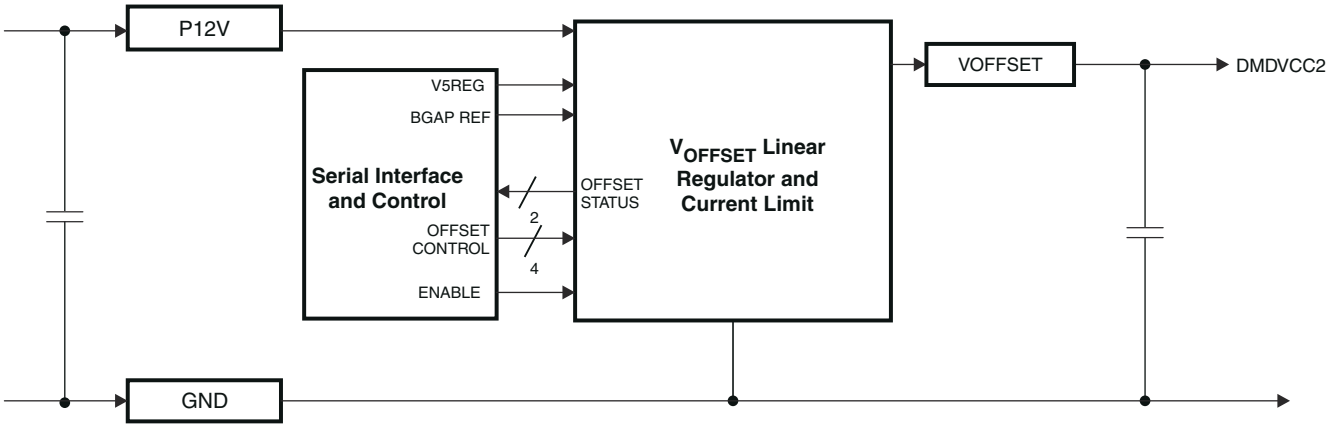



**図 7-3. Offset Voltage Boost Convertor Block Diagram**

### 7.3.5 Serial Communications Port (SCP)

The SCP is a full duplex, synchronous, character-oriented (byte) port that allows exchange of data between the DLPC4430 or DLPC4420 display controller, and the DLPA300 micromirror driver (and other DLP devices). The display controller is the primary on the SCP bus. The DLPA300 micromirror driver is the secondary on the SCP bus.

**表 7-1. Serial Communications Port Signal Definitions**

| SIGNAL | I/O | FROM/TO | TYPE | DESCRIPTION |
|---|---|---|---|---|
| SCPCK | I | SCP bus primary to secondary | LVTTL compatible | SCP bus serial transfer clock. The host processor (primary) generates this clock. |
| $\overline{\text{SCPEN}}$ | I | SCP bus primary to secondary | LVTTL compatible | SCP bus access enable (low true). When high, secondary resets to the idle state, and SCPDO output is tristated. Pulling $\overline{\text{SCPEN}}$ low initiates a read or write access. $\overline{\text{SCPEN}}$ must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull $\overline{\text{SCPEN}}$ high at any point. |
| SCPDI | I | SCP bus primary to secondary | LVTTL compatible | SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK. |
| SCPDO | O | SCP bus secondary to primary | LVTTL, open drain w/tristate | SCP bus serial data output. Data bits must clocked out on the rising edge of SCPCK. A 1-kΩ pullup resistor to the 3.3-V display controller supply is required. |
| $\overline{\text{IRQ}}$ | O | SCP bus secondary to primary | LVTTL, open drain | Not part of the SCP bus definition. Asynchronous interrupt signal from secondary to request service from the primary. A 1-kΩ pullup resistor to the 3.3-V display controller supply is required. |

## 7.4 Device Functional Modes

At power up, the DLPC4430 or DLPC4420 display controller configures the DLPA300 over the SCP bus. There are two device functional modes. When $\overline{\text{OE}}$ is high, OUT[0:14] are tristated. When $\overline{\text{OE}}$ is low, the OUT[0:14] are active under the control of the display controller.

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLP display controller. Typical applications using the DLP780NE, DLP800RE and DLP780TE chipsets include laserTVs, smart projectors, enterprise projectors and digital signage. The DLP781NE, DLP781TE, DLP801RE and DLP801XE are used in higher brightness applications such as ProAV and large venue projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller through the DLPA300. Refer to *Power Supply Recommendations* section in the DLP780NE, DLP780TE, DLP800RE, DLP781NE, DLP781TE, DLP801RE and DLP801XE datasheets for power-up and power-down specifications. To ensure reliable operation, the DLP780NE, DLP800RE, DLP781NE and DLP801RE DMDs must always be used with DLPC4430 display controller, a DLPA100 power management and motor driver and a DLPA300 micromirror driver. The DLP780TE, DLP781Te and DLP801XE DMDs must always be use with the DLPC4420 display controller, the DLPA100 power management and motor driver and a DLPA300 micromirror driver. For LED and RGB direct laser illumination, the DLPA100 power management and motor driver can be replaced with discrete power supplies that are sequenced to meet the display controller power supply sequencing.

## 8.2 Typical Application

The DLPA300 micromirror driver controls the switching of the bias, offset and reset voltage levels on the MBRST pins to assure correct DMD operation. It is a controlled by a DLP display controller which synchronizes the display data sent to the DMD with the correct sequencing of the bias, offset and reset voltage levels by the DLPA300 micromirror driver. The typical application shown in 図 8-1 is a Full-HD display using the DLP780NE chipset. The application is the same for the DLP800RE, DLP781NE or DLP801RE/DLPC4430 chipsets and the DLP780TE, DLP781TE or DLP801XE/dual-DLPC4420 chipsets. The DLPA300 micromirror driver creates $V_{BIAS}$ and $V_{OFFSET}$ with internal voltage regulators. $V_{RESET}$ is created by an external regulator. These voltages are switched by the DLPA300 micromirror driver on the OUT[0:14] pins which are connected to the MBRST pins on the DMD.

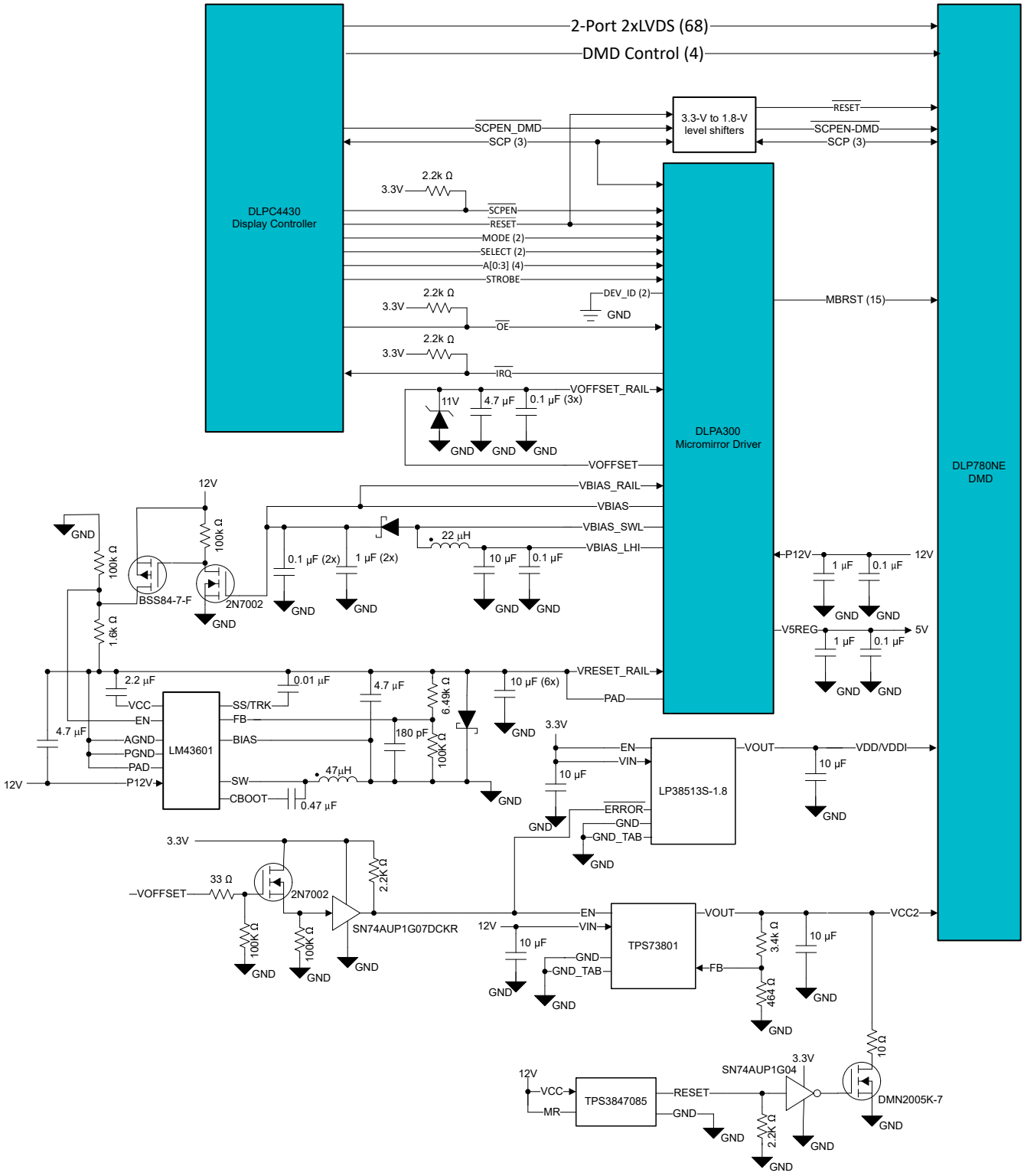



**図 8-1. DLPA300 Typical Application**

### 8.2.1 Design Requirements

For the correct operation of a display system based on the 9-µm pixel family of DMDs, the DLPA300 micromirror driver must be controlled by the DLPC4420 or DLPC4430 display controller. The embedded software in the DLPC4430 or DLPC4420 display controller coordinates the video data to the DMD and the bias, offset and reset

waveforms created by the DLPA300 micromirror driver that are input to the MBRST pins on the DMD. This results in the highest possible image quality and system efficiency.

The key design requirements are power supply sequencing for power up and power down. The 9-µm family of DMDs require that the VCC2 supply be turned on after the 1.8-V supply is full on and stable. Similarly, on power down, the DMDs require that the VCC2 supply be full off before the 1.8-V supply is begins its power off ramp.

The DLPA300 micromirror driver imparts one power supply sequencing constraint. Because $V_{RESET}$ is generated by an external supply, the DLPC4430 display controller cannot control this supply directly by software. Therefore, it is necessary to use the $V_{BIAS}$ supply to control the power up and power down of the external $V_{RESET}$ power supply.

These power supply sequencing requirements necessitate external circuitry to control the $V_{RESET}$ and VCC2 power supply sequencing, as seen in 図 8-1.

### 8.2.2 Detailed Design Procedure

The DLPC4430 or DLPC4420 display controller configures the $V_{BIAS}$ and $V_{OFFSET}$ voltage regulators in the DLPA300 micromirror driver through the SCP bus. $V_{BIAS}$ is then used to generate the enable signal for the $V_{RESET}$ external voltage regulator, LM43601 step-down voltage converter. When the $V_{BIAS}$ is enabled, it turns on the two-transistor buffer amplifier. The 2N7002 and BSS84-7-F FETs isolate $V_{BIAS}$ from the $V_{RESET\_RAIL}$ and shift the voltage reference to $V_{RESET\_RAIL}$.

The thermal pad on the DLPA300 micromirror controller and the LM43601 step-down voltage converter are electrically connected to the $V_{RESET\_RAIL}$. Furthermore, the AGND and PGND pins on the LM43601 step-down voltage converter are also connected to the $V_{RESET\_RAIL}$. Therefore, the logic levels and analog voltage levels for LM43601 step-down voltage converter are referenced to the –16.5-V $V_{RESET\_RAIL}$.

The LM43601 data sheet provides details for the component selection for the components in the voltage regulator circuit connected to the $V_{RESET\_RAIL}$. The output of the regulator is set to the VRESET value of –16.5 V. The selection of the resistors in the resistor divider sets the output voltages, 6.49 kΩ and 100 kΩ.

The DLP780NE power sequencing requires that the VCC2 power supply ramps up after the 1.8-V supply is powered on and stable, and $V_{OFFSET}$ is powered up and stable. The two conditions are met by the wired-or of the $\overline{\text{ERROR}}$ signal from the LP38513-1.8 ultra-low dropout linear regulator and an enable signal generated from $V_{OFFSET}$. The 2N7002 enhancement mode FET acts as an inverter and level shifter from $V_{OFFSET}$ to a 3.3-V logic level.

In the event of a power supply failure (such as a pull-the-plug event), VCC2 must be driven low before the 1.8-V supply starts to drop voltage. To achieve this, the TPS3847 12-V voltage monitor triggers a shunt-to-ground power FET to pull VCC2 to ground.

#### *8.2.2.1 Component Selection Guidelines*

**表 8-1. 5-V Regulator**

| COMPONENT | VALUE | TYPE OR PART NUMBER | CONNECTION 1 | CONNECTION 2 |
|---|---|---|---|---|
| P12V filter capacitor | 10 to 33 µF, 20 VDC, 1Ω max ESR | Tantalum or ceramic | Positive Terminal: P12V, pin 11 (locate near pin 11) | Negative Terminal: Ground |
| P12V bypass capacitor | 0.1 µF, 50 VDC, 0.1Ω max ESR | Ceramic | P12V, pin 11 (locate near pin 11) | Ground |
| V5REG filter capacitor | 0.1(1) to 1.0 µF, 10 VDC, 2.5Ω max ESR | Tantalum or ceramic | Positive Terminal: V5REG, pin 47 (locate near pin 47) | Negative Terminal: Ground |
| V5REG bypass capacitor | 0.1 µF(1), 16 VDC, 0.1Ω max ESR | Ceramic | V5REG, pin 47 (locate near pin 47) | Ground |

(1) To ensure stability of the linear regulator, use a capacitance with a value not less than 0.1 µF.

**表 8-2. Bias Voltage Boost Converter**

| COMPONENT | VALUE | TYPE OR PART NUMBER | CONNECTION 1 | CONNECTION 2 |
|---|---|---|---|---|
| LHI filter capacitor | 10 µF, 20 VDC, 1-Ω max ESR | Tantalum or ceramic | Positive Terminal: VBIAS_LHI, pin 10 (locate near pin 10) | Negative Terminal: Ground |
| LHI bypass capacitor | 0.1 µF, 50 VDC, 0.1-Ω max ESR | Ceramic | VBIAS_LHI, pin 10 (locate near pin 10) | Ground |
| VBIAS_RAIL filter capacitor (2 required) | 1 µF, 50 VDC, 0.1-Ω max ESR | Ceramic | VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71) | Ground |
| VBIAS_RAIL bypass capacitors (2 required) | 0.1 µF, 50 VDC, 0.1Ω max ESR | Ceramic | VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71) | Ground |
| Inductor | 22 µH, 0.5 A, 160 mΩ ESR | Coil Craft DT1608C-223 (or equivalent) | VBIAS_LHI, pin 10 | VBIAS_SWL, pin 8 |
| Schottky diode | 0.5 A, 40 V (minimum) | OnSemi MBR0540T1G or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent) | Anode: VBIAS_SWL, pin 8 | Cathode: VBIAS, pin 9 |

**表 8-3. Offset Voltage Regulator**

| COMPONENT | VALUE | TYPE OR PART NUMBER | CONNECTION 1 | CONNECTION 2 |
|---|---|---|---|---|
| VOFFSET filter capacitors | 1(1) to 4.7(2) µF, 35 VDC, 1Ω max ESR | Tantalum or ceramic | Positive Terminal: VOFFSET, pin 49 (1st Cap near pin 49) Positive Terminal: DMDVCC2 pins ( 2nd Cap at DMD) | Negative Terminal: Ground at DLPA300 Negative Terminal: VSS (Ground) at DMD |
| VOFFSET bypass capacitors (3 required) | 0.1 µF, 50 VDC, 0.1Ω max ESR | Ceramic | VOFFSET, pin 49 (locate 1 near pin 49) | Ground at DLPA300 Ground at DMD |
| Zener Diode | 11V 3W | Micro Commercial Components 3SMBJ5926B-TP or equivalent | VOFFSET | Ground |

(1) To ensure stability of the linear regulator, the absolute minimum output capacitance must not be less than 1.0 µF.
(2) Recommended value is 3.3 µF each. Different values are acceptable, provided that the sum of the two is 6.8 µF maximum.

**表 8-4. Pullup Resistors**

| COMPONENT | VALUE (kΩ) | TYPE OR PART NUMBER | CONNECTION 1 | CONNECTION 2 |
|---|---|---|---|---|
| Resistor | 2.2 | | SCPDO, pin 42 | Chipset controller 3.3-V $V_{DD}$ |
| Resistor | 2.2 | | $\overline{IRQ}$, pin 43 | Chipset Controller 3.3-V $V_{DD}$ |
| Resistor (optional) | 2.2 | | $\overline{OE}$, pin 6 | Chipset Controller 3.3-V $V_{DD}$ |

### 8.2.3 Application Curves

The power supply sequencing for $V_{BIAS}$, $V_{OFFSET}$ and $V_{RESET}$ are shown in 図 8-2 and 図 8-3. On power-up, the turn on of VBIAS enables the external VRESET voltage regulator. In power-down, when VBIAS powers off, it disables the VRESET regulator, which slowly decays to ground.

The power sequencing for VCC2 voltage regulator is shown in 図 8-4 and 図 8-5. The power up of $V_{OFFSET}$ enables the turn on of the VCC2 voltage regulator. As seen in the zoom out of 図 8-4, the 1.8-V supply is already on and stable. Similarly, the power down of $V_{OFFSET}$ disables the VCC2 voltage regulator. The 1.8-V supply powers down after both $V_{OFFSET}$ and VCC2 are powered down, as seen in the zoom out of 図 8-5.

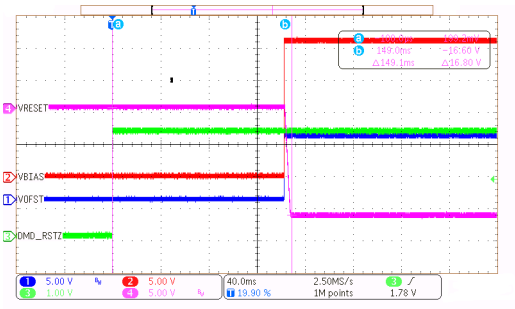



図 8-2. High Voltage Power-Up Sequence

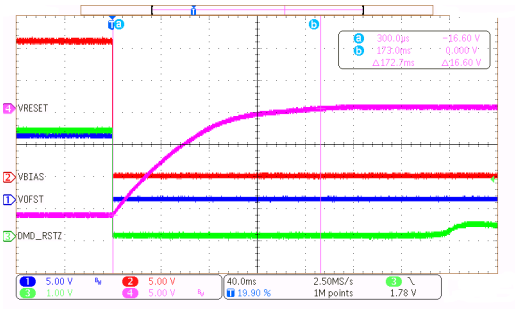



図 8-3. High Voltage Power-Down Sequence

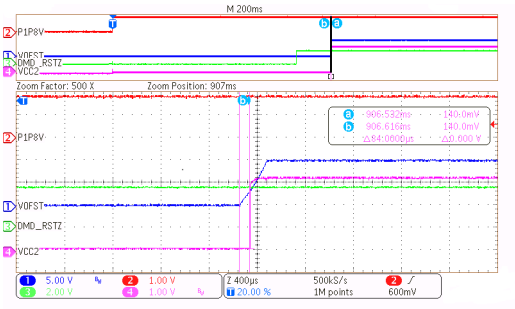



図 8-4. VCC2 Power-Up Sequence

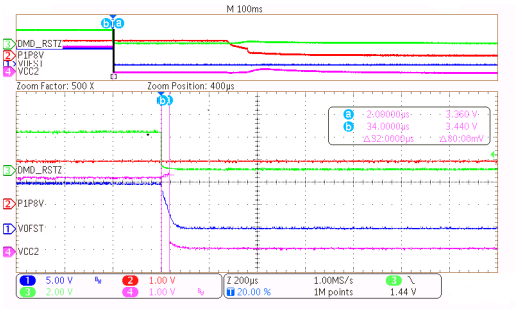



図 8-5. VCC2 Power-Down Sequence

# 9 Power Supply Recommendations

## 9.1 Power Supply Rail Guidelines

表 8-1 through 表 8-4 provides discrete component selection guidelines.

- Ensure that the P12V filter and bypass capacitors are distributed and connected to pin 11 and pin 48 and pin 50. Place these capacitors as close to their respective pins as possible and if necessary, place on the bottom layer.
- The V5REG filter and bypass capacitors must be placed near and connected to pin 47.
- It is best to route the VBIAS_RAIL etch runs in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. Ensure that the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Locate the bypass capacitors near and connected to pin 30 and pin 71 to provide bypassing on both sides.
- The VBIAS_LHI filter and bypass capacitors must be placed near and connected to pin 10.
- The VBIAS filter and bypass capacitors must be placed near and connected to pin 9.
- VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS_RAIL at or between pins 21 and 80.
- Route the VRESET_RAIL etch runs in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Bypass capacitors must be placed near and connected to pins 35 and 66 to provide bypassing on both sides.
- The VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-Ω resistor) to VRESET_RAIL at or between pin 25 and pin 76.
- Route the VOFFSET_RAIL etch runs in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Place the bypass capacitors near and connected to pin 28 and pin 73 to provide bypassing on both sides.
- The VOFFSET filter and bypass capacitors must be placed near and connected to pin 49.
- VOFFSET pin 49 must also be connected (optionally with a 0-Ω resistor) to VOFFSET_RAIL at or between pin 38 and pin 63.

注

Aluminum electrolytic capacitors may not be suitable for the DLPA300 application. At the switching frequencies used in the DLPA300 (up to 1.5 MHz), aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails, which could cause the device to shut down or perform in an unreliable manner.

# 10 Layout

## 10.1 Layout Guidelines

> 注意
>
> Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DLPA300.

> 注意
>
> Thermal pads must be tied to VRESET_RAIL. Do not connect to ground.

Provide suitable Kelvin connections for the switching regulator feedback pins: $V_{BIAS}$ (pin 9) and $V_{RESET}$ (pin 13).

Make the PCB traces that connect the switching devices: VBIAS_SWL (pin 8) and VRESET_SWL (pin 12) as short and wide as possible to minimize leakage inductances. Make the PCB traces that connect the switching converter components (inductors, flywheel diodes and filtering capacitors) as short and wide as possible. Ensure that the electrical loops that these components form are as small and compact as possible, with the ground referenced components forming a star connection.

Due to the fast switching transitions appearing on the sixteen reset OUTx pins, it is recommended to keep these traces as short as possible. Also, to minimize potential cross-talk between outputs, it is advisable to maintain as much clearance between each of the output traces.

### 10.1.1 Grounding Guidelines

Ensure that the PWB has an internal ground plane that extends under the DLPA300. All nine ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

## 10.2 Thermal Considerations

Thermally bond or solder the DLPA300 package to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 mm × 10 mm centered under the device. The metal bottom of the package is tied internally to the substrate at the VRESET_RAIL voltage level. Therefore, the thermal pad on the board must be isolated from any other extraneous circuit or ground and no circuit vias are allowed inside the pad area. Thermal pads are required on both sides of the PWB. Connect the thermal pads together through an array of 5 × 5 thermal vias, 0.5 mm in diameter.

**Thermal pads and the thermal vias are connected to VRESET_RAIL and must be isolated from ground, or any other circuit.**

Locate an internal P12V plane directly underneath the top layer and have an isolated area under the DLPA300. This isolated area must be a minimum of 20 $cm^2$ and connect to the thermal pad of the DLPA300 through the thermal vias. The potential of the isolated area is also at VRESET_RAIL. The internal ground plane must extend under the DLPA300 to help carry the heat away. Please refer to the PowerPAD Thermally Enhanced Package application report (SLMA002) for details on thermally efficient package design considerations.

Be careful to place the DLPA300 device away from local PWB hotspots. Heat generated from adjacent components may impact the DLPA300 thermal characteristics.

# 11 Device and Documentation Support

## 11.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

## 11.2 Device Support

### 11.2.1 Device Nomenclature

The device marking consists of the fields shown in 図 11-1.


**PART MARKING CODES**

LLLLLLLL = Lot trace code or date code

e4 = Pb-Free NiPdAu termial finish

● = Pin 1 designator

**図 11-1. Device Marking (Device Top View)**

## 11.3 Documentation Support

### 11.3.1 Related Documentation

The following documents contain additional information related to the chipsets supported by the DLPA300 micromirror driver and used in the typical application.

- DLP780NE data sheet
- DLP800RE data sheet
- DLP780TE data sheet
- DLP781NE data sheet
- DLP801RE data sheet
- DLP781TE data sheet
- DLP801XE data sheet
- DLPC4430 data sheet
- DLPC4420 data sheet
- DLPA100 data sheet
- LM43601 data sheet
- LP38513S data sheet
- TPS73801 data sheet
- TPS3847085 data sheet

## 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 11.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 11.7 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DLPA300PFP | ACTIVE | HTQFP | PFP | 80 | 119 | TBD | Call TI | Call TI | 0 to 70 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

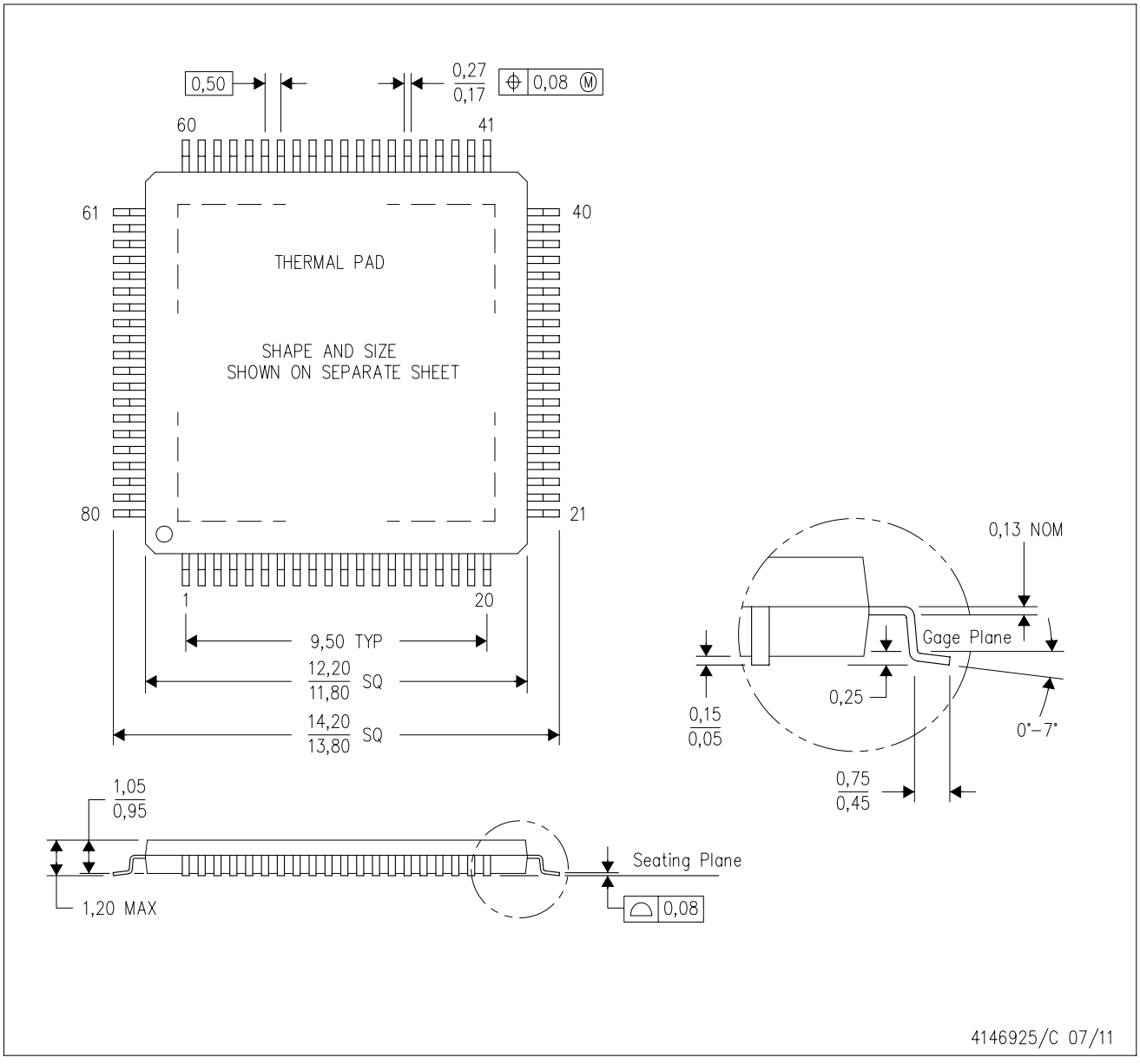
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

**PowerPAD is a trademark of Texas Instruments.**

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265