

# DRV8234 2A ブラシ付き DC モータドライバ、リップルカウント、ストール検出、および速度レギュレーション付き

## 1 特長

- N チャンネル、H ブリッジ、ブラシ付き DC モータードライバ
- 動作電源電圧範囲：4.5V ~ 38V
- 以下の用途のリップルカウント機能：
  - オンチップの速度および位置検出
  - 電圧および速度レギュレーションを内蔵
- ソフトスタートおよびストップ機能による突入電流からの保護
- 600mΩ の  $R_{DS(on)}$  (ハイサイド + ローサイド)
- 高い出力電流能力：3.7A ピーク、2A RMS
- I<sup>2</sup>C 制御インターフェイス搭載 PWM
  - I<sup>2</sup>C レジスタでの構成と診断
  - マルチフォロア動作のサポート
  - 標準およびファースト I<sup>2</sup>C モードをサポート
- 3.3V と 5V のロジック入力電圧をサポート
- 電流センスおよび電流レギュレーション機能を内蔵
- アナログ電流センス出力 (I<sub>PROPI</sub>)
- 100% デューティ サイクルの内部チャージポンプ
- 低消費電力のスリープモードによる長いバッテリー寿命
  - 1μA 未満の最大スリープ電流
- 小さなパッケージと占有面積
  - PowerPAD™ 付き 16 ピン WQFN、3 × 3mm
- 保護機能内蔵
  - VM 低電圧誤動作防止 (UVLO)
  - 過電流保護 (OCP)
  - サーマルシャットダウン (TSD)
  - ストール検出
  - 過電圧保護 (OVP)

## 2 アプリケーション

- プリンタ
- ロボット掃除機
- 洗濯機、乾燥機
- コーヒーメーカー
- POS プリンタ
- 電動病院用ベッド / ベッド制御
- フィットネス機器

## 3 概要

DRV8234 は、リップルカウントによる速度 / 位置検出機能に加えて、モータ速度 / 電圧レギュレーション、ストール検出、電流センス出力、電流レギュレーション、保護回路を内蔵した高性能統合型 H ブリッジモータドライバです。

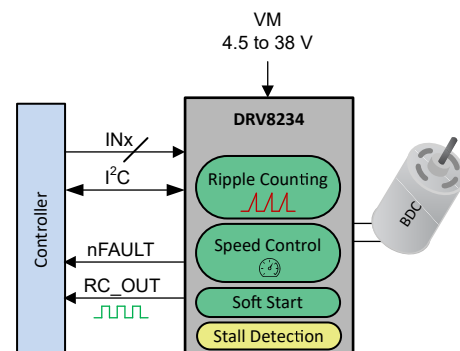
内蔵のリップルカウント アルゴリズムは、モータ電流のリップル数をカウントしてモータの相対位置と速度を判定するため、エンコーダ、ホールセンサ、光学センサは潜在的に不要です。これにより、基板面積と設計の複雑さが低減し、システム全体のコストが削減されます。内蔵の速度レギュレーション機能により、入力電源電圧が変化してもモータ速度が一定に保たれるため、消費電流が最小限に抑えられ、長期的に電力が節約されます。これは、さまざまな負荷条件を持つアプリケーションや、入力電圧が一定ではない操作に対してバッテリー電源に依存するアプリケーションで重要です。ソフトスタートおよびストップにより、制御されたターンオンおよびターンオフ時間が可能になり、大きな突入電流を低減してモータ巻線を損傷から保護することで、システムの信頼性と耐用期間が向上します。

内部カレントミラーは、電流センスとレギュレーションを実装しています。そのため、大電力シャント抵抗を使う必要がなく、基板面積を節約しシステムコストを低減できます。I<sub>PROPI</sub> 電流センス出力を使うと、マイコンはモータのストールまたは負荷条件の変化を検出できます。VREF ピンを使うことで、起動および高負荷イベント中もマイコンを使わずにモータ電流をレギュレーションできます。デバイスは、センサレスモータストール検出とマイコンへのレポートをサポートしています。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
DRV8234	WQFN (16)	3.00mm × 3.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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## 4 Device Comparison

表 4-1. Device Comparison Table

Part Number	Package	Supply VM (V)	$R_{DS(ON)}$ (m $\Omega$ )	Current Capacity (RMS)	Ripple Counting	Speed Regulation	Stall Detection	Package Size
DRV8214	RTE	1.65 to 11	240	2 A	Yes	Yes	Yes	3 mm × 3 mm
DRV8234	RTE	4.5 to 38	600	2 A	Yes	Yes	Yes	3 mm × 3 mm
DRV8215	RTE	1.65 to 11	240	2 A	No	Yes	Yes	3 mm × 3 mm
DRV8235	RTE	4.5 to 38	600	2 A	No	Yes	Yes	3 mm × 3 mm
<a href="#">DRV8213</a>	RTE	1.65 to 11	240	2 A	No	No	Yes	3 mm × 3 mm
<a href="#">DRV8213</a>	DSG	1.65 to 11	240	2 A	No	No	No	2 mm × 2 mm

## 5 Pin Configuration and Functions

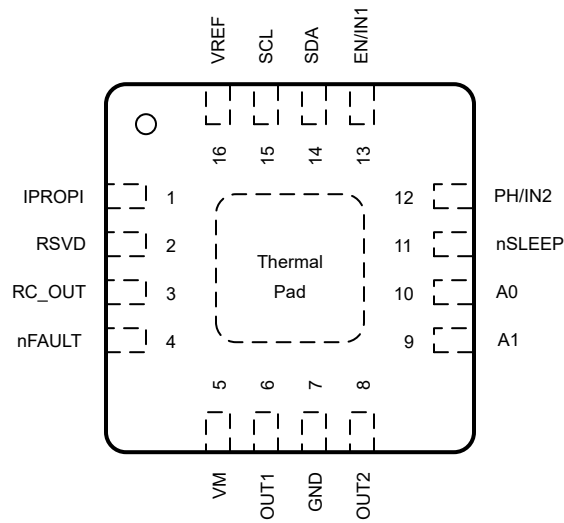


図 5-1. RTE Package 16-Pin WQFN Top View

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	RTE		
IPROPI	1	PWR	Analog current output proportional to load current. Connect a resistor from IPROPI to ground.
RSVD	2	—	Reserved. Leave this pin unconnected.
RC_OUT	3	OD	Output of Ripple Counting algorithm. Can be programmed by I <sup>2</sup> C to output pulse train or logic level signal.
nFAULT	4	OD	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation.
VM	5	PWR	Motor power supply. Bypass this pin to the GND pin with a 0.1- $\mu$ F ceramic capacitor as well as sufficient bulk capacitance rated for VM.
OUT1	6	O	H-bridge output. Connect directly to the motor.
GND	7	PWR	Device ground. Connect to system ground.
OUT2	8	O	H-bridge output. Connect directly to the motor.
A1	9	I	I <sup>2</sup> C base address select pin. Tri-level input.
A0	10	I	I <sup>2</sup> C base address select pin. Tri-level input.
nSLEEP	11	I	Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. Internal pulldown resistor.
PH/IN2	12	I	Controls the H-bridge output. Has internal pulldown.
EN/IN1	13	I	Controls the H-bridge output. Has internal pulldown.
SDA	14	I	I <sup>2</sup> C data signal. The SDA pin requires a pullup resistor.
SCL	15	I	I <sup>2</sup> C clock signal.
VREF	16	I	Analog input to set current regulation and stall detection level.
PAD	—	—	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

(1) I = Input, O = Output, PWR = Power, OD = Open-Drain Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	40	V
Power supply transient voltage ramp	VM	0	2	V/μs
Logic pin voltage	IN1, IN2, A1, A0, SDA, SCL, nSLEEP	-0.3	5.75	V
Open-drain output pin voltage	nFAULT, RC_OUT	-0.3	5.75	V
Proportional current output pin voltage, VM ≥ 5.45 V	IPROPI	-0.3	5.75	V
Proportional current output pin voltage, VM < 5.45 V		-0.3	V <sub>VM</sub> + 0.3	V
Reference input pin voltage	VREF	0.3	5.75	V
Output pin voltage	OUTx	-V <sub>SD</sub>	V <sub>VM</sub> +V <sub>SD</sub>	V
Output current	OUTx	Internally Limited	Internally Limited	A
Ambient temperature, T <sub>A</sub>		-40	125	°C
Junction temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 500 V may actually have higher performance.

### 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>VM</sub>	Power supply voltage	VM	4.5		38	V
V <sub>IN</sub>	Logic input voltage	IN1, IN2, A1, A0, SDA, SCL, nSLEEP	0		5.5	V
f <sub>PWM</sub>	PWM frequency	INx	0		200	kHz
V <sub>OD</sub>	Open drain pullup voltage	nFAULT, RC_OUT	0		5.5	V
I <sub>OD</sub>	Open drain output current	nFAULT, RC_OUT	0		5	mA
I <sub>OUT</sub> <sup>(1)</sup>	Peak output current	OUTx	0		3.7	A
I <sub>IPROPI</sub>	Current sense output current	IPROPI	0		3	mA
V <sub>VREF</sub>	Current limit reference voltage	VREF	0		3.3	V
T <sub>A</sub>	Operating ambient temperature		-40		125	°C
T <sub>J</sub>	Operating junction temperature		-40		150	°C

- (1) Power dissipation and thermal limits must be observed

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DEVICE	UNIT
		RTE (WQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	47.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	48.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

4.5 V ≤ V<sub>VM</sub> ≤ 38 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical values are at T<sub>J</sub> = 27°C, V<sub>VM</sub> = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES (VM)</b>						
I <sub>VMQ</sub>	VM sleep mode current	nSLEEP = 0 V, V <sub>VM</sub> = 24 V, T <sub>J</sub> = 27°C		0.1	1	μA
I <sub>VM</sub>	VM active mode current	nSLEEP = 3.3 V, IN1 = 3.3 V, IN2 = 0 V, V <sub>VM</sub> = 24 V		3.5	4	mA
t <sub>WAKE</sub>	Turnon time	nSLEEP = 1 to I <sup>2</sup> C ready			410	μs
<b>LOGIC-LEVEL INPUTS (IN1, IN2, SDA, SCL, nSLEEP)</b>						
V <sub>IL</sub>	Input logic low voltage		0		0.5	V
V <sub>IH</sub>	Input logic high voltage		1.5		5.5	V
V <sub>HYS</sub>	Input hysteresis			160		mV
V <sub>HYS</sub>	Input hysteresis	nSLEEP pin		60		
I <sub>IL</sub>	Input logic low current	V <sub>I</sub> = 0 V	-1		1	μA
I <sub>IH</sub>	Input logic high current	V <sub>I</sub> = 5 V		33	100	μA
R <sub>PD</sub>	Input pulldown resistance, INx	To GND		100		kΩ
t <sub>DEGLITCH</sub>	Input logic deglitch, INx			50		ns
<b>TRI-LEVEL INPUTS (A1, A0)</b>						
V <sub>TIL</sub>	Tri-level input logic low voltage		0		0.6	V
V <sub>TIHZ</sub>	Tri-level input Hi-Z voltage		1.8	2	2.2	V
V <sub>TIH</sub>	Tri-level input logic high voltage		2.7		5.5	V
R <sub>TPD</sub>	Tri-level pulldown resistance	to GND		200		kΩ
I <sub>TPU</sub>	Tri-level pullup current	to 3.3 V		10		μA
<b>OPEN-DRAIN OUTPUTS (nFAULT, RC_OUT, SDA)</b>						
V <sub>OL</sub>	Output logic low voltage	I <sub>OD</sub> = 5 mA			0.3	V
I <sub>OZ</sub>	Output logic high current	V <sub>OD</sub> = 3.3 V	-1		1	μA
t <sub>PW_RC</sub>	RC_OUT pulse width		30	50	70	μs
t <sub>PW_nFAULT</sub>	nFAULT low pulse width	RC Count overflow, RC_REP = 11b	30	50	70	μs
C <sub>B</sub>	SDA capacitive load for each bus line				400	pF
<b>DRIVER OUTPUTS (OUTx)</b>						
R <sub>DS(ON)_HS</sub>	High-side MOSFET on resistance	I <sub>OUTx</sub> = 1 A; T <sub>J</sub> = 25 °C		300	360	mΩ
R <sub>DS(ON)_HS</sub>	High-side MOSFET on resistance	I <sub>OUTx</sub> = 1 A; T <sub>J</sub> = 125 °C		450	540	mΩ
R <sub>DS(ON)_HS</sub>	High-side MOSFET on resistance	I <sub>OUTx</sub> = 1 A; T <sub>J</sub> = 150 °C		500	600	mΩ
R <sub>DS(ON)_LS</sub>	Low-side MOSFET on resistance	I <sub>OUTx</sub> = -1 A; T <sub>J</sub> = 25 °C		300	360	mΩ

4.5 V ≤ V<sub>VM</sub> ≤ 38 V, -40°C ≤ T<sub>J</sub> ≤ 150°C (unless otherwise noted). Typical values are at T<sub>J</sub> = 27°C, V<sub>VM</sub> = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DS(ON)_LS</sub>	Low-side MOSFET on resistance	I <sub>OUTx</sub> = -1 A; T <sub>J</sub> = 125 °C		450	540	mΩ
R <sub>DS(ON)_LS</sub>	Low-side MOSFET on resistance	I <sub>OUTx</sub> = -1 A; T <sub>J</sub> = 150 °C		500	600	mΩ
V <sub>SD</sub>	Body diode forward voltage	I <sub>OUTx</sub> = -1 A		0.8		V
t <sub>RISE</sub>	Output rise time	V <sub>OUTx</sub> rising from 10% to 90% of V <sub>VM</sub>		200		ns
t <sub>FALL</sub>	Output fall time	V <sub>OUTx</sub> falling from 90% to 10% of V <sub>VM</sub>		140		ns
t <sub>PD</sub>	Input to output propagation delay	Input to OUTx		650		ns
t <sub>DEAD</sub>	Output dead time			200		ns
<b>CURRENT SENSE AND REGULATION (IPROPI, VREF)</b>						
V <sub>REF_INT</sub>	Internal reference voltage	INT_VREF = 1b	2.88	3	3.12	V
A <sub>IPROPI</sub>	Current scaling factor			1500		μA/A
A <sub>ERR</sub>	Current mirror total error	I <sub>OUT</sub> = 0.1 A, V <sub>VM</sub> ≥ 5.5 V	-10		10	%
A <sub>ERR</sub>	Current mirror total error	0.15 A ≤ I <sub>OUT</sub> < 0.5 A, V <sub>VM</sub> ≥ 5.5 V	-7		7	%
A <sub>ERR</sub>	Current mirror total error	I <sub>OUT</sub> ≥ 0.5 A, V <sub>VM</sub> ≥ 5.5 V	-5		5	%
t <sub>OFF</sub>	Current regulation off time			20		μs
t <sub>BLANK</sub>	Current sense blanking time	TBLANK = 0b		1.8		μs
t <sub>BLANK</sub>	Current sense blanking time	TBLANK = 1b		1		μs
t <sub>DEG</sub>	Current regulation and stall detection deglitch time	TDEG = 0b		2		μs
t <sub>DEG</sub>	Current regulation and stall detection deglitch time	TDEG = 1b		1		μs
t <sub>INRUSH</sub>	Inrush time blanking for stall detection		5		6716	ms
<b>Voltage regulation</b>						
ΔV <sub>LINE</sub>	Line regulation	5.5 V ≤ V <sub>VM</sub> ≤ 38 V, V <sub>OUT</sub> = 5 V, I <sub>OUT</sub> = 2 A		±2%		
ΔV <sub>LOAD</sub>	Load regulation	V <sub>VM</sub> = 24 V, V <sub>OUT</sub> = 5 V, I <sub>OUT</sub> = 100 mA to 2 A		±1%		
<b>PROTECTION CIRCUITS</b>						
V <sub>UVLO_VM</sub>	VM supply undervoltage lockout (UVLO)	Supply rising	4.15	4.3	4.45	V
		Supply falling	4.05	4.2	4.35	V
V <sub>UVLO_HYS</sub>	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t <sub>UVLO</sub>	Supply undervoltage deglitch time	V <sub>VM</sub> falling to OUTx disabled		10		μs
V <sub>RST</sub>	VM UVLO reset	VM falling, device reset, no I <sup>2</sup> C communications			3.9	V
V <sub>OVP_TH</sub>	Overvoltage protection threshold	V <sub>OUT</sub> - V <sub>VM</sub>		200		mV
t <sub>OVP_ON</sub>	Overvoltage protection turn-on time			10		μs
t <sub>OVP_OFF</sub>	Overvoltage protection turn-off time			250		μs
I <sub>OC</sub>	Overcurrent protection trip point		3.7			A
t <sub>OC</sub>	Overcurrent protection deglitch time			2		μs
t <sub>RETRY</sub>	Retry time			1.7		ms
T <sub>TSD</sub>	Thermal shutdown temperature		150	175		°C
T <sub>HYS</sub>	Thermal shutdown hysteresis			40		°C

## 6.6 I2C Timing Requirements

		MIN	NOM	MAX	UNIT
<b>STANDARD MODE</b>					
f <sub>SCL</sub>	SCL Clock frequency	0		100	kHz

		MIN	NOM	MAX	UNIT
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4			$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	4.7			$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	4			$\mu$ s
$t_{SU,STA}$	Setup time for a repeated START condition	4.7			$\mu$ s
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.035		3.45	$\mu$ s
$t_{SU,DAT}$	Data set-up time	250			ns
$t_R$	SDA and SCL rise time			1000	ns
$t_F$	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	4			$\mu$ s
$t_{BUF}$	Bus free time between a STOP and START condition	4.7			$\mu$ s
<b>FAST MODE</b>					
$f_{SCL}$	SCL Clock frequency	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	1.3			$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	0.6			$\mu$ s
$t_{SU,STA}$	Setup time for a repeated START condition	0.6			$\mu$ s
$t_{HD,DAT}$	Data hold time: For I2C bus devices	0.035		0.9	$\mu$ s
$t_{SU,DAT}$	Data set-up time	250			ns
$t_R$	SDA and SCL rise time			300	ns
$t_F$	SDA and SCL fall time			300	ns
$t_{SU,STO}$	Set-up time for STOP condition	0.6			$\mu$ s
$t_{BUF}$	Bus free time between a STOP and START condition	1.3			$\mu$ s
$t_{SP}$	Pulse width of spikes to be suppressed by input noise filter		50		ns



## 6.7 Timing Diagrams

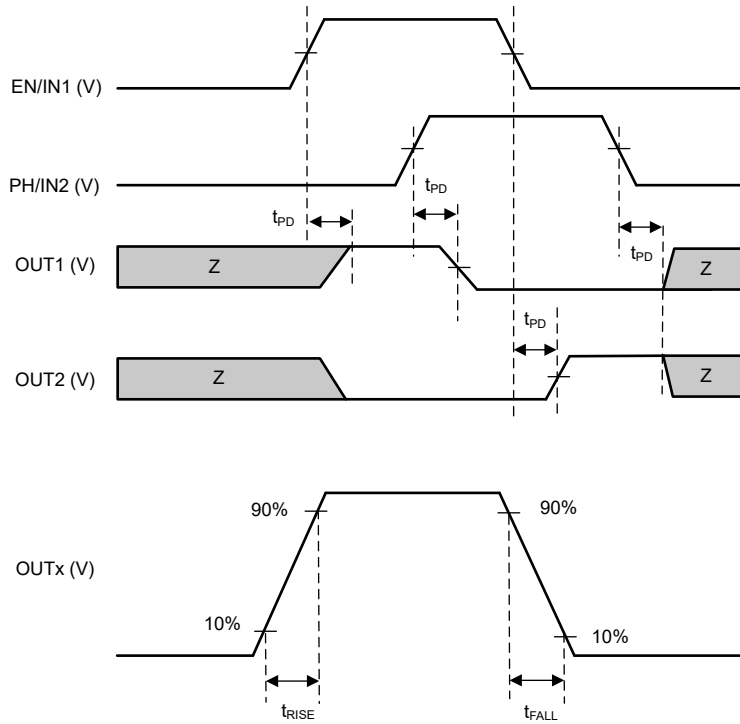


図 6-1. Input-to-Output Timing Diagram

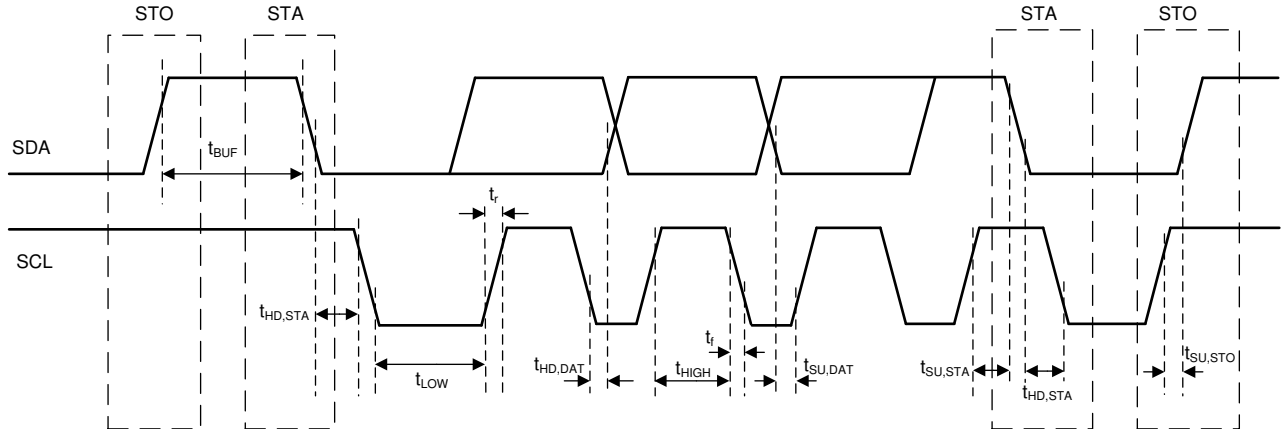
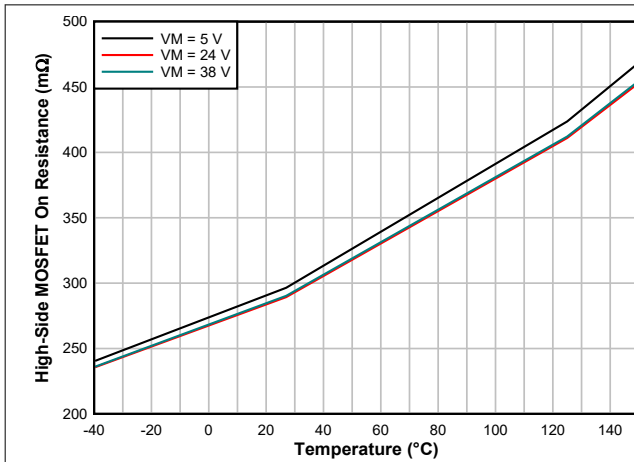
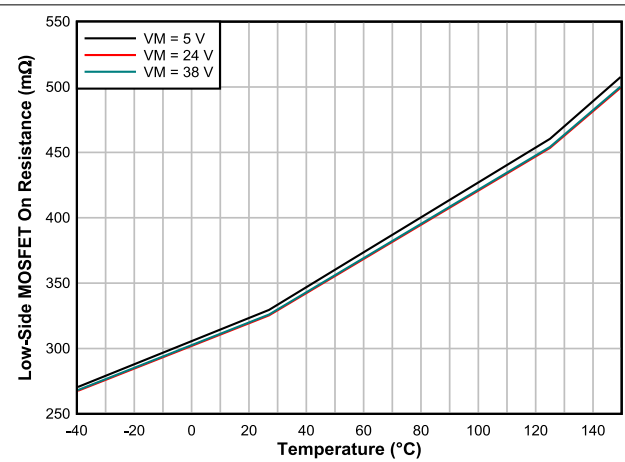


図 6-2. I<sup>2</sup>C Timing Diagram

## 6.8 Typical Operating Characteristics



6-3. High-Side MOSFET On Resistance (mΩ)



6-4. Low-Side MOSFET On Resistance (mΩ)

## 7 Detailed Description

### 7.1 Overview

The DRV8234 is a high-performance full-bridge motor driver with ripple counting for position detection, motor speed and voltage regulation, stall detection, integrated current sense, and integrated current regulation.

The Ripple Counting feature integrates DC motor relative position and speed detection in the device thereby reducing external components on a PCB and saving cost. The principle is based on counting the number of current ripples appearing in the motor current waveform due to commutations. Motor speed regulation feature maintains constant motor speed over varying battery voltages. The voltage regulation feature saves energy by driving the motor with a programmable lower terminal voltage.

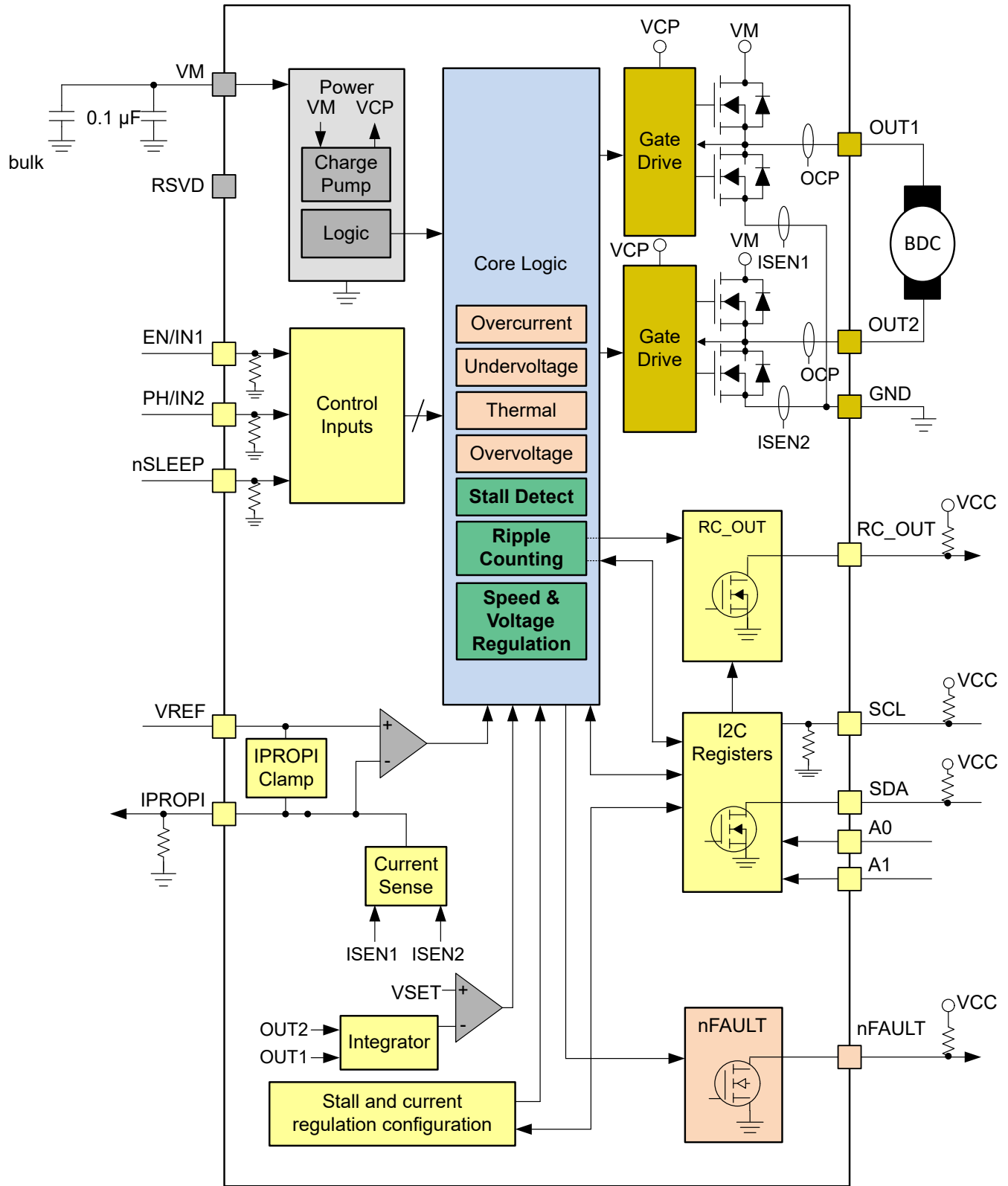
The DRV8234 uses a standard 2-pin (EN/IN1 & PH/IN2) PH/EN-PWM interface and I<sup>2</sup>C interface for configuration and detailed diagnostics. The EN/IN1 & PH/IN2 pins control the full bridge, which consists of four N-channel MOSFETs that have a typical  $R_{DS(ON)}$  of 600 m $\Omega$  (including one high-side and one low-side FET). Motor speed can be controlled with pulse-width modulation (PWM), at frequencies between 0 to 200 kHz. The PMODE bit in I<sup>2</sup>C registers allow operating the H-bridge in two different control modes. I<sup>2</sup>C interface reduces number of GPIO inputs in high motor-count systems and reduces firmware control effort.

The integrated current regulation feature limits motor current to a predefined maximum based on the VREF and IPROPI settings. The IPROPI signal can provide current feedback to a microcontroller during both the drive and brake/slow-decay states of the H-bridge. The DRV8234 also has I<sup>2</sup>C programmable registers to configure a hardware stall detection feature based on the IPROPI current sensing signal.

The integrated protection features protect the device in case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. Additionally, the overvoltage protection (OVP) feature puts the driver into the brake state when the motor is spun manually while the device is in sleep mode or when the H-bridge is disabled. This prevents the back EMF induced high voltages on the supply rail that could potentially damage the driver and other circuits in the system.

To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and the corresponding capacitors. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 External Components

表 7-1 lists the recommended external components for the device.

**表 7-1. Recommended External Components**

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C <sub>VM1</sub>	VM	GND	0.1- $\mu$ F, low ESR ceramic capacitor, VM-rated.
C <sub>VM2</sub>	VM	GND	<a href="#">Bulk Capacitance</a> , VM-rated.
R <sub>I<sub>PROPI</sub></sub>	I <sub>PROPI</sub>	GND	Resistor from I <sub>PROPI</sub> pin to GND, sets the current regulation level.
R <sub>n<sub>FAULT</sub></sub>	System VCC	n <sub>FAULT</sub>	10 k $\Omega$
R <sub>RC_OUT</sub>	System VCC	RC_OUT	10 k $\Omega$
R <sub>Pull-up</sub>	SDA, SCL, A0, A1	VM	2.2 k $\Omega$

### 7.3.2 Summary of Features

This section includes a summary of the key and advanced features of DRV8234.

1. [DRV8234 Functional Block Diagram](#)
2. [Current Sense and Regulation \(I<sub>PROPI</sub>\)](#)
3. [Bridge Control](#)
4. [Protection](#)
5. Advanced: [Stall Detection](#)
6. Advanced: [Ripple Counting](#)
7. Advanced: [Error Correction](#)
8. Advanced: [Speed and Voltage Regulation](#)
9. Advanced: [Soft-Start and Soft-Stop](#) using  $t_{INRUSH}$

### 7.3.3 Bridge Control

The DRV8234 output consists of four N-channel MOSFETs designed to drive high current. These outputs are controlled by the two inputs EN/IN1 and PH/IN2 or the I<sup>2</sup>C bits I2C\_EN\_IN1 and I2C\_PH\_IN2.

The I2C\_BC bit determines whether the bridge is controlled by the EN/IN1 and PH/IN2 pins or the I2C\_EN\_IN1 and I2C\_PH\_IN2 bits, as shown below.

**表 7-2. H-Bridge Control Interface**

I2C_BC	Description
0b	Bridge control configured by using the EN/IN1 and PH/IN2 pins.
1b	Bridge control configured by using the I2C_EN_IN1 and I2C_PH_IN2 bits.

The control interface is selected by the PMODE bit, as shown below.

**表 7-3. PMODE Functions**

PMODE	Control Mode
0b	PH/EN
1b	PWM

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. Following diagram shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.

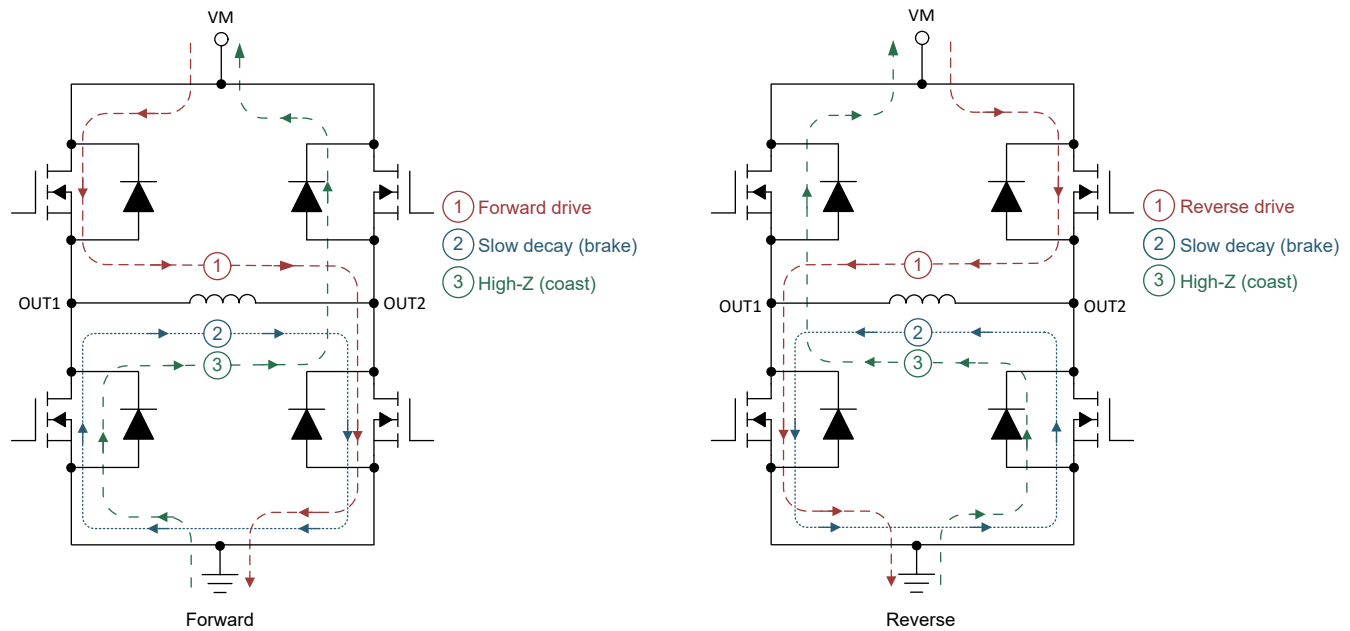


図 7-1. H-Bridge Current Paths

The truth tables for each control mode are shown below. Note that these tables do not take into account the internal current regulation feature. Additionally, when an output changes from driving high to driving low (or driving low to driving high), dead time is automatically inserted to prevent shoot-through.

PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. The truth table for PH/EN mode is shown below.

表 7-4. PH/EN Control Mode (PMODE = 0b)

nSLEEP	Enable	Phase	OUT1	OUT2	Description
0	X	X	High-Z	High-Z	Sleep Mode (H-bridge High-Z)
1	1	0	L	H	Reverse (Current OUT2 → OUT1)
1	1	1	H	L	Forward (Current OUT1 → OUT2)
1	0	X	L	L	Brake; low-side slow decay

注

Enable refers to the EN pin when bridge control is external (I2C\_BC=0b), and the I2C\_EN\_IN1 bit when bridge control is internal (I2C\_BC=1b).

Phase refers to the PH pin when bridge control is external (I2C\_BC=0b), and the I2C\_PH\_IN2 bit when bridge control is internal (I2C\_BC=1b).

PWM mode allows for the H-bridge to enter the High-Z state while the device is awake. The truth table for PWM mode is shown below.

表 7-5. PWM Control Mode (PMODE = 1b)

nSLEEP	Input1	Input2	OUT1	OUT2	Description
0	X	X	High-Z	High-Z	Sleep Mode (H-bridge High-Z)
1	0	0	High-Z	High-Z	Coast (H-bridge High-Z)
1	0	1	L	H	Reverse (Current OUT2 → OUT1)
1	1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	1	L	L	Brake; low-side slow decay

注

Input1 refers to the IN1 pin when bridge control is external (I2C\_BC=0b), and the I2C\_EN\_IN1 bit when bridge control is internal (I2C\_BC=1b).

Input2 refers to the IN2 pin when bridge control is external (I2C\_BC=0b), and the I2C\_PH\_IN2 bit when bridge control is internal (I2C\_BC=1b).

The following timing diagram shows the timing of the inputs and outputs of the motor driver.

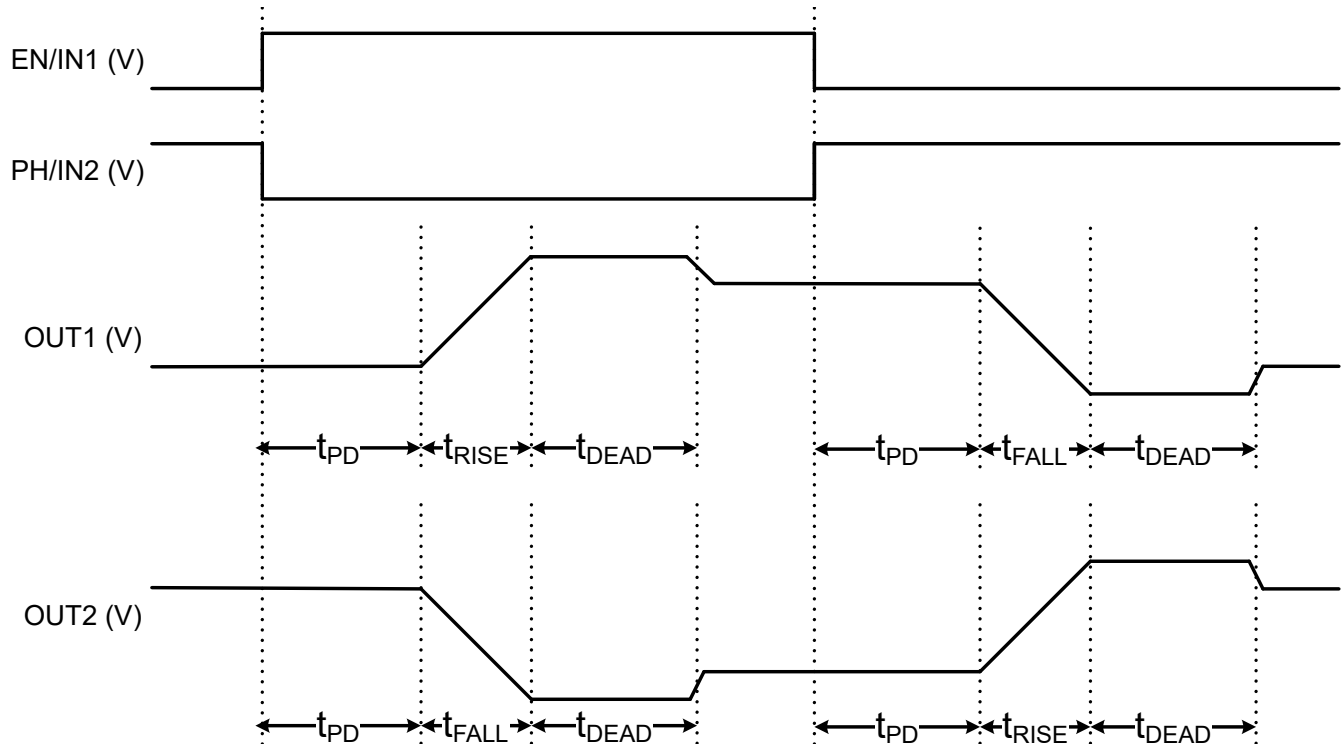


図 7-2. H-Bridge Timing Diagram

The  $t_{DEAD}$  time is the time in the middle when the output is High-Z. The output pin voltage during  $t_{DEAD}$  depends on the direction of the output current. If the current is sourced from the pin, the voltage is a diode voltage drop below ground. If the current is sunk to pin, the voltage is a diode voltage drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time ( $t_{PD}$ ) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times ( $t_{RISE}$  and  $t_{FALL}$ ).

### 7.3.4 Current Sense and Regulation (IPROPI)

The DRV8234 integrates current sensing, regulation, and current sense feedback. The internal current mirror allows the device to sense the output current without an external sense resistor or sense circuitry, thereby reducing system size, cost, and complexity. The current regulation feature allows for the device to limit the output current in case of motor stall or high load torque events. The IPROPI output provides a current output proportional to the load current. This  $I_{IPROPI}$  current can be converted to a  $V_{IPROPI}$  output voltage by connecting a suitable resistor  $R_{IPROPI}$  from this pin to the circuit ground. The following diagram shows the IPROPI timings specified in the Electrical Characteristics table.

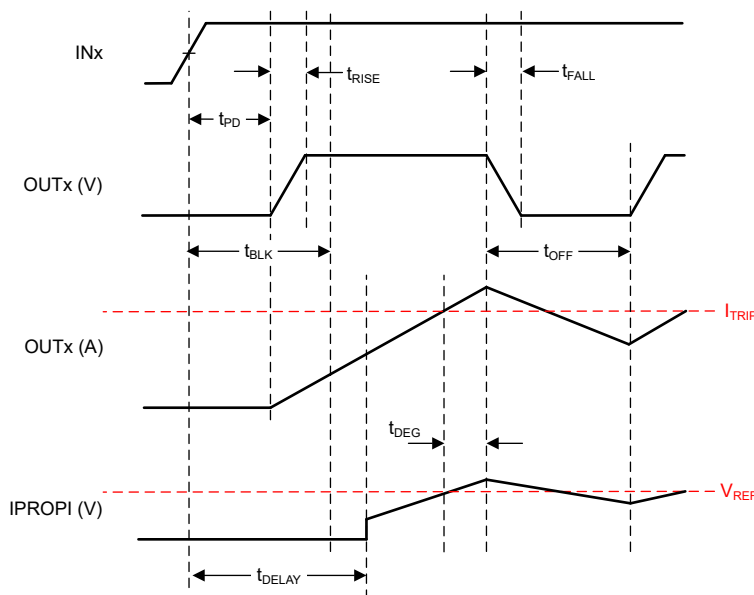


図 7-3. Detailed IPROPI Timing Diagram

#### 7.3.4.1 Current Sensing

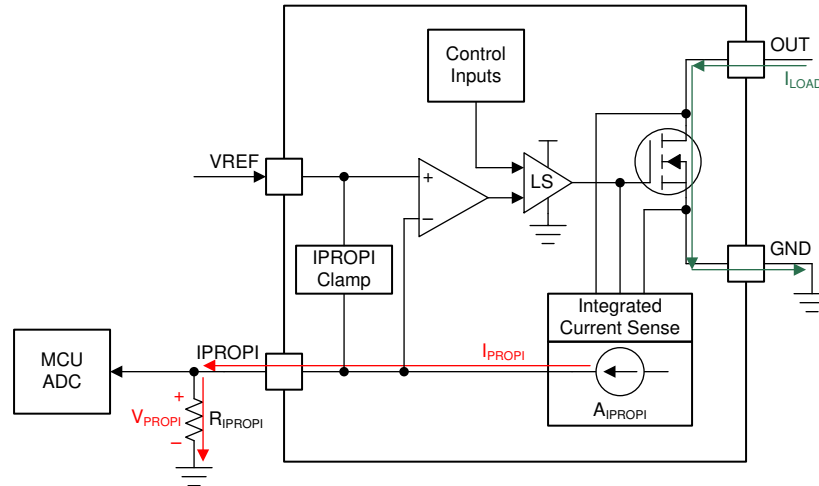
The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge and scaled by the current mirror gain ( $A_{IPROPI}$ ). The IPROPI output current can be calculated by the following equation. The  $I_{LSx}$  in the equation is only valid when the current flows from drain to source in the low-side MOSFET. If current flows from source to drain or through the body diode, the value of  $I_{LSx}$  for that channel is zero. For instance, if the bridge is in the brake, slow-decay state, then the current out of IPROPI is only proportional to the current in one of the low-side MOSFETs.

$$I_{IPROPI} (\mu A) = (I_{LS1} + I_{LS2}) (A) \times A_{IPROPI} (\mu A/A) \quad (1)$$

The  $A_{ERR}$  parameter in the Electrical Characteristics table is the error associated with the  $A_{IPROPI}$  gain. It indicates the combined effect of offset error added to the  $I_{OUT}$  current and gain error. The current mirror gain  $A_{IPROPI}$  is fixed at 1500  $\mu A/A$ .

The motor current is measured by an internal current mirror architecture on the low-side FETs which removes the need for an external power sense resistor as shown below. The current mirror architecture senses motor winding current in both the drive and brake low-side slow-decay periods, therefore allowing continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed because it flows from source to drain. However, the current can be sampled by briefly reenabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.





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図 7-4. Integrated Current Sensing

The IPROPI pin should be connected to an external resistor ( $R_{IPROPI}$ ) to ground in order to generate a proportional voltage ( $V_{IPROPI}$ ) on the IPROPI pin with the  $I_{IPROPI}$  analog current output. This allows for the load current to be measured as the voltage drop across the  $R_{IPROPI}$  resistor with a standard analog to digital converter (ADC). The  $R_{IPROPI}$  resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. Additionally, the DRV8234 implements an internal IPROPI voltage clamp circuit to limit  $V_{IPROPI}$  with respect to  $V_{VREF}$  on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events. TI recommends designing for at least 1.25 V of headroom between  $V_{VM}$  and the maximum  $V_{IPROPI}$  voltage to be measured by the ADC,  $V_{IPROPI\_MAX}$ . This ensures good accuracy across the range of  $V_{IPROPI}$  voltages measured by the ADC. For instance, if  $V_{VM}$  is 4.55 V to 11 V,  $V_{IPROPI\_MAX}$  can be as high as 3.3 V. However, if  $V_{VM}$  is 3.3 V, then  $V_{IPROPI}$  will have good accuracy up to 2.05 V.

The corresponding IPROPI voltage to the output current can be calculated as shown below -

$$V_{IPROPI} (V) = I_{IPROPI} (A) \times R_{IPROPI} (\Omega) \quad (2)$$

The IPROPI output bandwidth is limited by the sense delay time ( $t_{DELAY}$ ) of the internal current sensing circuit. This time is the delay from the low-side MOSFET enable command (from the INx pins) to the IPROPI output being ready.

If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output. If a command on the INx pins disables the low-side MOSFETs (according to the truth tables), the IPROPI output will disable with the input logic signal. Although the low-side MOSFETs may still conduct current as they disable according to the device slew rate (specified in the Electrical Characteristics table by  $t_{RISE}$  time), IPROPI will not represent the current in the low-side MOSFETs during this turnoff time.

### 7.3.4.2 Current Regulation

The DRV8234 integrates current regulation using either a fixed off-time or a cycle-by-cycle PWM current regulation scheme. This allows the device to limit the output current in case of a motor stall, high torque, or other high current load events autonomously. The current regulation scheme is selectable by the REG\_CTRL bit in I<sup>2</sup>C.

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND if current feedback is not required. Additionally, current regulation can also be disabled by setting IMODE to 00b as explained below. If current feedback is required and current regulation is not required, set  $V_{VREF}$  and  $R_{IPROPI}$  such that  $V_{IPROPI}$  never reaches the  $V_{VREF}$  threshold. For proper operation of the current

regulation circuit,  $V_{VREF}$  must be within the range of the VREF pin voltage specified in the Recommended Operating Conditions table.

**表 7-6. REG\_CTRL Functions**

Bit*	Current Regulation Mode
00b	Fixed Off-Time
01b	Cycle-By-Cycle

**注**

\*Additional REG\_CTRL options 10b and 11b allow selection between motor voltage or speed regulation described in [セクション 7.3.7.2.1](#).

The current regulation threshold ( $I_{TRIP}$ ) is set through a combination of the VREF voltage ( $V_{VREF}$ ) and IPROPI output resistor ( $R_{IPROPI}$ ). This is done by comparing the voltage drop across the external  $R_{IPROPI}$  resistor to  $V_{VREF}$  with an internal comparator.

$$I_{TRIP} (A) \times A_{IPROPI} (\mu A/A) = V_{VREF} (V) / R_{IPROPI} (\Omega) \quad (3)$$

For example, if  $V_{VREF} = 3.3 V$ ,  $R_{IPROPI} = 1100 \Omega$  and  $A_{IPROPI} = 1500 \mu A/A$ , then  $I_{TRIP}$  will be approximately 2 A.

$V_{VREF}$  must be lower than  $V_{VM}$  by at least 1.25 V. The maximum recommended value of  $V_{VREF}$  is 3.3 V. If INT\_VREF bit is set to 1b,  $V_{VREF}$  is internally selected with a fixed value of 3 V.

The  $I_{TRIP}$  comparator has both a blanking time ( $t_{BLANK}$ ) and a deglitch time ( $t_{DEG}$ ). The internal blanking time helps to prevent voltage and current transients during output switching from affecting the current regulation. These transients may be caused by a capacitor inside the motor or motor terminals. The internal deglitch time ensures that transient conditions do not prematurely trigger the current regulation. In certain cases where the transient conditions are longer than the deglitch time, placing a 10-nF capacitor on the IPROPI pin, close to the device, helps filter the transients on IPROPI output so current regulation does not prematurely trigger. The capacitor value can be modified as needed, however large capacitor values may slow down the response time of the current regulation circuit.

The IMODE bits determine the behavior of current regulation for the motor driver.

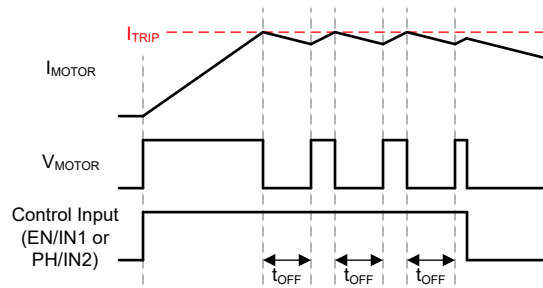
- When IMODE is 00b, current regulation is disabled.
- When IMODE is 01b, the device performs current regulation only during the  $t_{INRUSH}$  time when stall detection is enabled.
- When IMODE is 10b, current regulation is enabled at all times.

The following table summarizes the IMODE bit settings.

**表 7-7. IMODE configuration**

IMODE	EN_STALL	Description
00b	X	No current regulation at any time
01b	0b	Current regulation at all times
	1b	Current regulation during $t_{INRUSH}$ only
1Xb	X	Current regulation at all times

### 7.3.4.2.1 Fixed Off-Time Current Regulation



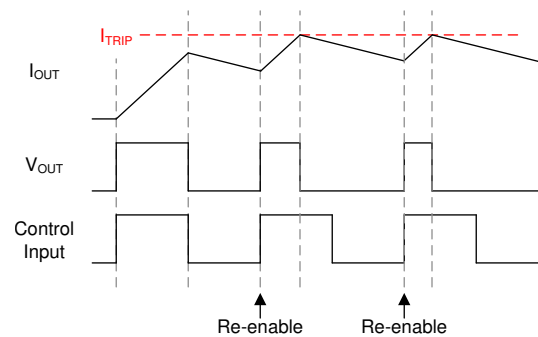
**図 7-5. Fixed Off-Time Current Regulation**

In the fixed off-time mode, the H-bridge enters a brake/low-side slow decay state (both low-side MOSFETs ON) for  $t_{OFF}$  duration after  $I_{OUT}$  exceeds  $I_{TRIP}$ . After  $t_{OFF}$  the outputs are re-enabled according to the control inputs unless  $I_{OUT}$  is still greater than  $I_{TRIP}$ . If  $I_{OUT}$  is still greater than  $I_{TRIP}$ , the H-bridge will enter another period of brake/low-side slow decay for  $t_{OFF}$ . If the state of the EN/IN1 or PH/IN2 control pin inputs or I2C\_EN\_IN1 or I2C\_PH\_IN2 bits changes during the  $t_{OFF}$  time, the remainder of the  $t_{OFF}$  time is ignored, and the outputs will again follow the inputs.

The fixed off-time mode allows for a simple current regulation scheme independent of the external controller. Fixed off-time mode will support 100% duty cycle current regulation since the H-bridge automatically enables after the  $t_{OFF}$  period and does not require a new control input edge on the control input pins or bits to reset the outputs.

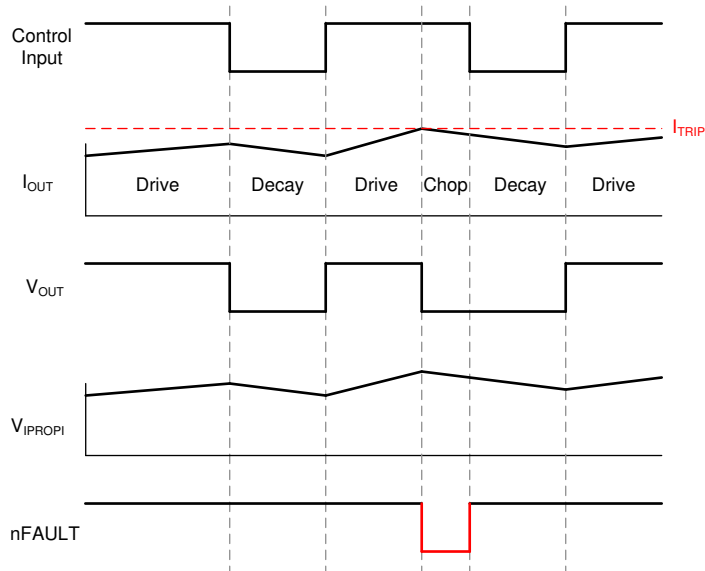
### 7.3.4.2.2 Cycle-By-Cycle Current Regulation

In cycle-by-cycle mode, the H-bridge enters a brake, low-side slow decay state (both low-side MOSFETs ON) after  $I_{OUT}$  exceeds  $I_{TRIP}$  until the next control input edge on either the EN/IN1 or PH/IN2 pins or 0 to 1 transitions on the I2C\_EN\_IN1 or I2C\_PH\_IN2 bits. This allows for additional control of the current regulation by the external controller. This is shown in the diagram below. Cycle-by-cycle mode will not support 100% duty cycle current regulation as a new control input edge is required to reset the outputs after the brake, low-side slow decay state has been entered.



**図 7-6. Cycle-By-Cycle Current Regulation**

In cycle-by-cycle mode, the device can indicate whenever the H-bridge enters internal current regulation by pulling the nFAULT pin low. This can be used to determine when the device outputs will differ from the control inputs or the load has reached the  $I_{TRIP}$  threshold. This behavior is controlled by the CBC\_REP bit. This is shown in the following diagram. In cycle-by-cycle mode, if the CBC\_REP bit is 1b, nFAULT will be pulled low when the H-bridge enters internal current regulation and nFAULT will be released whenever the next control input edge is received by the device and the outputs are reset.



**図 7-7. Cycle-By-Cycle Current Regulation, CBC\_REP = 1b**

No device functionality is affected when the nFAULT pin is pulled low for the current regulation indicator. The nFAULT pin is only used as an indicator and the device will continue normal operation. To distinguish a device fault from the current regulation indicator, the nFAULT pin can be compared with the control inputs. The current regulation indicator can only assert when the control inputs are commanding a forward or reverse drive state. If the nFAULT pin is pulled low and the control inputs are commanding the high-Z or slow-decay states, then a device fault has occurred.

### 7.3.5 Stall Detection

The DRV8234 integrates a stall detection feature. The principle of the stall detection scheme relies on the fact that motor current increases during stall conditions. The DRV8234 compares the voltage on the IPROPI pin to the voltage on the VREF pin or 3 V to determine whether a motor stall condition has occurred. The setting is determined by the INT\_VREF register. 表 7-8 shows the configurable options for INT\_VREF. The following paragraphs describe how to configure the I<sup>2</sup>C registers for the desired stall detection response.

**表 7-8. Settings for INT\_VREF**

Bit	Description
0b	V <sub>VREF</sub> not fixed
1b	V <sub>VREF</sub> fixed internally at 3 V

The STALL bit in status register changes to 1b when a motor stall is detected. The EN\_STALL bit is used to enable or disable stall detection. The following table summarizes the EN\_STALL bit settings.

**表 7-9. EN\_STALL configuration**

EN_STALL	Description
0b	Stall detection disabled. If IMODE = 01b, current regulation occurs at all times when V <sub>IPROPI</sub> ≥ V <sub>VREF</sub> .
1b	Stall detection enabled.

The IPROPI pin provides the current sense signal to the stall detection module. The VREF pin sets the I<sub>TRIP</sub> current level at which a stall condition is detected. As shown in 表 7-8, V<sub>VREF</sub> is internally fixed at 3 V when INT\_VREF = 1b. When V<sub>IPROPI</sub> ≥ V<sub>VREF</sub>, it implies I<sub>OUT</sub> ≥ I<sub>TRIP</sub>. The device detects a stall condition here. Stall detection is blanked for a period of time, t<sub>INRUSH</sub>, to avoid false detection due to high inrush currents during motor startup. The IPROPI and VREF pins also support current regulation, as described earlier.

The TINRUSH[15:0] bits set the period of time the stall detection logic will ignore the inrush current during motor startup ( $t_{INRUSH}$ ). After  $t_{INRUSH}$  time expires, the DRV8234 indicates a stall condition the next instant  $V_{IPROPI}$  is greater than or equal to  $V_{VREF}$ .

When voltage or speed soft-start is disabled, the  $t_{INRUSH}$  time directly reflects the setting of the TINRUSH bits. The  $t_{INRUSH}$  can be set to a value between 5 ms (corresponding to 0000h) and 6.7 s (corresponding to FFFFh), with a default value of 1 s. Each increment of LSB corresponds to 102.4  $\mu$ s of the inrush time.

When voltage or speed soft-start is enabled, target motor voltage or speed is soft-started and soft-stopped for the duration of  $t_{INRUSH}$  time. The TINRUSH bits should be setup such that the  $t_{INRUSH} = \text{TINRUSH bit setting} \times \text{WSET\_VSET}$ . For example, if WSET\_VSET = 10 and intended inrush time is 1 s, then TINRUSH bit setting should correspond to 100 ms.

The following conditions cause the stall detection scheme to ignore the inrush current for  $t_{INRUSH}$  time -

- Power-up of the DRV8234
- Recovering from faults
- After device exits from sleep mode
- After recovering from stall, as explained in [表 7-10](#)

The SMODE bit programs the device's response to a stall condition. When SMODE = 0b, the outputs disable, and the STALL bit becomes 1b. When SMODE = 1b, the STALL bit becomes 1b, but the outputs continue to drive current into the motor. [表 7-10](#) summarizes the SMODE bit settings.

**表 7-10. SMODE configuration**

SMODE	Description	Recovery from Stall Condition
0b	Latched disable with indication: the OUTx pins disable and the STALL bit becomes 1b.	A clear fault must be issued by writing 1b to the CLR_FLT bit. STALL bit changes to 0b after a clear fault is issued. After waking up from stall, the stall detection scheme ignores the inrush current for $t_{INRUSH}$ time as described earlier. After $t_{INRUSH}$ time, if motor current is still higher than $I_{TRIP}$ , a stall condition is detected again.
1b	Indication only: the OUTx pins remain active and the STALL bit becomes 1b.	A clear fault must be issued by writing 1b to the CLR_FLT bit to make STALL bit 0b. After $t_{INRUSH}$ time, if motor current is still higher than $I_{TRIP}$ , a stall condition is detected again.

The **IMODE** bits determine the behavior of current regulation in the motor driver. [表 7-7](#) summarizes the IMODE pin settings. For more details on current regulation, see [セクション 7.3.4.2](#).

The STALL\_REP bit determines whether stall is reported on nFAULT pin. When STALL\_REP bit is 1b, nFAULT is pulled low whenever stall is detected and STALL bit is 1b. If STALL\_REP bit is 0b, stall is not reported on nFAULT output.

The following diagrams show example timing diagrams for different configurations of the hardware stall detection feature.

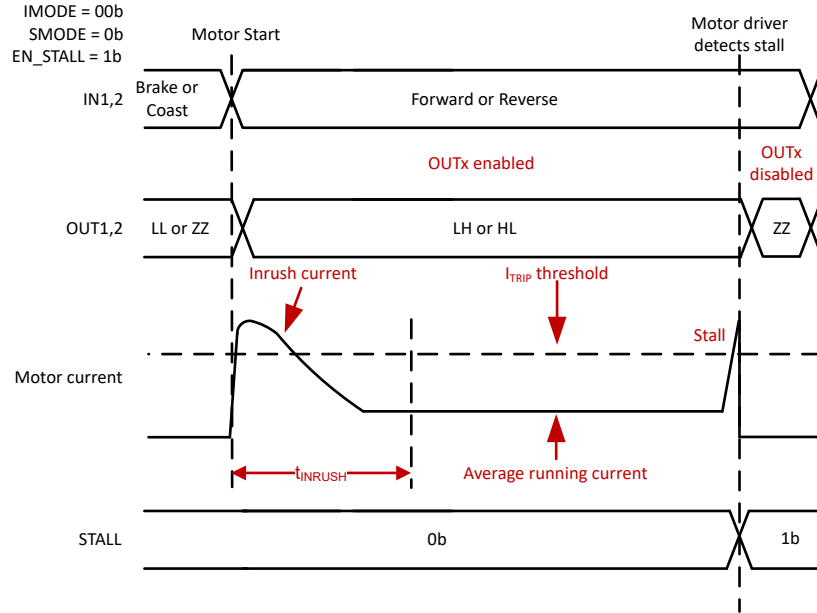


図 7-8. Stall Detection with Latched Disable

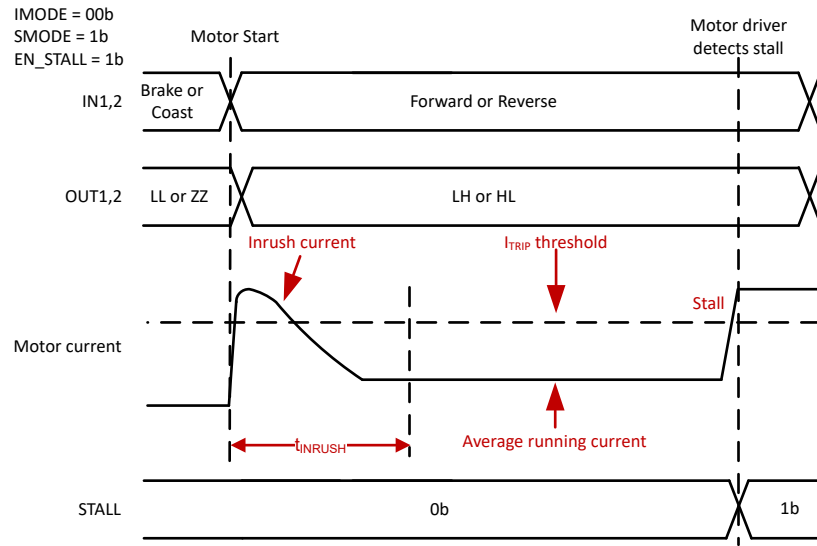
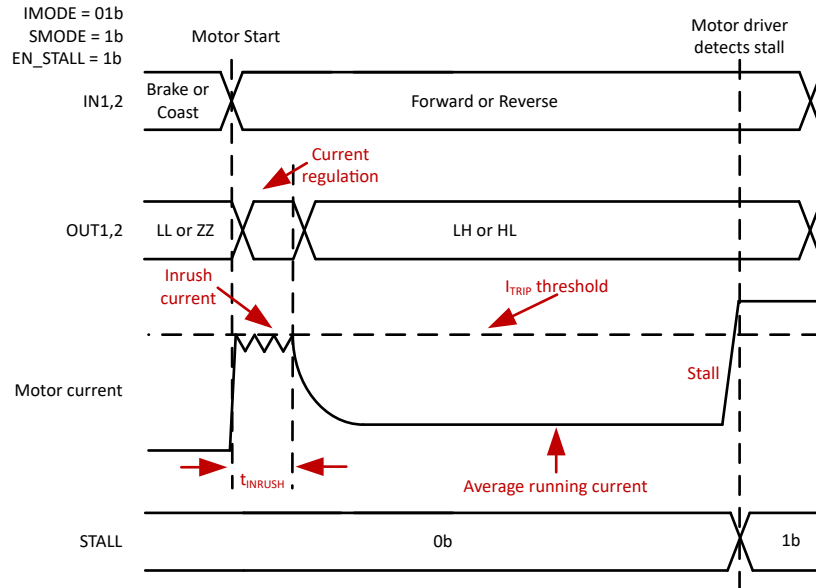
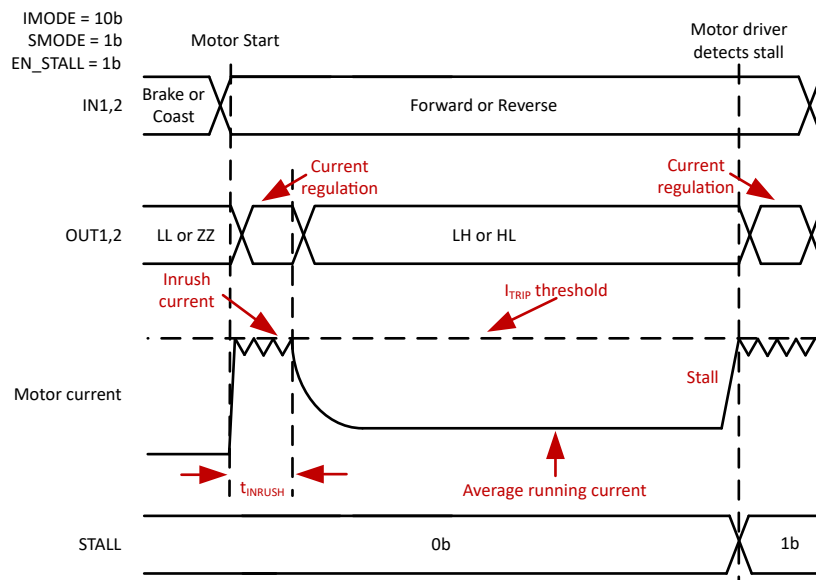


図 7-9. Stall Detection with STALL indication only



 **7-10. Stall Detection with current regulation during inrush**



 **7-11. Stall Detection with current regulation**

### 7.3.6 Ripple Counting

In applications such as electronic locks and gas valves, it may be required to identify the rotor position or speed of the brushed-DC motor to implement a variety of different functions at the system level. Most systems implement position or speed detection using encoders, limit switches or Hall sensors.

The DRV8234 supports an integrated Ripple counting algorithm to estimate motor position and speed without using any external sensors such as an encoder or a Hall sensor. This enables reduction in system BOM count, BOM cost, and design complexity.

Ripple counting with integrated stall detection allows increased system reliability. For example, in a gas valve system, although the timing of stall detection may change due to changes in temperature and gas pressure, the

number of ripples before stall will be same for each actuation. If a stall occurs, but the number of ripples is less than the target value, then this may indicate a loss of position, for example due to a jammed valve.

To enable the ripple counting feature, set EN\_RC to 1b.

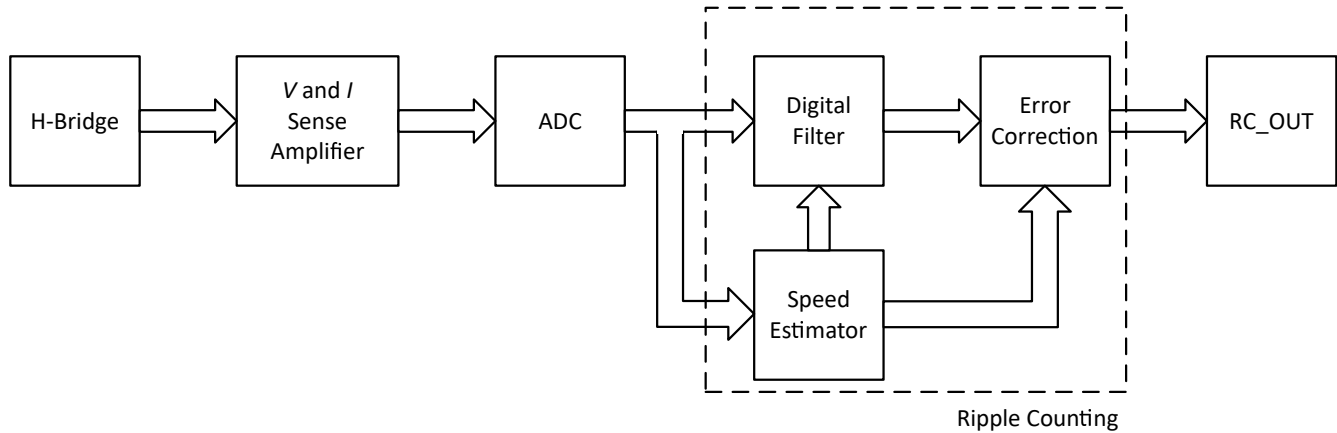


図 7-12. Ripple counting block diagram

### 7.3.6.1 Ripple Counting Parameters

To achieve an accurate ripple count, the following parameters must be configured accurately. Refer to [セクション 7.6](#) for additional details. Refer to [セクション 8.2.3.1](#) for the detailed tuning procedure.

#### 7.3.6.1.1 Motor Resistance Inverse

Denoted by INV\_R, this is the equivalent of the conductance (inverse of resistance) of the motor scaled by a scaling factor, INV\_R\_SCALE. Scaling allows a wide range of motor resistance values to be accepted using the combination of INV\_R and INV\_R\_SCALE.

#### 7.3.6.1.2 Motor Resistance Inverse Scale

Denoted by INV\_R\_SCALE, this is the scaling factor for the inverse of motor resistance (INV\_R). Since the inverse of a motor resistance is generally not an integer, the value must be rounded off to the nearest integer. Settings are described in [セクション 7.3.6.1.2](#).

表 7-11. Settings for INV\_R\_SCALE

Bit	Value of INV_R_SCALE
00b	2
01b	64
10b	1024
11b	8192

INV\_R is represented by the equation:

$$INV\_R = \frac{1}{\text{Motor Resistance}} \times INV\_R\_SCALE \tag{4}$$

Please note that the maximum value of INV\_R is 255.

#### 7.3.6.1.3 KMC Scaling Factor

Denoted by KMC\_SCALE, this is a scaling factor for the parameter KMC. KMC is represented by the following equation:

$$KMC = \frac{K_V}{N_R} \times KMC\_SCALE \tag{5}$$



Where,  $K_V$  is the motor back emf constant and  $N_R$  is the number of ripples per revolution.  $N_R$  is calculated by taking the LCM (Least Common Multiple) of the number of brushes,  $N_B$ , and the number of commutators,  $N_C$ :

$$N_R = \text{LCM}(N_B, N_C) \quad (6)$$

Please note that LCM can be easily calculated by using any online LCM calculator.

Tuning KMC appropriately is critical for the ripple counting algorithm to perform accurately. Scaling is done because the value of motor back emf constant is generally small. Scaling allows integer values to be written on to registers.

**表 7-12. Settings for KMC\_SCALE**

Bit	Value of KMC_SCALE
00b	$24 \times 2^8$
01b	$24 \times 2^9$
10b	$24 \times 2^{12}$
11b	$24 \times 2^{13}$

#### 7.3.6.1.4 KMC

This register is a motor constant representing a proportional value of the motor back emf constant. See [KMC Tuning](#) for a detailed tuning procedure.

#### 7.3.6.1.5 Filter Damping Constant

Denoted by  $FLT\_K$ , this parameter represents the quality factor or Q-factor of the band pass filter. Tune this parameter to increase or decrease the bandwidth to accommodate a wider or narrower range of ripple frequencies around the center frequency. Center frequency of the filter is based on the frequency estimation of the ripples in the motor current waveform.

#### 7.3.6.1.6 Filter Input Scaling Factor

Denoted by  $FLT\_GAIN\_SEL$ , this parameter selects the gain for the band pass filter. The gain scales the magnitude of current ripples for ease of detection and algorithmic calculation by the Ripple Counter. Settings are mentioned below.

**表 7-13. Settings for FLT\_GAIN\_SEL**

Bit	Value of FLT_GAIN_SEL
00b	2
01b	4
10b	8
11b	16

#### 7.3.6.1.7 Ripple Count Threshold

Denoted by  $RC\_THR$ , this parameter represents the threshold setting for the total number of ripple counts vs the total number of ripple counts estimated by the ripple counting algorithm based on the expected time of motor actuation.

Let  $N_{RT}$  be the number of ripples at threshold. Then,  $RC\_THR$  is represented by the equation:

$$N_{RT} = RC\_THR \times RC\_THR\_SCALE \quad (7)$$

The parameters further involved in ripple counting threshold are as follows:

- $RC\_CNT$  is a 16-bit register which corresponds to the number of current ripples counted. When  $RC\_CNT$  exceeds  $N_{RT}$ ,  $CNT\_DONE$  is latched high.

2. **CNT\_DONE** is a status register that latches high when RC\_CNT exceeds  $N_{RT}$ . This register can be cleared by using CLR\_CNT.
3. **RC\_REP** decides if nFAULT maintains previous value or is pulled low when RC\_CNT exceeds  $N_{RT}$ .
4. **CLR\_CNT**, when set to 1b, resets  $N_{RT}$  to 0 and CNT\_DONE to 0b.

#### 7.3.6.1.8 Ripple Count Threshold Scale

Denoted by RC\_THR\_SCALE, this is the scaling factor for the number of ripples for threshold. Settings are given below.

**表 7-14. Settings for RC\_THR\_SCALE**

Bit	Value of RC_THR_SCALE
00b	2
01b	8
10b	16
11b	64

Depending on the number of ripples per revolution,  $N_R$ , and the speed of rotations, RC\_THR\_SCALE can be chosen high or low based on user requirement of the nFAULT pin. If total number of ripple counts until the end of an operation cycle are low, choose a lower value of RC\_THR\_SCALE, otherwise a higher value is recommended.

#### 注

Please note that RC\_THR and RC\_THR\_SCALE do not affect the accuracy of ripple counting.

#### 7.3.6.1.9 T\_MECH\_FLT

This parameter determines the cut-off frequency of a low pass filter at the output of the ripple counter to control the response time of the ripple counter. Tune this parameter to match the inertia of the entire mechanical system. Increasing the value of this parameter slows down the ripple counter response time; decreasing the value speeds up the response time.

#### 7.3.6.1.10 VSNS\_SEL

This parameter is used to select the motor voltage output filtering method (analog or digital) during PWM. The analog filter filters out the noise based on the voltage difference between the output pins. The digital filter multiplies the PWM duty cycle with VM to render an average output voltage. Settings are shown in [表 7-15](#). When analog filter is selected, the cut-off frequency can be selected by the **OUT\_FLT** register.

**表 7-15. Settings for VSNS\_SEL**

Bit	Description
0b	Analog Output Filter
1b	Digital Output Filter

#### 7.3.6.1.11 Error Correction

Error correction involves the use of two registers, DIS\_EC and EC\_PULSE\_DIS.

DIS\_EC is used to enable/disable the error correction block shown in [図 7-12](#). [表 7-16](#) shows the settings for DIS\_EC.

**表 7-16. Settings for DIS\_EC**

Bit	Description
0b	Error Correction block is enabled.
1b	Error Correction block is disabled.

EC\_PULSE\_DIS is used to enable/disable the output of the Error Correction block when the Error Correction block is enabled. 表 7-17 describes the settings of EC\_PULSE\_DIS in detail.

表 7-17. Settings for EC\_PULSE\_DIS

Bit	Status of Error Correction block output
0b	Output follows settings for DIS_EC as displayed in 表 7-16. If DIS_EC is set to 0b, RC_OUT continues to output pulses even when the motor is: <ul style="list-style-type: none"> <li>Disconnected,</li> <li>Connected but not rotating, or</li> <li>Stalled (depending on the settings for SMODE), if ripple counting is enabled.</li> </ul> Please note that the Error Correction block is active in this setting.
1b	Output is disabled if the following two conditions are met: <ol style="list-style-type: none"> <li>Error corrector adds 12 consecutive pulses, and</li> <li>The bandpass filter does not give any pulse output during the time period of the 12 consecutive pulses.</li> </ol> Please note that the Error Correction block is active in this setting.

表 7-18 summarizes the settings described above.

表 7-18. Summary of Error Correction

DIS_EC	EC_PULSE_DIS	Error Corrector Status	Output Pulse Status
0b	0b	Enabled	Pulse train output from RC_OUT
0b	1b	Enabled	No pulses only if Error Corrector adds 12 consecutive pulses and bandpass filter gives no output.
1b	X	Disabled	No Pulses

#### 7.3.6.1.11.1 EC\_FALSE\_PER

EC\_FALSE\_PER is a 2-bit register that allows the user to select a blanking time window **after** a current ripple is detected. During this time window, the error corrector classifies any passed ripples from the digital filter as extra ripples and does not count them. The time window is represented as a percentage of time between two successive expected current ripples.

#### 7.3.6.1.11.2 EC\_MISS\_PER

EC\_MISS\_PER is a 2-bit register that allows the user to select a time window for when a current ripple is **expected** to be detected. During this time window, the error corrector takes action if an expected current ripple from the digital filter does not arrive. The time window is represented as a percentage of time between two successive expected current ripples.

#### 7.3.6.2 RC\_OUT Output

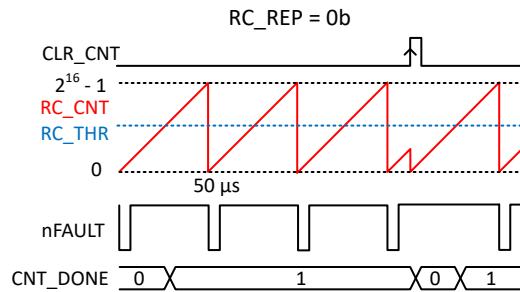
The RC\_OUT pin has an open-drain output and is to be pulled up to a 5-V or 3.3-V supply. The RC\_OUT pin outputs a pulse train corresponding to the number of ripples in the motor current. The positive pulse width of the pulse train is 50  $\mu$ s.

#### 7.3.6.3 Ripple Counting with nFAULT

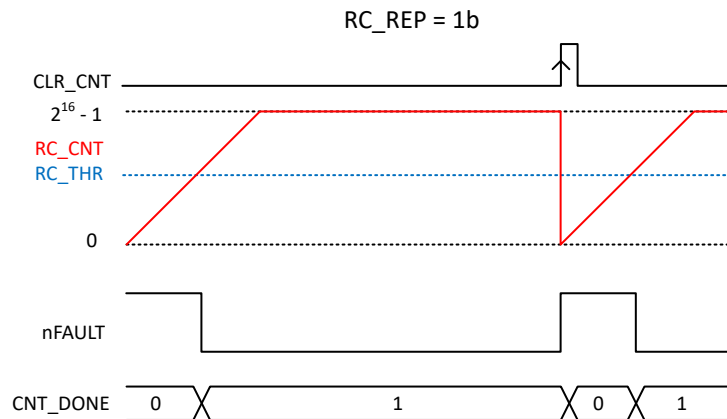
The DRV8234 allows the nFAULT pin to be configured for various settings of RC\_CNT using the RC\_REP register. 表 7-19 lists the settings for the RC\_REP register (refer to セクション 7.6 for details). Timing diagrams corresponding to RC\_REP settings are shown in 図 7-13 and 図 7-14.

**表 7-19. RC\_REP Settings**

RC_REP	nFAULT	RC_CNT
00b	Ripple counting has no effect on nFAULT	If RC_CNT reaches the maximum value of $2^{16} - 1$ , it is held at that value until a CLR_CNT command is issued.
01b	Ripple counting has no effect on nFAULT	If RC_CNT reaches the maximum value of $2^{16} - 1$ , RC_CNT is cleared and restarted from 0.
10b	nFAULT is pulled low if RC_CNT exceeds threshold	If RC_CNT reaches the maximum value of $2^{16} - 1$ , it is held at that value until a CLR_CNT command is issued.
11b	nFAULT is pulled low for 50 $\mu$ s if RC_CNT reaches the maximum value of $2^{16} - 1$	If RC_CNT reaches the maximum value of $2^{16} - 1$ , RC_CNT is cleared and restarted from 0.



**図 7-13. Ripple Counting Timing with RC\_REP = 11b**



**図 7-14. Ripple Counting Timing with RC\_REP = 10b**

### 7.3.7 Motor Voltage and Speed Regulation

The DRV8234 provides the ability to regulate the voltage applied to the motor winding or to regulate the speed of the motor. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery. The DRV8234 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The intended voltage or speed can be programmed by the WSET\_VSET bits. Refer to [セクション 7.3.7.2.1](#) for further explanation.

Four ranges of motor speed can be selected using the W\_SCALE bits to support low, moderate and high speed applications. The speed regulation loop compares the motor speed estimated by the ripple counting algorithm with the user defined target speed. The following section describes the internal bridge control logic taking voltage regulation as an example, but is also applicable for speed regulation.

Figure 7-15 shows the closed loop PI control for regulating speed and voltage.

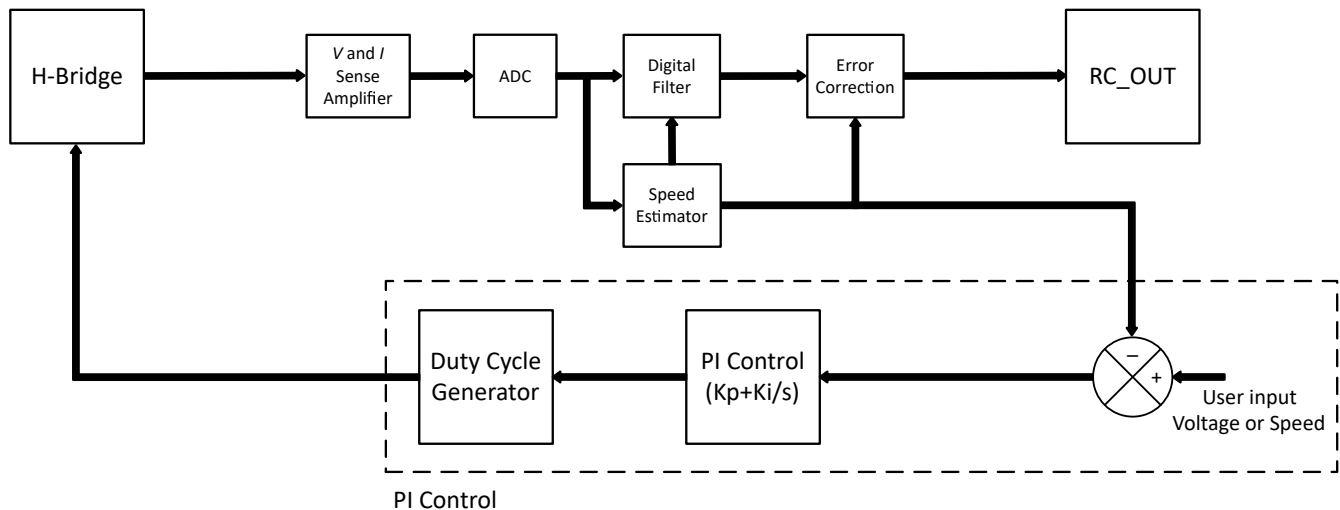


Figure 7-15. Speed and Voltage Regulation with PI Control

### 7.3.7.1 Internal Bridge Control

For voltage regulation, an internal circuit monitors the voltage difference between the output pins. This voltage difference is integrated over time to get an average DC voltage value. The time depends on the cut-off frequency of the output filter which can be set by the `OUT_FLT` register. For best results, choose a cut-off frequency setting equal to at least ten times the PWM frequency.

The DC voltage value is compared to the target motor voltage programmed by the I<sup>2</sup>C register, `WSET_VSET`. During voltage as well as speed regulation modes, an internal bridge control scheme is employed. `PMODE` is used to select the PH/EN mode or the PWM mode.

When Voltage or Speed Regulation mode is active, `DUTY_CTRL` must be set to 0b. Bridge control is internal in this case. Duty cycle can be programmed by using the `IN_DUTY` register.

- If the averaged output voltage is lower than `VSET`, the duty cycle of the internal bridge control output is increased.
- If the averaged output voltage is higher than `VSET`, the duty cycle of the internal bridge control output is decreased.
- During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. The current flow direction depends on the EN/IN1 and PH/IN2 polarity.
- During the PWM off time, winding current is recirculated by enabling both of the low-side FETs in the bridge.
- If the programmed output voltage (`VSET`) is greater than the VM supply voltage, the device operates at 100% duty cycle and the voltage regulation feature is disabled. In this mode, the device behaves like a conventional H-bridge driver.

注

The **IN\_DUTY** register outputs the actual duty cycle of the internal bridge control scheme in voltage regulation mode. **PWM\_FREQ** sets the PWM frequency for internal PWM generation.

Setting **DUTY\_CTRL** to 1b enables the user to program the duty cycle into **EXT\_DUTY** for external bridge control. For using the internal bridge control scheme, **DUTY\_CTRL** must be set to 0b. **IN\_DUTY** can then be used to program the desired duty cycle.

表 7-20. **PWM\_FREQ** Settings

Bit	Value
0b	25 kHz
1b	50 kHz

注

In voltage regulation mode, the motor speed can vary slightly because the voltage drop across the motor coil resistance introduces a small error. The speed regulation mode eliminates this error by directly regulating the target motor speed. To enable speed regulation, the **REG\_CTRL** bit must be set to 10b.

**7.3.7.2 Setting Speed/Voltage Regulation Parameters**

For obtaining an accurate output from speed and voltage regulation, the following parameters need to be set (for an in-depth explanation, refer to [セクション 7.6](#)).

**7.3.7.2.1 Speed and Voltage Set**

Denoted by **WSET\_VSET**, this parameter helps set the target ripple speed or motor voltage, based on the **REG\_CTRL** register setting.

When **REG\_CTRL** is set to 10b, the speed regulation mode is enabled. **WSET\_VSET** is an 8-bit register and can be set to a value between 00h (corresponds to 0 rad/s) and FFh (corresponds to the maximum speed allowable by **W\_SCALE**). The [speed control loop](#) matches the value of the **SPEED** register to the target speed set by **WSET\_VSET**. Please note that the maximum value of the **SPEED** register is 255. Also note that:

$$\text{Target Ripple Speed} = \text{SPEED} \times \text{W\_SCALE} \tag{8}$$

When **REG\_CTRL** is set to 11b, the motor voltage regulation mode is enabled. The motor voltage in this case can be set to a value between 0 for 0 V and 255 for approximately 42.67 V drive output voltage. Please note that the maximum value of **WSET\_VSET** is 255. Each bit corresponds to approximately a 0.167 mV resolution of the output voltage setting. Setting **WSET\_VSET** to 255 sets the target voltage to approximately 42.7 V.

For example, if desired target voltage is 5 V, Register Setting Value =  $5 \times (255 / 42.67) = 29.88$ . Hence, setting a value of 30 (or 1Eh) outputs approximately 5 V.

注

1. In practice, the driver's Over Voltage Protection shuts the device down before 42.67 V.
2. The maximum voltage for VM under [セクション 6.3](#) is 38 V.
  - a. Recommended to set the target voltage below 38 V for better accuracy.
3. To set the target voltage to 38 V, set **WSET\_VSET** to 227.

### 7.3.7.2.2 Speed Scaling Factor

Denoted by W\_SCALE, this is a scaling factor which helps in setting the target ripple speed when speed regulation mode is enabled. Settings for W\_SCALE are shown below. This register also sets the maximum value of ripple speed under each setting of W\_SCALE.

**表 7-21. Settings for W\_SCALE**

Bit	W_SCALE	Maximum Ripple Speed
00b	16	4080 rad/s
01b	32	8160 rad/s
10b	64	16320 rad/s
11b	128	32640 rad/s

Example setting for W\_SCALE: If **SPEED** register = 15, W\_SCALE = 01b, then the actual ripple speed =  $15 \times 32 = 480$  rad/s.

#### 注

Explanation for Maximum Ripple Speed: W\_SCALE inadvertently sets the upper limit for the target ripple speed under that setting of W\_SCALE. For example, if W\_SCALE = 00b, then the maximum ripple speed under this setting =  $255 \times 16$  rad/s = 4080 rad/s. Hence, the maximum target speed achievable under this setting is 4080 rad/s. Furthermore, under this setting of W\_SCALE, FFh corresponds to 4080 rad/s for WSET\_VSET when speed regulation mode is activated (**REG\_CTRL**=10b).

### 7.3.7.3 Soft-Start and Soft-Stop

The DRV8234 integrates a soft-start and stop feature to safeguard the device from high inrush currents during start up. This feature can be activated by setting the EN\_SS bit to 1b when the **REG\_CTRL** register is set to 10b (Speed Regulation) or 11b (Voltage Regulation). If speed or voltage regulation modes are inactive, the EN\_SS bit has no influence on the device performance.

Soft-start comes into effect during motor start up. The motor current is slowly ramped up to the current value corresponding to the target speed over the duration of  $t_{\text{INRUSH}}$  time. The inrush time  $t_{\text{INRUSH}}$  can be set by the user via the 16-bit **TINRUSH** register. During this time  $t_{\text{INRUSH}}$ , the FETs are internally PWMed with a duty cycle generated using the PI control loop.

Soft-stop results in a slow ramp down of motor current in time  $t_{\text{INRUSH}}$ . This can be triggered by the following methods:

1. The direction of rotation is changed on-the-fly. The soft stop function prevents a high current build-up through the motor windings by ramping down the current slowly and performing soft-start on the other direction.
2. Setting I2C\_EN\_IN1 and I2C\_PH\_IN2 to 0. Please note that this method sets outputs to Hi-Z after triggering soft stop, which deviates from conventional device operation where setting inputs to 0 causes the device to immediately go Hi-Z and enter coast mode.
3. Set WSET\_VSET to 0x00.

A reference [block diagram](#) containing the PI loop can be found in [セクション 7.3.7](#). [図 7-16](#) shows the motor current slow ramp up at start up and ramp down at motor stop within time  $t_{\text{INRUSH}}$ .

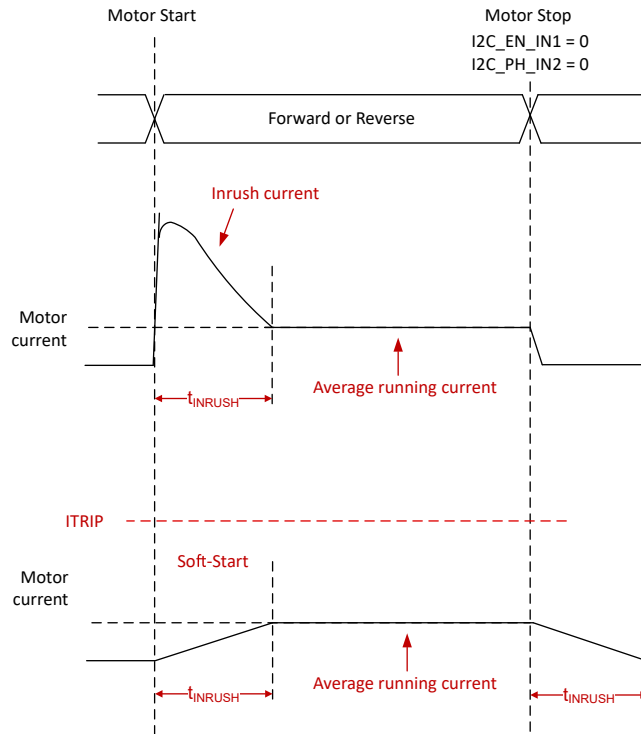


图 7-16. Soft Start and Soft Stop

### 7.3.7.3.1 $T_{\text{INRUSH}}$

The inrush time,  $t_{\text{INRUSH}}$ , is set using the 16-bit [TINRUSH](#) register. As described earlier,  $t_{\text{INRUSH}}$  has a dual purpose:

1.  $t_{\text{INRUSH}}$  is duration of time for which the stall detection scheme ignores the motor inrush current. This prevents false detection of stall during start up. Stall detection is blanked for this duration of time. A detailed description can be found in the [Stall Detection](#) section.
2. Additionally,  $t_{\text{INRUSH}}$  is also the duration of time for which the soft-start and stop feature ramps up the speed or voltage from 0 to a value set by [WSET\\_VSET](#), or ramps down the speed or voltage from the existing value to 0.
  - a. When [EN\\_SS](#) is set to 0b, the [TINRUSH](#) register bit settings directly reflect the  $t_{\text{INRUSH}}$  time. Time  $t_{\text{INRUSH}}$  can be set to a value between 5 ms (0000h) and 6.7 s (FFFFh). Default value is 1 s.
  - b. When [EN\\_SS](#) is set to 1b during motor speed or voltage regulation mode, the target motor speed or voltage is soft-started and stopped over the duration of  $t_{\text{INRUSH}}$  as describe above. In this case,  $t_{\text{INRUSH}} = \text{TINRUSH} \times \text{WSET\_VSET}$ . As an example, if [WSET\\_VSET](#) = 10 and intended  $t_{\text{INRUSH}}$  time is 1 s, then [TINRUSH](#) is to be set to 100 ms.

## 7.3.8 Protection Circuits

The DRV8234 is fully protected against supply undervoltage, overcurrent, and overtemperature events. In addition, the device supports overvoltage protection in sleep mode and when the H-bridge is disabled.

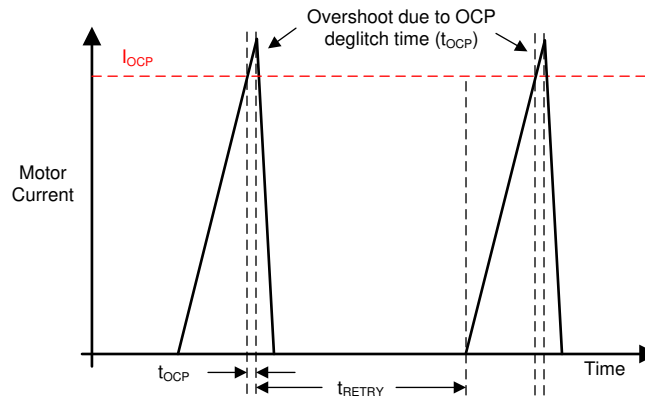
### 7.3.8.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this analog current limit persists for longer than the OCP deglitch time ( $t_{\text{OCP}}$ ), all FETs in the H-bridge will disable, [FAULT](#) and [OCP](#) bits become 1b and [nFAULT](#) is pulled low.

The [OCP\\_MODE](#) bit programs the response of the device to overcurrent event. The device can either latch-off or perform automatic retry to recover from an overcurrent event.



In automatic retry mode, the MOSFETs will be disabled and the nFAULT pin driven low for a duration of  $t_{RETRY}$ . After  $t_{RETRY}$ , the MOSFETs are re-enabled according to the control inputs. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes. This is explained by the following diagram -



**図 7-17. OCP Operation**

In latch-off mode, the MOSFETs will remain disabled and the nFAULT pin will be driven low until the device is reset by a CLR\_FLT command or by cycling the VM power supply.

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for current regulation, so it functions regardless of VREF and IPROPI settings.

### 7.3.8.2 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown temperature threshold ( $T_{TSD}$ ), all FETs in the H-bridge are disabled, TSD and FAULT bits become 1b, and nFAULT is pulled low. The TSD\_MODE bit programs the response of the device to overtemperature event. The device can either latch-off or perform automatic retry to recover from overtemperature.

In automatic retry mode, normal operation will resume (driver operation starts, nFAULT is released and FAULT bit changes to 0b) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ( $T_{TSD} - T_{HYS}$ ). The TSD bit remains at 1b indicating that a thermal shutdown event occurred until a CLR\_FLT command is issued.

In latch-off mode, once the overtemperature condition is removed, normal operation resumes after sending a CLR\_FLT command, or a power cycling.

### 7.3.8.3 VM Undervoltage Lockout (VM UVLO)

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage:

- All the outputs are disabled (High-Z)
- The internal charge pump is disabled
- nFAULT is driven low

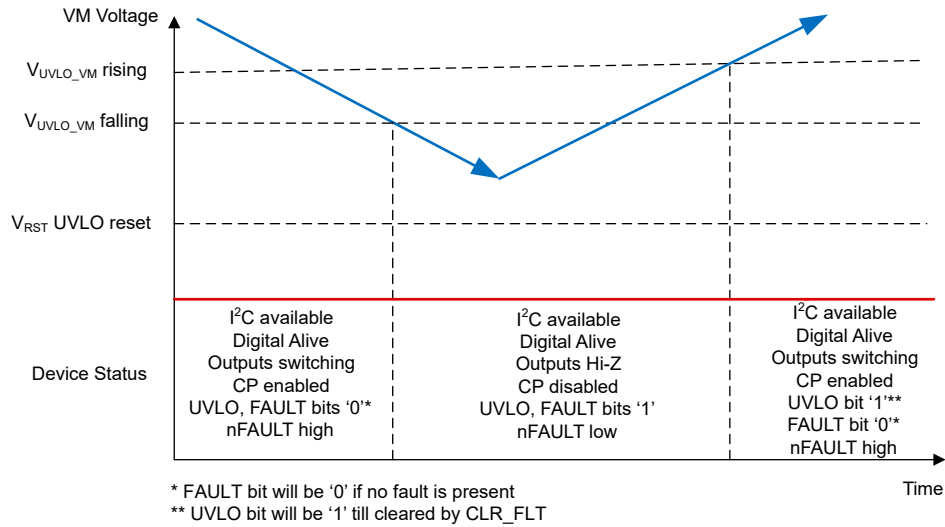
Normal operation resumes when the VM voltage recovers above the UVLO rising threshold.

If the voltage on the VM pin falls below the UVLO falling threshold voltage, but is above the  $V_{RST}$ :

- I<sup>2</sup>C communication is available and the digital core of the device is active
- The FAULT and UVLO bits are made high
- The nFAULT pin is driven low

From this condition, if the VM voltage recovers above the UVLO rising threshold voltage:

- nFAULT pin is released (is pulled-up to the external voltage)
- The FAULT bit is reset
- The UVLO bit remains latched high until cleared through the CLR\_FLT command.



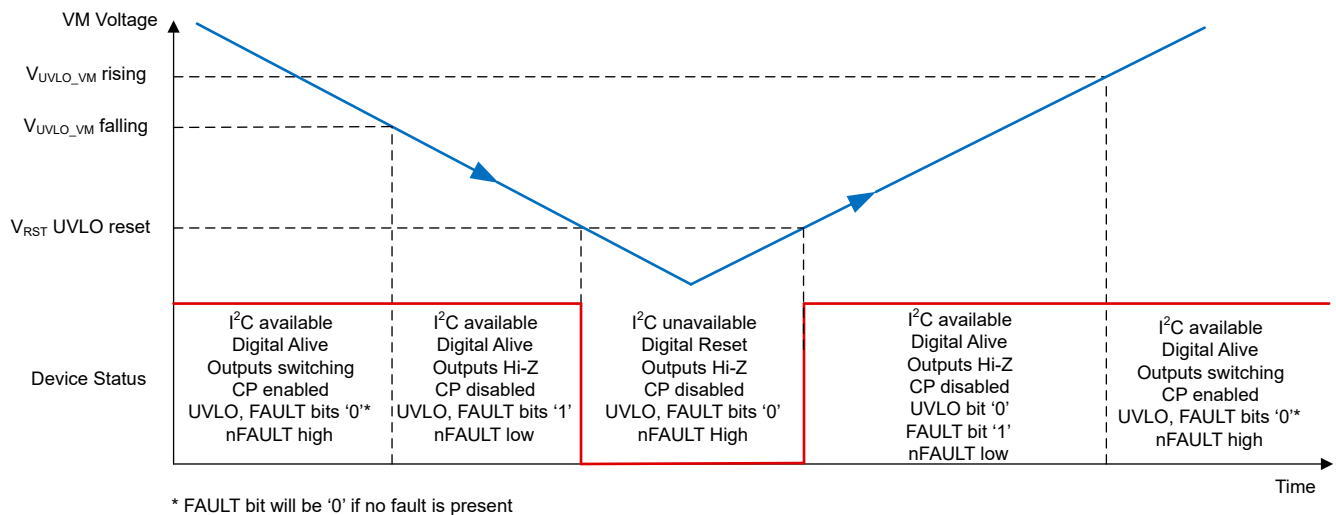
**図 7-18. Supply Voltage Ramp Profile**

When the voltage on the VM pin falls below the  $V_{RST}$ :

- I<sup>2</sup>C communication is unavailable and the digital core is shutdown
- The FAULT and UVLO bits are low
- The nFAULT pin is high

During a subsequent power-up, when the VM voltage exceeds the  $V_{RST}$  voltage:

- The digital core comes alive
- UVLO bit stays low
- The FAULT bit is made high
- The nFAULT pin is pulled low
- When the VM voltage exceeds the VM UVLO rising threshold
  - FAULT bit is reset
  - UVLO bit stays low
  - nFAULT pin is pulled high.



**図 7-19. Supply Voltage Ramp Profile**

### 7.3.8.4 Overvoltage Protection (OVP)

When the motor is driven by external force, it acts as a generator and pumps back current to the supply voltage rail. This can potentially damage other circuits connected to the supply rail. In low-power sleep mode or when the H-bridge is disabled (High-Z), if the voltage of the output nodes rise above the supply voltage by about 200 mV, the DRV8234 turns on the two low-side MOSFETs. This allows the device to actively brake a motor connected to the outputs by shorting the back emf across the motor terminals.

The overvoltage protection (OVP) function is enabled by default. After power-up, the EN\_OVP bit can be made 0b to disable this feature. The EN\_OVP logic state is latched, so that in sleep mode the device behaves as per the EN\_OVP bit setting, even though the internal digital logic is reset.

In sleep mode, if there is a short circuit to power supply fault present in the power stage, a simple overcurrent detector circuit is provided to disable the low-side MOSFET if a high current event is detected while braking. This is needed since the normal overcurrent protection circuits are disabled during the low-power sleep mode.

### 7.3.8.5 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. nFAULT pin will be high after power-up. When a fault is detected, the nFAULT pin will be logic low.

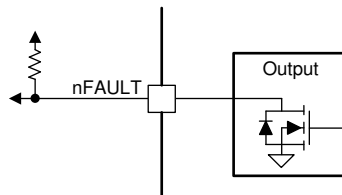


図 7-20. nFAULT Pin

## 7.4 Device Functional Modes

The following table summarizes the DRV8234 functional modes described in this section.

表 7-22. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	nSLEEP = 1, EN_OUT = 1b	Operating	Operating
Low-Power Sleep Mode	nSLEEP = 0	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See Fault Mode section

### 7.4.1 Active Mode

After the supply voltage on the VM pin has crossed the rising undervoltage threshold, if nSLEEP is logic high and  $t_{WAKE}$  has elapsed, and if the EN\_OUT bit is 1b, the device enters active mode. In this mode, the full-bridge, and internal logic are active and the device is ready to receive inputs.

### 7.4.2 Low-Power Sleep Mode

When the nSLEEP pin is low for  $t_{TURNOFF}$  time, the DRV8234 enters a low-power sleep mode. In sleep mode, the outputs remain High-Z and the device draws minimal current from the supply pin. After nSLEEP is set high for longer than the duration of  $t_{WAKE}$ , the device becomes fully operational.

### 7.4.3 Fault Mode

The DRV8234 enters fault mode when it encounters a fault condition. This protects the device and the load on the outputs. 表 7-23 describes the device behavior in the fault mode which depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the system meets the recovery condition.

表 7-23. Fault Conditions Summary

FAULT	FAULT CONDITION	CONFIGURATION	ERROR REPORT	FULL-BRIDGE	INTERNAL CIRCUITS	RECOVERY CONDITION
VM undervoltage (VM UVLO)	$V_{VM} < V_{UVLO\_VM}$	–	nFAULT / I <sup>2</sup> C	Disabled	Disabled	$V_{VM} > V_{UVLO\_VM}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	OCP_MODE = 0b	nFAULT / I <sup>2</sup> C	Disabled	Operating	Latched: CLR_FLT
		OCP_MODE = 1b	nFAULT / I <sup>2</sup> C	Disabled	Operating	Automatic retry: t <sub>RETRY</sub>
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	TSD_MODE = 0b	nFAULT / I <sup>2</sup> C	Disabled	Operating	Latched: CLR_FLT
		TSD_MODE = 1b	nFAULT / I <sup>2</sup> C	Disabled	Operating	Automatic: $T_J < T_{TSD} - T_{HYS}$
Overvoltage protection (OVP)	OUTx = Hi-Z or nSLEEP = 0; $V_{VOUT} - V_{VM} > V_{SD}$	–	I <sup>2</sup> C when OUTx = Hi-Z	Disabled	Disabled	Automatic: $V_{VOUT} - V_{VM} < V_{SD}$

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C Communication

The I<sup>2</sup>C interface allows control and monitoring of the DRV8234 by a microcontroller. The I<sup>2</sup>C bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A leader device, usually a microcontroller or a digital signal processor, controls the bus. The leader is responsible for generating the SCL signal and device addresses. The leader also generates specific conditions that indicate the START and STOP of data transfer. A follower device receives and/or transmits data on the bus under control of the leader device. DRV8234 is a follower device.

The lower four bits of the device address are derived from the inputs from the pins A1 and A0, which can be tied to board level power supply for logic high, GND for logic low, or left open. These four address bits are latched into the device at power up, so cannot be changed dynamically. The upper address bits of the device address are fixed at 0x60h, so the device address is as follows -

表 7-24. Device Addresses

A1 Pin	A0 Pin	A3A2A1A0 bits	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000b	0x60h	0x61h
0	High-Z	0001b	0x62h	0x63h
0	1	0010b	0x64h	0x65h
High-Z	0	0011b	0x66h	0x67h
High-Z	High-Z	0100b	0x68h	0x69h
High-Z	1	0101b	0x6Ah	0x6Bh
1	0	0110b	0x6Ch	0x6Dh
1	High-Z	0111b	0x6Eh	0x6Fh
1	1	1000b	0x70h	0x71h

Using the A0 and A1 pins, up to 9 DRV8234 follower devices can be controlled by one I<sup>2</sup>C bus. The DRV8234 does not respond to the general call address. It is recommended to use a 2.2kΩ pull-up resistor for these pins.

#### 7.5.1.1 I<sup>2</sup>C Write

To write on the I<sup>2</sup>C bus, the leader device sends a START condition on the bus with the address of the 7-bit follower device. Also, the last bit (the R/W bit) is set to 0b, which signifies a write. After the follower sends the

acknowledge bit, the leader device then sends the register address of the register to be written. The follower device sends an acknowledge (ACK) signal again which notifies the leader device that the follower device is ready. After this process, the leader device sends 8-bit write data and terminates the transmission with a STOP condition.

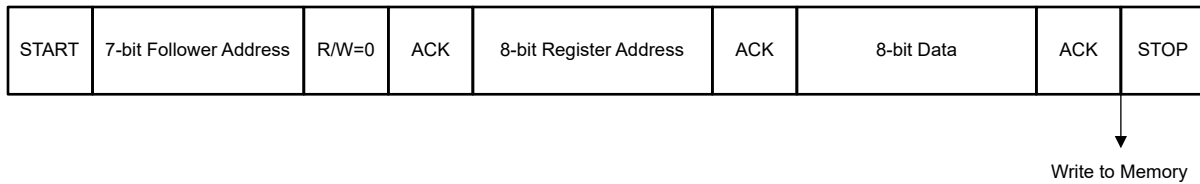


図 7-21. I<sup>2</sup>C Write Sequence

### 7.5.1.2 I<sup>2</sup>C Read

To read from a follower device, the leader device must first communicate to the follower device which register will be read from. This communication is done by the leader starting the transmission similarly to the write process which is by setting the address with the R/W bit equal to 0b (signifying a write). The leader device then sends the register address of the register to be read from. When the follower device acknowledges this register address, the leader device sends a START condition again, followed by the follower address with the R/W bit set to 1b (signifying a read). After this process, the follower device acknowledges the read request and the leader device releases the SDA bus, but continues supplying the clock to the follower device.

During this part of the transaction, the leader device becomes the leader-receiver, and the follower device becomes the follower-transmitter. The leader device continues sending out the clock pulses, but releases the SDA line so that the follower device can transmit data. At the end of the byte, the leader device sends a negative-acknowledge (NACK) signal, signaling to the follower device to stop communications and release the bus. The leader device then sends a STOP condition.

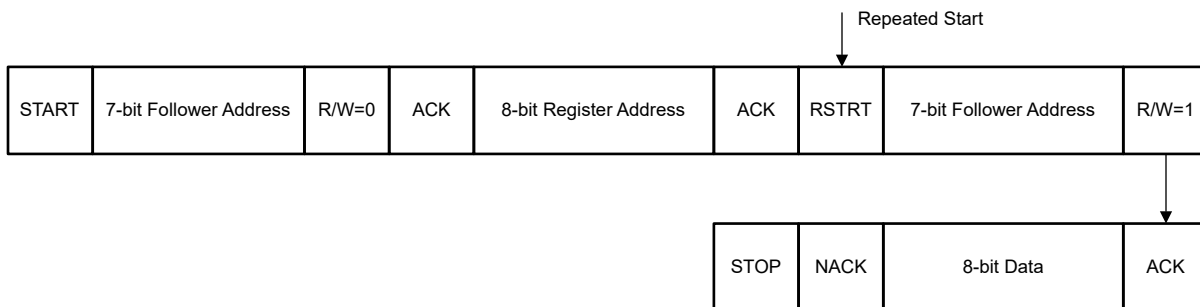


図 7-22. I<sup>2</sup>C Read Sequence

## 7.6 Register Map

The following table lists the memory-mapped I<sup>2</sup>C registers for the DRV8234. The I<sup>2</sup>C registers are used to configure the DRV8234 and for device diagnostics.

### 注

Do not modify reserved registers or addresses not listed in the register map (表 7-25). Writing to these registers can have unintended effects. For all reserved bits, the default value is 0b.

表 7-25. I<sup>2</sup>C Registers

Address	Name	7	6	5	4	3	2	1	0	Access
0x00	FAULT	FAULT	RSVD	STALL	OCF	OVP	TSD	NPOR	CNT_DONE	R

表 7-25. I<sup>2</sup>C Registers (続き)

Address	Name	7	6	5	4	3	2	1	0	Access	
0x01	RC_STATUS1	SPEED[7:0]								R	
0x02	RC_STATUS2	RC_CNT[7:0]								R	
0x03	RC_STATUS3	RC_CNT[15:8]								R	
0x04	REG_STATUS1	VMTR[7:0]								R	
0x05	REG_STATUS2	IMTR[7:0]								R	
0x06	REG_STATUS3	RSVD		IN_DUTY[5:0]						R	
0x09	CONFIG0	EN_OUT	EN_OVP	EN_STAL L	VSNS_S EL*	RSVD	CLR_CN T	CLR_FLT	DUTY_C TRL*	RW	
0x0A	CONFIG1	TINRUSH[7:0]								RW	
0x0B	CONFIG2	TINRUSH[15:8]								RW	
0x0C	CONFIG3	IMODE[1:0]*		SMODE*	INT_VRE F*	TBLANK*	TDEG*	OCP_MO DE*	TSD_MO DE*	RW	
0x0D	CONFIG4	RC_REP[1:0]		STALL_R EP	CBC_RE P	PMODE*	I2C_BC*	I2C_EN_I N1	I2C_PH_I N2	RW	
0x0E	REG_CTRL0	RSVD		EN_SS	REG_CTRL[1:0]*		PWM_FR EQ*	W_SCALE[1:0]		RW	
0x0F	REG_CTRL1	WSET_VSET[7:0]								RW	
0x10	REG_CTRL2	OUT_FLT[1:0]		EXT_DUTY[5:0]						RW	
0x11	RC_CTRL0	EN_RC	DIS_EC	RC_HIZ	FLT_GAIN_SEL[1:0]		CS_GAIN_SEL[2:0]			RW	
0x12	RC_CTRL1	RC_THR[7:0]								RW	
0x13	RC_CTRL2	INV_R_SCALE[1:0]		KMC_SCALE[1:0]		RC_THR_SCALE[1: 0]		RC_THR[9:8]		RW	
0x14	RC_CTRL3	INV_R[7:0]								RW	
0x15	RC_CTRL4	KMC[7:0]								RW	
0x16	RC_CTRL5	FLT_K[3:0]				RSVD					RW
0x17	RC_CTRL6	EC_PUL SE_DIS	T_MECH_FLT			EC_FALSE_PER		EC_MISS_PER		RW	
0x18	RC_CTRL7	KP_DIV[2:0]			KP[4:0]					RW	
0x19	RC_CTRL8	KI_DIV[2:0]			KI[4:0]					RW	

注

\*Writable only when EN\_OUT=0.

表 7-26. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.1 DRV8234\_STATUS Registers

表 7-27 lists the memory-mapped registers for the DRV8234\_STATUS registers. All register offset addresses not listed in 表 7-27 should be considered as reserved locations and the register contents should not be modified.

**表 7-27. DRV8234\_STATUS Registers**

Offset	Acronym	Register Name	Section
0h	FAULT	Various fault registers' status.	<a href="#">セクション 7.6.1.1</a>
1h	RC_STATUS1	Ripple Counting Status Registers - 1.	<a href="#">セクション 7.6.1.2</a>
2h	RC_STATUS2	Ripple Counting Status Registers - 2.	<a href="#">セクション 7.6.1.3</a>
3h	RC_STATUS3	Ripple Counting Status Registers - 3.	<a href="#">セクション 7.6.1.4</a>
4h	REG_STATUS1	Regulation Status Registers - (1/3).	<a href="#">セクション 7.6.1.5</a>
5h	REG_STATUS2	Regulation Status Registers - (2/3).	<a href="#">セクション 7.6.1.6</a>
6h	REG_STATUS3	Regulation Status Registers - (3/3).	<a href="#">セクション 7.6.1.7</a>

Complex bit access types are encoded to fit into small table cells. 表 7-28 shows the codes that are used for access types in this section.

**表 7-28. DRV8234\_STATUS Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.1.1 FAULT Register (Offset = 0h) [Reset = 00h]

FAULT is shown in [表 7-29](#).

Return to the [Summary Table](#).

Status of various fault and protection bits.

**表 7-29. FAULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	FAULT	R	0h	0b during normal operation, 1b during a fault condition. nFAULT pin is pulled down when FAULT bit is 1b. nFAULT pin is released during normal operation.
6	RSVD	R	0h	Reserved.
5	STALL	R	0h	When this bit is 1b, it indicates motor stall.
4	OCP	R	0h	0b during normal operation, 1b if OCP event occurs.
3	OVP	R	0h	0b during normal operation, 1b if OVP event occurs.
2	TSD	R	0h	0b during normal operation, 1b if TSD event occurs.
1	NPOR	R	0h	Reset and latched low if VM>VUVLO. Remains reset until the CLR_FLT bit is set to issue a clear fault command. After power up, automatically latched high once CLR_FLT command is issued. Refer to <a href="#">セクション 7.3.8.3</a> for further explanation.
0	CNT_DONE	R	0h	Status flag. Latched high when RC_CNT exceeds the ripple counting threshold. Can be cleared by CLR_CNT command.



### 7.6.1.2 RC\_STATUS1 Register (Offset = 1h) [Reset = 00h]

RC\_STATUS1 is shown in [表 7-30](#).

Return to the [Summary Table](#).

Speed estimated by the ripple counting algorithm.

**表 7-30. RC\_STATUS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	SPEED	R	0h	Outputs the motor speed estimated by the ripple counting algorithm.

### 7.6.1.3 RC\_STATUS2 Register (Offset = 2h) [Reset = 00h]

RC\_STATUS2 is shown in [表 7-31](#).

Return to the [Summary Table](#).

Output corresponding to number of current ripples (1/2).

**表 7-31. RC\_STATUS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RC_CNT_7:0	R	0h	Lower half 8-bit output out of the 16-bit output of the ripple counter corresponding to the number of current ripples.

#### 7.6.1.4 RC\_STATUS3 Register (Offset = 3h) [Reset = 00h]

RC\_STATUS3 is shown in [表 7-32](#).

Return to the [Summary Table](#).

Output corresponding to number of current ripples (2/2).

**表 7-32. RC\_STATUS3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RC_CNT_15:8	R	0h	Upper half 8-bit output out of the 16-bit output of the ripple counter corresponding to the number of current ripples.

### 7.6.1.5 REG\_STATUS1 Register (Offset = 4h) [Reset = 00h]

REG\_STATUS1 is shown in [表 7-33](#).

Return to the [Summary Table](#).

Value corresponding to the output voltage across the motor terminals.

**表 7-33. REG\_STATUS1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	VMTR	R	0h	Outputs the voltage across the motor terminals, maximum value FFh. 00h corresponds to 0 V and E4h corresponds to 38 V.

### 7.6.1.6 REG\_STATUS2 Register (Offset = 5h) [Reset = 00h]

REG\_STATUS2 is shown in [表 7-34](#).

Return to the [Summary Table](#).

Output corresponding to current flowing through the motor.

**表 7-34. REG\_STATUS2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	IMTR	R	0h	Outputs the current flowing through the motor. 00h corresponds to 0 A and C0h corresponds to the maximum value set by the CS_GAIN_SEL bits.

### 7.6.1.7 REG\_STATUS3 Register (Offset = 6h) [Reset = 00h]

REG\_STATUS3 is shown in [表 7-35](#).

Return to the [Summary Table](#).

Internal pwm duty cycle and device id.

**表 7-35. REG\_STATUS3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0h	Reserved.
5-0	IN_DUTY	R	0h	Represents the bridge control duty cycle generated by an internal regulation logic. This register is applicable when speed or voltage regulation is activated. When speed or voltage regulation is inactive, set DUTY_CTRL to 1b and program the duty cycle in EXT_DUTY explained later. The range of duty cycle is 0% (000000b) to 100% (111111b). Refer to <a href="#">セクション 7.3.7.1</a> for further explanation on the internal PWM generation scheme.

## 7.6.2 DRV8234\_CONFIG Registers

表 7-36 lists the memory-mapped registers for the DRV8234\_CONFIG registers. All register offset addresses not listed in 表 7-36 should be considered as reserved locations and the register contents should not be modified.

**表 7-36. DRV8234\_CONFIG Registers**

Offset	Acronym	Register Name	Section
9h	CONFIG0	Configuration Registers - Faults (1/5).	<a href="#">セクション 7.6.2.1</a>
Ah	CONFIG1	Configuration Registers - (2/5).	<a href="#">セクション 7.6.2.2</a>
Bh	CONFIG2	Configuration Registers - (3/5).	<a href="#">セクション 7.6.2.3</a>
Ch	CONFIG3	Configuration Registers - (4/5).	<a href="#">セクション 7.6.2.4</a>
Dh	CONFIG4	Configuration Registers - (5/5).	<a href="#">セクション 7.6.2.5</a>

Complex bit access types are encoded to fit into small table cells. 表 7-37 shows the codes that are used for access types in this section.

**表 7-37. DRV8234\_CONFIG Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.2.1 CONFIG0 Register (Offset = 9h) [Reset = 60h]

CONFIG0 is shown in [表 7-38](#).

Return to the [Summary Table](#).

Enable/Disable various faults like OCP, OVP, STALL, etc.

**表 7-38. CONFIG0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	EN_OUT	R/W	0h	0b: All driver FETs are Hi-Z. 1b: Enables the driver outputs.
6	EN_OVP	R/W	1h	Enables the OVP feature. 1b by default, can be made 0b after power-up to disable the OVP feature. Refer to <a href="#">セクション 7.3.8.4</a> for further explanation.
5	EN_STALL	R/W	1h	Enables the Stall Detection feature. Stall detection feature can be disabled by setting this bit to 0b. Refer to EN_STALL configuration under <a href="#">セクション 7.3.5</a> for further explanation.
4	VSNS_SEL	R/W	0h	0b: Use the analog low-pass filter to average out the output voltage for voltage regulation. Refer to OUT_FLT for further description of the analog low-pass filter. 0b is the recommended value. 1b: Use the digital low-pass filter for voltage regulation. This option performs multiplication of the duty cycle with VM to obtain the output voltage.
3	RSVD	R	0h	Reserved
2	CLR_CNT	R/W	0h	Resets the ripple counter to 0, and resets CNT_DONE. Also releases nFAULT when RC_REP = 10b. CLR_CNT is automatically reset.
1	CLR_FLT	R/W	0h	Clears all latched faults when set to 1b. CLR_FLT is automatically reset.
0	DUTY_CTRL	R/W	0h	When speed regulation is disabled and the DUTY_CTRL bit is 1b, user can write desired PWM duty to EXT_DUTY bits. The range of duty is 0% (000000b) to 100% (111111b).



### 7.6.2.2 CONFIG1 Register (Offset = Ah) [Reset = 00h]

CONFIG1 is shown in [表 7-39](#).

Return to the [Summary Table](#).

Configure the inrush time (1/2).

**表 7-39. CONFIG1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	TINRUSH_7:0	R/W	0h	Lower half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to <a href="#">セクション 7.3.7.3.1</a> for further explanation.

### 7.6.2.3 CONFIG2 Register (Offset = Bh) [Reset = 00h]

CONFIG2 is shown in [表 7-40](#).

Return to the [Summary Table](#).

Configure the inrush time (2/2).

**表 7-40. CONFIG2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	TINRUSH_15:8	R/W	0h	Upper half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to <a href="#">セクション 7.3.7.3.1</a> for further explanation.

#### 7.6.2.4 CONFIG3 Register (Offset = Ch) [Reset = 63h]

CONFIG3 is shown in [表 7-41](#).

Return to the [Summary Table](#).

Enable/Disable various device modes like IMODE, SMODE and parameters like blanking time.

**表 7-41. CONFIG3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	IMODE	R/W	1h	Determines the behavior of current regulation. Refer to IMODE configuration under <a href="#">セクション 7.3.4.2</a> for further explanation.
5	SMODE	R/W	1h	Programs device response to a stall condition. Refer to SMODE configuration under <a href="#">セクション 7.3.5</a> for further explanation.
4	INT_VREF	R/W	0h	If set to 1b, sets VREF voltage to 3 V internally. Voltage is not fixed if INT_VREF is set to 0b. Refer to <a href="#">セクション 7.3.5</a> for further explanation.
3	TBLANK	R/W	0h	Sets the current sense blanking time. If set to 0b, $t_{BLANK}=1.8\mu s$ . If set to 1b, $t_{BLANK}=1.0\mu s$ .
2	TDEG	R/W	0h	Sets the current regulation and stall detection deglitch time. If set to 0b, $t_{DEG}=2\mu s$ . If set to 1b, $t_{DEG}=1\mu s$ .
1	OCP_MODE	R/W	1h	Programs device response to an overcurrent event. If set to 0b, device is latched off in case of an OCP event. Can be cleared using CLR_FLT. If set to 1b, device performs auto-retry after time $t_{retry}$ in case of an OCP event. Refer to <a href="#">セクション 7.3.8.1</a> for further explanation.
0	TSD_MODE	R/W	1h	Programs device response to an overtemperature event. If set to 0b, device is latched off in case of a TSD event. If set to 1b, device performs auto-retry when $T_J < T_{TSD} - T_{HYS}$ .

### 7.6.2.5 CONFIG4 Register (Offset = Dh) [Reset = 38h]

CONFIG4 is shown in [表 7-42](#).

Return to the [Summary Table](#).

Configure the report registers like RC\_REP and STALL\_REP.

**表 7-42. CONFIG4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RC_REP	R/W	0h	Determines whether nFAULT is pulled low when RC_CNT exceeds threshold, and the behavior of RC_CNT when it reaches maximum value of $(2^{16}-1)$ . Refer to RC_REP Settings under <a href="#">セクション 7.3.6.3</a> for further explanation.
5	STALL_REP	R/W	1h	Determines whether stall is reported on the nFAULT pin. When set to 1b, nFAULT is low whenever stall is detected. When set to 0b, stall is not reported on nFAULT output. Refer to <a href="#">セクション 7.3.5</a> for further explanation.
4	CBC_REP	R/W	1h	When REG_CTRL is set to 01b, the device enters cycle-by-cycle mode of current regulation. In this mode, the device can indicate whenever the H-bridge enters internal current regulation. CBC_REP bit is used to determine device outputs' behavior in the cycle-by-cycle mode. 1b: nFAULT is pulled low when H-Bridge enters internal current regulation. 0b: nFAULT is not pulled low when H-Bridge enters internal current regulation. Refer to <a href="#">セクション 7.3.4.2.2</a> for further explanation.
3	PMODE	R/W	1h	Switch between phase/enable mode and PWM mode. 0b: PH/EN. 1b: PWM.
2	I2C_BC	R/W	0h	Decides the H-Bridge Control Interface. 0b: Bridge control configured by INx pins. 1b: Bridge control configured by I2C bits I2C_EN_IN1 and I2C_PH_IN2.
1	I2C_EN_IN1	R/W	0h	Enable/PWM Input Bit 1 for internal bridge control. Used when I2C_BC=1b. Ignored when I2C_BC=0b.
0	I2C_PH_IN2	R/W	0h	Phase/PWM Input Bit 2 for internal bridge control. Used when I2C_BC=1b. Ignored when I2C_BC=0b.

### 7.6.3 DRV8234\_CTRL Registers

表 7-43 lists the memory-mapped registers for the DRV8234\_CTRL registers. All register offset addresses not listed in 表 7-43 should be considered as reserved locations and the register contents should not be modified.

**表 7-43. DRV8234\_CTRL Registers**

Offset	Acronym	Register Name	Section
Eh	REG_CTRL0	Regulation control registers (1/3).	<a href="#">セクション 7.6.3.1</a>
Fh	REG_CTRL1	Regulation control registers (2/3).	<a href="#">セクション 7.6.3.2</a>
10h	REG_CTRL2	Regulation control registers (3/3).	<a href="#">セクション 7.6.3.3</a>
11h	RC_CTRL0	Ripple Counting Control Registers - (1/9).	<a href="#">セクション 7.6.3.4</a>
12h	RC_CTRL1	Ripple Counting Control Registers - (2/9).	<a href="#">セクション 7.6.3.5</a>
13h	RC_CTRL2	Ripple Counting Control Registers - (3/9).	<a href="#">セクション 7.6.3.6</a>
14h	RC_CTRL3	Ripple Counting Control Registers - (4/9).	<a href="#">セクション 7.6.3.7</a>
15h	RC_CTRL4	Ripple Counting Control Registers - (5/9).	<a href="#">セクション 7.6.3.8</a>
16h	RC_CTRL5	Ripple Counting Control Registers - (6/9).	<a href="#">セクション 7.6.3.9</a>
17h	RC_CTRL6	Ripple Counting Control Registers - (7/9).	<a href="#">セクション 7.6.3.10</a>
18h	RC_CTRL7	Ripple Counting Control Registers - (8/9).	<a href="#">セクション 7.6.3.11</a>
19h	RC_CTRL8	Ripple Counting Control Registers - (9/9).	<a href="#">セクション 7.6.3.12</a>

Complex bit access types are encoded to fit into small table cells. 表 7-44 shows the codes that are used for access types in this section.

**表 7-44. DRV8234\_CTRL Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.6.3.1 REG\_CTRL0 Register (Offset = Eh) [Reset = 27h]

REG\_CTRL0 is shown in [表 7-45](#).

Return to the [Summary Table](#).

Set features like Soft Start/Stop, speed scaling factor, etc.

**表 7-45. REG\_CTRL0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0h	Reserved.
5	EN_SS	R/W	1h	Used to enable/disable soft start/stop. 1b: Target motor voltage or speed is soft-started and soft-stopped over the duration of $t_{INRUSH}$ time. 0b: Soft-start/stop feature is disabled. Refer to <a href="#">セクション 7.3.7.3</a> for further explanation.
4-3	REG_CTRL	R/W	0h	Selects the current regulation scheme (fixed off-time or cycle-by-cycle) or motor speed and voltage regulation. 00b: Fixed Off-Time Current Regulation. 01b: Cycle-By-Cycle Current Regulation. 10b: Motor speed is regulated. Ripple counting must be enabled in this mode by setting EN_RC to 1b. 11b: Motor voltage is regulated. Refer to <a href="#">セクション 7.3.4.2</a> for further explanation.
2	PWM_FREQ	R/W	1h	Sets the PWM frequency when bridge control is configured by INx bits (I2C_BC=1b). 0b: PWM frequency is set to 50kHz. 1b: PWM frequency is set to 25kHz.
1-0	W_SCALE	R/W	3h	Scaling factor that helps in setting the target ripple speed. 00b: 16 01b: 32 10b: 64 11b: 128 Refer to <a href="#">セクション 7.3.7.2.2</a> for further explanation.

### 7.6.3.2 REG\_CTRL1 Register (Offset = Fh) [Reset = FFh]

REG\_CTRL1 is shown in [表 7-46](#).

Return to the [Summary Table](#).

Set the target motor voltage and speed.

**表 7-46. REG\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	WSET_VSET	R/W	FFh	Sets the target motor voltage or ripple speed. A detailed explanation is provided in <a href="#">セクション 7.3.7.2.1</a> .

### 7.6.3.3 REG\_CTRL2 Register (Offset = 10h) [Reset = 00h]

REG\_CTRL2 is shown in [表 7-47](#).

Return to the [Summary Table](#).

Set the duty cycle and cut-off frequency for output voltage filtering.

**表 7-47. REG\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	OUT_FLT	R/W	0h	Programs the cut-off frequency of the output voltage filtering. 00b: 250Hz 01b: 500Hz 10b: 750Hz 11b: 1000Hz For best results, choose a cut-off frequency equal to a value at least 20 times lower than the PWM frequency. Eg, if you PWM at 20kHz, OUT_FLT=11b (1000Hz) is sufficient.
5-0	EXT_DUTY	R/W	0h	Available when using external bridge control (I2C_BC=0b). DUTY_CTRL must be set to 1b. Speed and voltage regulation modes are inactive in this case. User can program the desired duty cycle in the EXT_DUTY bits. The range of duty cycle is 0% (000000b) to 100% (111111b).



### 7.6.3.4 RC\_CTRL0 Register (Offset = 11h) [Reset = 88h]

RC\_CTRL0 is shown in [表 7-48](#).

Return to the [Summary Table](#).

Set various functions for RC including enable/disable.

**表 7-48. RC\_CTRL0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	EN_RC	R/W	1h	Enable/Disable Ripple Counting. 0b: Disable 1b: Enable
6	DIS_EC	R/W	0h	Enable/Disable the Error Correction module. 0b: Error Correction is enabled. 1b: Error Correction is disabled. Please note that this is different from the EC_PULSE_DIS described earlier.
5	RC_HIZ	R/W	0h	0b: H-bridge stays enabled when RC_CNT exceeds threshold. 1b: H-bridge is disabled (High-Z) when RC_CNT exceeds threshold.
4-3	FLT_GAIN_SEL	R/W	1h	Filter input scaling factor. This factor scales the magnitude of current ripples for ease of detection and algorithmic calculation by the Ripple Counter. The options are: 00b: 2 01b: 4 10b: 8 11b: 16 Refer to <a href="#">セクション 8.2.3.1.3.1.1</a> for further explanation.
2-0	CS_GAIN_SEL	R/W	0h	Used to select the current scaling options. Settings are as follows: X00b: 4 A X01b: 2 A X10b: 1 A X11b: 0.5 A

### 7.6.3.5 RC\_CTRL1 Register (Offset = 12h) [Reset = FFh]

RC\_CTRL1 is shown in [表 7-49](#).

Return to the [Summary Table](#).

Threshold for ripple counting.

**表 7-49. RC\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	RC_THR	R/W	FFh	Lower 8 bits of the 10-bit RC_THR Register. Threshold level to compare against the RC_CNT based on the expected time of motor actuation. Ripple counting threshold = RC_THR x RC_THR_SCALE

### 7.6.3.6 RC\_CTRL2 Register (Offset = 13h) [Reset = 7Fh]

RC\_CTRL2 is shown in [表 7-50](#).

Return to the [Summary Table](#).

Set values of various scaling parameters.

**表 7-50. RC\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	INV_R_SCALE	R/W	1h	Scaling factor for the INV_R parameter. 00b: INV_R_SCALE = 2 01b: INV_R_SCALE = 64 10b: INV_R_SCALE = 1024 11b: INV_R_SCALE = 8192 Refer to <a href="#">セクション 7.3.6.1.2</a> for further explanation.
5-4	KMC_SCALE	R/W	3h	Scaling factor for KMC parameter. 00b: KMC_SCALE = $24 \times 2^8$ 01b: KMC_SCALE = $24 \times 2^9$ 10b: KMC_SCALE = $24 \times 2^{12}$ 11b: KMC_SCALE = $24 \times 2^{13}$ Refer to <a href="#">セクション 7.3.6.1.3</a> for further explanation.
3-2	RC_THR_SCALE	R/W	3h	Scaling factor for RC_THR. 00b: RC_THR_SCALE = 2 01b: RC_THR_SCALE = 8 10b: RC_THR_SCALE = 16 11b: RC_THR_SCALE = 64
1-0	RC_THR_9:8	R/W	3h	Upper two bits of the 10-bit RC_THR Register. Threshold level to compare against RC_CNT based on the expected time of motor actuation. Ripple counting threshold = RC_THR x RC_THR_SCALE

### 7.6.3.7 RC\_CTRL3 Register (Offset = 14h) [Reset = 00h]

RC\_CTRL3 is shown in [表 7-51](#).

Return to the [Summary Table](#).

Set the INV\_R parameter.

**表 7-51. RC\_CTRL3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	INV_R	R/W	0h	User input based on motor coil resistance. $INV\_R = INV\_R\_SCALE / \text{Motor Resistance}$ . Must not be set to 0. Refer to <a href="#">セクション 7.3.6.1.1</a> for further explanation.

### 7.6.3.8 RC\_CTRL4 Register (Offset = 15h) [Reset = 00h]

RC\_CTRL4 is shown in [表 7-52](#).

Return to the [Summary Table](#).

Set the KMC parameter.

**表 7-52. RC\_CTRL4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	KMC	R/W	0h	Represents a proportional value of the motor back emf constant. $KMC = (K_V) / N_R * KMC\_SCALE$ . Refer to <a href="#">セクション 7.3.6.1.4</a> for further explanation.

### 7.6.3.9 RC\_CTRL5 Register (Offset = 16h) [Reset = 00h]

RC\_CTRL5 is shown in [表 7-53](#).

Return to the [Summary Table](#).

Set the filter damping constant.

**表 7-53. RC\_CTRL5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	FLT_K	R/W	0h	Bandpass filter 1/Q factor. Sets the bandwidth of the bandpass filter. Recommended value is the default value: 6d. Refer to <a href="#">セクション 8.2.3.1.3.1.2</a> for further explanation.
3-0	RSVD	R	0h	Reserved

### 7.6.3.10 RC\_CTRL6 Register (Offset = 17h) [Reset = 45h]

RC\_CTRL6 is shown in [表 7-54](#).

Return to the [Summary Table](#).

Disable the Error Correction pulses for Ripple Counting.

**表 7-54. RC\_CTRL6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	EC_PULSE_DIS	R/W	0h	Disable the Error Correction Pulses. Differs from the EN_EC bit described previously. 0b: Error correction is always enabled. 1b: Error correction will stop giving pulses under certain conditions described in <a href="#">セクション 7.3.6.1.11</a> .
6-4	T_MECH_FLT	R/W	4h	This parameter determines the cut-off frequency of a low pass filter at the output of the ripple counter to control the response time of the ripple counter to match the inertia of the mechanical system. Increase this value to for a slower response and decrease it for a faster response.
3-2	EC_FALSE_PER	R/W	1h	Sets the window during which the error corrector classifies a current ripple as an extra ripple. 00b: 20% 01b: 30% 10b: 40% 11b: 50%
1-0	EC_MISS_PER	R/W	1h	Sets the window during which the error corrector adds a missed ripple. 00b: 20% 01b: 30% 10b: 40% 11b: 50%

### 7.6.3.11 RC\_CTRL7 Register (Offset = 18h) [Reset = 21h]

RC\_CTRL7 is shown in [表 7-55](#).

Return to the [Summary Table](#).

Set the proportional constant in PI control loop.

**表 7-55. RC\_CTRL7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	KP_DIV	R/W	1h	Used to select a division value for calculating the actual proportional constant for the PI control loop. Actual proportional constant = $KP/KP\_DIV$ . Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KP	R/W	1h	Represents the PI loop KP constant. This is not the actual proportional constant that is fed into the gain block of the PI control loop. Rather, the actual proportional constant can be calculated using this value of the KP register. Actual Proportional Constant = $KP/KP\_DIV$ . For example, if actual proportional constant is 0.0625, then KP can be set to 1 (00001b), and KP_DIV can be set to 16 (corresponds to 101b), hence, Actual proportional constant = $1/16 = 0.0625$ .



### 7.6.3.12 RC\_CTRL8 Register (Offset = 19h) [Reset = 21h]

RC\_CTRL8 is shown in [表 7-56](#).

Return to the [Summary Table](#).

Set the integral constant in PI control loop.

**表 7-56. RC\_CTRL8 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	KI_DIV	R/W	1h	Used to select a division value for calculating the actual integral constant for the PI control loop. Actual integral constant = KI/KI_DIV. Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KI	R/W	1h	Represents the PI loop KI constant. This is not the actual integral constant that is fed into the gain block of the PI control loop. Rather, the actual integral constant can be calculated using this value of the KI register. Actual Integral Constant = KI/KI_DIV. For example, if actual integral constant is 0.90625, then KI can be set to 29 (11101b), and KI_DIV can be set to 32 (corresponds to 000b), hence, Actual integral constant = 29/32 = 0.90625.

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The DRV8234 is intended to drive one brushed DC motor.

### 8.2 Typical Application: Brushed DC Motor

A typical application for the DRV8234 is to drive a brushed DC motor using the full-bridge outputs. [8-1](#) shows a schematic example. The resistor on the IPROPI pin can provide a voltage signal to the microcontroller analog-to-digital converter (ADC).

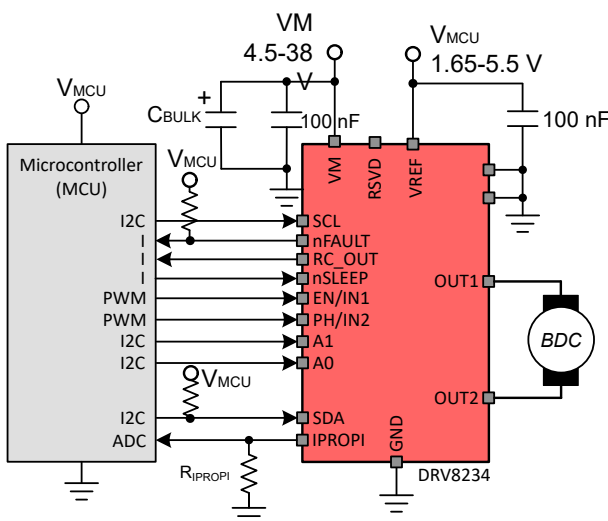


図 8-1. Typical Connections with stall detection disabled

#### 8.2.1 Design Requirements

表 8-1 lists example design parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	$V_{VM}$	8 V
Average motor current	$I_{AVG}$	0.8 A
Motor inrush (startup) current	$I_{INRUSH}$	2. A
Motor stall current	$I_{STALL}$	2.1 A
Motor current trip point	$I_{TRIP}$	1.9 A
VREF voltage	VREF	3.3 V
IPROPI resistance	$R_{IPROPI}$	8.45 kΩ
PWM frequency	$f_{PWM}$	20 kHz
Bulk Capacitance	$C_{BULK}$	50μF

## 8.2.2 Stall Detection

Some applications require stall detection to notify the microcontroller of a locked-rotor/stall condition. A stall could be caused by one of two things: unintended mechanical blockage or the load reaching an end-stop in a constrained travel path. The DRV8234 supports hardware stall detection by comparing the IPROPI pin voltage to the VREF pin voltage or 3 V as applicable.

### 8.2.2.1 Application Description

The principle of this stall detection scheme relies on the fact that motor current increases during stall conditions as shown in [Figure 8-2](#). The DRV8234 compares the voltage on the IPROPI pin to the voltage on the VREF pin to determine whether a stall condition has occurred. The TINRUSH register sets the timing,  $t_{INRUSH}$ , so the DRV8234 ignores the inrush current at motor startup. The SMODE pin configures how the DRV8234 responds to a stall condition. The IMODE pin configures whether the device regulates current during inrush and stall currents. When a stall condition occurs, nFAULT pin becomes low and the appropriate registers indicate stall to the microcontroller using the I<sup>2</sup>C pins. [セクション 7.3.5](#) provides all the details for configuring the stall detection feature.

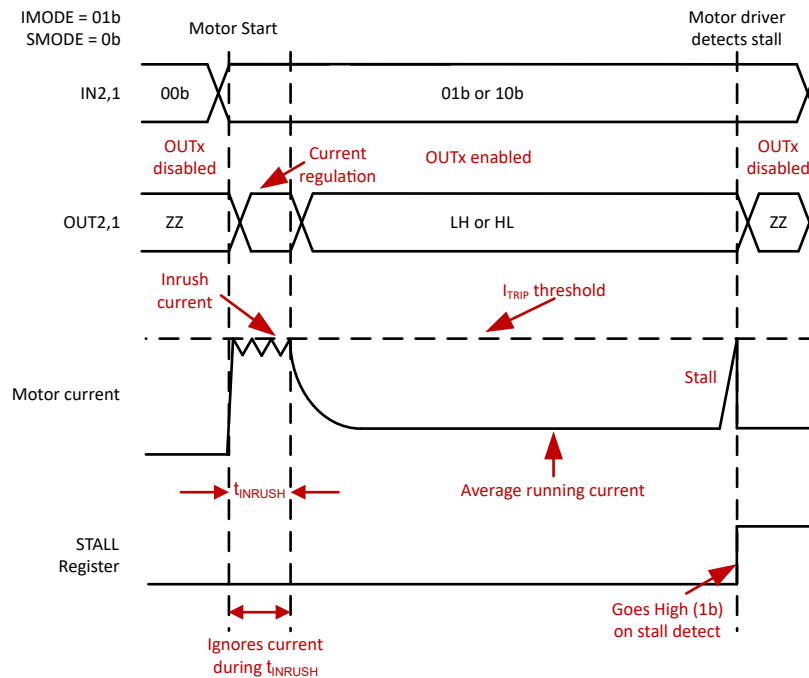


図 8-2. Example timing diagram for stall detection

#### 8.2.2.1.1 Stall Detection Timing

Large inrush current occurs during motor start up because motor speed is low. As the motor accelerates, the motor current drops to an average level because the back electromotive force (EMF) in the motor increases with speed. The inrush current should not be mistaken for a stall condition, so the DRV8234 uses the TINRUSH register to ignore the inrush current during the startup time,  $t_{INRUSH}$ . [セクション 7.3.5](#) describes the overall details for using the stall detection feature.

When designing for the  $t_{INRUSH}$  time, it is important to include enough margin to account for tolerances and variation in the DRV8234 and the system overall.

#### 8.2.2.1.2 Hardware Stall Threshold Selection

The voltage on the VREF pin selects  $I_{TRIP}$  threshold which sets the current level for stall detection and current regulation. This threshold should be chosen such that  $I_{TRIP}$  is less than the stall current of the motor when

current regulation is not used. It should also be set low enough to account for variation in the stall current due to changes in the motor supply voltage,  $V_{VM}$ , and temperature.

### 8.2.3 Ripple Counting Application

This section describes Ripple Counting and the associated tuning procedure using an example.

#### 8.2.3.1 Tuning Ripple Counting Parameters

This section explains the tuning process for the Ripple Counting parameters described in [セクション 7.3.6.1](#).

##### 8.2.3.1.1 Resistance Parameters

This section describes how to select INV\_R and INV\_R\_SCALE. The first step is to find the motor resistance. This can be done in three ways:

1. Use the motor resistance value mentioned in the data sheet of the motor. If this is not available, use one of the other methods listed below.
2. Perform a voltage sweep at the motor terminals, stall the motor at each voltage level, and measure the motor current. Please note that at least 10 measurements are required at every voltage level whilst rotating the motor by approximately 30° for each measurement. This is because it is unknown if the commutator segments are in contact with the brushes in a particular motor position which renders a lower, incorrect motor resistance value. **If motor resistance from the motor's data sheet is unavailable, then this method is recommended to obtain the value of motor resistance.** Take the average of all values to calculate motor resistance.
3. Measure the motor resistance using a digital multimeter. Please note that this process also needs to be done at every voltage level for 10 measurements each and then averaged out at the end for the same reason as mentioned above.

Once the motor resistance value is found, select an appropriate value of INV\_R\_SCALE and calculate INV\_R. The formula to calculate INV\_R is:

$$INV\_R = \frac{1}{\text{Motor Resistance}} \times INV\_R\_SCALE \quad (9)$$

For example, if the motor resistance is **25 Ω**, we have the following possible results based on the choice of INV\_R\_SCALE:

**表 8-2. Selection Example for INV\_R\_SCALE and INV\_R**

Bit	INV_R_SCALE value	INV_R_SCALE/Motor Resistance (Actual Value)	Rounded Value INV_R	Comment
00b	2	2/25=0.08	0	Do not select, since output is 0.
01b	64	64/25=2.56	3	Avoid selecting, since low bit precision.
<b>10b</b>	<b>1024</b>	<b>1024/25=40.96</b>	<b>41</b>	<b>Can select this value.</b>
11b	8192	8192/25=327.68	328	Cannot select this value because 328 exceeds the maximum limit for INV_R (255).

##### 8.2.3.1.2 KMC and KMC\_SCALE

Selection of KMC\_SCALE and KMC can be divided into two cases based on [式 5](#):

1. Value of the motor back emf constant,  $K_V$  is known to the user from the data sheet of the motor.
2. Value of the motor back emf constant,  $K_V$  is unknown to the user.

### 8.2.3.1.2.1 Case I

In case 1, 式 5 can be used. Choose the value of KMC\_SCALE such that KMC is within the range of 0 to 255 with highest bit resolution. As an example, if  $K_V = 0.01$  and number of ripples per revolution,  $N_R = 10$ ,  $K_V/N_R = 10^{-3}$ . The following table lists the available options:

**表 8-3. Selection Example for KMC\_SCALE**

Bit	KMC_SCALE value	$K_V/N_R \times KMC\_SCALE$ (Actual Value)	Rounded Value (KMC)	Comment
00b	$24 \times 2^8$	6.144	6	Avoid selecting, since low bit precision.
01b	$24 \times 2^9$	12.288	12	Avoid selecting, since low bit precision.
10b	$24 \times 2^{12}$	98.304	98	Avoid selecting, since low bit precision.
11b	$24 \times 2^{13}$	196.608	197	<b>Can select this value as this has the highest bit precision.</b>

### 8.2.3.1.2.2 Case II

In case 2, KMC and KMC\_SCALE need to be tuned manually using either of the two methods:

#### 8.2.3.1.2.2.1 Method 1: Tuning from Scratch

This method resets both parameters in the beginning before arriving at tuned values. 図 8-3 displays a flowchart for tuning KMC\_SCALE using this method. KMC can be found using Binary Search as shown in 図 8-4

##### 8.2.3.1.2.2.1.1 Tuning KMC\_SCALE

1. Obtain the value of actual ripple speed in rad/s using either of the two methods:
  - a. Use an oscilloscope to observe motor current waveform to measure the ripple frequency. This can be done in two ways:
    - Through the IPROPI pin which provides an output proportional to the motor current.
    - Through a current probe.

The frequency of ripples is observed in Hz on the oscilloscope. Please consider at least 20 ripples while calculating frequency. Divide the number of ripples by the time taken for calculating the frequency in Hz. Convert into rad/s using 式 11. Please note that **this is the recommended method**.

- b. Use a tachometer to obtain the motor speed in rpm. Convert the motor speed into ripple speed using 式 10. Finally, convert the ripple speed in rpm to ripple speed in rad/s using 式 12.

$$\text{Ripple Speed} = \text{Motor Speed} \times N_R \quad (10)$$

$$\text{Ripple Speed (in rad/s)} = \text{Ripple Speed (in Hz)} \times 2\pi \quad (11)$$

$$\text{Ripple Speed (in rad/s)} = \text{Ripple Speed (in rpm)} \times \frac{2\pi}{60} \quad (12)$$

Where  $N_R$  is the number of ripples per revolution. Let this value be called OBS\_SPEED.

2. Select the lowest value of KMC\_SCALE, 00b. Set KMC to the highest possible value, 255.
3. Refer to 表 7-21 to set W\_SCALE to a value where maximum ripple speed is more than OBS\_SPEED. For example, if OBS\_SPEED is 6000 rad/s, set W\_SCALE to 01b allowing a maximum speed of 8160 rad/s.
4. Convert the ripple speed on the SPEED register into rad/s by multiplying SPEED with W\_SCALE. For example, if SPEED reads 0x04 and W\_SCALE is set to 10b (corresponds to 64 rad/s), then ripple speed in rad/s =  $4 \times 64 = 256$  rad/s. Let this value be called EST\_SPEED.
5. If EST\_SPEED is lower than OBS\_SPEED, increase KMC\_SCALE by one bit.
6. Repeat steps 4-5 until EST\_SPEED is higher than OBS\_SPEED.

- Set KMC\_SCALE to the previous value. For example, if 11b was obtained in the previous step, set KMC\_SCALE to 10b. This is the tuned value of KMC\_SCALE.

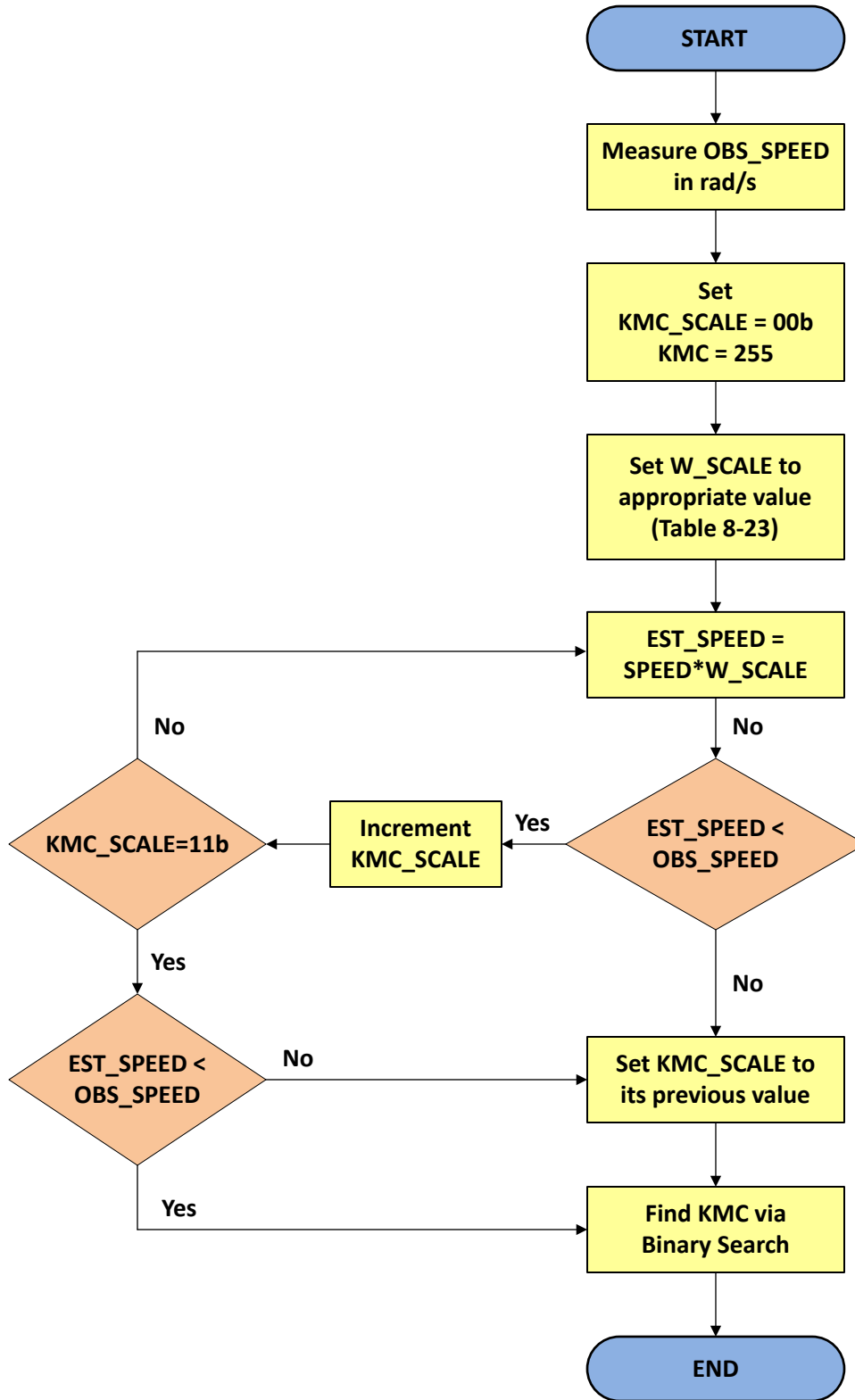


図 8-3. KMC\_SCALE Tuning Procedure

#### 8.2.3.1.2.2.1.2 Tuning KMC

1. Verify that  $EST\_SPEED < OBS\_SPEED$  and value of KMC is 255. If this is not the case, please restart the tuning process.
2. Let  $START = 0$  and  $END = 255$ .
3. Set KMC to START and obtain the value of OBS\_SPEED in rad/s **from step 1 of the KMC\_SCALE tuning procedure**.
4. If  $EST\_SPEED$  is within  $OBS\_SPEED \pm W\_SCALE$  value from [表 7-21](#), stop the tuning process and record the value of KMC. For example, if  $W\_SCALE = 10b$  (corresponds to 64 rad/s),  $OBS\_SPEED = 6000$  rad/s, and  $EST\_SPEED = 5937$  rad/s, stop the tuning process.
5. Let  $MID = (START+END)/2$ , rounded off to the nearest integer.
6. If  $EST\_SPEED$  is higher than  $OBS\_SPEED$  in this step, set KMC to MID. If  $EST\_SPEED$  is lower than  $OBS\_SPEED$  in this step, decrement KMC\_SCALE by one bit and repeat the binary search procedure to tune KMC.
7. If  $EST\_SPEED$  is higher than  $OBS\_SPEED$ , update  $START = MID$ . If  $EST\_SPEED$  is lower than  $OBS\_SPEED$ , update  $END = MID$ .
8. Repeat steps 4-7 until  $EST\_SPEED$  is within  $OBS\_SPEED \pm W\_SCALE$  value from [表 7-21](#). Record the value of KMC.

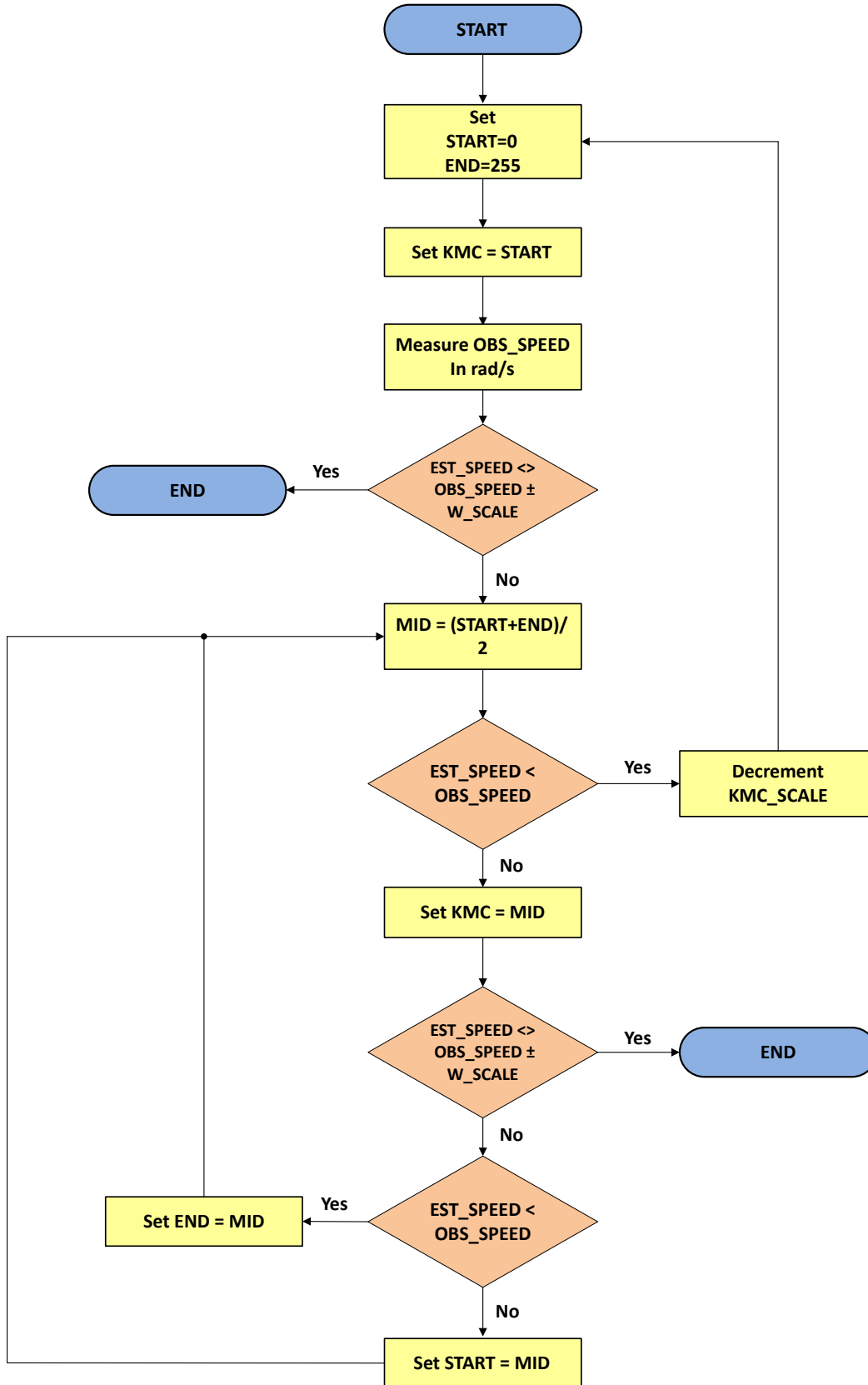


図 8-4. Binary Search Algorithm to Find KMC



注

1. Tuning is not possible in the following cases:
  - a. EST\_SPEED is higher than OBS\_SPEED after step 4 in the KMC\_SCALE tuning process (KMC\_SCALE = 00b; KMC = 255), or
  - b. EST\_SPEED is lower than OBS\_SPEED after step 3 in the Binary Search Method for KMC (KMC\_SCALE = 11b, KMC = 0).
2. Multiple sets of KMC and KMC\_SCALE exist. If found, then choose the set with highest bit resolution.

**8.2.3.1.2.2.2 Method 2: Using the Proportionality factor**

This method utilises the factor of proportionality that associates KMC and KMC\_SCALE with the ripple speed,  $\omega_{\text{ripple}}$ .  $\omega_{\text{ripple}}$  is directly proportional to KMC\_SCALE but varies inversely with KMC. Let  $k_d$  be a dummy constant. We have:

$$\omega_{\text{ripple}} = k_d \frac{\text{KMC\_SCALE}}{\text{KMC}} \quad (13)$$

Using the subscript 'def' to denote default, we have the following equation for default values of KMC and KMC\_SCALE:

$$\omega_{\text{def}} = k_d \frac{\text{KMC\_SCALE}_{\text{def}}}{\text{KMC}_{\text{def}}} \quad (14)$$

Using the subscript 'tuned', we similarly have the following equation for tuned values of KMC and KMC\_SCALE:

$$\omega_{\text{tuned}} = k_d \frac{\text{KMC\_SCALE}_{\text{tuned}}}{\text{KMC}_{\text{tuned}}} \quad (15)$$

Taking the ratio of the two equations above, the dummy constant,  $k_d$ , cancels out:

$$\frac{\omega_{\text{tuned}}}{\omega_{\text{def}}} = \frac{\text{KMC\_SCALE}_{\text{tuned}}}{\text{KMC}_{\text{tuned}}} \times \frac{\text{KMC}_{\text{def}}}{\text{KMC\_SCALE}_{\text{def}}} \quad (16)$$

At this point, the following is known:

1.  $\text{KMC\_SCALE}_{\text{def}} = 11\text{b} (24 \times 2^{13})$  is the default value of KMC\_SCALE from the register map.
2.  $\text{KMC}_{\text{def}} = 163$  is the default value of KMC from the register map.
3.  $\omega_{\text{tuned}}$  is the actual value of the ripple speed in rad/s. Please refer to step 1 of the [KMC\\_SCALE Tuning Method 1](#) for obtaining this value.

To obtain  $\omega_{\text{def}}$ , select a value of W\_SCALE based on step 3 of [KMC\\_SCALE Tuning Method 1](#). Next, convert the ripple speed on the [SPEED](#) register obtained using  $\text{KMC\_SCALE}_{\text{def}}$  and  $\text{KMC}_{\text{def}}$  into rad/s by multiplying [SPEED](#) with [W\\_SCALE](#). For example, if [SPEED](#) reads 0x04 and [W\\_SCALE](#) is set to 10b (corresponds to 64 rad/s), then ripple speed in rad/s =  $4 \times 64 = 256$  rad/s.

Plugging the four values above and simplifying, we get a ratio of  $\text{KMC\_SCALE}_{\text{tuned}}$  and  $\text{KMC}_{\text{tuned}}$  as a constant number. Select  $\text{KMC\_SCALE}_{\text{tuned}}$  from the four available values such that  $\text{KMC}_{\text{tuned}}$  has the highest bit precision within limits (0 to 255). A working example is shown below.

**8.2.3.1.2.2.2.1 Working Example**

As a working example, let  $\omega_{\text{tuned}} = 500$  rad/s. Thus,

- [W\\_SCALE](#) is chosen as 00b (16 rad/s) since  $500 < 4080$ , the maximum value allowable by [W\\_SCALE](#) based on [表 7-21](#).
- Let [SPEED](#) = 0x30. Thus,  $\omega_{\text{def}} = 48 \times 16 = 768$  rad/s.
- Plugging these values into [式 17](#), we have:

$$\frac{500}{768} = \frac{KMC\_SCALE_{tuned}}{KMC_{tuned}} \times \frac{163}{24 \times 2^{13}} \tag{17}$$

- Simplifying, we get:

$$785.276 = \frac{KMC\_SCALE_{tuned}}{KMC_{tuned}} \tag{18}$$

- The final step is to choose  $KMC\_SCALE_{tuned}$  such that  $KMC_{tuned}$  has the highest precision within limits (0 to 255). The following table illustrates the possible choices:

**表 8-4. Selection Example for KMC\_SCALE**

Bit	KMC_SCALE <sub>tuned</sub> value	KMC_SCALE <sub>tuned</sub> / 785.276 (Actual Value)	KMC <sub>tuned</sub> (Rounded Value)	Comment
00b	24 x 2 <sup>8</sup>	7.82	8	Avoid selecting, since low precision.
01b	24 x 2 <sup>9</sup>	15.64	16	Avoid selecting, since low precision.
10b	24 x 2 <sup>12</sup>	125.18	125	Avoid selecting, since low precision.
11b	24 x 2 <sup>13</sup>	250.36	250	Can select this value, since highest precision.

### 8.2.3.1.3 Advanced Parameters

#### 8.2.3.1.3.1 Filter Constants

This section describes how to tune the two filter constants: FLT\_K and FLT\_GAIN\_SEL.

##### 8.2.3.1.3.1.1 FLT\_GAIN\_SEL

Denoted by FLT\_GAIN\_SEL, this parameter selects the gain for the band pass filter. The gain scales the magnitude of current ripples for ease of detection and algorithmic calculation by the Ripple Counter. Recommended to set this to the maximum value (11b) to utilize the full signal range. Settings are as shown in [表 7-13](#).

##### 8.2.3.1.3.1.2 FLT\_K

Denoted by FLT\_K, this parameter represents the quality factor or Q-factor of the band pass filter. Tune this parameter to increase or decrease the bandwidth to accommodate a wider or narrower range of ripple frequencies around the center frequency. Center frequency of the filter is based on the frequency estimation of the motor for the ripples.

Settings are shown in [表 8-5](#). Recommended value is the default value: 0110b.

**表 8-5. Settings for FLT\_K**

Bit	Decimal	Value
0000	0	0.007813
0001	1	0.015265
0010	2	0.03125
0011	3	0.0625
0100	4	0.125
0101	5	0.25
0110	6	0.5
0111	7	0.625
1000	8	0.75
1001	9	0.825

**表 8-5. Settings for FLT\_K (続き)**

Bit	Decimal	Value
1010 - 1111	10-15	1

#### 8.2.3.1.3.2 T\_MECH\_FLT

This parameter determines the cut-off frequency of a low pass filter at the output of the ripple counter to control the response time of the ripple counter. Tune this parameter to match the inertia of the entire mechanical system. This can be done by observing the ripple counter response during dynamic speed events such as inrush or transient loading. Increasing the value of this parameter slows down the ripple counter response time; decreasing the value speeds up the response time. Setting this parameter to the default value (100b) is recommended since that suffices for most mechanical systems.

#### 8.2.3.1.3.3 VSNS\_SEL

This parameter is used to select the motor voltage output filtering method (analog or digital) during PWM. The analog filter (0b) filters out the noise based on the voltage difference between the output pins. The digital filter (1b) multiplies the PWM duty cycle with VM to render an average output voltage. Settings are shown in 表 7-15. When analog filter is selected, the cut-off frequency can be selected using the OUT\_FLT register. Recommended setting is the analog filter (0b).

#### 8.2.3.1.3.4 Additional Error Corrector Parameters

This section describes two additional parameters, EC\_FALSE\_PER and EC\_MISS\_PER. Please note that these are advanced parameters used for fine tuning the error corrector and used only in extreme scenarios. The default settings work in most cases.

##### 8.2.3.1.3.4.1 EC\_FALSE\_PER

EC\_FALSE\_PER is a 2-bit register that allows the user to select a blanking time window **after** a current ripple is detected. During this time window, the error corrector classifies any passed ripples from the digital filter as extra ripples and does not count them. The time window is represented as a percentage of time between two successive expected current ripples. The settings are shown in 表 8-6:

**表 8-6. Settings for EC\_FALSE\_PER**

Bit	Value
00b	20%
01b	30%
10b	40%
11b	50%

##### 8.2.3.1.3.4.2 EC\_MISS\_PER

EC\_MISS\_PER is a 2-bit register that allows the user to select a time window for when a current ripple is **expected** to be detected. During this time window, the error corrector identifies any ripples filtered out from the digital filter to classify them as missed and adds them manually. The time window is represented as a percentage of time between two successive expected current ripples. During this time window, the error corrector takes action if an expected ripple from the digital filter does not arrive. The time window is represented as a percentage of time between two successive expected current ripples. The settings are shown in 表 8-7:

**表 8-7. Settings for EC\_MISS\_PER**

Bit	Value
00b	20%
01b	30%
10b	40%
11b	50%

### 8.2.4 Motor Voltage

The motor voltage to use depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

### 8.2.5 Motor Current

Motors experience large currents at low speed, initial startup, and stalled rotor conditions. The large current at motor startup is sometimes called inrush current. The current regulation feature in the DRV8234 can help to limit these large currents. Additionally, DRV8234's soft-start feature can be used to limit the inrush current by ramping the PWM duty cycle during startup time. Alternatively, the microcontroller may limit the inrush current via a similar procedure.

## 8.2.6 Application Curves

RC\_OUT denotes the pulse train output of the RC\_OUT pin

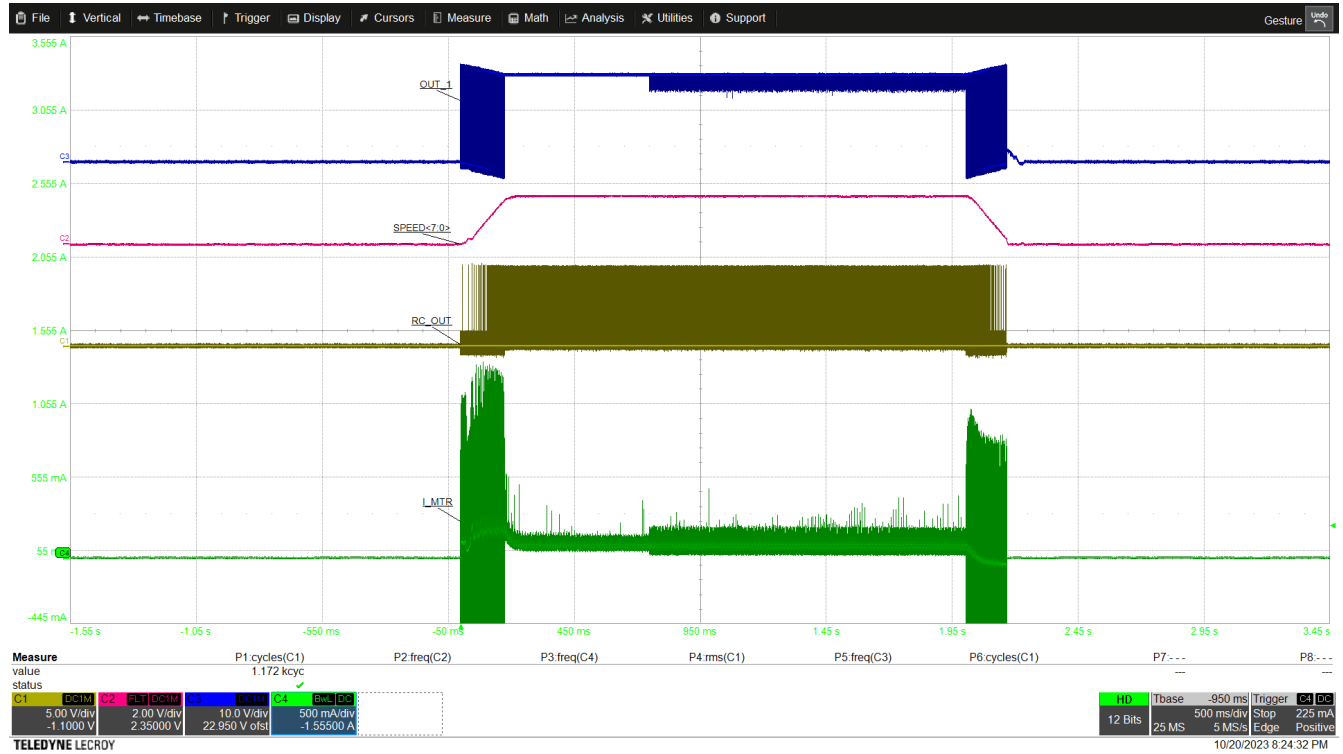


図 8-5. Example Operation at VM = 12 V

RC\_OUT denotes the pulse train output of the RC\_OUT pin

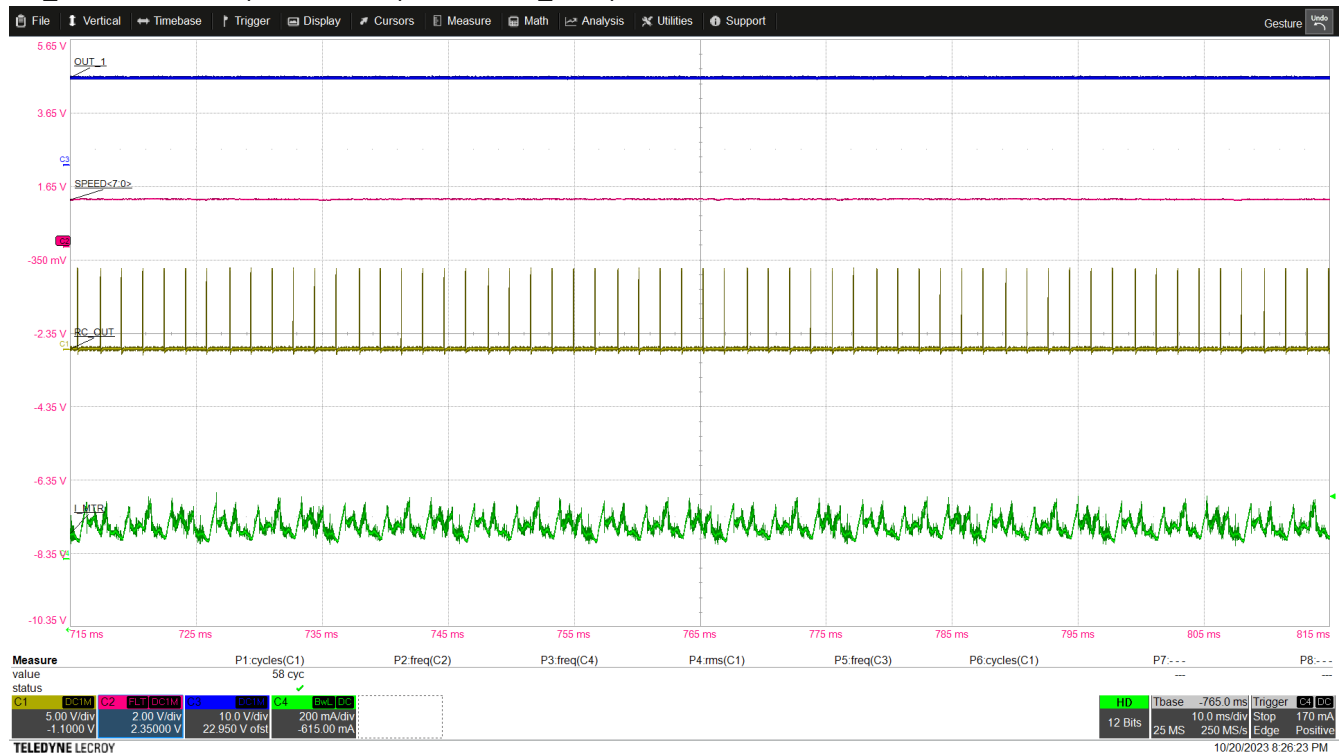


図 8-6. Steady State Operation at VM = 12 V

RC\_OUT denotes the pulse train output of the RC\_OUT pin

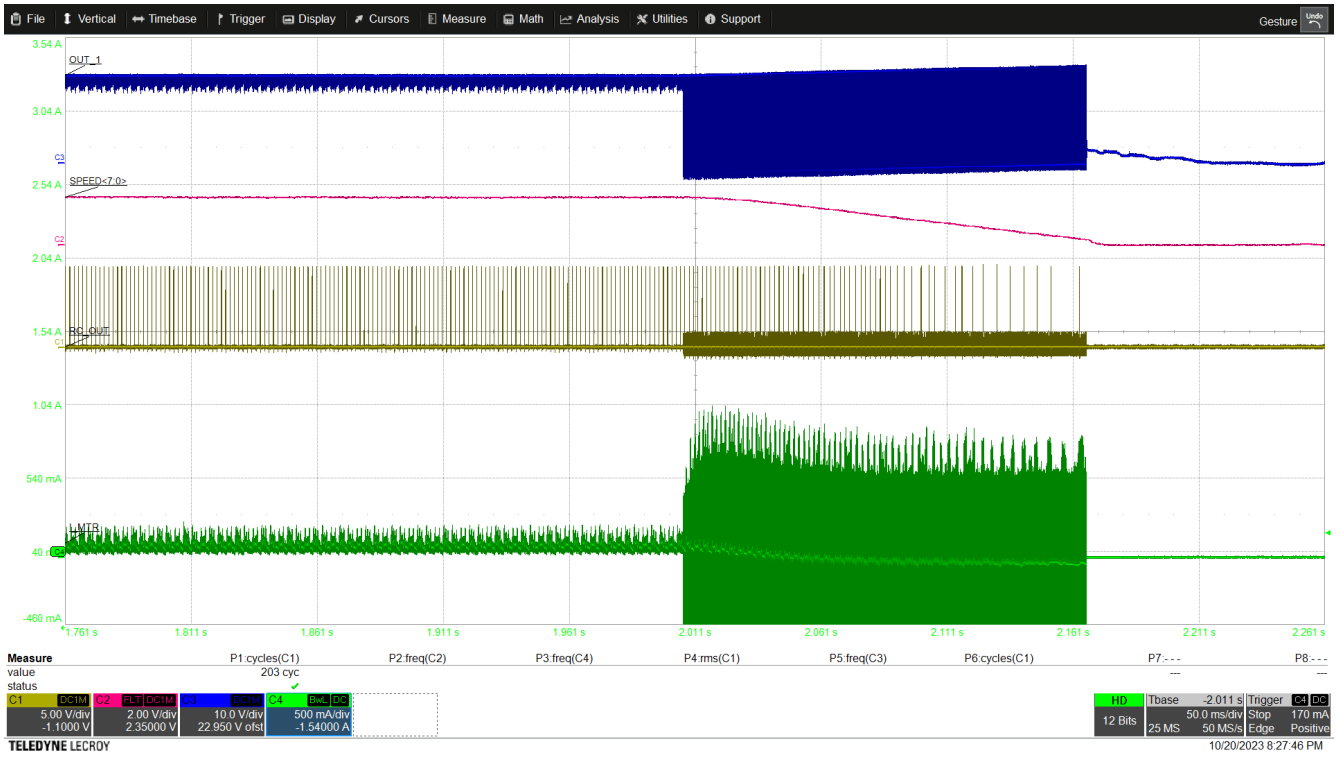


图 8-7. Soft Stop at VM = 12 V

RC\_OUT denotes the pulse train output of the RC\_OUT pin

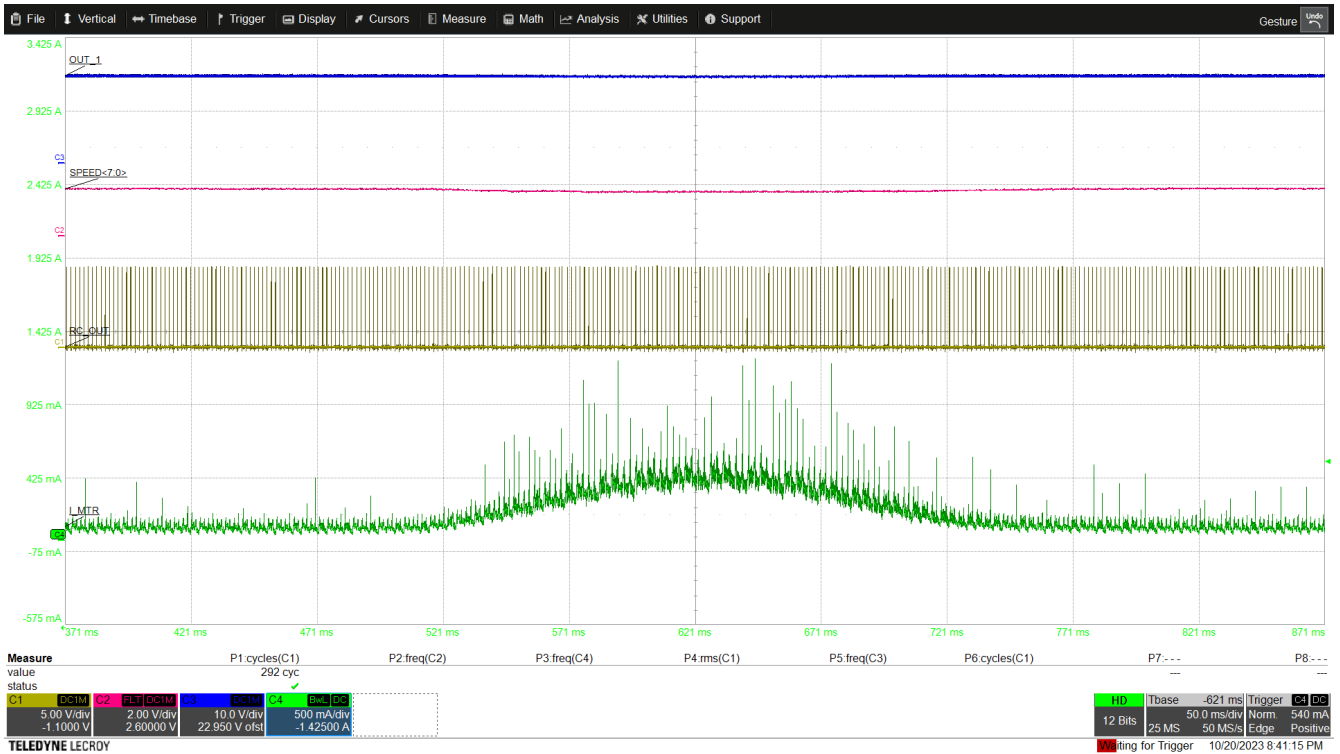


图 8-8. Transient Loading Conditions - Full Profile

## 9 Power Supply Recommendations

### 9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

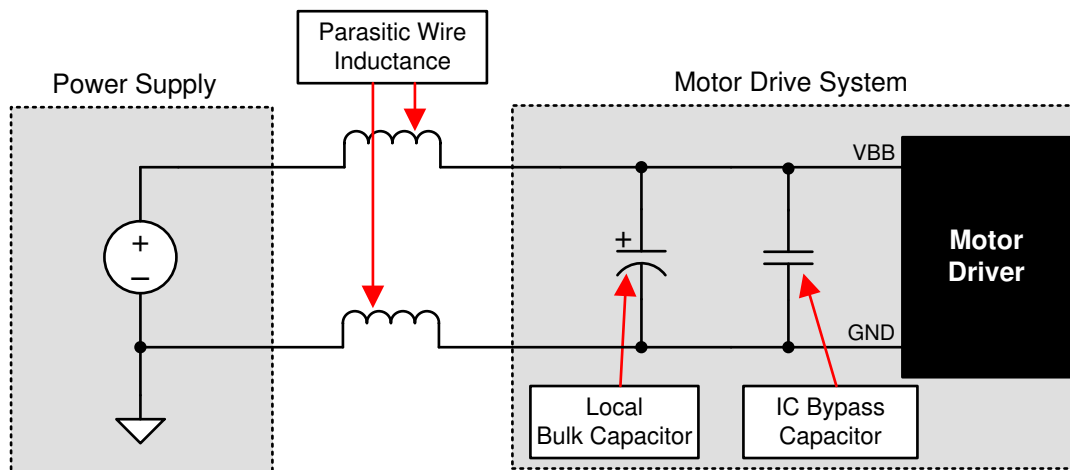


図 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

## 10 Layout

### 10.1 Layout Guidelines

Since the DRV8234 integrates power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor. X5R and X7R types are recommended.
- The VM power supply capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.



## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。  
[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8234RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8234	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8234RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8234RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

**RTE 16**

**WQFN - 0.8 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

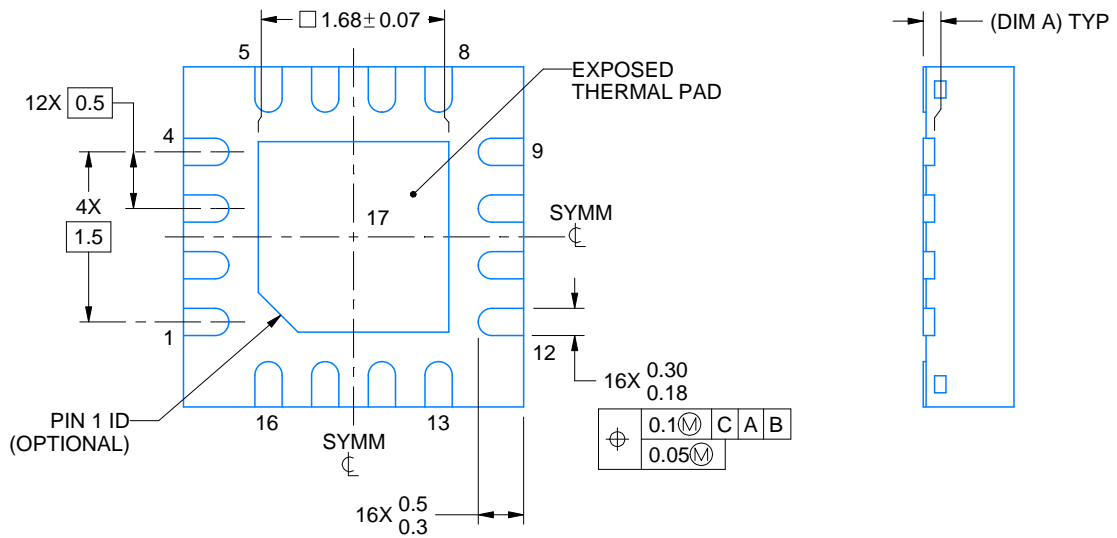
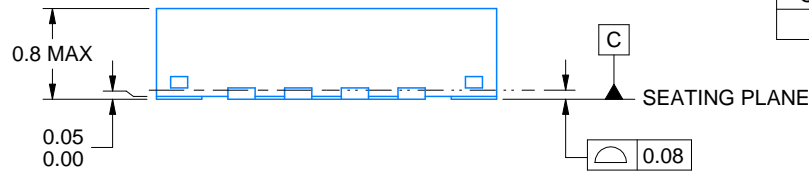
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

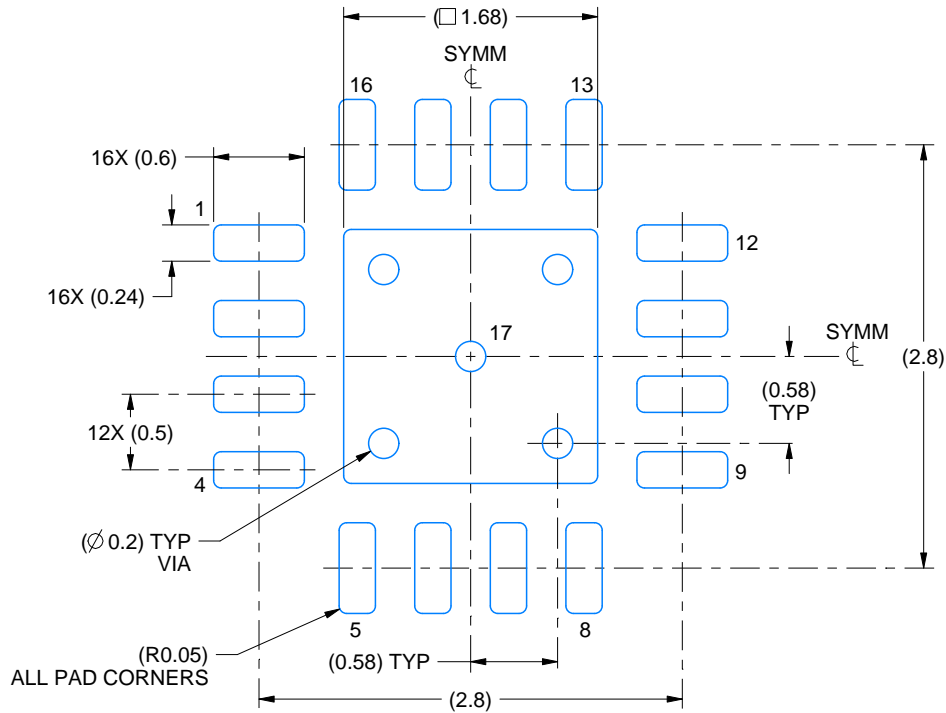
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

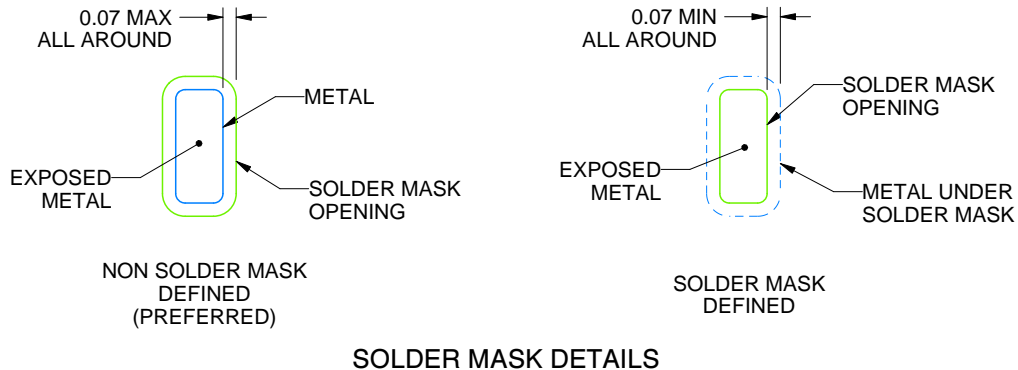
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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