DRV8421 18V 2A デュアル H ブリッジ ステッパ ドライバ

1 特長

- デュアル H ブリッジ モータ ドライバ
  - シングル／デュアルのブラシ付き DC
  - ステッパ
  - ソレノイド
- 4～18V の動作電源電圧範囲
- 低オン抵抗：HS + LS = 900mΩ (標準値、25°C)
- H ブリッジごとの高出力電流
  - 12V および T_A = 25°C での最大駆動電流：2A
  - 12V および T_A = 25°C で最大駆動電流 **4A** を並列モードで対応可能
- デバイス バージョン：
  - **DRV8421A (4 線式入力)**：独立したハーフブリッジ制御
  - **DRV8421B (2 線式入力)**：スリープ モード、障害検出
- 類似の LV ステッパ ドライバ：
  - DRV8410：1.65～11V (800mΩ $R_{DS(ON)}$)
  - DRV8411：1.65～11V (400mΩ $R_{DS(ON)}$)
  - DRV8411A：1.65～11V (400mΩ $R_{DS(ON)}$)
- PWM 制御インターフェイス
- 低電流 3μA スリープ モード (2 線式入力バージョンのみ)
- 熱特性強化型の表面実装パッケージ
- 保護機能
  - VM 低電圧誤動作防止 (UVLO)
  - 過電流保護 (OCP)
  - サーマル シャットダウン (TSD)
  - 故障状態表示ピン (nFAULT) (2 線式入力バージョンのみ)

2 アプリケーション

- 家電製品
  - プリンタ／スキャナ
  - 冷蔵庫
  - 掃除機
  - 洗濯乾燥機
- 汎用ブラシ付きモーターおよびステッパ モーター

3 概要

DRV8421 は、家電機器やその他のメカトロニクス用途を対象としたデュアル H ブリッジ モータ ドライバです。このデバイスを使用すると、1 つまたは 2 つの DC モータ、1 つのバイポーラ ステッパ モータ、またはその他の負荷を駆動できます。単純な PWM インターフェイスにより、簡単に制御回路と接続できます。

各 H ブリッジドライバの出力ブロックには、モータ巻線を駆動するフル H ブリッジとして構成された N チャネル パワー MOSFET が搭載されています。DRV8421 は、各出力から最大 2A または並列モードで 4A の最大電流を駆動できます (12V および T_A = 25°C で適切なヒートシンクを使用した場合)。

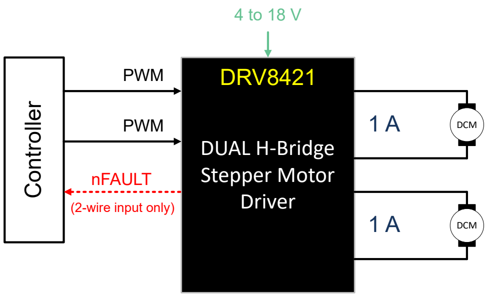
このデバイスには、4 線式入力 (DRV8421A) または 2 線式入力（DRV8421B) の 2 つのバージョンがあります。2 線式入力バージョン (DRV8421B) はイネーブルや障害検出などの機能を備えており、4 線式入力バージョン (DRV8421A) は 4 つの入力端子への信号に基づいて 4 つのハーフブリッジを駆動できます。2 線式入力バージョンは、低消費電力のスリープモードも備えています。これにより、内部回路がシャットダウンされ、静止消費電流が非常に小さくなります。このスリープモードは、イネーブル ピンを Low にすることで設定できます。

OCP、短絡保護、過熱に対する保護機能が内蔵されています。故障状態は、2 線式入力デバイス DRV8421B では nFAULT ピンで示されます。

製品情報 (1)

部品番号	パッケージ	パッケージ サイズ (2)
DRV8421ADGQ	HVSSOP (10)	3.00mm × 3.00mm
DRV8214BDGQ	HVSSOP (10)	3.00mm × 3.00mm
DRV8421ADFU	SSOP (10)	3.90mm × 4.90mm
DRV8421BDFU	SSOP (10)	3.90mm × 4.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます



概略回路図

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4 Device Comparison

表 4-1. Device Comparison Table

Part Number	Package	Supply VM (V)	$R_{DS(ON)}$ (mΩ)	Overcurrent Protection (OCP) Limit (A)	Current Regulation	Current Sense	Package Size
DRV8421	HVSSOP (10)	4 to 18	900	2	No	No	3.0mm x 3.0mm
	SSOP (10)	4 to 18	900	2	No	No	3.9mm x 4.9mm
DRV8848	HTSSOP (16)	4 to 18	900	2	Yes	External Shunt Resistor	5.0mm x 6.4mm
DRV8410	HTSSOP (16)	1.65 to 11	800	2.5	Yes	External Shunt Resistor	5.0mm x 6.4mm
	WQFN (16)	1.65 to 11	800	2.5	Yes	External Shunt Resistor	3.0mm x 3.0mm
	Thin-SOT (16)	1.65 to 11	800	2.5	Yes	External Shunt Resistor	4.2mm x 2.0mm
DRV8411	HTSSOP (16)	1.65 to 11	400	4	Yes	External Shunt Resistor	5.0mm x 6.4mm
	WQFN (16)	1.65 to 11	400	4	Yes	External Shunt Resistor	3.0mm x 3.0mm
	Thin-SOT (16)	1.65 to 11	400	4	Yes	External Shunt Resistor	4.2mm x 2.0mm
DRV8411A	HTSSOP (16)	1.65 to 11	400	4	Yes	Current Mirror (IPROPI)	5.0mm x 6.4mm
	WQFN (16)	1.65 to 11	400	4	Yes	Current Mirror (IPROPI)	3.0mm x 3.0mm
	Thin-SOT (16)	1.65 to 11	400	4	Yes	Current Mirror (IPROPI)	4.2mm x 2.0mm

5 Pin Configuration and Functions

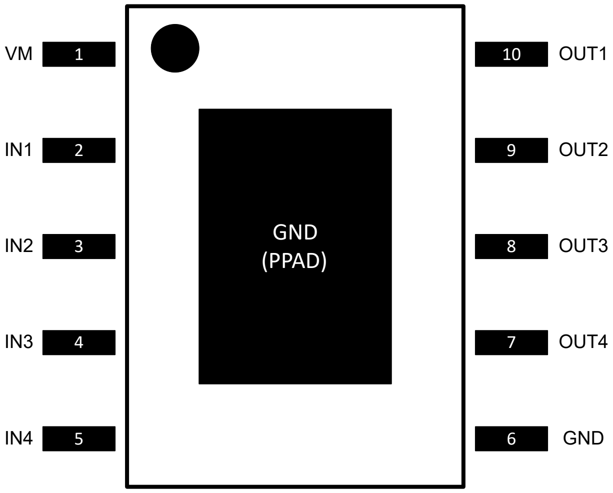

図 5-1. DRV8421A PWP Package 10-Pin HVSSOP Top View

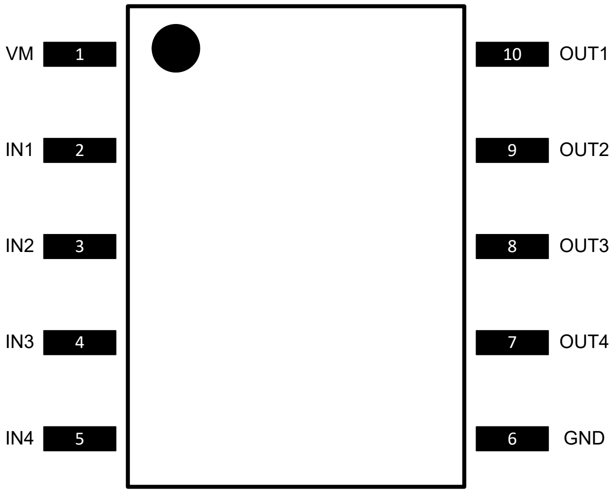

図 5-2. DRV8421A 10-Pin SSOP Top View

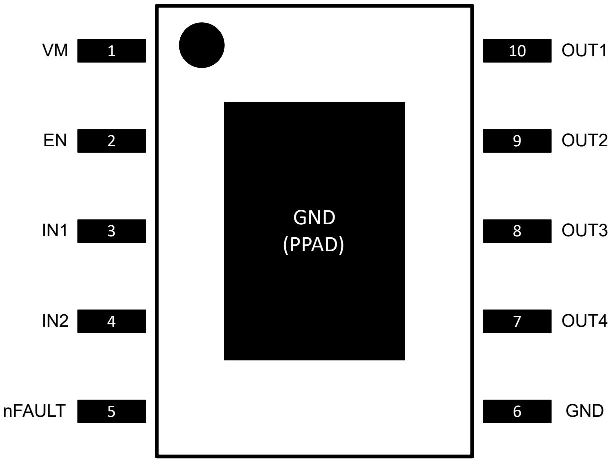

図 5-3. DRV8421B PWP Package 10-Pin HVSSOP Top View

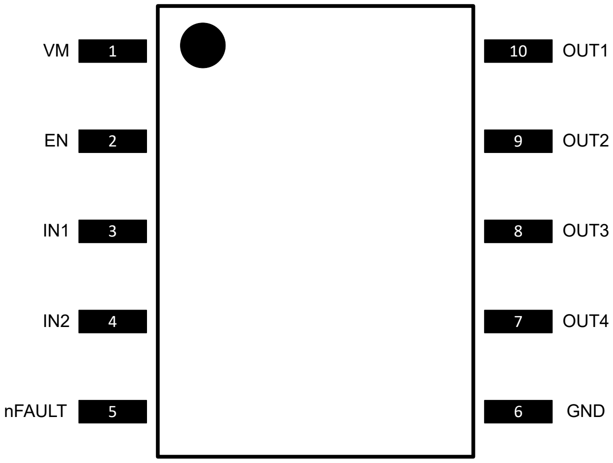

図 5-4. DRV8421B 10-Pin SSOP Top View

表 5-1. Pin Functions

PIN			TYPE[(1)]	DESCRIPTION	
NAME	NO.				
	4-wire input (8421A)	2-wire input (8421B)			
IN1	2	3	I	Input 1	Controls OUT1
IN2	3	4	I	Input 2	Controls OUT2
IN3	4	-	I	Input 3	Controls OUT3
IN4	5	-	I	Input 4	Controls OUT4
EN	-	2	I	Enable Pin	Enable or sleep mode input. Device enables with pin pulled high; sleep mode activated with pin pulled low for time more than t_{SLEEP}

表 5-1. Pin Functions (続き)

PIN			**TYPE**(1)	**DESCRIPTION**	
NAME	**NO.**				
	4-wire input (8421A)	**2-wire input (8421B)**			
nFAULT	-	5	OD	Fault Indication Pin	Pulled logic low with fault condition; open-drain output requires external pullup
OUT1	10	10	O	Output 1	Controls OUT1; internal pulldown
OUT2	9	9	O	Output 2	Controls OUT2; internal pulldown
OUT3	8	8	O	Output 3	Controls OUT3; internal pulldown
OUT4	7	7	O	Output 4	Controls OUT4; internal pulldown
GND	6	6	PWR	Device ground	GND pin to be connected to ground
VM	1	1	PWR	Power supply	Connect to motor power supply; bypass to GND with a 0.1 and 10µF (minimum) ceramic capacitor rated for VM

(1) I = Input, O = Output, PWR = Power

表 5-2. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	10µF (minimum) ceramic capacitor rated for VM
C_{VM}	VM	GND	0.1µF ceramic capacitor rated for VM
R_{nFAULT}	VCC(1)	nFAULT	>1kΩ

(1) VCC is not a pin on the DRV8421, but a VCC supply voltage pullup is required for open-drain output nFAULT

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range referenced with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Power supply voltage (VM)	-0.3	20	V
	Power supply voltage ramp rate (VM)	0	2	V/µs
	Control pin voltage (IN1, IN2, IN3, IN4, EN, nFAULT)	-0.3	7	V
	Continuous phase node pin voltage (OUT1, OUT2, OUT3, OUT4)	-0.3	V_{VM} + 0.6	V
	Peak drive current (OUT1, OUT2, OUT3, OUT4)	Internally limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{VM}	Power supply voltage range(1)	4		18	V
f_{PWM}	Applied INPUT Signal	0		250	kHz
Irms	Motor rms current per H-bridge(2)	0		2	A
T_A	Operating ambient temperature	–40		85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8421		UNIT
		DFU (SSOP)	DGQ (HVSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	62.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.5	80.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.7	28.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.2	6.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.0	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)					

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VM}	VM operating voltage		4		18	V
I_{VM}	VM operating supply current	V_{VM} = 12 V, excluding winding current	1.2	1.35	1.5	mA
I_{VMQ}	VM sleep mode supply current (2-wire input only)	V_{VM} = 12V, EN = 0 (2-wire input only)	0.5	1.2	3	µA
t_{SLEEP}	Sleep time (2-wire input only)	EN = 1 to sleep mode (2-wire input only)			1	ms
t_{WAKE}	Wake time (2-wire input only)	EN = 0 to output transition (2-wire input only)			1	ms
t_{ON}	Power-on time	V_{VM} > V_{UVLO} rising to output transition			1	ms
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, EN)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_I = 0 V	-1		1	µA
I_{IH}	Input logic high current	V_I = 5 V	1		30	µA
R_{PD}	Pulldown resistance (2-wire input version)	IN1		200		kΩ
		IN2		170		kΩ
R_{PD}	Pulldown resistance (4-wire input version)	IN1/IN2		200		kΩ
		IN3/IN4		170		kΩ
R_{PD}	Pulldown resistance	EN (2-wire input only)		500		kΩ
t_{DEG}	Input deglitch time	INx		200		ns
t_{PROP}	Propagation delay	INx edge to output change		400		ns
CONTROL OUTPUTS (NFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	-1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 25°C		550		mΩ
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 85°C(1)		660		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 25°C		350		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 12 V, I_O = 0.5 A, T_J = 85°C(1)		420		mΩ
I_{OFF}	Off-state leakage current	V_{VM} = 5 V, T_J = 25°C (2-wire input only)	-1		1	µA
t_{RISE}	Output rise time			60		ns
t_{FALL}	Output fall time			60		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	V_{VM} falling; UVLO report			2.9	V
		V_{VM} rising; UVLO recovery			3	V
I_{OCP}	Overcurrent protection trip level		2			A
t_{DEG}	Overcurrent deglitch time			2.8		µs
t_{OCP}	Overcurrent protection period			1.6		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C
T_{HYS} (1)	Thermal shutdown hysteresis	Die temperature T_J		35		°C

(1) Not tested in production; limits are based on characterization data

6.6 Timing Requirements

NO.			MIN	MAX	UNIT
1	t_1	Delay time, xIN1 to xOUT1	100	600	ns

NO.			MIN	MAX	UNIT
2	t_2	Delay time, xIN2 to xOUT1	100	600	ns
3	t_3	Delay time, xIN1 to xOUT2	100	600	ns
4	t_4	Delay time, xIN2 to xOUT2	100	600	ns
5	t_R	Output rise time	50	150	ns
6	t_F	Output fall time	50	150	ns

6.7 Typical Characteristics

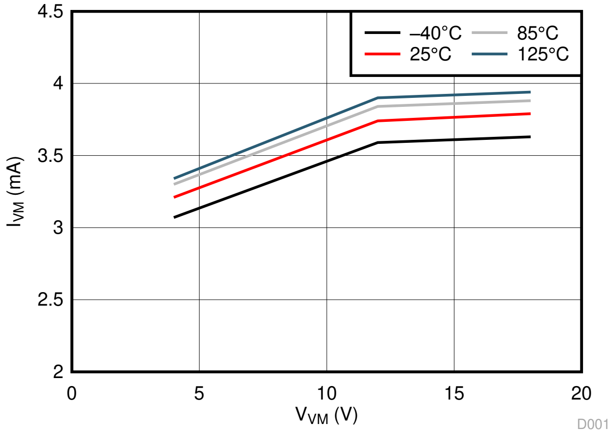

図 6-1. I_{VM} vs V_{VM}

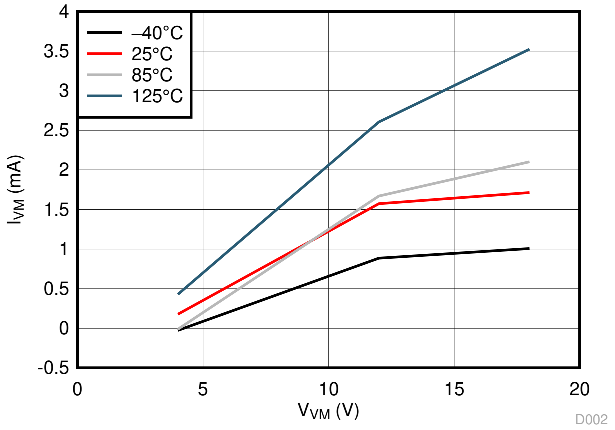

図 6-2. I_{VMQ} vs V_{VM}

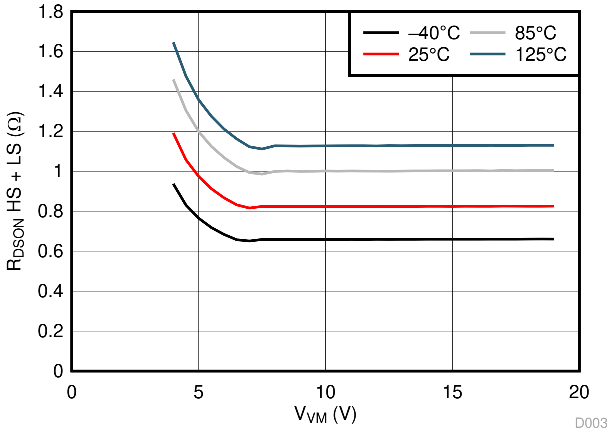

図 6-3. R_{DSON} vs V_{VM}

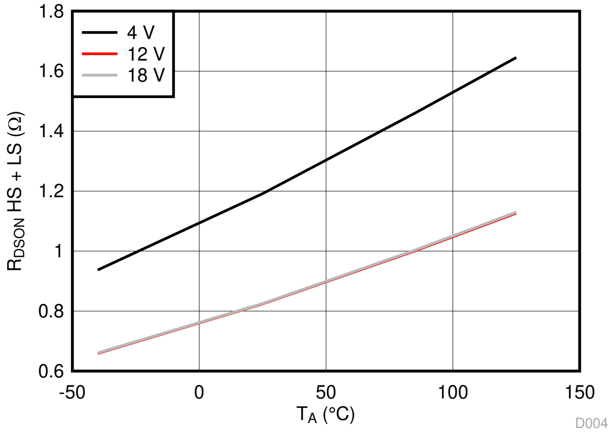

図 6-4. R_{DSON} vs Temperature

7 Detailed Description

7.1 Overview

The DRV8421 is an integrated stepper motor driver solution for two DC motors or a bipolar stepper motor. The device integrates two H-bridges that use NMOS drivers. It can be powered with a supply range between 4 to 18 V and is capable of driving a maximum of 2 A driver current (4 A in parallel mode operation).

A simple PWM interface allows easy interfacing to the controller circuit.

Two versions exist in the device, namely, DRV8421A, a 4-wire input device, and DRV8421B, a 2-wire input device. The DRV8421A allows control of four half bridges using four inputs while the DRV8421B has two inputs to control four half bridges. The DRV8421B consists of additional features like the low-power sleep mode to save power when not driving the motor and fault detection using the nFAULT pin.

7.2 Functional Block Diagrams

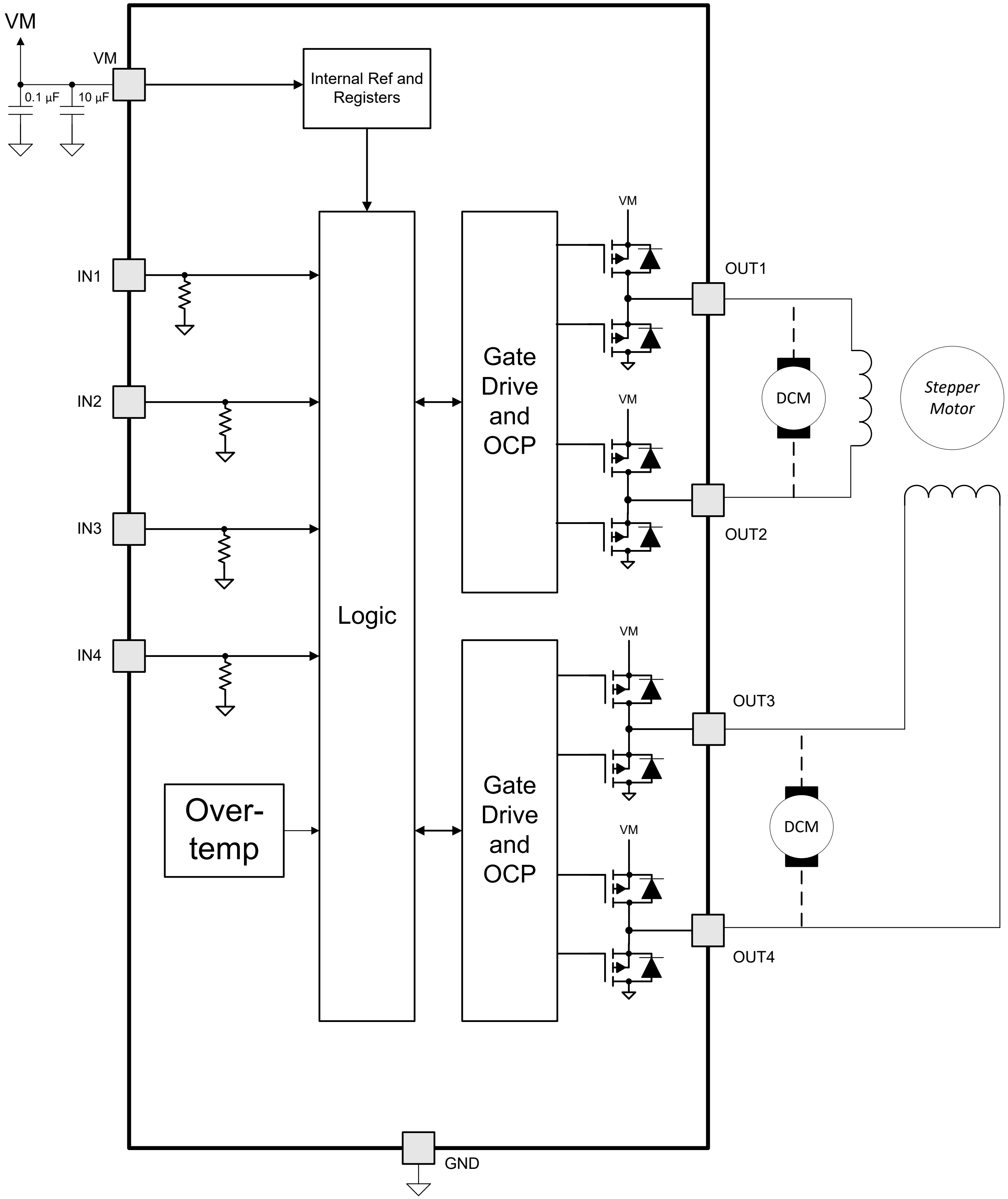

図 7-1. DRV8421A: 4-wire input

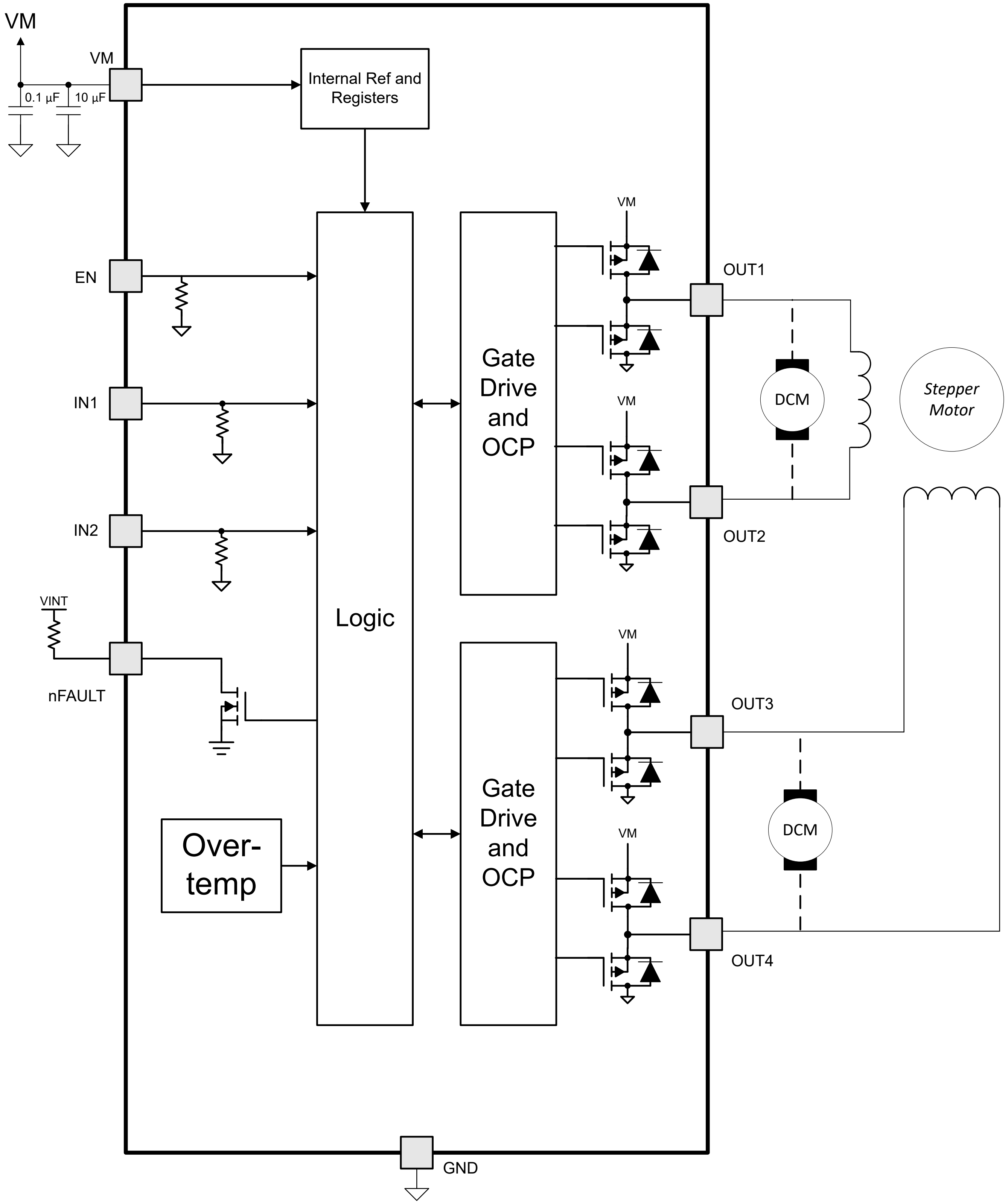

図 7-2. DRV8421B: 2-wire input

7.3 Feature Description

7.3.1 PWM Motor Drivers

DRV8421 contains two identical H-bridge motor drivers with current-control PWM circuitry. 図 7-3 shows a block diagram of the circuitry for DRV8421.

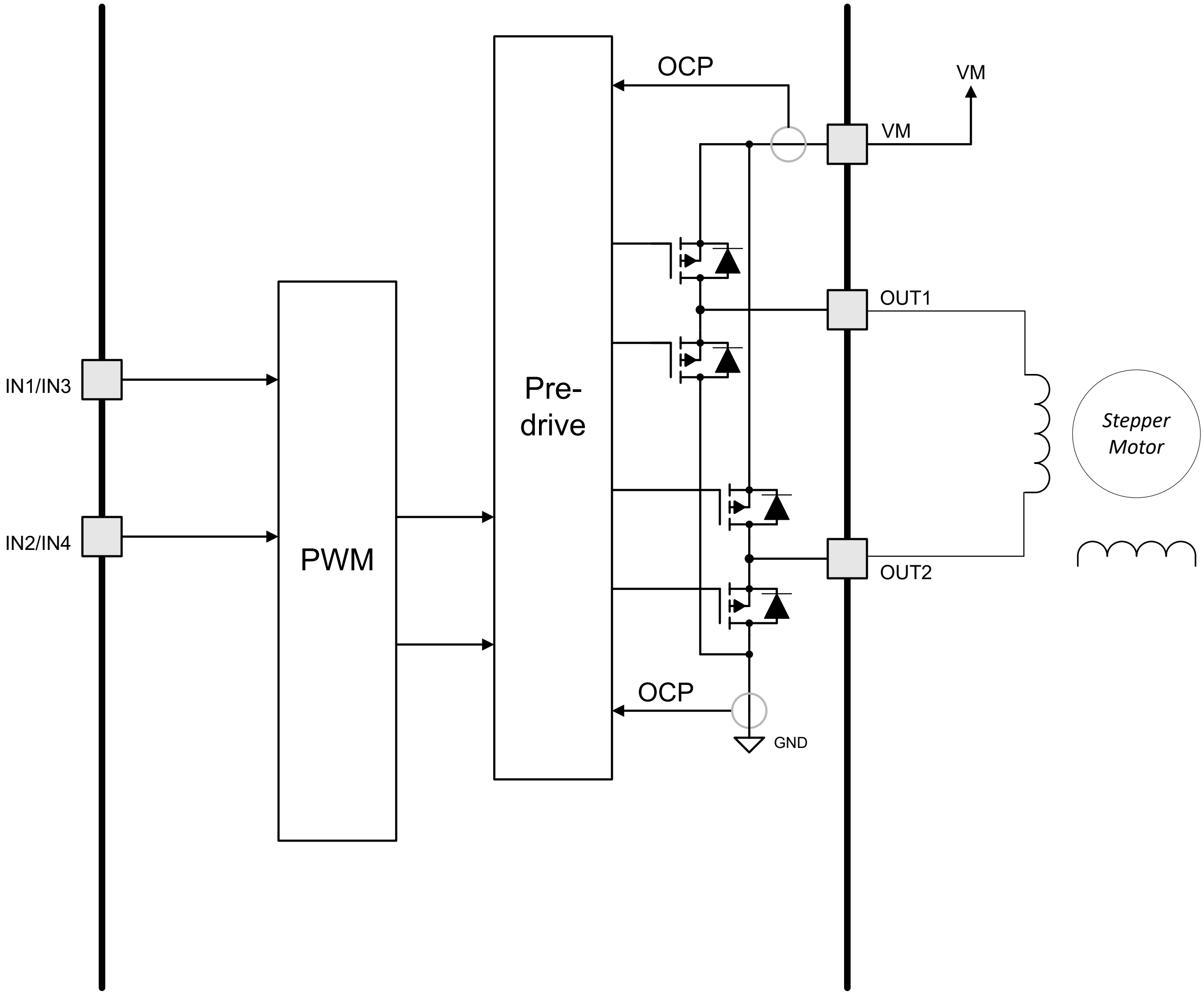

図 7-3. PWM Motor Driver Circuitry

7.3.2 Truth Tables

DRV8421A: 4-wire input version shows the logic for the inputs IN1, IN2, IN3, and IN4. DRV8421B: 2-wire input version shows the logic for the inputs IN1 and IN2.

表 7-1. DRV8421A: 4-wire input version

Inputs				Outputs				Function	
IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4		
0	0	0	0	Off	Off	Off	Off	Standby (Hi-Z)	
0	0	-		Off	Off	-		Channel 1	Standby (Hi-Z)
1	0			1	0				Forward
0	1			0	1				Reverse
1	1			0	0				Brake
-		0	0	-		Off	Off	Channel 2	Standby (Hi-Z)
		1	0			1	0		Forward
		0	1			0	1		Reverse
		1	1			0	0		Brake

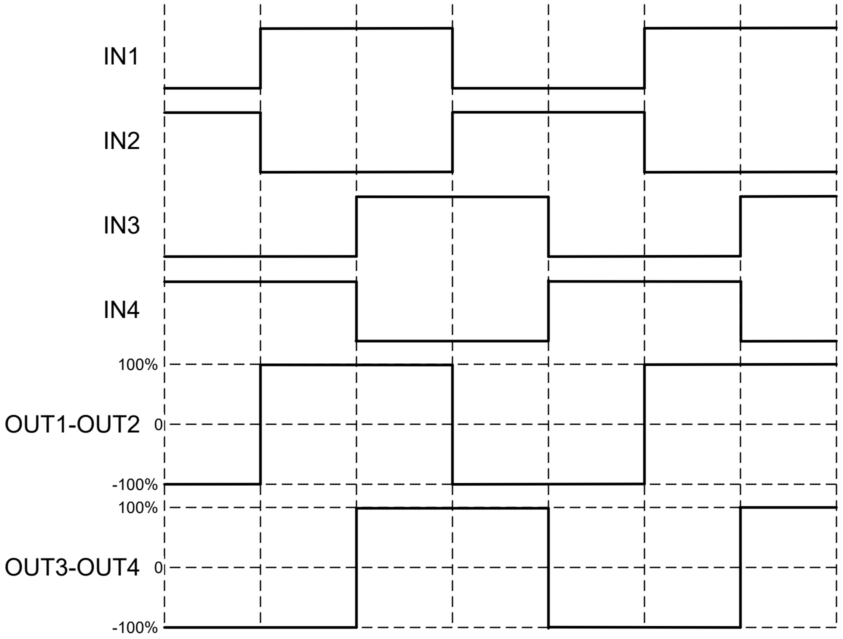

図 7-4. Full-Step Mode

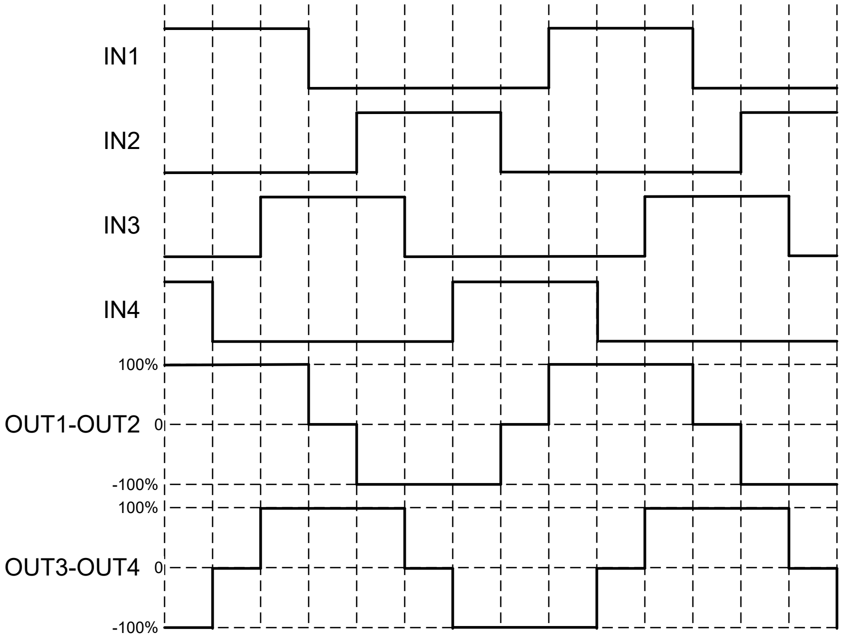

図 7-5. Half-Step Mode

表 7-2. DRV8421B: 2-wire input version

Inputs			Outputs				Function	
EN	**IN1**	**IN2**	**OUT1**	**OUT2**	**OUT3**	**OUT4**		
L	X	X	Off	Off	Off	Off	Standby/Low Power Sleep Mode	
H	L	-	H	L	-		Channel 1	Forward
	H		L	H				Reverse
	-	L	-		H	L	Channel 2	Forward
		H			L	H		Reverse

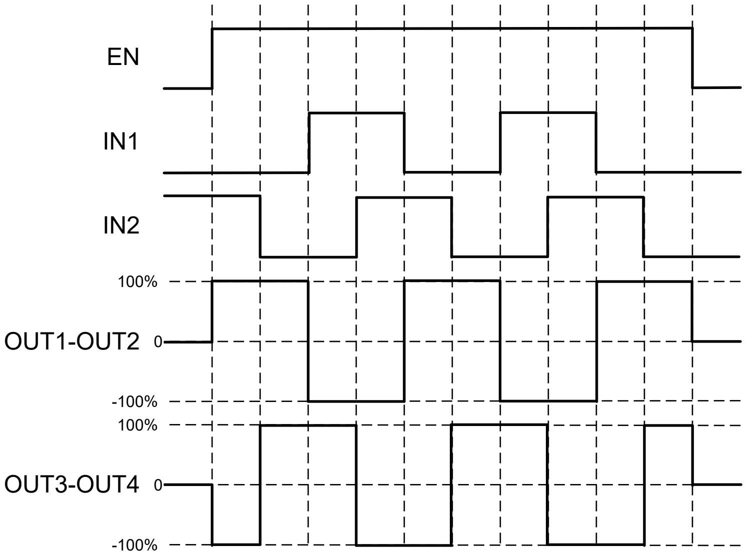

図 7-6. Full-Step Mode

7.3.3 Parallel Operation

The two drivers can be used in parallel to deliver twice the current to a single motor. To enter parallel mode in DRV8421A, the 4-wire input version, the following actions must be taken (refer to 図 7-7):

1. IN1 and IN3 must be tied together
2. IN2 and IN4 must be tied together
3. OUT1 and OUT3 must be tied together
4. OUT2 and OUT4 must be tied together

To exit parallel mode, all inputs must be made independent and the device must be powered-up.

表 7-3. Parallel Mode Operation: DRV8421A (4-wire input)

Inputs				Outputs				Function
IN1	**IN2**	**IN3**	**IN4**	**OUT1**	**OUT2**	**OUT3**	**OUT4**	
0	0	0	0	Off	Off	Off	Off	Standby (Hi-Z)
1	0	1	0	1	0	1	0	Forward
0	1	0	1	0	1	0	1	Reverse
1	1	1	1	0	0	0	0	Brake

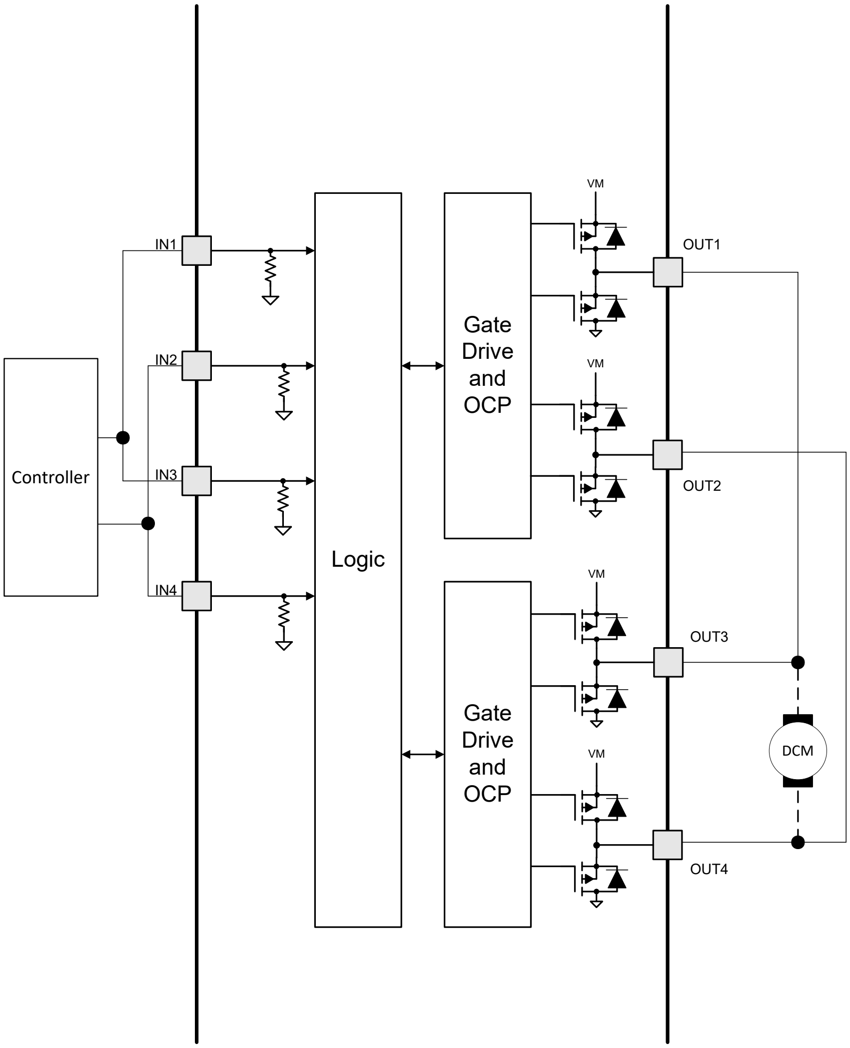

図 7-7. Parallel Mode Operation: DRV8421A

For the DRV8421B, the 2-wire input version, parallel mode operation can be achieved by taking the following steps (refer to 図 7-8):

1. IN1 and IN2 must be tied together
2. OUT1 and OUT3 must be tied together
3. OUT2 and OUT4 must be tied together

To exit parallel mode, all inputs must be made independent and the device must be powered-up.

表 7-4. Parallel Mode Operation: DRV8421B (2-wire input)

Inputs			Outputs				Function
EN	**IN1**	**IN2**	**OUT1**	**OUT2**	**OUT3**	**OUT4**	
L	X	X	Off	Off	Off	Off	Standby/Low Power Sleep Mode
H	L	L	H	L	H	L	Forward
	H	H	L	H	L	H	Reverse

注

Providing 50% duty cycle to IN1/IN2 tied together will stop the motor in DRV8421B Parallel Mode. To move forward, provide a duty cycle lower than 50%. To move reverse, provide a duty cycle higher than 50%.

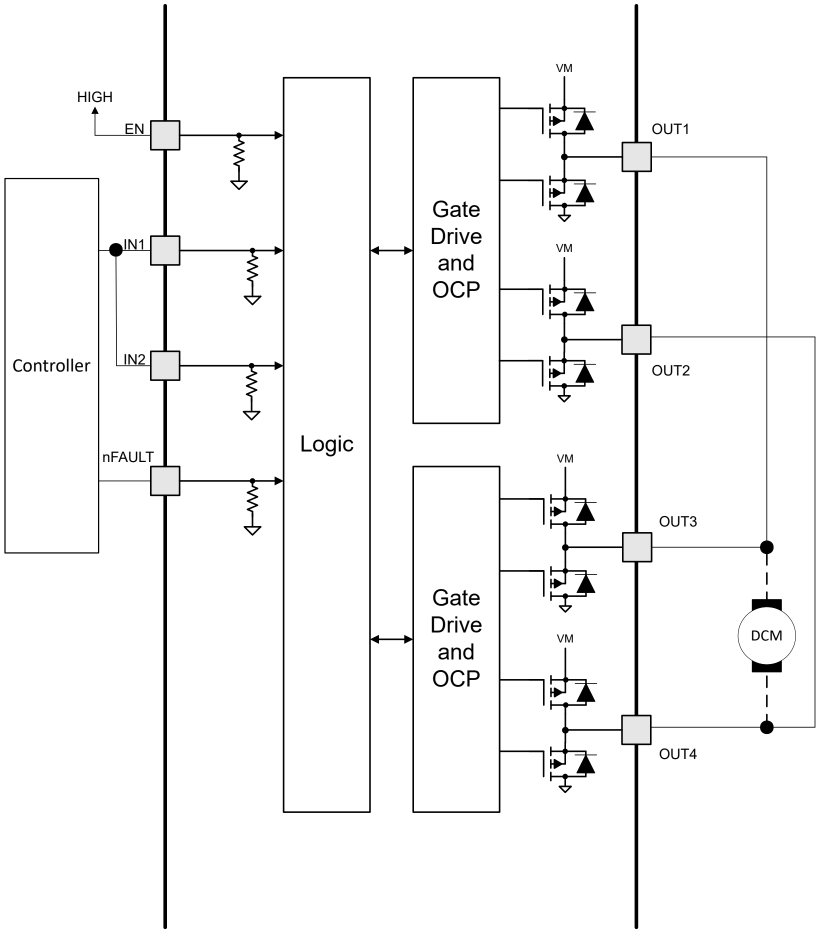

図 7-8. Parallel Mode Operation: DRV8421B

7.3.4 Protection Circuits

The DRV8421 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.4.1 OCP

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled. In addition, in DRV8421B, the nFAULT pin is driven low. The device remains disabled until the retry time t_{RETRY} occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event.

7.3.4.2 TSD

If the die temperature exceeds safe limits T_{TSD}, all FETs in the H-bridge are disabled. In addition, in DRV8421B, the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin in DRV8421B is released after operation has resumed.

7.3.4.3 UVLO

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_{VM} rises above the UVLO rising threshold. In DRV8421B, the nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

表 7-5. Fault Handling

FAULT	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	nFAULT unlatched (DRV8421B only)	Disabled	Shut down	System and fault clears on recovery
Overcurrent (OCP)	nFAULT unlatched (DRV8421B only)	Disabled	Operating	System and fault clears on recovery and motor is driven after time, t_{RETRY}
Thermal shutdown (TSD)	nFAULT unlatched (DRV8421B only)	Disabled	Operating	System and fault clears on recovery

7.4 Device Functional Modes

The DRV8421A is active until power is switched off. The DRV8421B is active until power is switched off or unless the EN pin is brought logic low which forces the device into sleep mode. In sleep mode, the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse EN pin before the device goes to sleep mode. The DRV8421B is brought out of sleep mode automatically if EN pin is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the VM UVLO threshold (V_{UVLO}), the output driver and internal logic are reset.

表 7-6. Functional Modes

MODE	CONDITION	H-BRIDGE	VINT
Operating	$4 V < V_{VM} < 18 V$ nSLEEP pin = 1	Operating	Operating
Sleep	$4 V < V_{VM} < 18 V$ EN pin = 0	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8421 is used in stepper or brushed DC motor control.

8.2 Typical Application

The user can configure the DRV8421 with the following design procedure.

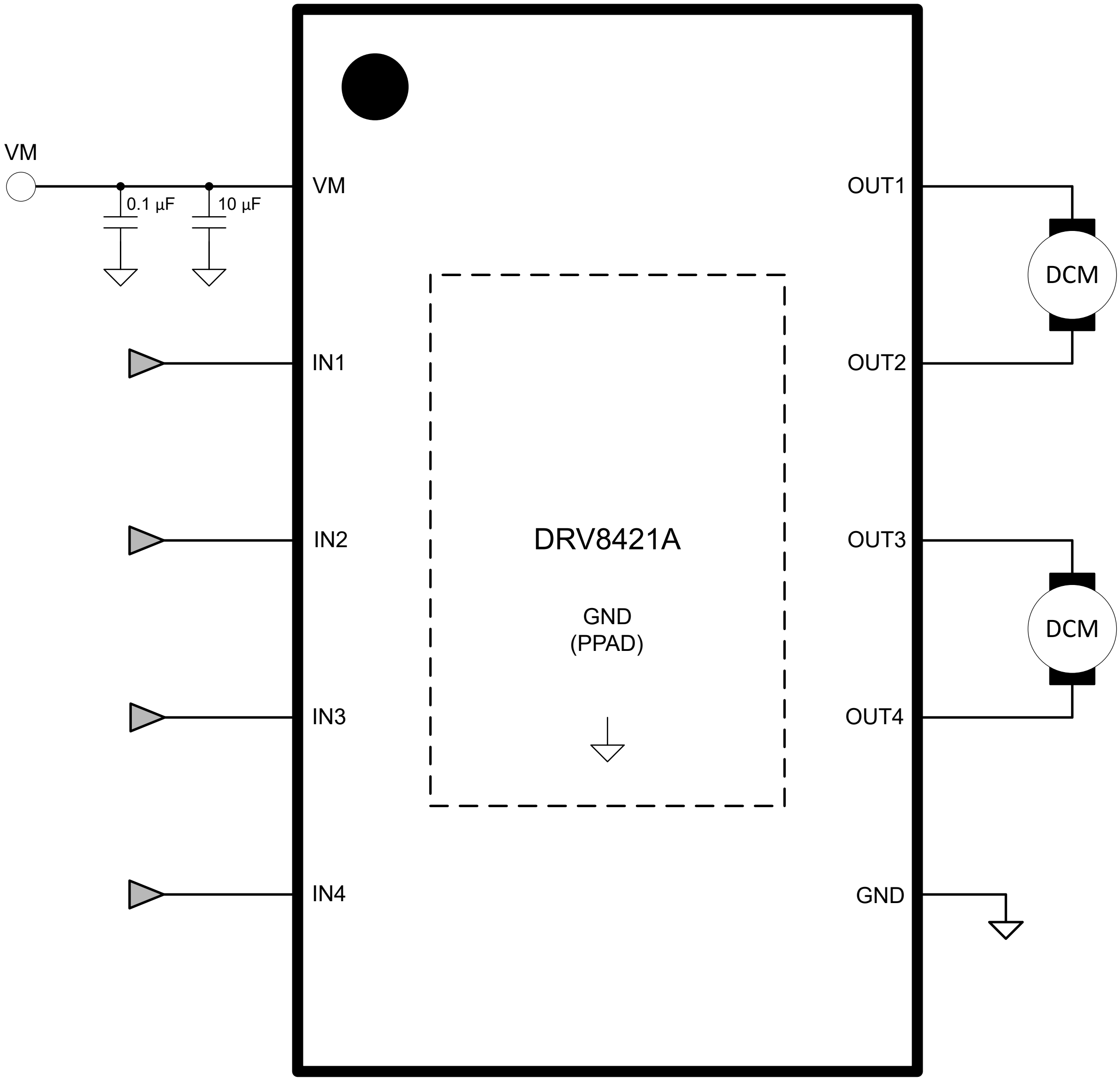

図 8-1. Typical Application Schematic: 4-wire input version

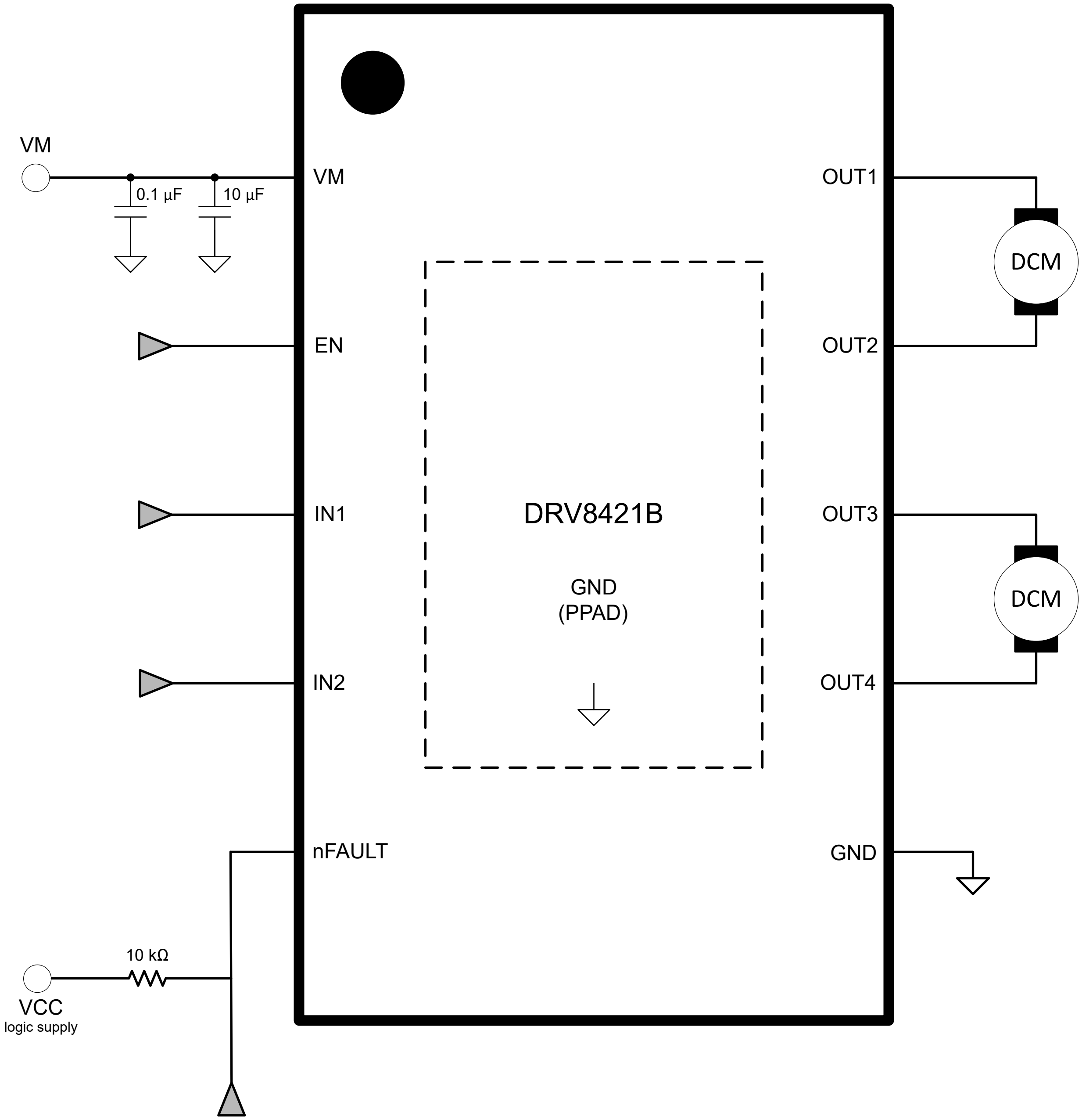

図 8-2. Typical Application Schematic: 2-wire input version

8.2.1 Design Requirements

表 8-1 gives design input parameters for system design.

表 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	12 V
Supply voltage range		4 to 18 V
Motor winding resistance	R_L	3 Ω/phase
Motor winding inductance	L_L	330 µH/phase

8.2.2 Application Curves

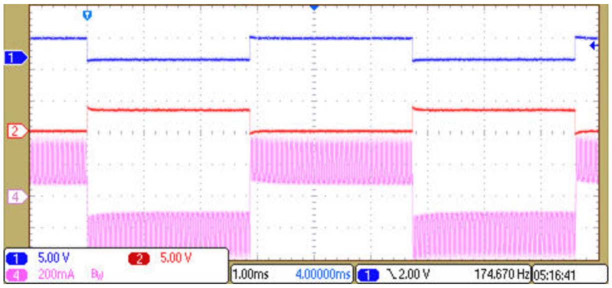

図 8-3. Stepper Mode Operation

8.3 Power Supply Recommendations

The DRV8421 is designed to operate from an input voltage supply (V_{VM}) range between 4 and 18V. Place a 0.1µF ceramic capacitor rated for VM as close to the DRV8421 as possible. In addition, the user must include a bulk capacitor of at least 10µF on VM.

8.3.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

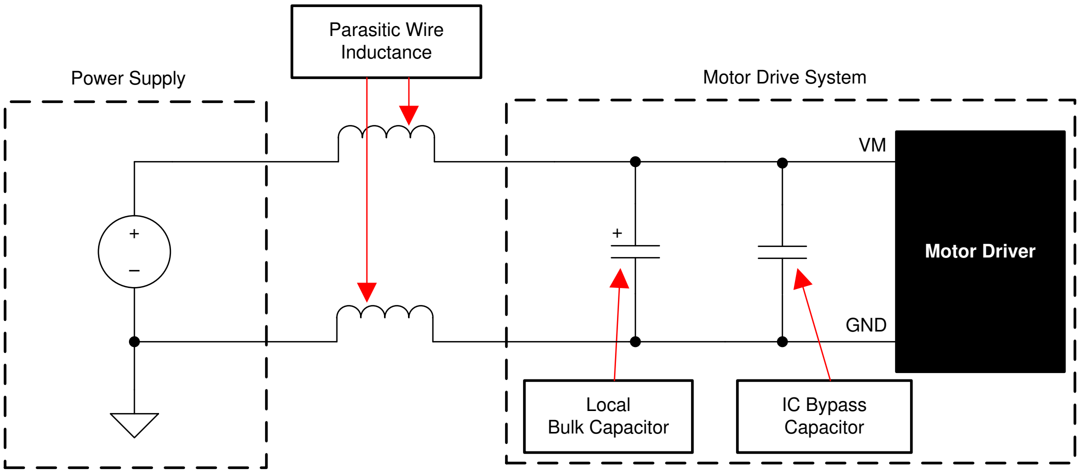

図 8-4. Setup of Motor Drive System With External Power Supply

8.4 Layout

8.4.1 Layout Guidelines

Bypass the VM terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

8.4.2 Layout Example

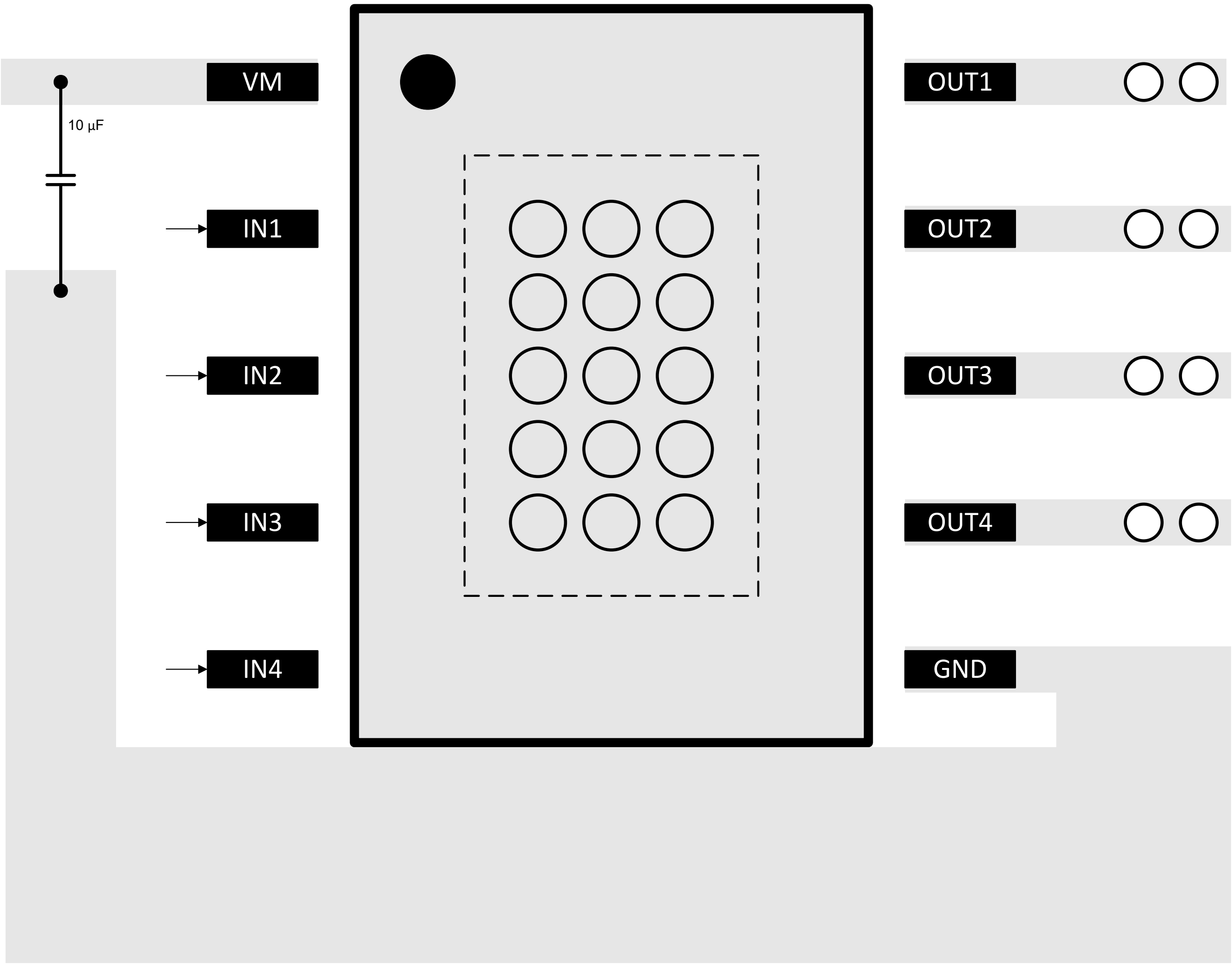

図 8-5. Layout Recommendation: DRV8421A

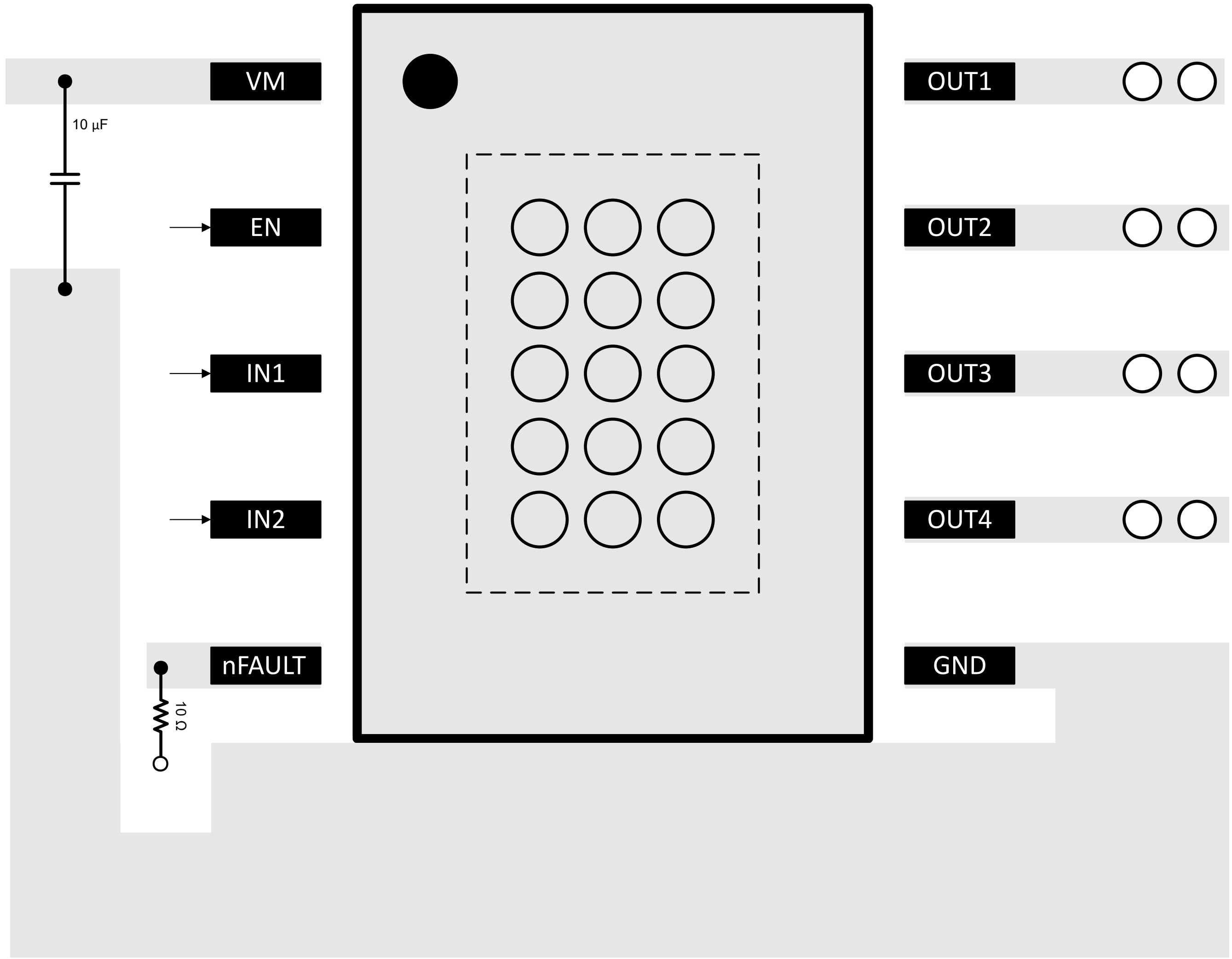

図 8-6. Layout Recommendation: DRV8421B

9 Device and Documentation Support

9.1 Community Resources

9.2 Trademarks

すべての商標は、それぞれの所有者に帰属します。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8421ADGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	8421A	Samples
DRV8421BDGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	8421B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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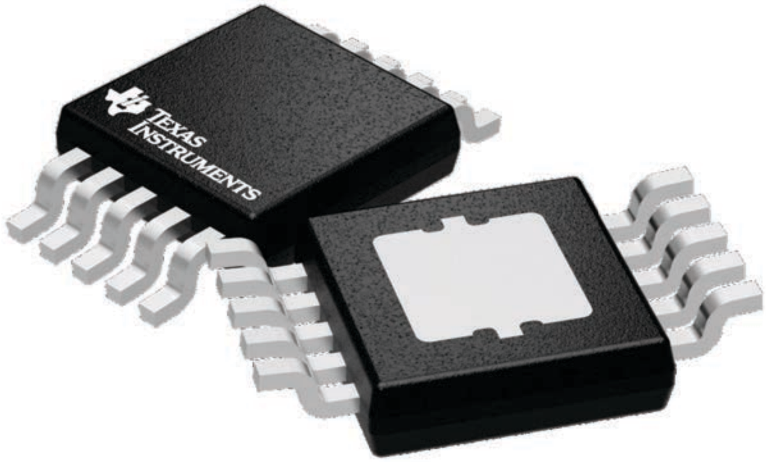
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

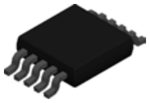
DGQ 10 **PowerPAD™ HVSSOP - 1.1 mm max height**

3 x 3, 0.5 mm pitch PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

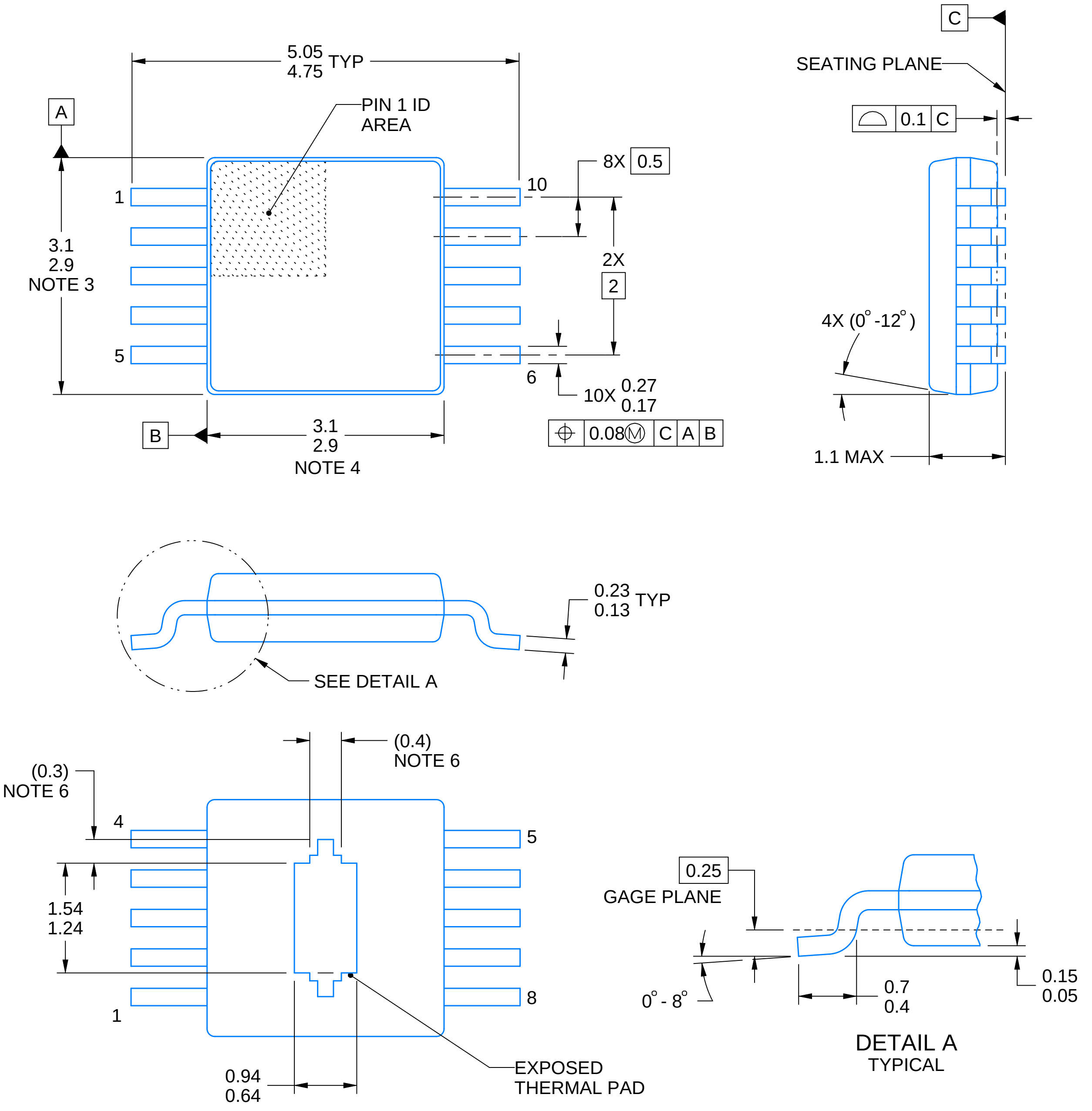
DGQ0010J



PACKAGE OUTLINE

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

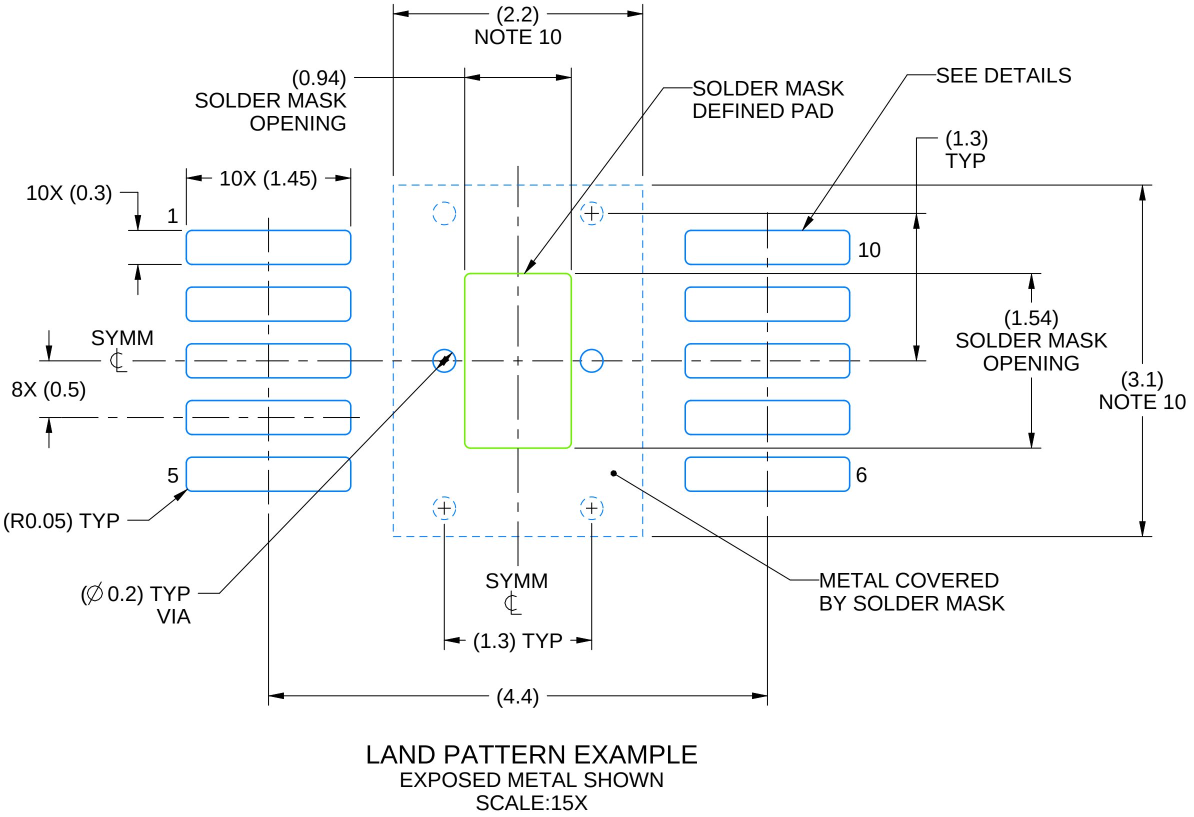


4230014/A 09/2023

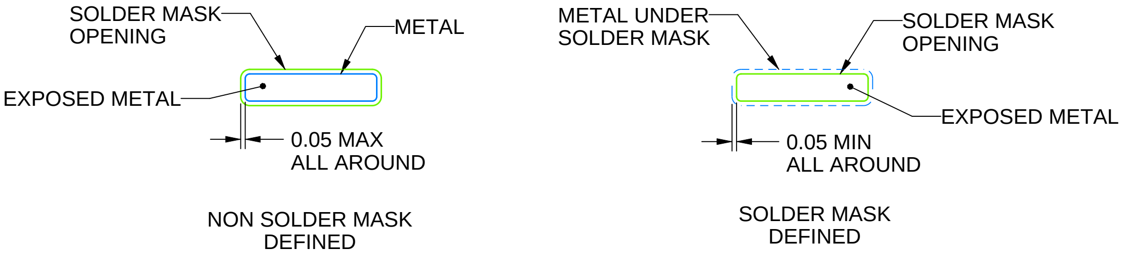
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

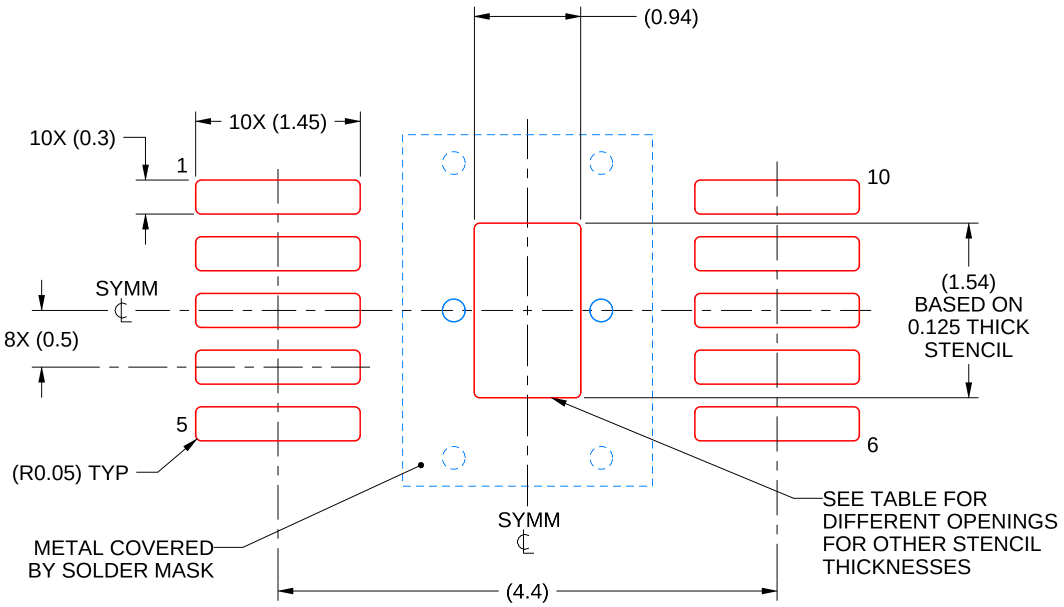


SOLDER MASK DETAILS

4230014/A 09/2023

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.05 X 1.72
0.125	0.94 X 1.54 (SHOWN)
0.150	0.86 X 1.41
0.175	0.79 X 1.30

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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