TEXAS INSTRUMENTS
DRV8845
JAJSM95A – MAY 2023 – REVISED DECEMBER 2023

DRV8845：38V、1.5A クワッド H-ブリッジ・モーター・ドライバ、スマート・チューン・テクノロジー付き

1 特長

- 4 つの H-ブリッジを統合
- さまざまな構成を駆動可能
  - 2 つのステッピング・モーター
  - 4 つのブラシ付き DC モーター
  - 3 つのブラシ付き DC モーター
  - 1 つのステッピング・モーターと 2 つのブラシ付き DC モーター
  - 1 つのステッピング・モーターと 1 つのブラシ付き DC モーター
- 他のベンダの類似のドライバと**互換性のあるフットプリントとソフトウェア**
- 動作電源電圧範囲：**4.5V～38V**
- 低い $R_{DS(ON)}$：24V、25℃で **900mΩ** HS + LS
- ブリッジごとのフルスケール電流 **1.5A**
- 業界標準の **PHASE/Ixx** インターフェイス
- 同期整流
- ステッピング・モーターのフル、1/2、1/4 ステップ動作
- DC モーターの順方向、逆方向、惰行モード
- スマート・チューン・ディケイによるスムーズで静かな動作
- 3.3V および 5V のロジック入力をサポート
- 保護機能
  - VM 低電圧誤動作防止 (UVLO)
  - チャージ・ポンプ低電圧検出 (CPUV)
  - 過電流保護 (OCP)
  - サーマル・シャットダウン (OTSD)

2 アプリケーション

- IP ネットワーク・カメラ
- ブラシ付き DC モーター
- プリンタとスキャナ
- 医療用アプリケーション
- ATM、通貨計数機、EPOS
- オフィスおよびホーム・オートメーション
- 大型および小型家電

3 概要

DRV8845 デバイスは、さまざまな産業用アプリケーションに適したクワッド・フルブリッジ・モーター・ドライバです。このデバイスは、最大 2 つのステッピング・モーター、または最大 4 つのブラシ付き DC モーターの駆動に使用できます。各フルブリッジ出力の定格は、最大 1.5A および 38V です。DRV8845 には、パルス幅変調 (PWM) 電流レギュレータに加えて 2 ビットの非線形 DAC (デジタル・アナログ・コンバータ) が含まれており、ステッピング・モーターをフル、ハーフ、1/4 ステップで、DC モーターを順方向、逆方向、惰行モードで制御できます。

PWM 電流レギュレータは、スマート・チューン・ディケイ・モードを使用して、モーターの可聴ノイズと振動を低減し、精度を向上し、消費電力を低減します。内部の同期整流制御回路により、PWM 動作中の消費電力が改善されます。

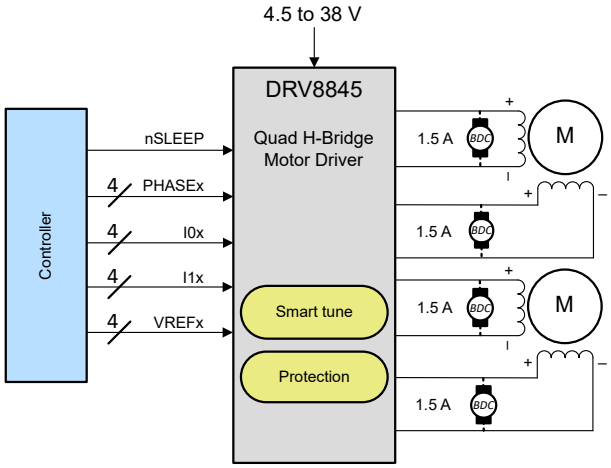
保護機能には、ヒステリシス付きのサーマル・シャットダウン (OTSD)、低電圧誤動作防止 (UVLO)、過電流保護 (OCP) が含まれます。特別な電源投入シーケンスは必要ありません。

DRV8845 は 6mm × 6mm の 36 ピン QFN パッケージで供給され、放熱性能を強化するために露出パッドが付属しています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DRV8845RHHR	QFN (36)	6mm × 6mm

(1) 巻末の注文情報を参照してください。



DRV8845 の概略回路図

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4 Device Comparison

表 4-1. Device Comparison Table

Device Name	Drives DC motor	Drives Stepper	Interface	Microstep	Current sensing
DRV8849	No	Yes	STEP/DIR	Up to 1/256	Internal sensing
DRV8845	Yes	Yes	PHASE/Ixx	Up to 1/4, higher microstepping by VREF pin	Sense Resistor

5 Pin Configuration and Functions

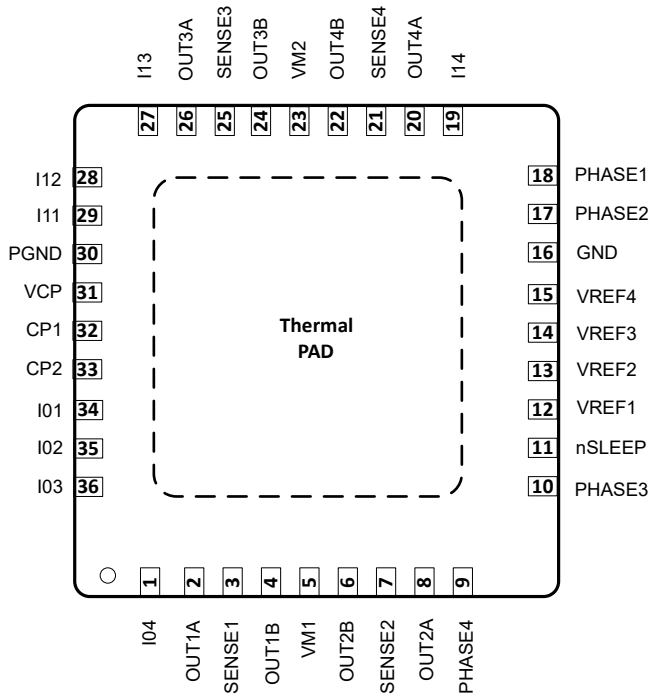


図 5-1. RHH Package, 36-Pin QFN, Top View DRV8845

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	QFN		
I04	1	I	Control Input for H-Bridge 4
OUT1A	2	O	H-Bridge 1 Output A
SENSE1	3	O	Sense resistor terminal for H-Bridge 1
OUT1B	4	O	H-Bridge 1 Output B
VM1	5	P	Supply Voltage. VM1 should be connected to VM2 pin close to the device.
OUT2B	6	O	H-Bridge 2 Output B
SENSE2	7	O	Sense resistor terminal for H-Bridge 2
OUT2A	8	O	H-Bridge 2 Output A
PHASE4	9	I	Control Input for H-Bridge 4. Leave this pin OPEN when H-Bridge 3 and H-Bridge 4 are paralleled.
PHASE3	10	I	Control Input for H-Bridge 3. When H-bridge 3 and 4 are paralleled, PHASE3 is used to control the combined H-bridge.
nSLEEP	11	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
VREF1	12	I	Reference voltage input to set the full scale chopping current in H-bridge 1
VREF2	13	I	Reference voltage input to set the full scale chopping current in H-bridge 2
VREF3	14	I	Reference voltage input to set the full scale chopping current in H-bridge 3. VREF3 controls the current of the combined bridge when H-Bridge 3 and H-Bridge 4 are paralleled.
VREF4	15	I	Reference voltage input to set the full scale chopping current in H-bridge 4. Voltage on this pin is ignored when H-Bridge 3 and H-Bridge 4 are paralleled.

表 5-1. Pin Functions (続き)

PIN		I/O(1)	DESCRIPTION
NAME	QFN		
GND	16	G	Analog ground
PHASE2	17	I	Control Input for H-Bridge 2
PHASE1	18	I	Control Input for H-Bridge 1
I14	19	I	Control Input for H-Bridge 4
OUT4A	20	O	H-Bridge 4 Output A
SENSE4	21	O	Sense resistor terminal for H-Bridge 4
OUT4B	22	O	H-Bridge 4 Output B
VM2	23	P	Supply Voltage. VM2 should be connected to VM1 pin close to the device.
OUT3B	24	O	H-Bridge 3 Output B
SENSE3	25	O	Sense resistor terminal for H-Bridge 3
OUT3A	26	O	H-Bridge 3 Output A
I13	27	I	Control Input for H-Bridge 3. When H-bridge 3 and 4 are paralleled, I13 is used to control the combined H-bridge.
I12	28	I	Control Input for H-Bridge 2
I11	29	I	Control Input for H-Bridge 1
PGND	30	G	Power ground
VCP	31	P	Reservoir capacitor terminal
CP1	32	P	Charge pump capacitor terminal
CP2	33	P	Charge pump capacitor terminal
I01	34	I	Control Input for H-Bridge 1
I02	35	I	Control Input for H-Bridge 2
I03	36	I	Control Input for H-Bridge 3. When H-bridge 3 and 4 are paralleled, I03 is used to control the combined H-bridge.
PAD	-	-	Exposed pad for enhanced thermal performance. Should be soldered to the PCB.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VMx)	–0.3	40	V
Charge pump voltage (VCP, CP1)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CP2)	–0.3	V_{VM}	V
Sleep mode input voltage (nSLEEP)	-0.3	5.75	V
Control input voltage	–0.3	5.75	V
SENSEx pin voltage (V_{SENSEx})	-0.5	0.5	V
SENSEx pin voltage (V_{SENSEx}) for < 1 µs	-2.5	2.5	V
Reference input pin voltage (VREFx)	–0.3	5.75	V
Continuous phase node pin voltage (OUTxA, OUTxB)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (OUTxA, OUTxB)	–3	V_{VM} + 3	V
Output current	0	1.5	A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (1)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	38	V
V_I	Control input voltage	0	5.5	V
V_{REFx}	Reference voltage (VREFx)	0	1.5	V
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC		RHH	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W

THERMAL METRIC		RHH	UNIT
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
I_{VM}	VM operating supply current	nSLEEP = 1, I_{OUT} = 0 mA, outputs on, PWM = 50 kHz, DC = 50%		9	14	mA
		nSLEEP = 1, Outputs off		3.5	4.5	mA
		nSLEEP = 0		1.3	3	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.62	0.8	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.62	0.8	ms
CHARGE PUMP (VCP, CP1, CP2)						
V_{VCP}	VCP operating voltage	V_{VM} > 6 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO, nSLEEP = 1		380		kHz
LOGIC-LEVEL INPUTS						
V_{IL}	Input logic-low voltage		0		0.8	V
V_{IH}	Input logic-high voltage		2		5.5	V
V_{HYS}	Input logic hysteresis		140	270	400	mV
I_{INL}	Logic input low current	V_{IN} = 0 V	-1		1	µA
I_{INH}	Logic input high current	V_{IN} = 5 V			30	µA
t_{PD}	Propagation delay	PWM change to source on	300	600	900	ns
		PWM change to source off	150		700	ns
		PWM change to sink on	300	600	900	ns
		PWM change to sink off	150		700	ns
MOTOR DRIVER OUTPUTS						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1. 2 A		450	550	mΩ
		T_J = 125 °C, I_O = -1.2 A		700	850	mΩ
		T_J = 150 °C, I_O = -1.2 A		780	950	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1.2 A		450	550	mΩ
		T_J = 125 °C, I_O = 1.2 A		700	850	mΩ
		T_J = 150 °C, I_O = 1.2 A		780	950	mΩ
V_f	Body diode forward voltage	I_O = ± 1.2 A			1.2	V
I_{DSS}	Output Leakage	Outputs, V_{OUT} = 0 to VM	-2		7	µA
t_{SR}	Output rise/fall time	VM = 24V, I_O = 1.2 A, Between 10% and 90%		100		ns

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Dead time		90	425	600	ns
t_{BLANK}	Current sense blanking time (1)			1		µs
PWM CURRENT CONTROL (VREFx)						
I_{VREFx}	VREFx pin reference input Current	VREF = 1.5 V	-1		1	µA
t_{OFF}	PWM off-time			16		µs
ΔI_{TRIP}	Current trip accuracy	V_{VREFx} = 1.5 V, phase current = 100%	–2		2	%
		V_{VREFx} = 1.5 V, phase current = 67%	–3		3	
		V_{VREFx} = 1.5 V, phase current = 33%	-7		7	
PROTECTION CIRCUITS						
VM_{UVLO}	VM UVLO threshold	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.34	4.45	
$VM_{UVLO,HYS}$	VM UVLO hysteresis	Rising to falling threshold		90		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	2.5			A
t_{OCP}	Overcurrent deglitch time			2.1		µs
T_{OTSD}	Thermal shutdown	Die temperature T_J	155	165	175	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

(1) Guaranteed by design.

6.6 Typical Operating Characteristics

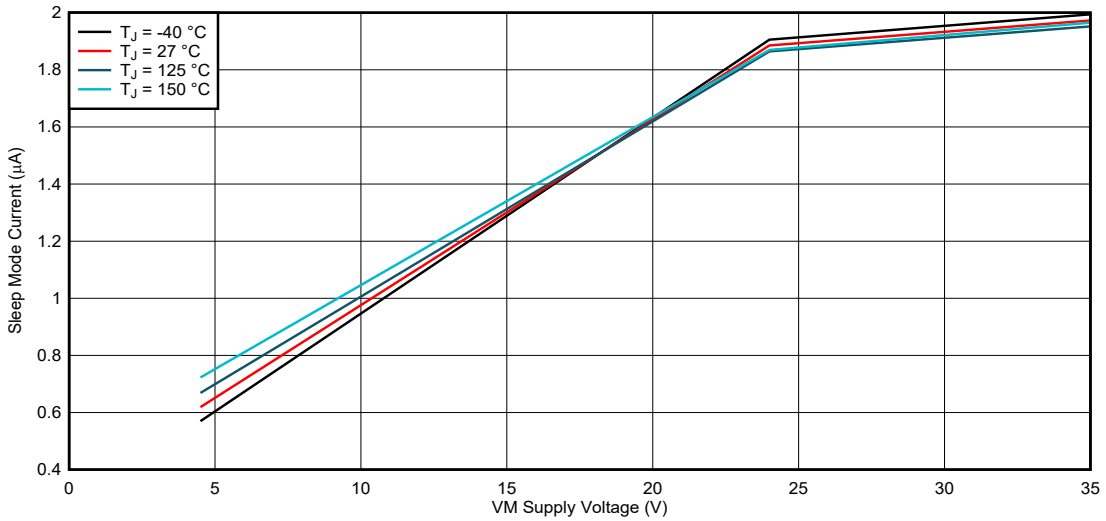


図 6-1. Sleep Mode Supply Current

6.6 Typical Operating Characteristics

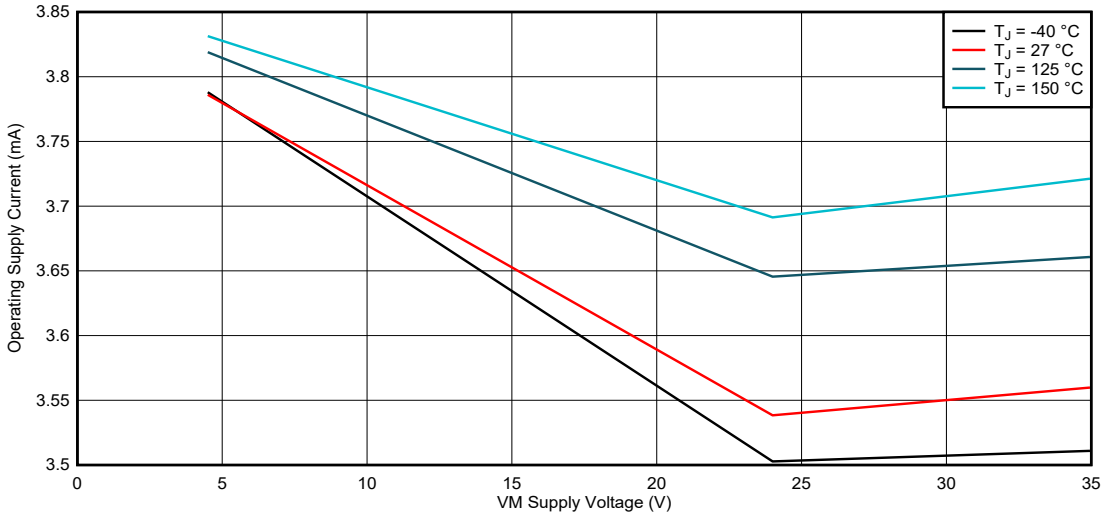


図 6-2. Operating Supply Current with Outputs OFF

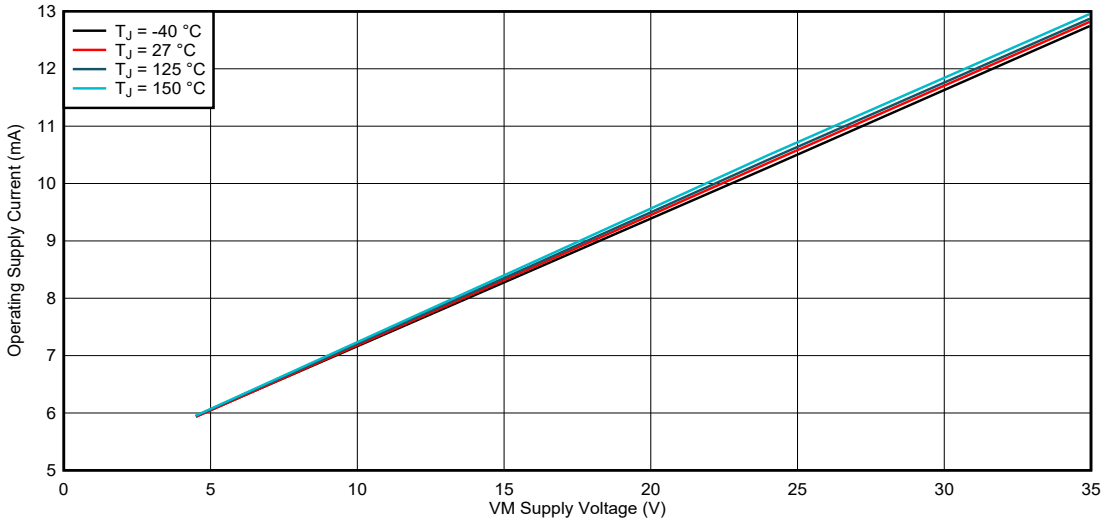


図 6-3. Operating Supply Current with Outputs ON

6.6 Typical Operating Characteristics

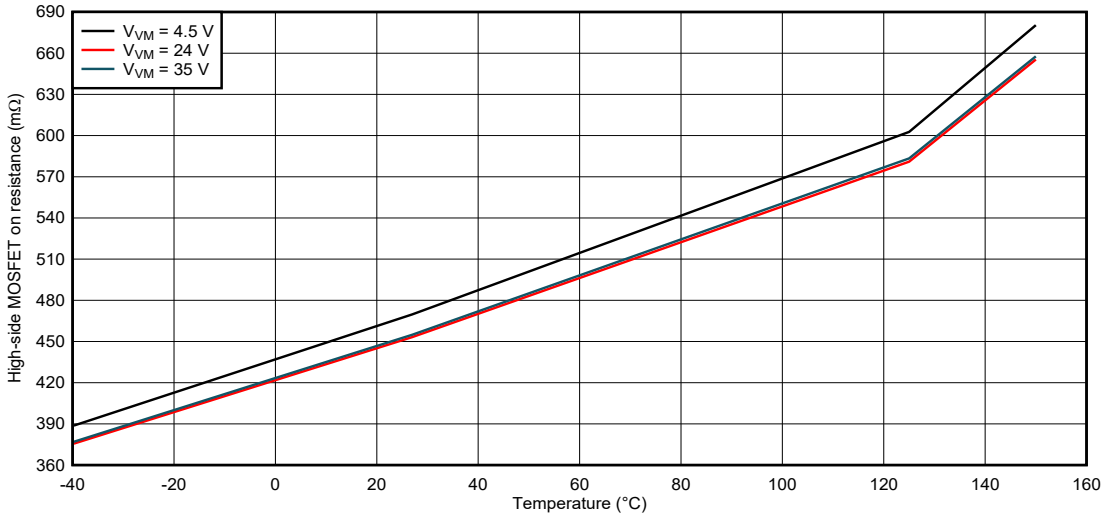


図 6-4. High-side FET on resistance

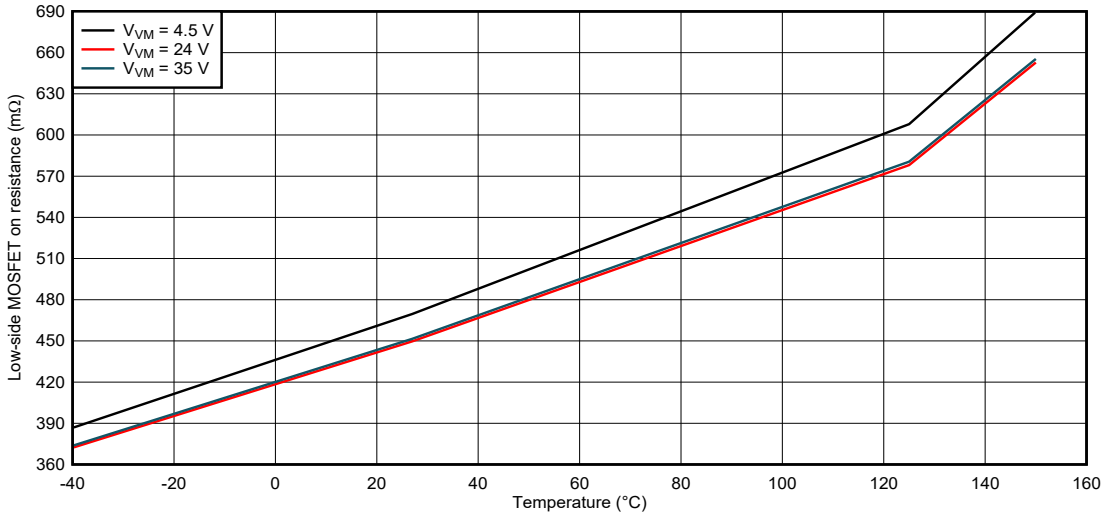


図 6-5. Low-side FET on resistance

7 Detailed Description

7.1 Overview

The DRV8845 is designed to operate two stepper motors, up to four DC motors, or one stepper and one or two DC motors. The device integrates four N-channel power MOSFET H-bridges. The DRV8845 is footprint and software compatible with similar quad H-Bridge motor drivers from other vendors. The DRV8845 can be powered with a supply voltage between 4.5 and 38 V. The device is capable of providing an output current up to 2.5-A peak or 1.5-A full-scale. The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The currents in each of the output full-bridges are regulated with pulse width modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor, R_{SENSEx} , and a reference voltage, VREFx.

A simple PHASE/I0/I1 interface allows easy interfacing to the controller circuit. With this interface, a stepper motor can be driven in full-step, half-step or quarter-step modes. Higher resolution step modes can be programmed by dynamically changing the voltage on the VREFx pins. Also, the DRV8845 supports driving brushed-DC motors in forward, reverse and coast modes. A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram

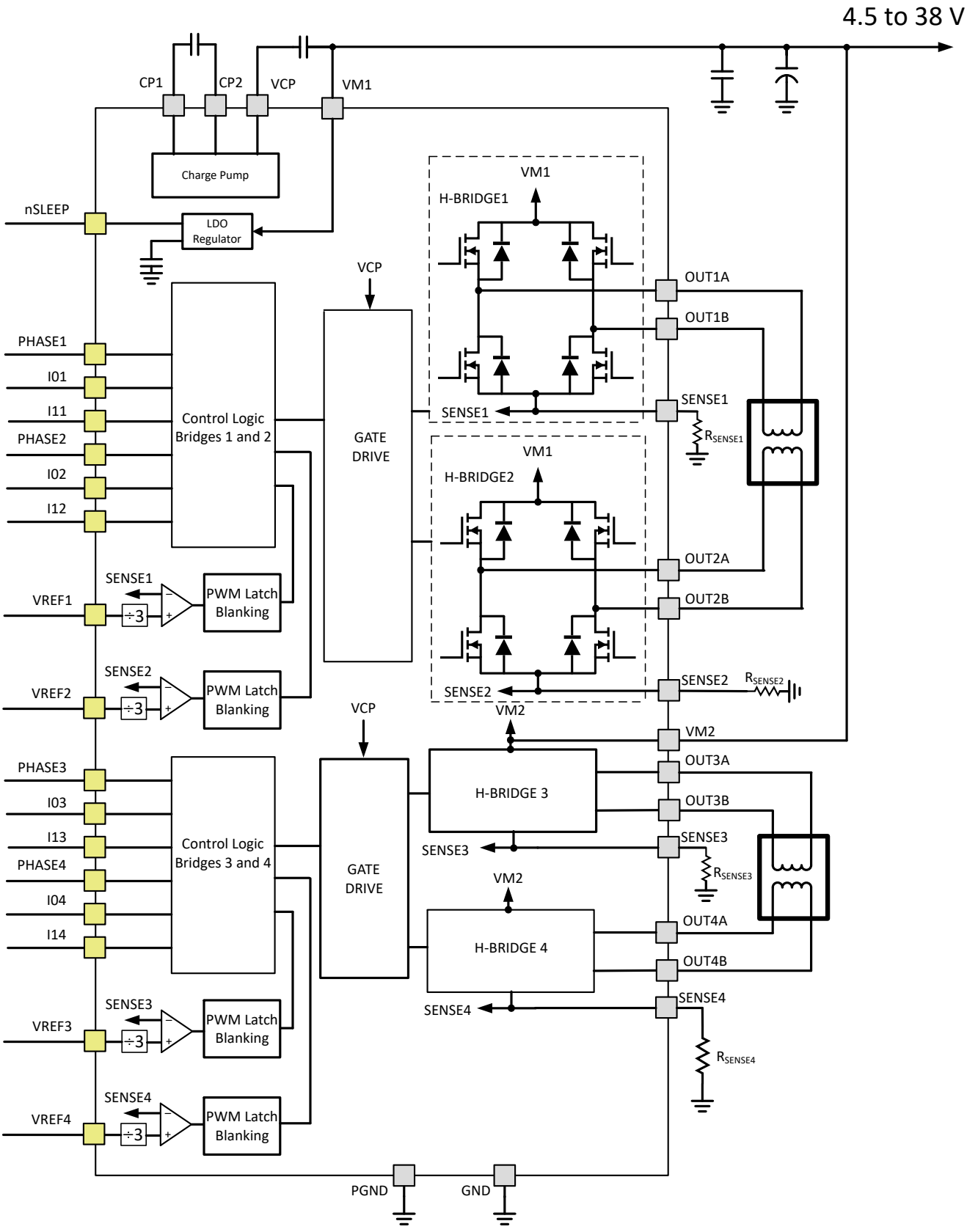


図 7-1. Functional Block Diagram

7.3 Feature Description

The following table shows the recommended values of the external components for the driver.

表 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM1	PGND	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM2	PGND	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VCP}	VCP	VM1	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CP1	CP2	X7R, 0.022-µF, VM-rated ceramic capacitor
R_{REF1}	VREFx	VCC (1)	Resistor to limit chopping current.
R_{REF2}	VREFx	GND	
R_{SENSEx}	SENSEx	GND	See the PWM Current Control section for details.

(1) VCC is not a pin on the device, but a VCC supply voltage can be used to set the VREF voltage.

7.3.1 Motor Configurations

Each of the four H-bridges have independent PWM current control circuitry, that makes the DRV8845 capable of driving the following configurations -

- Two stepper motors
- One stepper motor and two BDC motors
- Four BDC motors

In addition, H-bridge 3 and H-bridge 4 can be paralleled together. To enable this, PHASE4 must be left OPEN at start-up or when the device exits from sleep mode. By paralleling the two H-bridges, the DRV8845 supports two more configurations -

- One stepper motor (H-bridge 1 and 2) and one BDC motor (paralleled H-bridge 3, 4)
- Three BDC motors (H-bridge 1, H-bridge 2, paralleled H-bridge 3, 4)

Each H-bridge can deliver up to 1.5 A current. When paralleled, the combined H-bridge 3 and 4 can deliver up to 3 A current. Ensure OUT3A is shorted to OUT4A, OUT3B is shorted to OUT4B and SENSE3 is shorted to SENSE4 pin.

7.3.2 Stepper Control Logic

Control logic is implemented via the standard I0, I1, and PHASE interface. This logic allows for full, half, and quarter step modes. Each bridge also has an independent VREF input so that higher resolution step modes can be programmed by dynamically changing the voltage on the VREFx pins.

The PHASE inputs control the direction of current as shown in 表 7-2 -

表 7-2. PHASE Truth Table

PHASEx	OUTxA	OUTxB
L	L	H
H	H	L

The I0x, I1x inputs control the current flowing through the outputs as shown in 表 7-3 -

表 7-3. I0x, I1x Truth Table

I0x	I1x	Output Current
L	L	100%
H	L	67%
L	H	33%

表 7-3. I0x, I1x Truth Table (続き)

H	H	0

The step sequencing table for full step, half sep and quarter step modes is shown in 表 7-4 -

表 7-4. Step Sequencing Settings

Full	1/2	1/4	Phase 1 ($\%I_{TRIPMax}$)	I0x	I1x	PHASE	Phase 2 ($\%I_{TRIPMax}$)	I0x	I1x	PHASE
	1	1	0	H	H	X	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/67*	L/H*	L	1	100/67*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	1
2	4	7	100/67*	L/H*	L	1	100/67*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	X	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/67*	L/H*	L	0	100/67*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	0
4	8	15	100/67*	L/H*	L	0	100/67*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

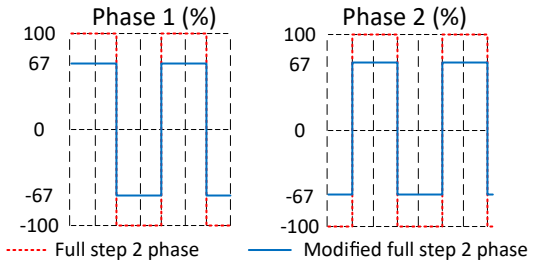


図 7-2. Step Sequencing for Full-Step Increments

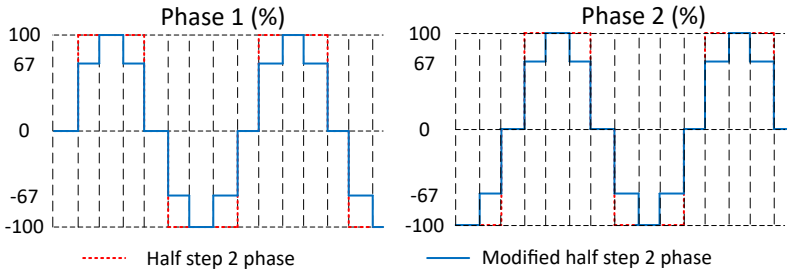


図 7-3. Step Sequencing for Half-Step Increments

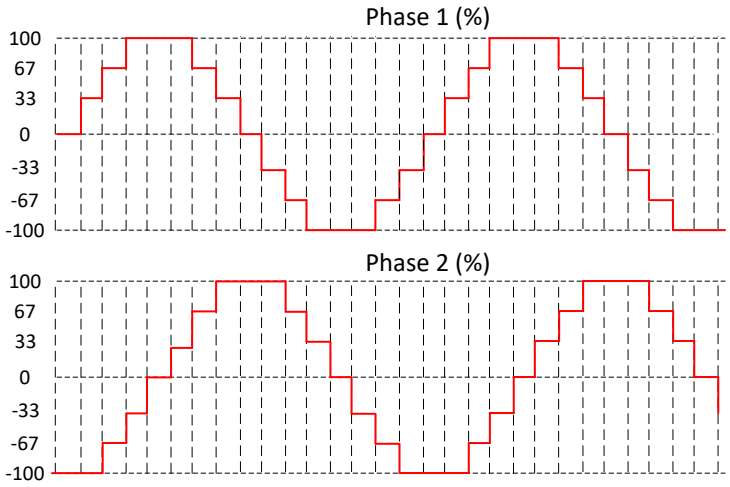


図 7-4. Step Sequence for Quarter-Step Increments

7.3.3 DC Motor Control

Control of the DC motors is accomplished by tying the I0x and I1x pins together, creating an equivalent ENABLE function with maximum current defined by the voltage on the corresponding VREF pin. The DC motors can be driven via a PWM signal on this enable signal, or on the corresponding PHASE pin. Motor control includes forward, reverse, and coast. The turth table is shown in 表 7-5 -

表 7-5. DC Motor truth table

ENABLEx (I0x = I1x)	PHASEx	OUTxA	OUTxB	Description
H	X	Hi-z	Hi-z	Coast
L	L	L	H	Reverse
L	H	H	L	Forward

When H-bridge 3 and 4 are paralleled, PHASE3, I03 and I13 are used to control the combined H-bridge. VREF3 alone controls the current of the combined H-bridge, and the voltage on VREF4 pin is ignored.

As mentioned in セクション 7.3.1, H-bridge 3 and H-bridge 4 can be paralleled together to drive a single DC motor with higher current. To enable this, ensure following steps -

- PHASE4 must be left OPEN at start-up or when the device exits from sleep mode.
- Leave I04 and I14 OPEN as well. The combined H-bridge is controlled by PHASE3, I03 and I13.
- Ensure OUT3A is shorted to OUT4A and OUT3B is shorted to OUT4B.
- Short SENSE3 to SENSE4 pin.
- VREF3 voltage alone controls the I_{TRIP} of the combined H-bridge. Leave VREF4 OPEN.
- $I_{TRIPMax} = 2 \times VREF3 / (3 \times R_{SENSE})$, where R_{SENSE} is the sense resistor connected from the shorted SENSE pin to ground.

Each H-bridge can deliver up to 1.5 A current. When paralleled, the combined H-bridge 3 and 4 can deliver up to 3 A current.

7.3.4 PWM Current Control

Each H-bridge is controlled by a PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink MOSFET outputs are enabled and current flows through the motor winding and R_{SENSEx}. When the voltage across the current sense resistor equals the voltage on the VREFx pin, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting is set by the selection of R_{SENSEx} and the voltage at the VREFx input with a transconductance function approximated by:

$I_{TRIPMax}$ = VREF / (3 × R_{SENSE})

When H-bridge 3 and H-bridge 4 are paralleled, and SENSE3 and SENSE4 pins are shorted together, the maximum value of current limiting is set by:

$I_{TRIPMax}$ = 2 × VREF3 / (3 × R_{SENSE}), where R_{SENSE} is the sense resistor from the shorted SENSE pin.

Each current step is a percentage of the maximum current, $I_{TRIPMax}$. The actual current at each step I_{TRIP} is approximated by:

I_{TRIP} = (% $I_{TRIPMax}$ / 100) x $I_{TRIPMax}$

where % $I_{TRIPMax}$ is given in the Step Sequencing table.

It is critical to ensure that the maximum rating of ± 500 mV on each SENSEx pin is not exceeded.

7.3.5 Current Regulation and Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the chopping current threshold is reached. This is shown in 図 7-5, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

- In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in 図 7-5, item 3.
- In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in 図 7-5, Item 2.

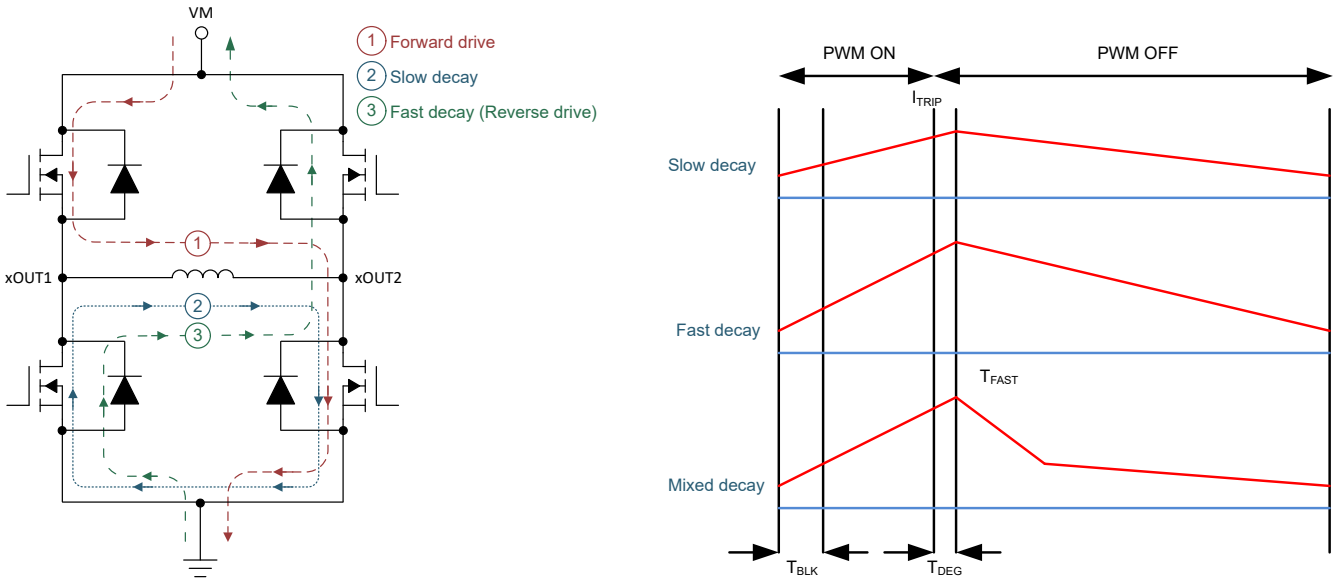


図 7-5. Decay Modes

The DRV8845 features the smart tune Dynamic Decay mode for current control. The smart tune is an advanced current regulation scheme compared to traditional mixed decay modes. Smart tune helps the stepper motor driver adjust the decay scheme based on changes in operating factors such as:

- Motor winding resistance and inductance
- Motor aging
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

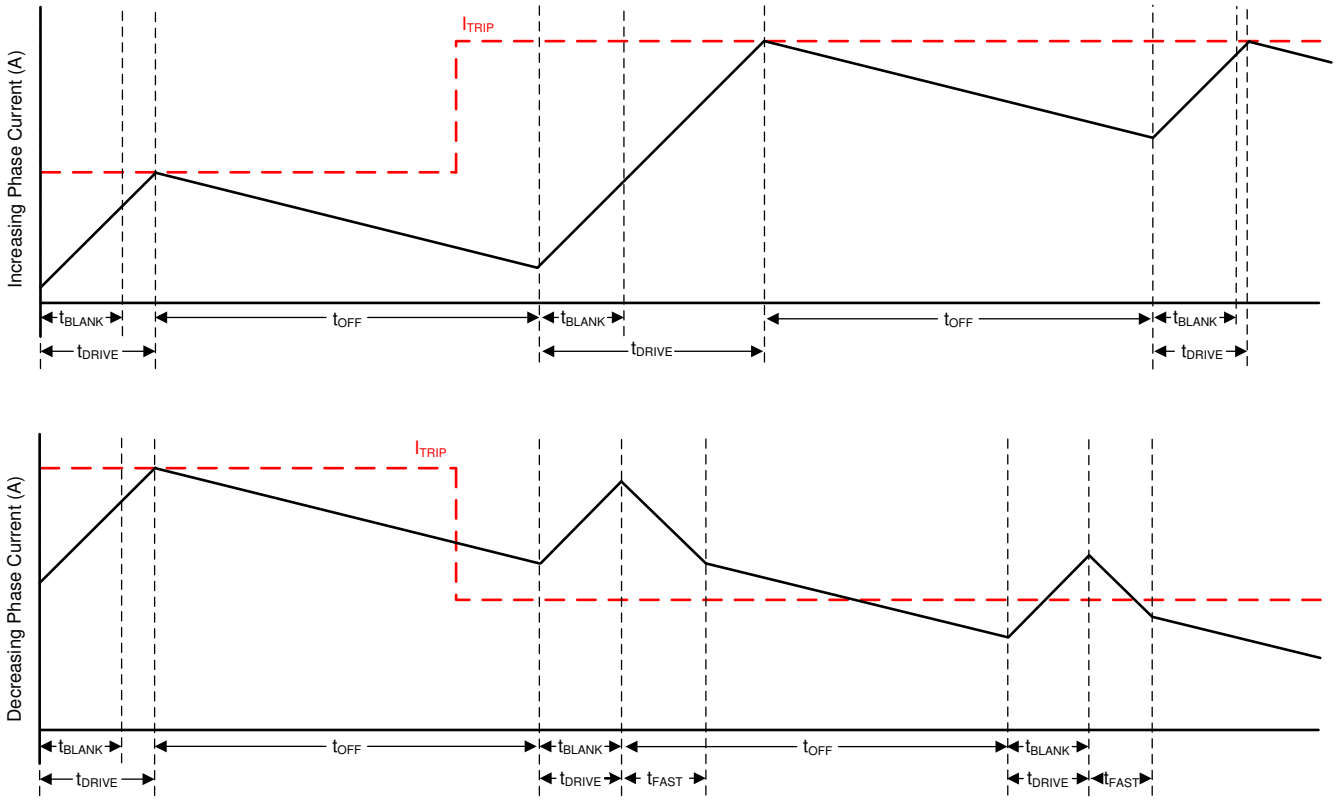


図 7-6. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay dynamically adjusts the fast decay percentage of the total mixed decay time. This eliminates the need for motor decay tuning by automatically determining the best mixed decay setting that results in the lowest ripple and best performance for the motor.

The fast decay percentage is optimized iteratively each PWM cycle. If the motor current overshoots the target I_{TRIP} level, then the mixed decay mode becomes more aggressive (by increasing fast decay percentage) on the next cycle to prevent loss of current regulation. If a long drive time must occur to reach the target I_{TRIP} level, the decay mode becomes less aggressive (by reducing fast decay percentage) on the next cycle to operate with less ripple. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly. Smart tune Dynamic Decay operates with fixed 16µs OFF time.

7.3.6 Blanking Time

This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The blank time, t_{BLANK} , is approximately 1 µs.

7.3.7 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CP1 and CP2 pins to act as the flying capacitor.

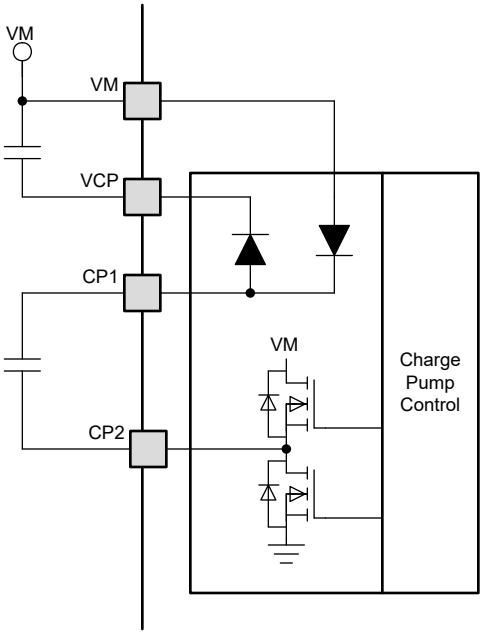


図 7-7. Charge pump

7.3.8 Logic-Level Pin Diagram

図 7-8 gives the input structure for logic-level pins PHASEx, I0x, I1x and nSLEEP.

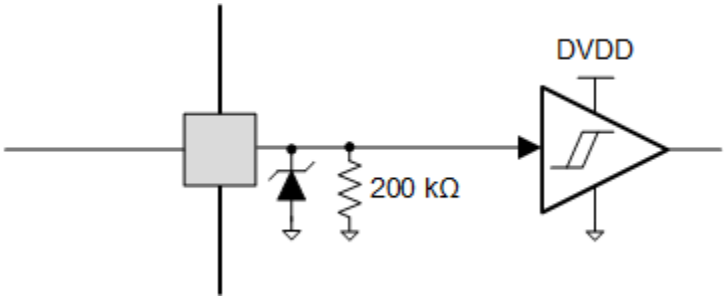


図 7-8. Logic-level Input Pin Diagram

7.3.9 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events. In the event of a fault, all the outputs are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

7.3.9.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VMx pins falls below the UVLO threshold voltage, all the outputs are disabled. The charge pump is disabled in this condition. Normal operation resumes when the VM undervoltage condition is removed.

7.3.9.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled. The charge pump remains active during this condition. Normal operation resumes when the VCP undervoltage condition is removed.

7.3.9.3 Overcurrent Protection (OCP)

In the event of an output short, an analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If the current limit persists for longer than the t_{OCP} time, all MOSFETs are disabled. The charge pump remains active during this condition.

Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse, a VM power cycling or nSLEEP cycling.

7.3.9.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}), all MOSFETs are disabled. Normal operation resumes after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

7.3.9.5 Fault Condition Summary

表 7-6. Fault Condition Summary

FAULT	CONDITION	H-BRIDGEs	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	Disabled	Disabled	Reset (VM < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	Disabled	Operating	Operating	VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	Disabled	Operating	Operating	Latched
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	Disabled	Disabled	Operating	Automatic: T_J < $T_{OTSD} – T_{HYS\_OTSD}$

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 nSLEEP Reset Pulse

A fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram. This reset pulse does not affect the status of the charge pump or other functional blocks.

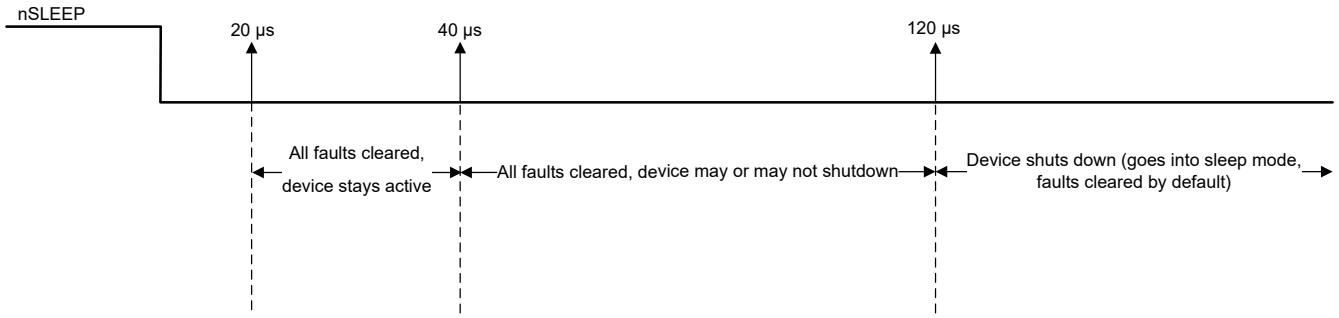


図 7-9. nSLEEP Reset Pulse

7.4.4 Functional Modes Summary

表 7-7 lists a summary of the functional modes.

表 7-7. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGEs	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 38 V	nSLEEP pin = 0	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 38 V	nSLEEP pin = 1	Operating	Operating	Operating

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DRV8845 can drive motors with the following configurations -

- Two stepper motors
- Four brushed-DC motors
- Three brushed-DC motors
- One stepper and two brushed-DC motors
- One stepper and one brushed-DC motor

8.2 Application Schematics

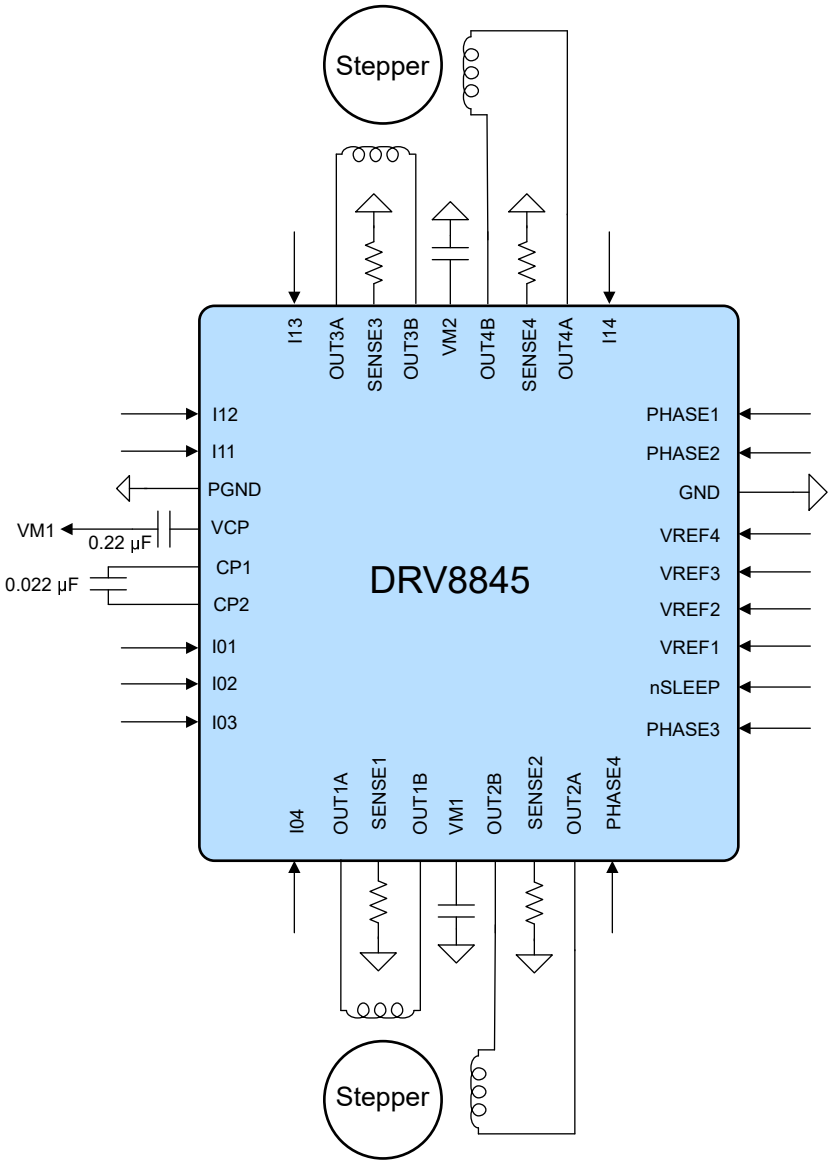


図 8-1. Application Schematic for Driving two Stepper Motors

8.3 Application Curves

CH3 = PHASE1,3 (5 V/div), CH6 = PHASE2,4 (5 V/div), CH1 = OUT1A (20 V/div), CH2 = OUT1B (20 V/div), CH7 = IOUT_1 (1 A/div), CH8 = IOUT_4 (1 A/div)

図 8-2. Driving two stepper motors in full-step

CH5 = IOUT_4 (1 A/div), CH6 = IOUT_3 (200 mA/div), CH7 = IOUT_1 (1 A/div), CH8 = IOUT_2 (1A/div), VREF1,2,4 = 1.62 V, VREF3 = 0.9 V, R_{SENSE1} = R_{SENSE2} = R_{SENSE4} = 0.36 Ω, R_{SENSE3} = 0.2 Ω

図 8-3. Driving four brushed-DC motors

CH1 = I01 (10 V/div), CH2 = I11 (10 V/div), CH3 = PHASE1 (10 V/div), CH5 = IOUT_4 (BDC 2, 2 A/div), CH6 = IOUT_3 (BDC 1, 2 A/div), CH7 = IOUT_1 (Stepper, 1 A/div), CH8 = IOUT_2 (Stepper, 1A/div), VREF1,2,4 = 1.62 V, VREF3 = 0.9 V, R_{SENSE1} = R_{SENSE2} = R_{SENSE4} = 0.36 Ω, R_{SENSE3} = 0.2 Ω

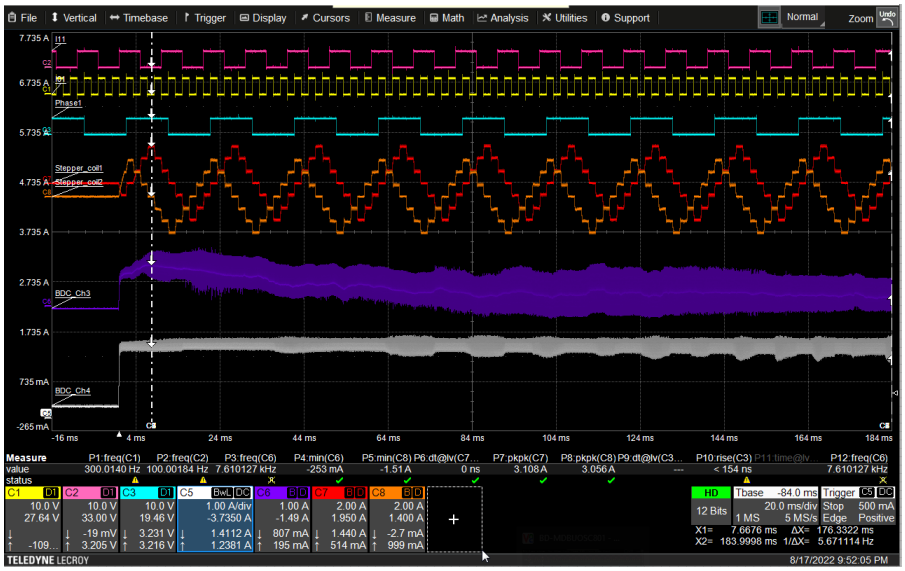


図 8-4. Driving one stepper in quarter-step and two brushed-DC motors

9 Layout

- A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- The device must be soldered directly onto the PCB. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias should be used to transfer heat to other layers of the PCB.
- It is important to have a low impedance single-point ground located very close to the device. Connect the exposed pad and the ground plane directly under the device ground.
- The input capacitors should be placed as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor.
- The sense resistors should have a very low impedance path to ground. SENSEx pins should have very short traces to the sense resistors and very thick, low impedance traces directly to the ground underneath the device. Ensure that the maximum voltage on the sense pins do not exceed +/- 500 mV.

9.1 Layout Guidelines

Follow the layout example of the DRV8845 EVM. The design files can be downloaded from the DRV8845EVM product folder.

9.2 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

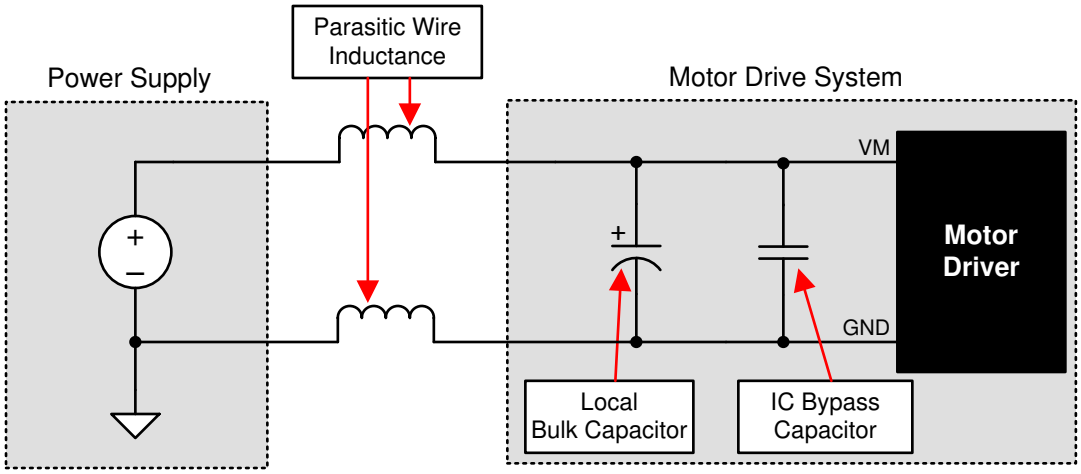


図 9-1. Example Setup of Motor Drive System With External Power Supply

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (December 2023)	Page
• Updated Current Regulation and Decay Mode section	17

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8845RHHR	ACTIVE	VQFN	RHH	36	4000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8845	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

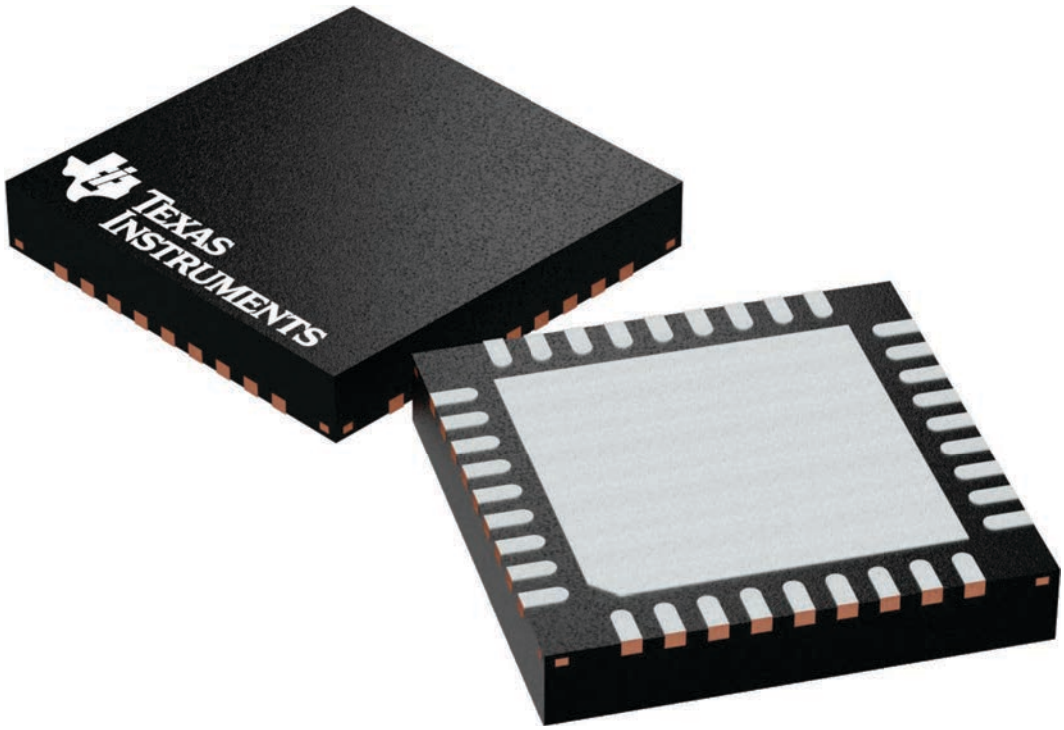
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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