DS150DF1610 12.5 to 15 Gbps 16-Channel Retimer

1 Features

- Pin-Compatible Family
  - DS150DF1610: 12.5 to 15G
  - DS125DF1610: 9.8 to 12.5G
  - DS110DF1610: 8.5 to 11.3G
- Fully Adaptive CTLE
- Self tuning DFE, with Optional Continuous Adaption
- Configurable VGA
- Adjustable Transmit V_{OD}
- Adjustable 3-tap Transmit FIR Filter
- On-chip AC Coupling on Receive Inputs
- Locks to Half/Quarter/Eighth Data Rates for Legacy Support
- On-chip Eye Monitor(EOM), PRBS Checker, Pattern Generator
- Supports JTAG Boundary Scan
- Programmable Output Polarity Inversion
- Input Signal Detection, CDR Lock Detection
- Single 2.5 V ±5% Power Supply
- SMBus Based Register Configuration
- Optional EEPROM Configuration
- 15 mm x 15 mm, 196-pin FCBGA Package
- Operating Temp Range : –10°C to +85°C

2 Applications

- Backplane/Midplane reach extension

3 Description

The DS150DF1610 is a sixteen-channel multi-rate retimer with integrated signal conditioning features. The device includes a fully adaptive Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), clock and data recovery (CDR), and a transmit FIR filter to enhance the reach and robustness over long, lossy, crosstalk impaired high speed serial links to achieve BER < 1×10^{-15}.

Each channel of the DS150DF1610 independently locks to serial data rates between 12.5 and 15 Gbps plus the divide by 2, 4 and 8 sub-multiples. A simple external oscillator (±100ppm) that is synchronous or asynchronous with the incoming data stream is used as a calibration clock.

A programmable transmit Finite Impulse Response (FIR) filter offers control of the pre-cursor, main tap and post-cursor for transmit equalization. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnects and backplanes with multiple connectors.

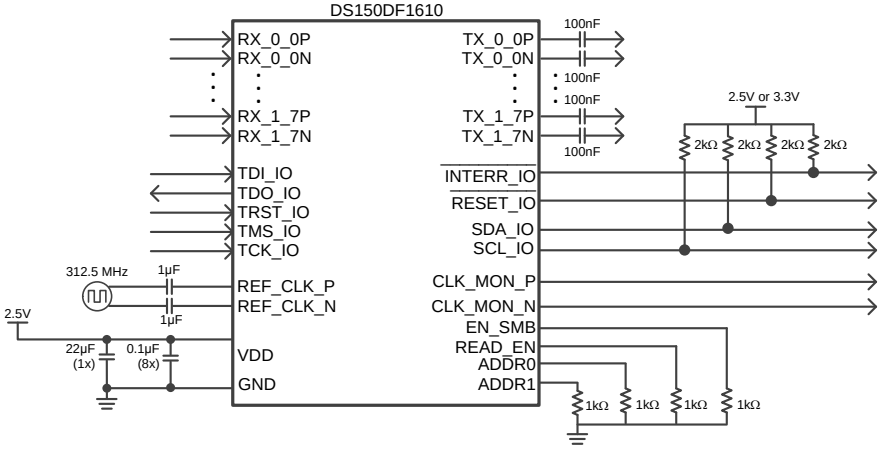
A non-disruptive mission mode eye-monitor feature allows link monitoring internal to the receiver. The built-in PRBS generator and checker compliment the internal diagnostic features to complete standalone BERT measurements. Built-in JTAG enables manufacturing tests.

To download the full datasheet, please send a request to: highspeed_datasheets@list.ti.com

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE NOM
DS150DF1610	FCBGA (196)	15.00 mm x 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	COMMENTS
November 2014	*	Initial Release

5 Device and Documentation Support

5.1 Trademarks

All trademarks are the property of their respective owners.

5.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designed devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

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