DS280BR820 低消費電力、28Gbps、8チャネル・リニア・リピータ

1 特長

- 8チャネルのマルチプロトコル・リニア・イコライザーで、最高28Gbpsのインターフェイスをサポート
- 低消費電力: 93mW/チャネル(標準値)
- ヒートシンク不要
- リニア均等化によりリンク・トレーニング、自動ネゴシエーション、FECパススルーをシームレスにサポート
- チャネルの範囲を、通常のACIS-to-ACIS能力よりも17dB以上拡張
- 非常に短いレイテンシ:100ps (標準値)
- 低い付加的ランダム・ジッタ
- 小型の8mm×13mm BGAパッケージにRX ACカップリングコンデンサを内蔵し、フロースルー配線が簡単
- 独自のピン配置により、パッケージの下に高速信号の配線が可能
- ピン互換のRetimerを利用可能
- 単一の2.5V ±5%電源
- –40℃～+85℃の動作温度範囲

2 アプリケーション

- バックプレーンおよびミッドプレーンの範囲拡張
- 光およびパッシブ銅線(100G-SR4/LR4/CR4)用のフロントポート・アイ・オープナー
- QSFP28、SFP28、CFP2、CFP4、CDFP

3 概要

DS280BR820は非常に消費電力が低く高パフォーマンスの8チャネル・リニア・イコライザーで、マルチレート、マルチプロトコルで最大28Gbpsのインターフェイスをサポートします。バックプレーン、フロントポート、チップ・ツー・チップのアプリケーションにおいて、高速シリアル・リンクの到達範囲を拡張し、堅牢性を強化するために使用されます。

DS280BR820の均等化の直線性から、送信信号の特性が保持され、ホストとリンク・パートナーのASICとが、送信イコライザーの係数を自由にネゴシエーションできるようになります(100G-CR4/KR4)。このリンク・トレーニング・プロトコルへの透過性により、レイテンシへの影響を最小限に抑えながら、システム・レベルの相互運用性を向上できます。各チャネルは独立に動作するため、DS280BR820は個別のレーン・フォワード・エラー訂正(FEC)パススルーをサポートできます。

DS280BR820はパッケージの寸法が小さく、高速信号エスケープが最適化され、Retimerポートフォリオとピン互換なため、高密度のバックプレーン・アプリケーションに理想的です。単純化された均等化制御、低い消費電力、非常に低い付加的ジッタから、100G-SR4/LR4/CR4などのフロントポート・インターフェイスに適しています。8mm x 13mm と占有面積が小さいため、QSFP、SFP、CFP2、CFP4、CDFP など各種の標準フロントポート・コネクタに簡単に収まり、ヒートシンクの必要もありません。

ACカップリング・コンデンサ(RX側)が内蔵されているため、PCB上に外付けのコンデンサが必要ありません。DS280BR820は単一電源で、必要な外部コンポーネントも最小限です。これらの特長により、PCBの配線の複雑性と、部品表(BOM)コストを低減できます。

より到達範囲の長いアプリケーション用には、ピン互換のRetimerデバイスを利用可能です。

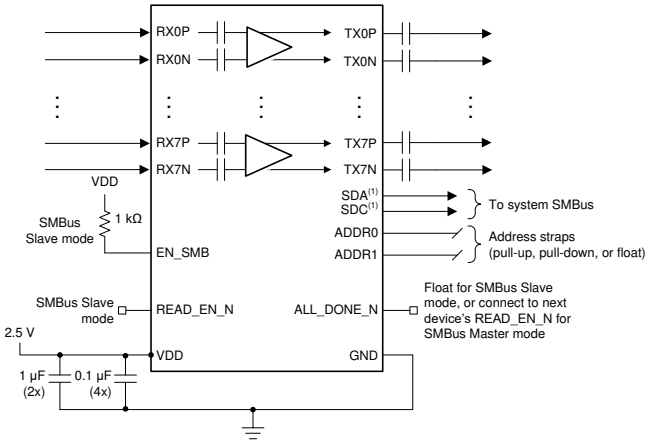
DS280BR820 は SMBus 経由、または外付けの EEPROM により構成可能です。単一のEEPROMを、最大16個のデバイスで共有できます。

製品情報 (1)

型番	パッケージ	本体サイズ(公称)
DS280BR820	nFBGA (135)	8.0mm×13.0mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



(1) SMBus signals need to be pulled up elsewhere in the system.

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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5 Pin Configuration and Functions

Top View

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
J	GND	GND	TX1N	GND	TX2N	GND	TX3N	GND	TX4N	GND	TX5N	GND	TX6N	GND	GND	J
H	TX0N	GND	TX1P	GND	TX2P	GND	TX3P	GND	TX4P	GND	TX5P	GND	TX6P	GND	TX7N	H
G	TX0P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TX7P	G
F	GND	GND	READ_EN_N	SDC	GND	VDD	GND	VDD	GND	VDD	GND	GND	INT_N (NC)	GND	GND	F
E	CAL_CLK_OUT	TEST 1	ADDR 1	SDA	GND	VDD	VDD	VDD	VDD	VDD	VDD	GND	EN_SMB	TEST 0	CAL_CLK_IN	E
D	GND	GND	ADDR 0	GND	GND	VDD	GND	VDD	GND	VDD	GND	GND	ALL_DONE_N	GND	GND	D
C	RX0P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RX7P	C
B	RX0N	GND	RX1P	GND	RX2P	GND	RX3P	GND	RX4P	GND	RX5P	GND	RX6P	GND	RX7N	B
A	GND	GND	RX1N	GND	RX2N	GND	RX3N	GND	RX4N	GND	RX5N	GND	RX6N	GND	GND	A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

GND — Ground pin
High-speed pin
VDD — Power pin
Control/Status pin
No connect on package
Test pin

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/O			
RX0N	B15	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX0P	C15	Input	
RX1N	A13	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX1P	B13	Input	
RX2N	A11	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX2P	B11	Input	
RX3N	A9	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX3P	B9	Input	
RX4N	A7	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX4P	B7	Input	
RX5N	A5	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX5P	B5	Input	
RX6N	A3	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX6P	B3	Input	
RX7N	B1	Input	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled with 220-nF capacitors assembled on the package substrate.
RX7P	C1	Input	
TX0N	H15	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX0P	G15	Output	
TX1N	J13	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX1P	H13	Output	

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TX2N	J11	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX2P	H11	Output	
TX3N	J9	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX3P	H9	Output	
TX4N	J7	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX4P	H7	Output	
TX5N	J5	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX5P	H5	Output	
TX6N	J3	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX6P	H3	Output	
TX7N	H1	Output	Inverting and non-inverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs.
TX7P	G1	Output	
CALIBRATION CLOCK PINS (FOR SUPPORTING UPGRADE PATH TO PIN-COMPATIBLE RETIMER DEVICE)			
CAL_CLK_IN	E1	Input	25-MHz (±100 PPM) 2.5-V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. ***A 25-MHz input clock is only required if there is a need to support a future upgrade to the pin-compatible Retimer device.*** If there is no need to support a future upgrade to a pin-compatible Retimer device, then a 25-MHz clock is not required. This input pin has a weak active pull-down and can be left floating if the CAL_CLK feature is not required.
CAL_CLK_OUT	E15	Output	2.5-V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.
SYSTEM MANAGEMENT BUS (SMBus) PINS			
ADDR0	D13	Input, 4-Level	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD
ADDR1	E13	Input, 4-Level	
ALL_DONE_N	D3	Output, LVCMOS	Indicates the completion of a valid EEPROM register load operation when in SMBus master mode (EN_SMB = Float): High = External EEPROM load failed or incomplete. Low = External EEPROM load successful and complete. When in SMBus slave mode (EN_SMB = 1 kΩ to VDD), this output will be high-Z until READ_EN_N is driven low, at which point ALL_DONE_N will be driven low. This behavior allows the reset signal connected to READ_EN_N of one device to propagate to the subsequent devices when ALL_DONE_N is connected to READ_EN_N in an SMBus slave mode application.
EN_SMB	E3	Input, 4-Level	4-level 2.5-V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED R: 10 kΩ to GND - RESERVED F: Float - SMBus master mode 1: 1 kΩ to VDD - SMBus slave mode
READ_EN_N	F13	Input, LVCMOS	Pin has weak pull-up. This pin is 3.3 V tolerant. SMBus master mode (EN_SMB = Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. SMBus slave mode (EN_SMB = 1 kΩ to VDD): When asserted low, this causes the device to be held in reset (SMBus state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus slave mode.
SDA	E12	I/O, 3.3-V LVCMOS, Open Drain	SMBus data input and open drain output. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SDC	F12	I/O, 3.3-V LVCMOS, Open Drain	SMBus clock input and open drain clock output. External 2-kΩ to 5-kΩ pull-up resistor is required. This pin is 3.3-V LVCMOS tolerant.
MISCELLANEOUS PINS			
INT_N	F3	No Connect	No connect on package. For applications using multiple repeaters and retimers, this pin should be connected to other devices' INT_N pins. This is only a recommendation for cases where there is a need to support a potential future upgrade to the pin-compatible retimer device, which uses this pin as an interrupt signal to a system controller.
TEST0	E2	Input, LVCMOS	Reserved test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5-V (max) output.
TEST1	E14	Input, LVCMOS	
POWER			
GND	A1, A2, A4, A6, A8, A10, A12, A14, A15, B2, B4, B6, B8, B10, B12, B14, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D4, D5, D7, D9, D11, D12, D14, D15, E4, E11, F1, F2, F4, F5, F7, F9, F11, F14, F15, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, H2, H4, H6, H8, H10, H12, H14, J1, J2, J4, J6, J8, J10, J12, J14, J15	Power	Ground reference. The GND pins on this device should be connected through a low-impedance path to the board GND plane.
VDD	D6, D8, D10, E5, E6, E7, E8, E9, E10, F6, F8, F10	Power	Power supply, VDD = 2.5 V ±5%. Use at least six de-coupling capacitors between the Repeater's VDD plane and GND as close to the Repeater as possible. For example, four 0.1-μF capacitors and two 1-μF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane. For more information, see *Power Supply Recommendations*.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). (1)

		MIN	MAX	UNIT
VDD_{ABSMAX}	Supply voltage (VDD)	–0.5	2.75	V
$VIO_{2.5V,ABSMAX}$	2.5 V I/O voltage (LVCMOS and CMOS)	–0.5	2.75	V
$VIO_{3.3V,ABSMAX}$	Open drain and 3.3 V-tolerance I/O voltage (SDA, SDC, READ_EN_N)	–0.5	4	V
$VIO_{HS,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN, TXnP, TXnN)	–0.5	2.75	V
TJ_{ABSMAX}	Junction temperature		150	°C
T_{stg}	Storage temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

			MIN	NOM	MAX	UNIT
VDD	Supply voltage, VDD to GND	DC plus AC power should not exceed these limits	2.375	2.5	2.625	V
N_{VDD}	Supply noise tolerance (1)	Supply noise, DC to <50 Hz, sinusoidal			250	mVpp
		Supply noise, 50 Hz to 10 MHz, sinusoidal			20	mVpp
		Supply noise, >10 MHz, sinusoidal			10	mVpp
$T_{RampVDD}$	VDD supply ramp time	From 0 V to 2.375 V	150			µs
T_J	Operating junction temperature		-40		110	C
T_A	Operating ambient temperature		-40		85	C
VDD_{SMBUS}	SMBus SDA and SDC Open Drain Termination Voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus clock (SDC) frequency in SMBus slave mode				400	kHz

(1) Sinusoidal noise is superimposed to supply voltage with negligible impact to device function or critical performance shown in the Electrical Table.

6.4 Thermal Information

THERMAL METRIC (1)		CONDITIONS / ASSUMPTIONS	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4-layer JEDEC board	45.2	°C/W
		10-layer 8-in x 6-in board	26.3	
		20-layer 8-in x 6-in board	24.8	
		30-layer 8-in x 6-in board	22.7	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4-layer JEDEC board	26.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4-layer JEDEC board	25.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4-layer JEDEC board	13.3	°C/W
		10-layer 8-in x 6-in board	13.0	
		20-layer 8-in x 6-in board	13.0	
		30-layer 8-in x 6-in board	13.0	
ψ_{JB}	Junction-to-board characterization parameter	4-layer JEDEC board	22.8	°C/W
		10-layer 8-in x 6-in board	21.4	
		20-layer 8-in x 6-in board	21.1	
		30-layer 8-in x 6-in board	20.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
$W_{channel}$	Power consumption per active channel	Channel enabled and in linear mode with maximum driver VOD (DRV_SEL_VOD = 3). Static power consumption not included.		82	97 (1)	mW
		Channel enabled and in linear mode with minimum driver VOD (DRV_SEL_VOD = 0). Static power consumption not included.		75	89 (1)	mW
$W_{channel\_FIR}$	Power consumption per active channel	Channel enabled and in FIR limiting mode with C0 = 31 and maximum driver VOD (DRV_SEL_VOD = 3). Static power consumption not included.		105	123 (1)	mW
		Channel enabled and in FIR limiting mode with C0 = 31 and minimum driver VOD (DRV_SEL_VOD = 0). Static power consumption not included.		97	115 (1)	mW
W_{static_total}	Idle (static) mode total device power consumption	Channels disabled and powered down (DRV_PD = 1, EQ_PD = 1).		110	132 (1)	mW
I_{total}	Active mode total device supply current consumption	All channels enabled and in linear mode with maximum driver VOD (DRV_SEL_VOD = 3).		307	347	mA
		All channels enabled and in linear mode with minimum driver VOD (DRV_SEL_VOD = 0).		283	322	mA

(1) Max values assume VDD = 2.5 V + 5%.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{total_FIR}	Active mode total device supply current consumption	All channels enabled and in FIR limiting mode with C0 = 31 and maximum driver VOD (DRV_SEL_VOD = 3).		380	426	mA
		All channels enabled and in FIR limiting mode with C0 = 31 and minimum driver VOD (DRV_SEL_VOD = 0).		355	401	mA
I_{static_total}	Idle (static) mode total device supply current consumption	All channels disabled and powered down (DRV_PD = 1, EQ_PD = 1).		44	50	mA
LVCMOS DC SPECIFICATIONS (CAL_CLK_IN, CAL_CLK_OUT, READ_EN_N, ALL_DONE_N, TEST[1:0])						
V_{IH}	High level input voltage		1.75		VDD	V
		READ_EN_N pin only	1.75		3.6	V
V_{IL}	Low level input voltage		GND		0.7	V
V_{OH}	High level output voltage	IOH = 4 mA	2			V
V_{OL}	Low level output voltage	IOL = –4 mA			0.4	V
I_{IH}	Input high leakage current	Vinput = VDD, TEST[1:0] pins			16	µA
		Vinput = VDD, CAL_CLK_IN pin			66	µA
		Vinput = VDD, READ_EN_N pin (2)			1	µA
I_{IL}	Input low leakage current	Vinput = 0 V, TEST[1:0] pins	–38			µA
		Vinput = 0 V, CAL_CLK_IN pin (3)	–1			µA
		Vinput = 0 V, READ_EN_N pin (2)	–55			µA
4-LEVEL LOGIC ELECTRICAL SPECIFICATIONS (APPLIES TO 4-LEVEL INPUT CONTROL PINS ADDR0, ADDR1, and EN_SMB)						
I_{IH}	Input high leakage current				105	µA
I_{IL}	Input low leakage current		–253			µA
V_{TH}	High level (1) input voltage			0.95 × VDD		V
	Float level input voltage			0.67 × VDD		V
	10 K to GND input voltage			0.33 × VDD		V
	Low level (0) input voltage			0.1		V
HIGH-SPEED DIFFERENTIAL INPUTS (RXnP, RXnN)						
BST	CTLE high-frequency boost	Measured with maximum CTLE setting and maximum BW setting (EQ_BST1 = 7, EQ_BST2 = 7, EQ_BW = 3). Boost is defined as the gain at 14 GHz relative to 20 MHz.		25.6		dB
		Measured with maximum CTLE setting and maximum BW setting (EQ_BST1 = 7, EQ_BST2 = 7, EQ_BW = 3). Boost is defined as the gain at 12.9 GHz relative to 20 MHz.		25.3		dB

(2) This pin has an internal weak pull-up.
(3) This pin has an internal weak pull-down.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BST	CTLE high-frequency boost	Measured with minimum CTLE setting and minimum BW setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_BW = 0, EQ_EN_BYPASS = 1). Boost is defined as the gain at 14 GHz relative to 20 MHz.		2.4		dB
		Measured with minimum CTLE setting and minimum BW setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_BW = 0, EQ_EN_BYPASS = 1). Boost is defined as the gain at 12.9 GHz relative to 20 MHz.		2.4		dB
BST_{delta}	CTLE high-frequency gain variation	Measured with maximum CTLE setting (EQ_BST1 = 7, EQ_BST2 = 7). Gain variation is defined as the total change in gain at 14 GHz due to temperature and voltage variation.		< 3		dB
		Measured with maximum CTLE setting (EQ_BST1 = 7, EQ_BST2 = 7). Gain variation is defined as the total change in gain at 12.9 GHz due to temperature and voltage variation.		< 3		dB
BST_{delta}	CTLE high-frequency gain variation	Measured with minimum CTLE setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_EN_BYPASS = 1). Gain variation is defined as the total change in gain at 14 GHz due to temperature and voltage variation.		< 2		dB
		Measured with minimum CTLE setting (EQ_BST1 = 0, EQ_BST2 = 0, EQ_EN_BYPASS = 1). Gain variation is defined as the total change in gain at 12.9 GHz due to temperature and voltage variation.		< 2		dB
RL_{SDD11}	Input differential return loss	50 MHz to 3.7 GHz		< -14		dB
		3.7 GHz to 10 GHz		< -12		dB
		10 GHz to 14.1 GHz		< -8		dB
		14.1 GHz to 20 GHz		< -6		dB
RL_{SDC11}	Input differential-to-common-mode return loss	100 MHz to 3.3 GHz		< -35		dB
		3.3 GHz to 12.9 GHz		< -26		dB
		12.9 GHz to 20 GHz		< -22		dB
RL_{SCC11}	Input common-mode return loss	100 MHz to 10 GHz		< -7		dB
		10 GHz to 20 GHz		< -8		dB
V_{SDAT}	AC signal detect assert (ON) differential voltage threshold level	Minimum input peak-to-peak amplitude level at device pins required to assert signal detect. 25.78125 Gbps with PRBS7 pattern and 20 dB loss channel.		196		mVpp
V_{SDDT}	AC signal detect de-assert (OFF) differential voltage threshold level	Maximum input peak-to-peak amplitude level at device pins which causes signal detect to de-assert. 25.78125 Gbps with PRBS7 pattern and 20 dB loss channel.		147		mVpp

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VID_{linear}	Input amplitude linear range. The maximum VID for which the repeater remains linear, defined as ≤1 dB compression of Vout/Vin.	Measured with the highest wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 3). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		850		mVpp
		Measured with a mid wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 0). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		900		mVpp
		Measured with a mid wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 3). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		1050		mVpp
		Measured with the lowest wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 0). Measured with minimal input channel and minimum EQ using a 1 GHz signal.		1250		mVpp
HIGH-SPEED DIFFERENTIAL OUTPUTS (TXnP, TXnN)						
$PRE_{DEM-MAX}$	Maximum pre-cursor de-emphasis in FIR limiting mode	Measured with an 16T pattern at 28.125 Gbps using C(0), Reg_0x0B[4:0], set to 0x0C, C(-1), Reg_0x0D[3:0], set to 0xF, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		-11		dB
$PST_{DEM-MAX}$	Maximum post-cursor de-emphasis in FIR limiting mode	Measured with an 16T pattern at 28.125 Gbps using C(0), Reg_0x0B[4:0], set to 0x0C, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0xF. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		-11		dB
T_{PRE}	Pre-cursor FIR tap delay in FIR limiting mode	Independent of data rate		28		ps
T_{PST}	Post-cursor FIR tap delay in FIR limiting mode	Independent of data rate		25		ps
$VOD_{LIM-MIN}$	Minimum differential output amplitude in FIR limiting mode	Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x0.		185		mVpp
		Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x3.		360		mVpp

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VOD_{LIM-MAX}$	Maximum differential output amplitude in FIR limiting mode	Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x0.		705		mVpp
		Measured with a 16T pattern at 25.78125 Gbps using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1. VOD, Reg_0x06[7:6], set to 0x3.		1260		mVpp
VOD_{idle}	Differential output amplitude, TX disabled or otherwise muted			< 10		mVpp
G_{DC}	Vout/Vin wide-band amplitude gain in linear mode	Measured with the highest wide-band gain setting (EQ_HIGH_GAIN = 1, DRV_SEL_VOD = 3) at 20 MHz.		4.5		dB
		Measured with the lowest wide-band gain setting (EQ_HIGH_GAIN = 0, DRV_SEL_VOD = 0) at 20 MHz.		–5		
$V_{cm-TX-AC}$	Common-mode AC output noise	Defined as (TXP + TXN)/2. Measured with a low-pass filter with 3-dB bandwidth at 33 GHz.		6		mV, RMS
$V_{cm-TX-DC}$	Common-mode DC output	Defined as (TXP + TXN)/2. Measured with a DC signal.	0.75	0.96	1.05	V
$RJ_{ADD-RMS}$	Additive random jitter	Measured single-endedly on a Keysight E5505A phase noise measurement solution with a 28-Gbps 1010 pattern, from 2 kHz to 20 MHz.		11		fs RMS
RL_{SDD22}	Output differential-to-differential return loss	50 MHz to 4.8 GHz		< –16		dB
		4.8 GHz to 10 GHz		< –15		
		10 GHz to 14.1 GHz		< –8		
		14.1 GHz to 20 GHz		< –8		
RL_{SCD22}	Output common-mode-to-differential return loss	50 MHz to 6.0 GHz		< –21		dB
		6.0 GHz to 12.9 GHz		< –22		
		12.9 GHz to 14.1 GHz		< –21		
		14.1 GHz to 20 GHz		< –20		
RL_{SCC22}	Output common-mode return loss	50 MHz to 3.3 GHz		< –13		dB
		3.3 GHz to 10.3 GHz		< –11		
		10.3 GHz to 20 GHz		< –9		
t_r, t_f	Transition time (20%-80%) in FIR limiting mode	Measured at 28.125 Gbps with 16T data pattern using C(0), Reg_0x0B[4:0], set to 0x00, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		19.9		ps
		Measured at 28.125 Gbps with 16T data pattern using C(0), Reg_0x0B[4:0], set to 0x1F, C(-1), Reg_0x0D[3:0], set to 0x0, and C(+1), Reg_0x0C[3:0], set to 0x0. TX drv_sel_fir, Reg_0x06[0], set to 0x1.		25.8		ps

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OTHER PARAMETERS						
t_D	Input-to-output latency (propagation delay) through a channel	Linear mode		100		ps
t_D	Input-to-output latency (propagation delay) through a channel	FIR limiting mode, Reg_0x06[0]=1		160		ps
t_{SK}	Channel-to-channel interpair skew	Latency difference between channels.		<14		ps
T_{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after REAN_EN_N has been asserted. Single device reading its configuration from an EEPROM with common channel configuration. This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.			4	ms
		Time to assert ALL_DONE_N after REAN_EN_N has been asserted. Single device reading its configuration from an EEPROM. Non-common channel configuration. This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.			7	
T_{POR}	Power-on reset assertion time	Internal power-on reset (PoR) stretch between stable power supply and de-assertion of internal PoR. The SMBus address is latched on the completion of the PoR stretch, and SMBus accesses are permitted once PoR completes.			60	ms

6.6 Electrical Characteristics – Serial Management Bus Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high level voltage	SDA and SDC	1.75		3.6	V
V_{IL}	Input low level voltage	SDA and SDC	GND		0.8	V
V_{OL}	Output low level voltage	SDA and SDC, I_{OL} = 1.25 mA	GND		0.4	V
C_{IN}	Input pin capacitance	SDA and SDC		15		pF
I_{IN}	Input current	SDA or SDC, VINPUT = VIN, VDD, GND	–18		18	µA

6.7 Timing Requirements – Serial Management Bus Interface

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECOMMENDED SMBus SWITCHING CHARACTERISTICS (SMBus SLAVE MODE)						
f_{SDC}	SDC clock frequency	EN_SMB = 1 k to VDD (Slave Mode)	10	100	400	kHz
T_{SDA-HD}	Data hold time			0.75		ns
T_{SDA-SU}	Data setup time			100		ns
T_{SDA-R}	SDA rise time, read operation	Pull-up resistor = 1 kΩ, Cb = 50 pF		150		ns
T_{SDA-F}	SDA fall time, read operation	Pull-up resistor = 1 kΩ, Cb = 50 pF		4.5		ns
SMBus SWITCHING CHARACTERISTICS (SMBus MASTER MODE)						
f_{SDC}	SDC clock frequency	EN_SMB = Float (Master Mode)	260	303	346	kHz
$T_{SDC-LOW}$	SDC low period		1.66	1.90	2.21	µs
$T_{SDC-HIGH}$	SDC high period		1.22	1.40	1.63	µs
$T_{HD-START}$	Hold time start operation			0.6		µs

Timing Requirements – Serial Management Bus Interface (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SU-START}$	Setup time start operation			0.6		µs
T_{SDA-HD}	Data hold time			0.9		µs
T_{SDA-SU}	Data setup time			0.1		µs
$T_{SU-STOP}$	Stop condition setup time			0.6		µs
T_{BUF}	Bus free time between Stop-Start			1.3		µs
T_{SDC-R}	SDC rise time	Pull-up resistor = 1 kΩ		300		ns
T_{SDC-F}	SDC fall time	Pull-up resistor = 1 kΩ		300		ns

6.8 Typical Characteristics

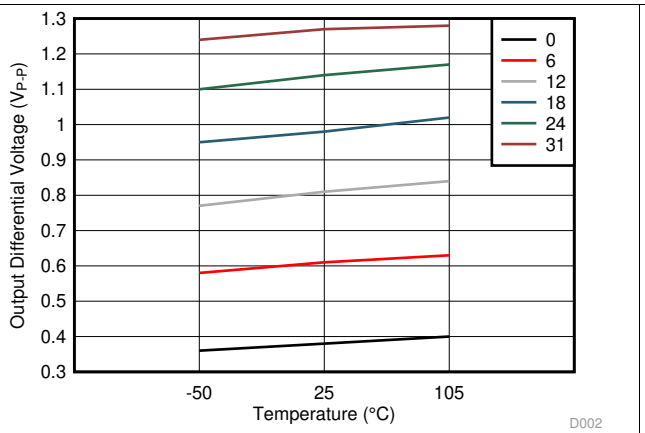

図 1. Limiting Mode: FIR VOD Variation Across Temperature

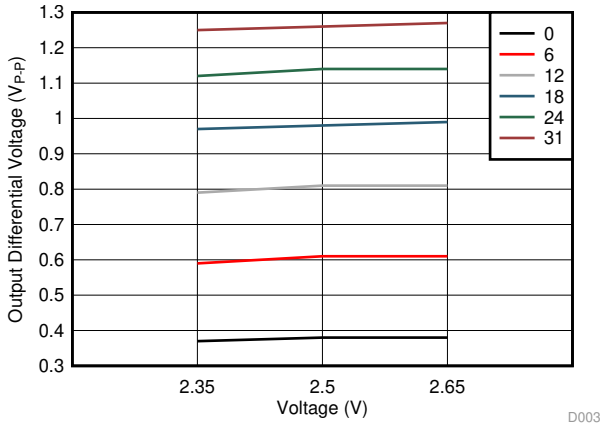

図 2. Limiting Mode: FIR VOD Variation Across VDD

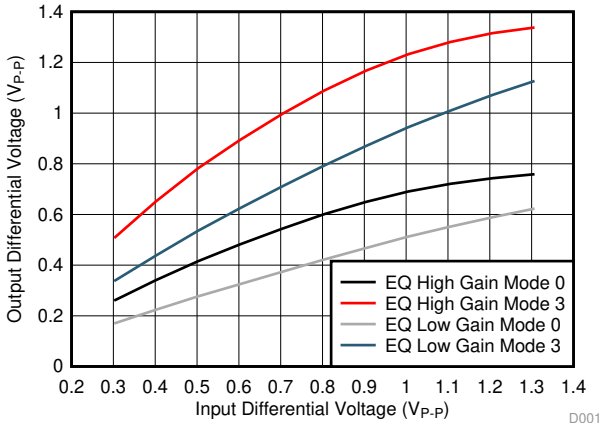

図 3. Typical Vin/Vout Linearity

7 Detailed Description

7.1 Overview

The DS280BR820 is an eight-channel multi-rate linear repeater with integrated signal conditioning. The eight channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE), an optional FIR filter and a linear output driver, which compensate for the presence of a dispersive transmission channel between the source transmitter and the final receiver.

All receive channels on the DS280BR820 are AC-coupled with physical AC coupling capacitors (220 nF ±20%) on the package substrate. This ensures common mode voltage compatibility with all link partner transmitters and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.

The DS280BR820 is configurable through a single SMBus port. The DS280BR820 can also act as an SMBus master to configure itself from an EEPROM.

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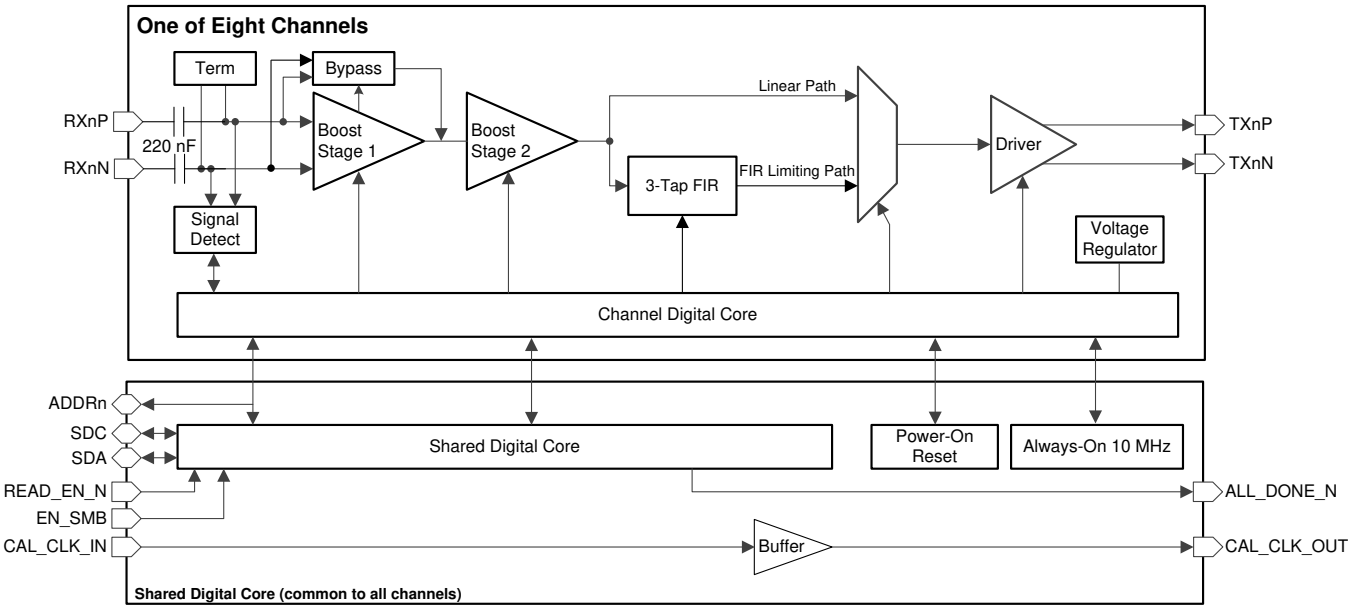
The DS280BR820 offers improved high-frequency boost and bandwidth compared to the DS280BR810. The DS280BR810 has series AC coupling capacitors on both the RX and TX pins, whereas the DS280BR820 has series AC coupling capacitors on the RX inputs only. The DS280BR820 and DS280BR810 are otherwise pin-to-pin compatible and share the same register programming interface.

The sections which follow describe the functionality of various circuits and features within the DS280BR820. For more information about how to program or operate these features, consult the DS280BR820 Programming Guide.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Data Path Operation

The DS280BR820 data path consists of several key blocks as shown in *Functional Block Diagram*. These key circuits are:

- *AC-Coupled Receiver Inputs*
- *Signal Detect*
- *2-Stage CTLE*
- *Driver DC Gain Control*
- *FIR Filter (Limiting Mode)*
- *Configurable SMBus Address*

7.3.2 AC-Coupled Receiver Inputs

The differential receiver for each DS280BR820 channel contains an integrated on-die 100-Ω differential termination as well as 220-nF ±20% series AC coupling capacitors embedded onto the package substrate.

7.3.3 Signal Detect

Each DS280BR820 high speed receiver has a signal detect circuit which monitors the energy level on the inputs. The signal detect circuit will enable the high-speed data path if a signal is detected, or power it off if no signal is detected. By default, this feature is enabled, but can be manually controlled though the SMBus channel registers. This can be useful if it is desired to manually force channels to be disabled. For information on how to manually operate the signal detect circuit refer to the DS280BR820 Programming Guide.

7.3.4 2-Stage CTLE

The continuous-time linear equalizer (CTLE) in the DS280BR820 consists of two stages which are configurable via the SMBus channel registers. This CTLE is designed to be highly linear to allow the DS280BR820 to preserve the transmitter's pre-cursor and post cursor signal characteristics. This highly linear behavior enables the DS280BR820 to be used in applications that use protocols such as link training, where it is important to recover and pass through incremental changes in transmit equalization.

Each stage in the CTLE has 3-bit boost control. The first CTLE stage provides a coarse adjustment of the total boost. Larger settings correspond to higher total boost. The first stage can be bypassed entirely to achieve the lowest possible total boost. The second CTLE stage acts as a fine adjustment on the total boost and impacts the shape of the boost curve accordingly. Larger settings correspond to higher total boost. The bandwidth of the CTLE can be adjusted using a 2-bit bandwidth control. Larger settings correspond to higher total bandwidth. For information on how to program the CTLE refer to the DS280BR820 Programming Guide.

In addition to high-frequency boost, the CTLE can apply wide-band amplitude gain. There are two settings (high-gain and low-gain) which work together with the driver DC gain control to affect the total input-to-output wide-band amplitude gain.

7.3.5 Driver DC Gain Control

In addition to the high-frequency boost provided by the CTLE, the DS280BR820 is also able to provide additional DC or low-frequency gain. The effective DC gain is controlled by a 3-bit field, allowing for eight levels of DC attenuation or DC gain. For information on how to configure the DC gain refer to the DS280BR820 Programming Guide.

7.3.6 FIR Filter (Limiting Mode)

The DS280BR820 has an optional limiting mode with a fixed-delay 3-tap finite impulse response (FIR) filter to provide transmit equalization. This FIR can be configured to apply pre-cursor and post-cursor boost to the high speed signal. The FIR filter also allows for main cursor amplitude control. The tap polarities in the FIR filter are fixed to allow for pre-cursor or post-cursor boost to be applied to the signal.

Feature Description (continued)

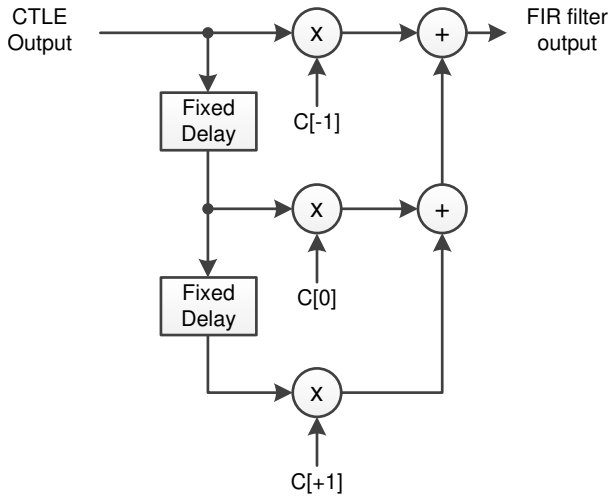


図 4. 3-Tap FIR Filter Block Diagram

Linear mode is recommended for the majority of applications, especially those which require Link Training. Common protocols such as 100 GbE and 40 GbE CR4/KR4, 50 GbE and 25 GbE CR, 10 GbE KR, InfiniBand EDR, and others require Link Training. Linear mode is required for Link Training so that the ASIC transmitter pre-cursor and post-cursor coefficients can propagate through the DS280BR820 in a transparent fashion. For applications which do not utilize Link Training, limiting mode may be used to provide output pre-cursor and post-cursor equalization for the purpose of improving the far-end eye opening. If the downstream receiver SerDes uses a decision feedback equalizer (DFE) to equalize the signal, the linear mode may be preferable to the limiting mode. DFE circuits often perform best when operating on a linear signal.

7.3.7 Configurable SMBus Address

The DS280BR820's SMBus slave address is strapped at power up using the ADDR[1:0] pins. The pin state is read on power up, after the internal power-on reset completes. The ADDR[1:0] pins are four-level LVCMOS IOs, which provide for 16 unique SMBus addresses. 表 1 lists the DS280BR820 SMBus slave address options.

表 1. SMBus Address Map

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	REQUIRED ADDRESS PIN STRAP VALUE	
		ADDR1	ADDR0
0x18	0x30	0	0
0x19	0x32	0	R
0x1A	0x34	0	F
0x1B	0x36	0	1
0x1C	0x38	R	0
0x1D	0x3A	R	R
0x1E	0x3C	R	F
0x1F	0x3E	R	1
0x20	0x40	F	0
0x21	0x42	F	R
0x22	0x44	F	F
0x23	0x46	F	1
0x24	0x48	1	0
0x25	0x4A	1	R
0x26	0x4C	1	F
0x27	0x4E	1	1

7.4 Device Functional Modes

7.4.1 SMBus Slave Mode Configuration

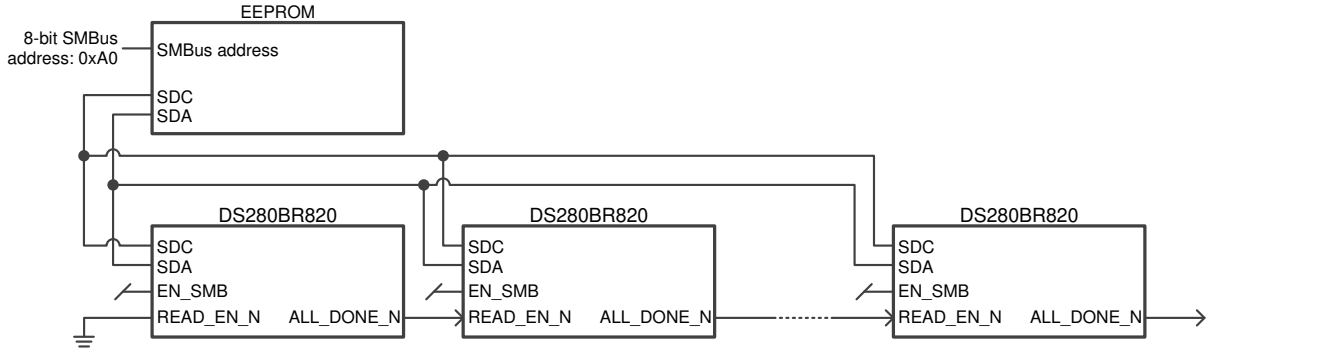
To configure the DS280BR820 for SMBus slave mode connect the EN_SMB pin to VDD with a 1 kΩ resistor. When the DS280BR820 is configured for SMBus slave mode operation the READ_EN_N becomes an active-low reset pin, resetting register values when driven to LOW, or V_{IL}. Additionally, when the DS280BR820 is configured for SMBus slave mode the ALL_DONE_N output pin is high-Z; except for when READ_EN_N is driven LOW which causes ALL_DONE_N to also be driven LOW. Refer to *Register Maps* for additional register information.

7.4.2 SMBus Master Mode Configuration (EEPROM Self Load)

To configure the DS280BR820 for SMBus master mode, leave the EN_SMB pin floating (no connect). If the DS280BR820 is configured for SMBus master mode, it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. Once the READ_EN_N pin is driven LOW, the DS280BR820 becomes an SMBus master and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS280BR820 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW and then change from an SMBus master to an SMBus slave. Not all bits in the register map can be configured through an EEPROM load. Refer to the Programming Guide for more information.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- Maximum EEPROM size is 8 kb (1024 x 8-bit)
- Set EN_SMB = FLOAT, configure for SMBus master mode
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 2.5-V or 3.3-V supply.
- Configure the ADDR[1:0] inputs to select the SMBus slave address for the DS280BR820. Once the DS280BR820 completes its EEPROM load the device becomes a slave on the control bus.



Tie first device's READ_EN_N pin low to automatically initiate EEPROM read at power up, or control this pin from a device to initiate EEPROM read manually.

Leave final device's ALL_DONE_N pin floating or connect to a control chip to monitor completion of final EEPROM read.

図 5. Example Daisy Chain for Multiple Device Single EEPROM Configuration

When tying multiple DS280BR820 devices to the SDA and SDC bus, use these guidelines to configure the devices for SMBus master mode:

- Use SMBus ADDR[1:0] address bits so that each device can load its configuration from the EEPROM. The example below is for four devices. The first device in the sequence conventionally uses the 8-bit slave write address 0x30, while subsequent devices follow the address order listed below.
  - DS280BR820 instance 1 (U1): ADDR[1:0] = {0, 0} = 0x30
  - DS280BR820 instance 2 (U2): ADDR[1:0] = {0, R} = 0x32
  - DS280BR820 instance 3 (U3): ADDR[1:0] = {0, F} = 0x34
  - DS280BR820 instance 4 (U4): ADDR[1:0] = {0, 1} = 0x36
- Use a pull-up resistor on SDA and SDC; resistor value = 2 kΩ to 5 kΩ is adequate.
- Float (no connect) the EN_SMB pin (E3) on all DS280BR820 devices to configure them for SMBus master mode. The EN_SMB pin should not be dynamically changed between the high and float states.

Device Functional Modes (continued)

- Daisy-chain READ_EN_N (pin F13) and ALL_DONE_N (pin D3) from one device to the next device in the following sequence so that they do not compete for master control of the EEPROM at the same time.
  1. Tie READ_EN_N of the first device in the chain (U1) to GND to trigger EEPROM read immediately after the DS280BR820 power-on reset (PoR) completes. Alternatively, drive the READ_EN_N pin from a control device (micro-controller or FPGA) to trigger the EEPROM read at a specific time.
  2. Tie ALL_DONE_N of U1 to READ_EN_N of U2
  3. Tie ALL_DONE_N of U2 to READ_EN_N of U3
  4. Tie ALL_DONE_N of U3 to READ_EN_N of U4
  5. Optional: Tie ALL_DONE_N output of U4 to a micro-controller or an LED to show the devices have been loaded successfully.

Once the ALL_DONE_N status pin of the last device is flagged to indicate that all devices sharing the SMBus line have been successfully programmed, control of the SMBus line is released by the DS280BR820. The device then reverts back to SMBus slave mode. At this point, an external MCU can perform any additional Read or Write operations to the DS280BR820.

Refer to the Programming Guide for additional information concerning SMBus master mode.

7.5 Programming

The DS280BR820 can be programmed in two ways. The DS280BR820 can be configured as an SMBus slave (EN_SMB = HIGH) or the device can temporarily act as an SMBus master and load its configuration settings from an external EEPROM (EN_SMB = FLOAT). Refer to *SMBus Slave Mode Configuration* and *SMBus Master Mode Configuration (EEPROM Self Load)* for details.

7.5.1 Transfer of Data with the SMBus Interface

The System Management Bus (SMBus) is a two-wire serial interface through which a master can communicate with various system components. Slave devices are identified by a unique device address. The two-wire serial interface consists of SDC and SDA signals. SDC is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The DS280BR820 SMBus SDC and SDA signals are open drain and require external pull-up resistors.

Start and Stop Conditions:

The master generates Start and Stop conditions at the beginning and end of each transaction:

- Start: HIGH to LOW transition (falling edge) of SDA while SDC is HIGH.
- Stop: LOW to HIGH transition (rising edge) of SDA while SDC is HIGH.

The master generates 9 clock pulses for each byte transfer. The 9th clock pulse constitutes the acknowledge (ACK) cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is when the device pulls SDA LOW, while a NACK (no acknowledge) is recorded if the line remains HIGH.

Writing data from a master to a slave consists of three parts:

- The master begins with a start condition followed by the slave device address with the R/W bit cleared.
- The master sends the 8-bit register address that will be written.
- The master sends the data byte to write for the selected register address. The register address pointer will then increment, so the master can send the data byte for the subsequent register without re-addressing the device, if desired. The final data byte to write should be followed by a stop condition.

SMBus read operations consist of four parts:

- The master initiates the read cycle with start condition followed by slave device address with the R/W bit cleared.
- The master sends the 8-bit register address that will be read.
- After acknowledgment from the slave, the master initiates a re-start condition.
- The slave device address is resent followed with R/W bit set.
- After acknowledgment from the slave, the data is read back from the slave to the master. The last ACK is HIGH if there are no more bytes to read.

7.6 Register Maps

Many of the registers in the DS280BR820 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS280BR820 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. This sequence is commonly referred to as Read-Modify-Write. If the entire register is changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first.

Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.

Register bits can have the following interface constraints:

- R - Read only
- RW - Read/Write
- RWSC - Read/Write, Self-Clearing

7.6.1 Register Types: Global, Shared, and Channel

The DS280BR820 has 3 types of registers:

1. Global Registers - These registers can be accessed at any time and are used to select between individual channel registers and shared registers, or to read back the TI ID and version information.
2. Shared Registers - These registers are used for device-level configuration, status read back or control. Set register 0xFF[0] = 0 and configure 0xFF[5:4] to access the shared registers.
3. Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other. Set register 0xFF[0] = 1 and configure register 0xFC to access the desired channel register set.

Refer to the Programming Guide for additional information on register configuration.

7.6.2 Global Registers: Channel Selection and ID Information

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS280BR820 global registers are located at address 0xEF - 0xFF.

表 2. Global Register Map

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0xEF		**0x0C**			General	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	1	R	N	DEVICE_ID_QUAD_CNT[3]	TI device ID (quad count). Contains 0x0C.
	2	1	R	N	DEVICE_ID_QUAD_CNT[2]	
	1	0	R	N	DEVICE_ID_QUAD_CNT[1]	
	0	0	R	N	DEVICE_ID_QUAD_CNT[0]	

Register Maps (continued)

表 2. Global Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0xF0		**0x00**			**Version Revision**	
	7	0	R	N	TYPE	TI version ID. Contains 0x00.
	6	0	R	N	VERSION[6]	
	5	0	R	N	VERSION[5]	
	4	0	R	N	VERSION[4]	
	3	0	R	N	VERSION[3]	
	2	0	R	N	VERSION[2]	
	1	0	R	N	VERSION[1]	
	0	0	R	N	VERSION[0]	
0xF1		**0x40**			**Channel Control**	
	7	0	R	N	DEVICE_ID[7]	TI device ID. Contains 0x40.
	6	1	R	N	DEVICE_ID[6]	
	5	0	R	N	DEVICE_ID[5]	
	4	0	R	N	DEVICE_ID[4]	
	3	0	R	N	DEVICE_ID[3]	
	2	0	R	N	DEVICE_ID[2]	
	1	0	R	N	DEVICE_ID[1]	
	0	0	R	N	DEVICE_ID[0]	
0xF3		**0x00**			**Channel Control**	
	7	0	R	N	CHAN_VERSION[3]	TI digital channel version ID. Contains 0x00.
	6	0	R	N	CHAN_VERSION[2]	
	5	0	R	N	CHAN_VERSION[1]	
	4	0	R	N	CHAN_VERSION[0]	
	3	0	R	N	SHARE_VERSION[3]	TI digital share version ID. Contains 0x00.
	2	0	R	N	SHARE_VERSION[2]	
	1	0	R	N	SHARE_VERSION[1]	
	0	0	R	N	SHARE_VERSION[0]	
0xFC		**0x00**			**General**	
	7	0	RW	N	EN_CH7	Select channel 7
	6	0	RW	N	EN_CH6	Select channel 6
	5	0	RW	N	EN_CH5	Select channel 5
	4	0	RW	N	EN_CH4	Select channel 4
	3	0	RW	N	EN_CH3	Select channel 3
	2	0	RW	N	EN_CH2	Select channel 2
	1	0	RW	N	EN_CH1	Select channel 1
	0	0	RW	N	EN_CH0	Select channel 0
0xFD		**0x00**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED

Register Maps (continued)

表 2. Global Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0xFE		**0x03**			**Vendor ID**	
	7	0	R	N	VENDOR_ID[7]	TI vendor ID. Contains 0x03.
	6	0	R	N	VENDOR_ID[6]	
	5	0	R	N	VENDOR_ID[5]	
	4	0	R	N	VENDOR_ID[4]	
	3	0	R	N	VENDOR_ID[3]	
	2	0	R	N	VENDOR_ID[2]	
	1	1	R	N	VENDOR_ID[1]	
	0	1	R	N	VENDOR_ID[0]	
0xFF		**0x10**			**Channel Control**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	EN_SHARE_Q1	Select shared registers for Quad 1 (Channels 4-7).
	4	1	RW	N	EN_SHARE_Q0	Select shared registers for Quad 0 (Channels 0-3).
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	WRITE_ALL_CH	Allows customer to write to all channels as if they are the same, but only allows to read back from the channel specified in 0xFC and 0xFD. Note: EN_CH_SMB must be = 1 or else this function is invalid.
	0	0	RW	N	EN_CH_SMB	1: Enables SMBus access to the channels specified in register 0xFC. 0: The shared registers are selected, see 0xFF[5:4].

7.6.3 Shared Registers

表 3. Shared Register Map

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0x00		**0x0C**			**General**	
	7	0	R	N	I²C_ADDR[3]	I²C strap observation. The device 7-bit slave address is 0x18 + I²C_ADDR[3:0].
	6	0	R	N	I²C_ADDR[2]	
	5	0	R	N	I²C_ADDR[1]	
	4	0	R	N	I²C_ADDR[0]	
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
0x01		**0x00**			**Version Revision**	
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
0x02		**0x00**			**Channel Control**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x03		**0x00**			**Channel Control**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x04		**0x01**			**General**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RWSC	N	RST_I²C_REGS	1: Reset shared registers, bit is self-clearing. 0: Normal operation
	5	0	RWSC	N	RST_I²C_MAS	1: Self-clearing reset for I²C master. 0: Normal operation
	4	0	RW	N	FRC_EEPRM_RD	1: Override EN_SMB and input chain status to force EEPROM Configuration. 0: Normal operation
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	REGS_CLOCK_EN	RESERVED
	1	0	RW	N	I²C_MAS_CLK_EN	RESERVED
	0	1	RW	N	I²CSLV_CLK_EN	RESERVED

表 3. Shared Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0x05		**0x00**			**General**	
	7	0	RW	N	DISAB_EEPRM_CFG	1: Disable Master Mode EEPROM Configuration (If not started, not effective midway or after configuration). 0: Normal operation
	6	0	RW	N	CRC_EN	RESERVED
	5	0	RW	N	ML_TEST _CONTROL	RESERVED
	4	0	R	N	EEPROM_READING _DONE	Sets 1 when EEPROM reading is done.
	3	0	R	N	RESERVED	RESERVED
	2	0	R	Y	CAL_CLK_INV_DIS	1: Disable the inversion of CAL_CLK_OUT. 0: Normal operation, CAL_CLK_OUT is inverted with respect to CAL_CLK_IN.
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	TEST0_AS_CAL _CLK	RESERVED
0x06		**0x00**			**General**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x07		**0x00**			**General**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	R	N	CAL_CLK_DET	1: Indicates that CAL_CLK has been detected. 0: Indicates that CAL_CLK has not been detected.
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	MR_CAL_CLK_DET _DIS	1: Disable CAL_CLK detect. 0: Enable CAL_CLK detect.
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	Y	DIS_CAL_CLK_OUT	1: Disable CAL_CLK_OUT, output is high-Z. 0: Enable CAL_CLK_OUT.
0x08		**0x00**			**General**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x09		**0x00**			**General**	
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED

表 3. Shared Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
0x0A		**0x00**			**General**	
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
0x0B		**0x00**				
	7	0	R	N	EECFG_CMPLT	11: Not valid 10: EEPROM load completed successfully.
	6	0	R	N	EECFG_FAIL	01: EEPROM load failed after 64 attempts. 00: EEPROM load in progress.
	5	0	R	N	EECFG_ATMPT[5]	Indicates number of attempts made to load EEPROM image.
	4	0	R	N	EECFG_ATMPT[4]	
	3	0	R	N	EECFG_ATMPT[3]	
	2	0	R	N	EECFG_ATMPT[2]	
	1	0	R	N	EECFG_ATMPT[1]	
	0	0	R	N	EECFG_ATMPT[0]	
0x0C		**0x91**				
	7	1	RW	N	I^2C_FAST	1: EEPROM load uses Fast I^2C Mode (400 kHz). 0: EEPROM load uses Standard I^2C Mode (100 kHz).
	6	0	RW	N	I^2C_SDA_HOLD[2]	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SDC input. Units are 100 ns.
	5	0	RW	N	I^2C_ SDA_HOLD[1]	
	4	1	RW	N	I^2C_ SDA_HOLD[0]	
	3	0	RW	N	I^2C_FLTR_DEPTH[3]	I^2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SDC and SDA inputs that will be rejected. Units are 100 ns.
	2	0	RW	N	I^2C_FLTR_DEPTH[2]	
	1	0	RW	N	I^2C_FLTR_DEPTH[1]	
	0	1	RW	N	I^2C_FLTR_DEPTH[0]	

7.6.4 Channel Registers

表 4. Channel Register Map

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
0x00		**0x00**			**General**	
	7	0	RW	N	CLK_CORE_DISAB	1: Disables 10 M core clock. This is the main clock domain for all the state machines. 0: Normal operation
	6	0	RW	N	CLK_REGS_EN	1: Force enable the clock to the registers. Normally, the register clock is enabled automatically on a needed basis. 0: Normal operation
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	CLK_REF_DISAB	1: Disables the 25 MHz CAL_CLK domain. 0: Normal operation
	3	0	RW	N	RST_CORE	1: Reset the 10 M core clock domain. This is the main clock domain for all the state machines. 0: Normal operation
	2	0	RWSC	N	RST_REGS	1: Reset channel registers to power-up defaults. 0: Normal operation
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RST_CAL_CLK	1: Resets the 25 MHz reference clock domain. 0: Normal operation
0x01		**0x00**			**SIG_DET**	
	7	0	R	N	SIGDET	Signal detect status. 1: Signal detected at RX inputs. 0: No signal detected at RX inputs.
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	R	N	RESERVED	RESERVED
	2	0	R	N	RESERVED	RESERVED
	1	0	R	N	RESERVED	RESERVED
	0	0	R	N	RESERVED	RESERVED
0x02		**0x00**				
	7	0	R	N	RESERVED	RESERVED
	6	0	R	N	RESERVED	RESERVED
	5	0	R	N	RESERVED	RESERVED
	4	0	R	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x03		**0x80**			**CTLE_BOOST**	
	7	1	RW	Y	EQ_BW[1]	EQ stage one buffer current (strength) control. Impacts EQ bandwidth. 2'b11 yields highest bandwidth, 2'b00 yields lowest bandwidth. Refer to the Programming Guide for more information.
	6	0	RW	Y	EQ_BW[0]	
	5	0	RW	Y	EQ_BST2[2]	EQ boost stage 2 controls. Directly goes to analog. No override bit is needed. Refer to the Programming Guide for more information.
	4	0	RW	Y	EQ_BST2[1]	
	3	0	RW	Y	EQ_BST2[0]	
	2	0	RW	Y	EQ_BST1[2]	EQ boost stage 1 controls. Directly goes to analog. No override bit is needed. Refer to the Programming Guide for more information.
	1	0	RW	Y	EQ_BST1[1]	
	0	0	RW	Y	EQ_BST1[0]	
0x04		**0x90**				
	7	1	RW	N	RESERVED	RESERVED
	6	0	RW	N	EQ_PD_SD	1: Power down signal detect 0: Normal operation

表 4. Channel Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	5	0	RW	Y	EQ_HIGH_GAIN	1: Enable EQ high gain 0: Enable EQ low gain
	4	1	RW	Y	EQ_EN_DC_OFF	RESERVED
	3	0	RW	Y	EQ_PD_EQ	1: Power down EQ 0: Enable EQ
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	Y	BG_SEL_IPP100[2]	CTLE bias programming. BG_SEL_IPP100[1:0] is in Reg_0x0F[5:4].
	0	0	RW	Y	EQ_EN_BYPASS	1: Enable EQ boost stage 1 (BST1) bypass 0: Normal operation, signal travels through boost stage 1 (BST1)
0x05		**0x04**			SIG_DET_CONFIG	
	7	0	RW	Y	EQ_SD_PRESET	1: Force signal detect result to 1 0: Normal operation This bit should not be set if 0x05[6] is also set.
	6	0	RW	Y	EQ_SD_RESET	1: Force signal detect result to 0 0: Normal operation This bit should not be set if 0x05[7] is also set.
	5	0	RW	Y	EQ_REFA_SEL[1]	Signal detect assert thresholds. Refer to the Programming Guide for more information.
	4	0	RW	Y	EQ_REFA_SEL[0]	
	3	0	RW	Y	EQ_REFD_SEL[1]	Signal detect de-assert thresholds. Refer to the Programming Guide for more information.
	2	1	RW	Y	EQ_REFD_SEL[0]	
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x06		**0xC0**				
	7	1	RW	Y	DRV_SEL_VOD[1]	Driver VOD adjust (DC gain), applicable to both linear and FIR limiting mode. Refer to the Programming Guide for more information.
	6	1	RW	Y	DRV_SEL_VOD[0]	
	5	0	RW	Y	DRV_EQ_PD_OV	1: Driver and equalizer power down manually with Reg_0x06[3] and Reg_0x04[3], respectively. 0: Driver and equalizer are powered down or up by default when LOS=1/0.
	4	0	RW	Y	DRV_SEL_MUTE_OV	Driver mute override: 1: Use register 0x06[1] for mute control. 0: Normal operation. Mute is automatically controlled by signal detect.
	3	0	RW	Y	DRV_PD	1: Power down the driver. 0: Normal operation, driver power on or off is controlled by signal detect.
	2	0	RW	Y	DRV_PD_CM_LOOP	1: Disable the driver's common mode loop control circuit. 0: Normal operation, common mode loop enabled.
	1	0	RW	Y	DRV_SEL_MUTE	1: Mute driver if override bit is enabled. 0: Normal operation
	0	0	RW	Y	DRV_SEL_FIR	Linear versus Limiting Mode select. Refer to the Programming Guide for more information. 1: Enable Limiting FIR mode. 0: Enable Linear mode (disable limiting FIR).
0x07		**0x20**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	1	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x08		**0x54**				
	7	0	RW	Y	RESERVED	RESERVED

表 4. Channel Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	Y	RESERVED	RESERVED
	4	1	RW	Y	RESERVED	RESERVED
	3	0	RW	Y	BG_SEL_IPTAT25	1: Increases the current to the CTLE by 5%. 0: Default
	2	1	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x09		**0x00**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x0A		**0x30**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	1	RW	Y	SD_REF_HIGH	Signal detect threshold controls: 11: Normal operation 10: Signal detect assert or de-assert thresholds reduced. 01: Signal detect assert or de-assert thresholds reduced. 00: Signal detect assert or de-assert thresholds reduced.
	4	1	RW	Y	SD_GAIN	
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x0B		**0x1A**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	1	RW	Y	FIR_MAIN[4]	FIR Limiting mode main-cursor control. Refer to the Programming Guide for more information.
	3	1	RW	Y	FIR_MAIN[3]	
	2	0	RW	Y	FIR_MAIN[2]	
	1	1	RW	Y	FIR_MAIN[1]	
	0	0	RW	Y	FIR_MAIN[0]	
0x0C		**0x40**				
	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	Y	FIR_PST[3]	FIR Limiting mode post-cursor control. There is no sign bit for the post-cursor. The post-cursor always provides a high-pass filter effect. Refer to the Programming Guide for more information.
	2	0	RW	Y	FIR_PST[2]	
	1	0	RW	Y	FIR_PST[1]	
	0	0	RW	Y	FIR_PST[0]	
0x0D		**0x40**				
	7	0	RW	N	RESERVED	RESERVED
	6	1	RW	Y	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED

表 4. Channel Register Map (continued)

Addr [HEX]	Bit	Default [HEX]	Mode	EEPROM	Field	Description
	3	0	RW	Y	FIR_PRE[3]	FIR Limiting mode pre-cursor control. There is no sign bit for the pre-cursor. The pre-cursor always provides a high-pass filter effect. Refer to the Programming Guide for more information.
	2	0	RW	Y	FIR_PRE[2]	
	1	0	RW	Y	FIR_PRE[1]	
	0	0	RW	Y	FIR_PRE[0]	
0x0E		**0x00**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	N	RESERVED	RESERVED
	4	0	RW	N	RESERVED	RESERVED
	3	0	RW	N	RESERVED	RESERVED
	2	0	RW	N	RESERVED	RESERVED
	1	0	RW	N	RESERVED	RESERVED
	0	0	RW	N	RESERVED	RESERVED
0x0F		**0x00**				
	7	0	RW	N	RESERVED	RESERVED
	6	0	RW	N	RESERVED	RESERVED
	5	0	RW	Y	BG_SEL_IPP100[1]	CTLE bias programming. BG_SEL_IPP100[2] is in Reg_0x04[1]. 000: 0% additional current (Default) 001: 5% additional current 010: 10% additional current 011: 15% additional current 100: 20% additional current 101: 25% additional current 110: 30% additional current 111: 35% additional current
	4	0	RW	Y	BG_SEL_IPP100[0]	
	3	0	RW	Y	BG_SEL_IPH200_v1[1]	Program pre-driver bias current: 00: 0% additional current (Default) 01: 12.5% additional current 10: 25% additional current 11: 37.5% additional current
	2	0	RW	Y	BG_SEL_IPH200_v1[0]	
	1	0	RW	Y	BG_SEL_IPH200_v0[1]	Program driver bias current: 00: 0% additional current (Default) 01: 12.5% additional current 10: 25% additional current 11: 37.5% additional current
	0	0	RW	Y	BG_SEL_IPH200_v0[0]	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS280BR820 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS280BR820 is typically used in three main application scenarios:

1. Backplane and mid-plane reach extension
2. Front-port eye opening for copper and optical applications

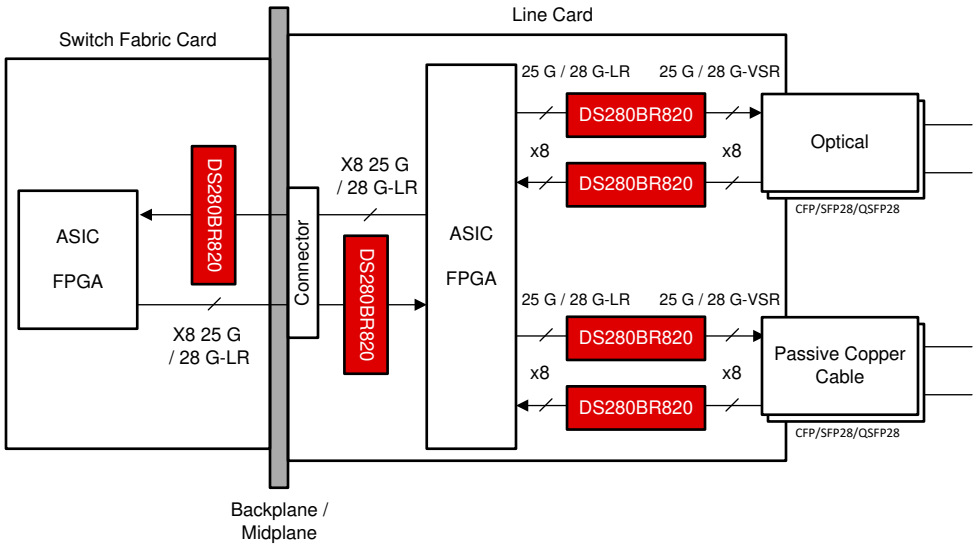


図 6. Typical Application Diagram

注

TI recommends to AC couple the DS280BR820's high-speed outputs. In some cases, ASIC or FPGA SerDes receivers support DC coupling, and it may be desirable to DC couple the DS280BR820 output with the ASIC/FPGA RX input to reduce the PCB area which would normally be consumed by AC coupling capacitors. To DC couple the DS280BR820 output with an ASIC RX input, the ASIC RX must support DC coupling and it must support an input common mode voltage of 1.05 V. To determine if the ASIC RX supports DC coupling, here are some items to consider based on 図 7:

1. The ASIC RX must be AC coupled on-chip.
2. The ASIC RX should not force a DC bias on the RX pins.
3. System designers should ensure that when the PCB powers on, the power supply rails are appropriately sequenced to prevent the DS280BR820's output common mode voltage from forward-biasing the ESD structure of the ASIC or violating the absolute maximum input voltage specifications of the ASIC.

Typical Applications (continued)

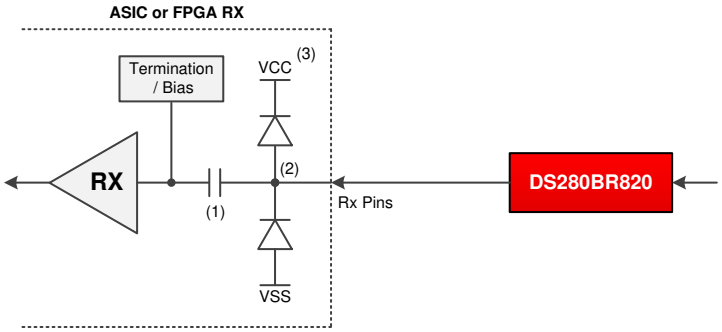


図 7. Considerations for DC Coupling to ASIC RX

8.2.1 Backplane and Mid-Plane Reach Extension

The DS280BR820 has strong equalization capabilities that allow it to equalize insertion loss and extend the reach of backplane channels by 17-22 dB beyond the normal capabilities of the ASICs operating over the channel. The DS280BR820 is designed to apply gain in a linear fashion. In most cases, the DS280BR820 should be placed with the higher loss channel segment at the input and the lower loss channel segment at the output; however, since the DS280BR820 operates in a linear fashion, it can also be used in applications where the lower loss channel segment is at the input and the higher loss channel segment is at the output. Refer to 図 8.

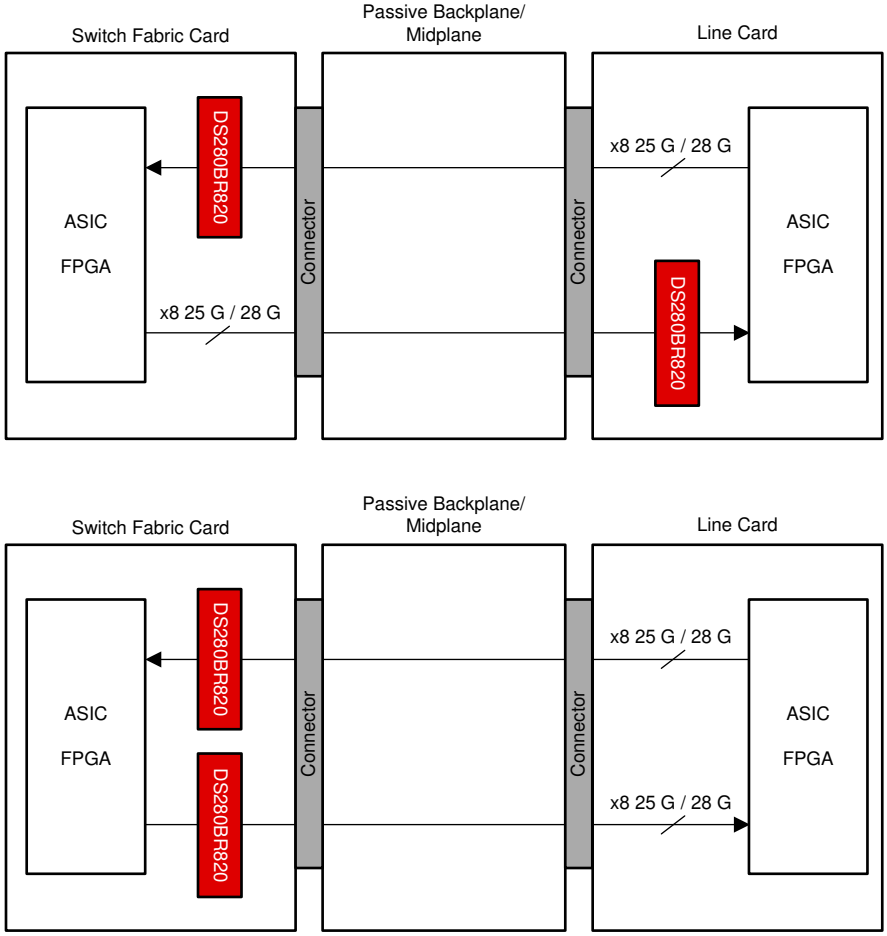
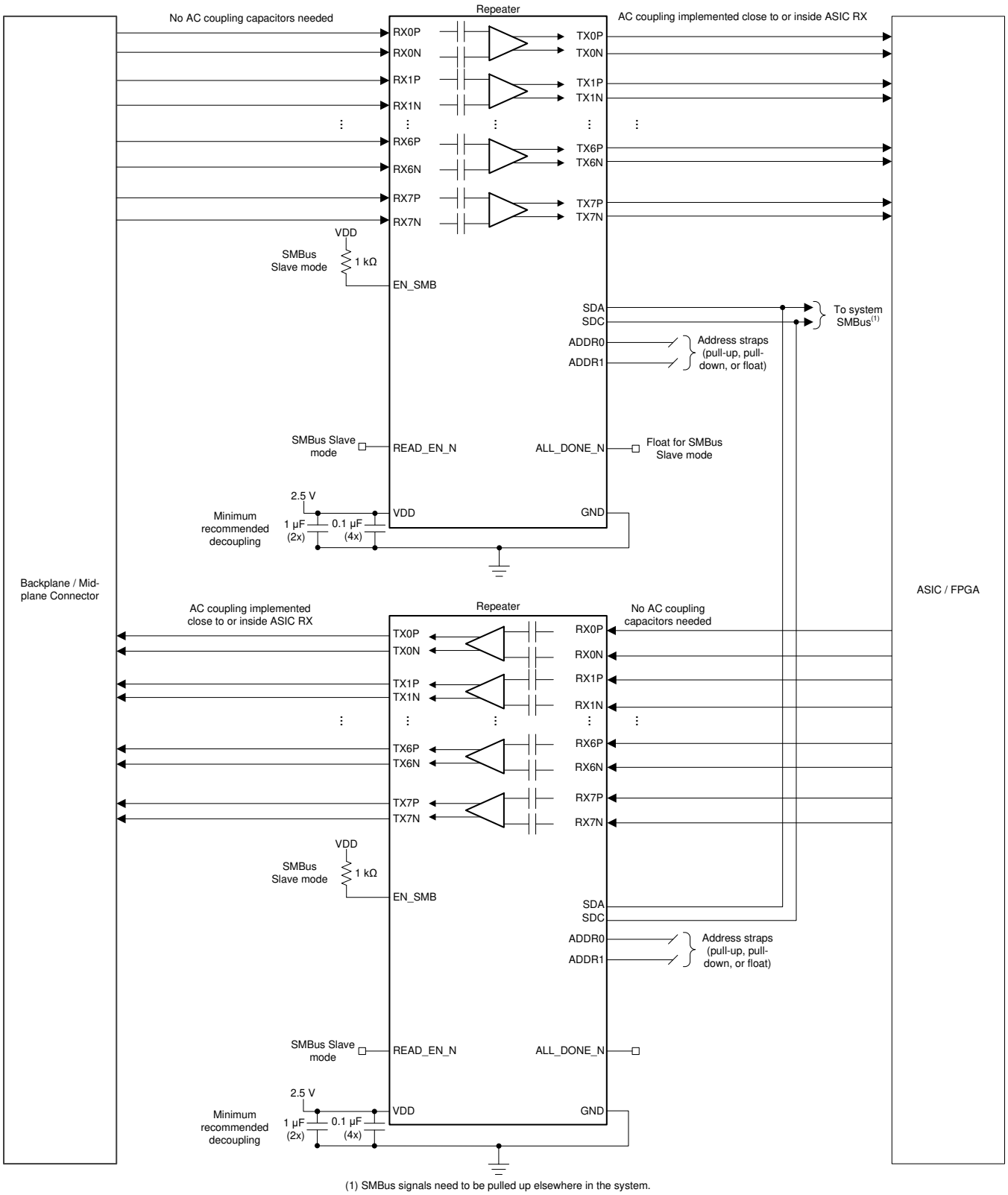


図 8. Typical Backplane and Mid-Plane Application Diagram

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

図 9. Typical Backplane and Mid-Plane Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

For backplane and mid-plane reach extension application use the guidelines in the table below.

DESIGN PARAMETER	REQUIREMENT
AC Coupling Capacitors	Generally not required. 220-nF AC coupling capacitors are included in the DS280BR820 package on the RX side.
Input Channel Insertion Loss	≥ 10 dB at 14 GHz as a rough guideline. For best performance, the input channel insertion loss should be greater than or equal to the equalizer boost setting used in the DS280BR820.
Output Channel Insertion Loss	Depends on downstream ASIC or FPGA SerDes capabilities. Should be ≥ 5 dB at 14 GHz as a rough guideline.
Total (Input + Output) Channel Insertion Loss	Depends on downstream ASIC or FPGA SerDes capabilities. The DS280BR820 can extend the reach between two ASICs by 17 to 22 dB beyond the ASICs' normal capabilities.
Link Partner TX Launch Amplitude	800 mV_{PP} to 1200 mV_{PP} differential.
Link Partner TX FIR Filter	Depends on the channel loss.

8.2.1.2 Detailed Design Procedure

The design procedure for backplane and mid-plane applications is as follows:

1. Determine the total number of channels on the board which require a DS280BR820 for signal conditioning. This will dictate the total number of DS280BR820 devices required. It is generally recommended that channels with similar total insertion loss on the board be grouped together in the same DS280BR820 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280BR820 devices. This may impact the selection of the regulator for the 2.5-V supply rail. To calculate the maximum current draw, multiply the maximum power supply current by the total number of DS280BR820 devices.
3. Determine the SMBus address scheme needed to uniquely address each DS280BR820 device on the board, depending on the total number of devices identified in step 1. Each DS280BR820 can be strapped with one of 16 unique SMBus addresses. If there are more DS280BR820 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I^2C expander like the TCA/PCA family of I^2C/SMBus switches and multiplexers to split the SMBus into multiple busses.
4. Determine if the device will be configured from EEPROM (SMBus master mode) or from the system SMBus (SMBus slave mode).
   a. If SMBus master mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
   b. If SMBus slave mode will be used for all device configurations, an EEPROM is not needed.
5. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to *Power Supply Recommendations* for more information.
6. If there is a need to potentially upgrade to a pin-compatible TI Retimer device, then make provisions in the schematic and layout for a 25-MHz (±100 ppm) single-ended CMOS clock. Each DS280BR820 buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) DS280BR820 calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5 V CMOS output, then no AC coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one DS280BR820 CAL_CLK_OUT output and the next DS280BR820's CAL_CLK_IN input. The final DS280BR820's CAL_CLK_OUT output can be left floating. A 25 MHz clock is not required for the DS280BR820, but it is good practice to provision for it in case there is a future plan to upgrade to a pin-compatible TI Retimer device.
7. If there is a need to potentially upgrade to a pin-compatible TI Retimer device, then connect the INT_N pin to an FPGA or CPU for interrupt monitoring. Note that multiple INT_N outputs can be connected together. The common INT_N net should be pulled high to 2.5 V or 3.3 V. The INT_N pin on the DS280BR820 does not perform the interrupt functionality that the equivalent pin on the pin-compatible Retimer device does; however, it is good practice to provision for this in case there is a future plan to upgrade to a pin-compatible TI Retimer device.

8.2.2 Front-Port Applications

The DS280BR820 has strong equalization capabilities that allow it to equalize insertion loss and extend the reach of front-port channels by 17 dB beyond the normal capabilities of the ASIC while support CAUI-4 and CR4 electrical requirements. The DS280BR820 is designed to apply gain in a linear fashion in order to support longer distances between the switch ASIC and the front-port module. A single DS280BR820 can be used to support all eight *egress* channels or all eight *ingress* channels for two 100 GbE ports. 図 10 illustrates this configuration.

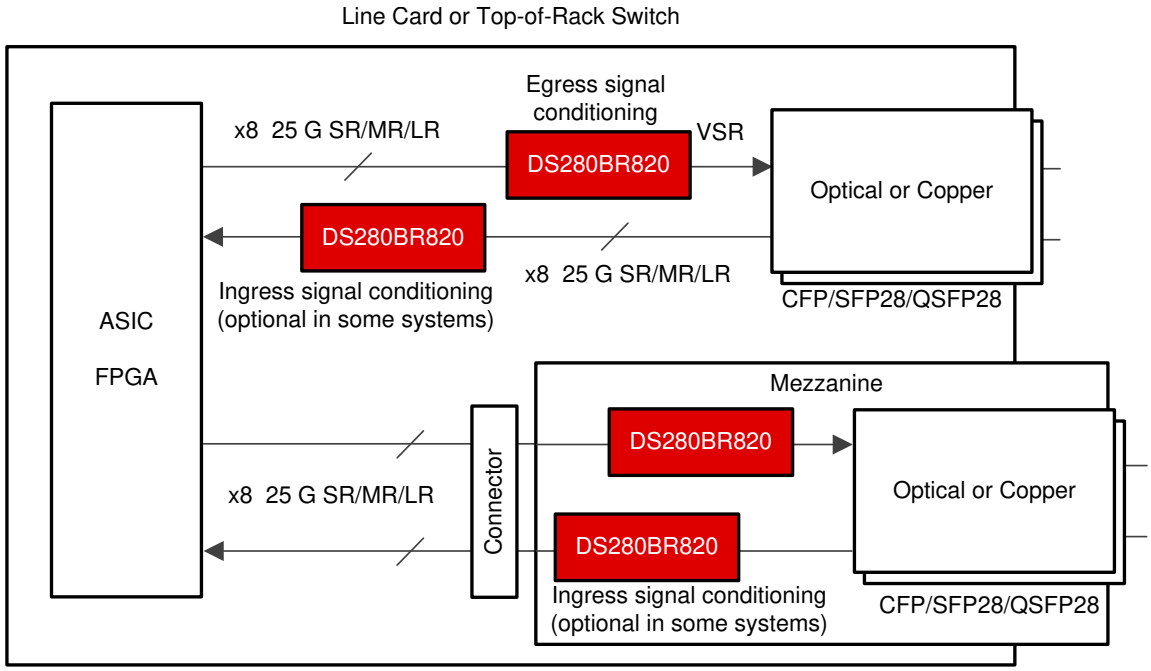


図 10. Typical Front-Port Application Diagram

Standard front-port modules have AC coupling capacitors included inside the module. The DS280BR820, therefore, is ideal for front-port Egress signal conditioning applications since it includes AC coupling capacitors on the input (RX) side and does not include AC coupling capacitors on the output (TX) side.

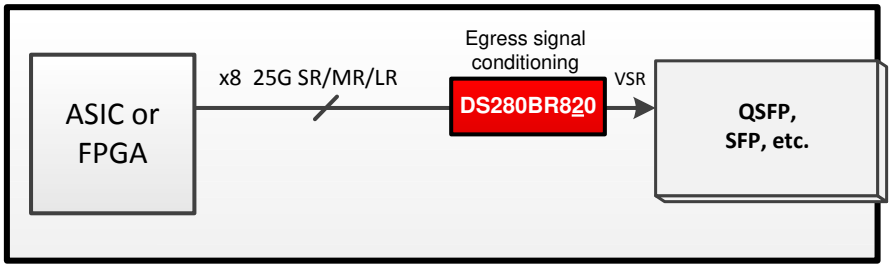


図 11. DS280BR820 Recommended for Front-port Egress

The optimum solution for front-port Ingress signal conditioning applications depends on whether the ASIC RX supports DC coupling and whether it can support an input common mode voltage of 1.05 V. For further guidance on determining if the ASIC RX supports DC coupling, refer to 図 7. If the ASIC RX supports DC coupling and can tolerate an input common mode voltage of 1.05 V or less, then the DS280BR820 is the optimum solution for front-port Ingress signal conditioning. If the ASIC RX does not support DC coupling or cannot tolerate an input common mode voltage of 1.05 V, then the pin-compatible DS280BR810 may be the optimum solution.

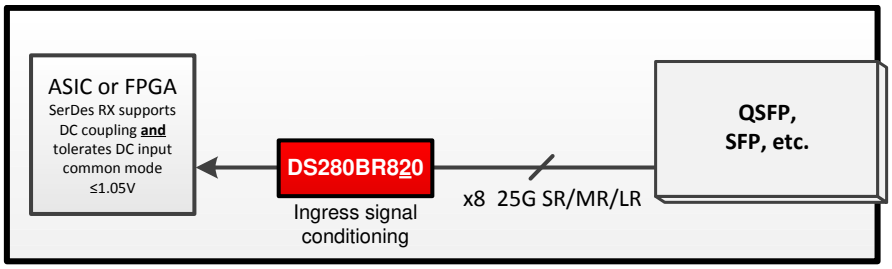


図 12. DS280BR820 Recommended for Front-port Ingress

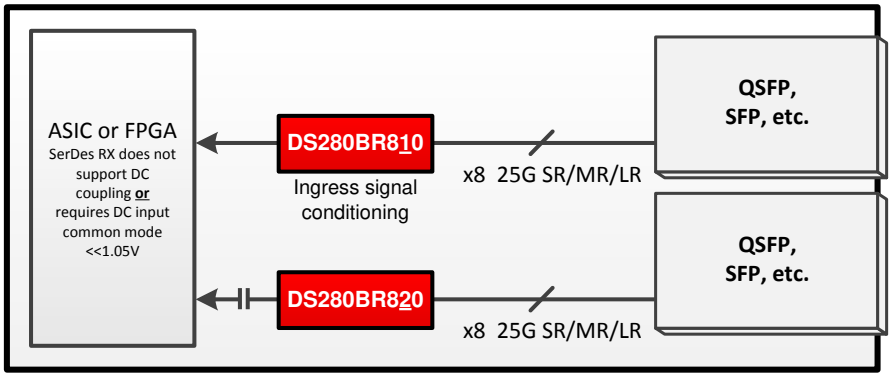
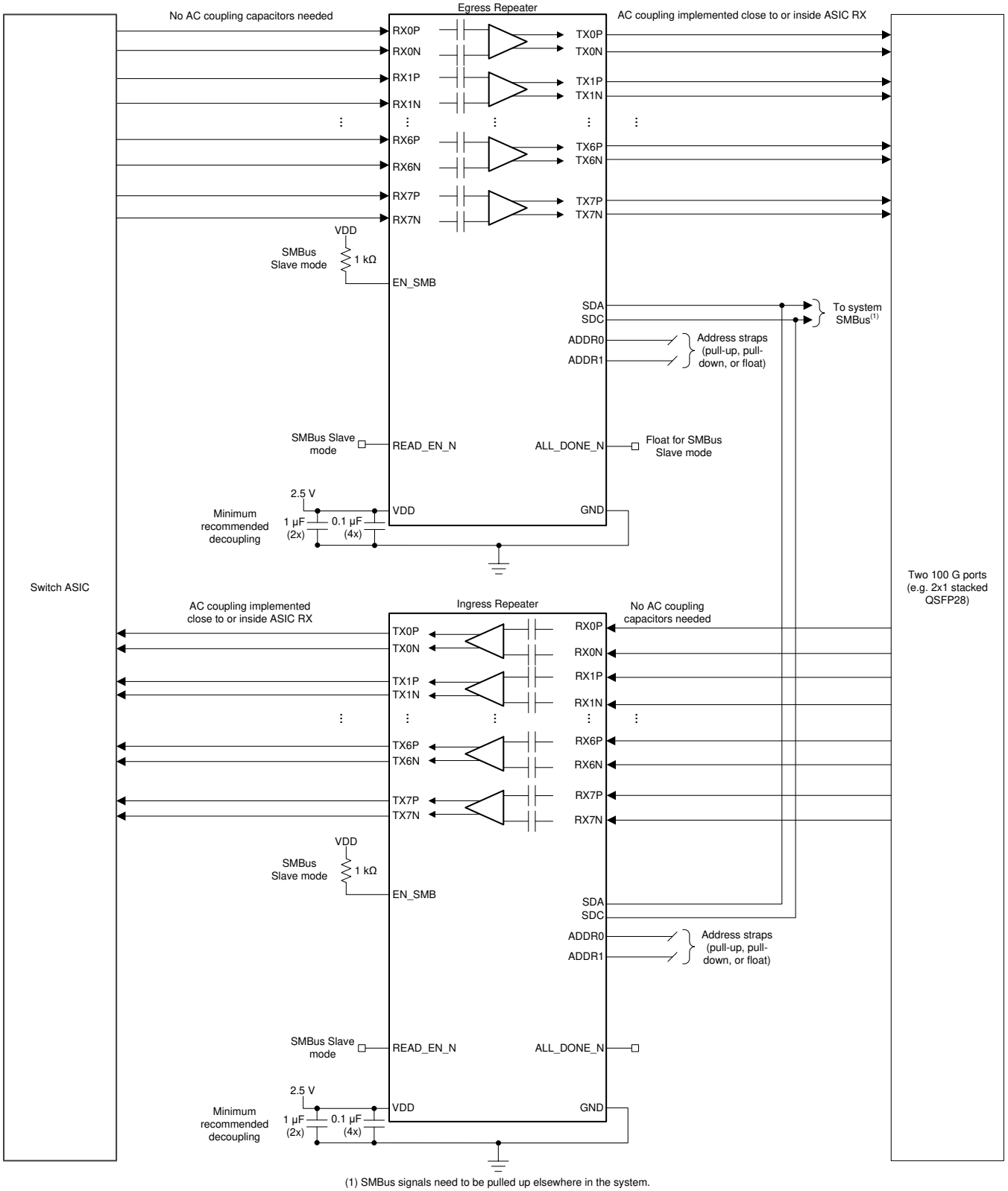


図 13. DS280BR820 or DS280BR810 Recommended for Front-port Ingress



(1) SMBus signals need to be pulled up elsewhere in the system.

図 14. Typical Front-port Schematic

8.2.2.1 Design Requirements

This section lists some critical areas for high speed printed circuit board design consideration and study.

DESIGN PARAMETER	REQUIREMENT
AC Coupling Capacitors	Generally not required. 220 nF AC coupling capacitors are included in the DS280BR820 package on the RX side.
Input Channel Insertion Loss	≥ 10 dB at 14 GHz as a *rough* guideline. For best performance, the input channel insertion loss should be greater than or equal to the equalizer boost setting used in the Repeater.
Output Channel Insertion Loss	For best performance in *egress* applications, place the Repeater close to the front-port cage. For best performance in *ingress* applications, place the Repeater with ≥ 5 dB loss at 14 GHz between the output and the downstream ASIC.
Switch ASIC TX Launch Amplitude	600 mVppd to 1000 mVppd

8.2.2.2 Detailed Design Procedure

The design procedure for front-port applications is as follows:

1. Determine the total number of channels on the board which require a DS280BR820 for signal conditioning. This will dictate the total number of DS280BR820 devices required for the board. It is generally recommended that channels belonging to the same QSFP port be grouped together in the same DS280BR820 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280BR820 devices. This may impact the selection of the regulator for the 2.5 V supply rail. To calculate the maximum current draw, multiply the maximum power supply current by the total number of DS280BR820 devices.
3. Determine the SMBus address scheme needed to uniquely address each DS280BR820 device on the board, depending on the total number of devices identified in step 1. Each DS280BR820 can be strapped with one of 16 unique SMBus addresses. If there are more DS280BR820 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I^2C expander like the TCA/PCA family of I^2C/SMBus switches and multiplexers to split the SMBus into multiple busses.
4. Determine if the device will be configured from EEPROM (SMBus master mode) or from the system I^2C bus (SMBus slave mode).
    1. If SMBus master mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
    2. If SMBus slave mode will be used for all device configurations, an EEPROM is not needed.
5. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to *Power Supply Recommendations* for more information.

8.2.3 Application Curves

8.2.3.1 Pattern Generator Characteristics

All of the example application results in the sections which follow were tested using a pattern generator with the following characteristics.

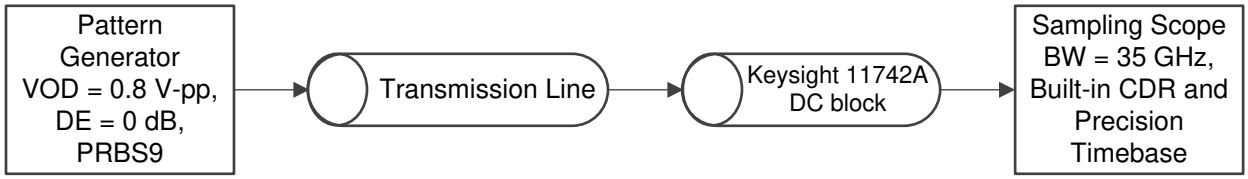


図 15. Pattern Generator Test Setup

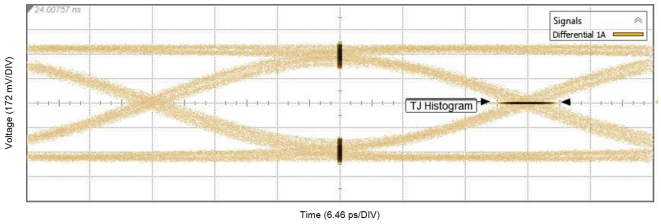


図 16. Pattern Generator Output at 25.78125 Gbps, 800 mVppd, PRBS9

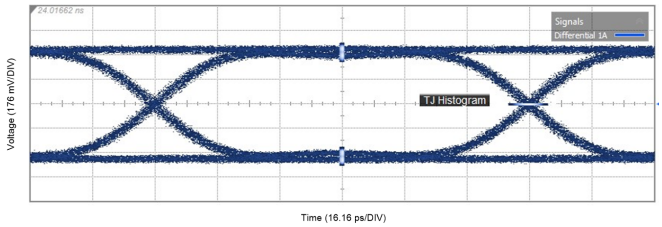


図 17. Pattern Generator Output at 10.31250 Gbps, 800 mVppd, PRBS9

表 5. Pattern Generator Characteristics

	25.78125 Gbps	10.3125 Gbps
Differential peak-to-peak voltage (VOD)	~800 mVppd	~800 mVppd
Channel loss between Pattern Generator and Scope	2 dB @ 12.9 GHz	1 dB @ 5.2 GHz
Total Jitter @ 1E-15	8.0 ps_{P-P}	13.4 ps_{P-P}
Differential Eye Height @ 1E-15	448 mV_{P-P}	596 mV_{P-P}

8.2.3.2 Equalizing Moderate Pre-Channel Loss

This example application result demonstrates the DS280BR820 equalizing for pre-channel insertion loss introduced by an FR4 channel.

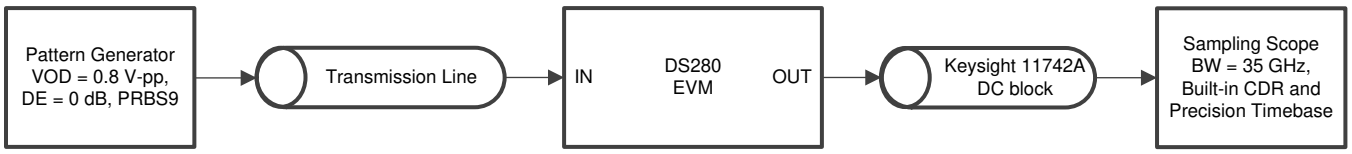


図 18. 5 in input Channel and Minimal Output Channel Test Setup

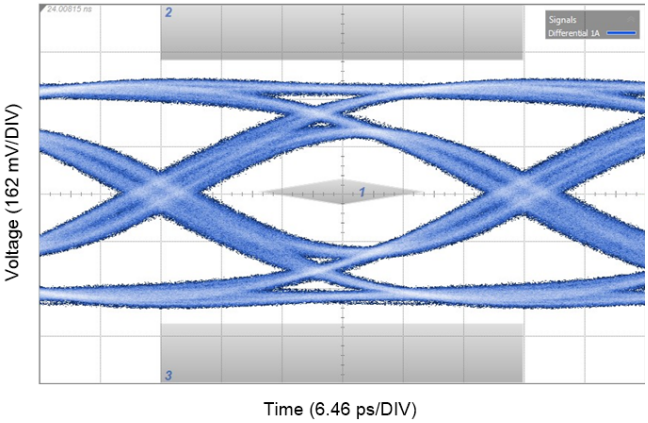


図 19. 25.78125 Gbps CAUI-4 Eye Mask with 5 in Input Channel and Minimal Output Channel

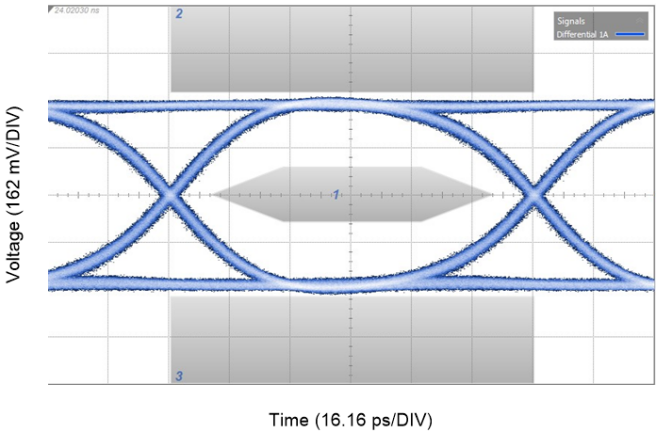


図 20. 10.3125 Gbps nPPI Eye Mask with 5 in Input Channel and Minimal Output Channel

表 6. Settings and Measurements for CAUI-4 and nPPI with 5 in Input Channel and Minimal Output Channel

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line 1	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR820 Rx Channel Loss	14 dB @ 12.9 GHz	6 dB @ 5.2 GHz
DS280BR820 Tx Channel Loss	4.5 dB @ 12.9 GHz	2 dB @ 5.2 GHz
EQ BST1	3	3
EQ BST2	0	0
EQ BW	3	3
VOD	3	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	11.9 ps_{P-P}	13.0 ps_{P-P}
Differential Eye Height @ 1E-15	338 mV_{P-P}	544 mV_{P-P}
Mask violations	0	0

8.2.3.3 Equalizing High Pre-Channel Loss

This example application result demonstrates the DS280BR820 equalizing for pre-channel insertion loss introduced by an FR4 channel.

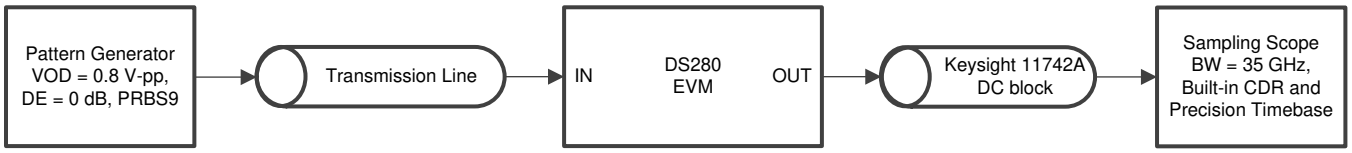


図 21. 10 in Input Channel and Minimal Output Channel Test Setup

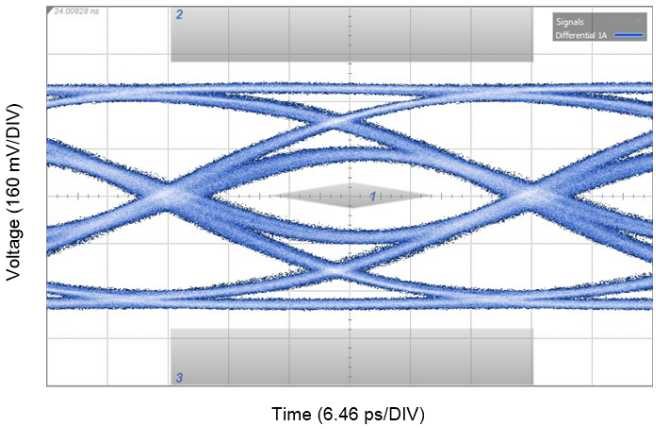


図 22. 25.78125 Gbps CAUI-4 Eye Mask with 10 in Input Channel and Minimal Output Channel

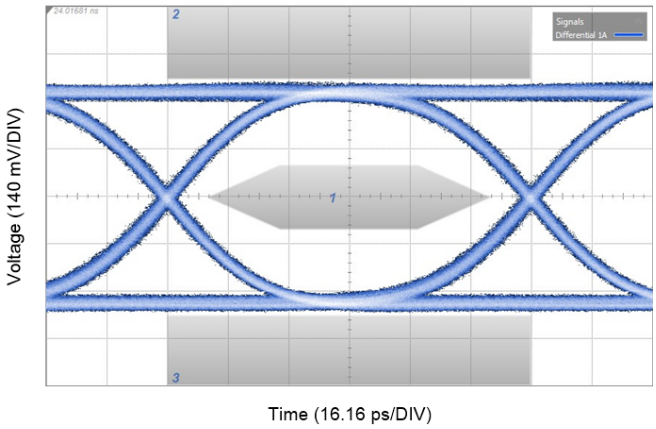


図 23. 10.1325 Gbps nPPI Eye Mask with 10 in Input Channel and Minimal Output Channel

表 7. Settings and Measurements for CAUI-4 and nPPI with 10 in Input Channel and Minimal Output Channel

	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line 1	10 in 5 mil FR4 + 8 in SMA cable	10 in 5 mil FR4 + 8 in SMA cable
DS280BR820 Rx Channel Loss	22 dB @ 12.9 GHz	10 dB @ 5.2 GHz
DS280BR820 Tx Channel Loss	4.5 dB @ 12.9 GHz	2 dB @ 5.2 GHz
EQ BST1	6	6
EQ BST2	1	1
EQ BW	3	3
VOD	3	2
EQ DC Gain Mode	Low	Low
Total Jitter @ 1E-15	11.3 ps_{P-P}	13.5 ps_{P-P}
Differential Eye Height @ 1E-15	210 mV_{P-P}	532 mV_{P-P}
Mask violations	0	0

8.2.3.4 Equalizing High Pre-Channel Loss and Moderate Post-Channel Loss

This example application result demonstrates the DS280BR820 equalizing for pre-channel and post-channel insertion loss introduced by FR4 channels.

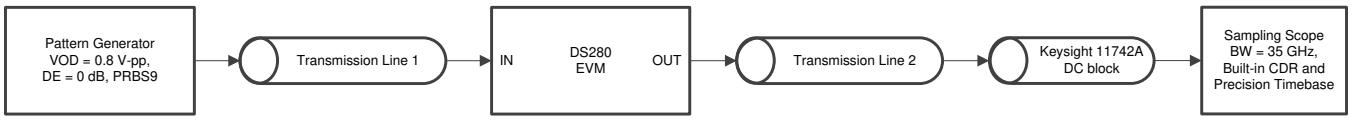


図 24. 10 in Input Channel and 5 in Output Channel Test Setup

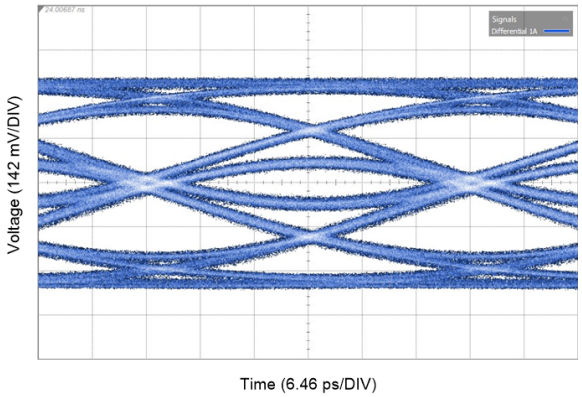


図 25. 25.78125 Gbps Eye Diagram with 10 in Input Channel and 5 in Output Channel, Linear Mode

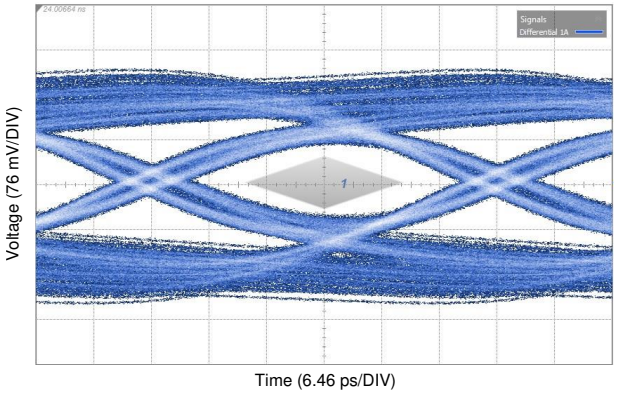


図 26. 25.78125 Gbps CAUI-4 Eye Mask with 10 in Input Channel and 5 in Output Channel, FIR Limiting Mode

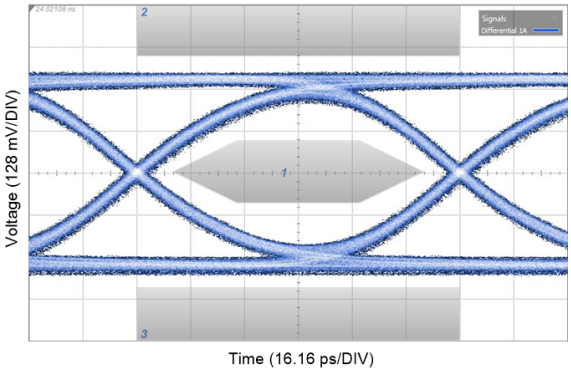


図 27. 10.1325 Gbps nPPI Eye Mask with 10 in Input Channel and 5 in Output Channel, Linear Mode

表 8. Settings and Measurements for CAUI-4 and nPPI with 10 in Input Channel and 5 in Output Channel

	25.78125 Gbps (CAUI-4)	25.78125 Gbps (CAUI-4)	10.3125 Gbps (nPPI)
Transmission Line 1	10 in 5 mil FR4 + 8 in SMA cable	10 in 5 mil FR4 + 8 in SMA cable	10 in 5 mil FR4 + 8 in SMA cable
Transmission Line 2	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable	5 in 5 mil FR4 + 8 in SMA cable
DS280BR820 Rx Channel Loss	22 dB @ 12.9 GHz	22 dB @ 12.9 GHz	10 dB @ 5.2 GHz
DS280BR820 Tx Channel Loss	14.5 dB @ 12.9 GHz	14.5 dB @ 12.9 GHz	6 dB @ 5.2 GHz
EQ BST1	7	7	7
EQ BST2	7	7	7
EQ BW	3	3	3
VOD	3	3	2
EQ DC Gain Mode	Low	Low	Low
Tx Mode	Linear	FIR Limiting	Linear
Tx Main-Cursor	N/A	16	N/A
Tx Pre-Cursor	N/A	5	N/A
Tx Post-Cursor	N/A	10	N/A
Total Jitter @ 1E-15	14.8 ps_{P-P}	14.8 ps_{P-P}	17.0 ps_{P-P}
Differential Eye Height @ 1E-15	67 mV_{P-P}	118 mV_{P-P}	407 mV_{P-P}
Mask violations	N/A	0	0

8.2.3.5 Output in FIR Limiting Mode with 16T Pattern

This example application result demonstrates the DS280BR820's output in FIR limiting mode.

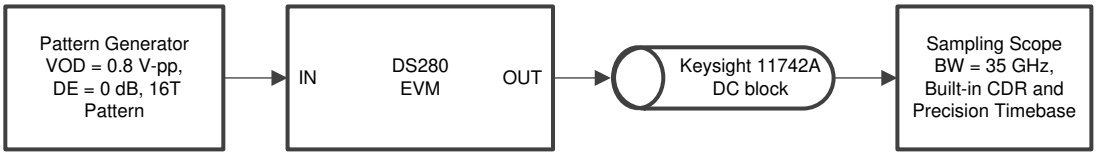


図 28. FIR Test Setup

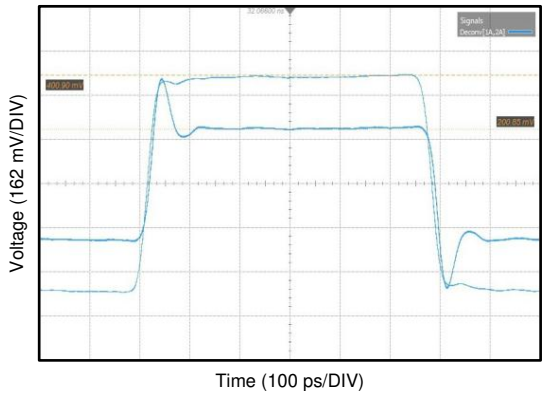


図 29. FIR Post-Cursor Example

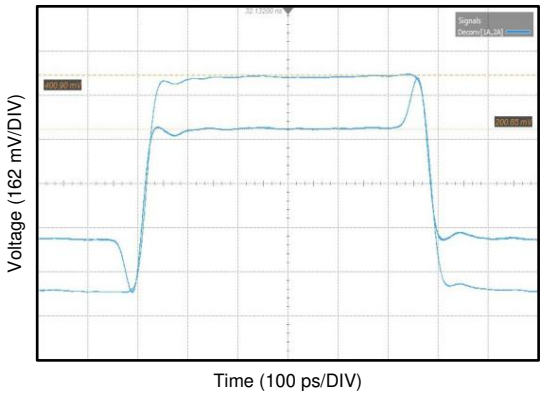


図 30. FIR Pre-Cursor Example

表 9. Example FIR Settings

図 29	図 30
(Pre, Main, Post) = (0, 12, 0)	(Pre, Main, Post) = (0, 12, 0)
(Pre, Main, Post) = (0, 16, 15)	(Pre, Main, Post) = (11, 12, 0)

8.3 Initialization Set Up

The DS280BR820 does not require any particular start-up or initialization sequence. The device defaults to a medium boost value for each channel. It is recommend that the channels be appropriately configured before data traffic is transmitted to the DS280BR820 to avoid issues with the link partner ASIC's adaption. Example configuration settings can be found in the DS280BR820 Programming Guide.

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions outlined in *Specifications* in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the DS280BR820 is provided in *Specifications*. This figure can be used to calculate the maximum current the supply must provide. Typical mission-mode current draw can be inferred from the typical power consumption in *Specifications*.
3. The DS280BR820 ***does not*** require any special power supply filtering, such as ferrite beads, provided the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1-µF capacitor per power pin, and single 1.0-µF and 10-µF bulk capacitors.

10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing them directly underneath the device is one option if the board design permits.
2. High-speed differential signals should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, care should be taken to minimize the via stub, either by transitioning through most or all layers, or by back drilling.
4. GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
6. BGA landing pads for a 0.8 mm pitch flip-chip BGA are typically 0.4 mm in diameter (exposed). The actual size of the copper pad will depend on whether solder-mask-defined (SMD) or non-solder-mask-defined solder land pads are used. For more information, refer to TI's Surface Mount Technology (SMT) References website.

10.2 Layout Examples

10.2.1 Stripline Example

The following example layout demonstrates how all signals can be escaped from the BGA array using stripline routing on a generic 8+ layer stackup. This example layout assumes the following:

- Trace width: 0.15 mm (6 mil)
- Trace edge-to-edge spacing: 0.16 mm (6.4 mil)
- VIA finished hole size (diameter): 0.254 mm (10 mil)
- VIA-to-VIA spacing: 1.0 mm (39 mil), to enhance PCB manufacturability
- No VIA-in-pad used

Note that many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing will depend on the PCB material, PCB routing density, and other factors. Microstrip escape routing is also possible and may be preferable in some application scenarios such as front-port applications.

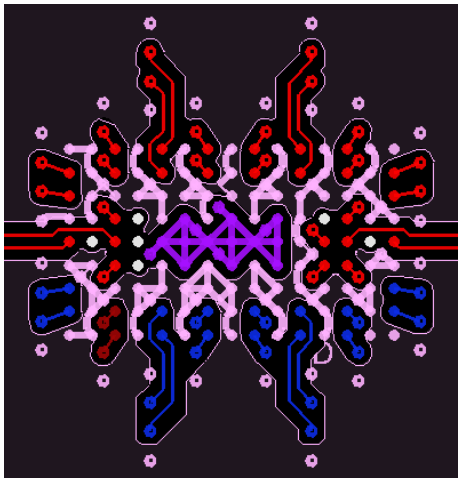


図 31. Stripline Example, Top Layer

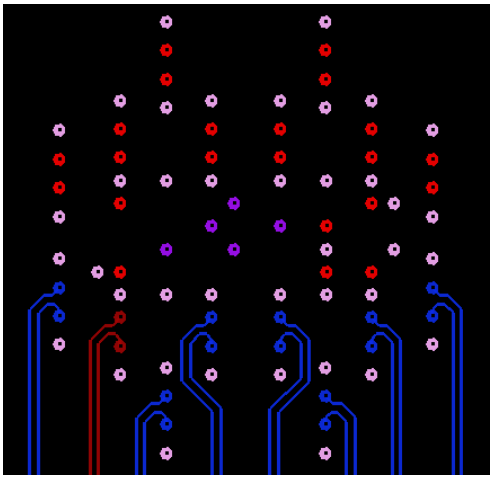


図 32. Stripline Example, Internal Signal Layer 1

Layout Examples (continued)

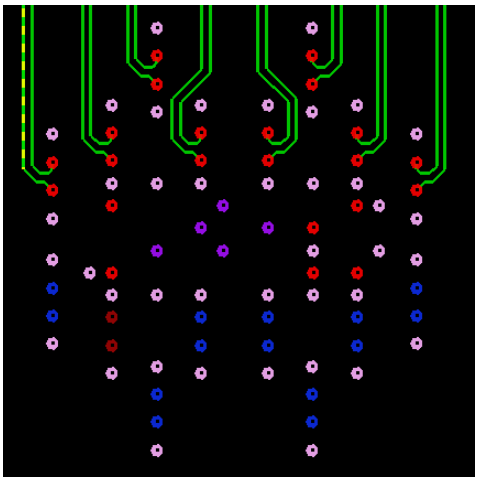


図 33. Stripline Example, Internal Signal Layer 2

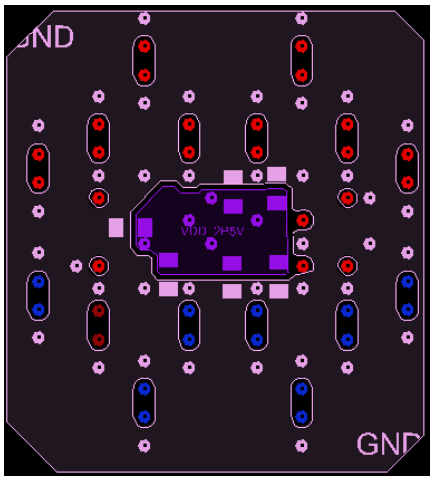


図 34. Stripline Example, Bottom Layer

10.2.2 Microstrip Example

The following example layout demonstrates how all signals can be escaped from the BGA array using microstrip routing on a generic 8+ layer stackup. This example layout assumes the following:

- Normal trace width: 0.27 mm (10.5 mil)
- Neck-down trace width: 0.18 mm (7 mil)
- Trace edge-to-edge spacing: 0.51 mm (20 mil)
- VIA finished hole size (diameter): 0.203 mm (8 mil)
- VIA-to-VIA spacing: 0.8 mm (31.5 mil)
- No VIA-in-pad used

Note that many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing will depend on the PCB material, PCB routing density, and other factors. Stripline escape routing is also possible and may be preferable in some application scenarios such as backplane applications.

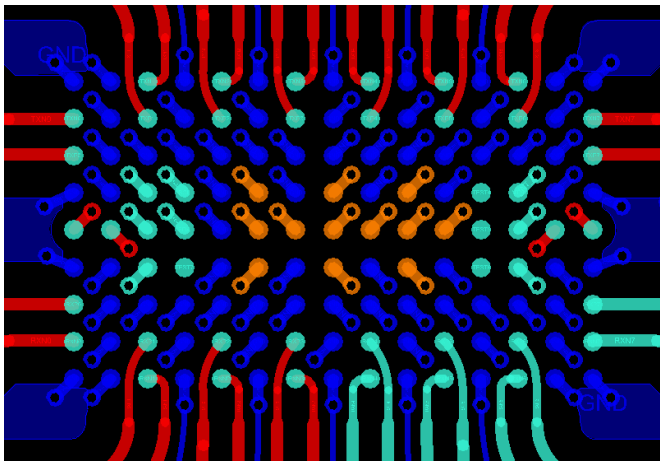


図 35. Microstrip Example, Top Layer

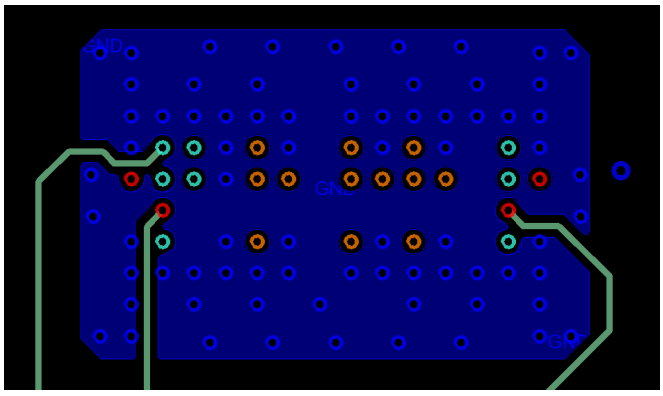


図 36. Microstrip Example, Internal Signal Layer 1

Layout Examples (continued)

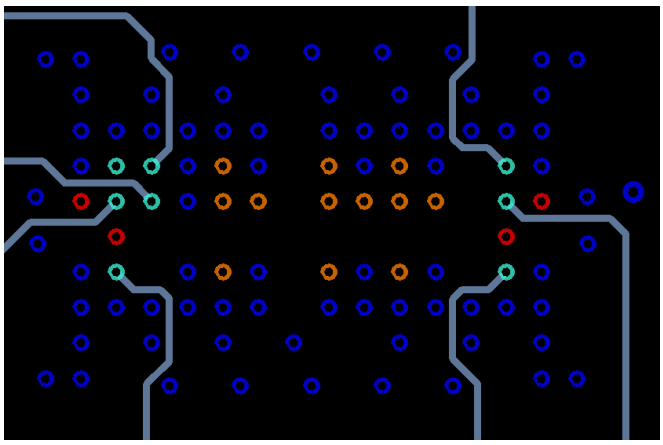


図 37. Microstrip Example, Internal Signal Layer 2

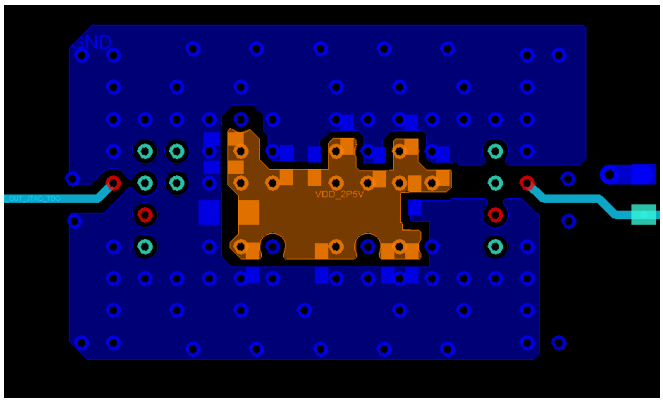


図 38. Microstrip Example, Bottom Layer

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『DS280BR810EVM, DS280BR820EVM』ユーザー・ガイド (英語)*
- テキサス・インスツルメンツ、*『DS280BR810』プログラミング・ガイド (英語)*
- テキサス・インスツルメンツ、*『Understanding EEPROM Programming for 25-G to 28-G Repeaters and Retimers』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『Selection Guide for TI 25G and 28G Retimers and Redrivers』アプリケーション・レポート (英語)*

11.2 ドキュメントの更新通知を受け取る方法

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11.4 静電気放電に関する注意事項

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS280BR820ZBLR	Active	Production	NFBGA (ZBL) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8A
DS280BR820ZBLR.A	Active	Production	NFBGA (ZBL) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8A
DS280BR820ZBLT	Active	Production	NFBGA (ZBL) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8A
DS280BR820ZBLT.A	Active	Production	NFBGA (ZBL) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280BR8A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

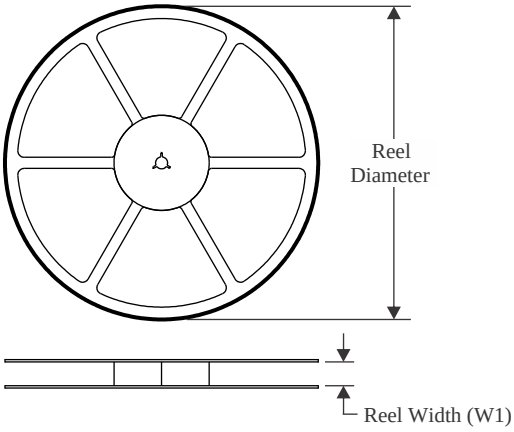
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

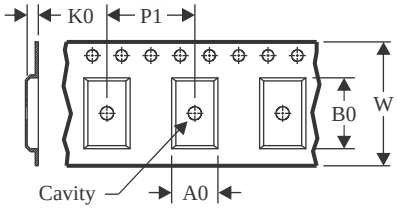
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

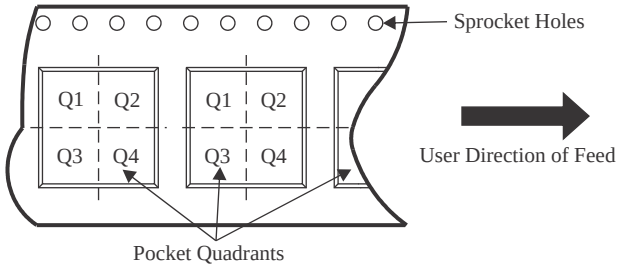


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

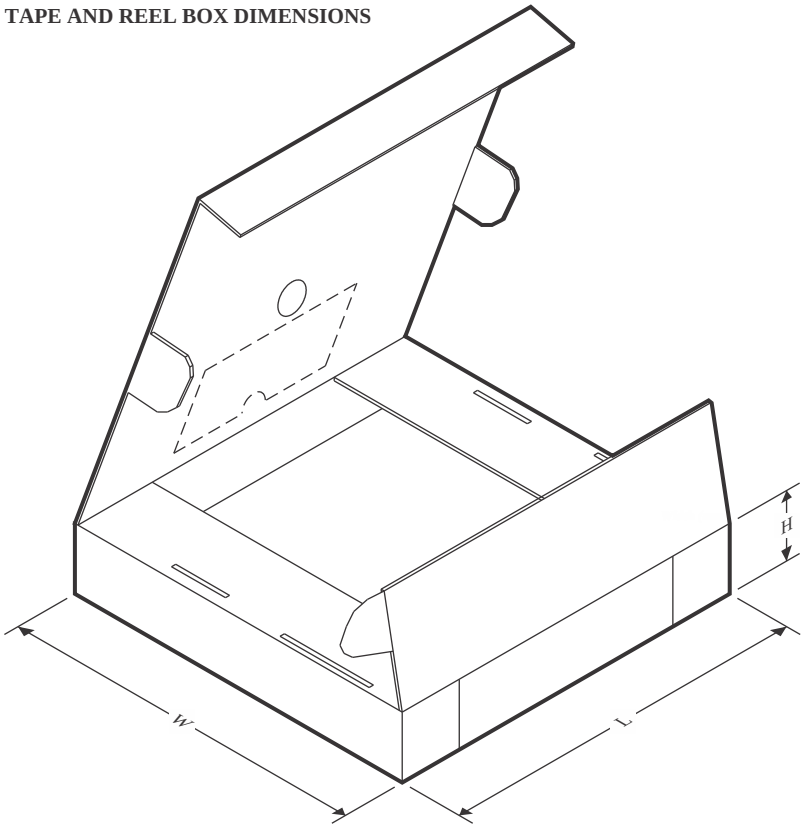
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS280BR820ZBLR	NFBGA	ZBL	135	1000	330.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2
DS280BR820ZBLT	NFBGA	ZBL	135	250	178.0	24.4	8.4	13.4	1.9	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

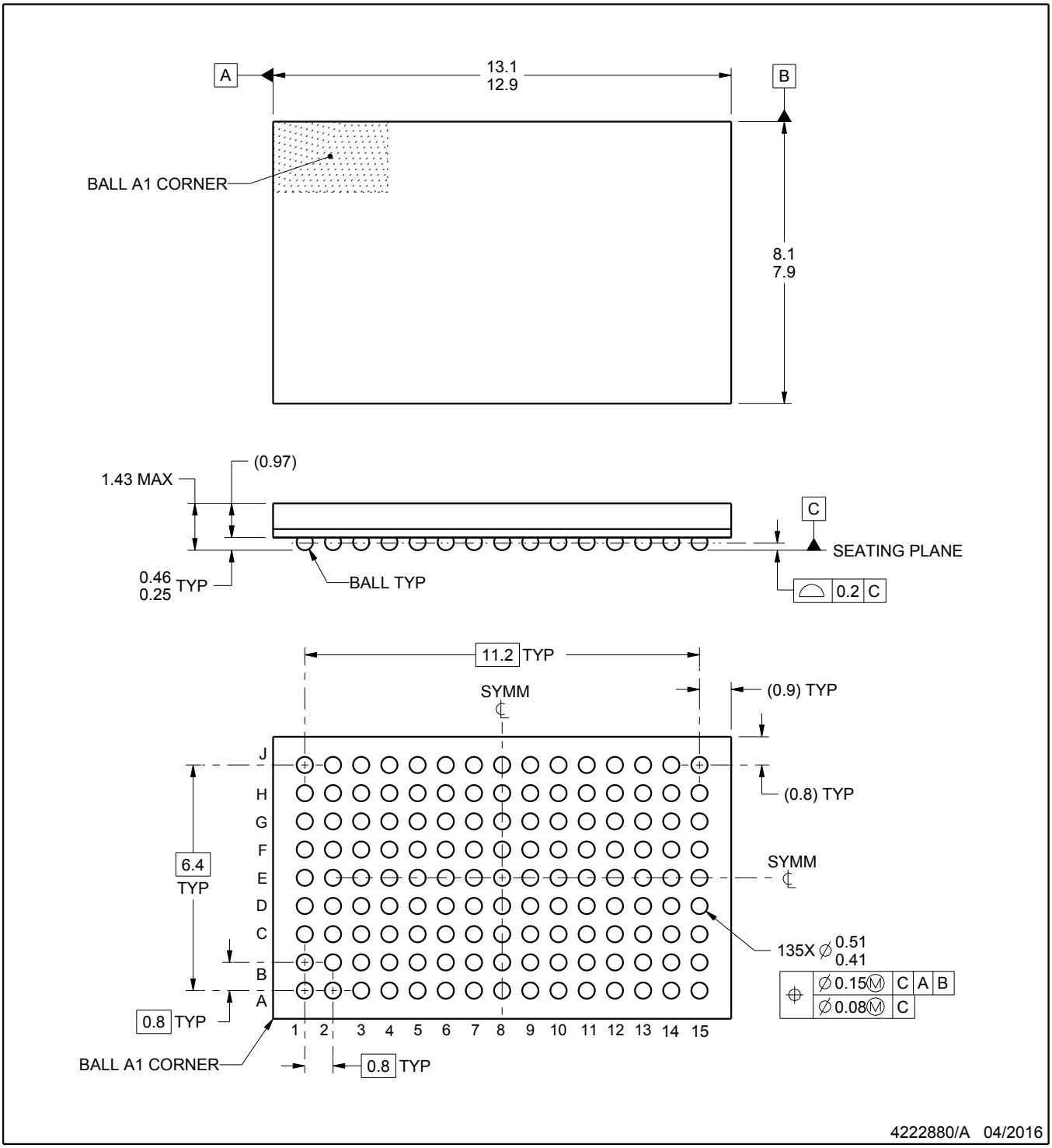
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS280BR820ZBLR	NFBGA	ZBL	135	1000	356.0	356.0	45.0
DS280BR820ZBLT	NFBGA	ZBL	135	250	213.0	191.0	55.0

PACKAGE OUTLINE

ZBL0135A

NFBGA - 1.43 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

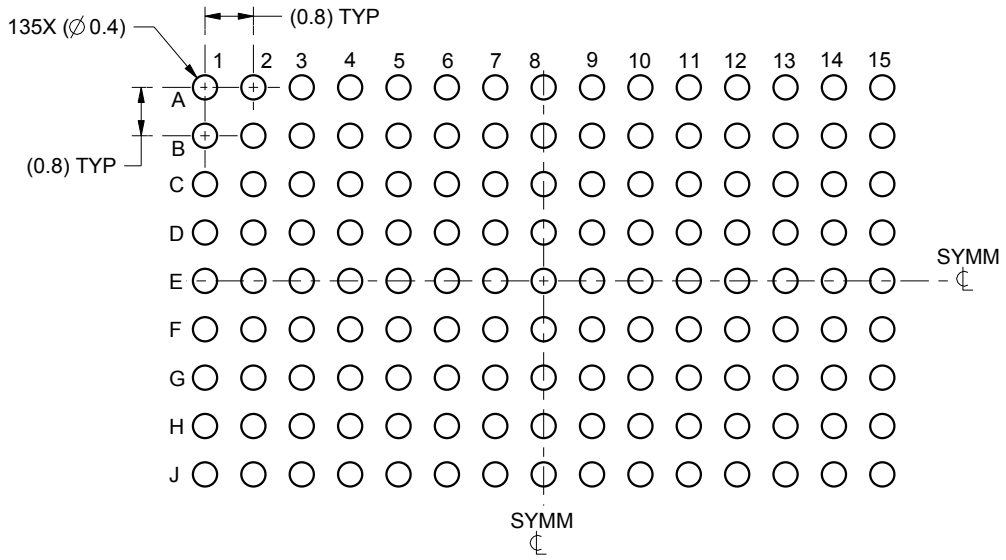
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

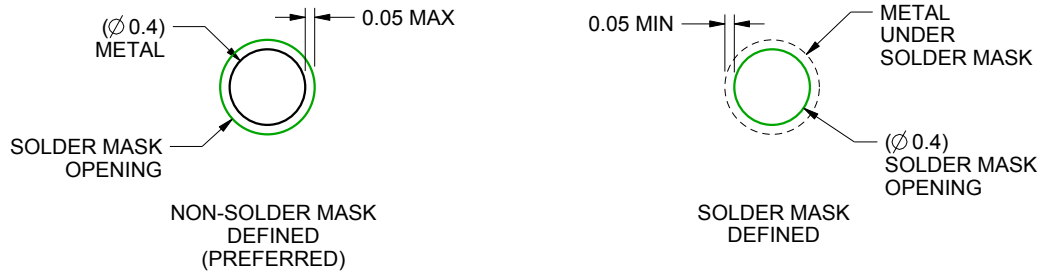
ZBL0135A

NFBGA - 1.43 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:8X

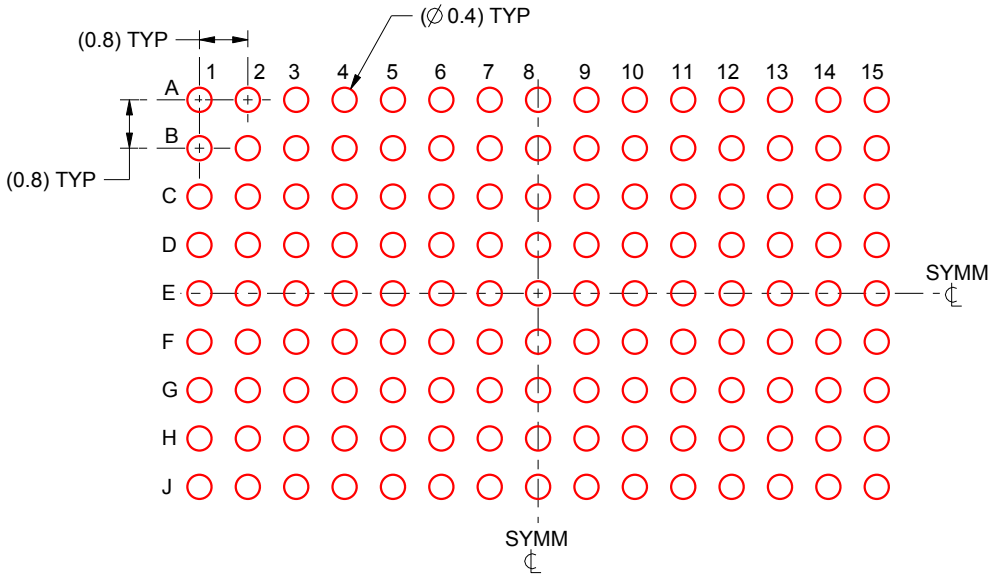


SOLDER MASK DETAILS
NOT TO SCALE

4222880/A 04/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4222880/A 04/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月