DS90UB936-Q1 デュアル 3Gbps FPD-Link III デシリアライザ・ハブ、

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 2:-40℃～+105℃の動作時周囲温度範囲
- チャネルごとに 2.528Gbps の CSI-2 ビデオ帯域幅
- MIPI DPHY バージョン 1.2 / CSI-2 バージョン 1 .3 準拠
  - CSI-2 出力ポート
  - 1、2、4 データ・レーンをサポート
  - CSI-2 のデータ・レートは、データ・レーンごとに 400Mbps / 800Mbps / 1.5Gbps / 1.6Gbps にスケーリング可能
  - データ型をプログラミング可能
  - 4 つの仮想チャネル
  - ECC および CRC 生成
- 2×2 出力複製モード
- 非常に短いデータおよび制御パスのレイテンシ
- シングル・エンドの同軸またはシールド付きツイストペア (STP) ケーブルに対応
- 適応型受信イコライゼーション
- I2C で最大 1Mbps のファスト・モード・プラスに対応
- 柔軟な GPIO によるカメラの診断
- DS90UB935-Q1、DS90UB953-Q1、DS90UB933-Q1、DS90UB913A-Q1 シリアライザと互換
- ライン・フォルト検出および高度な診断
- ISO 10605 および IEC 61000-4-2 ESD に準拠

2 アプリケーション

- 車載用 ADAS
  - リアビュー・カメラ (RVC)
  - サラウンド・ビュー・システム (SVS)
  - カメラ監視システム (CMS)
  - 前方視野カメラ (FC)
  - ドライバー監視システム (DMS)
  - 衛星用レーダー、タイム・オブ・フライト (ToF) および LIDAR センサ・モジュール
- セキュリティと監視
- 産業用および医療用イメージング

3 概要

DS90UB936-Q1 は、多用途なデシリアライザで、FPD-Link III インターフェイスを介してソースから、シリアル化されたセンサ・データを受信できます。ペアで使用することにより、DS90UB935-Q1 シリアライザを使用すると、DS90UB936-Q1 は最大 2.528Gbps の CSI-2 スループットでイメージャからデータを受信できます。DS90UB936-Q1 は、DS90UB933-Q1 や DS90UB913A-Q1 など、互換性のある他のシリアライザと組み合わせて使用することもできます。2 レーン動作用に CSI-2 インターフェイスを構成すれば、二重の MIPI CSI-2 クロック・レーンを利用して出力を複製できます。複製モードでは、ビデオ・ストリームの 2 つのコピーが作成され、データの記録や並列処理に使用できます。

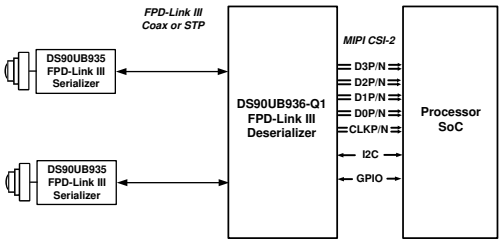
DS90UB935/936-Q1 チップセットは AEC-Q100 認定済みで、50Ω のシングルエンド同軸または 100Ω の差動 STP ケーブルでデータを受信するように設計されています。AEC-Q100 認定には、デバイス温度グレード 2 (動作時周囲温度範囲 -40℃～+105℃)、デバイス HBM ESD 分類レベル ±4.5kV、デバイス CDM ESD 分類レベル C5 が含まれています。このデシリアライザ・ハブは Power-over-Coax アプリケーションに最適で、受信イコライザは追加プログラミング不要で、ケーブルの損失特性に応じて自動的に補償を行い、ケーブルの経時劣化にも対応します。

各 FPD-Link III インターフェイスには、独立した低レイテンシの双方向制御チャネル (BCC) が含まれ、I2C、GPIO、その他の制御情報を連続的に伝送します。センサの同期および診断機能に必要な GPIO 信号も、この BCC を使用します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DS90UB936-Q1	VQFN (48)	7.00mm × 7.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2018) to Revision C (January 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 古い用語を使用している部分のすべてをコントローラとターゲットに変更	1
• 互換デバイスのリストを更新し、DS90UB953-Q1 を追加	1
• Revised the PDB pin voltage for normal operation	4
• Changed the VDD11 pin descriptions for clarity	4
• Added a link to Design Requirements under the RIN pins	4
• Updated the V_{IH} and V_{IL} specifications of pins PDB, XIN/REFCLK, and VDD_SEL	10
• Removed the mention of CSI-2 non-synchronous clocking mode	26
• Changed the bits that need to be modified for Clock Mode	27
• Removed the mention of setting the REF_CLK_MODE bit as it is a reserved bit	42
• Fixed typos in the internal FrameSync calculations	46
• Rewrote the basic synchronized forwarding code example to set both sensors to use CSI-2 serializers	48
• Added in that V_{VDDIO} must match V_{I2C}	54
• Removed the mention of 'PDB' from register 0x0D	76
• Changed BCC_Config Register[2:0] binary setting value 0b111 to reserved	100
• Changed PORT_CONFIG2[5] default value to 0x1	114
• Changed suggested ferrite beads for 4G FPD-Link PoC Network from 1500 kΩ to 1.5 kΩ	141
• Changed PoC network impedance recommendation from 2kΩ to 1kΩ	141
• Updated the PoC description	141
• Removed the insertion and return loss values from the table on Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks	141
• Added a note to explain the differences between the decoupling capacitors	145
• Changed the value of the capacitor for pin VDD11_CSI from 1-µF to 10-µF in the diagram where VDD_SEL = HIGH	145
• Moved the additional notes in the typical application diagram from the picture to below the diagram	145
• Added a note to clarify the power-up sequence between VDD18 and VDDIO	150

- Removed T0 and T2 from power-up sequence..... 150
- Added a note to clarify that a hard reset is optional in the power-up sequence..... 150
- Added in T7, the PDB to I2C ready delay, to the power-up sequence..... 150
- Changed the pull-up resistor for PDB from 33-kΩ to 10-kΩ..... 151

Changes from Revision A (April 2018) to Revision B (June 2018) **Page**

- Added discrete synch signals requirement when using DVP format 27
- Changed FPD3_PCLK to f_{PCLK} in the RAW mode line rate calculations 27
- Added information about YUV support 27
- Relaxed REFCLK Oscillator jitter specification to 200 ps maximum 28
- Relaxed REFCLK Oscillator rise and fall time to 6 ns maximum 28
- Added REFCLK spread-spectrum modulation percentage and frequency 28
- Updated Forward Channel GPIO typical latency value 36
- Updated Back Channel GPIO typical latency and jitter for 50 Mbps rate 37
- Added need for discrete synch signals in DVP mode and included RAW/YUV support 40
- Changed from GPIO7 pin to GPIO6 pin 44
- Deleted sentence "It is recommended to forward the relevant RX port data streams prior to enabling the 47
- CSI-2 TX output"..... 47
- Added Enabling and Disabling the CSI-2 Transmitter section 47
- Added sentence about RX port specific register for registers 0x4A, 0x4B, 0x4D - 0x7F, 0xD0 - 0xDF..... 93
- Updated RX_PORT_STS2 register bit 1 field and description 96
- Changed PAR_ERROR line _BYTE_1 to PAR_ERROR _BYTE_1 and RX PARITY CHECKER ENABLE to RX_PARITY_CHECKER_ENABLE 99
- Redraw the PoC Network diagram 141
- Updated Return Loss S11 values 141
- Redraw RINx STP setting for figure "Typical Connection Diagram STP With External 1.1-V supply"..... 145

Changes from Revision * (March 2018) to Revision A (April 2018) **Page**

- Deleted the duplicate $I_{DD2\text{-}R1T4}$ parameters from the *DC Electrical Characteristics* table..... 10
- Deleted the duplicate $I_{DD2\text{-}R2T22}$ parameter from the *DC Electrical Characteristics* table..... 10
- Deleted the duplicate $I_{DD2\text{-}R1T22}$ parameter from the *DC Electrical Characteristics* table..... 10
- Deleted the strap input current spec..... 10
- Changed the output short circuit current symbol from I_{SC} to I_{OS} 10
- Added 12-bit LF mode description and added 12-bit HF notation in the *Strap Configuration Mode Select* table 27
- Changed BCC_Config Register 0x58[2:0] binary setting value from 0b100 to 0b010 to select 10 Mbps non-synchronous back channel rate..... 100

5 Pin Configuration and Functions

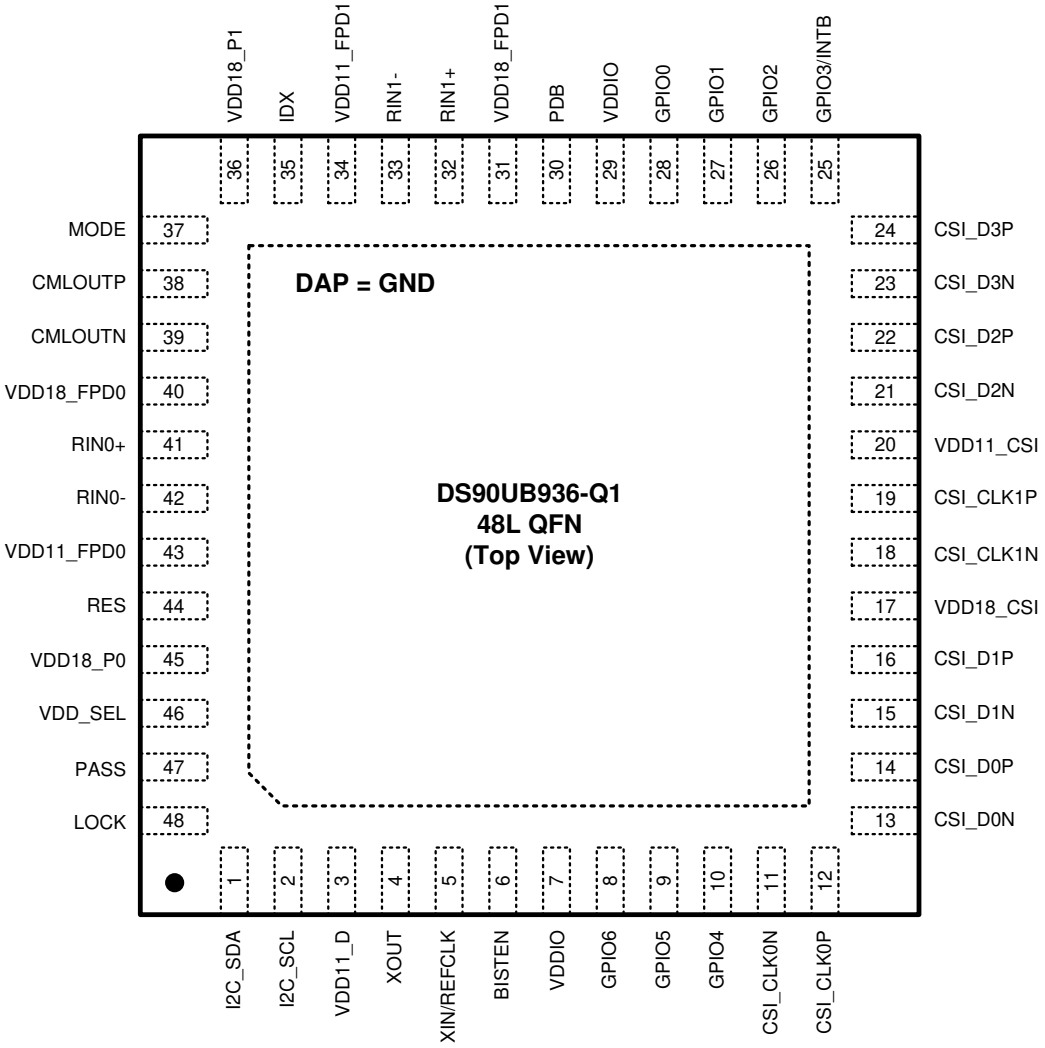


図 5-1. RGZ Package 48-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
RECEIVE DATA CSI-2 OUTPUT			

表 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
CSI_D3P	24	O	RECEIVE DATA OUTPUT: This signal carries data from the FPD-LINK III Deserializer to the processor over CSI-2 interface. Receive data is CSI-2 configured with DPHY outputs as one differential clock lane (CSI_CLK0P/N) and up to four differential data lanes (CSI_D0P/N: CSI_D3P/N) or two clock lanes (CSI_CLK0P/N, CSI_CLK1P/N) and two differential data lanes for each clock. When in replicate mode data lanes CSI_D2P/N and CSI_D3P/N are associated with clock lane CSI_CLK1P/N to provide the replicated output. For unused outputs leave as No Connect.
CSI_D3N	23		
CSI_D2P	22		
CSI_D2N	21		
CSI_CLK1P	19		
CSI_CLK1N	18		
CSI_D1P	16		
CSI_D1N	15		
CSI_D0P	14		
CSI_D0N	13		
CSI_CLK0P	12		
CSI_CLK0N	11		
CLOCK INTERFACE			
XOUT	4	O	Crystal oscillator output: Output Pin for providing crystal oscillator reference. Leave this pin NC when reference clock input is driving XIN/REFCLK.
XIN/REFCLK	5	S, I	Reference clock input or crystal oscillator input. Pin is shared with XIN and REFCLK. Typically REFCLK connected to 23- to 26-MHz reference oscillator output (100 ppm) or XIN configured with external 23- to 26-MHz crystal to XOUT. See *セクション 7.4.4*.
SYNCHRONIZATION AND GPIO			
GPIO0	28	I/O, PD	General-Purpose Input/Output: Pins can be used to control and respond to various commands. They may be configured to be the input signals for the corresponding GPIOs on the serializer or they may be configured to be outputs to follow local register settings. At power up, the GPIO are disabled and by default include a 35-k (typical) pulldown resistor. See *セクション 7.4.13* for programmability. Unused GPIO can be left open or no connect.
GPIO1	27		
GPIO2	26		
GPIO4	10		
GPIO5	9		
GPIO6	8		
GPIO3/INTB	25	I/O, OD	General-Purpose Input/Output: Pin GPIO3 can be configured to be input signals for GPOs on the Serializer. Pin 25 is shared with INTB. Pullup with 4.7 kΩ to $V_{(VDDIO)}$. The programmable input and output pin is an active-low open drain and controlled by the status registers. See *セクション 7.4.13* for programmability. Unused GPIO can be left open or no connect.
FPD-LINK III INTERFACE			
RIN0+	41	I/O	Receive Input Channel 0: Differential FPD-Link receiver and bidirectional control back channel output. The IO must be AC coupled. See *Design Requirements* for the correct AC-coupling capacitor values. If port is unused, leave NC and set RX_PORT_CTL register bit 0 = 0 to disable (see *セクション 7.4.6*).
RIN0–	42		
RIN1+	32	I/O	Receive Input Channel 1: Differential FPD-Link receiver and bidirectional control back channel output. The IO must be AC coupled. See *Design Requirements* for the correct AC-coupling capacitor values. If port is unused, leave NC and set RX_PORT_CTL register bit 1 = 0 to disable (see *セクション 7.4.6*).
RIN1–	33		
I2C PINS			
I2C_SCL	2	I/O, OD	I2C Serial Clock: Clock line for the bidirectional control bus communication. External 2-kΩ to 4.7-kΩ pullup resistor to 1.8-V or 3.3-V supply rail recommended per I2C interface standards. I2C_SCL and I2C_SDA inputs are 3.3-V tolerant. See *セクション 7.5.1* for more information.
I2C_SDA	1	I/O, OD	I2C Serial Data: Data line for bidirectional control bus communication. External 2-kΩ to 4.7-kΩ pullup resistor to 1.8-V or 3.3-V supply rail recommended per I2C interface standards. I2C_SCL and I2C_SDA inputs are 3.3-V tolerant. See *セクション 7.5.1* for more information.
CONFIGURATION AND CONTROL PINS			

表 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VDD_SEL	46	S, PD	VDD Select: Configuration pin to select internal LDO regulator supply. When VDD_SEL = LOW, internal 1.1-V supply mode is selected. Feed 1.8 V to VDD18 inputs = 1.8 V ±5%. An internal 1.1-V regulator will supply the VDD11. VDD11 inputs should be terminated with bypass capacitors. When VDD_SEL = HIGH, external 1.1-V supply mode is selected. After 1.8-V supply is applied to VDD18 inputs, then apply 1.1 V to VDD11 inputs = 1.1 V ±5%. **Voltage at VDD11 supply pins must always be less than main voltage applied to VDD18 when using external 1.1-V supply.**
IDX	35	S, PD	Input. I2C Serial Control Bus Primary Device ID Address Select. Once enabled the voltage at this pin will be sampled to configure the default I2C device address. Typically connected with external pullup resistor to VDD18 and pulldown resistor to GND to create a voltage divider. See *表 7-15*.
MODE	37	S, PD	Mode select configuration input to set operating mode based on input voltage level. Typically connected to voltage divider through external pullup to VDD18 and pulldown to GND. See 表 7-2.
PDB	30	I, PD	Power-down inverted Input Pin. Typically connected to processor GPIO with pull down. When PDB input is brought HIGH, the device is enabled and internal register and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power with CSI-2 Tx outputs in tri-state. The default function of this pin is PDB = LOW; POWER DOWN with internal 50 kΩ pull down enabled. PDB should remain low until after power supplies are applied and reach minimum required levels. **PDB INPUT IS 3.3-V TOLERANT**. See section *セクション 9.2*. PDB = 1.8 V, device is enabled (normal operation) PDB = 0, device is powered down.
DIAGNOSTIC PINS			
CMLOUTP	38	O	Monitor Loop-Through Driver differential output. Typically routed to test points and not connected. For monitoring, CMLOUT should be terminated with 100-Ω differential load. See *セクション 7.4.10*.
CMLOUTN	39		
BISTEN	6	S, PD	BIST Enable: BISTEN = H, BIST Mode is enabled BISTEN = L, BIST Mode is disabled. If unused connect BISTEN directly to GND. See BIST section *セクション 7.5.12* for more information.
PASS	47	O	PASS Output: PASS = H indicates pass conditions are met and PASS = L signals or more pass condition is not met. Typically route to processor input pin or test point for monitoring. May also be configured to indicate logical AND of pass status when both Rx ports are enabled. See *セクション 7.4.7* for more information. For BIST operation PASS = H, ERROR FREE Transmission in forward channel operation. PASS = L, one or more errors were detected in the received payload. See BIST section for more information. Leave No Connect if unused.
LOCK	48	O	LOCK Status: Output Pin for monitoring lock status of FPD-Link III channel, may be used as Link Status. LOCK = H, the FPD-Link III receiver is Locked and Rx Ports are active. LOCK = L, receiver is unlocked. May also be configured to indicate logical AND of lock status when both Rx ports are enabled. See *セクション 7.4.7* for more information. Leave No Connect if unused.
RES	44	PD	RES must be tied to GND for normal operation.
POWER AND GROUND			
VDDIO	7,29	P	VDDIO voltage supply input: The single-ended outputs and control input are powered from VDDIO. VDDIO can be connected to either a 1.8-V or 3.3-V supply rail. When VDDIO is connected to 1.8-V supply, VDDIO must be within ±100 mV of VDD18 to ensure output timing requirements are met. Each VDDIO pin requires a minimum 1-µF and 0.01-µF capacitor to GND.
VDD18_CSI	17	P	1.8-V (±5%) Power Supply. Requires 1-µF and 0.01-µF capacitors to GND.
VDD18_P0 VDD18_P1	45 36	P	1.8-V(±5%) Power Supplies. Requires 0.01-µF capacitors to GND at each VDD pin along with 10-µF bulk decoupling

表 5-1. Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VDD18_FPD0 VDD18_FPD1	40 31	P	1.8-V(±5%) Analog Power Supplies. Requires 10-µF, and 0.1-µF capacitors to GND at each VDD pin.
VDD11_FPD0	43	D, P	When VDD_SEL = LOW: **Do not connect to 1.1-V power rail** Requires 0.1 to 0.01-µF capacitor and a 4.7-µF capacitor to GND When VDD_SEL = HIGH: **Connect to external 1.1-V power rail** Requires a 0.01-µF capacitor to GND Requires a 10-µF capacitor to GND shared with VDD11_FPD1 See sections *Power Supply Recommendations* and *Typical Application* for more information
VDD11_FPD1	34	D, P	When VDD_SEL = LOW: **Do not connect to 1.1-V power rail** Requires a 0.1 to 0.01-µF capacitor and a 4.7-µF capacitor to GND When VDD_SEL = HIGH: **Connect to external 1.1-V power rail** Requires a 0.01-µF capacitor to GND Requires a 10-µF capacitor to GND shared with VDD11_FPD0
VDD11_CSI	20	D, P	When VDD_SEL = LOW: **Do not connect to 1.1-V power rail** Requires a 0.1 to 0.01-µF capacitor and a 4.7-µF capacitor to GND When VDD_SEL = HIGH: **Connect to external 1.1-V power rail** Requires a 0.01-µF capacitor and a 10-µF capacitor to GND
VDD11_D	3	D, P	When VDD_SEL = LOW: **Do not connect to 1.1-V power rail** Requires a 0.1 to 0.01-µF capacitor and a 4.7-µF capacitor to GND When VDD_SEL = HIGH: **Connect to external 1.1-V power rail** Requires a 0.01-µF capacitor and a 1-µF capacitor to GND
GND	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the QFN package. Connect to the ground plane (GND).

The definitions below define the functionality of the I/O cells for each pin. TYPE:

- I = Input
- O = Output
- I/O = Input/Output
- S = Configuration pin (All strap pins have internal pulldowns. If the default strap value is needed to be changed then use an external resistor.)
- PD = Internal pulldown
- OD = Open Drain
- P, G = Power supply, ground
- D = Decoupling pin for internal voltage rail

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Supply voltage	VDD18 (VDD18_CSI, VDD18_P1 , VDD18_P0 , VDD18_FPD0, VDD18_FPD1)		–0.3	2.16	V
	VDD11 (VDD11_CSI, VDD11_D , VDD11_FPD0, VDD11_FPD1)		–0.3	1.32 and < $V_{(VDD18)}$	V
	VDDIO		–0.3	3.96	V
FPD-Link III input voltage	RIN0+, RIN0–, RIN1+, RIN1–	Device powered up (VDD18, VDD11 and VDDIO within recommended operating conditions)	–0.3	2.75	V
		Device powered down (VDD18, VDD11 and VDDIO below recommended operating conditions) Transient Voltage	–0.3	1.45	V
		Device powered down (VDD18, VDD11 and VDDIO below recommended operating conditions) DC Voltage	–0.3	1.35	V
LVCMOS IO voltage	GPIO0, GPIO1, GPIO2, GPIOI4, GPIO5, GPIO6, XIN/REFCLK, VDD_SEL, XOUT, BISTEN, LOCK, PASS, CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLK1P/N, CSI_CLK0P/N		–0.3	$V_{(VDDIO)}$+ 0.3	V
	PDB		–0.3	3.96	V
Configuration input voltage	MODE, IDX		–0.3	$V_{(VDD18)}$+ 0.3	V
Open-drain voltage	GPIO3/INTB, I2C_SDA, I2C_SCL		–0.3	3.96	V
Junction temperature				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins except 32, 33, 41 and 42	±4500	V
			Pins 32, 33, 41 and 42	±8000	
		Charged device model (CDM), per AEC Q100-011		±1250	
		IEC 61000-4-2, powered-up only R_D = 330 Ω , C_S = 150 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1-)	±8000	
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1-	±18000	
		ISO 10605 R_D= 330 Ω, C_S= 150 pF and 330 pF R_D= 2 kΩ, C_S= 150 pF and 330 pF	Contact Discharge (RIN0+, RIN0-, RIN1+, RIN1-)	±8000	
			Air Discharge (RIN0+, RIN0-, RIN1+, RIN1-)	±18000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD18)}$	1.71	1.8	1.89	V
	$V_{(VDD11)}$ (VDD_SEL = HIGH ONLY)	1.045	1.1	1.155	V
Supply voltage offset	$V_{(VDD11)}$ - $V_{(VDDIO)}$, $V_{(VDDIO)}$ = 1.8V	-50		50	mV
LVCMOS supply voltage	$V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
	OR $V_{(VDDIO)}$ = 3.3 V	3	3.3	3.6	V
Open-drain voltage	GPIO3/INTB = $V_{(INTB)}$, I2C_SDA, I2C_SCL = $V_{(I2C)}$	1.71		3.6	V
Operating free-air temperature, T_A		–40	25	105	°C
MIPI data rate (per CSI-2 lane)		368		1664	Mbps
MIPI CSI-2 HS clock frequency		184		832	MHz
Reference clock oscillator frequency	REFCLK or XIN/XOUT	23		26	MHz
Spread-spectrum reference clock modulation percentage	Center Spread	-0.5		0.5	%
	Down Spread	-1		0	%
Local I^2C frequency, f_{I2C}				1	MHz
Supply noise(1)	$V_{(VDD11)}$			25	mV_{P-P}
	$V_{(VDD18)}$			50	mV_{P-P}
	$V_{(VDDIO)}$ = 1.8 V			50	mV_{P-P}
	$V_{(VDDIO)}$ = 3.3 V			100	mV_{P-P}
	RIN0+, RIN1+		10		mV_{P-P}

(1) DC-50 MHz

6.4 Thermal Information

THERMAL METRIC(1)		DS90UB936-Q1 RGC (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	15.7	°C/W
$R_{\theta JC(BOT)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W

(1) Thermal data in accordance with JESD51. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
TOTAL POWER CONSUMPTION							
P_T	Total power consumption for MIPI CSI-2 output mode, normal operation	2 x FPD-Link III Input, CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL = LOW, default registers	$V_{(VDD18)}$= 1.89 V, $V_{(VDDIO)}$ = 3.6 V		473	564	mW
		2 x FPD-Link III Input, CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL = HIGH, default registers	$V_{(VDD18)}$= 1.89 V, $V_{(VDD11)}$ = 1.155 V $V_{(VDDIO)}$ = 3.6 V			450	mW
DESERIALIZER SUPPLY CURRENT - FPD-Link III Rx Port0 AND Rx Port1 PAIRED WITH 2x DS90UB935							
$I_{DD-R2T4}$	Deserializer supply current 2 Rx 4 Tx	2 x FPD-Link III Input, CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL=LOW, default registers, includes CSI-2 load current	VDD18		240	279	mA
			VDDIO		5	10	
		2 x FPD-Link III Input, CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL=HIGH, default registers, includes CSI-2 load current	VDD18		110	140	mA
			VDD11		100	130	
			VDDIO		5	10	
$I_{DD-R2T22}$	Deserializer supply current 2 Rx 2x2 Tx	2 x FPD-Link III Input, Replicate mode, CSI-2 = 2x 2 DATA lanes and 2x 1 CLK lanes VDD_SEL=LOW, includes CSI-2 load current	VDD18		240	279	mA
			VDDIO		5	10	
		2 x FPD-Link III Input, Replicate mode, CSI-2 = 2x 2 DATA lanes and 2x 1 CLK lanes VDD_SEL=HIGH , includes CSI-2 load current	VDD18		110	140	mA
			VDD11		100	130	
			VDDIO		5	10	
DESERIALIZER SUPPLY CURRENT - FPD-Link III Rx Port0 OR Rx Port1 PAIRED WITH 1x DS90UB935							
$I_{DD-R1T4}$	Deserializer supply current 1 Rx 4 Tx	1 x FPD-Link III Input, CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL=LOW, default registers, includes CSI-2 load current	VDD18		170	188	mA
			VDDIO		5	10	
		1 x FPD-Link III Input, CSI2 = 4 DATA lanes + 1 CLK lane VDD_SEL=HIGH, default registers, includes CSI-2 load current	VDD18		65	80	mA
			VDD11		80	100	
			VDDIO		5	10	
DESERIALIZER SUPPLY CURRENT - FPD-Link III Rx Port0 AND Rx Port1 PAIRED WITH 2x DS90UB933							
$I_{DD2-R2T4}$	Deserializer supply current 2G 2 Rx 4 Tx	2 x FPD-Link III Input, FPD-Link III line-rate = 1.867 Gbps per Rx port CSI-2 = 4 DATA lanes + 1 CLK lanes VDD_SEL=LOW, includes CSI-2 load current	VDD18		220	265	mA
			VDDIO		5	10	
		2 x FPD-Link III Input, FPD-Link III line-rate = 1.867 Gbps per Rx port CSI-2 = 4 DATA lanes + 1 CLK lanes VDD_SEL=HIGH, includes CSI-2 load current	VDD18		110	148	mA
			VDD11		85	100	
			VDDIO		5	10	
DESERIALIZER SUPPLY CURRENT - FPD-Link III Rx Port0 OR Rx Port1 PAIRED WITH 1x DS90UB933							

6.5 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$I_{DD2-R1T4}$	Deserializer supply current 2G 1 Rx 4 Tx	1 x FPD-Link III Input, FPD-Link III line-rate = 1.867 Gbps CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL=LOW, includes CSI-2 load current		VDD18		150	205	mA
				VDDIO		5	10	
		1 x FPD-Link III Input, FPD-Link III line-rate = 1.867 Gbps CSI-2 = 4 DATA lanes + 1 CLK lane VDD_SEL=HIGH, includes CSI-2 load current		VDD18		65	86	mA
				VDD11		75	110	
				VDDIO		5	10	
DESERIALIZER SUPPLY CURRENT - Power Down								
I_{DDZ}	Deserializer shutdown current	PDB = HIGH to LOW, VDD_SEL = LOW		VDD18		82	115	mA
				VDIO		2.5	5	
		PDB = HIGH to LOW, VDD_SEL = HIGH		VDD18		10	15	
				VDD11		30	110	
				VDDIO		2.5	5	
1.8-V LVCMOS I/O								
V_{OH}	High level output voltage	I_{OH} = –2 mA, $V_{(VDDIO)}$ = 1.71 to 1.89 V; $V_{(VDDIO)}$ = VDD18 ±50 mV		GPIO[6:4], GPIO[2:0], LOCK, PASS	$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 2 mA, $V_{(VDDIO)}$ = 1.71 to 1.89 V; $V_{(VDDIO)}$ = VDD18 ±50 mV		GPIO[6:0], LOCK, PASS	GND		0.45	V
V_{IH}	High level input voltage	$V_{(VDDIO)}$ = 1.71 to 1.89 V; $V_{(VDDIO)}$ = VDD18 ±50 mV		GPIO[6:0], BISTEN	0.65 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
		$V_{(VDDIO)}$ = 1.71 to 1.89 V; $V_{(VDDIO)}$ = VDD18 ±50 mV		PDB, VDD_SEL	1.17		$V_{(VDDIO)}$	V
		$V_{(VDDIO)}$ = 1.71 to 1.89 V; $V_{(VDDIO)}$ = VDD18 ±50 mV		XIN/REFCLK	1.15		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage	$V_{(VDDIO)}$ = 1.71 to 1.89V; $V_{(VDDIO)}$ = VDD18 ±50 mV		GPIO[6:0], BISTEN	GND		0.35 × $V_{(VDDIO)}$	V
		$V_{(VDDIO)}$ = 1.71 to 1.89V; V(VDDIO) = VDD18 ±50 mV		PDB, VDD_SEL	GND		0.63	V
		$V_{(VDDIO)}$ = 1.71 to 1.89V; V(VDDIO) = VDD18 ±50 mV		XIN/REFCLK	GND		0.7	V
I_{IH}	Input high current	VIN = $V_{(VDDIO)}$ = 1.71 to 1.89 V,	Internal pulldown enabled	GPIO[6:0], BISTEN, PDB	–100		100	µA
I_{IH}	Input high current	VIN = $V_{(VDDIO)}$ = 1.71 to 1.89 V,	Internal pulldown disabled	GPIO[6:0], XIN/REFCLK, VDD_SEL	–20		30	µA
I_{IL}	Input low current	V_{IN} = 0V		GPIO[6:0], PDB, XIN/REFCLK, VDD_SEL, BISTEN	–20		30	µA
I_{OS}	Output short circuit current	V_{OUT} = 0 V	V_{OUT} = 0 V			–25		mA
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L	V_{OUT} = 0 V or V_{DDIO}, PDB = L		–25		25	µA
3.3-V LVCMOS I/O								
V_{OH}	High level output voltage	I_{OH} = –4 mA, $V_{(VDDIO)}$ = 3.0 to 3.6 V		GPIO[6:4], GPIO[2:0], LOCK, PASS	2.4		$V_{(VDDIO)}$	V

6.5 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	I_{OL} = 4 mA, $V_{(VDDIO)}$ = 3.0 to 3.6 V	GPIO[6:0], LOCK, PASS	GND		0.4	V
V_{IH}	High level input voltage	$V_{(VDDIO)}$ = 3 to 3.6 V	GPIO[6:0], BISTEN	2		$V_{(VDDIO)}$	V
		$V_{(VDDIO)}$ = 3 to 3.6 V	PDB, VDD_SEL	1.17		$V_{(VDDIO)}$	V
		$V_{(VDDIO)}$ = 3 to 3.6 V	XIN/REFCLK	1.15		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage	$V_{(VDDIO)}$ = 3 to 3.6 V	GPIO[6:0], BISTEN	GND		0.8	V
		$V_{(VDDIO)}$ = 3 to 3.6 V	PDB, VDD_SEL	GND		0.63	V
		$V_{(VDDIO)}$ = 3 to 3.6 V	XIN/REFCLK	GND		0.7	V
I_{IH}	Input high current	V_{IN} = 3 to 3.6 V, internal pulldown enabled	GPIO[6:0], BISTEN, PDB	–190		190	µA
		V_{IN} = 3 to 3.6 V, internal pulldown disabled	GPIO[6:0], XIN/ REFCLK, VDD_SEL	–20		30	µA
I_{IL}	Input low current	V_{IN} = 0 V	GPIO[6:0], PDB, XIN/REFCLK, VDD_SEL, BISTEN	–20		30	µA
I_{OS}	Output short circuit current	V_{OUT} = 0 V	GPIO[7:0], LOCK, PASS		–40		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or $V_{(VDDIO)}$, PDB = L	GPIO[7:0], LOCK, PASS	–25		35	µA
SERIAL CONTROL BUS[1]							
V_{IH}	Input high level		I2C_SDA, I2C_SCL	0.7 × $V_{(I2C)}$		$V_{(I2C)}$	V
V_{IL}	Input low level			GND		0.3 × $V_{(I2C)}$	V
V_{HY}	Input hysteresis				50		mV
V_{OL}	Output low level	Standard-mode/Fast-mode I_{OL} = 3 mA		0		0.4	V
		Fast-mode Plus I_{OL} = 20 mA		0		0.4	V
I_{IH}	Input high current	V_{IN} = $V_{(I2C)}$		–10		10	µA
I_{IL}	Input low current	V_{IN} = 0V		–10		10	µA
C_{IN}	Input capacitance				5		pF
FPD-LINK III INPUT							
V_{CM}	Common mode voltage		RIN0+, RIN0- RIN1+, RIN1-		1.2		V
R_T	Internal termination resistor	Single-ended	RIN0+, RIN1+	40	50	60	Ω
		Differential	RIN0+, RIN0- RIN1+, RIN1-	80	100	120	Ω
FPD-LINK III BIDIRECTIONAL CONTROL CHANNEL							
V_{OUT-BC}	Back Channel Output Single-ended voltage	RL = 50 Ω, coaxial configuration, forward channel disabled	RIN0+, RIN0- RIN1+, RIN1-	190	225	260	mV
V_{OD-BC}	Back channel output differential	RL = 100 Ω, STP configuration, forward channel disabled		380	450	520	mV
HSTX DRIVER							

6.5 DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
V_{CMTX}	HS transmit static common-mode voltage		CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLK1P/N, CSI_CLK0P/N	150	200	250	mV
$\lvert \Delta V_{CMTX(1,0)} \rvert$	VCMTX mismatch when output is 1 or 0					5	mV_{P-P}
$\lvert V_{OD} \rvert$	HS transmit differential voltage			140	200	270	mV
$\lvert \Delta V_{OD} \rvert$	VOD mismatch when output is 1 or 0					14	mV
V_{OHHS}	HS output high voltage					360	mV
Z_{OS}	Single-ended output impedance			40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single-ended output impedance					10	%
LPTX DRIVER							
V_{OH}	High level output voltage	Applicable when the supported data rate is ≤ 1.5 Gbps	CSI_D3P/N, CSI_D2P/N, CSI_D1P/N, CSI_D0P/N, CSI_CLK1P/N, CSI_CLK0P/N	1.1	1.2	1.3	V
		Applicable when the supported data rate is > 1.5 Gbps		0.95		1.3	V
V_{OL}	Low level output voltage			-50		50	mV
Z_{OLP}	Output impedance			110			Ω

(1) $V_{(VDDIO)}$ = 1.8 V ± 5% **OR** 3.3 V ± 10%

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
LVCMOS I/O							
t_{CLH}	LVCMOS low-to-high transition time	$V_{(VDDIO)}$ = 1.71 to 1.89 V = VDD18 ±50 mV OR $V_{(VDDIO)}$ = 3V to 3.6 V, C_L = 8pF	GPIO[6:0]		2.5		ns
t_{CHL}	LVCMOS high-to-low transition time				2.5		ns
t_{PDB}	PDB reset pulse width	Voltage supplies applied and stable	PDB	2			ms
FPD-LINK III RECEIVER INPUT							
V_{IN}	Single ended input voltage	Coaxial configuration, attenuation = 20dB @ 2.1 GHz	RIN0+, RIN1+	40			mV
V_{ID}	Differential input voltage	STP configuration, attenuation = 25dB @ 2.1 GHz	RIN0+, RIN0-, RIN1+, RIN1-	80			mV

6.6 AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
t_{DDLT}	Deserializer data lock time	CSI mode paired with DS90UB935-Q1, coaxial cable, attenuation = 20 dB @ 2.1GHz	AEQ full range 0x00 to 0x3F, SFILTER_CFG = 0xA9		20	300	ms
t_{DDLT}			AEQ range +/- 3, SFILTER_CFG = 0xA9		15	30	ms
t_{DDLT}		RAW mode paired with DS90UB933-Q1, coaxial cable, attenuation = 14 dB @ 1.2 GHz	AEQ full range 0x00 to 0x3F, SFILTER_CFG = 0xA9		15	200	ms
t_{DDLT}			AEQ range +/- 3, SFILTER_CFG = 0xA9		15	30	ms
t_{IJIT}	Input Jitter	CSI-2 mode paired with DS90UB935-Q1, coaxial configuration (attenuation = 20 dB) or STP configuration (attenuation = 25 dB) @ 2.1 GHz	Jitter Frequency > FPD3_PLCK/15			0.4	UI
FPD-LINK III BI-DIRECTIONAL CONTROL CHANNEL							
E_{H-BC}	Back channel output eye height	Coaxial configuration, f_{BC} = 52 MHz	RIN0+, RIN1+	130	160		mV
		STP configuration, f_{BC} = 52 MHz	RIN0+, RIN0-, RIN1+, RIN1-	260	320		mV
E_{W-BC}	Back channel output eye width	Coaxial or STP configuration, f_{BC} = 52 MHz	RIN0+, RIN0-, RIN1+, RIN1-	0.7	0.8		UI
f_{BC}	Back channel datarate(1)	Synchronous CSI-2 input mode, default register settings	Signal applied to REFCLK input		2× REFCLK		Mbps
			No signal present at REFCLK input	46		56	Mbps

(1) The backchannel data rate (Mbps) listed is for the encoded back channel data stream. The internal reference frequency used to generate the encoded back channel data stream is two times the back channel datarate.

6.7 AC Electrical Characteristics CSI-2

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
HSTX DRIVER AC SPECIFICATIONS							
$HSTX_{DBR}$	Data bit rate	REFCLK = 23 MHz	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	368	736	1472	Mbps
		REFCLK = 25 MHz		400	800	1600	Mbps
		REFCLK = 26 MHz		416	832	1664	Mbps

6.7 AC Electrical Characteristics CSI-2 (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
f_{CLK}	DDR clock frequency	REFCLK = 23 MHz		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	184	368	736	MHz
		REFCLK = 25 MHz			200	400	800	MHz
		REFCLK = 26 MHz			208	416	832	MHz
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF	Common-level variations above 450MHz		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF	Common-level variations between 50 and 450MHz					25	mV_{RMS}
t_{RHS} t_{FHS}	20% to 80% rise and fall HS	HS bit rates ≤ 1 Gbps (UI ≥ 1 ns)		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N			0.3	UI
		HS bit rates > 1 Gbps (UI					0.35	UI
		Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps			100			ps
		Applicable for all HS bit rates when supporting > 1.5 Gbps					0.4	UI
		Applicable for all HS bit rates when supporting > 1.5 Gbps. However, to avoid excessive radiation, bit rates ≤ 1.5 Gbps should not use values below 100 ps and bit rates ≤ 1 Gbps should not use values below 150 ps.			50			ps
SDD_{TX}	TX differential return loss	f_{LPMAX}		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N		–18		dB
		f_H	HSData rates < 1.5 Gbps			–9		dB
			HSData rates > 1.5 Gbps			-4.5		dB
		f_{MAX}	HSData rates < 1.5 Gbps			–-3		dB
			HSData rates > 1.5 Gbps			–-2.5		dB
SCC_{TX}	TX common mode return loss	f_{LPMAX}		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N		–20		dB
		f_H				–15		dB
		f_{MAX}				–9		dB
LPTX DRIVER AC SPECIFICATIONS								

6.7 AC Electrical Characteristics CSI-2 (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
t_{RLP}	Rise time LP	15% to 85% rise time	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N			25	ns
t_{FLP}	Fall time LP	15% to 85% fall time				25	ns
t_{REOT}	Rise time post-EoT	30%-85% rise time				35	ns
$t_{LP\text{-}PULSE\text{-}TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	40			ns
		All other pulses		20			ns
$t_{LP\text{-}PER\text{-}TX}$	Pulse width of the LP exclusive-OR clock			90			ns
DV/DtSR	Slew rate	CLoad = 0pF	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N			500	mV/ns
		CLoad = 5pF				300	mV/ns
		CLoad = 20pF				250	mV/ns
		CLoad = 70pF				150	mV/ns
		CLoad = 0 to 70pF (Falling Edge Only) Data rate < 1.5 Gbps		30			mV/ns
		CLoad = 0 to 70pF (Rising Edge Only) Data rate < 1.5 Gbps		30			mV/ns
		CLoad = 0 to 70pF (Falling Edge Only) Data rate > 1.5 Gbps		25			mV/ns
		CLoad = 0 to 70pF (Rising Edge Only) Data rate > 1.5 Gbps		25			mV/ns
		CLoad = 0 to 70pF (Rising Edge Only) Applicable when the supported Data rate is < 1.5 Gbps		0 - 0.075 × ($V_{O,INST}$ - 700)			mV/ns
		CLoad = 0 to 70pF (Rising Edge Only) Applicable when the supported Data rate is > 1.5 Gbps		25 - 0.0625 × ($V_{O,INST}$ - 550)			mV/ns
CLOAD	Load capacitance		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	0		50	pF
DATA-CLOCK TIMING SPECIFICATIONS							
UI_{INST}	UI instantaneous	In 1, 2, 3, or 4 Lane Configuration	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	0.6		2.7	ns
ΔUI	UI variation	UI ≥ 1ns		-10%		10%	UI
		0.667ns ≤ UI		-5%		5%	UI

6.7 AC Electrical Characteristics CSI-2 (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{SKEW(TX)}$	Data to Clock Skew (measured at transmitter) Skew between clock and data from ideal center	Data rate ≤ 1 Gbps	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	-0.15		0.15	UI_{INST}
		Data rate: 1 Gbps to 1.5 Gbps		-0.2		0.2	UI_{INST}
$t_{SKEW(TX)STATIC}$	Static Data to Clock Skew (TX)	Data rate > 1.5 Gbps	CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	-0.2		0.2	UI_{INST}
$t_{SKEW(TX)DYNAMIC}$	Dynamic Data to Clock Skew (TX)			-0.15		0.15	UI_{INST}
ISI	Channel ISI					0.2	UI_{INST}
CSI-2 TIMING SPECIFICATIONS							
$t_{CLK-MISS}$	Timeout for receiver to detect absence of clock transitions and disable the clock lane HS-RX		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	60			ns
$t_{CLK-POST}$	HS exit			60 + 52×UI			ns
$t_{CLK-PRE}$	Time HS clock shall be driver prior to any associated data lane beginning the transition from LP to HS mode			8			UI
$t_{CLK-PREPARE}$	Clock lane HS entry			38		95	ns
$t_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any clock lane HS transitions			95		300	ns
$t_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS termination			Time for Dn to reach VTERM-EN		38	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst			60			ns
$t_{CLK-PREPARE} + t_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the clock			300			ns

6.7 AC Electrical Characteristics CSI-2 (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN OR FREQUENCY	MIN	TYP	MAX	UNIT
$t_{D-TERM-EN}$	Time for the data lane receiver to enable the HS line termination		CSI_D0P/N, CSI_D1P/N, CSI_D2P/N, CSI_D3P/N, CSI_CLK0P/N, CSI_CLK1P/N	Time for Dn to reach $V_{TERM-EN}$		35 + 4×UI	ns
t_{EOT}	Transmitted time interval from the start of tHS-TRAIL to the start of the LP-11 state following a HS burst					105 + 12×UI	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst			100			ns
$t_{HS-PREPARE}$	Data lane HS entry			40 + 4×UI		85 + 6×UI	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence			145 + 10×UI			ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any data lane HS transitions, starting from the beginning of tHS-SETTLE			85 + 6×UI		145 + 10×UI	ns
$t_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.			40		55 + 4×UI	ns
$t_{HS-TRAIL}$	Data lane HS exit			60 + 4×UI			ns
t_{LPX}	Transmitted length of LP state			50			ns
t_{WAKEUP}	Recovery Time from Ultra Low Power State (ULPS)			1			ms
t_{INIT}	Initialization period			100			µs

6.8 Recommended Timing for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode Plus	>0		1	MHz
t_{LOW}	SCL Low Period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL High Period	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs

6.8 Recommended Timing for the Serial Control Bus (continued)

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
$t_{SU;STA}$	Set up time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data set up time	Standard-mode	250			ns
		Fast -mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Set up time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL & SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL & SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
$t_{VD:DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD;ACK}$	Data vallid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

6.9 Timing Diagrams

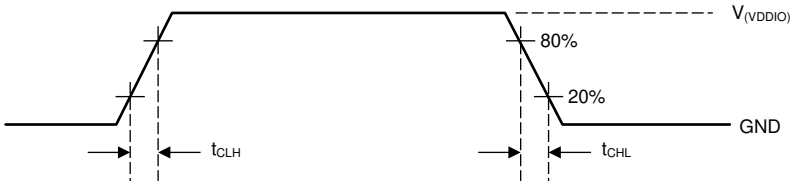


図 6-1. LVCMOS Transition Times

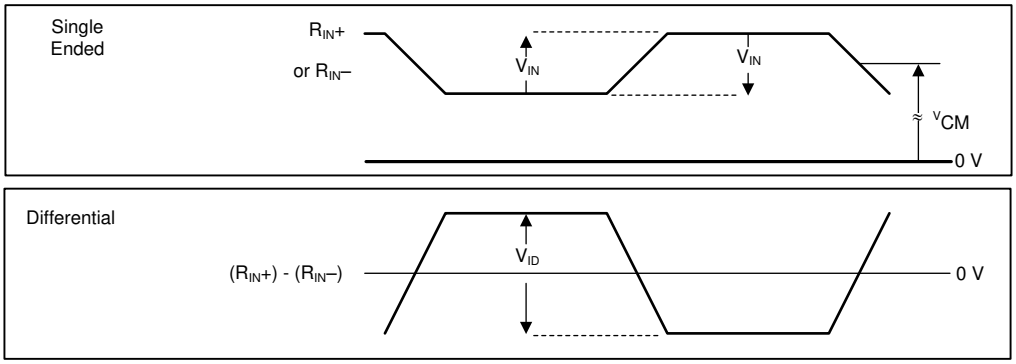


図 6-2. FPD-Link III Receiver V_{ID}, V_{IN}, V_{CM}

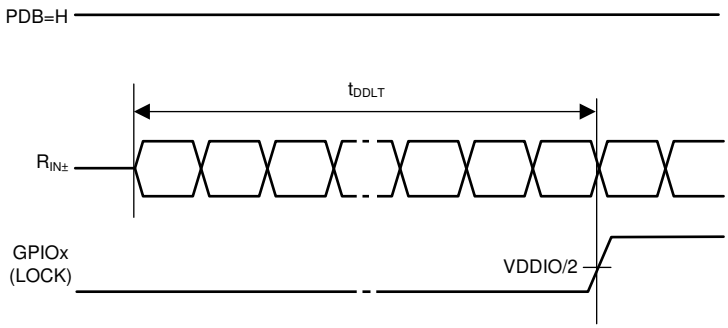


図 6-3. Deserializer Data Lock Time

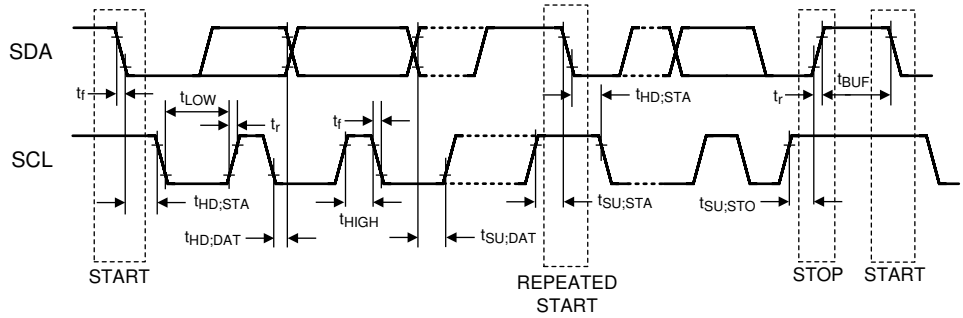


図 6-4. I2C Serial Control Bus Timing

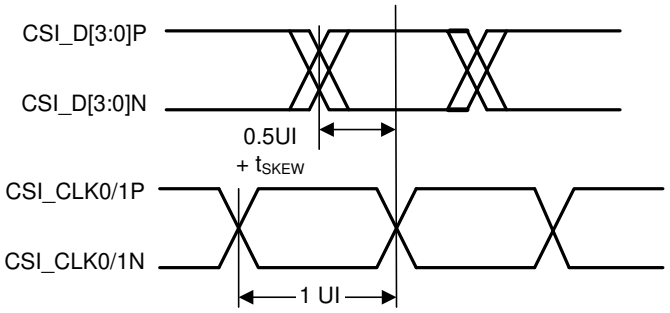


図 6-5. Clock and Data Timing in HS Transmission

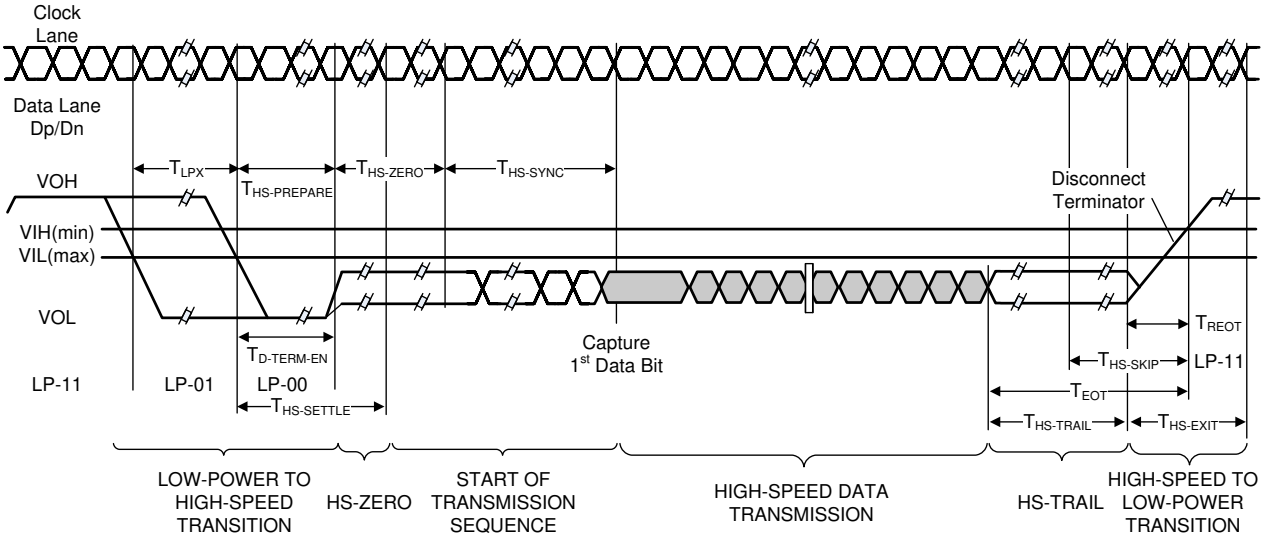


図 6-6. High-Speed Data Transmission Burst

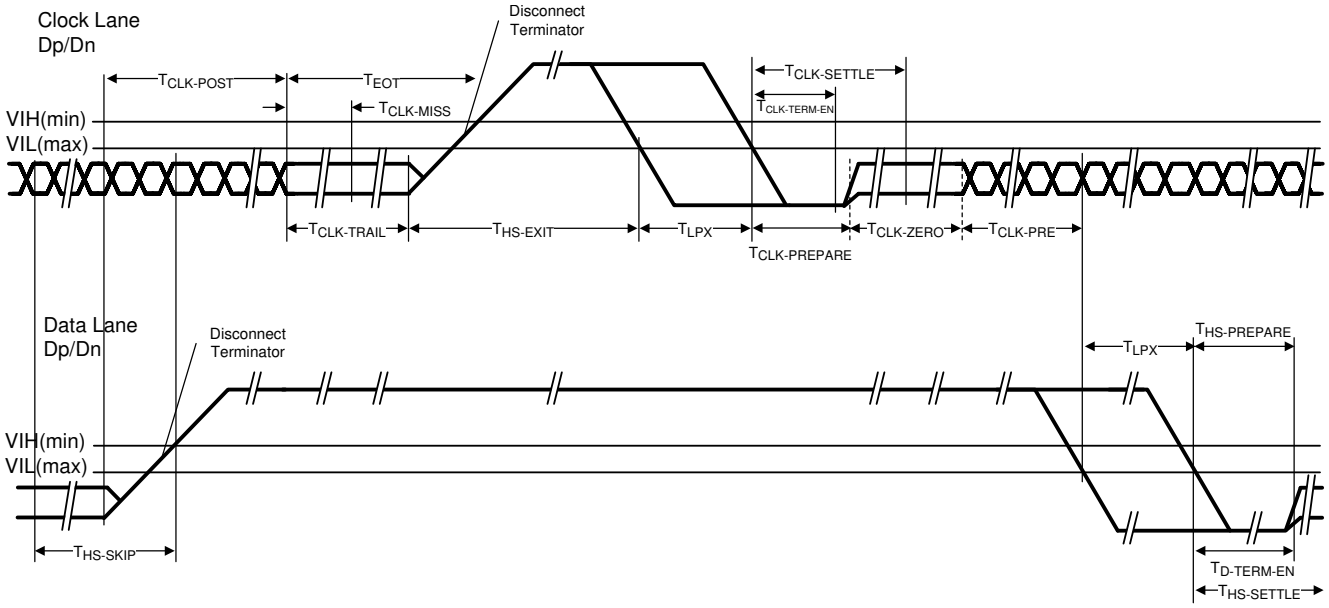


図 6-7. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

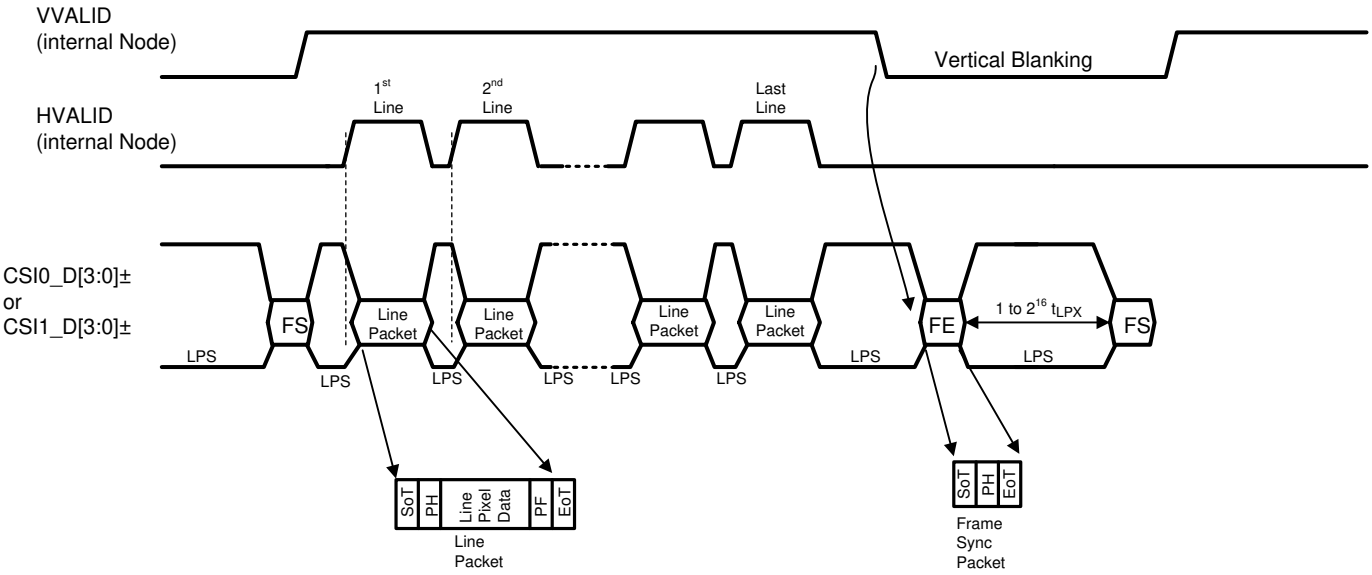


図 6-8. Long Line Packets and Short Frame Sync Packets

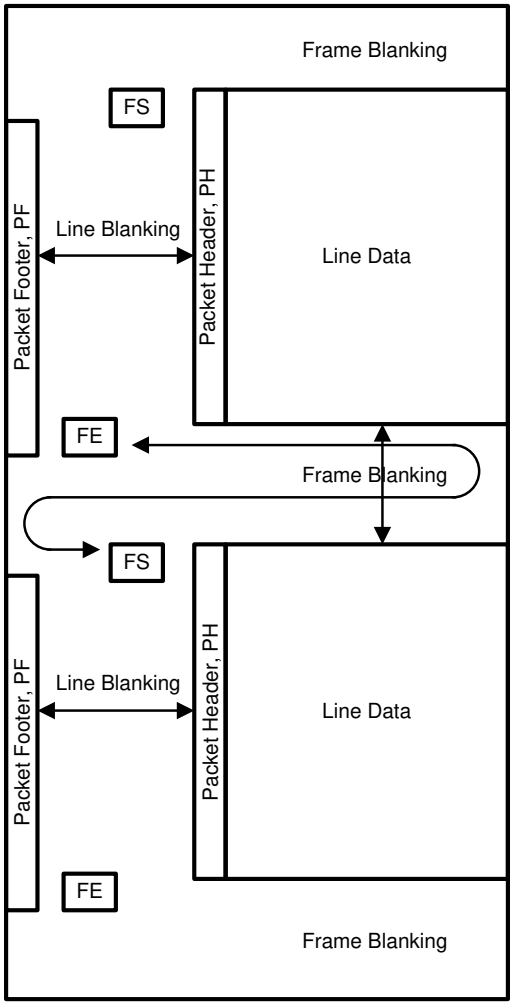
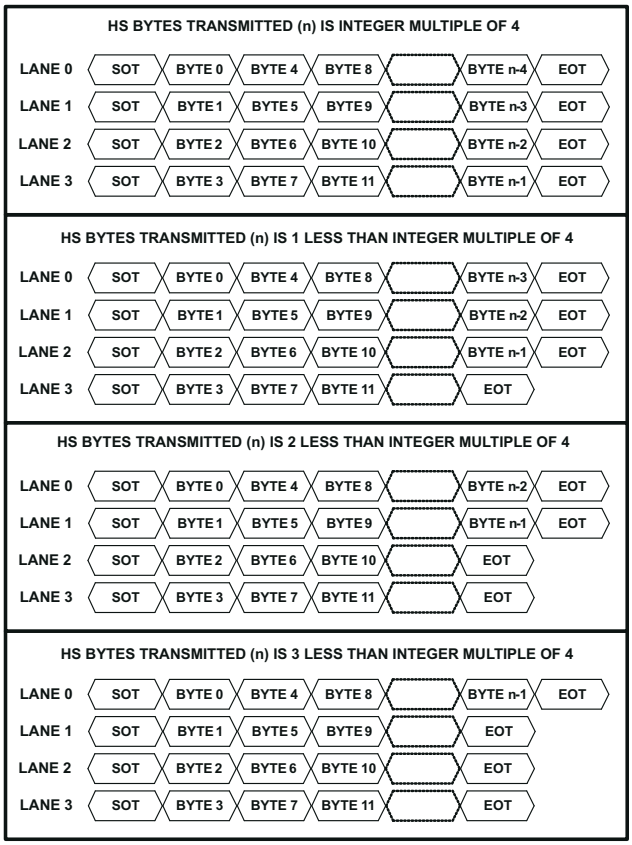
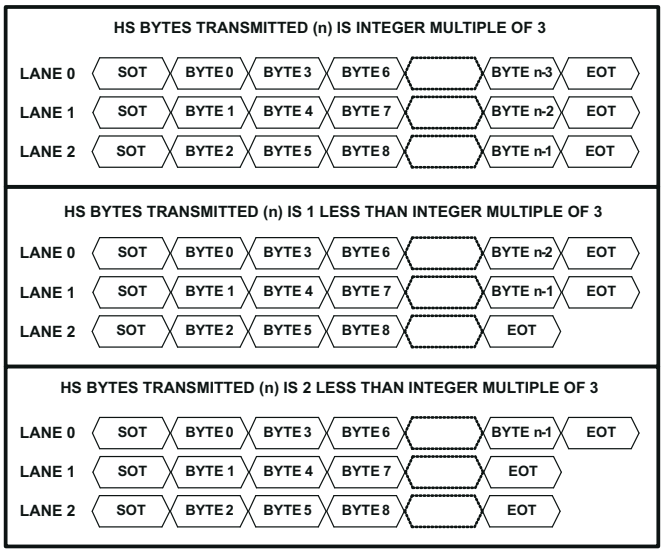


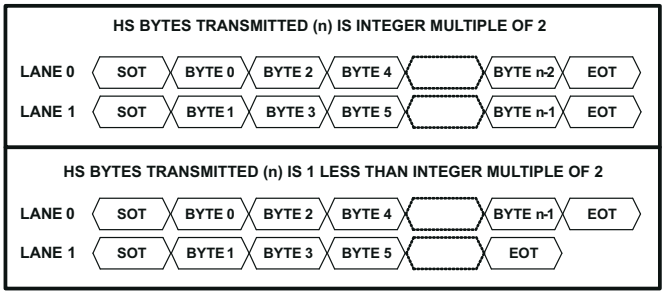
図 6-9. CSI-2 General Frame Format



4 CSI-2 Data Lane Configuration (default)



3 CSI-2 Data Lane Configuration



2 CSI-2 Data Lane Configuration

図 6-10. MIPI CSI-2 Data Lane Configuration

6.10 Typical Characteristics

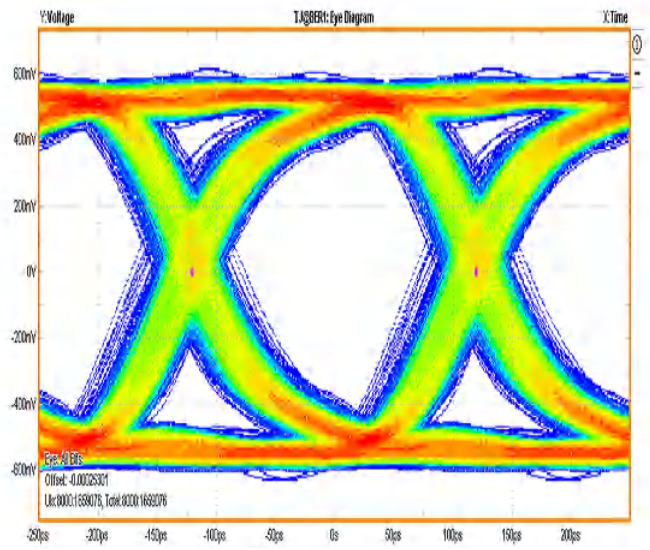


図 6-11. Forward Channel Monitor Loop Through Typical Rx Waveform (CMLOUT)

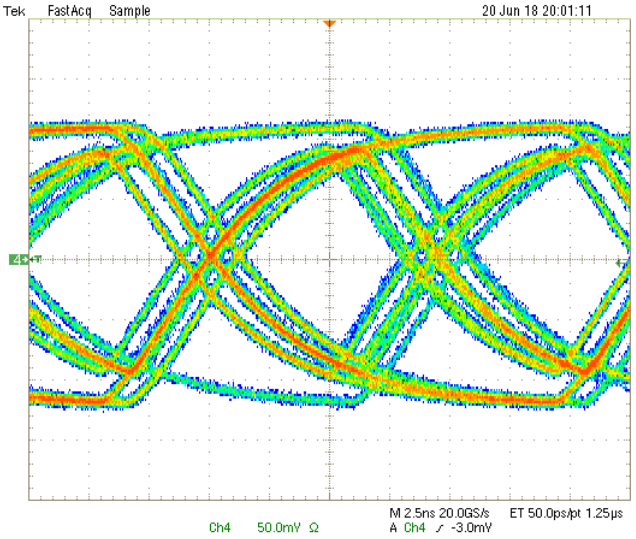


図 6-12. Back Channel Output Typical Waveform

7 Detailed Description

7.1 Overview

The DS90UB936-Q1 is a versatile deserializer that aggregates up to two inputs acquired from a FPD-Link III stream and transmits the received data over a MIPI camera serial interface (CSI-2). When coupled with an ADAS FPD-Link III serializer (DS90UB935-Q1, DS90UB933-Q1 or DS90UB913A-Q1), the DS90UB936-Q1 receives data streams from multiple sensors to be multiplexed on the same CSI-2 links.

表 7-1. Serializer Compatibility

Serializer	DS90UB935-Q1	DS90UB953-Q1	DS90UB933-Q1	DS90UB913A-Q1
Compatibility	Yes	No	Yes	Yes

7.1.1 Functional Description

The DS90UB936-Q1 FPD-Link III Deserializer, in conjunction with an ADAS FPD-Link III serializer supports the video transport needs with an ultra-high speed forward channel and an embedded bidirectional control channel. The DS90UB936-Q1 received data is output from a configurable MIPI CSI-2 port. The CSI-2 port may be configured as either a single CSI-2 output with four lanes up to 1.662 Gbps per lane or as two 2 lane CSI-2 outputs for sending replicated data on both ports. A second differential clock is available for the second replicated output when configured for dual CSI-2 outputs supporting one clock lane and one or two data lanes each. The DS90UB936-Q1 can support multiple data formats and different resolutions as provided by the sensor. Conversion between different data formats is not supported. The CSI-2 Tx module accommodates both image data and non-image data (including synchronization or embedded data packets).

The DS90UB936-Q1 CSI-2 interface combines each of the sensor data streams into packets designated for each virtual channel. The output generated is composed of virtual channels to separate different streams to be interleaved. Each virtual channel is identified by a unique channel identification number in the packet header.

When the DS90UB936-Q1 is paired with a DS90UB935-Q1 serializer, the received FPD-Link III forward channel is constructed in 40-bit long frames. Each encoded frame contains video payload data, I2C forward channel data, and additional information on framing, data integrity and link diagnostics. The high-speed, serial bit stream from the DS90UB935-Q1 contains an embedded clock and DC-balancing ensuring sufficient data line transitions for enhanced signal quality. When paired with ADAS serializers in RAW input mode, the received FPD-Link III forward channel is similarly constructed at a lower line rate in 28-bit long frames. The DS90UB936-Q1 device recovers a high-speed, FPD-Link III forward channel signal and generates a bidirectional control channel control signal in the reverse channel direction. The DS90UB936-Q1 converts the FPD-Link III stream into a MIPI CSI-2 output interface designed to support automotive sensors, including image sensors supplying up to 2.5-Gbps CSI-2 data.

The DS90UB936-Q1 device has two receive input ports to accept up to two sensor streams simultaneously. The control channel function of the DS90UB93x-Q1 chipset provides bidirectional communication between the image sensors and ECU. The integrated bidirectional control channel transfers data bidirectionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bidirectional control channel bus is controlled through an I2C port. The bidirectional control channel offers continuous low latency communication and is not dependent on video blanking intervals. The DS90UB935-Q1/936-Q1 chipset can operate entirely off of the back channel frequency clock generated by the DS90UB936-Q1 and recovered by the DS90UB935-Q1. The DS90UB935-Q1 provides the reference clock source for the sensor based on the recovered back channel clock. Synchronous clocking mode provides distinct advantages in a multi-sensor system by locking all of the sensors and the receiver to a common reference in the same clock domain, which reduces or eliminates the need for data buffering and re-synchronization. This mode also eliminates the cost, space, and potential failure point of a reference oscillator within the sensor. The DS90UB93x-Q1 chipset offer customers the choice to work with different clocking schemes. The DS90UB93x-Q1 chipset can also use an external oscillator as the reference clock source for the PLL as the primary reference clock to the serializer (see the DS90UB935-Q1 data sheet).

7.2 Functional Block Diagram

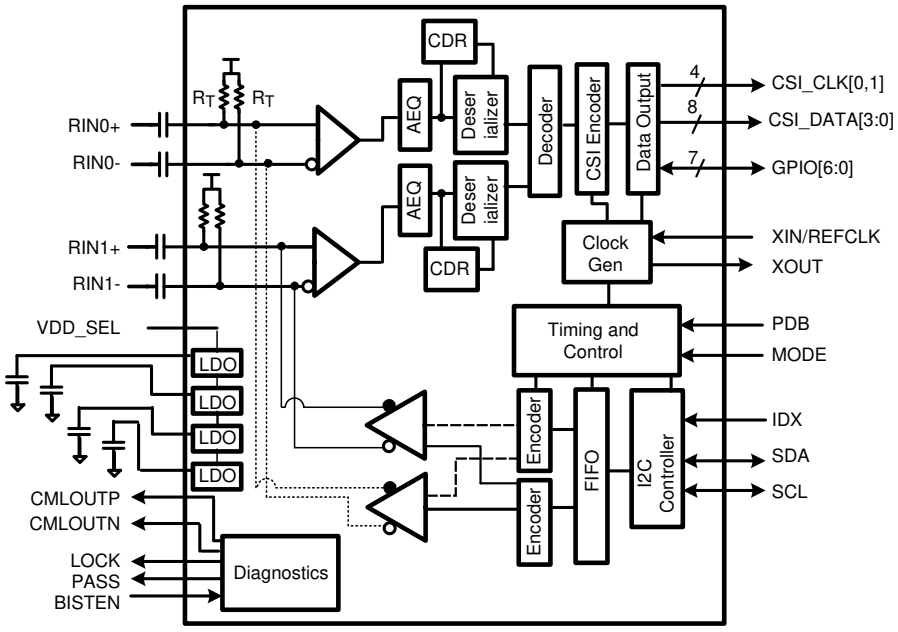


図 7-1. Functional Block Diagram

7.3 Feature Description

The DS90UB936-Q1 provides a flexible deserializer for automotive sensor applications. The device includes two FPD-Link III inputs for sensor data streams from one or two DS90UB935-Q1 serializers. The FPD-Link III interface is also compatible with DS90UB933-Q1 and DS90UB913A-Q1 ADAS serializers. Data received from the two input ports is aggregated onto a CSI-2 TX output with up to 4 data lanes.

7.4 Device Functional Modes

The DS90UB936-Q1 operating modes:

- CSI-2 Mode (DS90UB935-Q1 compatible)
- RAW Mode (DS90UB913A-Q1 and DS90UB933-Q1 compatible)

The two modes control the FPD-Link III receiver operation of the device. In cases, the output format for the device is CSI-2 through the CSI-2 transmit port.

Each input port can be individually configured for CSI-2 or RAW modes of operation.

The input mode of operation is controlled by the FPD3_MODE (Register 0x6D[1:0]) setting in the Port Configuration register. The input mode may also be controlled by the MODE strap pin.

7.4.1 CSI-2 Mode

When operating in CSI-2 FPD-Link III input mode (with DS90UB935-Q1), the DS90UB936-Q1 receives CSI-2 formatted data on one or two FPD-Link III input ports and forwards the data to the CSI-2 transmit port. The deserializer can operate in CSI-2 mode with synchronous back channel reference or non-synchronous mode. The forward channel line rate is independent of the CSI-2 rate in synchronous or non-synchronous with external clock mode, with the DS90UB936-Q1 supporting up to 2.5 Gbps CSI-2 throughput per link. Each CSI-2 mode supports remapping of Virtual Channel IDs at the input of each receive port. This allows handling of conflicting VC-IDs for input streams from dual sensors and sending those streams to the same CSI-2 transmit port.

In CSI-2 mode each deserializer Rx Port can support an FPD-Link line rate up to 4.16 Gbps, where the forward channel and back channel rates are based on the reference frequency used for the serializer:

- In Synchronous mode based on REFCLK input frequency reference, the FPD-Link line rate is a fixed value of 160 × REFCLK. FPD3_PCLK = 4 × REFCLK and Back channel rate = 2 × REFCLK. For example with REFCLK = 25 MHz, line rate = 4.0 Gbps, FPD3_PCLK = 100 MHz, back channel data rate = 50 Mbps.
- In Non-synchronous clocking mode when the DS90UB935-Q1 uses external reference clock (f_{CLKIN}) the FPD-Link line rate is typically f_{CLKIN} × 80, FPD3_PCLK = 2 × f_{CLKIN} or 1 x f_{CLKIN} and back channel data rate is set to 10 Mbps. For example, with f_{CLKIN} = 50 MHz, line rate = 4Gbps, FPD3_PCLK = 100 MHz, and the back channel rate is 10 Mbps. The sensor CSI-2 rate is independent of the f_{CLKIN}.

7.4.2 RAW Mode

When operating in Raw FPD-Link III input mode, the DS90UB936-Q1 receives RAW10 or RAW12 data from a DS90UB913A-Q1 or DS90UB933-Q1 serializer. The data is translated into a RAW10 or RAW12 CSI-2 video stream for forwarding to the CSI-2 transmit port. For each input port, the CSI-2 packet header VC-ID and Data Type are programmable.

DVP RAW8 data format is also supported in serializer RAW10 transmit mode with 8/10 data input bits (MSB or LSB) connected to the serializer DVP source. DVP format serializer inputs must have discrete synch signals. When paired with DS90UB9x3x-Q1 serializers, the DS90UB936-Q1 utilizes the HSYNC and VSYNC inputs to construct the MIPI CSI-2 Tx data packets. Ensure the Frame Valid to Line Valid setup time is configured appropriately for DVP input system use cases as a minimum setup timing is required as per 表 7-11.

In RAW mode the DS90UB936-Q1 deserializer each Rx Port can support up to:

- 12 bits of DATA + 2 SYNC bits for an input PCLK range of 37.5 MHz to 100 MHz (75 MHz for 913A-Q1) in the 12-bit, high frequency mode. Line rate = f_{PCLK} × (2/3) × 28; for example, f_{PCLK} = 100 MHz, line rate = (100 MHz) × (2/3) × 28 = 1.87 Gbps. Note: No HS/VS restrictions (raw).
- 10 bits of DATA + 2 SYNC bits for an input PCLK range of 50 MHz to 100 MHz in the 10-bit mode. Line rate = f_{PCLK}/2 × 28; for example, f_{PCLK} = 100 MHz, line rate = (100 MHz/2) × 28 = 1.40 Gbps. Note: HS/VS is restricted to no more than one transition per 10 PCLK cycles.
- 12 bits of DATA + 2 bits SYNC for an input PCLK range of 25 MHz to 50 MHz in the 12-bit low frequency mode. Note: No HS/VS restrictions (raw).

When operating with DVP serializer, the DS90UB936-Q1 deserializer also supports DVP formats such as YUV-422 which have the same pixel packing as RAW8, RAW10 or RAW12. For example; there are 3 YUV CSI-2 data types that have the same pixel packing as RAW10: YUV420 10 bit, YUV420 10 bit Chroma shifted or YUV422 10bit. These formats can be used as well as 8 bit and 12 bit YUV formats which adhere to the same structure as RAW8 and RAW12 respectively.

7.4.3 RX MODE Pin

Configuration of the FPD-Link III operating input mode may be done through the MODE input strap pin, or through the configuration register bits. A pullup resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE input (V_{TARGET}) and $V_{(VDD18)}$ to select one of the 8 possible selected modes. The DS90UB936-Q1 waits 1 ms after PDB goes high to allow time for power supply transients before sampling the MODE pin strap value and configuring the device to set the I2C address. Possible configurations are:

- CSI-2 input Rx REFCLK mode
- RAW12 / RAW10 DVP Rx modes

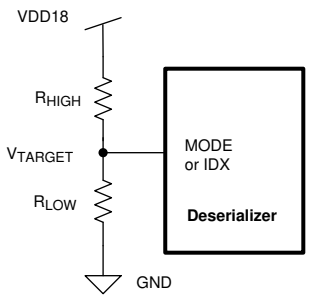


図 7-2. Strap Pin Connection Diagram

表 7-2. Strap Configuration Mode Select

MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	CSI-2 non-synchronous back channel
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	RAW12 LF
	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	RAW12 HF
	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	RAW10
	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	CSI-2 synchronous back channel

The strapped values can be viewed and modified in the following locations:

- RX Mode – Port Configuration FPD3_MODE (Register 0x6D[1:0])
- Clock Mode – Device Status and CSI_PLL_CTL (Register bits 0x04[4] and 0x1F[1:0])

7.4.4 REFCLK

A valid 23-MHz to 26-MHz reference clock is required on the REFCLK pin 5 for precise frequency operation. The REFCLK frequency defines all internal clock timers, including the back channel rate, I2C timers, CSI-2 datarate, FrameSync signal parameters, and other timing critical internal circuitry. REFCLK input must be continuous. If the REFCLK input does not detect a transition more than 20 µS, this may cause a disruption in the CSI-2 output. REFCLK should be applied to the DS90UB936-Q1 only when the supply rails are above minimum levels (see セクション 9.2). At start-up, the DS90UB936-Q1 defaults to an internal oscillator to generate an backup internal reference clock at nominal frequency of 25 MHz ±10%.

The REFCLK LVCMOS input oscillator specifications are listed in 表 7-3.

表 7-3. REFCLK Oscillator Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency tolerance	–40°C ≤ T_A ≤ 105°C			±50	ppm
Frequency stability	Aging			±50	ppm
Amplitude		800	1200	$V_{(VDDIO)}$	mVp-p
Symmetry	Duty Cycle	40%	50%	60%	
Rise and fall time	10% – 90%			6	ns
Jitter	200 kHz – 10 MHz		50	200	ps p-p
Frequency		23	25	26	MHz
Spread-spectrum clock modulation percentage	Center Spread	-0.5		+0.5	%
	Down Spread	-1		0	%
Spread-spectrum clock modulation frequency				33	KHz

7.4.5 Crystal Recommendations

A 25-MHz, parallel, 18-pF load crystal resonator should be used if a crystal source is desired. 図 7-3 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

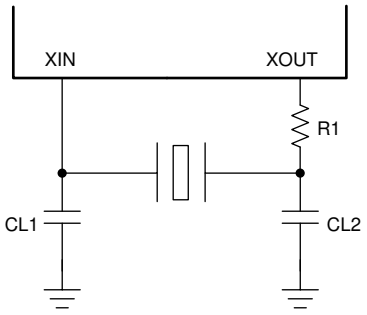


図 7-3. Crystal Oscillator Circuit

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, CL1 and CL2 should be set at 27 pF and R1 should be set at 0 Ω. Specification for 25-MHz crystal are listed in 表 7-4.

表 7-4. 25 MHz Crystal Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency			25		MHz
Frequency Tolerance and Stability	Across operational temperature and aging			±100	ppm

7.4.6 Receiver Port Control

The DS90UB936-Q1 can support single or dual simultaneous inputs to Rx port 0 and Rx port 1. The Receiver port control register RX_PORT_CTL 0x0C (表 7-31) allows for disabling one or both of the Rx inputs when not in use. These bits can only be written by a local I2C controller at the deserializer side of the FPD-Link.

Each FPD-Link III Receive port has a unique set of registers that provides control and status corresponding to Rx port 0 or Rx port 1. Control of the FPD-Link III port registers is assigned by the FPD3_PORT_SEL register, which sets the page controls for reading or writing individual ports unique registers. For each of the FPD-Link III Receive Ports, the FPD3_PORT_SEL 0x4C register defaults to selecting that port's registers as detailed in register description (表 7-86).

As an alternative to paging to access FPD-Link III Receive unique port registers, separate I2C addresses may be enabled to allow direct access to the port-specific registers. The Port I2C address registers allow programming a separate 7-bit I2C address to allow access to unique, port-specific registers without paging. I2C commands to these assigned I2C addresses are also allowed access to all shared registers (see 表 7-179).

7.4.6.1 Video Stream Forwarding

Video stream forwarding is handled by the Rx Port forwarding control in register 0x20 (see *セクション 7.6.33*). Forwarding from input ports are disabled by default and must be enabled using per-port controls. Different options for forwarding CSI-2 packets can also be selected as described starting in *セクション 7.4.28*.

7.4.7 LOCK and PASS Status

The DS90UB936-Q1 provides dedicated PASS and LOCK outputs for monitoring status as well as through the DEVICE_STS register (address 0x04).The source of the deserializer LOCK and PASS signals for pin monitoring and interrupt operation is also controlled by the LOCK_SEL and PASS_SEL fields in the RX_PORT_CTL register. The source of the LOCK and PASS can be allocated to either of the following system use cases: 00: Port 0 Receiver, 01: Port 1 Receiver, 10: Any Enabled Receiver Port (Logical OR), and 11: All Enabled Receiver Ports (logical AND). At start-up, the deserializer will synchronize with the input signal provided by the serializer and assert the LOCK indication once stable. The lock detect circuit includes an option to check for link bit errors as part of the lock detection and determine if LOCK is lost. The Receive Port Lock status is available for each port through the RX_PORT_STS1 register 0x4D. The LOCK status may also be used to enable video forwarding and other options. I2C communication across the FPD-Link should be attempted only during LOCK condition.

In RAW12 mode, the LOCK pin is only high if there is a link with a serializer that has an active PCLK input. LOCK is low if there is a serializer connected and there is a link established using the internal oscillator of the serializer. Therefore, when using this mode, it is preferred to use the port-specific LOCK_STS register (0x4D[0]), which is high when linked to a serializer with internal oscillator. This LOCK_STS signal can also be an output to a GPIO pin for monitoring in real time. Once LOCK_STS is high for a specific port, remote I2C is available to that serializer. In RAW 10-bit mode, the LOCK pin is high when there is a link with a serializer regardless of whether there is an active PCLK input. The port-specific LOCK_STS register is also valid in either of these modes.

If the deserializer loses LOCK, the receiver will reset and perform the LOCK algorithm again to reacquire the serial data stream sent by the serializer. The receive port will truncate video frames containing errors and resume forwarding the video when LOCK is re-established.

The Receive port will indicate Pass status once specific conditions are met, including a number of valid frames received. Valid frames may include requiring no link bit errors and consistent frame size including video line length or number of video lines. The receive port may be programmed to truncate video frames containing errors and prevent the forwarding of video until the Pass conditions are met.

7.4.8 Input Jitter Tolerance

Input jitter tolerance is the ability of the Clock and Data Recovery (CDR) Phase-Lock Loop (PLL) of the receiver to track and recover the incoming serial data stream. Jitter tolerance at a specific frequency is the maximum jitter permissible before data errors occur. The following shows the allowable total jitter of the receiver inputs and must be less than the values in the chart.

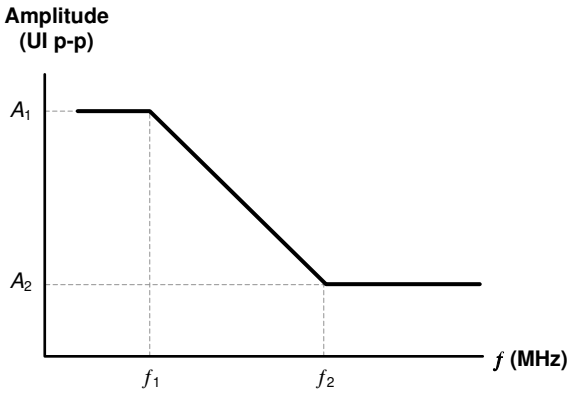


図 7-4. Input Jitter Tolerance Plot

表 7-5. Input Jitter Tolerance Limit

INTERFACE	JITTER AMPLITUDE (UI p-p)		FREQUENCY (MHz) (1)	
FPD-Link III	A1	A2	*f*1	*f*2
	1	0.4	FPD3_PCLK / 80	FPD3_PCLK / 15

(1) FPD3_PCLK is proportional to REFCLK, CSI-2 or PCLK frequency based on the operating MODE (セクション 7.4):
RAW 10-bit mode: PCLK_Freq. / 2
RAW 12-bit mode: PCLK_Freq. x 2/3

7.4.9 Adaptive Equalizer

The FPD-Link III receiver inputs incorporates an adaptive equalizer (AEQ), to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI),

crosstalk, and so forth, must also be considered. The equalization configuration and status are programmed in registers 0xD2–0xD3 (see 表 7-159).

7.4.9.1 Adaptive Equalizer Algorithm

The AEQ process steps through allowed values of the equalizer controls find a value that allows the Clock Data Recovery (CDR) circuit to maintain valid lock condition. For each EQ setting, the circuit waits for a programmed re-lock time period, then checks results for valid lock. If valid lock is detected, the circuit will stop at the current EQ setting and maintain constant value as long as lock state persists. If the deserializer loses LOCK, the adaptive equalizer will resume the LOCK algorithm and the EQ setting is incremented to the next valid state. Once lock is lost, the circuit will continue searching EQ settings to find a valid setting to reacquire the serial data stream sent by the serializer that remains locked.

7.4.9.2 AEQ Settings

7.4.9.2.1 AEQ Start-Up and Initialization

The AEQ circuit can be restarted at any time by setting the AEQ_RESTART bit in the AEQ_CTL2 register 0xD2 (see 表 7-159). Once the deserializer is powered on, the AEQ is continually searching through EQ settings and could be at any setting when signal is supplied from the serializer. If the Rx Port CDR locks to the signal, it may be good enough for low bit errors, but could be not optimized or over-equalized. The DS90UB936-Q1 when connected to a ADAS serializer (DS90UB935-Q1, DS90UB933-Q1, or DS90UB913A-Q1) will by default restart the AEQ adaption upon achieving first positive lock indication to provide more consistent start-up from known conditions. With this feature disabled, the AEQ may lock at a relatively random EQ setting based on when the FPD-Link III input signal is initially present. Alternatively, AEQ_RESTART or DIGITAL_RESET0 could be applied once the ADAS serializer input signal frequency is stable to restart adaption from the minimum EQ gain value. These techniques allow for a more consistent initial EQ setting following adaption.

7.4.9.2.2 AEQ Range

AEQ Min/Max settings: The AEQ circuit can be programmed with minimum and maximum settings used during the EQ adaption. Using the full AEQ range will provide the most flexible solution, however if the channel conditions are known an improved deserializer lock time can be achieved by narrowing the search window for allowable EQ gain settings. For example in a system use case with a longer cable and multiple interconnects creating higher channel attenuation, the AEQ would not adapt to the minimum EQ gain settings. Likewise in a system use case with short cable and low channel attenuation AEQ would not generally adapt to the highest EQ gain settings. The AEQ range is determined by the AEQ_MIN_MAX register 0xD5 (see *セクション 7.6.144*) where AEQ_MAX sets the maximum value of EQ gain. The ADAPTIVE_EQ_FLOOR_VALUE determines the starting value for EQ gain adaption. To enable the minimum AEQ limit, SET_AEQ_FLOOR bit in the AEQ_CTL2 register 0xD2[2] must also be set. An AEQ range (AEQ_MAX - AEQ_FLOOR) to allow a variation around the nominal setting of –2/+4 or ±3 around the nominal AEQ value specific to Rx port channel characteristics provides a good trade off in lock time and adaptability. The setting for the AEQ after adaption can be readback from the AEQ_STATUS register 0xD3 (see *セクション 7.6.142*).

7.4.9.2.3 AEQ Timing

The dwell time for AEQ to wait for lock or error free status is also programmable. When checking each EQ setting the AEQ will wait for a time interval, controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register (see 表 7-159) before incrementing to the next allowable EQ gain setting. The default wait time is set to 2.62 ms based on REFCLK = 25 MHz. Once the maximum setting is reached, if there is no lock acquired during the programmed relock time, the AEQ will restart adaption at the minimum setting or AEQ_FLOOR value.

7.4.9.2.4 AEQ Threshold

The DS90UB936-Q1 receiver will by default adapt based on FPD-Link error checking during the Adaptive Equalization process. The specific errors linked to equalizer adaption, FPD-Link III clock recovery error, packet encoding error, and parity error can be individually selected in AEQ_CTL1 register 0x42 (see *セクション 7.6.63*). Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting.

7.4.10 Channel Monitor Loop-Through Output Driver (CMLOUT)

The DS90UB936-Q1 includes an internal **C**hannel **M**onitor **L**oop-through output on the CMLOUTP and CMLOUTN pins. A buffered loop-through output driver is provided on the CMLOUTP and CMLOUTN for observing jitter after equalization for each of the two RX receive channels. The CMLOUT monitors the post EQ stage thus providing the recovered input of the deserializer signal. The measured serial data width on the CMLOUT loop-through is the total jitter including the internal driver, AEQ, back channel echo, and so forth. Each channel also has its own CMLOUT monitor and can be used for debug purposes. This CMLOUT is useful in identifying gross signal conditioning issues.

表 7-7 includes details on selecting the corresponding RX receiver of CMLOUTP and CMLOUTN configuration. To disable the CMLOUT, either follow the instructions in table to reload register default values, or reset the DS90UB936-Q1.

表 7-6. CML Monitor Output Driver

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
E_W	Differential Output Eye Opening	R_L = 100 Ω (図 7-5)	CMLOUTP, CMLOUTN	0.45			UI(1)

(1) UI – Unit Interval is equivalent to one ideal serialized FPD-Link III data bit width. The UI scales with serializer input PCLK frequency. Refer to the serializer datasheets for more PCLK information
CSI-2 mode: 1 UI = 1 / (PCLK_Freq x 40) (typical)
10-bit mode: 1 UI = 1 / (PCLK_Freq. / 2 × 28)
12-bit mode: 1 UI = 1 / (PCLK_Freq. × 2 / 3 × 28)

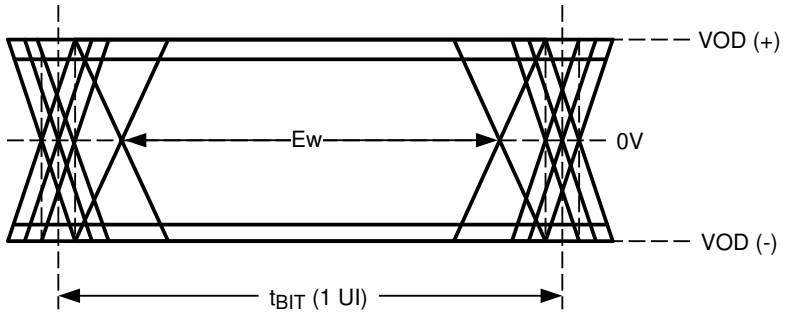


図 7-5. CMLOUT Output Driver

表 7-7. Channel Monitor Loop-Through Output Configuration

	FPD-Link III RX Port 0	FPD-Link III RX Port 1
ENABLE MAIN LOOP-THROUGH DRIVER	0xB0 = 0x14; 0xB1 = 0x00; 0xB2 = 0x80 0xB1 = 0x03; 0xB2 = 0x28 0xB1 = 0x04; 0xB2 = 0x28	
SELECT CHANNEL MUX	0xB1 = 0x02; 0xB2 = 0x20	0xB1 = 0x02; 0xB2 = 0xA0
SELECT RX PORT	0xB0 = 0x04; 0xB1 = 0x0F; 0xB2 = 0x01 0xB1 = 0x10; 0xB2 = 0x02	0xB0 = 0x08; 0xB1 = 0x0F; 0xB2 = 0x01 0xB1 = 0x10; 0xB2 = 0x02
DISABLE MAIN LOOP-THROUGH DRIVER	0xB0 = 0x14; 0xB1 = 0x00; 0xB2 = 0x00 0xB1 = 0x03 ; 0xB2 = 0x08 0xB1 = 0x04; 0xB2 = 0x08	
DESELECT CHANNEL MUX	0xB1 = 0x02; 0xB2 = 0x20	0xB1 = 0x02; 0xB2 = 0x20
DESELECT RX PORT	0xB0 = 0x04; 0xB1 = 0x0F; 0xB2 = 0x00 0xB1 = 0x10; 0xB2 = 0x00	0xB0 = 0x08; 0xB1 = 0x0F; 0xB2 = 0x00 0xB1 = 0x10; 0xB2 = 0x00

7.4.10.1 Code Example for CMLOUT FPD-Link III RX Port 0:

```
WriteI2C(0xB0,0x14)    # FPD-Link III RX Shared, page 0
WriteI2C(0xB1,0x00)    # Offset 0
WriteI2C(0xB2,0x80)    # Enable loop through driver
WriteI2C(0xB1,0x03)    #
WriteI2C(0xB2,0x28)    #
WriteI2C(0xB1,0x04)    #
WriteI2C(0xB2,0x28)    #
#
WriteI2C(0xB1,0x02)    #
WriteI2C(0xB2,0x20)    #
#
WriteI2C(0xB0,0x04)    # Offset 4
WriteI2C(0xB1,0x0F)    #
WriteI2C(0xB2,0x01)    #
WriteI2C(0xB1,0x10)    #
WriteI2C(0xB2,0x02)    # Enable CML data output
```

7.4.11 RX Port Status

In addition to the Lock and PASS indications, the deserializer is able to monitor and detect several other RX port-specific conditions and interrupt states. This information is latched into the RX port status registers RX_PORT_STS1 (0x4D) and RX_PORT_STS2 (0x4E). There are bits to flag any change in LOCK status (LOCK_STS_CHG) or detect any errors in the control channel over the forward link (BCC_CRC_ERROR, BCC_SEQ_ERROR) which are cleared upon read. The Rx Port status registers also allow the user to monitor the presence of the stable input signal, along with parity and CRC errors, line length, and lines per video frame.

7.4.11.1 RX Parity Status

The FPD-Link III receiver checks the decoded data parity to detect any errors in the received FPD-Link III frame. Parity errors are counted up and accessible through the RX_PAR_ERR_HI and RX_PAR_ERR_LO registers 0x55 and 0x56 to provide combined 16-bit error counter. In addition, a parity error flag can be set once a programmed number of parity errors have been detected. This condition is indicated by the PARITY_ERROR flag in the RX_PORT_STS1 register. Reading the counter value will clear the counter value and PARITY_ERROR flag. An interrupt may also be generated based on assertion of the parity error flag. By default, the parity error counter will be cleared and the flag will be cleared on loss of Receiver lock. To ensure an exact read of the parity error counter, parity checking should be disabled in the GENERAL_CFG register 0x02 before reading the counter.

7.4.11.2 FPD-Link Decoder Status

The FPD-Link III receiver also checks the decoded data for encoding or sequence errors in the received FPD-Link III frame. If either of these error conditions are detected the FPD3_ENC_ERROR bit will be latched in the RX_PORT_STS2 register 0x4E[5]. An interrupt may also be generated based on assertion of the encoded error

flag. To detect FPD-Link III Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error. The FPD3_ENC_ERROR flag is cleared on read.

When partnered with a DS90UB935-Q1, the FPD3 Encoder may be configured to include a CRC check of the FPD3 encoder sequence. The CRC check provides an extra layer of error checking on the encoder sequence. This CRC checking adds protection to the encoder sequence used to send link information comprised of Datapath Control (registers 0x59 and 0x5A), Sensor Status (registers 0x51-0x54), and Serializer ID (register 0x5B). TI recommends enabling the CRC error checking on the FPD3 Encoder sequence to prevent any updates of link information values from encoded packets that do not pass CRC check. The FPD3 Encoder CRC is enabled by setting the FPD3_ENC_CRC_DIS (register 0xBA[7] 表 7-151) to 0. In addition, the FPD3_ENC_CRC_CAP flag should be set in register 0x4A[4] (see セクション 7.6.66).

7.4.11.3 RX Port Input Signal Detection

The DS90UB936-Q1 can detect and measure the approximate input frequency and frequency stability of each RX input port and indicate status in bits [2:1] of RX_PORT_STS2. Frequency measurement stable FREQ_STABLE indicates the FPD-Link III input clock frequency is stable. When no FPD-Link III input clock is detected at the RX input port the CABLE_FAULT bit indicates that condition has occurred. Setting of these error flags is dependent on the stability control settings in the FREQ_DET_CTL register 0x77. The CABLE_FAULT bit will be set if the input frequency is below the setting programmed in the FREQ_LO_THR setting in the FREQ_DET_CTL register. A change in frequency FREQ_STABLE = 0, is defined as any change in MHz greater than the value programmed in the FREQ_HYST value. The frequency is continually monitored and provided for readback through the I2C interface less than every 1 ms. A 16-bit value is used to provide the frequency in units of 2 to 8 MHz. An interrupt can also be generated for any of the ports to indicate if a change in frequency is detected on any port.

7.4.11.4 Line Counter

For each video frame received, the deserializer will count the number of video lines in the frame. In CSI-2 input mode, any long packet will be counted as a video line. In RAW mode, any assertion of the Line Valid (LV) signal will be interpreted as a video line. The LINE_COUNT_1 and LINE_COUNT_0 registers in 0x73 and 0x74 can be used to read the line count for the most recent video frame. Line Length may not be consistent when receiving multiple CSI-2 video streams differentiated by VC-ID. An interrupt may be enabled based on a change in the LINE_COUNT value. If interrupts are enabled, the LINE_COUNT registers will be latched at the interrupt and held until read back by the processor through I2C.

7.4.11.5 Line Length

For each video line, the length (in bytes) will be determined. The LINE_LEN_1 and LINE_LEN_0 registers 0x75 and 0x76 can be used to read the line count for the most recent video frame. If the line length is not stable throughout the frame, the length of the last line of the frame will be reported. Line Count may not be consistent when receiving multiple CSI-2 video streams differentiated by VC-ID. An interrupt may be enabled based on a change in the LINE_LEN value. If interrupts are enabled, the LINE_LEN registers will be latched at the interrupt and held until read by the processor through I2C.

7.4.12 Sensor Status

When paired with the DS90UB935-Q1 serializer, the DS90UB936-Q1 is capable of receiving diagnostic indicators from the serializer. The sensor alarm and status diagnostic information are reported in the SENSOR_STS_X registers (0x51 to 0x54 in 表 7-92). The interrupt capability from detected status changes in sensor are described in セクション 7.5.8.2.2. Sensor Status This interrupt condition will be cleared by reading the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers (registers 0xDE and 0xDF).

7.4.13 GPIO Support

In addition to the dedicated LOCK and PASS output pins, the DS90UB936-Q1 supports seven pins, GPIO0 through GPIO6, which can be monitored, configured, and controlled through I2C in registers 0x0E - 0x16. GPIO3 programmable I/O pin is an active-low open drain and is shared with INTB. The current status of all GPIO can be

readback from register 0x0E. Each GPIO is programmable for multiple uses options through the GPIOx_PIN_CTL registers 0x10 - 0x16.

7.4.13.1 GPIO Input Control and Status

Upon initialization GPIO0 through GPIO6 are enabled as inputs by default. Each GPIO pin has an input disable and a pulldown disable control bit, with the exception of GPIO3 which is open drain. By default, the GPIO pin input paths are enabled and the internal pulldown circuit for the GPIO is enabled. The GPIO_INPUT_CTL (0x0F) and GPIO_PD_CTL (0xBE) registers allow control of the input enable and the pulldown, respectively. For example, to disable GPIO1 and GPIO2 as inputs the user would program in register 0x0F[2:1] = 11. For most applications, there is no need to modify the default register settings for the pulldown resistors. The status HIGH or LOW of each GPIO pin 0 through 6 may be read through the GPIO_PIN_STS register 0x0E. This register read operation provides the status of the GPIO pin independent of whether the GPIO pin is configured as an input or output.

7.4.13.2 GPIO Output Pin Control

Individual GPIO output pin control is programmable through the GPIOx_PIN_CTL registers 0x10 to 0x16 (表 7-35). To enable any of the GPIO as output, set bit 0 = 1 in the respective register 0x10 to 0x16 after clearing the corresponding input enable bit in register 0x0F (表 7-34). The configuration register for each GPIO is listed in 表 7-8.

7.4.13.3

図 7-6. GPIOx Register Content (0x10 - 0x16)

7	6	5	4	3	2	1	0
GPIOX_OUTPUT_SEL[2:0]			GPIOX_OUT_SRC[2:0]			GPIOX_OUT_VAL	GPIOX_OUT_EN

表 7-8. GPIOx Output Function Programming

GPIO OUTPUT FUNCTION	GPIOX OUTPUT SOURCE SELECT GPIOX_OUT_SRC[2:0]		GPIOX OUTPUT FUNCTION SELECT GPIOX_OUTPUT_SEL[2:0]	GPIOX OUTPUT VALUE (GPIOX_OUT_VAL)	GPIO OUTPUT ENABLE (GPIOX_OUT EN)
	VALUE	OUTPUT SIGNAL SOURCE			
GPIOX output disabled	X	No output. GPIO is Disabled or set to input mode	X	X	0
GPIOX linked to Forward channel received GPIO0 from RX Port 0 Serializer	000	RX Port 0	000	X	1
GPIOX linked to Forward channel received GPIO1 from RX Port 0 Serializer			001	X	1
GPIOX linked to Forward channel received GPIO2 from RX Port 0 Serializer			010	X	1
GPIOX linked to Forward channel received GPIO3 from RX Port 0 Serializer			011	X	1
RX Port 0 Lock indication			100	X	1
RX Port 0 Pass indication			101	X	1
RX Port 0 Frame Valid signal			110	X	1
RX Port 0 Line Valid signal			111	X	1

表 7-8. GPIOx Output Function Programming (continued)

GPIO OUTPUT FUNCTION	GPIOX OUTPUT SOURCE SELECT GPIOX_OUT_SRC[2:0]		GPIOX OUTPUT FUNCTION SELECT GPIOX_OUTPUT_SEL[2:0]	GPIOX OUTPUT VALUE (GPIOX_OUT_VAL)	GPIO OUTPUT ENABLE (GPIOX_OUT EN)
	VALUE	OUTPUT SIGNAL SOURCE			
GPIOX linked to Forward channel received GPIO0 from RX Port 1 Serializer	001	RX Port 1	000	X	1
GPIOX linked to Forward channel received GPIO1 from RX Port 1 Serializer			001	X	1
GPIOX linked to Forward channel received GPIO2 from RX Port 1 Serializer			010	X	1
GPIOX linked to Forward channel received GPIO3 from RX Port 1 Serializer			011	X	1
RX Port 1 Lock indication			100	X	1
RX Port 1 Pass indication			101	X	1
RX Port 1 Frame Valid signal			110	X	1
RX Port 1 Line Valid signal			111	X	1
Reserved	010	Reserved	X	X	X
Set GPI0X = LOW value programmed by register	100	Device Status	000	0	1
Set GPIOX = HIGH value programmed by register			000	1	1
Logical OR of Lock indication from enabled RX ports			001	X	1
Logical AND of Lock indication from enabled RX ports			010	X	1
Logical AND of Pass indication from enabled RX ports			011	X	1
FrameSync signal (internal or external)			100	X	1
Device interrupt active high			101	X	1
Device interrupt active low			110	X	1
Reserved	100	Reserved	111	X	X
Pass (AND of selected RX port status)	101	CSI-2 Tx Port	000	X	1
Pass (OR of selected RX port status)			001	X	1
Frame Valid signal corresponding to video frame recovered at deserializer (Note) Insert cross reference			010	X	1
Line Valid signal corresponding to video frame recovered at deserializer (Note) Insert cross reference			011	X	1
RX Ports synchronized, RX Port 0 synchronized with RX Port 1			100	X	1
:CSI-2 TX Port Interrupt active high			101	X	1
Reserved	101	Reserved	110	X	X
Reserved	101	Reserved	111	X	X
Reserved	110	Reserved	X	X	X
Reserved	111	Reserved	X	X	X

7.4.13.4 Forward Channel GPIO

The DS90UB936-Q1 has seven GPIO pins that can output data received from the forward channel when paired with the DS90UB935-Q1 serializer. The remote Serializer GPIO are mapped to GPIO. Each GPIO pin can be

programmed for output mode and mapped. Up to four GPIOs are supported in the forward direction on each FPD-Link III Receive port (see 表 7-99). Each forward channel GPIO (from any port) can be mapped to any GPIO output pin. The DS90UB933-Q1 and DS90UB913A-Q1 GPIOs cannot be configured as inputs for remote communication over the forward channel to the DS90UB936-Q1.

The timing for the forward channel GPIO is dependant on the number of GPIOs assigned at the serializer. When a single GPIO input from the DS90UB935-Q1 serializer is linked to a DS90UB936-Q1 deserializer, the GPIO output value is sampled every forward channel transmit frame. Two linked GPIO are sampled every two forward channel frames and three or four linked GPIO are sampled every five frames. The typical minimum latency for the GPIO remains consistent (approximately 225 ns), but as the information gets spread over multiple frames, the jitter is typically increased on the order of the sampling period (number of forward channel frames). TI recommends maintaining a 4x oversampling ratio for linked GPIO throughput. For example, when operating in 4-Gbps synchronous mode with REFCLK = 25 MHz, the maximum recommended GPIO input frequency based on the number of GPIO linked over the forward channel is shown in 表 7-9.

表 7-9. Forward Channel GPIO Typical Timing

NUMBER OF LINKED FORWARD CHANNEL GPIOs (FC_GPIO_EN 表 7-99)	SAMPLING FREQUENCY (MHz) AT FPD-Link III LINE RATE = 4 Gbps	MAXIMUM RECOMMENDED FORWARD CHANNEL GPIO FREQUENCY (MHz)	TYPICAL JITTER (ns)
1	100	25	12
2	50	12.5	24
4	20	5	60

In addition to mapping remote serializer GPI, an internally generated FrameSync (see *セクション 7.4.27*) or other control signals may be output from any of the deserializer GPIOs for synchronization with a local processor or another deserializer.

7.4.13.5 Back Channel GPIO

Each DS90UB936-Q1 GPIO pin defaults to input mode at start-up. The deserializer can link GPIO pin input data on up to four available slots to send on the back channel per each remote serializer connection. Any of the seven GPIO pin data can be mapped to send over the available back channel slots for each FPD-Link III Rx port. The same GPIO on the deserializer pin can be mapped to multiple back channel GPIO signals. For each 50-Mbps back channel operation, the frame period is 600 ns (30 bits × 20 ns/bit). For each 2.5-Mbps back channel , the frame period is 12 µs (30 bits × 400 ns/bit). As the back channel GPIOs are sampled and sent each back channel frame by the DS90UB936-Q1 deserializer, the latency and jitter timing are each on the order of one back channel frame. The back channel GPIO is effectively sampled at a rate of 1/30 of the back channel rate or 1.67 MHz at f_{BC} = 50 Mbps. TI recommends that the input to back channel GPIO switching frequency is < 1/4 of the sampling rate or 416 kHz at f_{BC} = 50 Mbps. For example, when operating in 4-Gbps synchronous mode with REFCLK = 25 MHz, the maximum recommended GPIO input frequency based on the data rate when linked over the back channel is shown in 表 7-10.

表 7-10. Back Channel GPIO Typical Timing

BACK CHANNEL RATE (Mbps)	SAMPLING FREQUENCY (kHz)	MAXIMUM RECOMMENDED BACK CHANNEL GPIO FREQUENCY (kHz)	TYPICAL LATENCY (us)	TYPICAL JITTER (us)
50	1670	416	1.5	0.7
10	334	83.5	3.2	3
2.5	83.5	20	12.2	12

In addition to sending GPIO from pins, an internally generated FrameSync or external FrameSync input signal may be mapped to any of the back channel GPIOs for synchronization of multiple sensors with extremely low skew. (see *セクション 7.4.27*).

For each port, GPIO control is available through the BC_GPIO_CTL0 register 0x6E (see 表 7-120) and BC_GPIO_CTL1 register 0x6F (see 表 7-121).

7.4.13.6 Other GPIO Pin Controls

Each GPIO pin can has a input disable and a pulldown disable. By default, the GPIO pin input paths are enabled and the internal pulldown circuit in the GPIO is enabled. The GPIO_INPUT_CTL register 0x0F and GPIO_PD_CTL register 0xBE allow control of the input enable and the pulldown respectively. For most applications, there is no need to modify the default register settings.

7.4.14 Line Valid and Frame Valid Indicators

The FrameValid (FV) and LineValid (LV) indications from the Receive Port indicate approximate frame and line boundaries at the FPD-Link III Receiver input. These signals may not be accurate if the receiver is in CSI-2 input mode and multiple video streams are present at the Receive Port input. A common example of this scenario would be multiple Virtual Channel IDs received on a single port.

When the receiver is in one of the Raw modes the LV and FV provides controls for the video framing. The FV is equivalent to a Vertical Sync (VSYNC) while the LineValid is equivalent to a Horizontal Sync (HSYNC) input to the DS90UB933A-Q1 and DS90UB913A-Q1 device (see *セクション 7.4.27*).

The DS90UB936-Q1 allows setting the polarity of these signals by register programming. The FV and LV polarity are controlled on a per-port basis and can be independently set in the PORT_CONFIG2 register 0x7C.

To prevent false detection of FrameValid, FV must be asserted for a minimum number of clocks prior to first video line to be considered valid. The minimum FrameValid time is programmable in the FV_MIN_TIME register 0xBC. Because the measurement is in FPD-Link III clocks, the minimum FrameValid setup to LineValid timing at the Serializer will vary based on the RAW input operating mode.

A minimum FV to LV timing is required when processing RAW video frames at the serializer input. If the FV to LV minimum setup is not met (by default), the first video line is discarded. Optionally, a register control (PORT_CONFIG:DISCARD_1ST_ON_ERR) forwards the first video line missing some number of pixels at the start of the line.

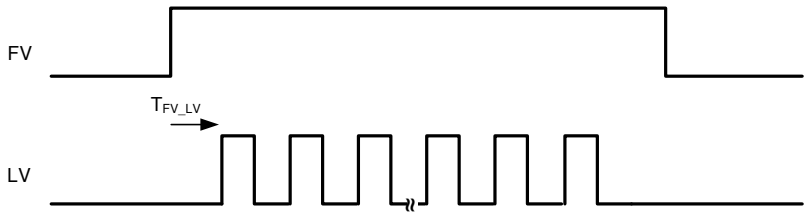


図 7-7. Minimum FV to LV

表 7-11. Minimum FV to LV Setup Requirement (in RAW Mode Serializer FPD-Link III PCLKs)

MODE	FV_MIN_TIME CONVERSION FACTOR	ABSOLUTE MIN (FV_MIN_TIME = 0)	DEFAULT (FV_MIN_TIME = 128)
RAW12 HF	1.5	3	195
RAW10	2	5	261

For other settings of FV_MIN_TIME, the required FV to LV setup in Serializer PCLKs can be determined by:

Absolute Min + (FV_MIN_TIME × Conversion factor)

7.4.15 CSI-2 Protocol Layer

The DS90UB936-Q1 implements High-Speed mode to forward CSI-2 Low Level Protocol data. This includes features as described in the Low Level Protocol section of the MIPI CSI-2 Specification. It supports short and long packet formats.

The feature set of the protocol layer implemented by the CSI-2 TX is:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for frame start, frame end, line start and line end information
- Descriptor for the type, pixel depth and format of the Application Specific Payload data
- 16-bit Checksum Code for error detection

図 7-8 shows the CSI-2 protocol layer with short and long packets.

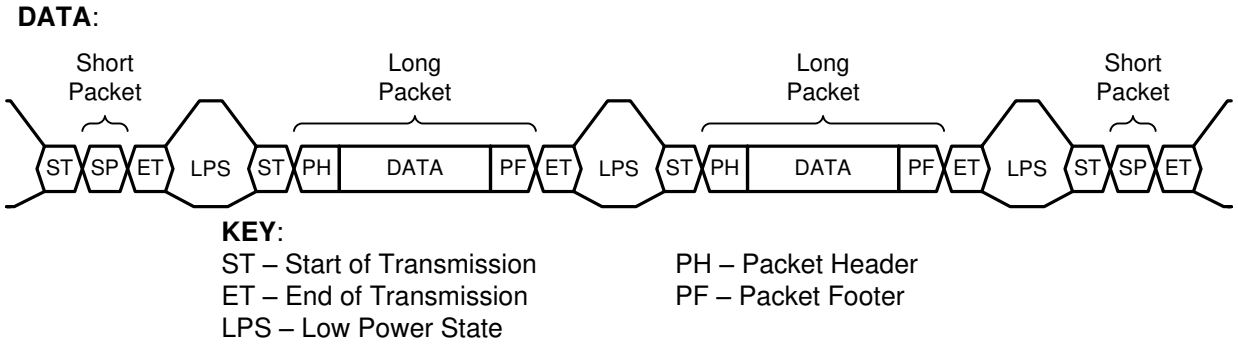


図 7-8. CSI-2 Protocol Layer With Short and Long Packets

7.4.16 CSI-2 Short Packet

The short packet provides frame or line synchronization. 図 7-9 shows the structure of a short packet. A short packet is identified by data types 0x00 to 0x0F.

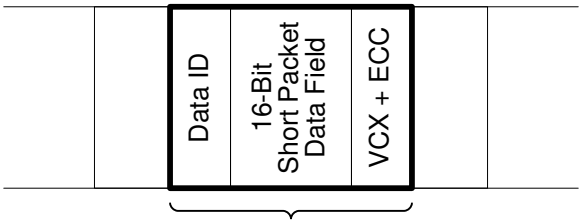


図 7-9. CSI-2 Short Packet Structure

7.4.17 CSI-2 Long Packet

A long packet consists of three elements: a 32-bit packet header (PH), an application-specific data payload with a variable number of 8-bit data words, and a 16-bit packet footer (PF). The packet header is further composed of three elements: an 8-bit data identifier, a 16-bit word count field, and an 8-bit ECC. The packet footer has one element, a 16-bit checksum. 図 7-10 shows the structure of a long packet.

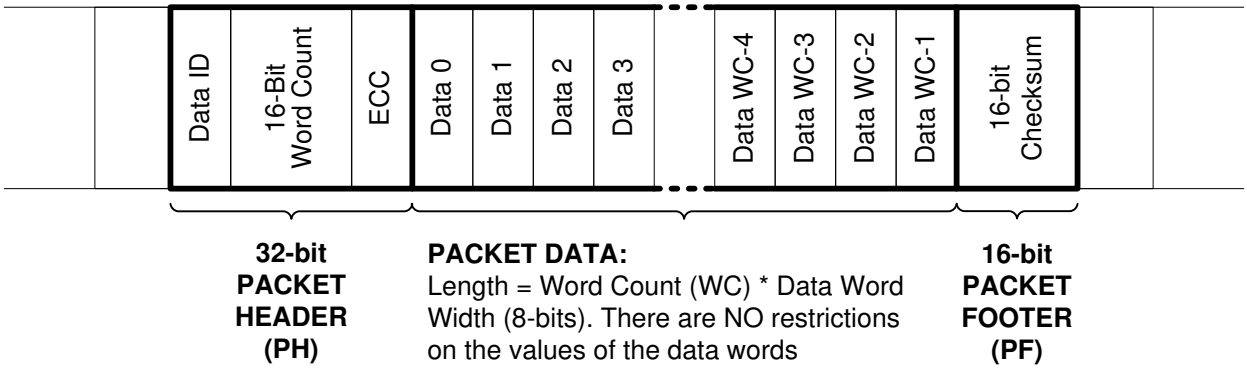


図 7-10. CSI-2 Long Packet Structure

表 7-12. CSI-2 Long Packet Structure Description

PACKET PART	FIELD NAME	SIZE (BIT)	DESCRIPTION
Header	VC / Data ID	8	Contains the virtual channel identifier and the data-type information.
	Word Count	16	Number of data words in the packet data. A word is 8 bits.
	ECC	8	ECC for data ID and WC field. Allows 1-bit error recovery and 2-bit error detection.
Data	Data	WC × 8	Application-specific payload (WC words of 8 bits).
Footer	Checksum	16	16-bit cyclic redundancy check (CRC) for packet data.

7.4.18 CSI-2 Data Type Identifier

The DS90UB936-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in 図 7-11. The virtual channel ID is contained in the 2 MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the six LSBs of the data identifier byte. When partnered with a DS90UB935-Q1 serializer, the Data Type is passed through from the received CSI-2 packets. When partnered with DS90UB933-Q1 or DS90UB913A-Q1 the received RAW mode data is converted to CSI-2 Tx packets with assigned data type and virtual channel ID and matches what is sent by the video source.

DVP format serializer inputs must have discrete synch signals. When interfacing with DS90UB9x3x-Q1 serializers, the DS90UB936-Q1 utilizes the HSYNC and VSYNC inputs to construct the MIPI CSI-2 Tx data packets. When paired with a DVP serializer, the DS90UB936-Q1deserializer supports RAW8, RAW10 or RAW12 as well as formats which have the same pixel packing as RAW8, RAW10 or RAW12 such as YUV-422.

For each RX Port, registers define with which virtual channel and data type the RAW data context is associated:

- For FPD Receiver port operating in RAW input mode connected to a DS90UB933-Q1 or DS90UB913A-Q1 serializer, register 0x70 (see 表 7-122) describes RAW10 Mode and 0x71 (see 表 7-123) RAW12 Mode.
- RAW1x_VC[7:6] field defines the associated virtual ID transported by the CSI-2 protocol from the sensor.
- RAW1x_ID[5:0] field defines the associated data type. The data type is a combination of the data type transported by the CSI-2 protocol.

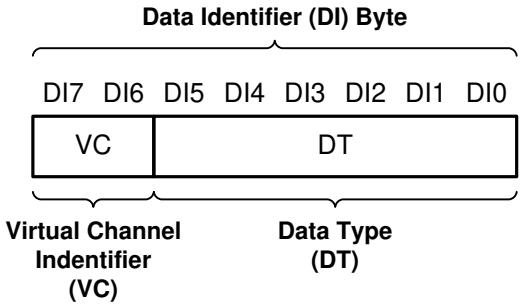


図 7-11. CSI-2 Data Identifier Structure

7.4.19 Virtual Channel and Context

The CSI-2 protocol layer transports virtual channels. The purpose of virtual channels is to separate different data flows interleaved in the same data stream. Each virtual channel is identified by a unique channel identification number in the packet header. Therefore, a CSI-2 TX context can be associated with a virtual channel and a data type. Virtual channels are defined by a 2-bit field. This channel identification number is encoded in the 2-bit code.

The CSI-2 TX transmits the channel identifier number and multiplexes the interleaved data streams. The CSI-2 TX supports up to four concurrent virtual channels.

7.4.20 CSI-2 Input Mode Virtual Channel Mapping

The CSI-2 Input mode (see *セクション 7.4.1*) provides per-port Virtual Channel ID mapping. For each FPD-Link III input port, separate mapping may be done for each input VC-ID to any of four VC-ID values. The mapping is controlled by the VC_ID_MAP register 0x72 (see 表 7-124). This function sends the output as a time-multiplexed CSI-2 stream, where the video sources are differentiated by the virtual channel. The equivalent registers 0x70-0x71 can be used for mapping VC-IDs when operating in RAW FPD-Link III mode connected to DS90UB9x3x-Q1.

7.4.20.1 Example 1

The DS90UB936-Q1 is capable of receiving data from sensors attached to each port. Each port is sending a video stream using VC-ID of 0. The DS90UB936-Q1 can be configured to re-map the incoming VC-IDs to ensure each video stream has a unique ID. The direct implementation would map incoming VC-ID of 0 for RX Port 0, and VC-ID of 1 for RX Port 1.

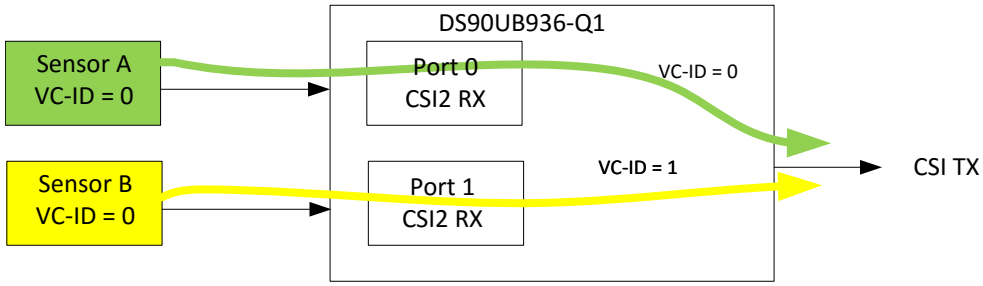


図 7-12. VC-ID Mapping Example 1

7.4.20.2 Example 2:

The DS90UB936-Q1 is receiving two video streams from sensors on each input port. Each sensor is sending video streams using VC-IDs 0 and 1. Receive Port 0 maps the VC-IDs directly without change. Receive Port 1 maps the VC-IDs 0 and 1 to VC-IDs 2 and 3. This is required because each CSI-2 transmitter is limited to 4 VC-IDs per MIPI specification.

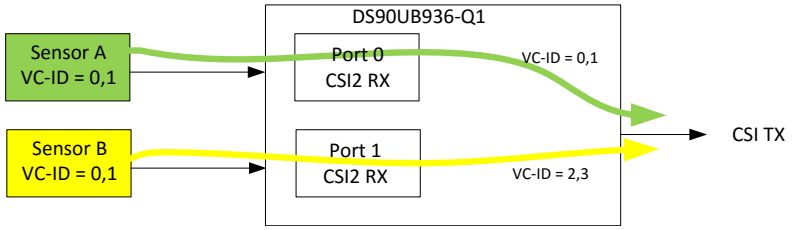


図 7-13. VC-ID Mapping Example 2

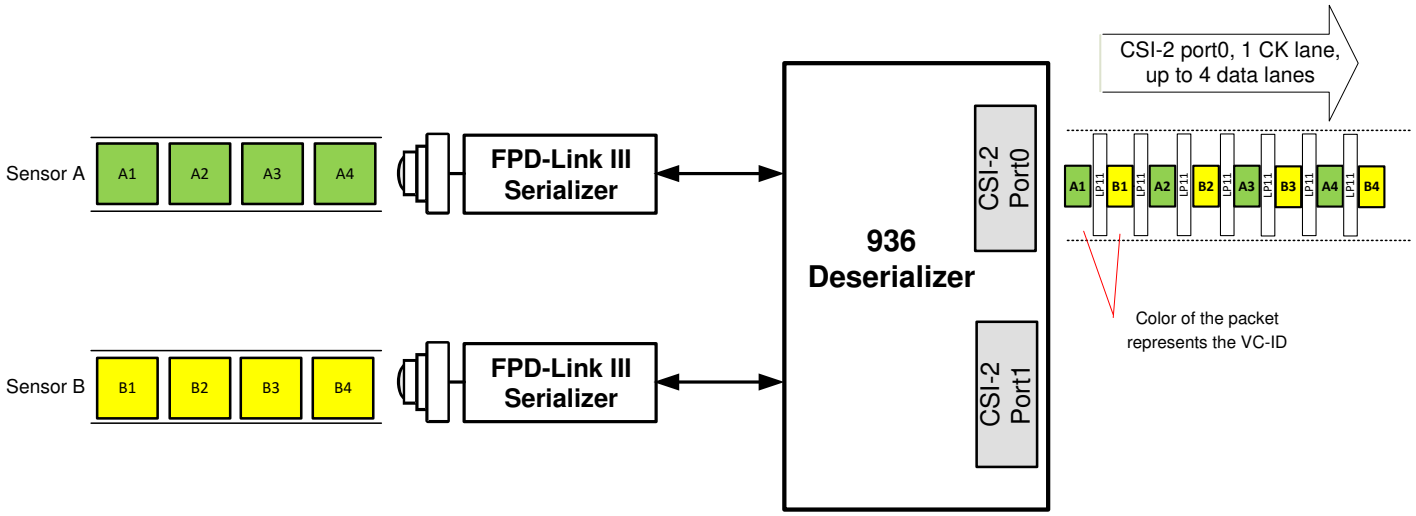


図 7-14. Two Sensor Data onto CSI-2 With Virtual Channels (VC-ID)

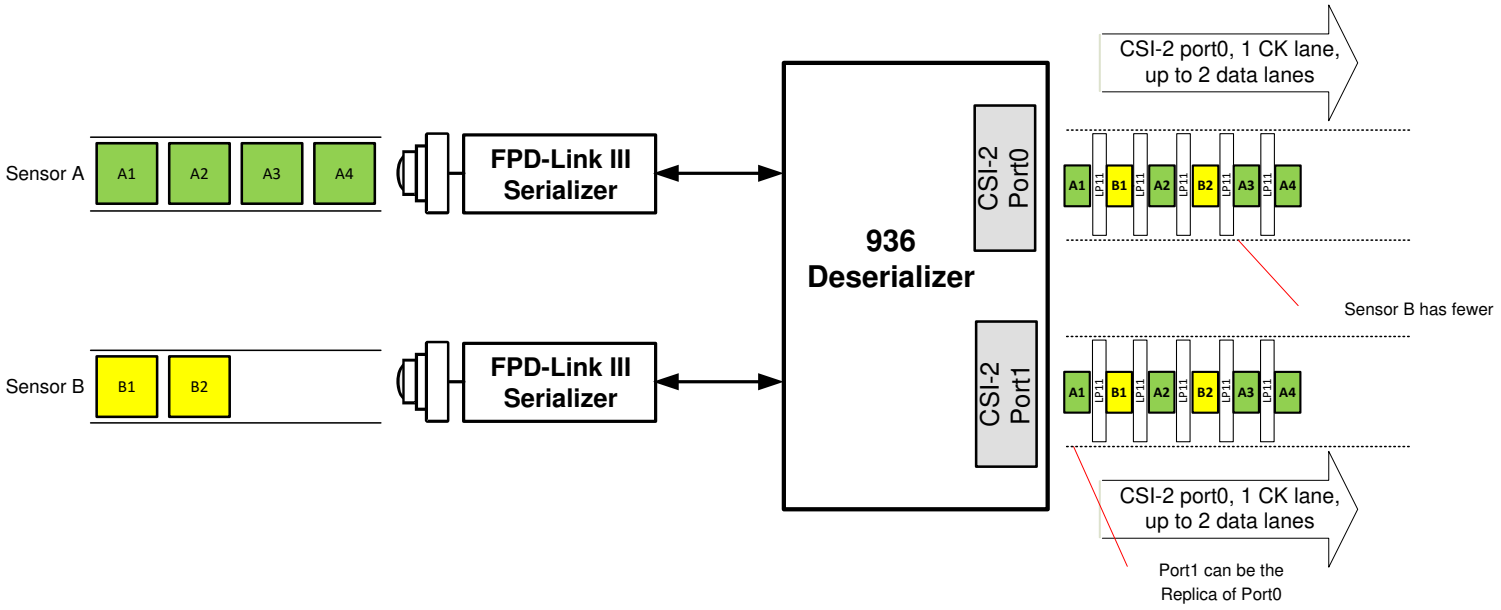


図 7-15. Two Sensor Data With Different Frame Size Replicated onto CSI-2 With Virtual Channels (VC-ID)

7.4.21 CSI-2 Transmitter Frequency

The CSI-2 Transmitters may operate nominally at 400 or 800 Mbps, 1.5 Gbps, or 1.6 Gbps. This operation is controlled through the CSI_PLL_CTL 0x1F register (see 表 7-50). The actual CSI-2 rate is proportional to the REFCLK frequency.

表 7-13. Net CSI-2 Bandwidth Options

CSI_PLL_CTL[1:0]	CSI-2 TX DATA RATE PER LANE (Mbps)	REFCLK FREQUENCY (MHz)	NET CSI-2 VIDEO BANDWIDTH PER RX PORT (Gbps)
00	1664	26	2.528
	1600	25	2.528
	1472	23	2.528
01	Reserved	Reserved	Reserved
10	800	25	1.6 (RX Port 0 and RX Port 1)
11	400	25	0.8 (RX Port 0 and RX Port 1)

When configuring to 800 Mbps or 1.6 Gbps, the CSI-2 timing parameters are automatically set based on the CSI_PLL_CTL 0x1F register. In the case of alternate settings, the respective CSI-2 timing parameters registers must be programmed, and the appropriate override bit must be set. For the 1.664-Gbps and 1.472-Gbps options, these settings will also affect internal device timing for back channel operation, I2C, Bidirectional Control Channel, and FrameSync operation which scale with the REFCLK frequency. Net CSI-2 video bandwidth shown for CSI-2 TX frequency of 400 Mbps and 800 Mbps in 表 7-13 are for both RX ports enabled. When operating with a single RX port, the net CSI-2 video bandwidth can be up to 1.6 Gbps and 2.525 Gbps, respectively.

To operate CSI-2 at speed of 400-Mbps mode, set CSI_PLL_CTL to 11b (0x1F[1:0] =11) to enable 400-Mbps operation for the CSI-2 Transmitters. Internal PLL and Timers are then automatically adjusted for the reduced reference clock frequency. Software control of CSI-2 Transmitter timing registers is required to provide proper interface timing on the CSI-2 Output. The following are the recommended timer settings for 400-Mbps operation.

```
# Set CSI-2 Timing parameters
WriteI2C(0xB0,0x2)     # set auto-increment, page 0
WriteI2C(0xB1,0x40)    # CSI-2 Port 0
WriteI2C(0xB2,0x83)    # TCK Prep
WriteI2C(0xB2,0x8D)    # TCK Zero
WriteI2C(0xB2,0x87)    # TCK Trail
WriteI2C(0xB2,0x87)    # TCK Post
WriteI2C(0xB2,0x83)    # THS Prep
WriteI2C(0xB2,0x86)    # THS Zero
WriteI2C(0xB2,0x84)    # THS Trail
WriteI2C(0xB2,0x86)    # THS Exit
WriteI2C(0xB2,0x84)    # TLPX
```

7.4.22 CSI-2 Replicate Mode

In CSI-2 Replicate mode, both ports can be programmed to output the same data. The output from CSI-2 port 0 is also presented on CSI-2 port 1.

To configure this mode of operation, set the CSI_REPLICATE bit in the FWD_CTL2 register (Address 0x21 in 表 7-52). Enabling replicate mode will automatically enable the second CSI-2 Clock output signal. The CSI-2 transmitter must be programmed for one or two lanes only through the CSI_LANE_COUNT field in the CSI_CTL register as only one or two lanes are supported.

7.4.23 CSI-2 Transmitter Output Control

Two register bits allow controlling the CSI-2 Transmitter output state. If the OUTPUT_SLEEP_STATE_SELECT (OSS_SEL) control is set to 0 in the GENERAL_CFG 0x02 register (see 表 7-21), the CSI-2 Transmitter outputs are forced to the HS-0 state. If the OUTPUT_ENABLE (OEN) register bit is set to 0 in the GENERAL_CFG register, the CSI-2 pins are set to the high-impedance state.

For normal operation (OSS_SEL and OEN both set to 1), activity on either of the Rx Port determines the state of the CSI-2 outputs. The CSI-2 Pin State during FPD-Link III inactive includes two options, controlled by the OUTPUT_EN_MODE bit in the GENERAL_CFG register and FWD_PORTx_DIS in the FWD_CTL1 register 0x20. If OUTPUT_EN_MODE is set to 0, a lack of activity will force the outputs to Hi-Z condition. If OUTPUT_EN_MODE is set to 1, or if the forwarding for the Rx Port is disabled (FWD_PORTx_DIS = 1), the output enters LP-11 state as there is no data available to the CSI-2 Transmitter input. The FPD-Link III inputs are considered active if the Receiver indicates valid lock to the incoming signal. For a CSI-2 TX port, lock is

considered valid if any Received port mapped to the TX port is indicating Lock. See section セクション 7.4.6 for description of Rx port forwarding.

表 7-14. CSI-2 Output Control Options

PDB pin	OSS_SEL	OEN	OUTPUT_OEN_MODE	FWD_PORTx_DIS	FPD-Link III INPUT	CSI-2 PIN STATE
0	X	X	X	X	X	Hi-Z
1	0	X	X	X	X	HS-0
1	1	0	X	X	X	Hi-Z
1	1	1	0	X	All inactive	Hi-Z
1	1	1	1	X	All inactive	LP-11
1	1	1	X	1	Any active	LP-11
1	1	1	X	0	Any active	Valid

7.4.24 CSI-2 Transmitter Status

The status of the CSI-2 Transmitter may be monitored by readback of the CSI_STS register 0x35, or brought to one of the configurable GPIO pins as an output. The TX_PORT_PASS 0x35[0] indicates valid CSI-2 data being presented on CSI-2 port. If no data is being forwarded or if error conditions have been detected on the video data, the CSI-2 Pass signal will be cleared. The TX_PORT_SYNC 0x35[0] indicates the CSI-2 Tx port is able to properly synchronize input data streams from multiple sources. TX_PORT_SYNC will always return 0 if Synchronized Forwarding is disabled. Interrupts may also be generated based on changes in the CSI-2 port status.

7.4.25 Video Buffers

The DS90UB936-Q1 implements two video line buffer and FIFO, one for each RX channel. The video buffers provide storage of data payload and forward requirements for sending multiple video streams on the CSI-2 transmit ports. The total line buffer memory size is a 16-kB block for each RX port.

The CSI-2 transmitter waits for an entire packet to be available before pulling data from the video buffers.

7.4.26 CSI-2 Line Count and Line Length

The DS90UB936-Q1 counts the number of received lines (long packets) to determine line count on LINE_COUNT_1 and LINE_COUNT_0 registers 0x73–74. For received line length, DS90UB936-Q1 reads the number of bytes per line in LINE_LEN_1 and LINE_LEN_0 registers 0x75–0x76. Line Count and Line Length values are valid when receiving a single video stream. If multiple virtual channels are received on a FPD-Link III Receive port in CSI-2 input mode, the values in registers 0x73-74 may not be accurate

7.4.27 FrameSync Operation

A frame synchronization signal (FrameSync) can be sent through the back channel using any of the back channel GPIOs. The signal can be generated in two different methods. The first option offers sending the external FrameSync using one of the available GPIO pins on the DS90UB936-Q1 and mapping that GPIO to a back channel GPIO on one or two of the FPD-Link III ports.

The second option is to have the DS90UB936-Q1 internally generate a FrameSync signal to send through the back channel GPIO to one or two of the attached Serializers.

FrameSync signaling is synchronous on each of the two back channels. Thus, the FrameSync signal arrives at both of the serializers with limited skew.

7.4.27.1 External FrameSync Control

In External FrameSync mode, an external signal is input to the DS90UB936-Q1 through one of the GPIO pins on the device. The external FrameSync signal may be propagated to one or more of the attached FPD-Link III Serializers through a GPIO signal in the back channel. The expected skew timing for external FrameSynch mode is on the order of one back channel frame period or 600 ns when operating at 50 Mbps.

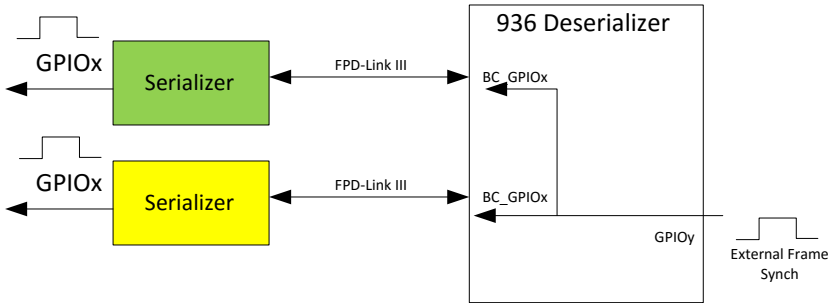


図 7-16. External FrameSync

Enabling the external FrameSync mode is done by setting the FS_MODE control in the FS_CTL register to a value between 0x8 (GPIO0 pin) to 0xE (GPIO6 pin). Set FS_GEN_ENABLE to 0 for this mode.

To send the FrameSync signal on a port's BC_GPIOx signal, the BC_GPIO_CTL0 or BC_GPIO_CTL1 register should be programmed for that port to select the FrameSync signal.

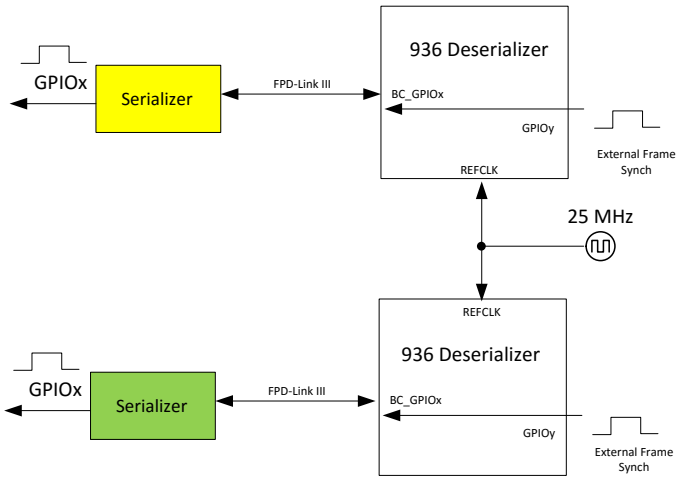


図 7-17. External FrameSync With Two DS90UB936 Deserializers

7.4.27.2 Internally Generated FrameSync

In Internal FrameSync mode, an internally generated FrameSync signal is sent to one or more of the attached FPD-Link III Serializers through a GPIO signal in the back channel.

FrameSync operation is controlled by the FS_CTL 0x18, FS_HIGH_TIME_x, and FS_LOW_TIME_x 0x19–0x1A registers. The resolution of the FrameSync generator clock (FS_CLK_PD) is derived from the back channel frame period (see BC_FREQ_SELECT[2:0] in 表 7-98). For example, each 50-Mbps back channel operation, the frame period is 600 ns (30 bits × 20 ns/bit), and for each 2.5-Mbps back channel , the frame period is 12 µs (30 bits × 400 ns/bit).

Once enabled, the FrameSync signal is sent continuously based on the programmed conditions.

Enabling the internal FrameSync mode is done by setting the FS_GEN_ENABLE control in the FS_CTL register to a value of 1. The FS_MODE field controls the clock source used for the FrameSync generation. The FS_GEN_MODE field configures whether the duty cycle of the FrameSync is 50/50 or whether the high and low periods are controlled separately. The FrameSync high and low periods are controlled by the FS_HIGH_TIME and FS_LOW_TIME registers.

The accuracy of the internally generated FrameSync is directly dependent on the accuracy of the 25-MHz oscillator used as the reference clock and timing values should be scaled if reference other than 25 MHz is used.

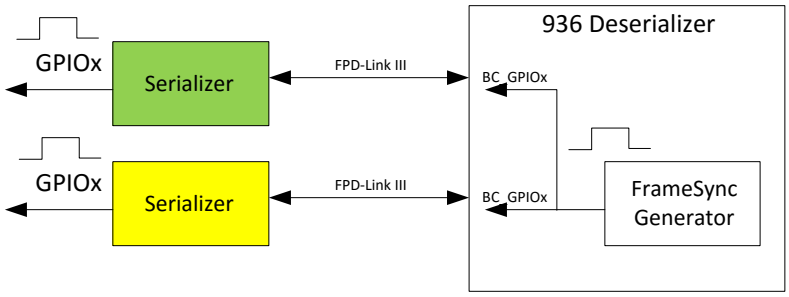
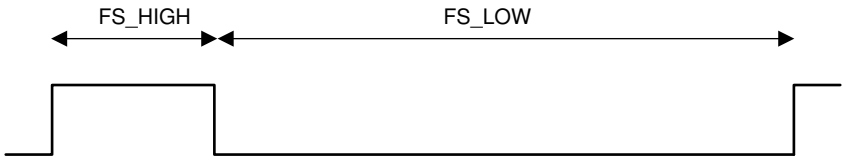


図 7-18. Internal FrameSync



FS_LOW = FS_LOW_TIME * FS_CLK_PD
FS_HIGH = FS_HIGH_TIME * FS_CLK_PD
where FS_CLK_PD is the resolution of the FrameSync generator clock

図 7-19. Internal FrameSync Signal

The following example shows generation of a FrameSync signal at 60 pulses per second. Mode settings:

- Programmable High/Low periods: FS_GEN_MODE 0x18[1]=0
- Use port 0 back channel frame period: FS_MODE 0x18[7:4]=0x0
- Back channel rate of 50 Mbps: BC_FREQ_SELECT for port 0 0x58[2:0]=110b
- Initial FS state of 0: FS_INIT_STATE 0x18[2]=0

Based on mode settings, the FrameSync is generated based upon FS_CLK_PD of 600 ns.

The total period of the FrameSync is (1 / 60 hz) / 600 ns or approximately 27778 counts. The high time is programmed to 2778 and the low time is programmed to 25000.

For a 10% duty cycle, set the high time to 2777 (0x0AD9) cycles, and the low time to 24999 (0x61A7) cycles:

- FS_HIGH_TIME_1: 0x19=0x0A
- FS_HIGH_TIME_0: 0x1A=0xD9
- FS_LOW_TIME_1: 0x1B=0x61
- FS_LOW_TIME_0: 0x1C=0xA7

7.4.27.2.1 Code Example for Internally Generated FrameSync

```
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x6E,0xAA) # BC_GPIO_CTL0: FrameSync signal to GPIO0/1
WriteI2C(0x10,0x91A) # FrameSync signal; Device Status; Enabled
WriteI2C(0x19,0x0A) # FS_HIGH_TIME_1
WriteI2C(0x1A,0xD9) # FS_HIGH_TIME_0
WriteI2C(0x1B,0x61) # FS_LOW_TIME_1
WriteI2C(0x1C,0xA7) # FS_LOW_TIME_0
WriteI2C(0x18,0x01) # Enable FrameSync
```

7.4.28 CSI-2 Forwarding

Video stream forwarding is handled by the forwarding control in the DS90UB936-Q1 on FWD_CTL1 register 0x20. The forwarding control pulls data from the video buffers for each FPD-Link III RX port and forwards the data to the CSI-2 output interfaces. It also handles generation of transitions between LP and HS modes as well as sending of Synchronization frames. The forwarding control monitors each of the video buffers for packet and data availability.

Forwarding from input ports may be disabled using per-port controls. Each of the forwarding engines may be configured to pull data from either of the two video buffers, although both buffer may only be assigned to one CSI-2 Transmitter at a time unless in replicate mode. The two forwarding engines operate independently.

7.4.28.1 Enabling and Disabling the CSI-2 Transmitter

When CSI-2 Transmitter is enabled in CSI_CTL register bit 0x33[0], by default the output will transition to LP11 state. Once enabled, it is typically best to leave the CSI-2 Transmitter enable, and only change the forwarding controls if changes are required to the system. When enabling and disabling the CSI-2 Transmitter, forwarding should be disabled to ensure proper start and stop of the CSI Transmitter.

When enabling and disabling the CSI-2 Transmitter, use the following sequence:

To Disable:

1. Disable forwarding for assigned ports in the FWD_CTL1 register.
2. Disable CSI periodic calibration (if enabled) in the CSI_ CTL2 register.
3. Disable continuous clock operation (if enabled) in the CSI_ CTL register.
4. Clear CSI Transmit enable in CSI_ CTL register.

To Enable:

1. Set CSI Transmit enable (and continuous clock if desired) in CSI_ CTL register.
2. Enable CSI periodic calibration (if desired) in the CSI_CTL2 register.
3. Enable forwarding for assigned ports in the FWD_CTL1 register.

7.4.28.2 Best-Effort Round Robin CSI-2 Forwarding

Best-Effort Round Robin (RR) CSI-2 Forwarding allows for combining sensor sources with different resolutions and timing to the same CSI-2 Tx output. By default, the RR forwarding of packets use standard CSI-2 method of video stream determination. No special ordering of CSI-2 packets are specified, effectively relying on the Virtual Channel Identifier (VC) and Data Type (DT) fields to distinguish video streams. Each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel are also supported in this mode.

When receiving FPD-Link RAW packets from DS90UB9x3x-Q1, each image sensor is assigned a VC-ID to identify the source. Different data types within a virtual channel is also supported in this mode.

The forwarding engine forwards packets as they become available to the forwarding engine. In the case where multiple packets may be available to transmit, the forwarding engine typically operates in an RR fashion based on the input port from which the packets are received.

Best-effort CSI-2 RR forwarding has the following characteristics and capabilities:

- Uses Virtual Channel ID to differentiate each video stream
- Separate Frame Synchronization packets for each VC
- No synchronization requirements

This mode of operation allows input RX ports to have different video characteristics and there is no requirement that the video be synchronized between ports. The attached video processor would be required to properly decode the various video streams based on the VC and DT fields.

Best-effort forwarding is enabled by setting the CSIx_RR_FWD bits in the FWD_CTL2 register 0x21.

7.4.28.3 Synchronized Forwarding

In cases with multiple input sources, synchronized forwarding offers synchronization of all incoming data stored within the buffer. If packets arrive within a certain window, the forwarding control may be programmed to attempt to synchronize the video buffer data. In this mode, it attempts to send each channel synchronization packets in order (VC0, VC1) as well as sending packet data in the same order. In the following sections, Sensor A (SA) and Sensor B (SB) refer to the sensors connected at FPD-Link III RX port 0, and RX port 1, respectively. The following describe only the 2-port operation, but single port configuration also can be applied.

The forwarding engine for the CSI-2 Transmitter can be configured to synchronize both video sources.

Requirements:

- Video arriving at input ports should be synchronized within approximately one video line period
- All enabled ports should have valid, synchronized video
- Each port must have identical video parameters, including number and size of video lines, presence of synchronization packets, and so forth.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempt to restart sending synchronized video at the next FrameStart indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Status is provided to indicate when the forwarding engine is synchronized. In addition, a flag is used to indicate that synchronization has been lost (status is cleared on a read).

Three options are available for Synchronized forwarding:

- Basic Synchronized forwarding
- Line-Interleave forwarding
- Line-Concatenated forwarding

Synchronized forwarding modes are selected by setting the CSIx_SYNC_FWD controls in the FWD_CTL2 register. To enable synchronized forwarding the following order of operations is recommended:

1. Disable Best-effort forwarding by clearing the CSIx_RR_FWD bits in the FWD_CTL2 register
2. Enable forwarding per Receive port by clearing the FWD_PORTx_DIS bits in the FWD_CTL1 register
3. Enable Synchronized forwarding in the FWD_CTL2 register

7.4.28.4 Basic Synchronized Forwarding

During Basic Synchronized Forwarding, each forwarded frame is an independent CSI-2 video frame including FrameStart (FS), video lines, and FrameEnd (FE) packets. Each forwarded stream may have a unique VC ID. If the forwarded streams do not have a unique VC-ID, the receiving process may use the frame order to differentiate the video stream packets.

The forwarding engine attempts to send the video synchronized. If synchronization fails, the CSI-2 transmitter stops forwarding packets and attempts to restart sending synchronized video at the next FS indication. Packets are discarded as long as the forwarding engine is unable to send the synchronized video.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS_A – FS_B – SA_L1 – SB_L1 SA_L2 – SB_L2 – SA_L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... SA_LN – SB_LN – FE_A – FE_B

Notes:

FS_x	FrameStart for Sensor X
FE_x	FrameEnd for Sensor X
Sx_Ly	Line Y for Sensor X video frame
Sx_LN	Last line for Sensor X video frame

Each packet includes the virtual channel ID assigned to receive port for each sensor.

7.4.28.4.1 Code Example for Basic Synchronized Forwarding

```
# Configure RX0 to map VC0 from data received on RX0 to VC0
WriteI2C(0x4C,0x01) # FPD3_PORT_SEL
WriteI2C(0x72,0xE4) # CSI_VC_MAP
#  Configure RX1 to map VC1 from data received on RX1 to VC1
WriteI2C(0x4C,0x12) # FPD3_PORT_SEL
WriteI2C(0x70,0xE5) # CSI_VC_MAP
#  Enable CSI Output and set 4 CSI lanes
WriteI2C(0x33,0x1) # CSI_CTL
#  Enable synchronized basic forwarding for output port 0
WriteI2C(0x21,0x04) # FWD_CTL2
#  Enable forwarding from RX0 and RX1
WriteI2C(0x20,0x00) # FWD_CTL1
```

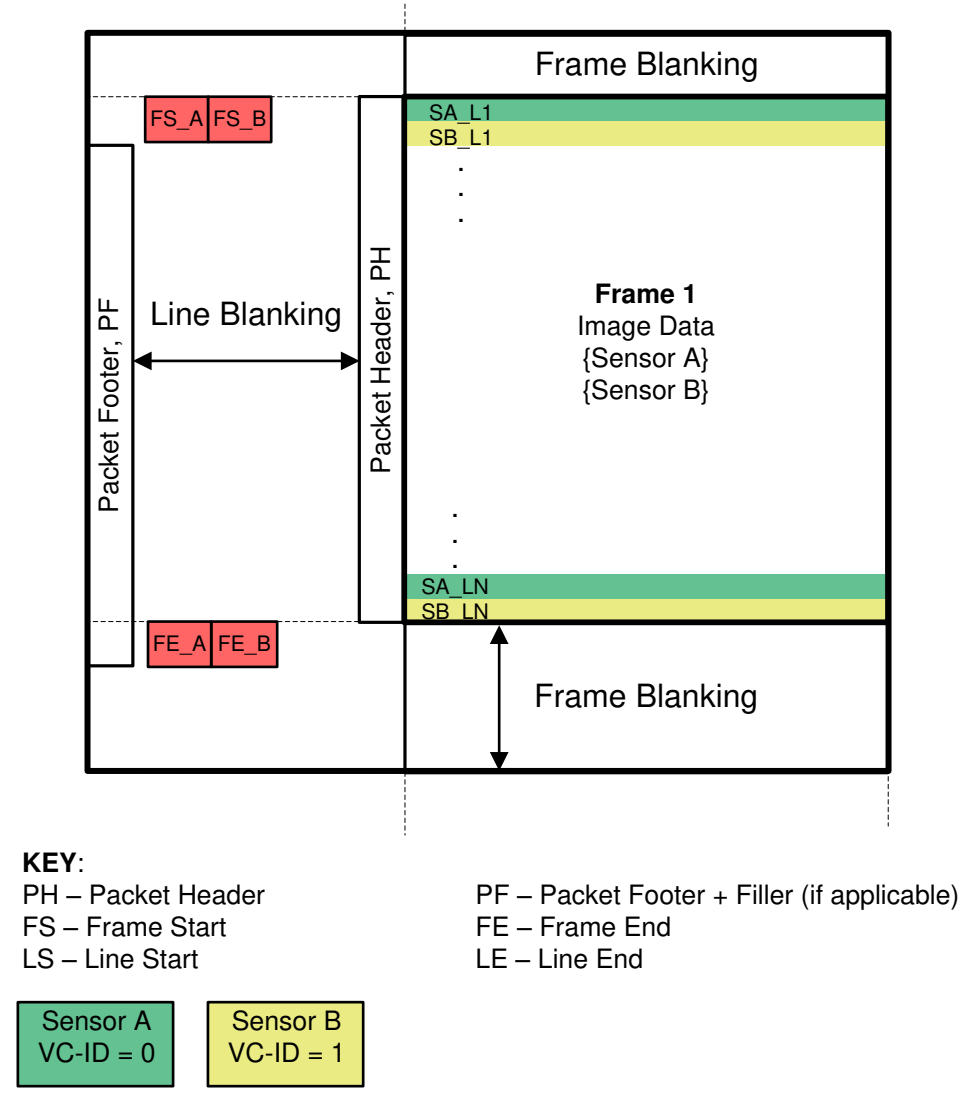


図 7-20. Basic Synchronized Format

7.4.28.5 Line-Interleave Forwarding

In synchronized forwarding, the forwarding engine may be programmed to send only one of each synchronization packet. For example, if forwarding from both input ports, only one FS and FE packet is sent for each video frame. The synchronization packets for the other port is dropped. The video line packets for each video stream are sent as individual packets. This effectively merges the frames from N video sources into a single frame that has N times the number of video lines.

In this mode, all video streams must also have the same VC, although this is not checked by the forwarding engine. This is useful when connected to a controller that does not support multiple VCs. The receiving processor must process the image based on order of video line reception.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS_A – SA_L1 – SB_L1 – SA_L2 – SB_L2 – SA_L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... SA_LN – SB_LN – FE_A

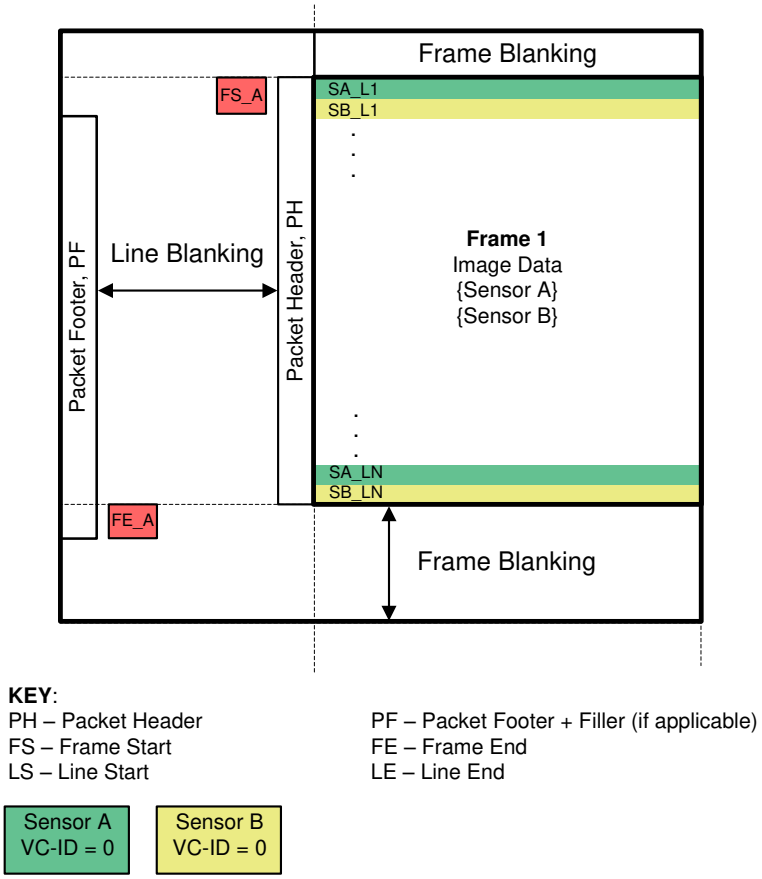
Notes:

FS_x	FrameStart for Sensor X
FE_x	FrameEnd for Sensor X
Sx_Ly	Line Y for Sensor X video frame
Sx_LN	Last line for Sensor X video frame

All packets would have the same VC ID.

7.4.28.5.1 Code Example for Line-Interleave Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x72,0xE8) # Map Sensor A VC0 to CSI-Tx VC0
# "*** RX1 VC=0 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0xE8) # Map Sensor B VC0 to CSI-Tx VC0
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line interleaving ***"
WriteI2C(0x21,0x28) # synchronous forwarding with line interleaving
#  "*** FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```



*Blanking intervals do not provide accurate synchronization timing

図 7-21. Line-Interleave Format

7.4.28.6 Line-Concatenated Forwarding

In synchronized forwarding, the forwarding engine may be programmed to merge video frames from multiple sources into a single video frame by concatenating video lines. Each of the sensors attached to each RX Port carry different data streams that get concatenated into one CSI-2 stream. For example, if forwarding from both input ports, only one FS an FE packet is sent for each video frame. The synchronization packets for the other port is dropped. In addition, the video lines from each sensor are combined into a single line. The controller must separate the single video line into the separate components based on position within the concatenated video line.

Example Synchronized traffic to CSI-2 Transmit port at start of frame:

FS_A – SA_L1,SB_L1 – SA_L2,SB_L2 – SA_L3,SB_L3 …

Example Synchronized traffic to CSI-2 Transmit port at end of frame:

... SA_LN,SB_LN – FE_A

Notes:

FS_x	FrameStart for Sensor X
FE_x	FrameEnd for Sensor X
Sx_Ly	Line Y for Sensor X video frame
Sx_LN	Last line for Sensor X video frame

SA_L1,SB_L1 indicate concatenation of the first video line from each Sensor into a single video line. This packet has a modified header and footer that matches the concatenated line data.

Packets would have the same VC ID, based on the VC ID for the lowest number Sensor port being forwarded.

Lines are concatenated on a byte basis without padding between video line data.

7.4.28.6.1 Code Example for Line-Concatenate Forwarding

```
# "*** RX0 VC=0 ***"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x72,0xE8) # Map Sensor A VC0 to CSI-Tx VC0
# "*** RX1 VC=1 ***"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x70,0xED) # Map Sensor B VC0 to CSI-Tx VC1
#  "CSI_EN"
WriteI2C(0x33,0x1) # CSI_EN & CSI0 4L
# "*** CSI0_SYNC_FWD synchronous forwarding with line concatenation ***"
WriteI2C(0x21,0x3c) # synchronous forwarding with line concatenation
#  "***FWD_PORT all RX to CSI0"
WriteI2C(0x20,0x00) # forwarding of all RX to CSI0
```

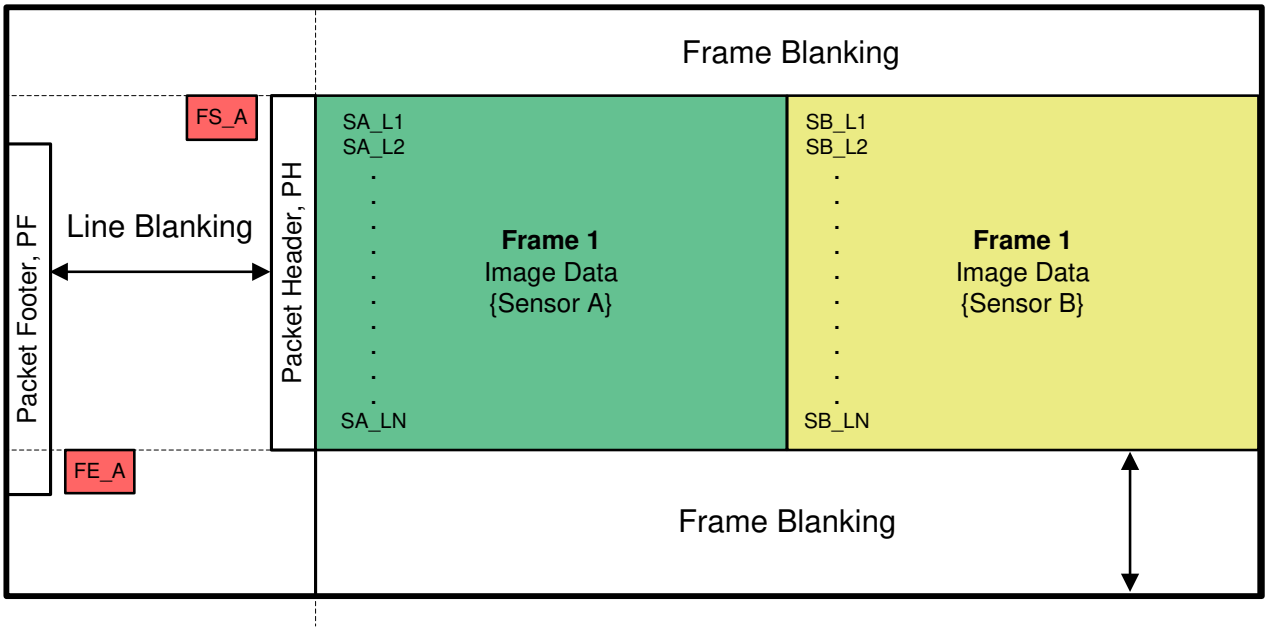


図 7-22. Line-Concatenated Format

7.5 Programming

7.5.1 Serial Control Bus and Bidirectional Control Channel

The DS90UB936-Q1 implements an I2C-compatible serial control bus. The I2C is for local device configuration and incorporates a Bidirectional Control Channel (BCC) that allows communication across the FPD-Link cable with remote serializers as well as remote I2C target devices. The DS90UB936-Q1 implements an I2C compatible target capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation. This allows I2C operation at up to 1-MHz clock frequencies. When paired with a DS90UB935-Q1 serializer the DS90UB936-Q1 supports combined format I2C read and write access. When paired with the DS90UB933-Q1 or DS90UB913A-Q1 serializers, all I2C remote writes must be terminated with a STOP rather than repeated START. The timing for the I2C interface is detailed in 図 6-4.

For accesses to local registers, the I2C Target operates without stretching the clock. Accesses to remote devices over the Bidirectional Control Channel results in clock stretching to allow for response time across the link. The DS90UB936-Q1 can also act as I2C Controller for regenerating Bidirectional Control Channel accesses originating from the remote devices across FPD-Link. Set I2C_CONTROLLER_EN in register 0x02[5] = 1 to enable the proxy controller functionality of the deserializer.

7.5.1.1 Bidirectional Control

The Bidirectional Control Channel (BCC) supports higher frequency operation when attached to the DS90UB935-Q1 and is also backward compatible with the DS90UB933-Q1 or DS90UB913A-Q1 serializers. The Bidirectional Control Channel is compatible with I2C devices, allowing local I2C target access to device registers as well as bidirectional I2C operation across the link to the Serializer and attached devices. I2C access should not be attempted across the link when Rx Port Lock status is Low. In addition to providing BCC operation, the back channel signaling also supports GPIO operations and advertising device capabilities to the attached Serializer device. The default back channel frequency is selected by the strap setting of the MODE pin. Additional speeds are also available, controlled separately for each Rx Port through the BC_FREQ_SELECT register field in the BCC_CONFIG register 0x58. Back channel frequency operates in 50-Mbps and 2.5-Mbps modes to support DS90UB935-Q1, and DS90UB933-Q1 or DS90UB913A-Q1 Serializers.

7.5.1.2 Device Address

The primary device address is set through a resistor divider (R_{HIGH} and R_{LOW} — see 図 7-23 below) connected to the IDX pin. **Note that the voltage of V_{I2C} must match the voltage of V_{VDDIO}.** The DS90UB936-Q1 waits 1 ms after PDB goes high to allow time for power supply transients before sampling the IDX value and configuring the device to set the I2C address. The primary I2C target address is stored in the I2C Device ID register at address 0x0. In addition to the primary I2C target address, the DS90UB936-Q1 may be programmed to respond to up to 2 other I2C addresses. The two RX Port ID addresses provide direct access to the Receive Port 0 and Por1 registers without needing to set the paging controls normally required to access the port registers. In addition, these Rx port assigned I2C IDs also allow access to the shared registers in the same manner as the primary I2C target address. The I2C_RX0_ID and I2C_RX1_ID, registers are located in register address 0xF8 and 0xF9, respectively.

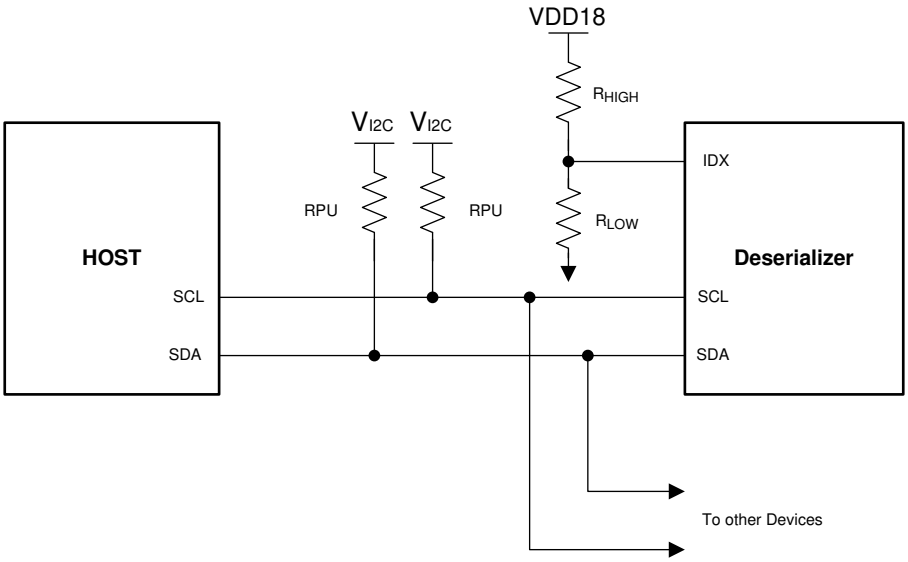


図 7-23. Serial Control Bus Connection

The IDX pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDX input pin (V_{IDX}) and $V_{(VDD18)}$, each ratio corresponding to a specific device address. See 表 7-15, Serial Control Bus Addresses for IDX.

表 7-15. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	(V); VDD1P8 = 1.80V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0x3D	0x7A

7.5.1.3 Basic I2C Serial Bus Operation

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to 1.8-V or 3.3-V nominal V_{I2C}. For most applications, TI recommends a 4.7-kΩ pullup resistor to V_{I2C}. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High or driven Low.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See 図 7-24.

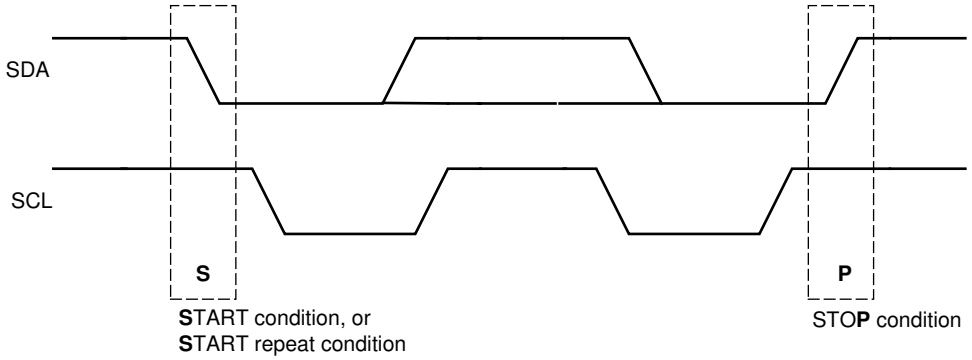


図 7-24. START and STOP Conditions

To communicate with a target device, the host controller (controller) sends the target address and listens for a response from the target. This response is referred to as an acknowledge bit (ACK). If a target on the bus is addressed correctly, it acknowledges (ACKs) the controller by driving the SDA bus low. If the address does not match the target address of the device, it not-acknowledges (NACKs) the controller by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the controller is writing data, the target ACKs after every data byte is successfully received. When the controller is reading data, the controller ACKs after every data byte is received to let the target know it wants to receive another data byte. When the controller wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in 図 7-25 and a WRITE is shown in 図 7-26.

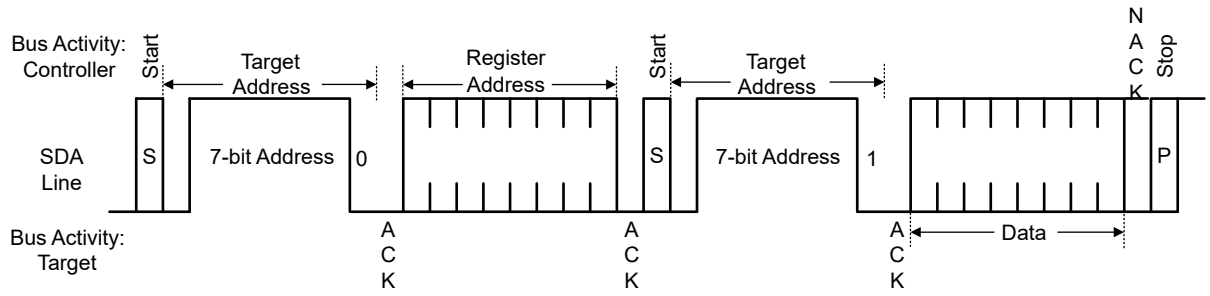


図 7-25. Serial Control Bus — READ

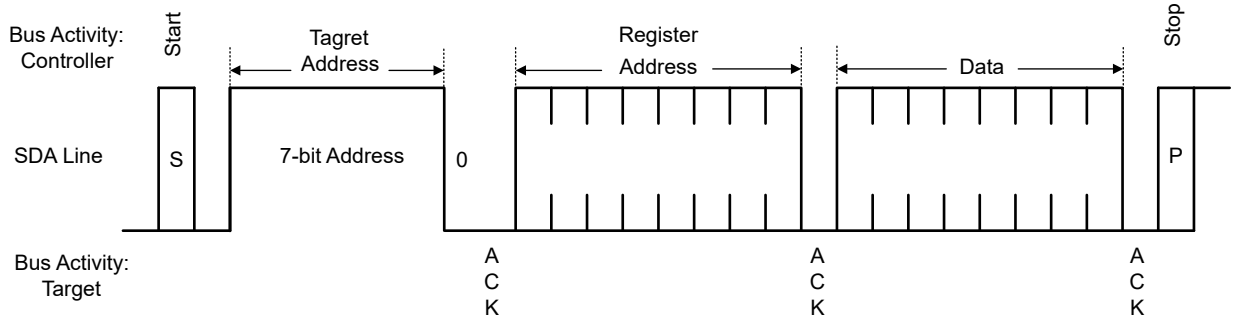


図 7-26. Serial Control Bus — WRITE

For more information on I2C interface requirements and throughput considerations, refer to *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131) and *I2C Over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222).

7.5.2 I2C Target Operation

The DS90UB936-Q1 implements an I2C-compatible target capable of operation compliant to the Standard, Fast, and Fast-plus modes of operation allowing I2C operation at up to 1-MHz clock frequencies. Local I2C

transactions to access DS90UB936-Q1 registers can be conducted 2 ms after power supplies are stable and PDB is brought high. For accesses to local registers, the I2C Target operates without stretching the clock. The primary I2C target address is set through the IDx pin. The primary I2C target address is stored in the I2C Device ID register at address 0x0. In addition to the primary I2C target address, the DS90UB936-Q1 may be programmed to respond to up to two other I2C addresses. The two RX Port ID addresses provide direct access to the Receive Port registers without needing to set the paging controls normally required to access the port registers.

7.5.3 Remote Target Operation

The Bidirectional control channel provides a mechanism to read or write I2C registers in remote devices over the FPD-Link III interface. The I2C Controller located at the Deserializer must support I2C clock stretching. Accesses to serializer or remote target devices over the Bidirectional Control Channel will result in clock stretching to allow for response time across the link. The DS90UB936-Q1 acts as an I2C target on the local bus, forwards read and write requests to the remote device, and returns the response from the remote device to the local I2C bus. To allow for the propagation and regeneration of the I2C transaction at the remote device, the DS90UB936-Q1 will stretch the I2C clock while waiting for the remote response. To communicate with a remote target device, the Rx Port which is intended for messaging also must be selected in register 0x4C. The I2C address of the currently selected RX Port serializer will be populated in register 0x5B of the DS90UB936-Q1. The BCC_CONFIG register 0x58 also must have bit 6, I2C_PASS_THROUGH set to one. If enabled, local I2C transactions with valid address decode will then be forwarded through the Bidirectional Control Channel to the remote I2C bus. When I2C PASS THROUGH is set, the deserializer will only propagate messages that the DS90UB936-Q1 recognizes, such as the registered serializer alias address (SER ALIAS), or any registered remote target alias attached to the serializer I2C bus (TARGET ALIAS) assigned to the specific Rx Port0 or Port 1. Setting PASS THROUGH ALL and AUTO ACK are less common use cases and primarily used for debugging I2C messaging as they will respectively pass all addresses regardless of valid I2C address (PASS_THROUGH_ALL) and acknowledge all I2C commands without waiting for a response from serializer (AUTO_ACK).

7.5.3.1 Remote I^2C Targets Data Throughput

Since the BCC buffers each I^2C data byte and regenerates the I^2C protocol on the remote side of the link, the overall I^2C throughput will be reduced. The reduction is dependent on the operating frequencies of the local and remote interfaces. The local I^2C rate is based on the host controller clock rate, while the remote rate depends on the settings for the proxy I^2C controller (SCL frequency).

For purposes of understanding the effects of the BCC on data throughput from a host controller to a remote I^2C controller, the approximate bit rate including latency timings across the control channel can be calculated by the following:

9 bits / ((Host_bit * 9) + (Remote_bit * 9) + FCdelay + BCCdelay)

Example of DS90UB935/936 chipset:

For the 100 kbit/s (100 kHz) :

Host_bit = 10us (100 kHz)

Remote_bit = 13.5us (default 74 kHz)

FCdelay = 225ns (typical value)

BCCdelay = 1.5us (typical value for 50 Mbps back channel rate)

Effective rate = 9bits / (90us + 121us + 0.225us + 1.5us) = 42.3 kbit/s

表 7-16. Typical Achievable Bit Rates

Host I2C rate	Remote I2C rate	Net bit rate
100 kbit/s	74 kbit/s (default settings)	42.3 kbit/s
400 kbit/s	100 kbit/s	78.8 kbit/s
1 Mbit/s	100 kbit/s	89.4 kbit/s
1 Mbit/s	400 kbit/s	270.88 kbit/s

表 7-16. Typical Achievable Bit Rates (continued)

Host I2C rate	Remote I2C rate	Net bit rate
1 Mbit/s	1 Mbit/s	456.27 kbit/s

Since the I2C protocol includes overhead for sending address information as well as START and STOP bits, the actual data throughput depends on the size and type of transactions used. Use of large bursts to read and write data will result in higher data transfer rates.

7.5.4 Remote Target Addressing

Various system use cases require multiple sensor devices with the same fixed I2C target address to be remotely accessible from the same I2C bus at the deserialilzer. The DS90UB936-Q1 provides target ID virtual addressing to differentiate target target addresses when connecting two or more remote devices. Eight pairs of TargetAlias and TargetID registers are allocated for each FPD-Link III Receive port in registers 0x5C through 0x6C. The TargetAlias register allows programming a virtual address which the host controller uses to access the remote device. The TargetID register provides the actual target address for the device on the remote I2C bus. Since eight pairs of registers are available for each port (total of 16 pairs), multiple devices may be directly accessible remotely without need for reprogramming. Multiple TargetAlias can be assigned to the same TargetID as well.

7.5.5 Broadcast Write to Remote Target Devices

The DS90UB936-Q1 provides a mechanism to broadcast I2C writes to remote devices (either remote targets or serializers). For each Receive port, the TargetID and TargetAlias register pairs would be programmed with the same TargetAlias value so they would each respond to the local I2C access. The TargetID value would match the intended remote device address, either remote target or serializers. For each receive port, on of the TargetAlias registers is set with an Alias value. For each port, the TargetID value is set to the address of the remote device. These values may be the same. To access the remote serializer registers rather than a remote target, the serializer ID (SER_IDX or SER_IDY) would be used as the TargetID value.

7.5.5.1 Code Example for Broadcast Write

```
#  "FPD3_PORT_SEL Boardcast RX0/1"
WriteI2C(0x4c,0x0f) # RX_PORT0 read; RX0/1 write
#  "enable pass through"
WriteI2C(0x58,0x58) # enable pass through
WriteI2C(0x5c,0x18) # "SER_ALIAS_ID"
WriteI2C(0x5d,0x60) # "TargetID[0]"
WriteI2C(0x65,0x60) # "TargetAlias[0]"
WriteI2C(0x7c,0x01) # "FV_POLARITY"
WriteI2C(0x70,0x1f) # RAW10_datatype_yuv422b10_VC0
```

7.5.6 I2C Controller Proxy

The DS90UB936-Q1 implements an I2C controller that acts as a proxy controller to regenerate I2C accesses originating from a remote serializer (DS90UB935-Q1, DS90UB933-Q1, DS90UB913A-Q1). By default, the I2C Controller Enable bit (I2C_CONTROLLER_EN) in register 0x05[2]= 0 to block Controller access to local deserialilzer I2C from remote serializers. Set I2C_CONTROLLER_EN] = 1 if system requires the deserializer to act as proxy controller for remote serializers on the local deserializer I2C bus. The proxy controller is an I2C compatible controller, capable of operating with Standard-mode, Fast-mode, or Fast-mode Plus I2C timing. It is also capable of arbitration with other controllers, allowing multiple controllers and targets to exist on the I2C bus. A separate I2C proxy controller is implemented for each Receive port. This allows independent operation for all sources to the I2C interface. Arbitration between multiple sources is handled automatically using I2C multi-controller arbitration.

7.5.7 I2C Controller Proxy Timing

The proxy controller timing parameters are based on the REFCLK timing. Timing accuracy for the I2C proxy controller based on the REFCLK or XTL clock source attached to the DS90UB936-Q1 deserializer. Before REFCLK is applied the deserializer will default to internal reference clock with accuracy of 25 MHz ±10%.The I2C Controller regenerates the I2C read or write access using timing controls in the registers 0xA and 0xB to

regenerate the clock and data signals to meet the desired I2C timing in standard, fast, or fast-plus modes of operation.

I2C Controller SCL High Time is set in register 0x0A[7:0]. This field configures the high pulse width of the SCL output when the Serializer is the Controller on the local deserializer I2C bus. The default value is set to provide a minimum 5-µs SCL high time with the reference clock at 25 MHz + 100 ppm including four additional oscillator clock periods or synchronization and response time. Units are 40 ns for the nominal oscillator clock frequency, giving Min_delay = 40 ns × (SCL_HIGH_TIME + 4).

I2C Controller SCL Low Time is set in register 0x0B[7:0]. This field configures the low pulse width of the SCL output when the Serializer is the Controller on the local deserializer I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the BiDirectional Control Channel. The default value is set to provide a minimum 5-µs SCL high time with the reference clock at 25 MHz + 100 ppm including four additional oscillator clock periods or synchronization and response time. Units are 40 ns for the nominal oscillator clock frequency, giving Min_delay = 40 ns × (SCL_HIGH_TIME + 4). See 表 7-17 example settings for Standard mode, Fast mode, and Fast Mode Plus timing.

表 7-17. Typical I2C Timing Register Settings

I2C MODE	SCL HIGH TIME		SCL LOW TIME	
	0x0A[7:0]	NOMINAL DELAY AT REFCLK = 25 MHz	0x0B[7:0]	NOMINAL DELAY AT REFCLK = 25 MHz
Standard	0x7A	5.04 us	0x7A	5.04 us
Fast	0x13	0.920 us	0x25	1.64 us
Fast - Plus	0x06	0.400 us	0x0C	0.640 us

7.5.7.1 Code Example for Configuring Fast Mode Plus I2C Operation

```
#  "RX0 I2C Controller Fast Plus Configuration"
WriteI2C(0x02,0x3E) # Enable Proxy
WriteI2C(0x4c,0x01) # Select RX_PORT0
# Set SCL High and Low Time delays
WriteI2C(0x0a,0x06) # SCL High
WriteI2C(0x0b,0x0C) # SCL Low
```

7.5.8 Interrupt Support

Interrupts can be brought out on the INTB pin as controlled by the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers. The main interrupt control registers provide control and status for interrupts from the individual sources. Sources include each of the two FPD-Link III Receive ports as well as the CSI-2 Transmit port. Clearing interrupt conditions requires reading the associated status register for the source. The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

The DS90UB936-Q1 devices have built in flexibility such that the main interrupt may be brought to any GPIO pin through the GPIOx_PIN_CTL register for that pin (see *表 7-35*). Note that the GPIO3 pin is the only GPIO that is implemented as open-drain, so this is the preferred pin for signaling the interrupt.

For an interrupt to be generated based on one of the interrupt status assertions, both the individual interrupt enable and the INT_EN control must be set in the INTERRUPT_CTL 0x23 register. For example, to generate an interrupt if IS_RX0 is set, both the IE_RX0 and INT_EN bits must be set. If IE_RX0 is set but INT_EN is not, the INT status is indicated in the INTERRUPT_STS register, and the INTB pin does not indicate the interrupt condition.

See the INTERRUPT_CTL 0x23 and INTERRUPT_STS 0x24 registers for details.

7.5.8.1 Code Example to Enable Interrupts

```
#  "RX0/1 INTERRUPT_CTL enable"
WriteI2C(0x23,0xBF) # RX all & INTB PIN EN
# Individual RX0/1 INTERRUPT_CTL enable
# "RX0 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x01) # RX0
WriteI2C(0x23,0x81) # RX0 & INTB PIN EN
# "RX1 INTERRUPT_CTL enable"
WriteI2C(0x4C,0x12) # RX1
WriteI2C(0x23,0x82) # RX1 & INTB PIN EN
```

7.5.8.2 FPD-Link III Receive Port Interrupts

For each FPD-Link III Receive port, multiple options are available for generating interrupts. Interrupt generation is controlled through the PORT_ICR_HI 0xD8 and PORT_ICR_LO 0xD9 registers. In addition, the PORT_ISR_HI 0xDA and PORT_ISR_LO 0xDB registers provide read-only status for the interrupts. Clearing of interrupt conditions is handled by reading the RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS registers. The status bits in the PORT_ISR_HI/LO registers are copies of the associated bits in the main status registers.

To enable interrupts from one of the Receive port interrupt sources:

1. Enable the interrupt source by setting the appropriate interrupt enable bit in the PORT_ICR_HI or PORT_ICR_LO register
2. Set the RX Port X Interrupt control bit (IE_RXx) in the INTERRUPT_CTL register
3. Set the INT_EN bit in the INTERRUPT_CTL register to allow the interrupt to assert the INTB pin low

To clear interrupts from one of the Receive port interrupt sources:

1. (optional) Read the INTERRUPT_STS register to determine which RX Port caused the interrupt
2. (optional) Read the PORT_ISR_HI and PORT_ISR_LO registers to determine source of interrupt
3. Read the appropriate RX_PORT_STS1, RX_PORT_STS2, or CSI_RX_STS register to clear the interrupt.

The first two steps are optional. The interrupt could be determined and cleared by just reading the status registers.

7.5.8.2.1 Interrupts on Forward Channel GPIO

When connected to the DS90UB935-Q1 serializer, interrupts can be generated on changes in any of the four forward channel GPIOs per port. Interrupts are enabled by setting bits in the FC_GPIO_ICR register. Interrupts may be generated on rising and/or falling transitions on the GPIO signal. The GPIO interrupt status is cleared by reading the FC_GPIO_STS register.

Interrupts should only be used for GPIO signals operating at less than 10 MHz. High or low pulses that are less than 100 ns might not be detected at the DS90UB936-Q1. To avoid false interrupt indications, the interrupts should not be enabled until after the Forward Channel GPIOs are enabled at the serializer.

7.5.8.2.2 Interrupts on Change in Sensor Status

The FPD-Link III Receiver recovers 32-bits of Sensor status from the attached DS90UB935-Q1 serializer. Interrupts may be generated based on changes in the Sensor Status values received from the forward channel. The Sensor Status consists of 4 bytes of data, which may be read from the SENSOR_STS_x registers for each Receive port. Interrupts may be generated based on a change in any of the bits in the first byte (SENSOR_STS_0). Each bit can be individually masked for Rising and/or Falling interrupts.

Two registers control the interrupt masks for the SENSOR_STS bits: SEN_INT_RISE_CTL and SEN_INT_FALL_CTL.

Two registers provide interrupt status: SEN_INT_RISE_STS, SEN_INT_FALL_STS.

If a mask bit is set, a change in the associated SENSOR_STS_0 bit will be detected and latched in the SEN_INT_RISE_STS or SEN_INT_FALL_STS registers. If the mask bit is not set, the associated interrupt status bit will always be 0. If any of the SEN_INT_RISE_STS or SEN_INT_FALL_STS bits is set, the IS_FC_SEN_STS bit will be set in the PORT_ISR_HI register.

7.5.8.3 Code Example to Readback Interrupts

```
INTERRUPT_STS = ReadI2C(0x24) # 0x24 INTERRUPT_STS
if ((INTERRUPT_STS & 0x80) >> 7):
    print "# GLOBAL INTERRUPT DETECTED "
if ((INTERRUPT_STS & 0x40) >> 6):
    print "# RESERVED "
if ((INTERRUPT_STS & 0x10) >> 4):
    print "# IS_CSI_TX DETECTED "
if ((INTERRUPT_STS & 0x02) >> 1):
    print "# IS_RX1 DETECTED "
if ((INTERRUPT_STS & 0x01) ):
    print "# IS_RX0 DETECTED "
# "################################################"
#  "RX0 status"
# "################################################"
WriteReg(0x4C,0x01) # RX0
PORT_ISR_LO = ReadI2C(0xDB)
print "0xDB PORT_ISR_LO : ", hex(PORT_ISR_LO) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
###############################################
PORT_ISR_HI = ReadI2C(0xDA)
print "0xDA PORT_ISR_HI : ", hex(PORT_ISR_HI) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
###############################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
###############################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
```

```
    print "# CABLE_FAULT DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
##############################################
# "################################################"
#  "RX1 status"
# "################################################"
WriteReg(0x4C,0x12) # RX1
PORT_ISR_LO = ReadI2C(0xDB) # PORT_ISR_LO readout; cleared by RX_PORT_STS2
if ((PORT_ISR_LO & 0x40) >> 6):
    print "# IS_LINE_LEN_CHG INTERRUPT DETECTED "
if ((PORT_ISR_LO & 0x20) >> 5):
    print "# IS_LINE_CNT_CHG DETECTED "
if ((PORT_ISR_LO & 0x10) >> 4):
    print "# IS_BUFFER_ERR DETECTED "
if ((PORT_ISR_LO & 0x08) >> 3):
    print "# IS_CSI_RX_ERR DETECTED "
if ((PORT_ISR_LO & 0x04) >> 2):
    print "# IS_FPD3_PAR_ERR DETECTED "
if ((PORT_ISR_LO & 0x02) >> 1):
    print "# IS_PORT_PASS DETECTED "
if ((PORT_ISR_LO & 0x01) ) :
    print "# IS_LOCK_STS DETECTED "
##############################################
PORT_ISR_HI = ReadI2C(0xDA) # readout; cleared by RX_PORT_STS2
if ((PORT_ISR_HI & 0x04) >> 2):
    print "# IS_FPD3_ENC_ERR DETECTED "
if ((PORT_ISR_HI & 0x02) >> 1):
    print "# IS_BCC_SEQ_ERR DETECTED "
if ((PORT_ISR_HI & 0x01) ) :
    print "# IS_BCC_CRC_ERR DETECTED "
##############################################
RX_PORT_STS1 = ReadI2C(0x4D) # R/COR
if ((RX_PORT_STS1 & 0xc0) >> 6) == 1:
    print "# RX_PORT_NUM = RX1"
elif ((RX_PORT_STS1 & 0xc0) >> 6) == 0:
    print "# RX_PORT_NUM = RX0"

if ((RX_PORT_STS1 & 0x20) >> 5):
    print "# BCC_CRC_ERR DETECTED "
if ((RX_PORT_STS1 & 0x10) >> 4):
    print "# LOCK_STS_CHG DETECTED "
if ((RX_PORT_STS1 & 0x08) >> 3):
    print "# BCC_SEQ_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x04) >> 2):
    print "# PARITY_ERROR DETECTED "
if ((RX_PORT_STS1 & 0x02) >> 1):
    print "# PORT_PASS=1 "
if ((RX_PORT_STS1 & 0x01) ):
    print "# LOCK_STS=1 "
##############################################
RX_PORT_STS2 = ReadI2C(0x4E)
if ((RX_PORT_STS2 & 0x80) >> 7):
    print "# LINE_LEN_UNSTABLE DETECTED "
if ((RX_PORT_STS2 & 0x40) >> 6):
    print "# LINE_LEN_CHG "
if ((RX_PORT_STS2 & 0x20) >> 5):
    print "# FPD3_ENCODE_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x10) >> 4):
    print "# BUFFER_ERROR DETECTED "
if ((RX_PORT_STS2 & 0x08) >> 3):
    print "# CSI_ERR DETECTED "
if ((RX_PORT_STS2 & 0x04) >> 2):
    print "# FREQ_STABLE DETECTED "
if ((RX_PORT_STS2 & 0x02) >> 1):
    print "# CABLE_FAULT DETECTED "
if ((RX_PORT_STS2 & 0x01) ):
    print "# LINE_CNT_CHG DETECTED "
##############################################
```

7.5.8.4 CSI-2 Transmit Port Interrupts

The following interrupts are available for each CSI-2 Transmit Port:

- Pass indication
- Synchronized status

- Deassertion of Pass indication for an input port assigned to the CSI-2 TX Port
- Loss of Synchronization between input video streams
- RX Port Interrupt – interrupts from RX Ports mapped to this CSI-2 Transmit port

See the CSI_TX_ICR address 0x36 and CSI_TX_ISR address 0x37 registers for details.

The setting of the individual interrupt status bits is not dependent on the related interrupt enable controls. The interrupt enable controls whether an interrupt is generated based on the condition, but does not prevent the interrupt status assertion.

7.5.9 Error Handling

In the DS90UB936-Q1, the FPD-Link III receiver transfers incoming video frames to internal video buffers for forwarding to the CSI-2 Transmit ports. When the DS90UB936-Q1 detects an error condition the standard operation would be to flag this error condition and truncate sending the CSI-2 frame to avoid sending corrupted data downstream. When the DS90UB936-Q1 recovers from an error condition, it will provide Start of Frame and resume sending valid data. Consequently, when the downstream CSI-2 input receives a repeated Start of Frame condition, this will indicate that the data received in between the prior start of frame is suspect and the signal processor can then discard the suspected data. The settings in registers PORT_CONFIG2 (0x7C) and PORT_PASS_CTL (0x7D) can be used to change how the 936 handles errors when passing video frames. The receive ports may be configured to qualify the incoming video, providing a status indication and preventing forwarding of video frames until certain error free conditions are met. The Pass indication may be used to prevent forwarding packets to the internal video buffers by setting the PASS_DISCARD_EN bit in the PORT_PASS_CTL register. When this bit is set, video input will be discarded until the Pass signal indicates valid receive data. The Receive port will indicate Pass status once specific conditions are met including a number of valid frames received. Valid frames may include requiring no FPD-Link III Parity errors and consistent frame size including video line length and/or number of video lines.

In addition, the Receive port may be programmed to truncate video frames containing errors or prevent the forwarding of video until the Pass conditions are met. Register settings in PORT_CONFIG2 register 0x7C can be used to truncate frames on different line/frame sizes or a CSI-2 parity error is detected. When the deserializer truncates frames in cases of different line/frame sizes different line/frame sizes, the video frame will stop immediately with no frame end packet. Often the condition will not be cleared until the next valid frame is received.

The Rx Port PASS indication may be used to prevent forwarding packets to the internal video buffers by setting the PASS_DISCARD_EN bit in the PORT_PASS_CTL register 0x7D. When this bit is set, video input will be discarded until the Pass signal indicates valid receive data. The incoming video frames may be truncated based on error conditions or change in video line size or number of lines. These functions are controlled by bits in the PORT_CONFIG2 register. When truncating video frames, the video frame may be truncated after sending any number of video lines. A truncated frame will not send a Frame End packet to the CSI-2 Transmit port.

7.5.9.1 Receive Frame Threshold

The FPD-Link III Receiver may be programmed to require a specified number of valid video frames prior to indicating a Pass condition and forwarding video frames. The number of required valid video frames is programmable through the PASS_THRESH field in the PORT_PASS_CTL register 0x7D (表 7-135). The threshold can be programmed from 0 to 3 video frames. If set to 0, Pass will typically be indicated as soon as the FPD-Link III Receiver reports Lock to the incoming signal. If set greater than 0, the Receiver will require that number of valid frames before indicating Pass. Determination of valid frames will be dependent on the control bits in the PORT_PASS_CTL register. In the case of a Parity Error, when PASS_PARITY_ERR is set to 1 forwarding will be enabled one frame early. To ensure at least one good frame occurs following a parity error the counter should be set to 2 or higher when PASS_PARITY_ERR = 1.

7.5.9.2 Port PASS Control

When the PASS_LINE_SIZE control is set in the PORT_PASS_CTL register, the Receiver will qualify received frames based on having a consistent video line size. For PASS_LINE_SIZE to be clear, the deserializer checks that the received line length remains consistent during the frame and between frames. For each video line, the length (in bytes) will be determined. If it varies then we will flag this condition. Each video line in the packet must

be the same size, and the line size must be consistent across video frames. A change in video line size will restart the valid frame counter.

When the PASS_LINE_CNT control is set in the PORT_PASS_CTL register, the Receiver will qualify received frames based on having a consistent frame size in number of lines. A change in number of video lines will restart the valid frame counter.

When the PASS_PARITY_ERR control is set in the PORT_PASS_CTL register, the Receiver will clear the Pass indication on receipt of a parity error on the FPD-Link III interface. The valid frame counter will also be cleared on the parity error event. When PASS_PARITY_ERR is set to 1, TI also recommends setting PASS_THRESHOLD to 2 or higher to ensure at least one good frame occurs following a parity error.

7.5.10 Timestamp – Video Skew Detection

The DS90UB936-Q1 implements logic to detect skew between video signaling from attached Sensors. For each input port, the DS90UB936-Q1 provides the ability to capture a timestamp for both a start-of-frame and start-of-line event. Comparison of timestamps can provide information on the relative skew between the ports. Start-of-frame timestamps are generated at the active edge of the Vertical Sync signal in Raw mode. Start-of-line timestamps are generated at the start of reception of the Nth line of video data after the start-of-frame for either mode of operation. The function does not use the Line Start (LS) packet or Horizontal Sync controls to determine the start of lines. Timestamp operation is not supported if multiple video streams (Virtual Channels) are present on a single Rx port.

The skew detection can run in either a FrameSync mode or free-run mode.

Skew detection can be individually enabled for each RX port.

For start-of-line timestamps, a line number must be programmed. The same line number is used for all channels. Prior to reading timestamps, the TS_FREEZE bit for each port that will be read should be set. This will prevent overwrite of the timestamps by the detection circuit until all timestamps have been read. The freeze condition will be released automatically once all frozen timestamps have been read. The freeze bits can also be cleared if it does not read all the timestamp values.

The TS_STATUS register includes the following:

- Flags to indicate multiple start-of-frame per FrameSync period
- Flag to indicate Timestamps Ready
- Flags to indicate Timestamps valid (per port) – if ports are not synchronized, all ports may not indicate valid timestamps

The Timestamp Ready flag will be cleared when the TS_FREEZE bit is cleared.

7.5.11 Pattern Generation

The DS90UB936-Q1 supports an internal pattern generation feature to provide a simple way to generate video test patterns for the CSI-2 transmitter outputs. Two types of patterns are supported: Reference Color Bar pattern and Fixed Color patterns and accessed by the Pattern Generator page 0 in the indirect register set.

Prior to enabling the Packet Generator, the following should be done:

1. Disable video forwarding by setting bits [5:4] of the FWD_CTL1 register (that is, set register 0x20 to 0x30).

2. Configure CSI-2 Transmitter operating speed using the CSI_PLL_CTL register.

3. Enable the CSI-2 Transmitter for port 0 using the CSI_CTL register

7.5.11.1 Reference Color Bar Pattern

The Reference Color Bar Patterns are based on the pattern defined in Appendix D of the mipi_CTS_for_D-PHY_v1-1_r03 specification. The pattern is an eight color bar pattern designed to provide high, low, and medium frequency outputs on the CSI-2 transmit data lanes.

The CSI-2 Reference pattern provides eight color bars by default with the following byte data for the color bars: X bytes of 0xAA (high-frequency pattern, inverted) X bytes of 0x33 (mid-frequency pattern) X bytes of 0xF0 (low-

frequency pattern, inverted) X bytes of 0x7F (lone 0 pattern) X bytes of 0x55 (high-frequency pattern) X bytes of 0xCC (mid-frequency pattern, inverted) X bytes of 0x0F (low-frequency pattern) Y bytes of 0x80 (lone 1 pattern) In most cases, Y will be the same as X. For certain data types, the last color bar may need to be larger than the others to properly fill the video line dimensions.

The Pattern Generator is programmable with the following options:

- Number of color bars (1, 2, 4, or 8)
- Number of bytes per line
- Number of bytes per color bar
- CSI-2 DataType field and VC-ID
- Number of active video lines per frame
- Number of total lines per frame (active plus blanking)
- Line period (possibly program in units of 10 ns)
- Vertical front porch – number of blank lines prior to FrameEnd packet
- Vertical back porch – number of blank lines following FrameStart packet

The pattern generator relies on proper programming by software to ensure the color bar widths are set to multiples of the block (or word) size required for the specified DataType. For example, for RGB888, the block size is 3 bytes which also matches the pixel size. In this case, the number of bytes per color bar must be a multiple of 3. The Pattern Generator is implemented in the CSI-2 Transmit clock domain, providing the pattern directly to the CSI-2 Transmitter. The circuit generates the CSI-2 formatted data.

7.5.11.2 Fixed Color Patterns

When programmed for Fixed Color Pattern mode, Pattern Generator can generate a video image with a programmable fixed data pattern. The basic programming fields for image dimensions are the same as used with the Color Bar Patterns. When sending Fixed Color Patterns, the color bar controls allow alternating between the fixed pattern data and the bit-wise inverse of the fixed pattern data.

The Fixed Color patterns assume a fixed block size for the byte pattern to be sent. The block size is programmable through the register and is designed to support most 8-bit, 10-bit, and 12-bit pixel formats. The block size should be set based on the pixel size converted to blocks that are an integer multiple of bytes. For example, an RGB888 pattern would consist of 3-byte pixels and therefore require a 3-byte block size. A 2x12-bit pixel image would also require 3-byte block size, while a 3x12-bit pixel image would require nine bytes (two pixels) to send an integer number of bytes. Sending a RAW10 pattern typically requires a 5-byte block size for four pixels, so 1x10-bit and 2x10-bit could both be sent with a 5-byte block size. For 3x10-bit, a 15-byte block size would be required.

The Fixed Color patterns support block sizes up to 16 bytes in length, allowing additional options for patterns in some conditions. For example, an RGB888 image could alternate between four different pixels by using a twelve-byte block size. An alternating black and white RGB888 image could be sent with a block size of 6-bytes and setting first three bytes to 0xFF and next three bytes to 0x00.

To support up to 16-byte block sizes, a set of sixteen registers are implemented to allow programming the value for each data byte. The line period is calculated in units of 10 ns, unless the CSI-2 mode is set to 400-Mb operation in which case the unit time dependancy is 20 ns.

7.5.11.3 Packet Generator Programming

The information in this section provides details on how to program the Pattern Generator to provide a specific color bar pattern, based on datatype, frame size, and line size.

Most basic configuration information is determined directly from the expected video frame parameters. The requirements should include the datatype, frame rate (frames per second), number of active lines per frame, number of total lines per frame (active plus blanking), and number of pixels per line.

- PGEN_ACT_LPF – Number of active lines per frame
- PGEN_TOT_LPF – Number of total lines per frame
- PGEN_LSIZE – Video line length size in bytes. Compute based on pixels per line multiplied by pixel size in bytes

- CSI-2 DataType field and VC-ID
- Optional: PGEN_VBP – Vertical back porch. This is the number of lines of vertical blanking following Frame Valid
- Optional: PGEN_VFP – Vertical front porch. This is the number of lines of vertical blanking preceding Frame Valid
- PGEN_LINE_PD – Line period in 10-ns units. Compute based on Frame Rate and total lines per frame
- PGEN_BAR_SIZE – Color bar size in bytes. Compute based on datatype and line length in bytes (see details below)

7.5.11.3.1 Determining Color Bar Size

The color bar pattern should be programmed in units of a block or word size dependent on the datatype of the video being sent. The sizes are defined in the Mipi CSI-2 specification. For example, RGB888 requires a 3-byte block size which is the same as the pixel size. RAW10 requires a 5-byte block size which is equal to 4 pixels. RAW12 requires a 3-byte block size which is equal to 2 pixels.

When programming the Pattern Generator, software should compute the required bar size in bytes based on the line size and the number of bars. For the standard eight color bar pattern, that would require the following algorithm:

- Select the desired datatype, and a valid length for that datatype (in pixels).
- Convert pixels/line to blocks/line (by dividing by the number of pixels/block, as defined in the datatype specification).
- Divide the blocks/line result by the number of color bars (8), giving blocks/bar
- Round result down to the nearest integer
- Convert blocks/bar to bytes/bar and program that value into the PGEN_BAR_SIZE register

As an alternative, the blocks/line can be computed by converting pixels/line to bytes/line and divide by bytes/block.

7.5.11.4 Code Example for Pattern Generator

```
#Patgen Fixed Colorbar 1280x720p30
WriteI2C(0x33,0x01) # CSI0 enable
WriteI2C(0xB0,0x00) # Indirect Pattern Gen Registers
WriteI2C(0xB1,0x01) # PGEN_CTL
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x02) # PGEN_CFG
WriteI2C(0xB2,0x33)
WriteI2C(0xB1,0x03) # PGEN_CSI_DI
WriteI2C(0xB2,0x24)
WriteI2C(0xB1,0x04) # PGEN_LINE_SIZE1
WriteI2C(0xB2,0x0F)
WriteI2C(0xB1,0x05) # PGEN_LINE_SIZE0
WriteI2C(0xB2,0x00)
WriteI2C(0xB1,0x06) # PGEN_BAR_SIZE1
WriteI2C(0xB2,0x01)
WriteI2C(0xB1,0x07) # PGEN_BAR_SIZE0
WriteI2C(0xB2,0xE0)
WriteI2C(0xB1,0x08) # PGEN_ACT_LPF1
WriteI2C(0xB2,0x02)
WriteI2C(0xB1,0x09) # PGEN_ACT_LPF0
WriteI2C(0xB2,0xD0)
WriteI2C(0xB1,0x0A) # PGEN_TOT_LPF1
WriteI2C(0xB2,0x04)
WriteI2C(0xB1,0x0B) # PGEN_TOT_LPF0
WriteI2C(0xB2,0x1A)
WriteI2C(0xB1,0x0C) # PGEN_LINE_PD1
WriteI2C(0xB2,0x0C)
WriteI2C(0xB1,0x0D) # PGEN_LINE_PD0
WriteI2C(0xB2,0x67)
WriteI2C(0xB1,0x0E) # PGEN_VBP
WriteI2C(0xB2,0x21)
WriteI2C(0xB1,0x0F) # PGEN_VFP
WriteI2C(0xB2,0x0A)
```

7.5.12 FPD-Link BIST Mode

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and the back channel without external data connections. The BIST mode is enabled by either applying a logic high level to the BISTEN pin or programming the BIST configuration register 0xB3. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

When BIST is activated, the DS90UB936-Q1 sends register writes to the Serializer through the Back Channel. The control channel register writes configure the Serializer for BIST mode operation. The serializer outputs a continuous stream of a pseudo-random sequence and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The LOCK, PASS and CMLOUT output functions are all available during BIST mode. While the lock indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BIST_ERR_COUNT register 0x57 for each RX port. The test may select whether the Serializer uses an external or internal clock as reference for the BIST pattern frequency.

7.5.12.1 BIST Operation Through BISTEN Pin

One method to enable BIST is by driving a logic high level on the BISTEN pin. During pin control BIST, the values on GPIO1 and GPIO0 pins will control whether the Serializer uses an external or internal clock for the BIST pattern. The values on GPIO1 and GPIO0 will be written to the Serializer register 0x14[2:1]. A value of 00 will select an external clock. A non-zero value will enable an internal clock of the frequency defined in the Serializer register 0x14. Note that when the DS90UB936-Q1 is paired with DS90UB933-Q1 or DS90UB913A-Q1, a setting of 11 may result in a frequency that is too slow for the DS90UB936-Q1 to recover. The GPIO1 and GPIO0 values are sampled at the start of BIST (when BISTEN pin transitions to high). Changing this value after BIST is enabled will not change operation. Link BIST can also be enabled by register control through the BIST Control register (address 0xB3)

7.5.12.2 BIST Operation Through Register Control

The FPD-Link III BIST is configured and enabled by programming the BIST Control register (address 0xB3). BIST pass or fail status may be brought to GPIO pins by selecting the Pass indication for each receive port using the GPIOx_PIN_CTL registers. The Pass/Fail status will be deasserted low for each data error detected on the selected port input data. In addition, it is advisable to bring the Receiver Lock status for selected ports to the GPIO pins as well. After completion of BIST, the BIST Error Counter may be read to determine if errors occurred during the test. If the DS90UB936-Q1 failed to lock to the input signal or lost lock to the input signal, the BIST Error Counter will indicate 0xFF. The maximum normal count value will be 0xFE. The SER_BIST_ACT register bit 0xD0[5] can be monitored during testing to ensure BIST is activated in the serializer.

During BIST, DS90UB936-Q1 output activity are gated by BIST_Control[7:6] (BIST_OUT_MODE[1:0]). as follows:

00 : Outputs disabled during BIST

10 : Outputs enabled during BIST

When enabling the outputs by setting BIST_OUT_MODE = 10, the CSI-2 will be inactive by default (LP11 state). To exercise the CSI-2 interface during BIST mode, it is possible to Enable Pattern Generator to send a video data pattern on the CSI-2 outputs.

The BIST clock frequency is controlled by the BIST_CLOCK_SOURCE field in the BIST Control register. This 2-bit value will be written to the Serializer register 0x14[2:1]. A value of 00 will select an external clock. A non-zero value will enable an internal clock of the frequency defined in the Serializer register 0x14. Note that when the DS90UB936-Q1 is paired with DS90UB933-Q1or DS90UB913A-Q1, a setting of 11 may result in a frequency that is too slow for the DS90UB936-Q1 to recover. The BIST_CLOCK_SOURCE field is sampled at the start of BIST. Changing this value after BIST is enabled will not change operation.

7.6 Register Maps

In the register definitions under the *TYPE* and *DEFAULT* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- (R/W)/SC = Read / Write access, Self-Clearing bit
- (R/W)/S = Read / Write access, Set based on strap pin configuration at startup
- LL = Latched Low and held until read
- LH = Latched High and held until read
- S = Set based on strap pin configuration at startup

The DS90UB936-Q1 implements the following register blocks, accessible through I2C as well as the bi-directional control channel:

- Main Registers
- FPD-Link III RX Port Registers (separate register block for each of the four RX ports)
- CSI-2 Port Registers (separate register block for each of the CSI-2 ports)

表 7-18. Main Register Map Descriptions

ADDRESS RANGE	DESCRIPTION	ADDRESS MAP	
0x00-0x31	Digital Shared Registers	Shared	
0x32-0x3A	Digital CSI-2 Tx Port Registers	Shared	
0x3B - 0x4B	Reserved	Reserved	
0x4C-0x7F	Digital RX Port Registers (paged, broadcast write allowed)	FPD3 RX Port 0 *R: 0x4C[5:4]=00* *W: 0x4C[0]=1*	FPD3 RX Port 1 *R: 0x4C[5:4]=01* *W: 0x4C[1]=1*
0x80-0xAF	Reserved	Reserved	
0xB0-0xB2	Indirect Access Registers	Shared	
0xB0-0xBF	Digital Share Registers	Shared	
0xC0-0xCF	Reserved	Reserved	
0xD0-0xDF	Digital RX Port Test Mode Registers	FPD3 RX Port 0	FPD3 RX Port 1
0xE0-0xEF	Reserved	Reserved	
0xF0-0xF5	FPD3 RX ID	Shared	
0xF8-0xFB	Port I2C Addressing	Shared	
0xF6-0xF7 0xFC-0xFF	Reserved	Reserved	

7.6.1 I2C Device ID Register

The I2C Device ID Register field always indicates the current value of the I2C ID. When bit 0 of this register is 0, this field is read-only and shows the strapped ID from device initialization after power on. When bit 0 of this register is 1, this field is read/write and can be used to assign any valid I2C ID address to the deserializer.

表 7-19. I2C Device ID (Address 0x00)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	DEVICE_ID	R/W	0x3D	7-bit I2C ID of Deserializer.
0	DES_ID	R/W	0x0	0: Device ID is from strap 1: Register I2C Device ID overrides strapped value

7.6.2 Reset Register

The Reset register allows for soft digital reset of the DS90UB936-Q1 device internal circuitry without using PDB hardware analog reset. Digital Reset 0 is recommended if desired to reset without overwriting configuration registers to default values.

表 7-20. Reset (Address 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R/W	0x00	Reserved
2	RESTART _AUTOLOAD	(R/W)/SC	0x0	Restart Auto-load Setting this bit to 1 causes a re-load of the default settings including MODE and IDX. This bit is self-clearing. Software may check for Auto-load complete by checking the CFG_INIT_DONE bit in the DEVICE_STS register.
1	DIGITAL_RESET1	(R/W)/SC	0x0	Digital Reset 1 Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation
0	DIGITAL_RESET0	(R/W)/SC	0x0	Digital Reset 0 Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

7.6.3 General Configuration Register

The general configuration register enables and disables high level block functionality.

表 7-21. General Configuration (Address 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R/W	0x0	Reserved
5	I2C_CONTROLLER _ENABLE	R/W	0x0	I2C Controller Enable. This bit must be set if system requires the deserializer to act as proxy controller for remote I2C access to the local I2C bus from remote serializers. 0: Block proxy Controller access to local I2C from remote serializers 1: Enable proxy Controller access to local I2C from remote serializers
4	OUTPUT_EN_MODE	R/W	0x1	Output Enable Mode. If set to 0, the CSI TX output port will be forced to the high-impedance state if no assigned RX ports have an active Receiver lock. If set to 1 and no assigned RX ports have an active Receiver lock the CSI TX output port will continue in normal operation and enter the LP-11 state. CSI TX operation will remain under register control via the CSI_CTL register for each port.
3	OUTPUT_ENABLE	R/W	0x1	Output Enable Control (usage dependant on Output Sleep State Select). If OUTPUT_SLEEP_STATE_SEL is set to 1 and OUTPUT_ENABLE is set to 0, the CSI TX outputs will be forced into a high impedance state.
2	OUTPUT_SLEEP _STATE _SELECT	R/W	0x1	OSS Select to control output state when LOCK is low (usage dependant on Output Enable) When OUTPUT_SLEEP _STATE _SELECT is set to 0, the CSI TX outputs will be forced into a HS-0 state.
1	RX_PARITY _CHECKER _ENABLE	R/W	0x1	FPD-Link III Parity Checker Enable 0: Disable 1: Enable
0	FORCE_REFCLK _DET	R/W	0x0	Force indication of external reference clock 0: Normal operation, reference clock detect circuit indicates the presence of an external reference clock 1: Force reference clock to be indicated present

7.6.4 Revision/Mask ID Register

Revision ID field for production silicon version can be read back from this register.

表 7-22. Revision/Mask ID (Address 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	REVISION_ID	R	0x2	Revision ID field
3:0	MASK_ID	R	0x0	Mask ID

7.6.5 DEVICE_STS Register

Device status register provides read back access to high level link diagnostics.

表 7-23. DEVICE_STS (Address 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CFG_CKSUM_STS	R	0x1	Configuration Checksum Passed. CFG_CKSUM_STS bit is set to one following initialization if the Configuration data had a valid checksum
6	CFG_INIT_DONE	R	0x1	Power-up initialization complete. CFG_INIT_DONE bit is set to one after Initialization is complete.
5	RESERVED	R	0x0	Reserved
4	REFCLK_VALID	R	0x0	REFCLK valid frequency bit indicates when a valid frequency has been detected on the REFCLK pin. 0 : Invalid frequency detected 1 : REFCLK frequency between 12MHz and 64MHz.
3	PASS	R	0x0	Device PASS status This bit indicates the PASS status for the device. The value in this register matches the indication on the PASS pin.
2	LOCK	R	0x0	Device LOCK status This bit indicates the LOCK status for the device. The value in this register matches the indication on the LOCK pin.
1:0	RESERVED	R	0x3	Reserved

7.6.6 PAR_ERR_THOLD_HI Register

For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to total value in PAR_ERR_THOLD[15:0], the PARITY_ERROR flag is set in the RX_PORT_STS1 register. PAR_ERR_THOLD_HI contains bits [15:8] of the 16 bit parity error threshold PAR_ERR_THOLD[15:0].

表 7-24. PAR_ERR_THOLD_HI (Address 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERR_THOLD_HI	R/W	0x01	FPD3 Parity Error Threshold High byte This register provides the 8 most significant bits [15:8] of the Parity Error Threshold value PAR_ERR_THOLD[15:0].

7.6.7 PAR_ERR_THOLD_LO Register

For each port, if the FPD-Link III receiver detects a number of parity errors greater than or equal to total value in PAR_ERR_THOLD[15:0], the PARITY_ERROR flag is set in the RX_PORT_STS1 register. PAR_ERR_THOLD_LO contains bits [7:0] of the 16 bit parity error threshold PAR_ERR_THOLD[15:0].

表 7-25. PAR_ERR_THOLD_LO (Address 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERR_THOLD_LO	R/W	0x0	FPD3 Parity Error Threshold Low byte This register provides the 8 least significant bits [7:0] of the Parity Error Threshold value PAR_ERR_THOLD[15:0].

7.6.8 BCC Watchdog Control Register

The BCC watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time.

表 7-26. BCC Watchdog Control (Address 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	BCC_WATCHDOG_TIMER	R/W	0x7F	Sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0x0	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

7.6.9 I2C Control 1 Register

表 7-27. I2C Control 1 (Address 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LOCAL_WRITE_DISABLE	R/W	0x0	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C controller attached to the Serializer. Setting this bit does not affect remote access to I2C targets at the Deserializer.
6:4	I2C_SDA_HOLD	R/W	0x1	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
3:0	I2C_FILTER_DEPTH	R/W	0xC	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

7.6.10 I2C Control 2 Register

表 7-28. I2C Control 2 (Address 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	SDA_OUTPUT_SETUP	R/W	0x1	Remote Ack SDA Output Setup When a Control Channel (remote) access is active, this field configures setup time from the SDA output relative to the rising edge of SCL during ACK cycles. Setting this value will increase setup time in units of 640ns. The nominal output setup time value for SDA to SCL are: 00 : 80ns 01: 720ns 10: 1400ns 11: 2080ns
3:2	SDA_OUTPUT_DELAY	R/W	0x0	SDA Output Delay This field configures additional delay on the SDA output relative to the falling edge of SCL. Setting this value increases output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00 : 240ns 01: 280ns 10: 320ns 11: 360ns
1	I2C_BUS_TIMER_SPEEDUP	R/W	0x0	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.

表 7-28. I2C Control 2 (Address 0x09) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	I2C_BUS_TIMER_DISABLE	R/W	0x0	Disable I2C Bus Watchdog Timer When enabled, the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

7.6.11 SCL High Time Register

The SCL High Time register field configures the high pulse width of the I2C SCL output when the Serializer is the Controller on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional oscillator clock periods. The internal oscillator has ±10% variation when REFCLK is not applied, which must be taken into account when setting the SCL High and Low Time registers.

表 7-29. SCL High Time (Address 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_HIGH_TIME	R/W	0x7A	I2C Controller SCL high time Default set to approximately 100 kHz when REFCLK = 25 MHz. Nominal High Time = 40 ns × (SCL HIGH TIME + 4)

7.6.12 SCL Low Time Register

The SCL Low Time register field configures the low pulse width of the SCL output when the serializer is the controller on the local I2C bus. This value is also used as the SDA setup time by the I2C Target for providing data prior to releasing SCL during accesses over the Bidirectional control channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to approximately 100 kHz with the internal oscillator clock running at nominal 25 MHz. Delay includes 4 additional oscillator clock periods. The internal oscillator has ±10% variation when REFCLK is not applied, which must be taken into account when setting the SCL High and Low Time registers.

表 7-30. SCL Low Time (Address 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SCL_LOW_TIME	R/W	0x7A	I2C SCL low time Default set to approximately 100 kHz when REFCLK = 25 MHz. Nominal low time = 40 ns × (SCL LOW TIME + 4)

7.6.13 RX_PORT_CTL Register

Receiver port control register assigns rules for lock and pass in the general status register and allows for enabling and disabling each Rx port.

表 7-31. RX_PORT_CTL (Address 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x2	Reserved
5:4	PASS_SEL	R/W	0x00	Pass Output Select Both receivers can be active at the same time. This field controls the source of the PASS output. 00: Port 0 Receiver Pass 01: Port 1 Receiver Pass 10: Any Enabled Receiver Port Pass 11: All Enabled Receiver Ports Pass This field can only be written via a local I2C controller.
3:2	LOCK_SEL	R/W	0x0	Lock Output Select Both receivers can be active at the same time. This field controls the source of the LOCK output. 00: Port 0 Receiver Lock 01: Port 1 Receiver Lock 10: Any Enabled Receiver Port Lock 11: All Enabled Receiver Ports Lock. This field can only be written via a local I2C controller.
1	PORT1_EN	R/W	0x1	Port 1 Receiver Enable 0: Disable Port 1 Receiver 1: Enable Port 1 Receiver

表 7-31. RX_PORT_CTL (Address 0x0C) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	PORT0_EN	R/W	0x1	Port 0 Receiver Enable 0: Disable Port 0 Receiver 1: Enable Port 0 Receiver

7.6.14 IO_CTL Register

表 7-32. IO_CTL (Address 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SEL3P3V	R/W	0x0	3.3V I/O Select on I2C_SCL, I2C_SDA and INTB pins. 0: 1.8V I/O Supply 1: 3.3V I/O Supply If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
6	IO_SUPPLY _MODE_OV	R/W	0x0	Override I/O Supply Mode bit 0: Detected I/O voltage level will be used for both SEL3P3V and IO_SUPPLY_MODE controls. 1: Register values written to the SEL3P3V and IO_SUPPLY_MODE fields will be used.
5:4	IO_SUPPLY_MODE	R/W	0x0	I/O Supply Mode 00: 1.8V 01: Reserved 10: Reserved 11: 3.3V If IO_SUPPLY_MODE_OV is 0, a read of this register will return the detected I/O voltage level.
3:0	RESERVED	R/W	0x9	Reserved

7.6.15 GPIO_PIN_STS Register

This register reads the current values on each of the 7 GPIO pins.

表 7-33. GPIO_PIN_STS (Address 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6:0	GPIO_STS	R	0x0	GPIO Pin High/ Low Status. Bit 6 reads GPIO6 and bit 0 reads GPIO0.

7.6.16 GPIO_INPUT_CTL Register

表 7-34. GPIO_INPUT_CTL (Address 0x0F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	GPIO6_INPUT_EN	R/W	0x1	GPIO6 Input Enable. Must be set to zero if GPIO6 is configured as an output by setting 0x16[0] = 1 0: Disabled 1: Enabled
5	GPIO5_INPUT_EN	R/W	0x1	GPIO5 Input Enable. Must be set to zero if GPIO5 is configured as an output by setting 0x15[0] = 1 0: Disabled 1: Enabled
4	GPIO4_INPUT_EN	R/W	0x1	GPIO4 Input Enable. Must be set to zero if GPIO4 is configured as an output by setting 0x14[0] = 1 0: Disabled 1: Enabled
3	GPIO3_INPUT_EN	R/W	0x1	GPIO3 Input Enable. Must be set to zero if GPIO3 is configured as an output by setting 0x13[0] = 1 0: Disabled 1: Enabled
2	GPIO2_INPUT_EN	R/W	0x1	GPIO2 Input Enable. Must be set to zero if GPIO2 is configured as an output by setting 0x12[0] = 1 0: Disabled 1: Enabled
1	GPIO1_INPUT_EN	R/W	0x1	GPIO1 Input Enable. Must be set to zero if GPIO1 is configured as an output by setting 0x11[0] = 1 0: Disabled 1: Enabled
0	GPIO0_INPUT_EN	R/W	0x1	GPIO0 Input Enable. Must be set to zero if GPIO0 is configured as an output by setting 0x10[0] = 1 0: Disabled 1: Enabled

7.6.17 GPIO0_PIN_CTL Register

表 7-35. GPIO0_PIN_CTL (Address 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO0_OUT_SEL	R/W	0x0	GPIO0 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO0_OUT_SRC	R/W	0x0	GPIO0 Output Source Select Selects output source for GPIO0 data: See 表 7-8.
1	GPIO0_OUT_VAL	R/W	0x0	GPIO0 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO0_OUT_SRC[2:0] = 100 and GPIO0_OUT_SEL[2:0] = 000.
0	GPIO0_OUT_EN	R/W	0x0	GPIO0 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[0] = 1 0: Disabled 1: Enabled

7.6.18 GPIO1_PIN_CTL Register

表 7-36. GPIO1_PIN_CTL (Address 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO1_OUT_SEL	RW	0x0	GPIO1 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO1_OUT_SRC	R/W	0x0	GPIO1 Output Source Select Selects output source for GPIO1 data: See 表 7-8.
1	GPIO1_OUT_VAL	R/W	0x0	GPIO1 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO1_OUT_SRC[2:0] = 100 and GPIO1_OUT_SEL[2:0] = 000
0	GPIO1_OUT_EN	R/W	0x0	GPIO1 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[1] = 1. 0: Disabled 1: Enabled

7.6.19 GPIO2_PIN_CTL Register

表 7-37. GPIO2_PIN_CTL (Address 0x12)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO2_OUT_SEL	R/W	0x0	GPIO2 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO2_OUT_SRC	R/W	0x0	GPIO2 Output Source Select Selects output source for GPIO2 data: See 表 7-8.
1	GPIO2_OUT_VAL	R/W	0x0	GPIO2 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO2_OUT_SRC[2:0] = 100 and GPIO2_OUT_SEL[2:0] = 00
0	GPIO2_OUT_EN	R/W	0x0	GPIO2 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[2] = 1. 0: Disabled 1: Enabled

7.6.20 GPIO3_PIN_CTL Register

表 7-38. GPIO3_PIN_CTL (Address 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO3_OUT_SEL	R/W	0x0	GPIO3 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO3_OUT_SRC	R/W	0x0	GPIO3 Output Source Select Selects output source for GPIO3 data. See 表 7-8.
1	GPIO3_OUT_VAL	R/W	0x0	GPIO3 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO3_OUT_SRC[2:0] = 100 and GPIO3_OUT_SEL[2:0] = 000
0	GPIO3_OUT_EN	R/W	0x0	GPIO3 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[3] = 1. 0: Disabled 1: Enabled

7.6.21 GPIO4_PIN_CTL Register

表 7-39. GPIO4_PIN_CTL (Address 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO4_OUT_SEL	R/W	0x0	GPIO4 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO4_OUT_SRC	R/W	0x0	GPIO4 Output Source Select Selects output source for GPIO4 data. See *セクション 7.4.13.2*.
1	GPIO4_OUT_VAL	R/W	0x0	GPIO4 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO4_OUT_SRC[2:0] = 100 and GPIO4_OUT_SEL[2:0] = 000
0	GPIO4_OUT_EN	R/W	0x0	GPIO4 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[4] = 1. 0: Disabled 1: Enabled

7.6.22 GPIO5_PIN_CTL Register

表 7-40. GPIO5_PIN_CTL (Address 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO5_OUT_SEL	R/W	0x0	GPIO5 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO5_OUT_SRC	R/W	0x0	GPIO5 Output Source Select Selects output source for GPIO5 data: See 表 7-8.
1	GPIO5_OUT_VAL	R/W	0x0	GPIO5 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO5_OUT_SRC[2:0] = 100 and GPIO5_OUT_SEL[2:0] = 00
0	GPIO5_OUT_EN	R/W	0x0	GPIO5 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[5] = 1. 0: Disabled 1: Enabled

7.6.23 GPIO6_PIN_CTL Register

表 7-41. GPIO6_PIN_CTL (Address 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	GPIO6_OUT_SEL	R/W	0x0	GPIO6 Output Select Determines the output data for the selected source. See *セクション 7.4.13.2*.
4:2	GPIO6_OUT_SRC	R/W	0x0	GPIO6 Output Source Select Selects output source for GPIO6 data: See 表 7-8
1	GPIO6_OUT_VAL	R/W	0x0	GPIO6 Output Value This register provides the output data value when the GPIO pin is enabled to output the local register controlled value by setting GPIO6_OUT_SRC[2:0] = 100 and GPIO6_OUT_SEL[2:0] = 00
0	GPIO6_OUT_EN	R/W	0x0	GPIO6 Output Enable. Must be set to zero when configured as an input in GPIO Input Control register, 0x0F[6] = 1. 0: Disabled 1: Enabled

7.6.24 RESERVED Register

表 7-42. RESERVED (Address 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved.

7.6.25 FS_CTL Register

表 7-43. FS_CTL (Address 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	FS_MODE	R/W	0x0	FrameSync Mode 0000: Internal Generated FrameSync, use back channel frame clock from port 0 0001: Internal Generated FrameSync, use back channel frame clock from port 1 0010: Reserved. 0011: Reserved 01xx: Internal Generated FrameSync, use 25MHz clock 1000: External FrameSync from GPIO0 1001: External FrameSync from GPIO1 1010: External FrameSync from GPIO2 1011: External FrameSync from GPIO3 1100: External FrameSync from GPIO4 1101: External FrameSync from GPIO5 1110: External FrameSync from GPIO6 1111: Reserved
3	FS_SINGLE	(R/W)/SC	0x0	Generate Single FrameSync pulse When this bit is set, a single FrameSync pulse will be generated. The system should wait for the full duration of the desired pulse before generating another pulse. When using this feature, the FS_GEN_ENABLE bit should remain set to 0. This bit is self-clearing and will always return 0.
2	FS_INIT_STATE	R/W	0x0	Initial State. This register controls the initial state of the FrameSync signal. 0: FrameSync initial state is 0 1: FrameSync initial state is 1
1	FS_GEN_MODE	R/W	0x0	FrameSync Generation Mode This control selects between Hi/Lo and 50/50 modes. In Hi/Lo mode, the FrameSync generator uses the FS_HIGH_TIME [15:0] and FS_LOW_TIME [15:0] register values to separately control the High and Low periods for the generated FrameSync signal. In 50/50 mode, the FrameSync generator uses the values in the FS_HIGH_TIME_0, FS_LOW_TIME_1 and FS_LOW_TIME_0 registers as a 24-bit value for both the High and Low periods of the generated FrameSync signal. 0: Hi/Lo 1: 50/50
0	FS_GEN_ENABLE	R/W	0x0	FrameSync Generation Enable 0: Disabled 1: Enabled

7.6.26 FS_HIGH_TIME_1 Register

表 7-44. FS_HIGH_TIME_1 (Address 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_HIGH_TIME_1	R/W	0x0	FrameSync High Time bits 15:8 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.27 FS_HIGH_TIME_0 Register

表 7-45. FS_HIGH_TIME_0 (Address 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC _HIGH_TIME_0	R/W	0x0	FrameSync High Time bits 7:0 The value programmed to the FS_HIGH_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_HIGH_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.28 FS_LOW_TIME_1 Register

表 7-46. FS_LOW_TIME_1 (Address 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC _LOW_TIME_1	R/W	0x0	FrameSync Low Time bits 15:8 The value programmed to the FS_LO_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_LO_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.29 FS_LOW_TIME_0 Register

表 7-47. FS_LOW_TIME_0 (Address 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAMESYNC_LOW_ TIME_0	R/W	0x0	FrameSync Low Time bits 7:0 The value programmed to the FS_LO_TIME register should be reduced by 1 from the desired delay. For example, a value of 0 in the FRAMESYNC_LO_TIME field will result in a 1 cycle high pulse on the FrameSync signal.

7.6.30 MAX_FRM_HI Register

表 7-48. MAX_FRM_HI (Address 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAX_FRAME_HI	R/W	0x00	CSI-2 Maximum Frame Count bits 15:8 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

7.6.31 MAX_FRM_LO Register

表 7-49. MAX_FRM_LO (Address 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAX_FRAME_LO	R/W	0x04	CSI-2 Maximum Frame Count bits 7:0 In RAW mode operation, the FPD3 Receiver will create CSI-2 video frames. For the Frame Start and Frame End packets of each video frame, a 16-bit frame number field will be generated. If the Maximum Frame Count value is set to 0, the frame number is disabled and will always be 0. If Maximum Frame Count value is non-zero, the frame number will increment for each from 1 up to the Maximum Frame Count value before resetting to 1.

7.6.32 CSI_PLL_CTL Register

表 7-50. CSI_PLL_CTL (Address 0x1F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R	0x0	Reserved
3:2	RESERVED	R/W	0x0	Reserved
1:0	CSI_TX_SPEED	R/W	0x2	CSI Transmitter Speed select: Controls the CSI Transmitter frequency. 00 : 1.6 Gbps serial rate 01 : Reserved 10 : 800 Mbps serial rate 11 : 400 Mbps serial rate

7.6.33 FWD_CTL1 Register

Forwarding control enables or disables video stream from each Rx Port.

表 7-51. FWD_CTL1 (Address 0x20)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R/W	0x0	Reserved.
5	FWD_PORT1_DIS	R/W	0x1	Disable forwarding of RX Port 1 0: Forwarding enabled for RX Port 1 1: Forwarding disabled for RX Port 1
4	FWD_PORT0_DIS	R/W	0x1	Disable forwarding of RX Port 0 0: Forwarding enabled for RX Port 0 1: Forwarding disabled for RX Port 0
3:0	RESERVED	R	0x0	Reserved.

7.6.34 FWD_CTL2 Register

表 7-52. FWD_CTL2 (Address 0x21)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CSI_REPLICATE	R/W	0x0	CSI Replicate Mode. When set to a 1, the CSI output from port 0 will also be generated on CSI port 1. In this mode, each CSI port may be one or two lanes only. The same output data will be presented on both ports.
6	FWD_SYNC_AS_AVAIL	R/W	0x0	Synchronized Forwarding. As Available During Synchronized Forwarding, each forwarding engine will wait for video data to be available from each enabled port, prior to sending the video line. Setting this bit to a 1 will allow sending the next video line as it becomes available. For example if RX Ports 0 and 1 are being forwarded, port 0 video line is forwarded when it becomes available, rather than waiting until both ports 0 and ports 1 have video data available. This operation may reduce the likelihood of buffer overflow errors in some conditions. This bit will have no effect in video line concatenation mode and only affects video lines (long packets) rather than synchronization packets. (See *セクション 7.4.28.3*.)
5:4	RESERVED	R	0x0	Reserved.
3:2	CSI0_SYNC_FWD	R/W	0x00	Enable synchronized forwarding for CSI output port 0. (See *セクション 7.4.28.3*.) 00: Synchronized forwarding disabled 01: Basic Synchronized forwarding enabled 10: Synchronous forwarding with line interleaving 11: Synchronous forwarding with line concatenation Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be set at a time.
1	RESERVED	R/W	0x0	Reserved.

表 7-52. FWD_CTL2 (Address 0x21) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	CSI0_RR_FWD	R/W	0x1	Enable round robin forwarding for CSI TX output port. When this mode is enabled, no attempt is made to synchronize the video traffic. When multiple sources have data available to forward, the data will tend to be forwarded in a round-robin fashion. 0: Round robin forwarding disabled 1: Round robin forwarding enabled Only one of CSI0_RR_FWD and CSI0_SYNC_FWD must be set at a time.

7.6.35 FWD_STS Register

表 7-53. FWD_STS (Address 0x22)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R	0x0	Reserved
2	FWD_SYNC_FAIL0	R/RC	0x0	Forwarding synchronization failed for CSI TX output port During Synchronized forwarding, this flag indicates a failure of synchronized video has been detected. For this bit to be set, the forwarding process must have previously been successful at sending at least one synchronized video frame. 0: No failure 1: Synchronization failure This bit is cleared on read.
1	RESERVED	R	0x0	Reserved
0	FWD_SYNC0	R	0x0	Forwarding synchronized for CSI TX output port: During Synchronized forwarding, this bit indicates that the forwarding engine is currently able to provide synchronized video from enabled Receive ports. This bit is always 0 if Synchronized forwarding is disabled. 0: Not synchronized 1: Synchronized

7.6.36 INTERRUPT_CTL Register

表 7-54. INTERRUPT_CTL (Address 0x23)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	INT_EN	R/W	0x0	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
6:5	RESERVED	R	0x0	Reserved
4	IE_CSI_TX0	R/W	0x0	CSI Transmit Port Interrupt: Enable interrupt from CSI Transmitter Port.
3:2	RESERVED	R	0x0	Reserved
1	IE_RX1	R/W	0x0	RX Port 1 Interrupt: Enable interrupt from Receiver Port 1.
0	IE_RX0	R/W	0x0	RX Port 0 Interrupt: Enable interrupt from Receiver Port 0.

7.6.37 INTERRUPT_STS Register

表 7-55. INTERRUPT_STS (Address 0x24)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	INTERRUPT_STS	R	0x0	Global Interrupt: Set if any enabled interrupt is indicated in the individual status bits in this register. The setting of this bit is not dependent on the INT_EN bit in the INTERRUPT_CTL register but does depend on the IE_xxx bits. For example, if IE_RX0 and IS_RX0 are both asserted, the INTERRUPT_STS bit is set to 1.
6:5	RESERVED	R	0x0	Reserved
4	IS_CSI_TX0	R	0x0	CSI Transmit Port Interrupt: An interrupt has occurred for CSI Transmitter Port 0. This interrupt is cleared upon reading the CSI_TX_ISR register for CSI Transmit Port.
3:2	RESERVED	R	0x0	Reserved
1	IS_RX1	R	0x0	RX Port 1 Interrupt: An interrupt has occurred for Receive Port 1. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.
0	IS_RX0	R	0x0	RX Port 0 Interrupt: An interrupt has occurred for Receive Port 0. This interrupt is cleared by reading the associated status register(s) for the event(s) that caused the interrupt. The status registers are RX_PORT_STS1, RX_PORT_STS2, and CSI_RX_STS.

7.6.38 TS_CONFIG Register

表 7-56. TS_CONFIG (Address 0x25)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	FS_POLARITY	R/W	0x0	Framesync Polarity Indicates active edge of FrameSync signal 0: Rising edge 1: Falling edge
5:4	TS_RES_CTL	R/W	0x0	Timestamp Resolution Control. For typical applications of 30-Hz and 60-Hz frame rate 1.0-µs setting 11 = 1.0 µs should be selected to give counter duration of 1.0 µs × 65535 = 65.5 ms 00: 40 ns 01: 80 ns 10: 160 ns 11: 1.0 µs
3	TS_AS_AVAIL	R/W	0x0	Timestamp Ready Control 0: Normal operation 1: Indicate timestamps ready as soon as all port timestamps are available
2	RESERVED	R	0x0	Reserved
1	TS_FREERUN	R/W	0x0	FreeRun Mode 0: FrameSync mode 1: FreeRun mode
0	TS_MODE	R/W	0x0	Timestamp Mode 0: Line start 1: Frame start

7.6.39 TS_CONTROL Register

表 7-57. TS_CONTROL (Address 0x26)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved
4	TS_FREEZE	R/W	0x0	Freeze Timestamps 0: Normal operation 1: Freeze timestamps Setting this bit freezes timestamps and clears the TS_READY flag. The TS_FREEZE bit should be cleared after reading timestamps to resume operation.
3:2	RESERVED	R	0x0	Reserved
1	TS_ENABLE1	R/W	0x0	Timestamp Enable RX Port 1 0: Disabled 1: Enabled
0	TS_ENABLE0	R/W	0x0	Timestamp Enable RX Port 0 0: Disabled 1: Enabled

7.6.40 TS_LINE_HI Register

表 7-58. TS_LINE_HI (Address 0x27)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TS_LINE_HI	R/W	0x0	Timestamp Line, upper 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

7.6.41 TS_LINE_LO Register

表 7-59. TS_LINE_LO (Address 0x28)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TS_LINE_LO	R/W	0x0	Timestamp Line, lower 8 bits This field is the line number at which to capture the timestamp when Line Start mode is enabled. For proper operation, the line number should be set to a value greater than 1. During Frame Start mode, if TS_FREERUN is set, the TS_LINE value is used to determine when to begin checking for Frame Start

7.6.42 TS_STATUS Register

表 7-60. TS_STATUS (Address 0x29)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved
4	TS_READY	R	0x0	Timestamp Ready This flag indicates when timestamps are ready to be read. This flag is cleared when the TS_FREEZE bit is set.
3:2	RESERVED	R	0x0	Reserved
1	TS_VALID1	R	0x0	Timestamp Valid, RX Port 1
0	TS_VALID0	R	0x0	Timestamp Valid, RX Port 0

7.6.43 TIMESTAMP_P0_HI Register

表 7-61. TIMESTAMP_P0_HI (Address 0x2A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P0_HI	R	0x0	Timestamp, upper 8 bits, RX Port 0

7.6.44 TIMESTAMP_P0_LO Register

表 7-62. TIMESTAMP_P0_LO (Address 0x2B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP_P0_LO	R	0x0	Timestamp, lower 8 bits, RX Port 0

7.6.45 TIMESTAMP_P1_HI Register

表 7-63. TIMESTAMP_P1_HI (Address 0x2C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP _P1_HI	R	0x0	Timestamp, upper 8 bits, RX Port 1

7.6.46 TIMESTAMP_P1_LO Register

表 7-64. TIMESTAMP_P1_LO (Address 0x2D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	TIMESTAMP _P1_LO	R	0x0	Timestamp, lower 8 bits, RX Port 1

7.6.47 RESERVED Register

表 7-65. RESERVED (Address 0x2E – 0x32)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x00	Reserved

7.6.48 CSI_CTL Register

表 7-66. CSI_CTL (Address 0x33)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	CSI_CAL_EN	R/W	0x0	Enable initial CSI Skew-Calibration sequence When the initial skew-calibration sequence is enabled, the CSI Transmitter will send the sequence at initialization, prior to sending any HS data. This bit should be set when operating at 1.6 Gbps CSI speed (as configured in the CSI_PLL_CTL register). 0: Disabled 1: Enabled
5:4	CSI_LANE_COUNT	R/W	0x0	CSI lane count 00: 4 lanes 01: 3 lanes 10: 2 lanes 11: 1 lane If CSI_REPLICATE is set in the FWD_CTL2 register, the device must be programmed for 1 or 2 lanes only.
3:2	CSI_ULP	R/W	0x0	Force LP00 state on data/clock lanes 00: Normal operation 01: LP00 state forced only on data lanes 10: Reserved 11: LP00 state forced on data and clock lanes
1	CSI_CONTS_CLOCK	R/W	0x0	Enable CSI continuous clock mode. CSI-2 Tx outputs will provide a continuous clock output signal once first packet is received. 0: Disabled 1: Enabled
0	CSI_ENABLE	R/W	0x0	Enable CSI output 0: Disabled 1: Enabled

7.6.49 CSI_CTL2 Register

表 7-67. CSI_CTL2 (Address 0x34)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R	0x4	Reserved
3	CSI_PASS_MODE	R/W	0x0	CSI PASS indication mode Determines whether the CSI Pass indication is for a single port or all enabled ports. 0 : Assert PASS if at least one enabled Receive port is providing valid video data 1 : Assert PASS only if ALL enabled Receive ports are providing valid video data
2	CSI_CAL_INV	R/W	0x0	CSI Calibration Inverted Data pattern During the CSI skew-calibration pattern, the CSI Transmitter will send a sequence of 01010101 data (first bit 0). Setting this bit to a 1 will invert the sequence to 10101010 data.
1	CSI_CAL_SINGLE	(R/W)/SC	0x0	Enable single periodic CSI Skew-Calibration sequence Setting this bit will send a single skew-calibration sequence from the CSI Transmitter. The skew-calibration sequence is the 1010 bit sequence required for periodic calibration. The calibration sequence is sent at the next idle period on the CSI interface. This bit is self-clearing and will reset to 0 after the calibration sequence is sent.
0	CSI_CAL_PERIODIC	R/W	0x0	Enable periodic CSI Skew-Calibration sequence When the periodic skew-calibration sequence is enabled, the CSI Transmitter will send the periodic skew-calibration sequence following the sending of Frame End packets. 0: Disabled 1: Enabled

7.6.50 CSI_STS Register

表 7-68. CSI_STS (Address 0x35)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:2	RESERVED	R	0x0	Reserved
1	TX_PORT_SYNC	R	0x0	TX Port Synchronized This bit indicates the CSI Transmit Port is able to properly synchronize input data streams from multiple sources. This bit is 0 if synchronization is disabled via the FWD_CTL2 register. 0 : Input streams are not synchronized 1 : Input streams are synchronized
0	TX_PORT_PASS	R	0x0	TX Port Pass Indicates valid data is available on at least one port, or on all ports if configured for all port status via the CSI_PASS_MODE bit in the CSI_CTL2 register. The function differs based on mode of operation. In non-synchronous operation, the TX_PORT_PASS indicates the CSI port is actively delivering valid video data. The status is cleared based on detection of an error condition that interrupts transmission. During Synchronized forwarding, the TX_PORT_PASS indicates valid data is available for delivery on the CSI TX output. Data may not be delivered if ports are not synchronized. The TX_PORT_SYNC status is a better indicator that valid data is being delivered to the CSI transmit port.

7.6.51 CSI_TX_ICR Register

表 7-69. CSI_TX_ICR (Address 0x36)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved
4	IE_RX_PORT_INT	R/W	0x0	RX Port Interrupt Enable Enable interrupt based on receiver port interrupt for the RX Ports being forwarded to the CSI Transmit Port.
3	IE_CSI_SYNC _ERROR	R/W	0x0	CSI Sync Error interrupt Enable Enable interrupt on CSI Synchronization enable.
2	IE_CSI_SYNC	R/W	0x0	CSI Synchronized interrupt Enable Enable interrupts on CSI Transmit Port assertion of CSI Synchronized Status.
1	IE_CSI_PASS _ERROR	R/W	0x0	CSI RX Pass Error interrupt Enable Enable interrupt on CSI Pass Error
0	IE_CSI_PASS	R/W	0x0	CSI Pass interrupt Enable Enable interrupt on CSI Transmit Port assertion of CSI Pass.

7.6.52 CSI_TX_ISR Register

表 7-70. CSI_TX_ISR (Address 0x37)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved
4	IS_RX_PORT_INT	R	0x0	RX Port Interrupt A Receiver port interrupt has been generated for one of the RX Ports being forwarded to the CSI Transmit Port. A read of the associated port receive status registers will clear this interrupt. See the PORT_ISR_HI and PORT_ISR_LO registers for details.
3	IS_CSI_SYNC_ERROR	R/RC	0x0	CSI Sync Error interrupt A synchronization error has been detected for multiple video stream inputs to the CSI Transmitter.
2	IS_CSI_SYNC	R/RC	0x0	CSI Synchronized interrupt CSI Transmit Port assertion of CSI Synchronized Status. Current status for CSI Sync can be read from the TX_PORT_SYNC flag in the CSI_STS register.
1	IS_CSI_PASS_ERROR	R/RC	0x0	CSI RX Pass Error interrupt A deassertion of CSI Pass has been detected on one of the RX Ports being forwarded to the CSI Transmit Port
0	IS_CSI_PASS	R/RC	0x0	CSI Pass interrupt CSI Transmit Port assertion of CSI Pass detected. Current status for the CSI Pass indication can be read from the TX_PORT_PASS flag in the CSI_STS register

7.6.53 CSI_TEST_CTL Register

表 7-71. CSI_TEST_CTL (Address 0x38)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.54 CSI_TEST_PATT_HI Register

表 7-72. CSI_TEST_PATT_HI (Address 0x39)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_TEST_PATT	R/W	0x00	Bits 15:8 of fixed pattern for characterization test

7.6.55 CSI_TEST_PATT_LO Register

表 7-73. CSI_TEST_PATT_LO (Address 0x3A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_TEST_PATT	R/W	0x00	Bits 7:0 of fixed pattern for characterization test

7.6.56 RESERVED Register

表 7-74. RESERVED (Address 0x3B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x01	Reserved

7.6.57 RESERVED Register

表 7-75. RESERVED (Address 0x3C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x14	Reserved

7.6.58 RESERVED Register

表 7-76. RESERVED (Address 0x3D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x6F	Reserved

7.6.59 RESERVED Register

表 7-77. RESERVED (Address 0x3E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.60 RESERVED Register

表 7-78. RESERVED (Address 0x3F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x40	Reserved

7.6.61 RESERVED Register

表 7-79. RESERVED (Address 0x40)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.62 SFILTER_CFG Register

The SFilter configuration register controls the minimum and maximum values allow for the clock to data sample timing. It is recommended to program this register to 0xA9 during initialization for optimal startup time and ensure consistent AEQ performance across different channel characteristics.

表 7-80. SFILTER_CFG (Address 0x41)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	SFILTER_MAX	R/W	0xA	SFILTER maximum setting This field controls the maximum SFILTER setting. Allowed values are 0-14 with 7 being the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The maximum setting must be greater than or equal to the minimum setting.
3:0	SFILTER_MIN	R/W	0x7	SFILTER minimum setting. This field controls the maximum SFILTER setting. Allowed values are 0-14, where 7 is the mid point. These values are used for both AEQ adaption and dynamic SFILTER control. The minimum setting must be less than or equal to the SFILTER_MAX. Recommend to set SFILTER_MIN = 0x9 for normal operation in typical system use cases.

7.6.63 AEQ_CTL1 Register

表 7-81. AEQ_CTL1 (Address 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6:4	AEQ_ERR_CTL	R/W	0x7	AEQ Error Control Setting any bits in AEQ_ERR_CTL will enable FPD3 error checking during the Adaptive Equalization process. Errors are accumulated over 1/2 of the period of the timer set by the ADAPTIVE_EQ_RELOCK_TIME filed in the AEQ_CTL2 register. If the number of errors is greater than the programmed threshold (AEQ_ERR_THOLD), the AEQ will attempt to increase the EQ setting. The errors may also be checked as part of EQ setting validation if AEQ_2STEP_EN is set. The following errors are checked based on this three bit field: [6] FPD-Link III clock errors [5] Packet encoding errors [4] Parity errors
3	RESERVED	R/W	0x0	Reserved
2	AEQ_2STEP_EN	R/W	0x0	AEQ 2-step enable This bit enables a two-step operation as part of the Adaptive EQ algorithm. If disabled, the state machine will wait for a programmed period of time, then check status to determine if setting is valid. If enabled, the state machine will wait for 1/2 the programmed period, then check for errors over an additional 1/2 the programmed period. If errors occur during the 2nd step, the state machine will immediately move to the next setting. 0 : Wait for full programmed delay, then check instantaneous lock value 1 : Wait for 1/2 programmed time, then check for errors over 1/2 programmed time. The programmed time is controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register
1	AEQ_OUTER_LOOP	R/W	0x0	AEQ outer loop control This bit controls whether the Equalizer or SFILTER adaption is the outer loop when the AEQ adaption includes SFILTER adaption. 0 : AEQ is inner loop, SFILTER is outer loop 1 : AEQ is outer loop, SFILTER is inner loop
0	AEQ_SFILTER_EN	R/W	0x1	Enable SFILTER Adaption with AEQ Setting this bit allows SFILTER adaption as part of the Adaptive Equalizer algorithm.

7.6.64 AEQ_ERR_THOLD Register

表 7-82. AEQ_ERR_THOLD (Address 0x43)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	AEQ_ERR _THRESHOLD	R/W	0x1	AEQ Error Threshold This register controls the error threshold to determine when to re-adapt the EQ settings. This register should not be programmed to a value of 0.

7.6.65 RESERVED Register

表 7-83. RESERVED (Address 0x44 – 0x49)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x00	Reserved

7.6.66 FPD3_CAP Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

It is recommended to set bit four in the FPD-Link III capabilities register to one, to flag errors detected from the enhanced CRC on FPD-Link III encoded link control information. The FPD-Link III Encoder CRC must also be enabled by setting the FPD3_ENC_CRC_DIS (register 0xBA[7]) to 0.

表 7-84. FPD3_CAP (Address 0x4A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R/W	0x0	Reserved
4	FPD3_ENC_CRC_CAP	R/W	0x0	0: Disable CRC error flag from FPD-Link III encoder 1: Enable CRC error flag from FPD-Link III encoder (recommended)
3:0	RESERVED	R/W	0x0	Reserved

7.6.67 RAW_EMBED_DTYPE Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

When the receiver is programmed for Raw mode data, this register field allows setting the Data Type field for the first N lines to indicated embedded non-image data. RAW_EMBED_DTYPE has no effect on CSI-2 receiver modes.

表 7-85. RAW_EMBED_DTYPE (Address 0x4B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	EMBED_DTYPE_EN	R/W	0x00	Embedded Data Type Enable. 00 : All long packets will be forwarded as RAW10 or RAW12 video data 01, 10, or 11 : Send first N long packets (1, 2, or 3) as Embedded data using the data type in the EMBED_DTYPE_ID field of this register. This control has no effect if the Receiver is programmed to receive CSI formatted data.
5:0	EMBED_DTYPE_ID	R/W	0x12	Embedded Data Type. If sending embedded data is enabled via the EMBED_DTYPE_EN control in this register, the Data Type field for the first N lines of each frame will use this value rather than the value programmed in the RAW12_ID or RAW10_ID registers. The default setting matches the CSI-2 specification for Embedded 8-bit non Image Data

7.6.68 FPD3_PORT_SEL Register

The FPD-Link III Port Select register configures which port is accessed in I2C commands to unique Rx Port registers 0x4A, 0x4B, 0x4D - 0x7F and 0xD0 - 0xDF. A 2-bit RX_READ_PORT field provides for reading values from a single port. The 4-bit RX_WRITE_PORT field provides individual enables for each port, allowing simultaneous writes broadcast to both of the FPD-Link III Receive port register blocks in unison. The DS90UB936-Q1 maintains separate page control, preventing conflict between sources.

表 7-86. FPD3_PORT_SEL (Address 0x4C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	PHYS_PORT_NUM	R	0x0 Port#	Physical port number This field provides the physical port connection when reading from a remote device via the Bi-directional Control Channel. When accessed via local I2C interfaces, the value returned is always 0. When accessed via Bi-directional Control Channel, the value returned is the port number of the Receive port connection.
5	RESERVED	R	0x0	Reserved
4	RX_READ_PORT	R/W	0x0 Port#	Select RX port for register read This field selects one of the two RX port register blocks for readback. This applies to all paged FPD-Link III Receiver port registers. 0: Port 0 registers 1: Port 1 registers When accessed via local I2C interfaces, the default setting is 0. When accessed via Bi-directional Control Channel, the default value is the port number of the Receive port connection.
3:2	RESERVED	R	0x00	Reserved
1	RX_WRITE_PORT_1	R/W	0x0 0x1 for RX Port 1	Write Enable for RX port 1 registers This bit enables writes to RX port 1 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD-Link III Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 1.
0	RX_WRITE_PORT_0	R/W	0x0 0x1 for RX Port 0	Write Enable for RX port 0 registers This bit enables writes to RX port 0 registers. Any combination of RX port registers can be written simultaneously. This applies to all paged FPD-Link III Receiver port registers. 0: Writes disabled 1: Writes enabled When accessed via Bi-directional Control Channel, the default value is 1 if accessed over RX port 0.

7.6.69 RX_PORT_STS1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-87. RX_PORT_STS1 (Address 0x4D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	RX_PORT_NUM	R	0x0	RX Port Number. This read-only field indicates the number of the currently selected RX read port.
5	BCC_CRC_ERROR	R/RC	0x0	Bi-directional Control Channel CRC Error Detected This bit indicates a CRC error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
4	LOCK_STS_CHG	R/RC	0x0	Lock Status Changed This bit is set if a change in receiver lock status has been detected since the last read of this register. Current lock status is available in the LOCK_STS bit of this register. This bit is cleared on read.
3	BCC_SEQ_ERROR	R/RC	0x0	Bi-directional Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in the forward control channel. If this bit is set, an error may have occurred in the control channel operation. This bit is cleared on read.
2	PARITY_ERROR	R	0x0	FPD-Link III parity errors detected This flag is set when the number of parity errors detected is greater than the threshold programmed in the PAR_ERR_THOLD registers. 1: Number of FPD-Link III parity errors detected is greater than the threshold 0: Number of FPD-Link III parity errors is below the threshold This bit is cleared when the RX_PAR_ERR_HI/LO registers are cleared.
1	PORT_PASS	R	0x0	Receiver PASS indication. This bit indicates the current status of the Receiver PASS indication. The requirements for setting the Receiver PASS indication are controlled by the PORT_PASS_CTL register. 1: Receive input has met PASS criteria 0: Receive input does not meet PASS criteria
0	LOCK_STS	R	0x0	FPD-Link III receiver is locked to incoming data 1: Receiver is locked to incoming data 0: Receiver is not locked

7.6.70 RX_PORT_STS2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-88. RX_PORT_STS2 (Address 0x4E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	LINE_LEN _UNSTABLE	R/RC	0x0	Line Length Unstable If set, this bit indicates the line length was detected as unstable during a previous video frame. The line length is considered to be stable if all the lines in the video frame have the same length. This flag will remain set until read.
6	LINE_LEN_CHG	R/RC	0x0	Line Length Changed 1: Change of line length detected 0: Change of line length not detected This bit is cleared on read.
5	FPD3_ENCODE _ERROR	R/RC	0x0	FPD-Link III Encoder error detected If set, this flag indicates an error in the FPD-Link III encoding has been detected by the FPD-Link III receiver. This bit is cleared on read. Note, to detect FP3 Encoder errors, the LINK_ERROR_COUNT must be enabled with a LINK_ERR_THRESH value greater than 1. Otherwise, the loss of Receiver Lock will prevent detection of the Encoder error.
4	BUFFER_ERROR	R/RC	0x0	Packet buffer error detected. If this bit is set, an overflow condition has occurred on the packet buffer FIFO. 1: Packet Buffer error detected 0: No Packet Buffer errors detected This bit is cleared on read.
3	CSI_ERROR	R	0x0	CSI Receive error detected. See the CSI_RX_STS register for details.
2	FREQ_STABLE	R	0x0	Frequency measurement stable
1	CABLE_FAULT	R	0x0	When link is expected to be operational, CABLE_FAULT would indicate open or short on the cable as no FPD-Link clock is detected at the deserializer Rx input.
0	LINE_CNT_CHG	R/RC	0x0	Line Count Changed 1: Change of line count detected 0: Change of line count not detected This bit is cleared on read.

7.6.71 RX_FREQ_HIGH Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-89. RX_FREQ_HIGH (Address 0x4F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FREQ_CNT_HIGH	R	0x00	Frequency Counter High Byte (MHz) The Frequency counter reports the measured frequency for the FPD-Link III Receiver. This portion of the field is the integer value in MHz.

7.6.72 RX_FREQ_LOW Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-90. RX_FREQ_LOW (Address 0x50)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FREQ_CNT_LOW	R	0x00	Frequency Counter Low Byte (1/256 MHz) The Frequency counter reports the measured frequency for the FPD-Link III Receiver. This portion of the field is the fractional value in 1/256 MHz.

7.6.73 SENSOR_STS_0 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Sensor Status Register 0 field provides additional status information when paired with a DS90UB935-Q1 Serializer. This field is automatically loaded from the forward channel.

表 7-91. SENSOR_STS_0 (Address 0x51)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x00	Reserved
5	CSI_ALARM	R	0x0	Alarm flag for CSI error from serializer
4	BCC_ALARM	R	0x0	Alarm flag for back channel error from serializer
3	LINK_DETECT_ALARM	R	0x0	Alarm flag for link detect from serializer
2	TEMP_SENSE_ALARM	R	0x0	Alarm flag for temp sensor from serializer
1	VOLT1_SENSE_ALARM	R	0x0	Alarm flag for voltage sensor 1 from serializer
0	VOLT0_SENSE_ALARM	R	0x0	Alarm flag for voltage sensor 0 from serializer

7.6.74 SENSOR_STS_1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Sensor Status Register 1 field provides additional status information when paired with a DS90UB935-Q1 Serializer. This field is automatically loaded from the forward channel.

表 7-92. SENSOR_STS_1 (Address 0x52)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6:4	VOLT1_SENSE_LEVEL	R	0x0	Voltage sensor sampled value from serializer
3	RESERVED	R	0x0	Reserved
2:0	VOLT0_SENSE_LEVEL	R	0x0	Voltage sensor sampled value from serializer

7.6.75 SENSOR_STS_2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Sensor Status Register 2 field provides additional status information when paired with a DS90UB935-Q1 Serializer. This field is automatically loaded from the forward channel.

表 7-93. SENSOR_STS_2 (Address 0x53)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R	0x0	
2:0	TEMP_SENSE_LEVEL	R	0x0	Temperature sensor sampled value from serializer

7.6.76 SENSOR_STS_3 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Sensor Status Register 3 field provides additional status information on the CSI-2 input when paired with a DS90UB935-Q1 Serializer. This field is automatically loaded from the forward channel.

表 7-94. SENSOR_STS_3 (Address 0x54)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	RESERVED	R	0x0	Reserved
4	CSI_ECC_2BIT_ERR	R	0x0	CSI -2 ECC error flag from serializer
3	CSI_CHKSUM_ERR	R	0x0	CSI-2 checksum error from serializer
2	CSI_SOT_ERR	R	0x0	CSI-2 start of transmission error from serializer
1	CSI_SYNC_ERR	R	0x0	CSI-2 synchronization error from serializer
0	CSI_CNTRL_ERR	R	0x0	CSI-2 control error from serializer

7.6.77 RX_PAR_ERR_HI Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-95. RX_PAR_ERR_HI (Address 0x55)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERROR _ BYTE_1	R/RC	0x0	Number of FPD-Link III parity errors 8 most significant bits. The parity error counter registers return the number of data parity errors that have been detected on the FPD-Link III Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX_PARITY_CHECKER_ENABLE bit in register 0x02 prior to reading the parity error count registers. This register is cleared upon reading the RX_PAR_ERR_LO register.

7.6.78 RX_PAR_ERR_LO Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-96. RX_PAR_ERR_LO (Address 0x56)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PAR_ERROR _BYTE_0	R/RC	0x0	Number of FPD-Link III parity errors 8 least significant bits. The parity error counter registers return the number of data parity errors that have been detected on the FPD-Link III Receiver data since the last detection of valid lock or last read of the RX_PAR_ERR_LO register. For accurate reading of the parity error count, disable the RX_PARITY_CHECKER_ENABLE bit in register 0x02 prior to reading the parity error count registers. This register is cleared on read.

7.6.79 BIST_ERR_COUNT Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-97. BIST_ERR_COUNT (Address 0x57)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	BIST_ERROR _COUNT	R	0x0	Bist Error Count Returns BIST error count

7.6.80 BCC_CONFIG Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-98. BCC_CONFIG (Address 0x58)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	I2C_PASS _THROUGH_ALL	R/W	0x0	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6	I2C_PASS _THROUGH	R/W	0x0	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
5	AUTO_ACK_ALL	R/W	0x0	Automatically Acknowledge all I2C writes independent of the forward channel lock state or status of the remote Acknowledge 1: Enable 0: Disable
4	BC_ALWAYS_ON	R/W	0x1	Back channel enable 1: Back channel is always enabled independent of I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL 0: Back channel enable requires setting of either I2C_PASS_THROUGH and I2C_PASS_THROUGH_ALL This bit may only be written through a local I2C controller.
3	BC_CRC _GENERATOR _ENABLE	R/W	0x1	Back Channel CRC Generator Enable 0: Disable 1: Enable
2:0	BC_FREQ_SELECT	R/W	S	Back Channel Frequency Select. Default value set by strap condition upon asserting PDB = HIGH. 000: 2.5 Mbps (select for DS90UB933-Q1 or DS90UB913A-Q1 compatibility) 001- 011: Reserved 010: 10 Mbps (select for non-synchronous back channel compatibility) 101: 25 Mbps 110: 50 Mbps (default for CSI Synchronous back channel compatibility) 111: Reserved Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation to avoid a control channel timeout due to lack of response from the Deserializer.

7.6.81 DATAPATH_CTL1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-99. DATAPATH_CTL1 (Address 0x59)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	OVERRIDE_FC _CONFIG	R/W	0x0	1: Disable loading of the DATAPATH_CTL registers from the forward channel, keeping locally written values intact 0: Allow forward channel loading of DATAPATH_CTL registers
6:2	RESERVED	R/W	0x0	Reserved
1:0	FC_GPIO_EN	R/W	0x0	Forward Channel GPIO Enable Configures the number of enabled forward channel GPIOs 00: GPIOs disabled 01: One GPIO 10: Two GPIOs 11: Four GPIOs This field is normally loaded from the remote serializer. It can be overwritten if the OVERRIDE_FC_CONFIG bit in this register is 1.

7.6.82 DATAPATH_CTL2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-100. DATAPATH_CTL2 (Address 0x5A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x0	Reserved

7.6.83 SER_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-101. SER_ID (Address 0x5B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SER_ID	R/W	0x00	Remote Serializer ID This field is normally loaded automatically from the remote Serializer.
0	FREEZE_DEVICE_ID	R/W	0x0	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID is frozen at the value written.

7.6.84 SER_ALIAS_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-102. SER_ALIAS_ID (Address 0x5C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	SER_ALIAS_ID	R/W	0x0	7-bit Remote Serializer Alias ID Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Deserializer. The transaction is remapped to the address specified in the Target ID register. A value of 0 in this field disables access to the remote I2C Target.
0	SER_AUTO_ACK	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Serializer independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.85 TargetID[0] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-103. TargetID[0] (Address 0x5D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID0	R/W	0x0	7-bit Remote Target Device ID 0 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID0, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.86 TargetID[1] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-104. TargetID[1] (Address 0x5E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID1	R/W	0x0	7-bit Remote Target Device ID 1 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID1, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.87 TargetID[2] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-105. TargetID[2] (Address 0x5F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID2	R/W	0x0	7-bit Remote Target Device ID 2 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID2, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.88 TargetID[3] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-106. TargetID[3] (Address 0x60)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID3	R/W	0x0	7-bit Remote Target Device ID 3 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID3, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.89 TargetID[4] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-107. TargetID[4] (Address 0x61)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID4	R/W	0x0	7-bit Remote Target Device ID 4 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID4, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.90 TargetID[5] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-108. TargetID[5] (Address 0x62)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID5	R/W	0x0	7-bit Remote Target Device ID 5 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID5, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.91 TargetID[6] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-109. TargetID[6] (Address 0x63)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID6	R/W	0x0	7-bit Remote Target Device ID 6 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID6, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.92 TargetID[7] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-110. TargetID[7] (Address 0x64)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ID7	R/W	0x0	7-bit Remote Target Device ID 7 Configures the physical I2C address of the remote I2C Target device attached to the remote Serializer. If an I2C transaction is addressed to the Target Alias ID7, the transaction is remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R	0x0	Reserved.

7.6.93 TargetAlias[0] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-111. TargetAlias[0] (Address 0x65)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID0	R/W	0x0	7-bit Remote Target Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID0 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_0	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 0 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.94 TargetAlias[1] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-112. TargetAlias[1] (Address 0x66)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID1	R/W	0x0	7-bit Remote Target Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID1 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_1	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 1 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.95 TargetAlias[2] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-113. TargetAlias[2] (Address 0x67)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID2	R/W	0x0	7-bit Remote Target Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID2 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK 2	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 2 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.96 TargetAlias[3] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-114. TargetAlias[3] (Address 0x68)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID3	R/W	0x0	7-bit Remote Target Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID3 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK _3	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 3 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.97 TargetAlias[4] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-115. TargetAlias[4] (Address 0x69)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID4	R/W	0x0	7-bit Remote Target Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID4 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_AC K_4	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 4 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.98 TargetAlias[5] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-116. TargetAlias[5] (Address 0x6A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID5	R/W	0x0	7-bit Remote Target Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID5 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_5	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 5 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.99 TargetAlias[6] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-117. TargetAlias[6] (Address 0x6B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID6	R/W	0x0	7-bit Remote Target Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID6 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK_6	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 6 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.100 TargetAlias[7] Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-118. TargetAlias[7] (Address 0x6C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	TARGET_ALIAS_ID7	R/W	0x0	7-bit Remote Target Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Target device attached to the remote Serializer. The transaction is remapped to the address specified in the Target ID7 register. A value of 0 in this field disables access to the remote I2C Target.
0	TARGET_AUTO_ACK 7	R/W	0x0	Automatically Acknowledge all I2C writes to the remote Target 7 independent of the forward channel lock state or status of the remote Serializer Acknowledge 1: Enable 0: Disable

7.6.101 PORT_CONFIG Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-119. PORT_CONFIG (Address 0x6D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	CSI_WAIT_FS1	R/W	0x0	CSI Wait for FrameStart packet with count 1 The CSI Receiver will wait for a Frame Start packet with count of 1 before accepting other packets
6	CSI_WAIT_FS	R/W	0x1	CSI Wait for FrameStart packet CSI-2 Receiver will wait for a Frame Start packet before accepting other packets
5	CSI_FWD_CKSUM	R/W	0x1	Forward CSI packets with checksum errors 0: Do not forward packets with errors 1: Forward packets with errors
4	CSI_FWD_ECC	R/W	0x1	Forward CSI packets with ECC errors 0: Do not forward packets with errors 1: Forward packets with errors
3	CSI_FWD_LEN/ DISCARD_1ST _LINE_ON_ERR	R/W	0x1	In CSI FPD-Link III Input Mode, Forward CSI packets with length errors. In RAW Input Mode, forward truncated 1st video line. 0: CSI: Do not forward packets with errors. RAW: Forward truncated 1st video line 1: CSI: Forward packets with errors. RAW: Discard truncated 1st video line
2	COAX_MODE	R/W	S	Enable coax cable mode Default value set by strap condition of MODE pin upon asserting PDB = HIGH at start-up. 0: Shielded-twisted pair (STP) mode 1: Coax mode
1:0	FPD3_MODE	R/W	S	FPD-Link III Input Mode Default value set by strap condition of MODE pin upon asserting PDB = HIGH at start-up. 00: CSI Mode (DS90UB935 compatible) 01: RAW12 Mode/50 MHz (DS90UB913A/933 compatible) 10: RAW12 Mode/75 MHz (DS90UB913A/933 compatible) 11: RAW10 Mode/100 MHz (DS90UB913A/933 compatible)

7.6.102 BC_GPIO_CTL0 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-120. BC_GPIO_CTL0 (Address 0x6E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	BC_GPIO1_SEL	R/W	0x8	Back channel GPIO1 Select: Determines the data sent on GPIO1 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO1_SEL[2:0] 0111 : Reserved 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
3:0	BC_GPIO0_SEL	R/W	0x8	Back channel GPIO0 Select: Determines the data sent on GPIO0 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO0_SEL[2:0] 0111 : Reserved 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved

7.6.103 BC_GPIO_CTL1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-121. BC_GPIO_CTL1 (Address 0x6F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	BC_GPIO3_SEL	R/W	0x8	Back channel GPIO3 Select: Determines the data sent on GPIO3 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO3_SEL[2:0] 0111 : Reserved 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved
3:0	BC_GPIO2_SEL	R/W	0x8	Back channel GPIO2 Select: Determines the data sent on GPIO2 for the port back channel. 0xxx : Pin GPIOx where x is BC_GPIO2_SEL[2:0] 0111 : Reserved 1000 : Constant value of 0 1001 : Constant value of 1 1010 : FrameSync signal 1011 - 1111 : Reserved

7.6.104 RAW10_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

RAW10 virtual channel mapping only applies when FPD-Link III operating in RAW10 input mode. See register 0x71 for RAW12 and register 0x72 for CSI-2 mode operation.

表 7-122. RAW10_ID (Address 0x70)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_VC	R/W	<RX Port #>	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number (0 or 1)
5:0	RAW10_DT	R/W	0x2B	RAW10 DT This field configures the CSI data type used in RAW10 mode. The default of 0x2B matches the CSI specification.

7.6.105 RAW12_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

RAW12 virtual channel mapping only applies when FPD-Link III operating in RAW12 input mode. See register 0x70 for RAW10 and register 0x72 for CSI-2 mode operation.

表 7-123. RAW12_ID (Address 0x71)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW12_VC	R/W	<RX Port #>	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number (0 or 1)

表 7-123. RAW12_ID (Address 0x71) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
5:0	RAW12_DT	R/W	0x2C	RAW12 DT This field configures the CSI data type used in RAW12 mode. The default of 0x2C matches the CSI specification.

7.6.106 CSI_VC_MAP Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

CSI virtual channel mapping only applies when FPD-Link III operating in CSI-2 input mode. See registers 0x70 and 0x71 for RAW mode operation.

表 7-124. CSI_VC_MAP (Address 0x72)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_VC_MAP	R/W	0xE4	CSI-2 Virtual Channel Mapping Register This register provides a method for replacing the Virtual Channel Identifier (VC-ID) of incoming CSI packets. [7:6] : Map value for VC-ID of 3 [5:4] : Map value for VC-ID of 2 [3:2] : Map value for VC-ID of 1 [1:0] : Map value for VC-ID of 0

7.6.107 LINE_COUNT_HI Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-125. LINE_COUNT_HI (Address 0x73)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read.

7.6.108 LINE_COUNT_LO Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-126. LINE_COUNT_LO (Address 0x74)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO is latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

7.6.109 LINE_LEN_1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-127. LINE_LEN_1 (Address 0x75)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_HI	R	0x0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read.

7.6.110 LINE_LEN_0 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-128. LINE_LEN_0 (Address 0x76)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_LO	R	0x0	Low byte of Line Length The Line Length reports the length of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO is latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

7.6.111 FREQ_DET_CTL Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-129. FREQ_DET_CTL (Address 0x77)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	FREQ_HYST	R/W	0x3	Frequency Detect Hysteresis The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
5:4	FREQ_STABLE_THR	R/W	0x0	Frequency Stable Threshold The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40 µs 01 : 80 µs 10 : 320 µs 11 : 1.28 ms
3:0	FREQ_LO_THR	R/W	0x5	Frequency Low Threshold Sets the low threshold for the Clock frequency detect circuit in MHz. This value is used to determine if the clock frequency is too low for proper operation.

7.6.112 MAILBOX_1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-130. MAILBOX_1 (Address 0x78)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAILBOX_0	R/W	0x00	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

7.6.113 MAILBOX_2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-131. MAILBOX_2 (Address 0x79)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	MAILBOX_1	R/W	0x01	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C controllers on opposite ends of the link.

7.6.114 CSI_RX_STS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-132. CSI_RX_STS (Address 0x7A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	RESERVED	R	0x0	Reserved
3	LENGTH_ERR	R/RC	0x0	Packet Length Error detected for received CSI packet If set, this bit indicates a packet length error was detected on at least one CSI packet received from the sensor. Packet length errors occur if the data length field in the packet header does not match the actual data length for the packet. 1: One or more Packet Length errors have been detected 0: No Packet Length errors have been detected This bit is cleared on read.
2	CKSUM_ERR	R/RC	0x0	Data Checksum Error detected for received CSI packet If set, this bit indicates a data checksum error was detected on at least one CSI packet received from the sensor. Data checksum errors indicate an error was detected in the packet data portion of the CSI packet. 1: One or more Data Checksum errors have been detected 0: No Data Checksum errors have been detected This bit is cleared on read.
1	ECC2_ERR	R/RC	0x0	2-bit ECC Error detected for received CSI packet If set, this bit indicates a multi-bit ECC error was detected on at least one CSI packet received from the sensor. Multi-bit errors are not corrected by the device. 1: One or more multi-bit ECC errors have been detected 0: No multi-bit ECC errors have been detected This bit is cleared on read.

表 7-132. CSI_RX_STS (Address 0x7A) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	ECC1_ERR	R/RC	0x0	1-bit ECC Error detected for received CSI packet If set, this bit indicates a single-bit ECC error was detected on at least one CSI packet received from the sensor. Single-bit errors are corrected by the device. 1: One or more 1-bit ECC errors have been detected 0: No 1-bit ECC errors have been detected This bit is cleared on read.

7.6.115 CSI_ERR_COUNTER Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-133. CSI_ERR_COUNTER (Address 0x7B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_ERR_CNT	R/RC	0x00	CSI Error Counter Register This register counts the number of CSI packets received with errors since the last read of the counter.

7.6.116 PORT_CONFIG2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-134. PORT_CONFIG2 (Address 0x7C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data is processed as 8-bit data and packed accordingly for transmission over CSI. 00 : Normal Raw10 Mode 01 : Reserved 10 : 8-bit processing using upper 8 bits. When selecting this value, change CSI data type value RAW10_DT in register 0x70[5:0] 11 : 8-bit processing using lower 8 bits. When selecting this value, change CSI data type value RAW10_DT in register 0x70[5:0]
5	DISCARD_ON_PAR_ERR	R/W	0x1	Discard frames on Parity Error 0 : Forward packets with parity errors 1 : Truncate Frames if a parity error is detected
4	DISCARD_ON_LINE_SIZE	R/W	0x0	Discard frames on Line Size 0 : Allow changes in Line Size within packets 1 : Truncate Frames if a change in line size is detected
3	DISCARD_ON_FRAME_SIZE	R/W	0x0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0 : Allow changes in Frame Size 1 : Truncate Frames if a change in frame size is detected
2	RESERVED	R/W	0x0	Reserved
1	LV_POLARITY	R/W	0x0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1 : LineValid is low for the duration of the video line 0 : LineValid is high for the duration of the video line

表 7-134. PORT_CONFIG2 (Address 0x7C) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	FV_POLARITY	R/W	0x0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1 : FrameValid is low for the duration of the video frame 0 : FrameValid is high for the duration of the video frame

7.6.117 PORT_PASS_CTL Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-135. PORT_PASS_CTL (Address 0x7D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	PASS_DISCARD_EN	R/W	0x0	Pass Discard Enable Discard packets if PASS is not indicated. 0 : Ignore PASS for forwarding packets 1 : Discard packets when PASS is not true
6	RESERVED	R/W	0x0	Reserved
5	PASS_LINE_CNT	R/W	0x0	Pass Line Count Control This register controls whether the device will include line count in qualification of the Pass indication: 0 : Don't check line count 1 : Check line count When checking line count, Pass is deasserted upon detection of a change in the number of video lines per frame. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
4	PASS_LINE_SIZE	R/W	0x0	Pass Line Size Control This register controls whether the device will include line size in qualification of the Pass indication: 0 : Don't check line size 1 : Check line size When checking line size, Pass is deasserted upon detection of a change in video line size. Pass will not be reasserted until the PASS_THRESHOLD setting is met.
3	PASS_PARITY_ERR	R/W	x00	Parity Error Mode If this bit is set to 0, the port Pass indication is deasserted for every parity error detected on the FPD-Link III Receive interface. If this bit is set to a 1, the port Pass indication is cleared on a parity error and remain clear until the PASS_THRESHOLD is met. When PASS_PARITY_ERR is set to 1, TI also recommends setting PASS_THRESHOLD to 2 or higher to ensure at least one good frame occurs following a parity error
2	PASS_WDOG_DIS	R/W	0x0	RX Port Pass Watchdog disable When enabled, if the FPD Receiver does not detect a valid frame end condition within two video frame periods, the Pass indication is deasserted. The watchdog timer will not have any effect if the PASS_THRESHOLD is set to 0. 0 : Enable watchdog timer for RX Pass 1 : Disable watchdog timer for RX Pass
1:0	PASS_THRESHOLD	R/W	0x0	Pass Threshold Register This register controls the number of valid frames before asserting the port Pass indication. If set to 0, PASS is asserted after Receiver Lock detect. If non-zero, PASS is asserted following reception of the programmed number of valid frames.

7.6.118 SEN_INT_RISE_CTL Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-136. SEN_INT_RISE_CTL (Address 0x7E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT _RISE_MASK	R/W	0x0	Sensor Interrupt Rise Mask This register provides the interrupt mask for detecting rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_RISE_STS register.

7.6.119 SEN_INT_FALL_CTL Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-137. SEN_INT_FALL_CTL (Address 0x7F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT _FALL_MASK	R/W	0x0	Sensor Interrupt Fall Mask This register provides the interrupt mask for detecting falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in this register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in the SEN_INT_FALL_STS register.

7.6.120 RESERVED Register

表 7-138. RESERVED (Address 0xA0 – 0xA4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.121 REFCLK_FREQ Register

表 7-139. REFCLK_FREQ (Address 0xA5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	REFCLK_FREQ	R	0x00	REFCLK frequency measurement in MHz. REFCLK_FREQ measurement is not synchronized. Value in this register should read twice and only considered valid if REFCLK_FREQ is unchanged between reads.

7.6.122 RESERVED Register

表 7-140. RESERVED (Address 0xA7 – 0xAF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x00	Reserved

7.6.123 IND_ACC_CTL Register

表 7-141. IND_ACC_CTL (Address 0xB0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved
5:2	IA_SEL	R/W	0x0	Indirect Access Register Select: Selects target for register access 0000 : CSI-2 Pattern Generator & Timing Registers 0001 : FPD-Link III RX Port 0 Reserved Registers 0010 : FPD-Link III RX Port 1 Reserved Registers 00011–0100: Reserved 0101 : FPD-Link III RX Shared Reserved Registers 0110 : Simultaneous write to FPD-Link III RX Reserved Registers 0111 : CSI-2 Reserved Registers 1000–1111 : Reserved
1	IA_AUTO_INC	R/W	0x0	Indirect Access Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
0	IA_READ	R/W	0x0	Indirect Access Read: Setting this allows generation of a read strobe to the selected register block upon setting of the IND_ACC_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the IND_ACC_DATA register. This function is only required for blocks that need to pre-fetch register data.

7.6.124 IND_ACC_ADDR Register

表 7-142. IND_ACC_ADDR (Address 0xB1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IA_ADDR	R/W	0x0	Indirect Access Register Offset: This register contains the 8-bit register offset for the indirect access.

7.6.125 IND_ACC_DATA Register

表 7-143. IND_ACC_DATA (Address 0xB2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	IA_DATA	R/W	0x0	Indirect Access Data: Writing this register will cause an indirect write of the IND_ACC_DATA value to the selected analog block register. Reading this register will return the value of the selected block register

7.6.126 BIST Control Register

表 7-144. BIST Control (Address 0xB3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	BIST_OUT_MODE	R/W	0x0	BIST Output Mode 00 : Outputs disabled during BIST 01 : Reserved 10 : Outputs enabled during BIST 11 : Reserved
5:4	RESERVED	R/W	0x0	Reserved
3	BIST_PIN_CONFIG	R/W	0x1	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
2:1	BIST_CLOCK_SOURCE	R/W	0x00	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. When connected to a DS90UB913A/933, a setting of 0x3 may result in a clock frequency that is too slow for proper recovery.
0	BIST_EN	R/W	0x0	BIST Control 1: Enabled 0: Disabled

7.6.127 RESERVED Register

表 7-145. RESERVED (Address 0xB4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x25	Reserved

7.6.128 RESERVED Register

表 7-146. RESERVED (Address 0xB5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.129 RESERVED Register

表 7-147. RESERVED (Address 0xB6)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x18	Reserved

7.6.130 RESERVED Register

表 7-148. RESERVED (Address 0xB7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.131 MODE_IDX_STS Register

表 7-149. MODE_IDX_STS (Address 0xB8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	IDX_DONE	R	0x1	IDX Done If set, indicates the IDX decode has completed and latched into the IDX status bits.
6:4	IDX	R	S	IDX Decode 3-bit decode from IDX pin
3	MODE_DONE	R	0x1	MODE Done If set, indicates the MODE decode has completed and latched into the MODE status bits.
2:0	MODE	R	S	MODE Decode 3-bit decode from MODE pin

7.6.132 LINK_ERROR_COUNT Register

表 7-150. LINK_ERROR_COUNT (Address 0xB9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved
5	LINK_SFIL_WAIT	R/W	0x1	During SFILTER adaption, setting this bit will cause the Lock detect circuit to ignore errors during the SFILTER wait period after the SFILTER control is updated. 1: Errors during SFILTER Wait period will be ignored 0: Errors during SFILTER Wait period will not be ignored and may cause loss of Lock
4	LINK_ERR _COUNT_EN	R/W	0x1	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
3:0	LINK_ERR _THRESH	R/W	0x3	Link error count threshold. The Link Error Counter monitors the forward channel link and determines when link will be dropped. The link error counter is pixel clock based. FPD Link parity, clock, and control are monitored for link errors. If the error counter is enabled, the deserializer will lose lock once the error counter reaches the LINK_ERR_THRESH value. If the link error counter is disabled, the deserilizer will lose lock after one error.

7.6.133 FPD3_ENC_CTL Register

It is recommended to enable CRC error checking on the FPD3 Encoder sequence to prevent any updates of link information values from encoded packets that do not pass CRC check. The FPD3 Encoder CRC is enabled by setting the FPD3_ENC_CRC_DIS register 0xBA[7] to 0. In addition, the FPD3_ENC_CRC_CAP flag should be set in register 0x4A[4].

表 7-151. FPD3_ENC_CTL (Address 0xBA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	FPD3_ENC_CRC_DI S	R/W	0x1	0: Enable FPD-Link III encoder CRC (recommended) 1: Disable FPD-Link III encoder CRC
6:0	RESERVED	R/W	0x03	Reserved

7.6.134 RESERVED Register

表 7-152. RESERVED (Address 0xBB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x74	Reserved

7.6.135 FV_MIN_TIME Register

表 7-153. FV_MIN_TIME (Address 0xBC)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FRAME_VALID_MIN	R/W	0x80	Frame Valid Minimum Time in RAW input mode. This register controls the minimum time the FrameValid (FV) should be active before the Raw mode FPD-Link III receiver generates a FrameStart packet. Duration is in FPD-Link III clock periods.

7.6.136 RESERVED Register

表 7-154. RESERVED (Address 0xBD)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.137 GPIO_PD_CTL Register

表 7-155. GPIO_PD_CTL (Address 0xBE)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	GPIO6_PD_DIS	R/W	0x0	GPIOX Pulldown Resistor Disable: The GPIO pins by default include a 35-kΩ typical pulldown resistor that is automatically enabled when the GPIO is not in an output mode. When this bit is set, the corresponding pulldown resistor will also be disabled when the GPIO pin is in an input only mode. 1 : Disable GPIO pulldown resistor 0 : Enable GPIO pulldown resistor
5	GPIO5_PD_DIS	R/W	0x0	
4	GPIO4_PD_DIS	R/W	0x0	
3	GPIO3_PD_DIS	R/W	0x0	
2	GPIO2_PD_DIS	R/W	0x0	
1	GPIO1_PD_DIS	R/W	0x0	
0	GPIO0_PD_DIS	R/W	0x0	

7.6.138 RESERVED Register

表 7-156. RESERVED (Address 0xBF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.139 PORT_DEBUG Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-157. PORT_DEBUG (Address 0xD0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	SER_BIST_ACT	R	0x0	Serializer BIST active This register indicates the Serializer is in BIST mode. When in BIST mode this flag can be checked to ensure BIST is activated in the serializer during the test. If the Deserializer is not in BIST mode, this could indicate an error condition.
4:2	RESERVED	R/W	0x0	Reserved
1	FORCE _BC_ERRORS	R/W	0x0	Setting this bit introduces continuous single bit errors into Back Channel Frames
0	FORCE _1_BC_ERROR	R/W	0x0	Setting this bit introduces a single bit error into one Back Channel Frame

7.6.140 RESERVED Register

表 7-158. RESERVED Register (Address 0xD1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	-	0x43	Reserved

7.6.141 AEQ_CTL2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-159. AEQ_CTL2 (Address 0xD2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	ADAPTIVE_EQ _RELOCK_TIME	R/W	0x4	Time to wait for lock before incrementing the EQ to next setting 000 : 164 µs 001 : 328 µs 010 : 655 µs 011 : 1.31 ms 100 : 2.62 ms 101 : 5.24 ms 110 : 10.5 ms 111 : 21.0 ms
4	AEQ_1ST_LOCK _MODE	R/W	0x1	AEQ First Lock Mode. This register bit controls the Adaptive Equalizer algorithm operation at initial Receiver Lock. 0 : Initial AEQ lock may occur at any value 1 : Initial Receiver lock will restart AEQ at 0, providing a more deterministic initial AEQ value
3	AEQ_RESTART	(R/W)/SC	0x0	Set high to restart AEQ adaptation from initial value. This bit is self clearing. Adaption is restarted.
2	SET_AEQ_FLOOR	R/W	0x1	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations
1:0	RESERVED	R	0x0	Reserved

7.6.142 AEQ_STATUS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-160. AEQ_STATUS (Address 0xD3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RESERVED	R	0x0	Reserved
5:0	EQ_STATUS	R	0x00	Adaptive EQ Status

7.6.143 ADAPTIVE EQ BYPASS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-161. ADAPTIVE EQ BYPASS (Address 0xD4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	EQ_STAGE_1 _SELECT_VALUE	R/W	0x3	EQ select value [5:3] - Used if adaptive EQ is bypassed.
4	AEQ_LOCK_MODE	R/W	0x0	Adaptive Equalizer lock mode When set to a 1, Receiver Lock status requires the Adaptive Equalizer to complete adaption. When set to a 0, Receiver Lock is based only on the Lock circuit itself. AEQ may not have stabilized.

表 7-161. ADAPTIVE EQ BYPASS (Address 0xD4) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
3:1	EQ_STAGE_2 _SELECT_VALUE	R/W	0x0	EQ select value [2:0] - Used if adaptive EQ is bypassed.
0	ADAPTIVE_EQ _BYPASS	R/W	0x0	1: Disable adaptive EQ 0: Enable adaptive EQ

7.6.144 AEQ_MIN_MAX Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-162. AEQ_MIN_MAX (Address 0xD5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:4	AEQ_MAX	R/W	0xF	Adaptive Equalizer Maximum value This register sets the maximum value for the Adaptive EQ algorithm. Must be higher than ADAPTIVE_EQ_FLOOR_VALUE when SET_AEQ_FLOOR is enabled.
3:0	ADAPTIVE_EQ _FLOOR_VALUE	R/W	0x2	When AEQ floor is enabled by register 0xD2[2] the starting EQ gain setting for AEQ adaption is given by this register.

7.6.145 RESERVED Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-163. RESERVED (Address 0xD6)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.146 RESERVED Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-164. RESERVED (Address 0xD7)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x00	Reserved

7.6.147 PORT_ICR_HI Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-165. PORT_ICR_HI (Address 0xD8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	RESERVED	R	0x0	Reserved
2	IE_FPD3_ENC_ERR	R/W	0x0	Interrupt on FPD-Link III Receiver Encoding Error When enabled, an interrupt is generated on detection of an encoding error on the FPD-Link III interface for the receive port as reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register
1	IE_BCC_SEQ_ERR	R/W	0x0	Interrupt on BCC SEQ Sequence Error. When enabled, an interrupt is generated if a Sequence Error is detected for the Bi-directional Control Channel forward channel receiver as reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register.
0	IE_BCC_CRC_ERR	R/W	0x0	Interrupt on BCC CRC error detect When enabled, an interrupt is generated if a CRC error is detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel as reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register.

7.6.148 PORT_ICR_LO Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-166. PORT_ICR_LO (Address 0xD9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R/W	0x0	Reserved
6	IE_LINE_LEN_CHG	R/W	0x0	Interrupt on Video Line length When enabled, an interrupt is generated if the length of the video line changes. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register.
5	IE_LINE_CNT_CHG	R/W	0x0	Interrupt on Video Line count When enabled, an interrupt is generated if the number of video lines per frame changes. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register.
4	IE_BUFFER_ERR	R/W	0x0	Interrupt on Receiver Buffer Error When enabled, an interrupt is generated if the Receive Buffer overflow is detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register.
3	IE_CSI_RX_ERR	R/W	0x0	Interrupt on CSI Receiver Error. When enabled, an interrupt will be generated on detection of an error by the CSI Receiver. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A).
2	IE_FPD3_PAR_ERR	R/W	0x0	Interrupt on FPD-Link III Receiver Parity Error When enabled, an interrupt is generated on detection of parity errors on the FPD-Link III interface for the receive port. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register.
1	IE_PORT_PASS	R/W	0x0	Interrupt on change in Port PASS status When enabled, an interrupt is generated on a change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register.
0	IE_LOCK_STS	R/W	0x0	Interrupt on change in Lock Status When enabled, an interrupt is generated on a change in lock status. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register.

7.6.149 PORT_ISR_HI Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-167. PORT_ISR_HI (Address 0xDA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved	R	0x0	Reserved
4	IE_FC_GPIO	R	0x0	FC GPIO Interrupt Status A change in forward channel GPIO signal has been detected. Forward Channel GPIO status is reported in the FC_GPIO_STS register. This interrupt condition will be cleared by reading the FC_GPIO_STS register.
3	IE_FC_SENS_STS	R	0x0	Interrupt on change in Sensor Status A change in Sensor Status has been detected. Camera Status is reported in the SENSOR_STS_X registers. This interrupt condition will be cleared by reading the SEN_INT_RISE_STS and SEN_INT_FALL_STS registers.
2	IS_FPD3_ENC_ERR	R	0x0	FPD-Link III Receiver Encode Error Interrupt Status An encoding error on the FPD-Link III interface for the receive port has been detected. Status is reported in the FPD3_ENC_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
1	IS_BCC_SEQ_ERR	R	0x0	BCC CRC Sequence Error Interrupt Status A Sequence Error has been detected for the Bi-directional Control Channel forward channel receiver. Status is reported in the BCC_SEQ_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_BCC_CRC_ERR	R	0x0	BCC CRC error detect Interrupt Status A CRC error has been detected on a Bi-directional Control Channel frame received over the FPD-Link III forward channel. Status is reported in the BCC_CRC_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

7.6.150 PORT_ISR_LO Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-168. PORT_ISR_LO (Address 0xDB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	RESERVED	R	0x0	Reserved
6	IS_LINE_LEN_CHG	R	0x0	Video Line Length Interrupt Status A change in video line length has been detected. Status is reported in the LINE_LEN_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
5	IS_LINE_CNT_CHG	R	0x0	Video Line Count Interrupt Status A change in number of video lines per frame has been detected. Status is reported in the LINE_CNT_CHG bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
4	IS_BUFFER_ERR	R	0x0	Receiver Buffer Error Interrupt Status A Receive Buffer overflow has been detected as reported in the BUFFER_ERROR bit in the RX_PORT_STS2 register. This interrupt condition is cleared by reading the RX_PORT_STS2 register.
3	IS_CSI_RX_ERR	R	0x0	CSI Receiver Error Interrupt Status The CSI Receiver has detected an error. CSI Receiver errors are reported in the CSI_RX_STS register (address 0x7A). This interrupt condition will be cleared by reading the CSI_RX_STS register.
2	IS_FPD3_PAR_ERR	R	0x0	FPD-Link III Receiver Parity Error Interrupt Status A parity error on the FPD-Link III interface for the receive port has been detected. Parity error status is reported in the PARITY_ERROR bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
1	IS_PORT_PASS	R	0x0	Port Valid Interrupt Status A change in receiver port valid status as reported in the PORT_PASS bit in the PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.
0	IS_LOCK_STS	R	0x0	Lock Interrupt Status A change in lock status has been detected. Status is reported in the LOCK_STS_CHG bit in the RX_PORT_STS1 register. This interrupt condition is cleared by reading the RX_PORT_STS1 register.

7.6.151 FC_GPIO_STS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-169. FC_GPIO_STS (Address 0xDC)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO3_INT_STS	R/RC	0x0	GPIO3 Interrupt Status. This bit indicates an interrupt condition has been met for GPIO3. This bit is cleared on read.
6	GPIO2_INT_STS	R/RC	0x0	GPIO2 Interrupt Status. This bit indicates an interrupt condition has been met for GPIO2. This bit is cleared on read.
5	GPIO1_INT_STS	R/RC	0x0	GPIO1 Interrupt Status. This bit indicates an interrupt condition has been met for GPIO1. This bit is cleared on read.
4	GPIO0_INT_STS	R/RC	0x0	GPIO0 Interrupt Status. This bit indicates an interrupt condition has been met for GPIO0. This bit is cleared on read.
3	FC_GPIO3_STS	R	0x0	Forward Channel GPIO3 Status. This bit indicates the current value for forward channel GPIO3.
2	FC_GPIO2_STS	R	0x0	Forward Channel GPIO2 Status. This bit indicates the current value for forward channel GPIO2.
1	FC_GPIO1_STS	R	0x0	Forward Channel GPIO1 Status. This bit indicates the current value for forward channel GPIO1.
0	FC_GPIO0_STS	R	0x0	Forward Channel GPIO0 Status. This bit indicates the current value for forward channel GPIO0.

7.6.152 FC_GPIO_ICR Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-170. FC_GPIO_ICR (Address 0xDD)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	GPIO3_FALL_IE	R/W	0x0	GPIO3 Fall Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO3.
6	GPIO3_RISE_IE	R/W	0x0	GPIO3 Rise Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO3.
5	GPIO2_FALL_IE	R/W	0x0	GPIO2 Fall Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO2.
4	GPIO2_RISE_IE	R/W	0x0	GPIO2 Rise Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO2.
3	GPIO1_FALL_IE	R/W	0x0	GPIO1 Fall Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO1.
2	GPIO1_RISE_IE	R/W	0x0	GPIO1 Rise Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO1.
1	GPIO0_FALL_IE	R/W	0x0	GPIO0 Fall Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a falling edge on GPIO0.

表 7-170. FC_GPIO_ICR (Address 0xDD) (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	GPIO0_RISE_IE	R/W	0x0	GPIO0 Rise Interrupt Enable. If this bit is set, an interrupt will be generated based on detection of a rising edge on GPIO0.

7.6.153 SEN_INT_RISE_STS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-171. SEN_INT_RISE_STS (Address 0xDE)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_RISE	R/RC	0x00	Sensor Interrupt Rise Status. This register provides the interrupt status for rising edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_RISE_MASK register, a rising edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

7.6.154 SEN_INT_FALL_STS Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

表 7-172. SEN_INT_FALL_STS (Address 0xDF)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	SEN_INT_FALL	R/RC	0x00	Sensor Interrupt Fall Status. This register provides the interrupt status for falling edge transitions on the bits in SENSOR_STS_0. If a mask bit is set in the SEN_INT_RISE_MASK register, a falling edge transition on the corresponding SENSOR_STS_0 bit will generate an interrupt that will be latched in this register.

7.6.155 FPD3_RX_ID0 Register

表 7-173. FPD3_RX_ID0 (Address 0xF0)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID0	R	0x5F	FPD3_RX_ID0: First byte ID code: '_'

7.6.156 FPD3_RX_ID1 Register

表 7-174. FPD3_RX_ID1 (Address 0xF1)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID1	R	0x55	FPD3_RX_ID1: 2nd byte of ID code: 'U'

7.6.157 FPD3_RX_ID2 Register

表 7-175. FPD3_RX_ID2 (Address 0xF2)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID2	R	0x42	FPD3_RX_ID2: 3rd byte of ID code: 'B'

7.6.158 FPD3_RX_ID3 Register

表 7-176. FPD3_RX_ID3 (Address 0xF3)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID3	R	0x39	FPD3_RX_ID3: 4th byte of ID code: '9'

7.6.159 FPD3_RX_ID4 Register

表 7-177. FPD3_RX_ID4 (Address 0xF4)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID4	R	0x35	FPD3_RX_ID4: 5th byte of ID code: '5'

7.6.160 FPD3_RX_ID5 Register

表 7-178. FPD3_RX_ID5 (Address 0xF5)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FPD3_RX_ID5	R	0x34	FPD3_RX_ID5: 6th byte of ID code: '4'

7.6.161 I2C_RX0_ID Register

As an alternative to paging to access FPD-Link III receive port0 registers, a separate I2C address may be enabled to allow direct access to the port 0 specific registers. The I2C_RX_0_ID register provides a simpler method of accessing device registers specifically for port 0 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

表 7-179. I2C_RX0_ID (Address 0xF8)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT0_ID	R/W	0x0	7-bit Receive Port 0 I2C ID Configures the decoder for detecting transactions designated for Receiver port 0 registers. A value of 0x00 in this field disables the Port0 decoder.
0	RESERVED	R	0x0	Reserved

7.6.162 I2C_RX1_ID Register

As an alternative to paging to access FPD-Link III receive port 1 registers, a separate I2C address may be enabled to allow direct access to the port 1 specific registers. The I2C_RX_1_ID register provides a simpler method of accessing device registers specifically for port 1 without having to use the paging function to select the register page. Using this address also allows access to all shared registers.

表 7-180. I2C_RX1_ID (Address 0xF9)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RX_PORT1_ID	R/W	0x0	7-bit Receive Port 1 I2C ID Configures the decoder for detecting transactions designated for Receiver port 1 registers. A value of 0x00 in this field disables the Port1 decoder.
0	RESERVED	R	0x0	Reserved

7.6.163 RESERVED Register

表 7-181. RESERVED (Address 0xFA)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x00	Reserved

7.6.164 RESERVED Register

表 7-182. RESERVED (Address 0xFB)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x00	Reserved

7.6.165 Indirect Access Registers

Several functional blocks include register sets contained in the Indirect Access map (表 7-183); that is, Pattern Generator, CSI-2 timing, and Analog controls. Register access is provided via an indirect access mechanism through the Indirect Access registers (IND_ACC_CTL, IND_ACC_ADDR, and IND_ACC_DATA). These registers are located at offsets 0xB0-0xB2 in the main register space.

The indirect address mechanism involves setting the control register to select the desired block, setting the register offset address, and reading or writing the data register. In addition, an auto-increment function is provided in the control register to automatically increment the offset address following each read or write of the data register.

For writes, the process is as follows:
1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Write the data value to the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will write additional data bytes to subsequent register offset locations

For reads, the process is as follows:
1. Write to the IND_ACC_CTL register to select the desired register block
2. Write to the IND_ACC_ADDR register to set the register offset
3. Read from the IND_ACC_DATA register

If auto-increment is set in the IND_ACC_CTL register, repeating step 3 will read additional data bytes from subsequent register offset locations.

7.6.166

表 7-183. Indirect Register Map Description

IA SELECT 0xB0[5:2]	PAGE/BLOCK	INDIRECT REGISTERS	ADDRESS RANGE	DESCRIPTION
0000	0	Digital Page 0 Indirect Registers	0x01-0x1F	Pattern Gen Registers
			0x40-0x48	CSI TX port 0 Timing Registers
0001	1	FPD-Link III Channel 0 Reserved Registers	0x00-0x14	Test and Debug registers
0010	2	FPD-Link III Channel 1 Reserved Registers	0x00-0x14	Test and Debug registers
0011	3	Reserved	0x00-0x14	Reserved
0100	4	Reserved	0x00-0x14	Reserved
0101	5	FPD-Link III Share Reserved Registers	0x00-0x04	Test and Debug registers
0110	6	Write All FPD-Link III Reserved Registers	0x00-0x14	Test and Debug registers
0111	7	CSI TX Reserved Registers	0x00-0x1D	Test and Debug registers

7.6.167 Reserved Register

表 7-184. Reserved (Indirect Address Page 0x00; Register 0x00)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R	0x0	Reserved

7.6.168 PGEN_CTL Register

表 7-185. PGEN_CTL (Indirect Address Page 0x00; Register 0x01)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	RESERVED	R/W	0x0	Reserved
0	PGEN_ENABLE	R/W	0x0	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

7.6.169 PGEN_CFG Register

表 7-186. PGEN_CFG (Indirect Address Page 0x00; Register 0x02)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	PGEN_FIXED_EN	R/W	0x0	Fixed Pattern Enable Setting this bit enables Fixed Color Patterns. 0 : Send Color Bar Pattern 1 : Send Fixed Color Pattern
6	RESERVED	R/W	0x0	Reserved
5:4	NUM_CBARS	R/W	0x3	Number of Color Bars 00 : 1 Color Bar 01 : 2 Color Bars 10 : 4 Color Bars 11 : 8 Color Bars
3:0	BLOCK_SIZE	R/W	0x3	Block Size For Fixed Color Patterns, this field controls the size of the fixed color field in bytes. Allowed values are 1 to 15.

7.6.170 PGEN_CSI_DI Register

表 7-187. PGEN_CSI_DI (Indirect Address Page 0x00; Register 0x03)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	PGEN_CSI_VC	R/W	0x0	CSI Virtual Channel Identifier This field controls the value sent in the CSI packet for the Virtual Channel Identifier
5:0	PGEN_CSI_DT	R/W	0x24	CSI Data Type This field controls the value sent in the CSI packet for the Data Type. The default value (0x24) indicates RGB888.

7.6.171 PGEN_LINE_SIZE1 Register

表 7-188. PGEN_LINE_SIZE1 (Indirect Address Page 0x00; Register 0x04)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[15:8]	R/W	0x07	Most significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

7.6.172 PGEN_LINE_SIZE0 Register

表 7-189. PGEN_LINE_SIZE0 (Indirect Address Page 0x00; Register 0x05)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_SIZE[7:0]	R/W	0x80	Least significant byte of the Pattern Generator line size. This is the active line length in bytes. Default setting is for 1920 bytes for a 640 pixel line width.

7.6.173 PGEN_BAR_SIZE1 Register

表 7-190. PGEN_BAR_SIZE1 (Indirect Address Page 0x00; Register 0x06)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[15:8]	R/W	0x0	Most significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.6.174 PGEN_BAR_SIZE0 Register

表 7-191. PGEN_BAR_SIZE0 (Indirect Address Page 0x00; Register 0x07)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_BAR_SIZE[7:0]	R/W	0xF0	Least significant byte of the Pattern Generator color bar size. This is the active length in bytes for the color bars. This value is used for all except the last color bar. The last color bar is determined by the remaining bytes as defined by the PGEN_LINE_SIZE value.

7.6.175 PGEN_ACT_LPF1 Register

表 7-192. PGEN_ACT_LPF1 (Indirect Address Page 0x00; Register 0x08)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[15:8]	R/W	0x01	Active Lines Per Frame Most significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.6.176 PGEN_ACT_LPF0 Register

表 7-193. PGEN_ACT_LPF0 (Indirect Address Page 0x00; Register 0x09)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_ACT_LPF[7:0]	R/W	0xE0	Active Lines Per Frame Least significant byte of the number of active lines per frame. Default setting is for 480 active lines per frame.

7.6.177 PGEN_TOT_LPF1 Register

表 7-194. PGEN_TOT_LPF1 (Indirect Address Page 0x00; Register 0x0A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[15:8]	R/W	0x02	Total Lines Per Frame Most significant byte of the number of total lines per frame including vertical blanking

7.6.178 PGEN_TOT_LPF0 Register

表 7-195. PGEN_TOT_LPF0 (Indirect Address Page 0x00; Register 0x0B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_TOT_LPF[7:0]	R/W	0x0D	Total Lines Per Frame Least significant byte of the number of total lines per frame including vertical blanking

7.6.179 PGEN_LINE_PD1 Register

表 7-196. PGEN_LINE_PD1 (Indirect Address Page 0x00; Register 0x0C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[15:8]	R/W	0x0C	Line Period Most significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

7.6.180 PGEN_LINE_PD0 Register

表 7-197. PGEN_LINE_PD0 (Indirect Address Page 0x00; Register 0x0D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_LINE_PD[7:0]	R/W	0x67	Line Period Least significant byte of the line period in 10ns units. The default setting for the line period registers sets a line period of 31.75 microseconds.

7.6.181 PGEN_VBP Register

表 7-198. PGEN_VBP (Indirect Address Page 0x00; Register 0x0E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VBP	R/W	0x21	Vertical Back Porch This value provides the vertical back porch portion of the vertical blanking interval. This value provides the number of blank lines between the FrameStart packet and the first video data packet.

7.6.182 PGEN_VFP Register

表 7-199. PGEN_VFP (Indirect Address Page 0x00; Register 0x0F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_VFP	R/W	0x0A	Vertical Front Porch This value provides the vertical front porch portion of the vertical blanking interval. This value provides the number of blank lines between the last video line and the FrameEnd packet.

7.6.183 PGEN_COLOR0 Register

表 7-200. PGEN_COLOR0 (Indirect Address Page 0x00; Register 0x10)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR0	R/W	0xAA	Pattern Generator Color 0 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 0.For Fixed Color Patterns, this register controls the first byte of the fixed color pattern.

7.6.184 PGEN_COLOR1 Register

表 7-201. PGEN_COLOR1 (Indirect Address Page 0x00; Register 0x11)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR1	R/W	0x33	Pattern Generator Color 1 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 1. For Fixed Color Patterns, this register controls the second byte of the fixed color pattern.

7.6.185 PGEN_COLOR2 Register

表 7-202. PGEN_COLOR2 (Indirect Address Page 0x00; Register 0x12)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR2	R/W	0xF0	Pattern Generator Color 2 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 2. For Fixed Color Patterns, this register controls the third byte of the fixed color pattern.

7.6.186 PGEN_COLOR3 Register

表 7-203. PGEN_COLOR3 (Indirect Address Page 0x00; Register 0x13)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR3	R/W	0x7F	Pattern Generator Color 3 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 3. For Fixed Color Patterns, this register controls the fourth byte of the fixed color pattern.

7.6.187 PGEN_COLOR4 Register

表 7-204. PGEN_COLOR4 (Indirect Address Page 0x00; Register 0x14)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR4	R/W	0x55	Pattern Generator Color 4 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 4. For Fixed Color Patterns, this register controls the fifth byte of the fixed color pattern.

7.6.188 PGEN_COLOR5 Register

表 7-205. PGEN_COLOR5 (Indirect Address Page 0x00; Register 0x15)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR5	R/W	0xCC	Pattern Generator Color 5 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 5. For Fixed Color Patterns, this register controls the sixth byte of the fixed color pattern.

7.6.189 PGEN_COLOR6 Register

表 7-206. PGEN_COLOR6 (Indirect Address Page 0x00; Register 0x16)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR6	R/W	0x0F	Pattern Generator Color 6 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 6. For Fixed Color Patterns, this register controls the seventh byte of the fixed color pattern.

7.6.190 PGEN_COLOR7 Register

表 7-207. PGEN_COLOR7 (Indirect Address Page 0x00; Register 0x17)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR7	R/W	0x80	Pattern Generator Color 7 For Reference Color Bar Patterns, this register controls the byte data value sent during color bar 7. For Fixed Color Patterns, this register controls the eighth byte of the fixed color pattern.

7.6.191 PGEN_COLOR8 Register

表 7-208. PGEN_COLOR8 (Indirect Address Page 0x00; Register 0x18)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR8	R/W	0x0	Pattern Generator Color 8 For Fixed Color Patterns, this register controls the ninth byte of the fixed color pattern.

7.6.192 PGEN_COLOR9 Register

表 7-209. PGEN_COLOR9 (Indirect Address Page 0x00; Register 0x19)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR9	R/W	0x0	Pattern Generator Color 9 For Fixed Color Patterns, this register controls the tenth byte of the fixed color pattern.

7.6.193 PGEN_COLOR10 Register

表 7-210. PGEN_COLOR10 (Indirect Address Page 0x00; Register 0x1A)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR10	R/W	0x0	Pattern Generator Color 10 For Fixed Color Patterns, this register controls the eleventh byte of the fixed color pattern.

7.6.194 PGEN_COLOR11 Register

表 7-211. PGEN_COLOR11 (Indirect Address Page 0x00; Register 0x1B)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR11	R/W	0x0	Pattern Generator Color 11 For Fixed Color Patterns, this register controls the twelfth byte of the fixed color pattern.

7.6.195 PGEN_COLOR12 Register

表 7-212. PGEN_COLOR12 (Indirect Address Page 0x00; Register 0x1C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR12	R/W	0x0	Pattern Generator Color 12 For Fixed Color Patterns, this register controls the thirteenth byte of the fixed color pattern.

7.6.196 PGEN_COLOR13 Register

表 7-213. PGEN_COLOR13 (Indirect Address Page 0x00; Register 0x1D)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR13	R/W	0x0	Pattern Generator Color 13 For Fixed Color Patterns, this register controls the fourteenth byte of the fixed color pattern.

7.6.197 PGEN_COLOR14 Register

表 7-214. PGEN_COLOR14 (Indirect Address Page 0x00; Register 0x1E)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	PGEN_COLOR14	R/W	0x0	Pattern Generator Color 14 For Fixed Color Patterns, this register controls the fifteenth byte of the fixed color pattern.

7.6.198 RESERVED Register

表 7-215. RESERVED (Indirect Address Page 0x00; Register 0x1F)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	RESERVED	R/W	0x0	Reserved

7.6.199 CSI0_TCK_PREP Register

表 7-216. CSI0_TCK_PREP (Indirect Address Page 0x00; Register 0x40)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_PREP_OV	R/W	0x0	Override CSI Tck-prep parameter 0: Tck-prep is automatically determined 1: Override Tck-prep with value in bits 6:0 of this register
6:0	MR_TCK_PREP	R R/W	0x0	Tck-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.200 CSI0_TCK_ZERO Register

表 7-217. CSI0_TCK_ZERO (Indirect Address Page 0x00; Register 0x41)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_ZERO_OV	RW	0x0	Override CSI Tck-zero parameter 0: Tck-zero is automatically determined 1: Override Tck-zero with value in bits 6:0 of this register
6:0	MR_TCK_ZERO	R RW	0x0	Tck-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.201 CSI0_TCK_TRAIL Register

表 7-218. CSI0_TCK_TRAIL (Indirect Address Page 0x00; Register 0x42)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_TRAIL_OV	R/W	0x0	Override CSI Tck-trail parameter 0: Tck-trail is automatically determined 1: Override Tck-trail with value in bits 6:0 of this register
6:0	MR_TCK_TRAIL	R R/W	0x0	Tck-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.202 CSI0_TCK_POST Register

表 7-219. CSI0_TCK_POST (Indirect Address Page 0x00; Register 0x43)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TCK_POST_OV	R/W	0x0	Override CSI Tck-post parameter 0: Tck-post is automatically determined 1: Override Tck-post with value in bits 6:0 of this register
6:0	MR_TCK_POST	R R/W	0x0	Tck-post value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.203 CSI0_THS_PREP Register

表 7-220. CSI0_THS_PREP (Indirect Address Page 0x00; Register 0x44)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_PREP_OV	R/W	0x0	Override CSI Ths-prep parameter 0: Ths-prep is automatically determined 1: Override Ths-prep with value in bits 6:0 of this register
6:0	MR_THS_PREP	R R/W	0x0	Ths-prep value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.204 CSI0_THS_ZERO Register

表 7-221. CSI0_THS_ZERO (Indirect Address Page 0x00; Register 0x45)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_ZERO_OV	R/W	0x0	Override CSI Ths-zero parameter 0: Ths-zero is automatically determined 1: Override Ths-zero with value in bits 6:0 of this register
6:0	MR_THS_ZERO	R R/W	0x0	Ths-zero value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.205 CSI0_THS_TRAIL Register

表 7-222. CSI0_THS_TRAIL (Indirect Address Page 0x00; Register 0x46)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_TRAIL_OV	R/W	0x0	Override CSI Ths-trail parameter 0: Ths-trail is automatically determined 1: Override Ths-trail with value in bits 6:0 of this register
6:0	MR_THS_TRAIL	R R/W	0x0	Ths-trail value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.206 CSI0_THS_EXIT Register

表 7-223. CSI0_THS_EXIT (Indirect Address Page 0x00; Register 0x47)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_THS_EXIT_OV	R/W	0x0	Override CSI Ths-exit parameter 0: Ths-exit is automatically determined 1: Override Ths-exit with value in bits 6:0 of this register
6:0	MR_THS_EXIT	R R/W	0x0	Ths-exit value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

7.6.207 CSI0_TPLX Register

表 7-224. CSI0_TPLX (Indirect Address Page 0x00; Register 0x48)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	MR_TPLX_OV	R/W	0x0	Override CSI Tplx parameter 0: Tplx is automatically determined 1: Override Tplx with value in bits 6:0 of this register
6:0	MR_TPLX	R R/W	0x0	Tplx value If bit 7 of this register is 0, this field is read-only, indicating current automatically determined value. If bit 7 of this register is 1, this field is read/write.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 System

The DS90UB936-Q1 is a highly integrated sensor hub chip which includes two FPD-Link III inputs targeted at ADAS applications, such as front-, rear-, and surround-view cameras, camera monitoring systems, and sensor fusion.

8.1.2 Power Over Coax

The DS90UB936-Q1 is designed to support the Power-over-Coax (PoC) method of powering remote sensor systems. With this method, the power is delivered over the same medium (a coaxial cable) used for high-speed digital video data and bidirectional control and diagnostics data transmission. The method uses passive networks or filters that isolate the transmission line from the loading of the DC/DC regulator circuits and their connecting power traces on both sides of the link as shown in 図 8-1.

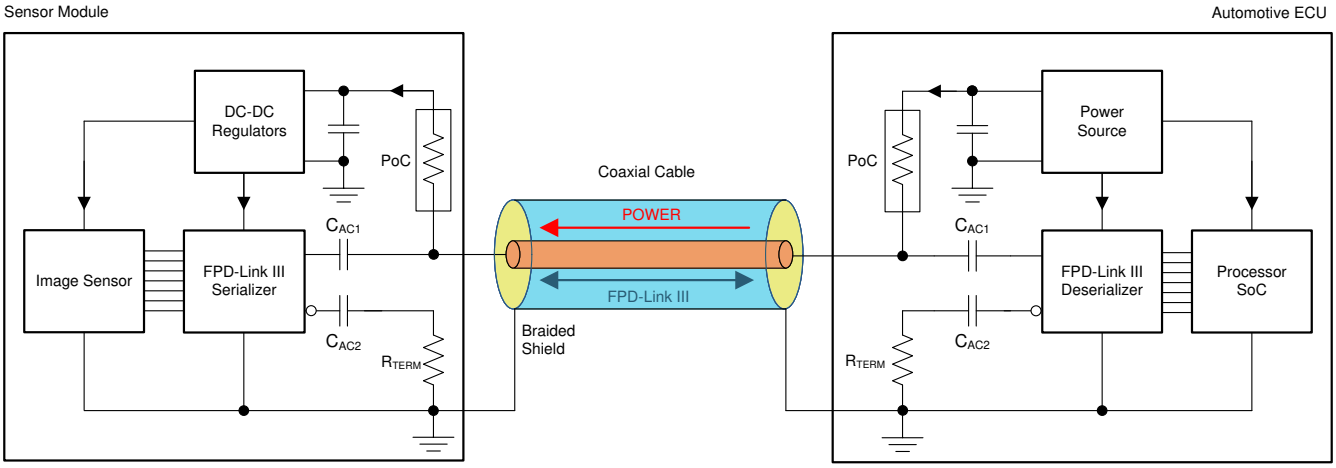


図 8-1. Power Over Coax (PoC) System Diagram

The PoC networks' impedance of ≥ 1 kΩ over a specific frequency band is recommended to isolate the transmission line from the loading of the regulator circuits. Higher PoC network impedance will contribute to favorable insertion loss and return loss characteristics in the high-speed channel. The lower limit of the frequency band is defined as ½ of the frequency of the bidirectional control channel, f_{BCC}. The upper limit of the frequency band is the frequency of the forward high-speed channel, f_{FC}. However, the main criteria that need to be met in the total high-speed channel, which consists of a serializer PCB, a deserializer PCB, and a cable, are the insertion loss and return loss limits defined in the Total Channel Requirements, while the system is under maximum current load and extreme temperature conditions(1) (2).

1. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device.
2. The PoC network and any components along the high-speed trace on the PCB will contribute to the PCB loss budget. TI has recommendations for the loss budget allocation for each individual PCB and cable component in the overall high-speed channel, but the loss limits defined for the total channel in the Channel Specifications must be met.

図 8-2 shows a PoC network recommended for a *4G* FPD-Link III consisting of DS90UB935-Q1 and DS90UB936-Q1 pair with the bidirectional channel operating at 50 Mbps (½ f_{BCC} = 25 MHz) and the forward channel operating at 4.16 Gbps (f_{FC} ≈ 2.1 GHz).

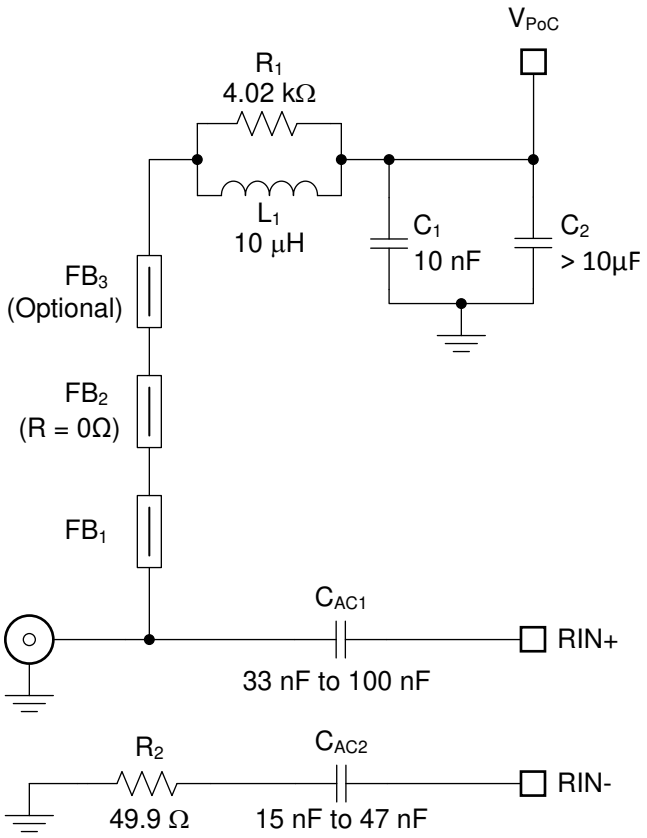


図 8-2. Typical PoC Network for a *4G* FPD-Link III

表 8-1 lists essential components for this particular PoC network.

表 8-1. Suggested Components for a *4G* FPD-Link PoC Network

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	L1	Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30-MHz SRF min, 3 mm × 3 mm, General-Purpose	LQH3NPN100MJR	Murata
		Inductor, 10 µH, 0.288 Ω maximum, 530 mA minimum (Isat, Itemp) 30-MHz SRF min, 3 mm × 3 mm, AEC-Q200	LQH3NPZ100MJR	Murata
		Inductor, 10 µH, 0.360 Ω maximum, 450 mA minimum (Isat, Itemp) 30-MHz SRF min, 3.2 mm x 2.5 mm, AEC-Q200	NLCV32T-100K-EFD	TDK
		Inductor, 10 µH, 0.400 Ω typical, 550 mA minimum (Isat, Itemp) 39-MHz SRF typ, 3 mm × 3 mm, AEC-Q200	TYS3010100M-10	Laird
		Inductor, 10 µH, 0.325 Ω maximum, 725 mA minimum (Isat, Itemp) 41-MHz SRF typ, 3 mm × 3 mm, AEC-Q200	TYS3015100M-10	Laird
3	FB1-FB3	Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , General-Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , AEC-Q200	BLM18HE152SZ1	Murata

図 8-3 shows a PoC network recommended for a *2G* FPD-Link III consisting of a DS90UB933-Q1 or DS90UB913A-Q1 serializer and DS90UB936-Q1 with the bidirectional channel operating at the data rate of 5 Mbps (½ f_{BCC} = 2.5 MHz) and the forward channel operating at the data rate as high as 1.87 Gbps (f_{FC} ≈ 1 GHz).

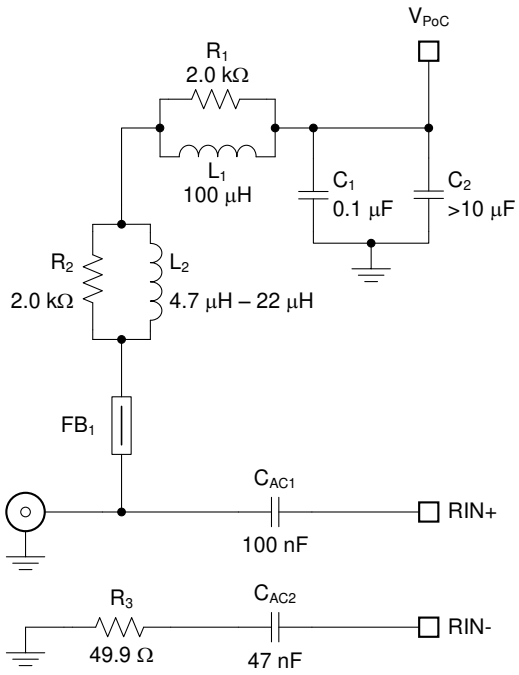


図 8-3. Typical PoC Network for a *2G* FPD-Link III

表 8-2 lists essential components for this particular PoC network.

表 8-2. Suggested Components for a *2G* FPD-Link III PoC Network

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	L1	Inductor, 100 µH, 0.310 Ω maximum, 710 mA minimum (Isat, Itemp) 7.2-MHz SRF typical, 6.6 mm × 6.6 mm, AEC-Q200	MSS7341-104ML	Coilcraft
1	L2	Inductor, 4.7 µH, 0.350 Ω maximum, 700 mA minimum (Isat, Itemp) 160-MHz SRF typical, 3.8 mm x 3.8 mm, AEC-Q200	1008PS-472KL	Coilcraft
		Inductor, 4.7 µH, 0.130 Ω maximum, 830 mA minimum (Isat, Itemp), 70-MHz SRF typical, 3.2 mm × 2.5 mm, AEC-Q200	CBC3225T4R7MRV	Taiyo Yuden
1	FB1	Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , General-Purpose	BLM18HE152SN1	Murata
		Ferrite Bead, 1.5 kΩ at 1 GHz, 0.5 Ω maximum at DC 500 mA at 85°C, 0603 SMD , AEC-Q200	BLM18HE152SZ1	Murata

Application report *Sending Power over Coax in DS90UB913A Designs* (SNLA224) discusses defining PoC networks in more detail.

In addition to the PoC network components selection, their placement and layout play a critical role as well.

- Place the smallest component, typically a ferrite bead or a chip inductor, as close to the connector as possible. Route the high-speed trace through one of its pads to avoid stubs.
- Use the smallest component pads as allowed by manufacturer's design rules. Add anti-pads in the inner planes below the component pads to minimize impedance drop.
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impactof the through-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.
- Use coupled 100-Ω differential signal traces from the device pins to the AC-coupling caps. Use 50-Ω single-ended traces from the AC-coupling capacitors to the connector.
- Terminate the inverting signal traces close to the connectors with standard 49.9-Ω resistors.

The suggested characteristics for single-ended PCB traces (microstrips or striplines) for serializer or deserializer boards are detailed in 表 8-3. The effects of the PoC networks must be accounted for when testing the traces for compliance to the suggested limits.

表 8-3. Suggested Characteristics for Single-Ended PCB Traces With Attached PoC Networks

PARAMETER		MIN	TYP	MAX	UNIT
L_{trace}	Single-ended PCB trace length from the device pin to the connector pin			5	cm
Z_{trace}	Single-ended PCB trace characteristic impedance	45	50	55	Ω
Z_{con}	Connector (mounted) characteristic impedance	40	50	60	Ω
$t_{\Delta Z\_con}$	Allowable electrical length of the connector impedance discontinuity as measured with a TDR (100 ps edge)			20	ps

The V_{POC} noise must be kept to 10 mVp-p or lower on the source / deserializer side of the system. The V_{POC} fluctuations on the serializer side, caused by the transient current draw of the sensor and the DC resistance of cables and PoC components,must be kept at minimum as well. Increasing the V_{POC} voltage and adding extra decoupling capacitance (> 10 µF) help reduce the amplitude and slew rate of the V_{POC} fluctuations.

8.2 Typical Application

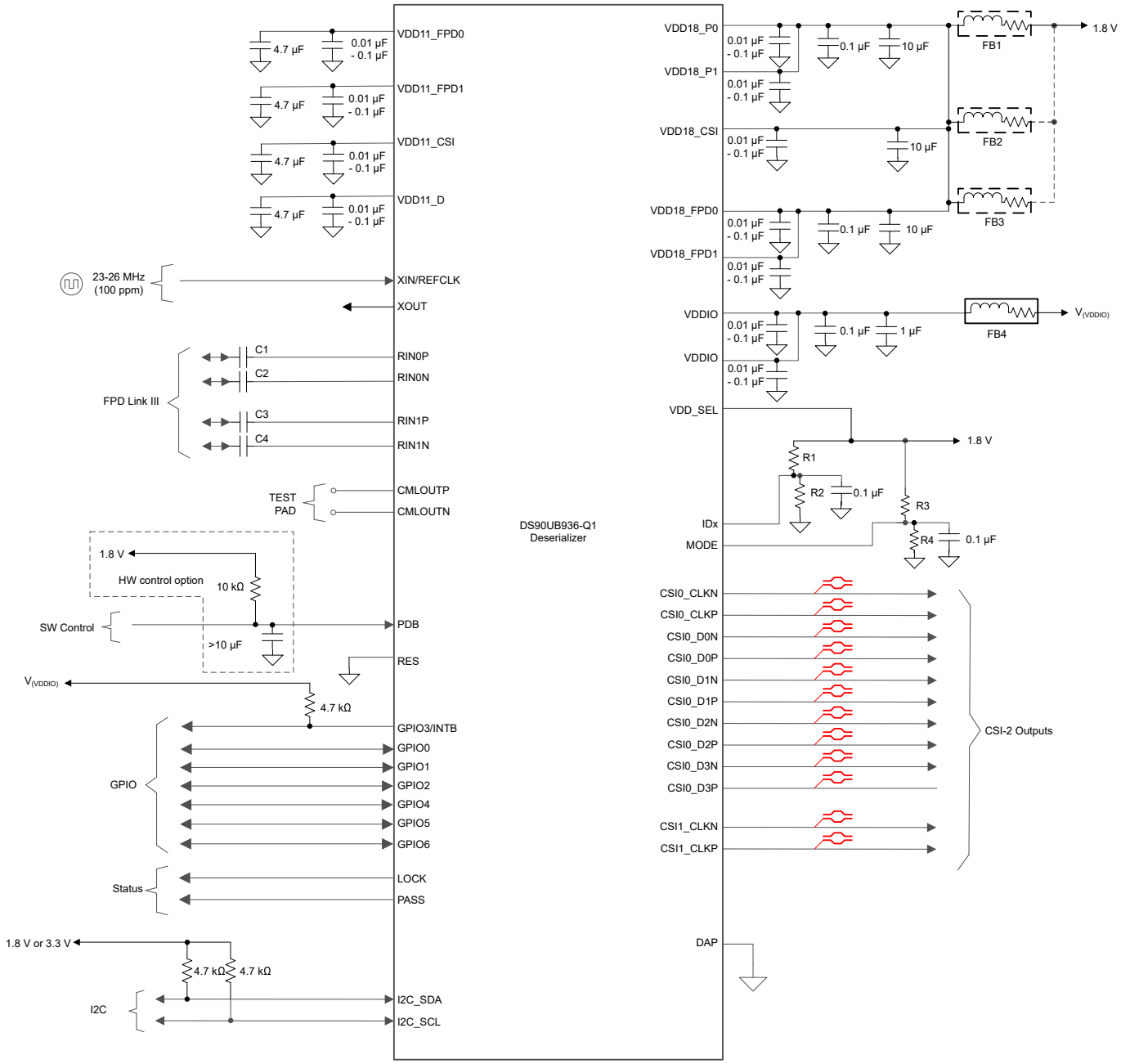


図 8-4. Typical Connection Diagram Coaxial With Internal 1.1-V LDO

注

- The decoupling capacitors for VDD11 are different between the two typical application diagrams because VDD_SEL is pulled to different levels. See the *Pin Functions* table for more information.
- FB2, F3 may be required depending on system power supply noise levels
- FB1-FB4: DCR ≤ 25mΩ; Z = 120Ω@100MHz
- C1, C2, C3, C4 (see *Design Parameters Values Table*)
- R1, R2 (see *IDX Resistor Values Table*)
- R3, R4 (see *MODE Resistor Values Table*)
- RTERM = 50Ω

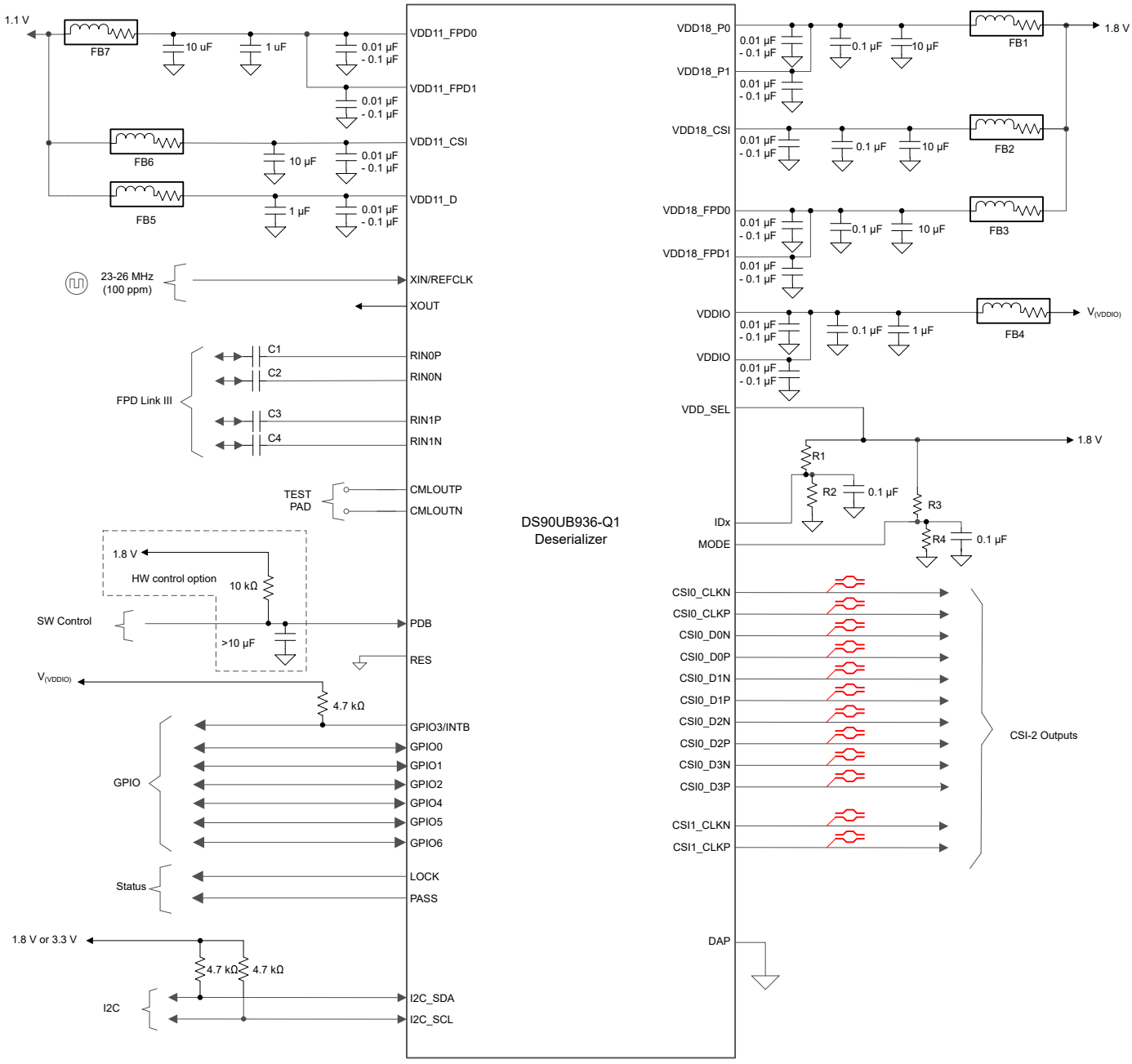


図 8-5. Typical Connection Diagram STP With External 1.1-V supply

注

- The decoupling capacitors for VDD11 are different between the two typical application diagrams because VDD_SEL is pulled to different levels. See the *Pin Functions* table for more information.
- FB1-FB7: DCR ≤ 25mΩ; Z = 120Ω@100MHz
- C1, C2, C3, C4 (see *Design Parameters Values Table*)
- R1, R2 (see *IDX Resistor Values Table*)
- R3, R4 (see *MODE Resistor Values Table*)
- RTERM = 50Ω

8.2.1 Design Requirements

For the typical design application, use the parameters listed in 表 8-4.

表 8-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{(VDDIO)}$	1.8 V or 3.3 V
$V_{(VDD18)}$	1.8 V
$V_{(VDD11)}$(When VDD_SEL = HIGH)	1.1 V
AC-coupling Capacitor for Synchronous Modes, Coaxial Connection: RIN0+ ,RIN1+	33 nF - 100nF (50 WV 0402)
AC-coupling Capacitor for Synchronous Modes, Coaxial Connection: RIN0- ,RIN1-	15 nF - 47nF (50 WV 0402)
AC-coupling Capacitor for Synchronous Modes, STP Connection: RIN0± ,RIN1±	33 nF - 100nF (50 WV 0402)
AC-coupling Capacitor for Non-Synchronous and DVP Backwards Compatible Modes, Coaxial Connection: RIN0+, RIN1+	100 nF (50 WV 0402)
AC-coupling Capacitor for Non-Synchronous and DVP Backwards Compatible Modes, Coaxial Connection: RIN0-, RIN1-	47 nF (50 WV 0402)
AC-coupling Capacitor for Non-Synchronous and DVP Backwards Compatible Modes, STP Connection: RIN0±, RIN1±	100 nF (50 WV 0402)

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in 図 8-6 and 図 8-7. When connected to the DS90UB935-Q1 or DS90UB953-Q1 serializer operating with 10-Mbps back channel, the higher value AC-coupling capacitors are recommended to reduce low frequency attenuation. For applications using single-ended 50-Ω coaxial cable, terminate the unused data pins (RIN0–, RIN1–) with an AC-coupling capacitor and a 50-Ω resistor.

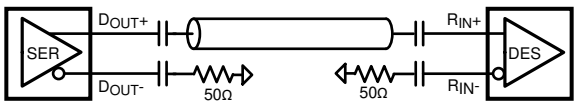


図 8-6. AC-Coupled Connection (Coaxial)

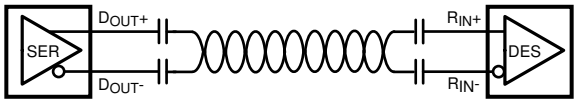


図 8-7. AC-Coupled Connection (STP)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor to help minimize degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

図 8-4 and 図 8-5 show typical applications of the DS90UB936-Q1 for multi-camera surround view system. From 図 8-4, the FPD-Link III is AC coupled an external 100-nF or 47-nF capacitors for coaxial interconnects. For 2G operation or back channel frequency of ≤ 10 Mbps, the higher value AC-coupling capacitors 100 nF /47 nF are recommended. The same AC-coupling capacitor values should be matched on the paired serializer boards. The deserializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, 0.1-µF or 0.01-µF capacitors should be used for each of the core supply pins for local device bypassing. Additional bulk decoupling capacitors and ferrite beads are placed on the VDD18 supplies for effective noise suppression.

8.2.3 Application Curves

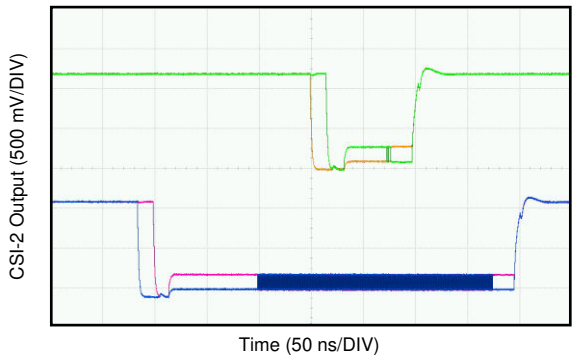


図 8-8. CSI-2 DATA and CLK Output

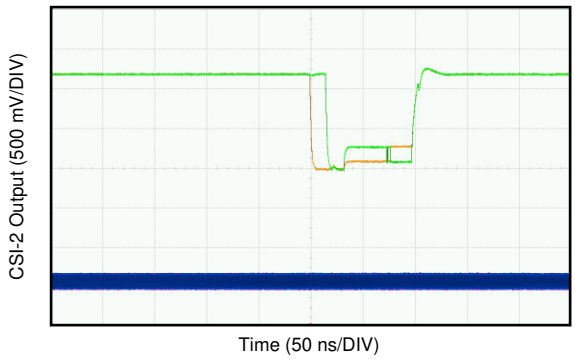


図 8-9. CSI-2 DATA and Continuous CLK Output

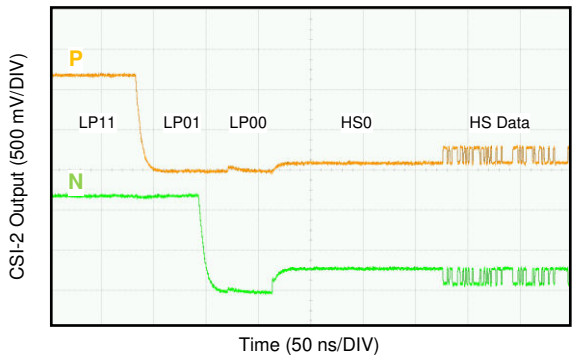


図 8-10. CSI-2 Start of Transmission (SoT)

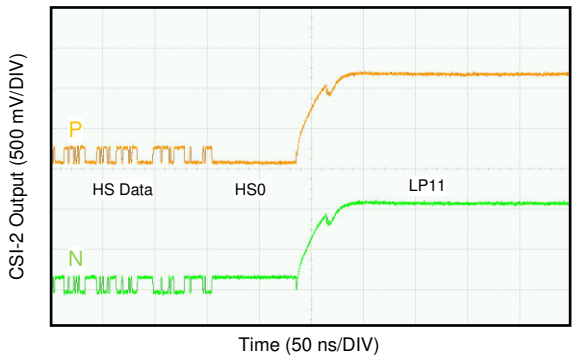


図 8-11. CSI-2 End of Transmission (EoT)

8.3 System Examples

The DS90UB936-Q1 has two input ports that are capable of operating independently. Two sensors can be connected simultaneously (図 8-12), or a single sensor can be connected to either Rx input port 0 or Rx input port 1 (図 8-13). The DS90UB936-Q1 deserializer is capable of receiving serialized sensor data from one or two independent video datastreams and aggregating into a single CSI-Tx output. Alternatively, Rx Data can be replicated onto two 2-Lane CSI-2 outputs for interconnect to two seperate CSI-2 Rx inputs for parallel downstream processing.

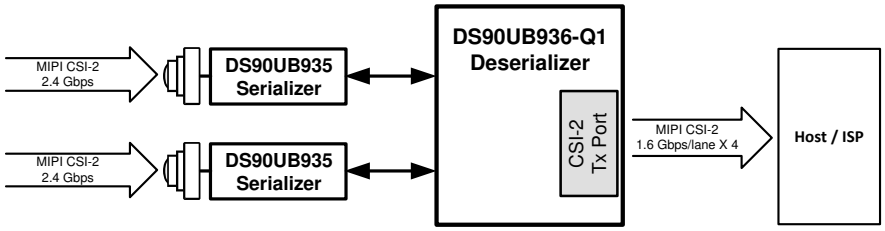


図 8-12. Two DS90UB935-Q1 Sensor Data onto CSI-2 Over 1 Port

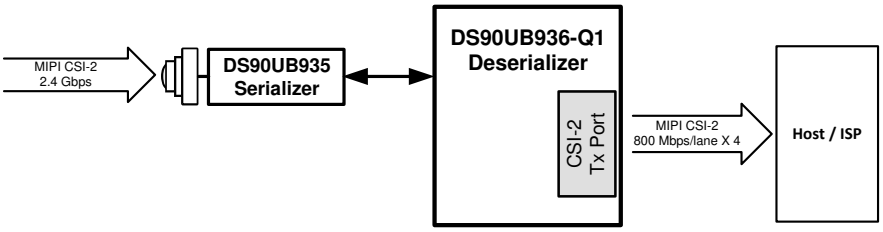


図 8-13. One DS90UB935-Q1 Sensor Data onto CSI-2 Over 1 Port

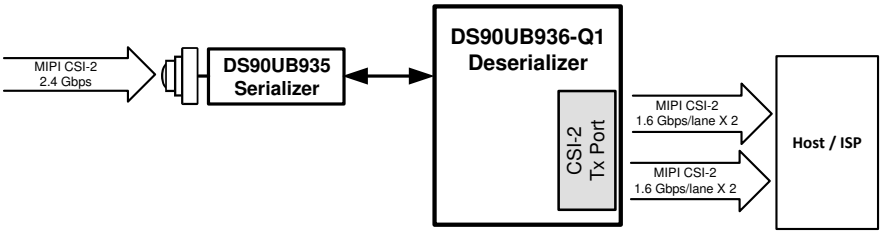


図 8-14. DS90UB935-Q1 Sensor Data Replicated onto 2x 2-Lane CSI-2

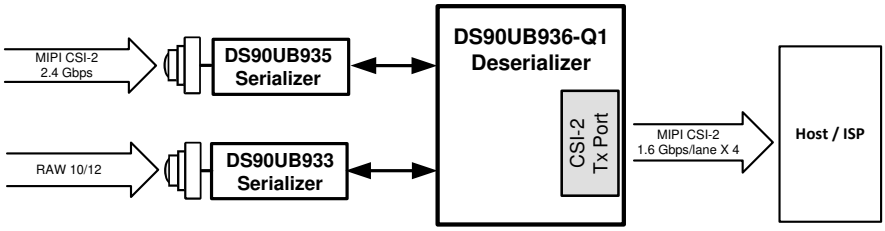


図 8-15. One DS90UB935-Q1 and One DS90UB933-Q1 Sensor Data Combined to One CSI-2 Output

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 VDD and VDDIO Power Supply

Each VDD power supply pin must have a 10-nF (or 100-nF) capacitor to ground connected as close as possible to DS90UB936-Q1 device. When operating VDDIO at 1.8-V nominal supply, the voltage at VDDIO must be within ±100 mV of VDD18 to ensure VIH, VIL specifications. TI recommends having additional decoupling capacitors (1 µF or 10 µF) connected to a common GND plane. Note that although average current for VDDIO is less than 10 mA maximum, the peak current into VDDIO may exceed 100 mA on device start-up.

9.2 Power-Up Sequencing

The power-up sequence for the DS90UB936-Q1 is as follows:

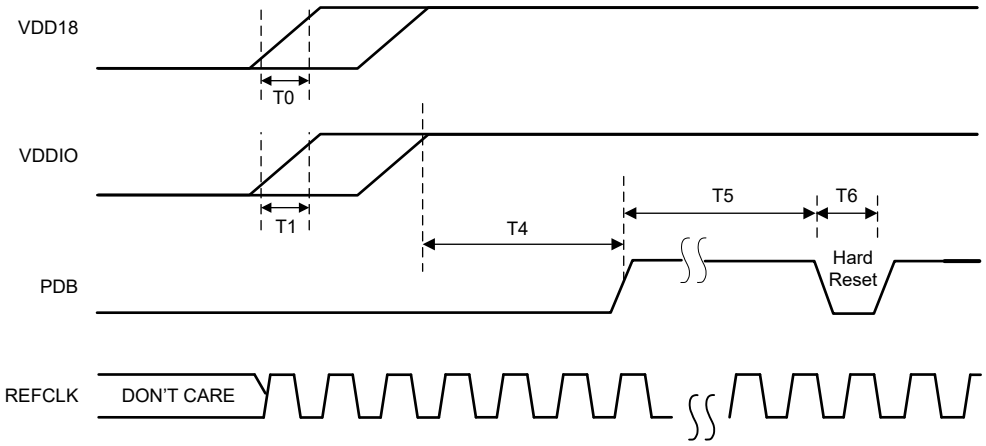


図 9-1. Power Supply Sequencing VDD_SEL = LOW, Internal VDD 1.1-V Supply

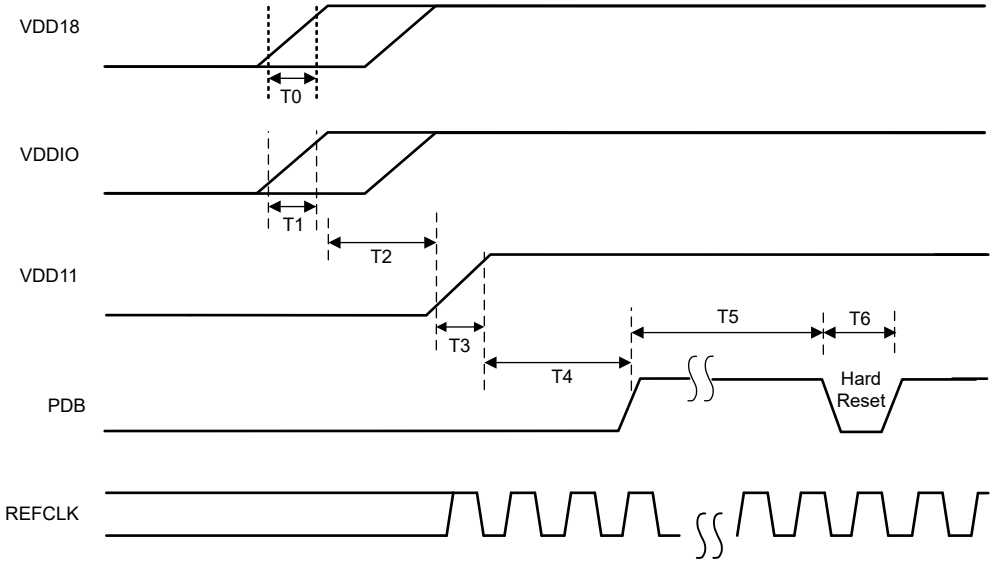


図 9-2. Power Supply Sequencing VDD_SEL = HIGH, External VDD 1.1-V Supply

表 9-1. Timing Diagram for the Power Supply Start-Up Sequence

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
T0	VDD18 rise time	0.05			ms	at 10/90%
T1	VDDIO rise time	0.2	1		ms	at 10/90%
T2	VDD18 High to VDD11 applied	0			ms	N/A when VDD_SEL = LOW
T3	VDD11 rise time	0.2	1		ms	at 10/90%
T4	VDD to PDB	0			ms	After all VDD are stable
T5	PDB high time before PDB hard reset	1			ms	
T6	PDB high to low pulse width	2			ms	Hard reset (optional)
T7	PDB to I2C ready (IDX and MODE valid) delay	2			ms	

Note: VDDIO can come up either before or after VDD18.

9.2.1 PDB Pin

The PDB pin is active HIGH and has internal 50 kΩ pull down resistor. PDB input must remain LOW while the VDD pin power supplies are in transition. Typically PDB will be connected to GPIO from processor also with internal pulldown. Alternatively, when VDD_SEL = LOW, an external RC network on the PDB pin may be connected to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD18, a 10-kΩ pullup and a > 10-µF capacitor to GND are recommended to delay the PDB input signal rise. All inputs must not be driven until both power supplies have reached steady state. When VDD_SEL = HIGH it is not recommended to connect PDB through RC circuit as this may conflict with the sequencing of the external 1.1-V supply rail.

表 9-2. PDB Pin Pulse Width

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PDB						
tLRST	PDB Reset Low Pulse		2	3		ms

9.2.2 System Initialization

When initializing the communications link between the DS90UB936-Q1 deserializer hub and a DS90UB935-Q1 serializer, the system timing will depend on the mode selected for generating the serializer reference clock. When synchronous clocking mode is selected, the serializer will re-lock onto the extracted back channel reference clock once available so there is no need for local crystal oscillator at the sensor module (図 9-3). When the DS90UB935-Q1 is operating in non-synchronous mode, or if connecting to DS90UB933-Q1 or DS90UB913A-Q1 serializer the sensor module requires a local reference clock and timing would follow 図 9-4.

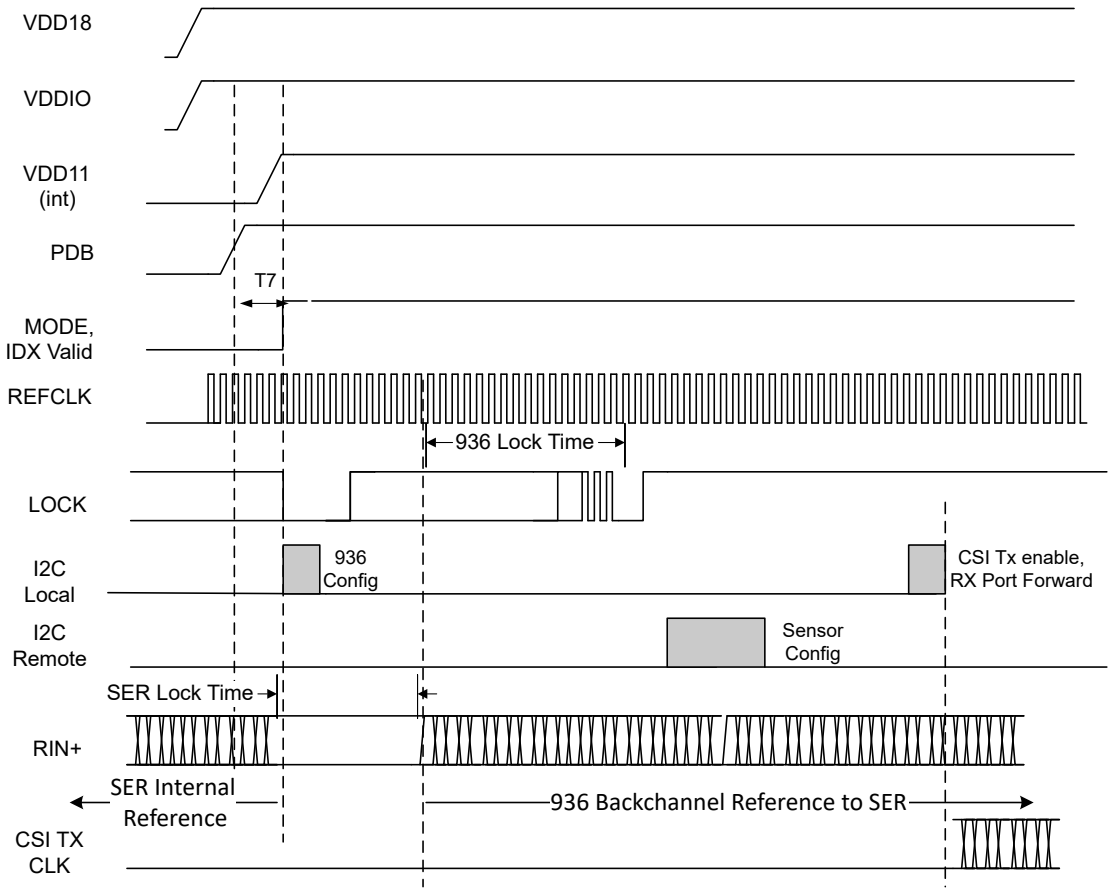


図 9-3. Power-Up Sequencing Synchronous Back Channel Clocking Mode, VDD_SEL = LOW

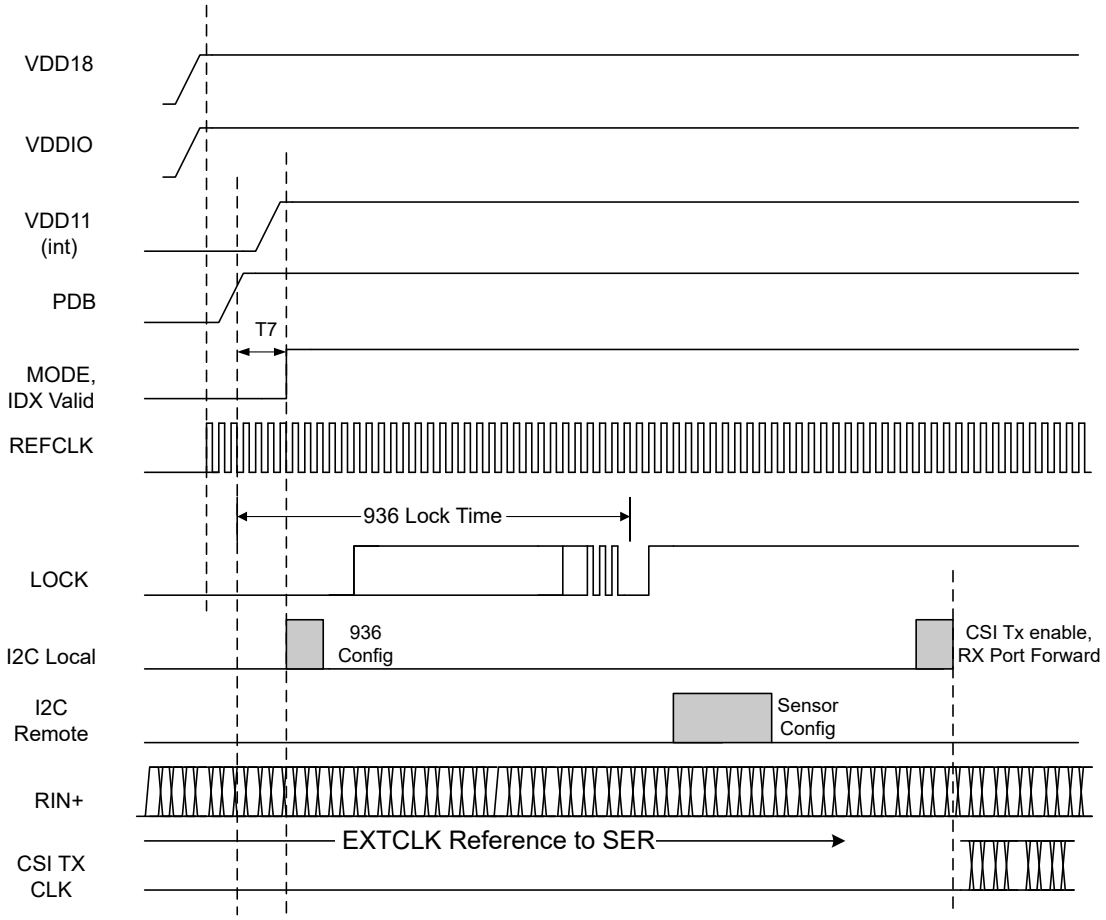


図 9-4. Power-Up Sequencing Non-synchronous Back Channel Clocking Mode, VDD_SEL = LOW

10 Layout

10.1 PCB Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high-frequency or high-level inputs and outputs to minimize unwanted noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power or ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypassing should be low-ESR ceramic capacitors with high-quality dielectric. The voltage rating of the ceramic capacitors must be at least 2× the power supply voltage being used.

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 47-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs

Use at least a four-layer board with a power and ground plane. Locate CSI-2 signals away from the single-ended or differential FPD RX input traces to prevent coupling from the CSI-2 signals to the RX inputs. The following sections provide important details for routing the FPD-Link III traces, PoC filter, and CSI-2 traces.

10.1.1 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the DS90UB936-Q1 to the GND plane with vias.

10.1.2 Routing FPD-Link III Signal Traces and PoC Filter

Routing the FPD-Link III signal traces between the R_{IN} pins and the connector as well as connecting the PoC filter to these traces are the most critical pieces of a successful DS90UB936-Q1 PCB layout. 図 10-1 shows an example PCB layout of the DS90UB936-Q1 configured for interface to remote sensor modules over coaxial cables. The layout example also uses a footprint of an edge-mount FAKRA connector provided by Rosenberger (P/N: 59S20X-40ML5-Z).

The following list provides essential recommendations for routing the FPD-Link III signal traces between the DS90UB936-Q1 receiver input pins (R_{IN}) and the FAKRA connector, and connecting the PoC filter.

- The routing of the FPD-Link III traces may be all on the top layer (as shown in the example) or partially embedded in middle layers if EMI is a concern
- The AC-coupling capacitors should be on the top layer and very close to the DS90UB936-Q1 receiver input pins to minimize the length of coupled differential trace pair between the pins and the capacitors.
- Route the RIN+ trace between the AC-coupling capacitor and the FAKRA connector as a 50-Ω single-ended micro-strip with tight impedance control (±10%). Calculate the proper width of the trace for a 50-Ω impedance based on the PCB stack-up. Ensure that the trace can carry the PoC current for the maximum load presented by the remote sensor module.

- The PoC filter should be connected to the RIN+ trace through the first ferrite bead (FB_1). The FB_1 should be touching the high-speed trace to minimize the stub length seen by the transmission line. Create an anti-pad or a moat under the FB_1 pad that touches the trace. The anti-pad should be a plane cutout of the ground plane directly underneath the top layer without cutting out the ground reference under the trace. The purpose of the anti-pad is to maintain the impedance as close to 50 Ω as possible.
- Route the RIN– trace loosely coupled to the RIN+ trace for the length similar to the RIN+ trace length when possible. This will help the differential nature of the receiver to cancel out any common-mode noise that may be present in the environment that may couple on to the RIN+ and RIN– signal traces. When routing on inner layers, length matching for single-ended traces does not provide as significant benefit.

When configured for STP and routing differential signals to the DS90UB936-Q1 receiver inputs, the traces should maintain 100-Ω differential impedance routed to the connector. When choosing to implement a common mode choke for common mode noise reduction, take care to minimize the effect of any mismatch. 図 10-2 shows an example PCB layout for STP configuration.

10.1.3 Routing CSI-2 Signal Traces

Routing the CSI-2 signal traces between the CSI-2 pins and the CSI-2 connector is also important for a successful DS90UB936-Q1 PCB layout. 図 10-1 shows essential details for routing the CSI-2 traces. Additional recommendations are given in the following list:

1. Route CSI_D0N, CSI_D0P, CSI_D1N, and CSI_D1P pairs as differential coupled striplines with controlled 100-Ω differential impedance (±10%)
2. Keep the trace length difference between CSI-2 traces to 5 mils of each other.
3. Length matching should be near the location of mismatch.
4. Each pair should be separated at least by 5 times the signal trace width.
5. Keep away from other high-speed signals.
6. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
7. Route all differential pairs on one or two inner layers.
8. Keep the number of signal vias to a minimum — TI recommends keeping the via count to the maximum of two per CSI-2 trace.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Examples

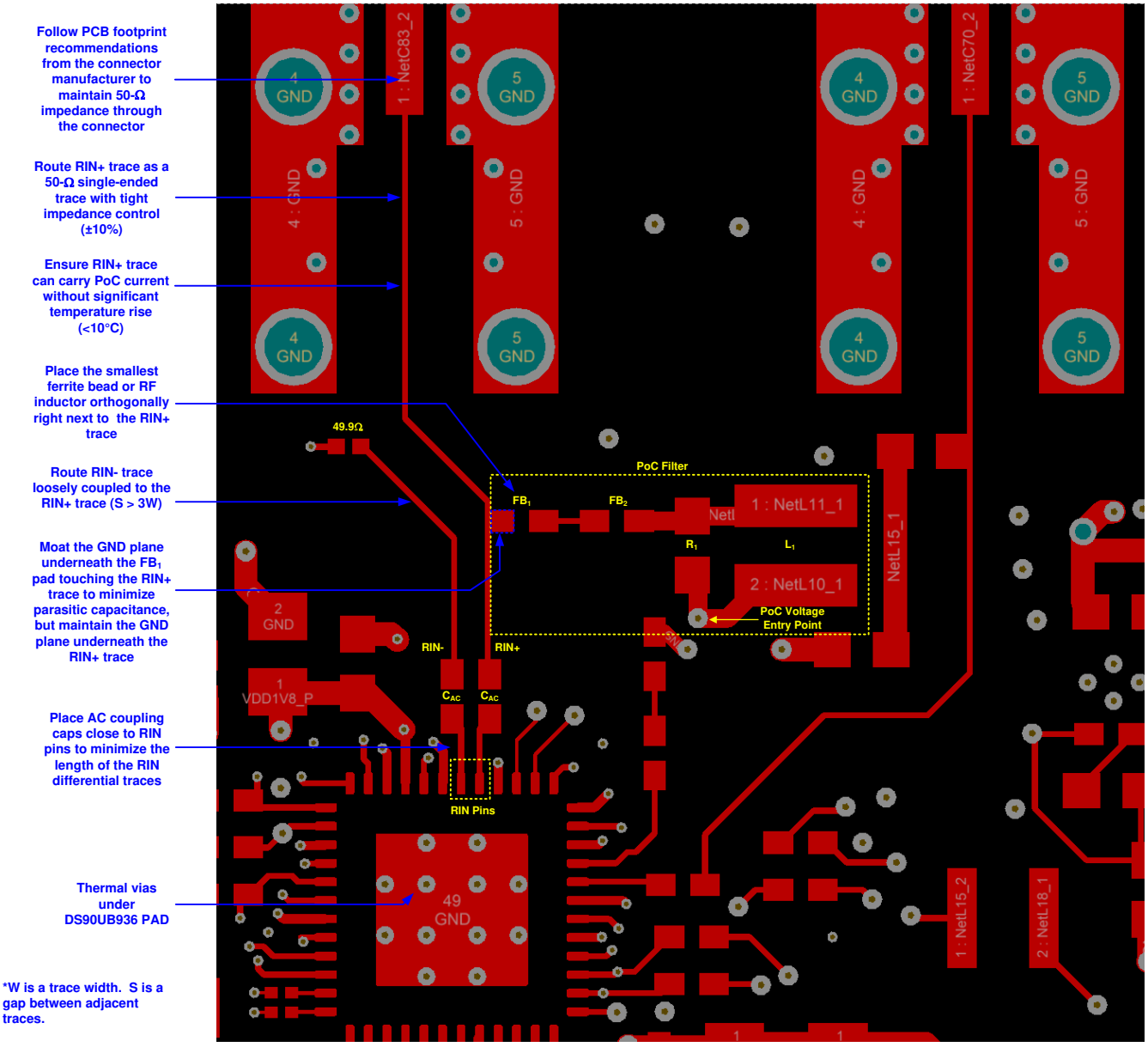


図 10-1. DS90UB936-Q1 PCB Layout Example: FPD-Link III Signal Traces and PoC Filter

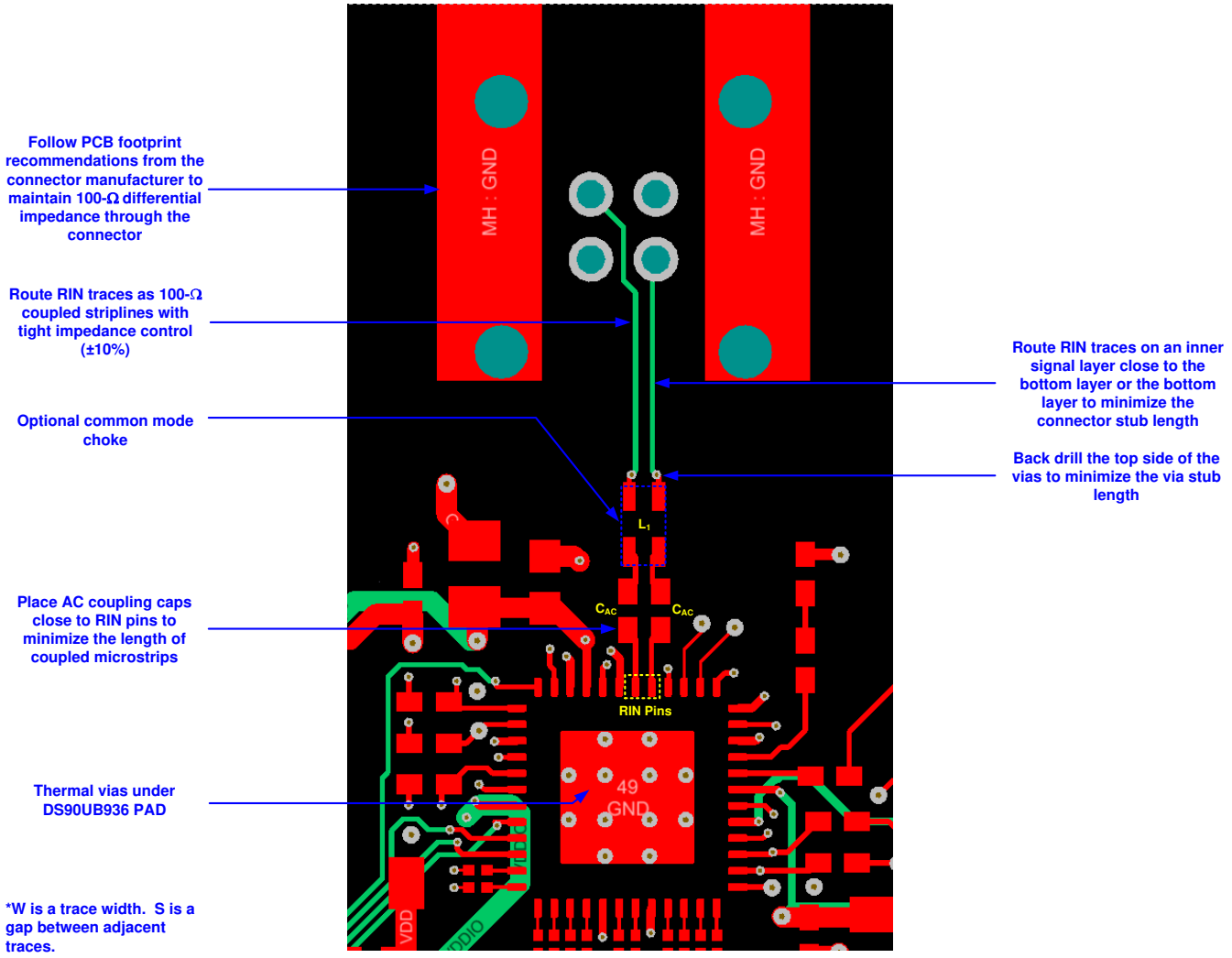


図 10-2. DS90UB936-Q1 PCB Layout Example: FPD-Link III Differential Signal Traces

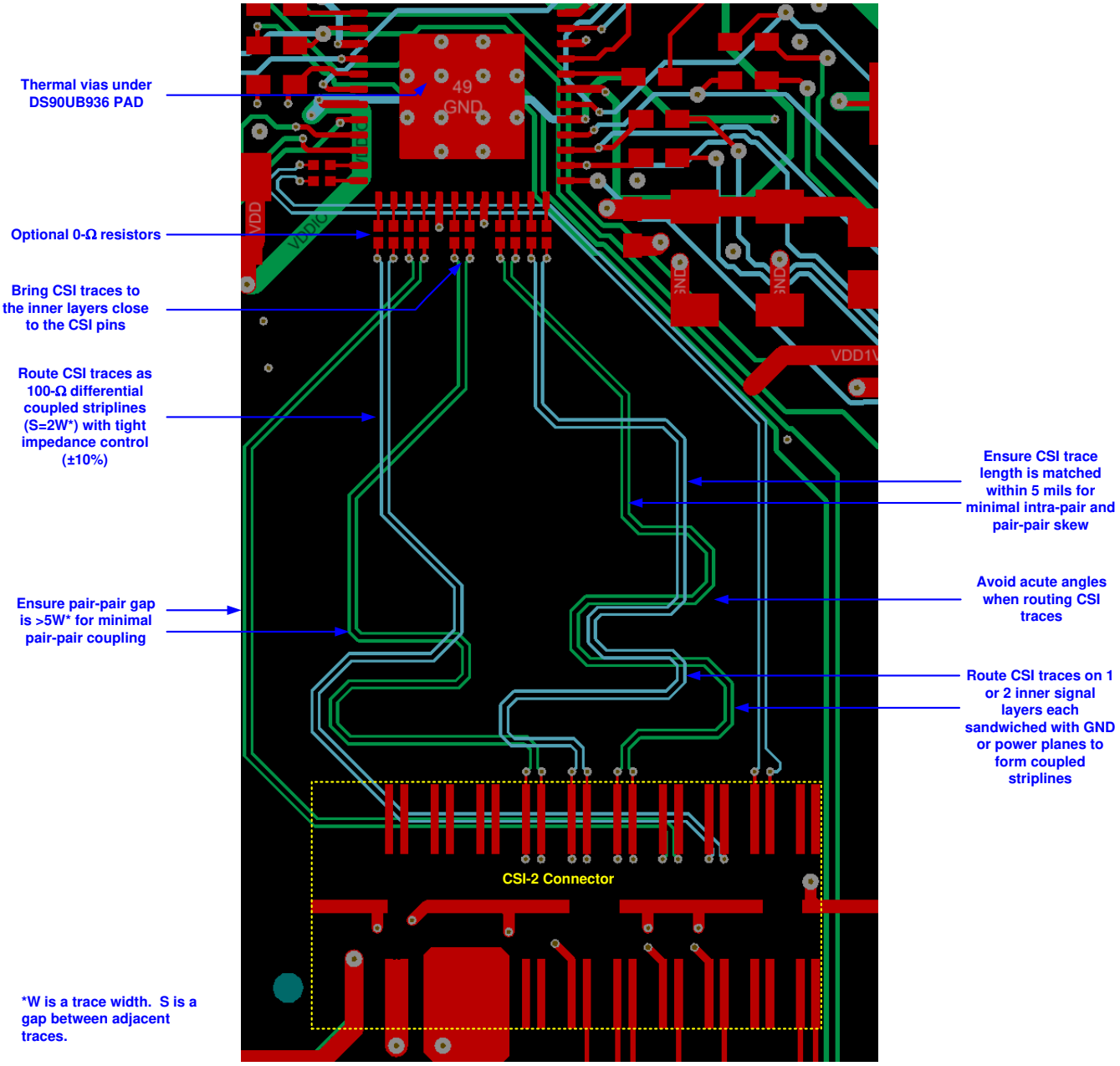


図 10-3. DS90UB936-Q1 PCB Layout Example: CSI-2 Traces

11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

-
- *I2C Communication Over FPD-Link III With Bidirectional Control Channel* (SNLA131)
- *I2C Bus Pullup Resistor Calculation* (SLVA689)
- *I2C Over DS90UB913/4 FPD-Link III With Bidirectional Control Channel* (SNLA222)
- *Sending Power Over Coax in DS90UB913A Designs* (SNLA224)
- FPD-Link Learning Center
- *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719)
- *Ten Tips for Successfully Designing With Automotive EMC/EMI Requirements* (SLYT636)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

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11.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

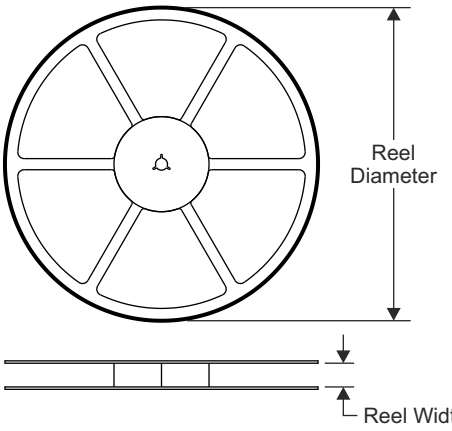
Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(4)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(5) (6)
DS90UB936TRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB936Q
DS90UB936TRGZTQ1	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB936Q

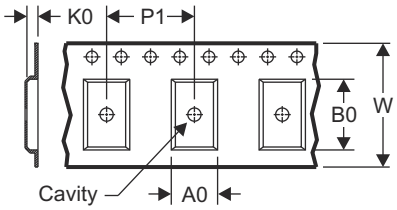
1. The marketing status values are defined as follows:
   ACTIVE: Product device recommended for new designs.
   LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
   PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
   OBSOLETE: TI has discontinued the production of the device.
2. **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
   RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
3. MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
5. Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
6. Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

12.1.1 Tape and Reel Information

REEL DIMENSIONS

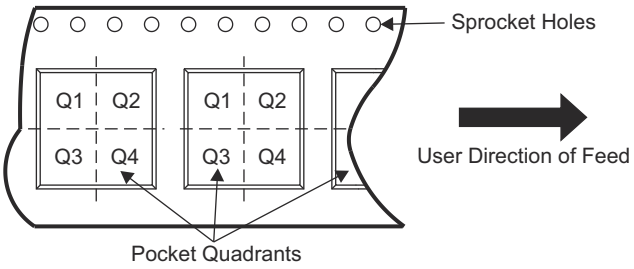


TAPE DIMENSIONS



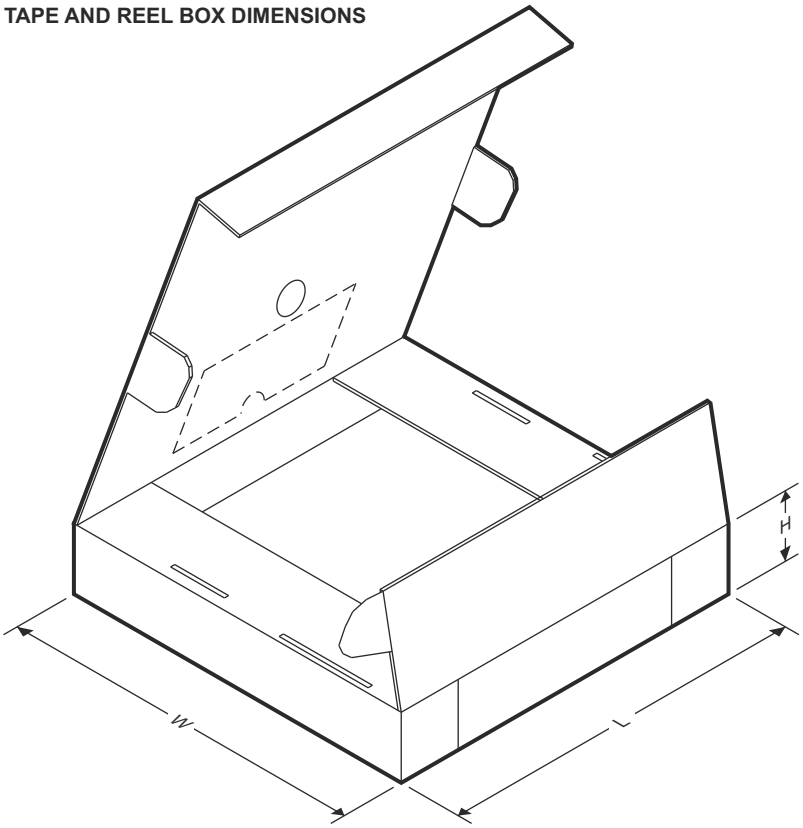
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



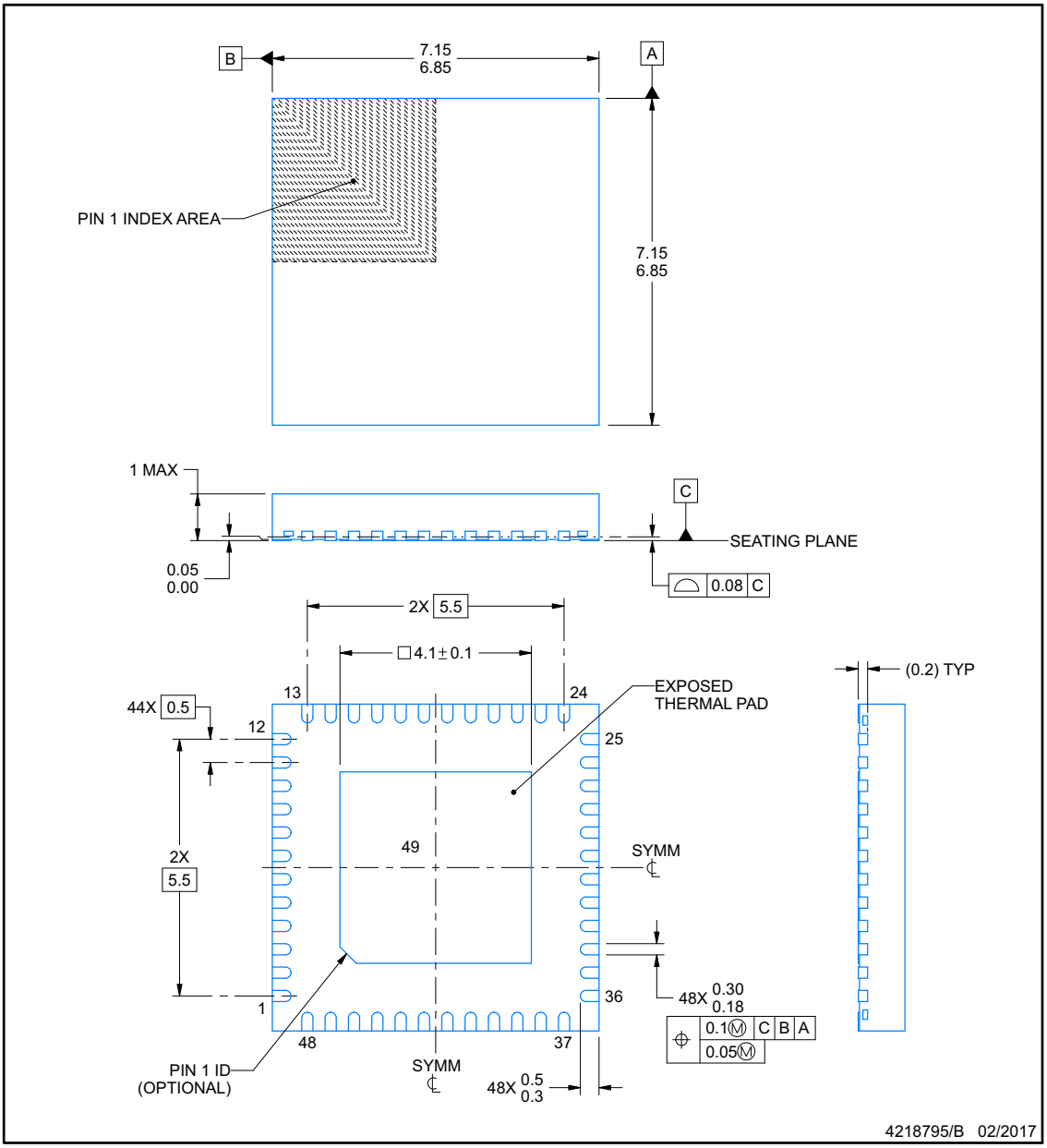
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB936TRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

PACKAGE OUTLINE

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



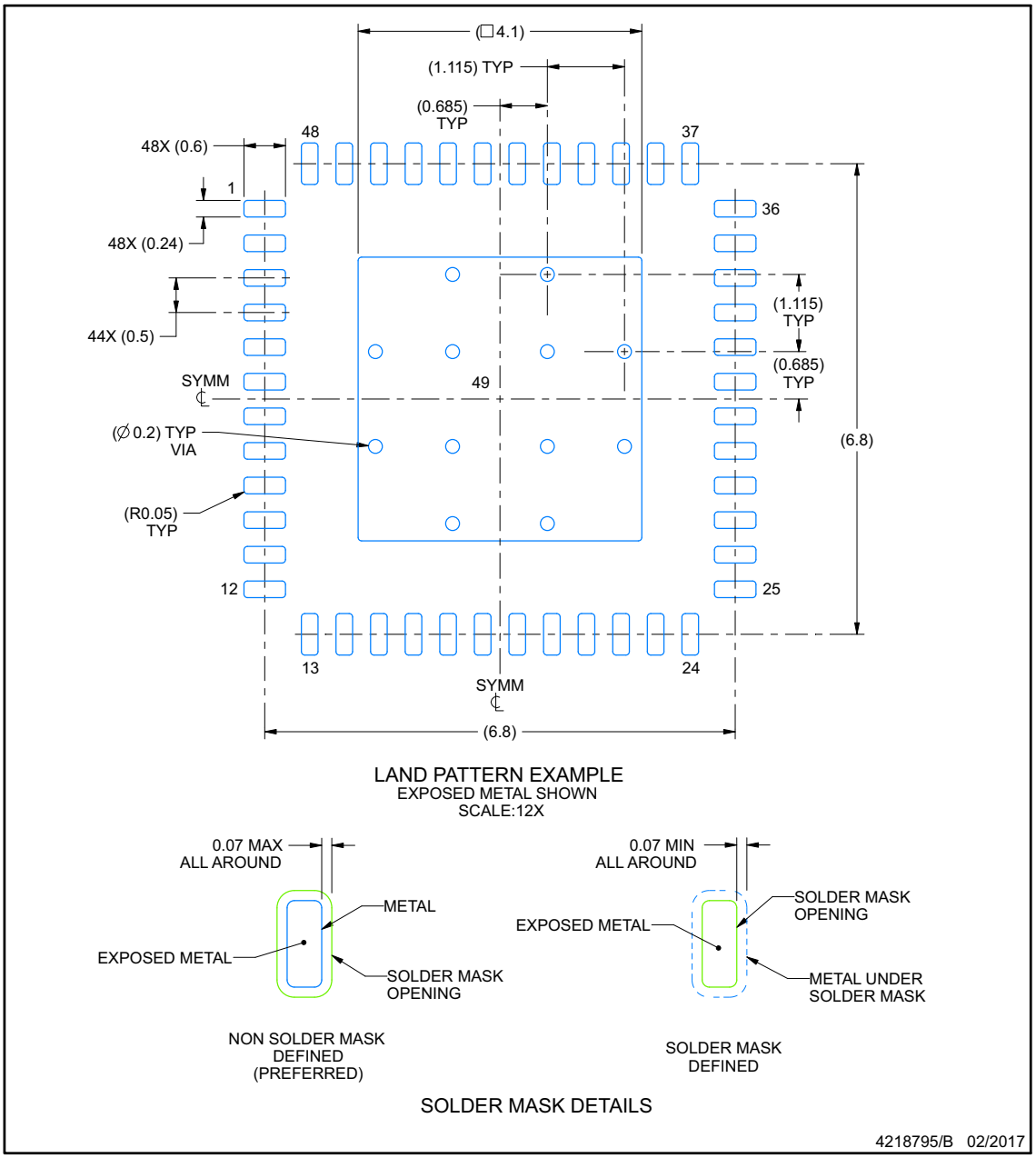
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



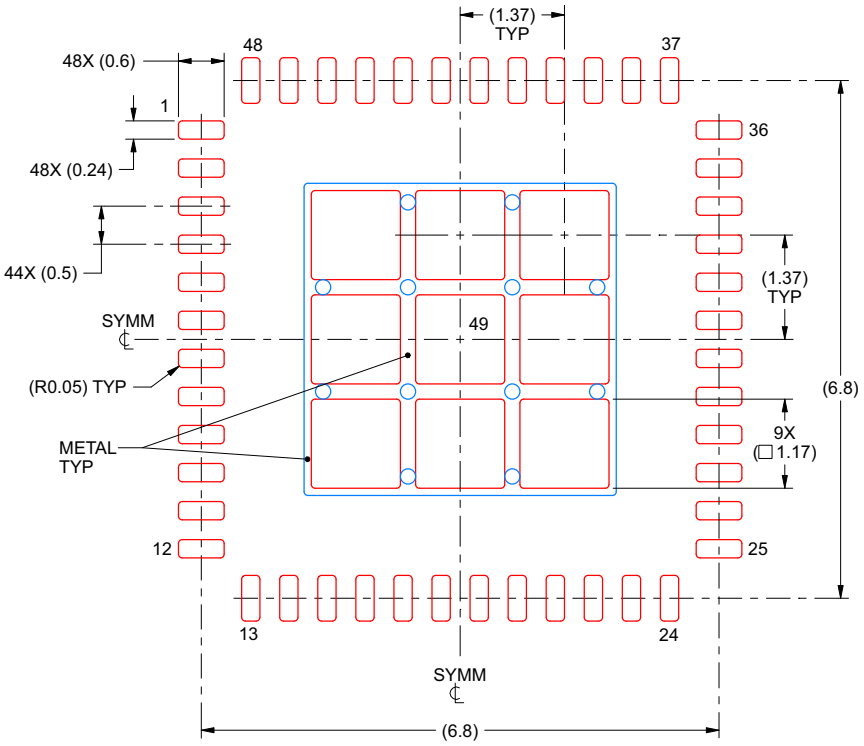
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB936TRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB936Q	Samples
DS90UB936TRGZTQ1	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB936Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

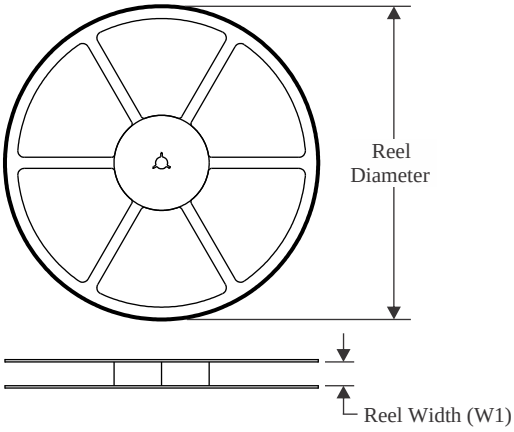
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

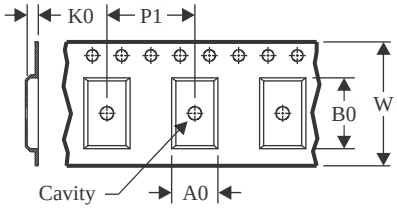
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

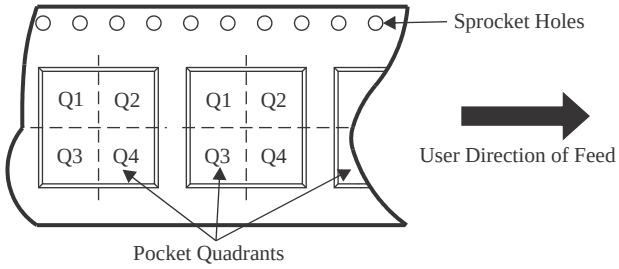


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

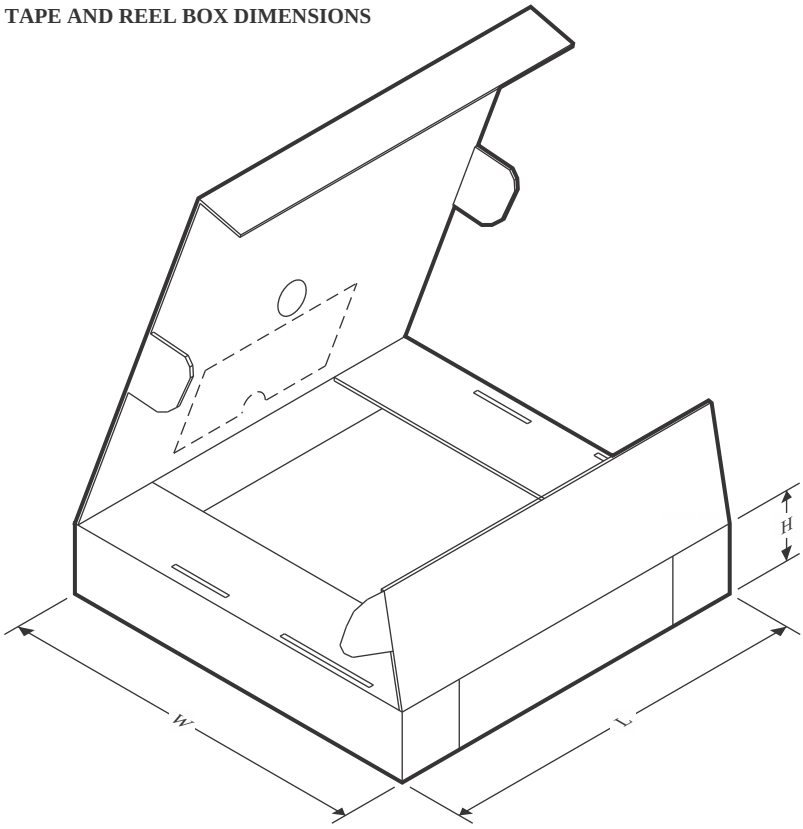
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB936TRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DS90UB936TRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB936TRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	35.0
DS90UB936TRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0
DS90UB936TRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

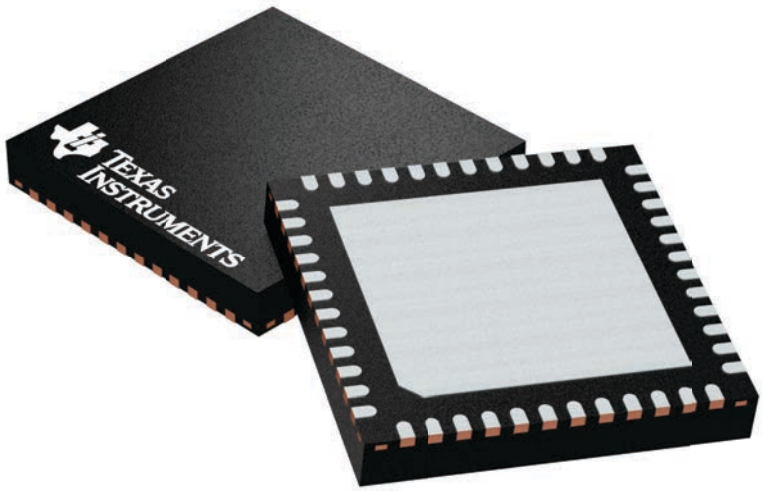
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

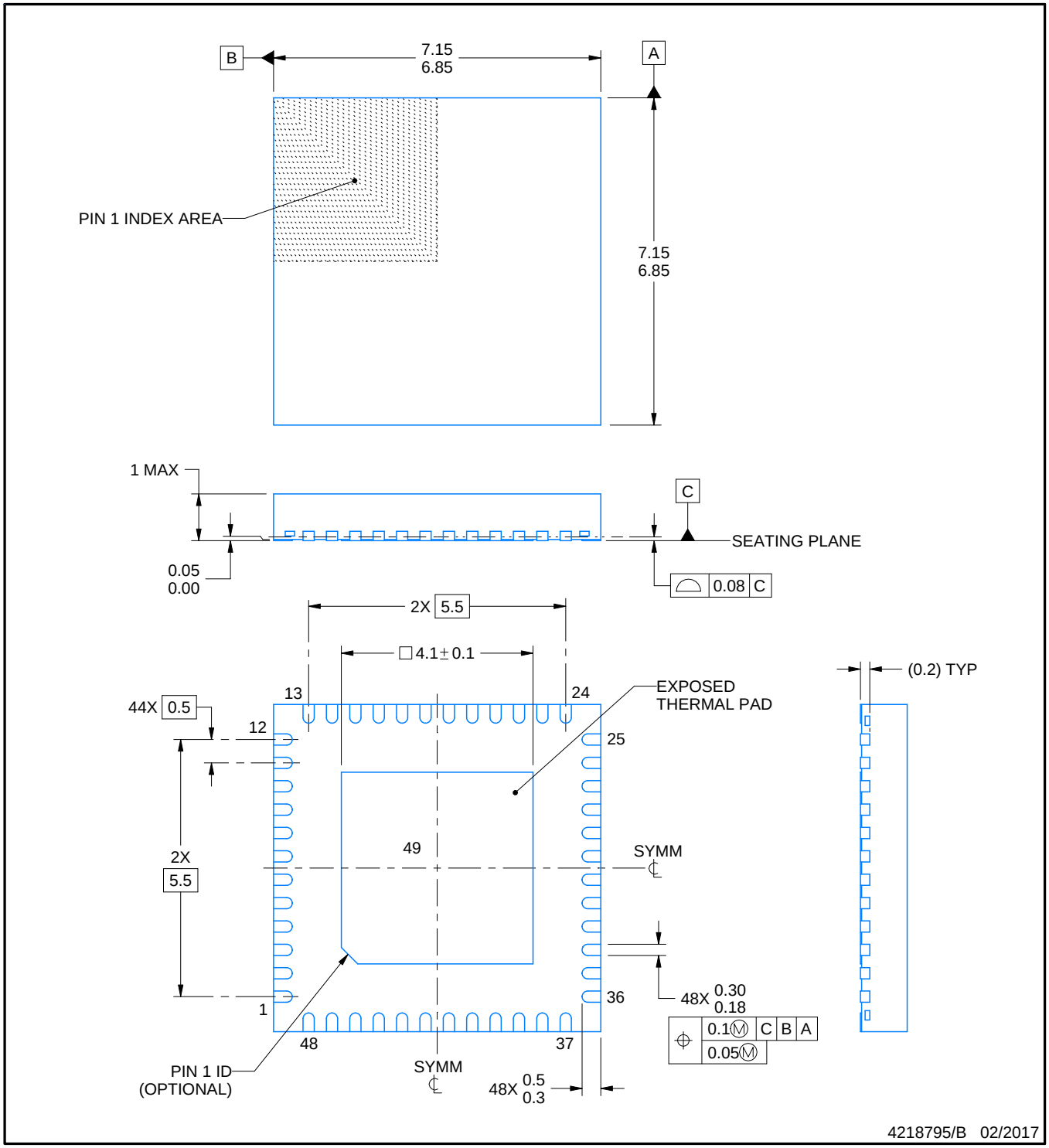
4224671/A

RGZ0048B

PACKAGE OUTLINE

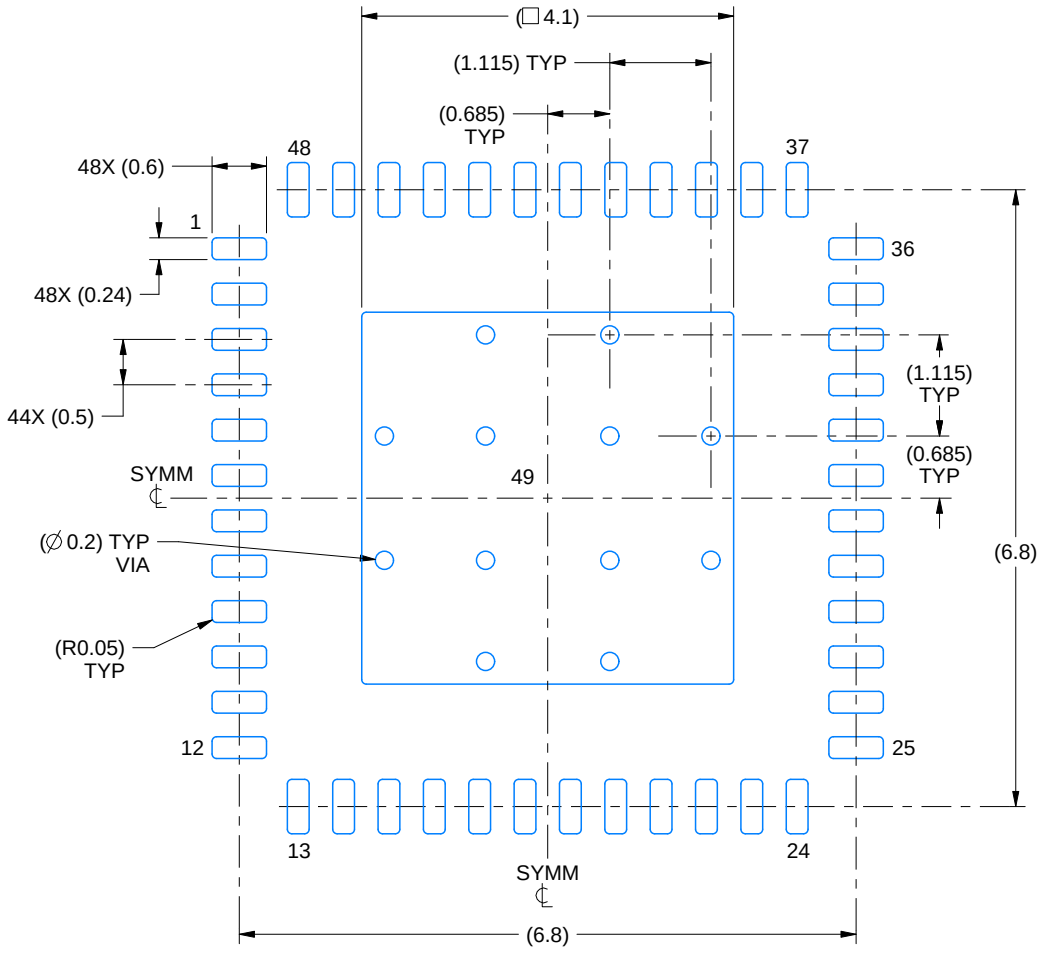
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

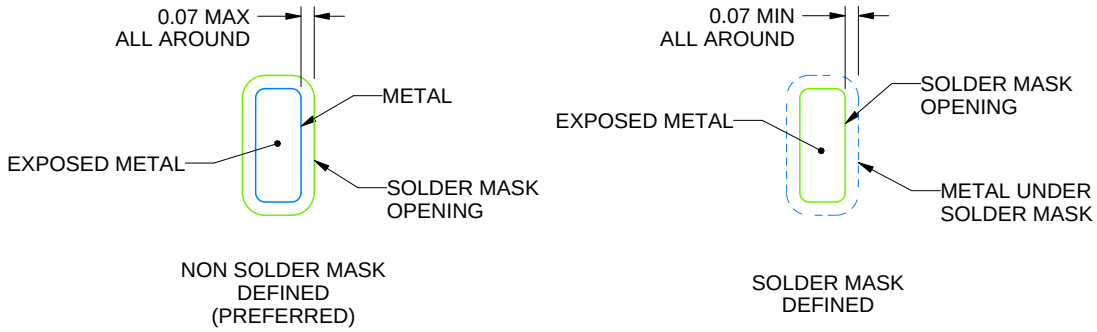


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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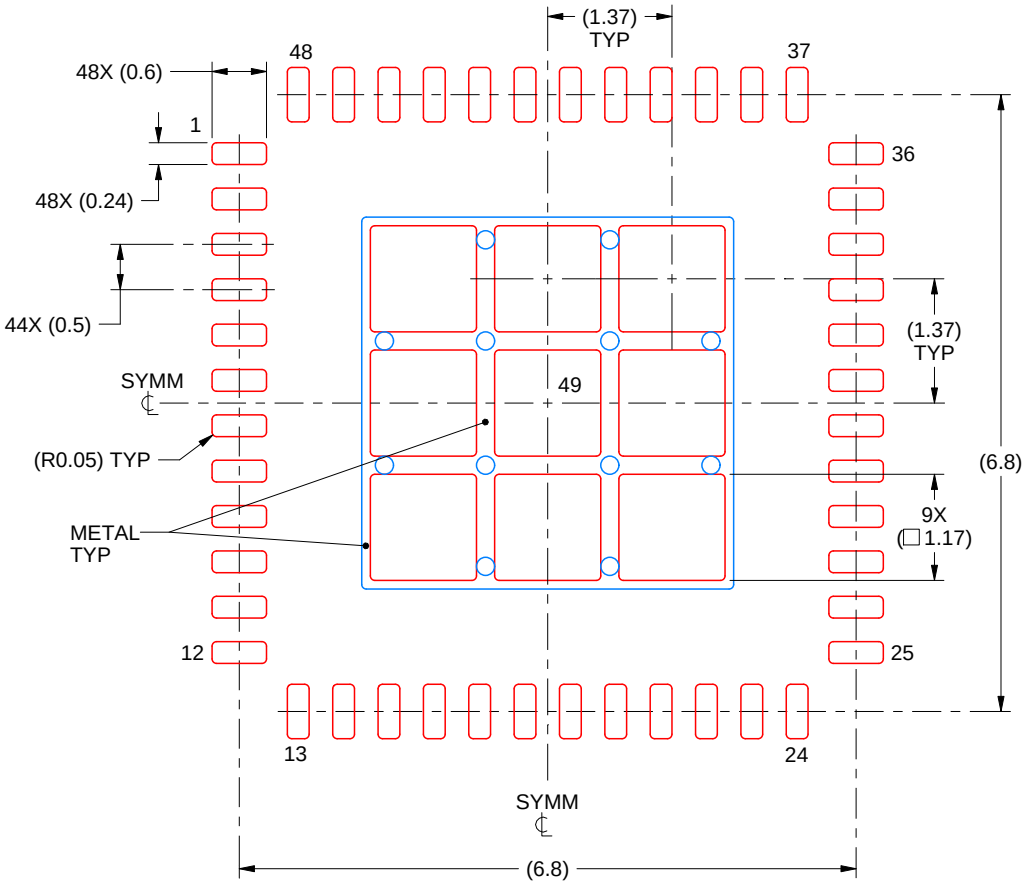
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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