TEXAS INSTRUMENTS
ESD751, ESD761
JAJSPA4C – NOVEMBER 2022 – REVISED DECEMBER 2022

ESD751 および ESD761 24V、1 チャネル ESD 保護ダイオード

1 特長

- IEC 61000-4-2 レベル 4 ESD 保護
  - ±22kV または ±15kV の接触放電
  - ±22kV または ±15kV のエアギャップ放電
- 強力なサージ保護:
  - IEC 61000-4-5 (8/20µs):2.8A または 1.8A
- 24V の動作電圧
- 双方向 ESD 保護
- 下流の部品を保護する低いクランピング電圧
- 温度範囲:-55℃～+150℃
- I/O 容量 = 1.6pF または 1.1pF (標準値)
- 標準的なリード付きパッケージと 0402 フットプリント・パッケージで供給:SOD-523 (DYA) および X1SON (DPY)
- 自動光学検査 (AOI) に適したリード付きパッケージ

2 アプリケーション

- USB Power Delivery (USB-PD)
  - VBUS 保護
  - I/O 保護
- 産業用制御ネットワーク:
  - DeviceNet
  - スマート・ディストリビューション・システム
  - 4/20mA 回路
  - PLC サージ保護
  - ADC サージ保護

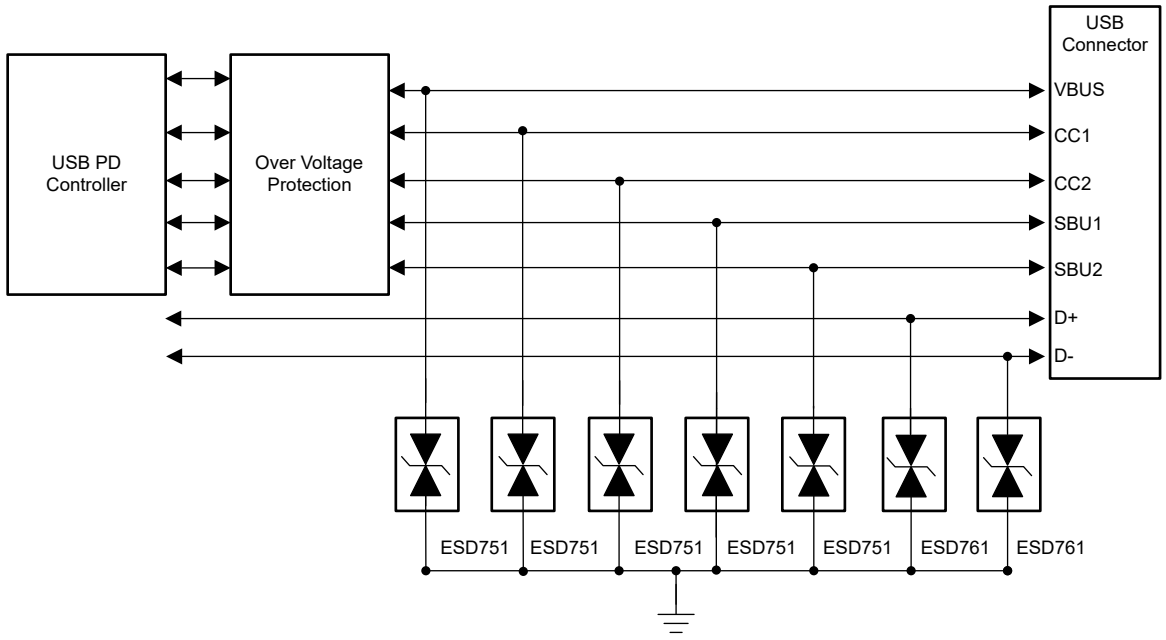
3 概要

ESD751 および ESD761 は、USB Power Delivery (USB-PD) 用のシングル・チャネル、低容量、双方向 ESD 保護デバイスです。これらのデバイスは、IEC 61000-4-2 国際規格で規定されている最大レベルを超える接触 ESD 衝撃 (それぞれ接触 ±22kV、エアギャップ ±22kV と接触 ±15kV、エアギャップ ±15kV) を吸収できるように仕様が規定されています。動的抵抗とクランプ電圧が低いため、過渡現象に対してシステム・レベルで確実な保護を行えます。産業用システムは高いレベルの堅牢性と信頼性を要求するため、この保護機能は重要です。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
ESD751	DYA (SOD-523、2)	1.60mm × 0.80mm
ESD761	DPY (X1SON、2)	1.00mm × 0.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2022) to Revision C (December 2022)	Page
• Updated *Thermal Information* table	5

Changes from Revision A (November 2022) to Revision B (December 2022)	Page
• ESD761 デバイスのステータスを「事前情報」から *「量産データ」に変更*	1

Changes from Revision * (November 2022) to Revision A (November 2022)	Page
• ESD751 デバイスのステータスを「事前情報」から *「量産データ」に変更*	1

5 Pin Configuration and Functions

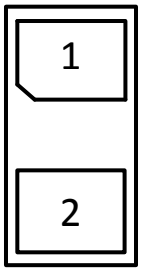


図 5-1. DPY Package, 2-Pin X1SON (Top View)

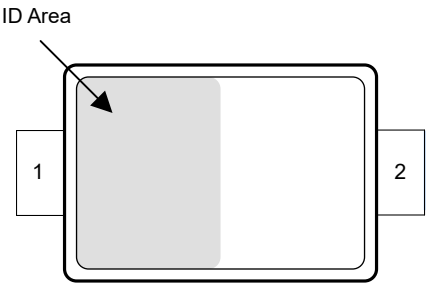


図 5-2. DYA Package, 2-Pin SOD523 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C	ESD751		102	W
		ESD761		65	
I_{PP}	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C	ESD751		2.8	A
		ESD761		1.8	
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD751	±22000	V
			ESD761	±15000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD751	±22000	
			ESD761	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.5 Thermal Information

THERMAL METRIC[1]		ESD751 DYA (SOD-523) 2 PINS	ESD761 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	746.3	282.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	301.2	150.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	509.6	98.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.8	9.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	503.0	97.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–24		24	V
V_{BRF}	Breakdown voltage[1]	I_{IO} = 10 mA, IO to GND		25.5		35.5	V
V_{BRR}		I_{IO} = –10 mA, IO to GND		–35.5		–25.5	
V_{CLAMP}	Clamping voltage[2]	I_{PP} = 2.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD751		36.5		V
		I_{PP} = 1.8 A, t_p = 8/20 µs, IO to GND and GND to IO	ESD761		36.3		
	Clamping voltage[3]	I_{PP} = 16 A, TLP, IO to GND and GND to IO	ESD751		41.5		V
			ESD761		42.5		
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND		-50	1	50	nA
R_{DYN}	Dynamic resistance[3]		ESD751		0.6		Ω
			ESD761		0.53		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV, IO to GND	ESD751		1.6	2.7	pF
			ESD761		1.1	1.8	

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

6.7 Typical Characteristics – ESD751

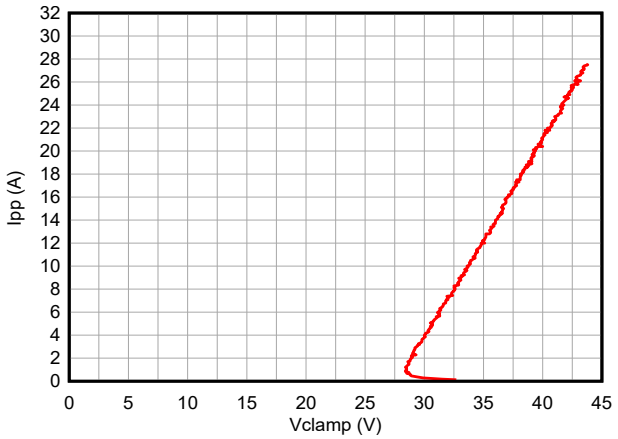


図 6-1. Positive TLP Curve

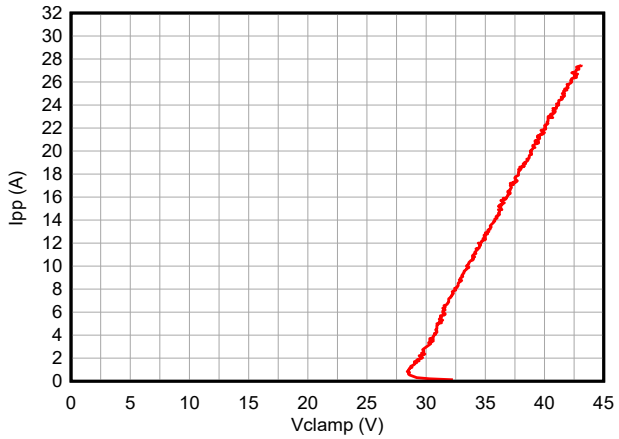


図 6-2. Negative TLP Curve

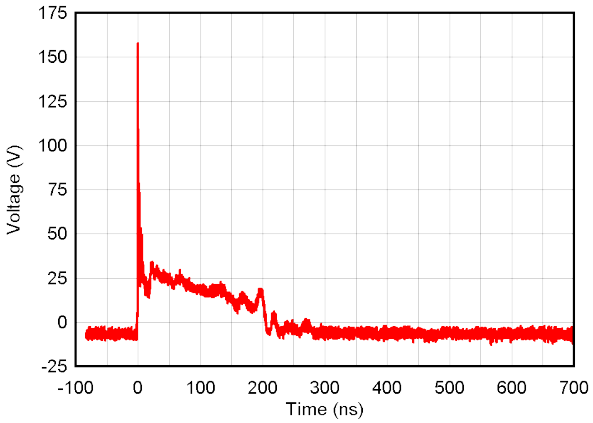


図 6-3. +8-kV Clamped IEC Waveform

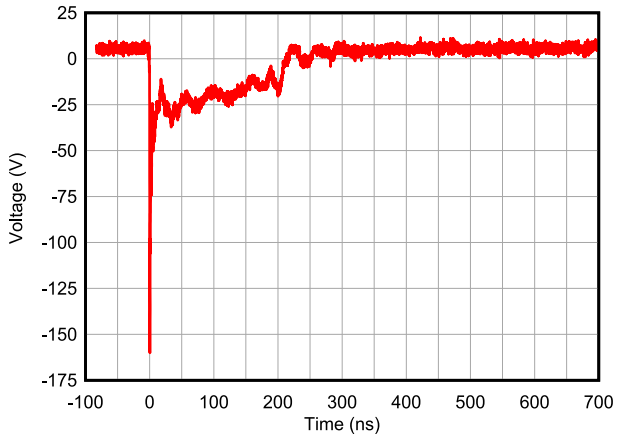


図 6-4. -8-kV Clamped IEC Waveform

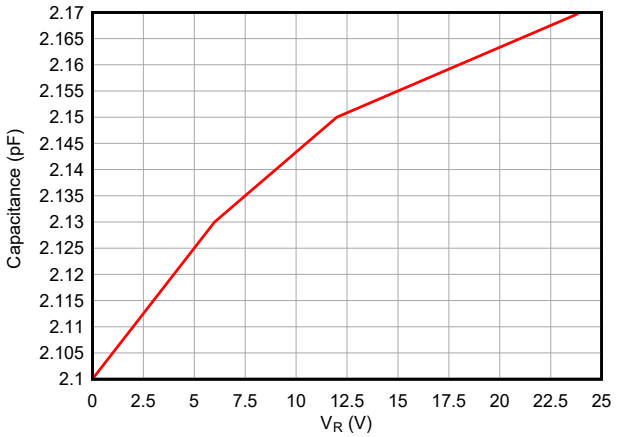


図 6-5. Capacitance vs. Bias Voltage

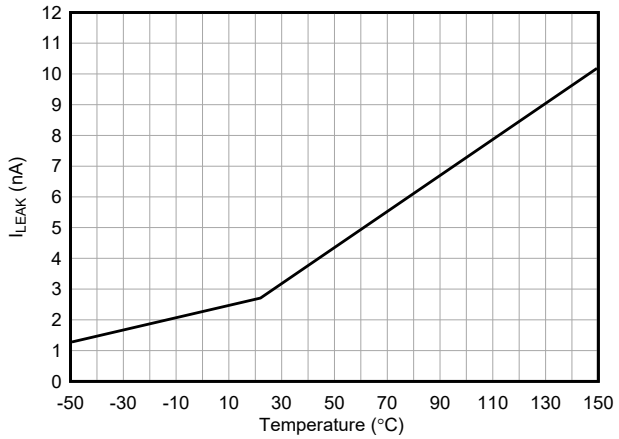


図 6-6. Leakage Current vs. Temperature

6.8 Typical Characteristics - ESD761

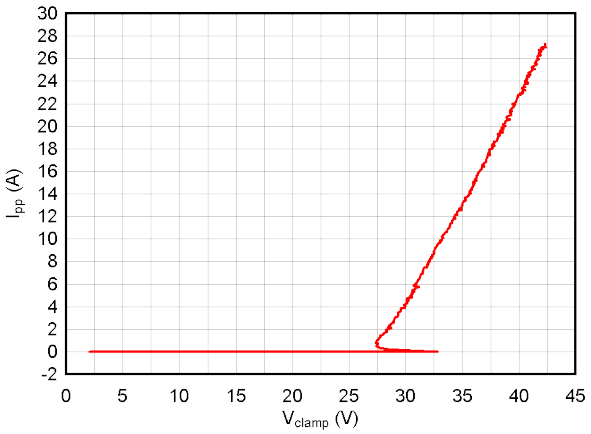


図 6-7. Positive TLP Curve

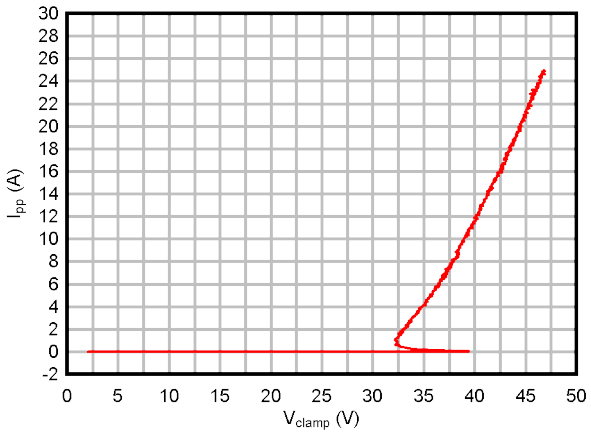


図 6-8. Negative TLP Curve

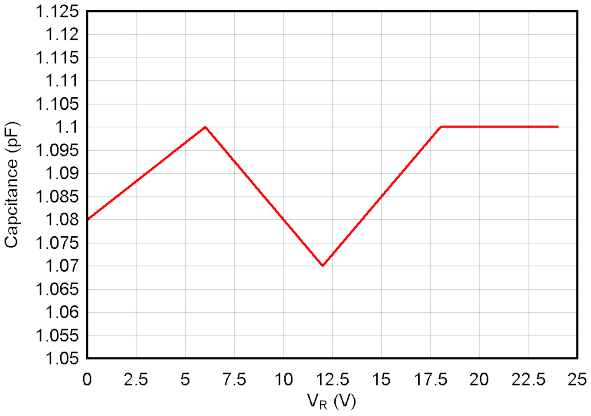


図 6-9. Capacitance vs. Bias Voltage

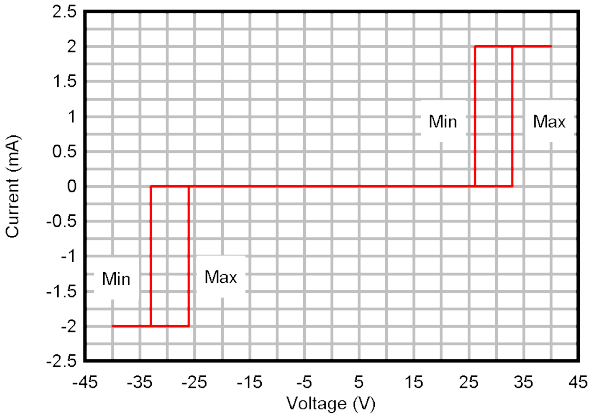


図 6-10. DC Voltage Sweep I-V Curve

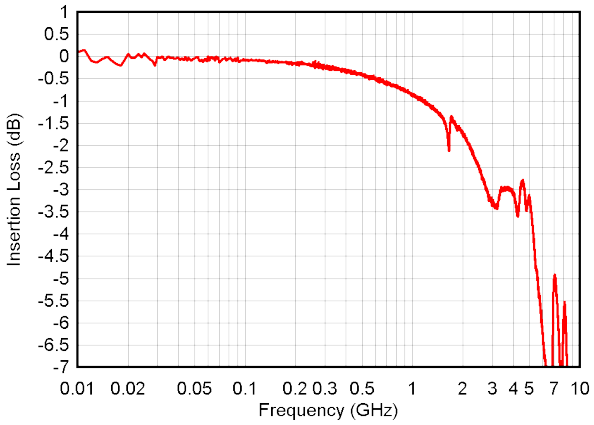


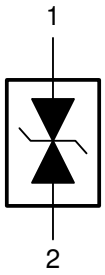
図 6-11. Insertion Loss

7 Detailed Description

7.1 Overview

The ESD751 and ESD761 are single-channel bidirectional ESD diodes. These devices can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 standard. The low capacitance between the I/O pins makes these devices suitable for slower speed signals such as USB-PD or industrial I/O applications. The surge current capability is suitable for VBUS protection or industrial I/Os requiring 2.8 A of surge current protection.

7.2 Functional Block Diagram



7.3 Feature Description

These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the devices are actively protecting other circuits. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes these ESD devices work at extensive temperatures in most environments. The leaded SOD-523 package is good for applications requiring autmotic optical inspection (AOI).

7.3.1 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.8 A and 1.8 A (8/20 µs waveform) for the ESD751 and ESD761 respectively.

7.3.2 I/O Capacitance

The capacitance between the I/O pins is 1.6 pF and 1.1 pF for the ESD751 and ESD761 respectively. The capacitance of these devices support data rates up to 1 Gbps.

7.4 Device Functional Modes

The ESD751 and ESD761 are single channel passive clamps that have low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD751 and ESD761 are single channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial I/O lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

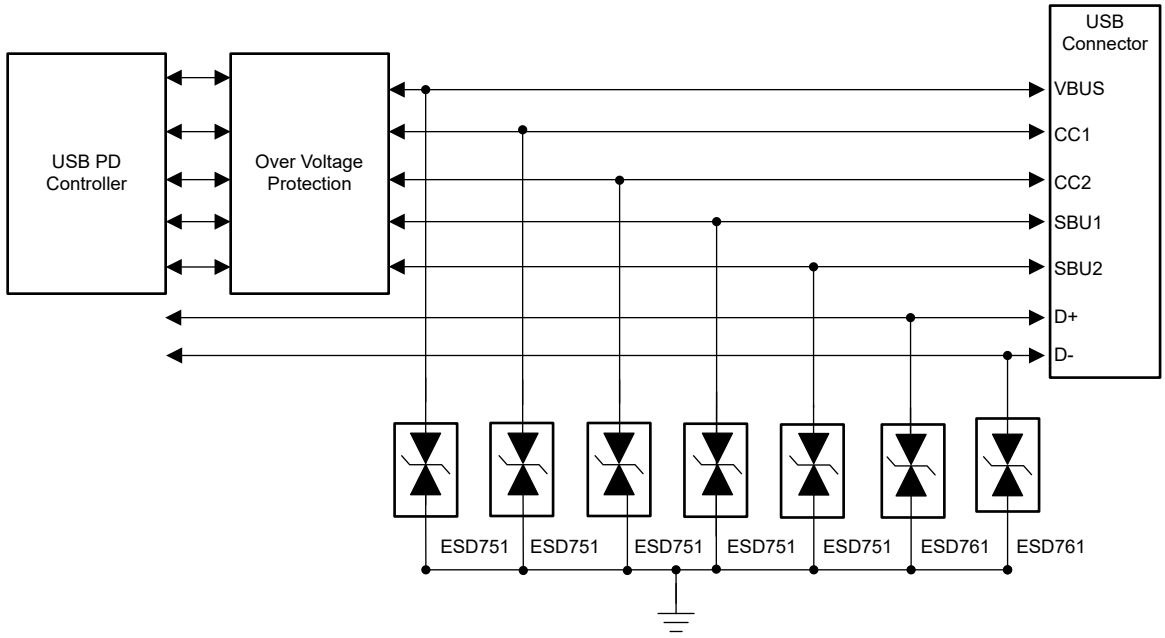


図 8-1. Typical Application

8.2.1 Design Requirements

For this design example, the ESD751 and ESD761 are used to provide ESD protection on a USB-PD connector. 表 8-1 lists the known design parameters for this application.

表 8-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20 V
V_{IO} differential signal range	±3.3 V
V_{RWM}	±24 V
Short to VBUS event on V_{IO}	±20 V
Data rate	Up to 480 Mbps

8.2.2 Detailed Design Procedure

The ESD751 and ESD761 have a V_{RWM} of ±24 V to protect the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 1.7 pF or less permits data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. These devices have an IPP = 2.8 A and 1.8 A (8/20 µs), respectively. The surge current capability of these devices is suitable for protecting the VBUS power rail.

8.2.2.1 Application Curves

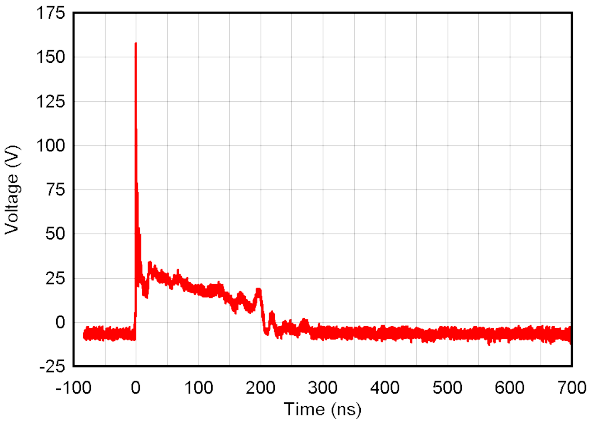


図 8-2. +8-kV Clamped IEC Waveform

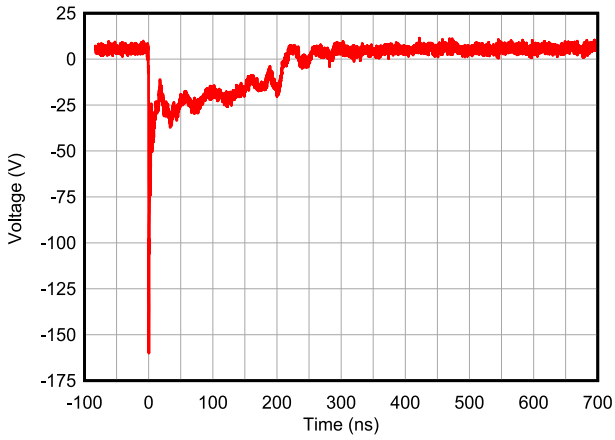


図 8-3. −8-kV Clamped IEC Waveform

9 Power Supply Recommendations

These devices are passive TVS diode-based ESD protection devices, therefore there is no requirement to power them. Ensure that the maximum voltage specifications for each pin is not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

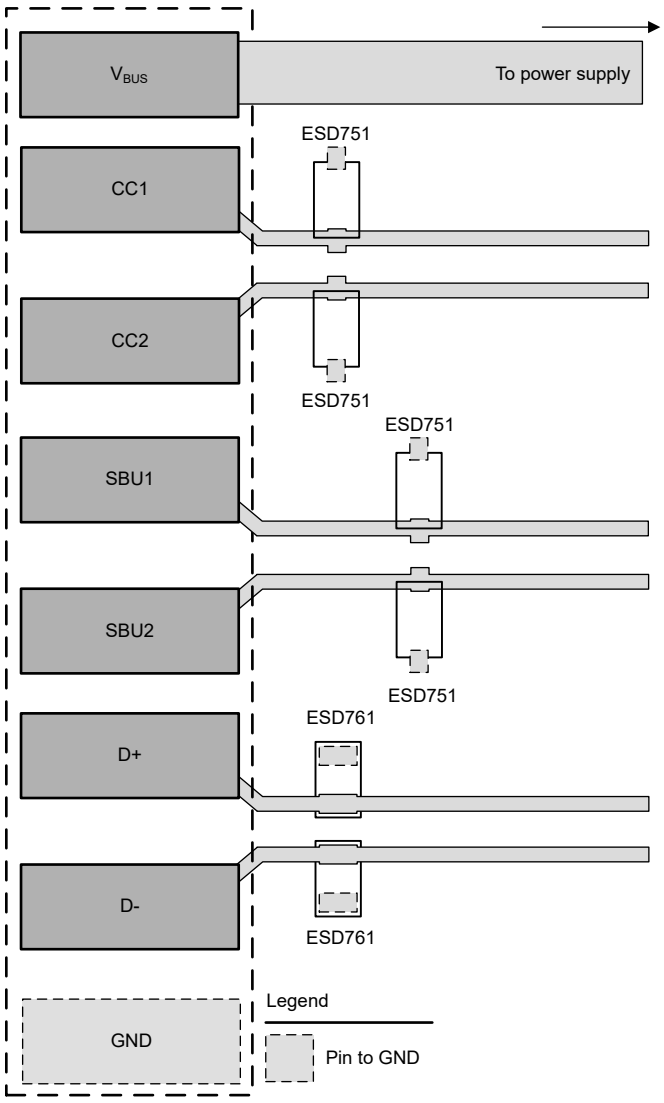


図 10-1. Layout Recommendation

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD751DYAR	ACTIVE	SOT-5X3	DYA	2	8000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	1MN	Samples
ESD761DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 150	NE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ESD751, ESD761 :

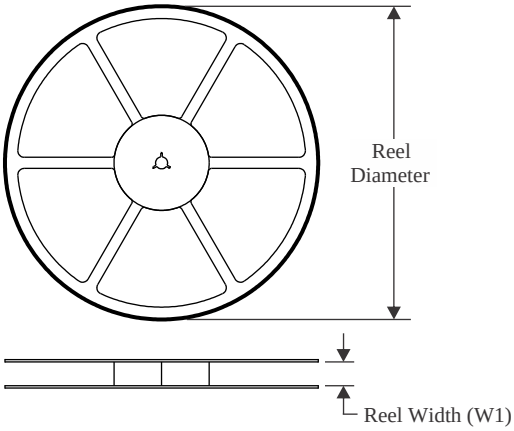
- Automotive : ESD751-Q1, ESD761-Q1

NOTE: Qualified Version Definitions:

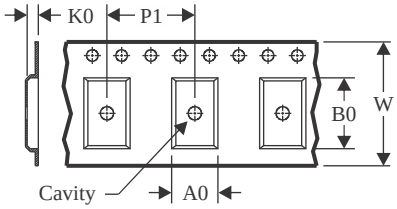
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

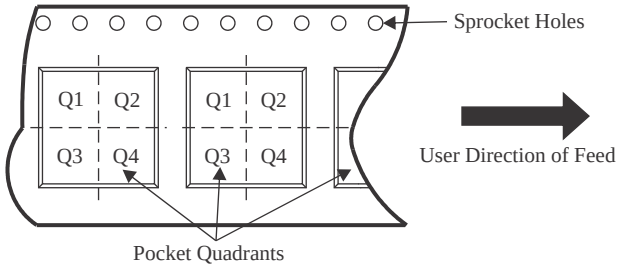


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

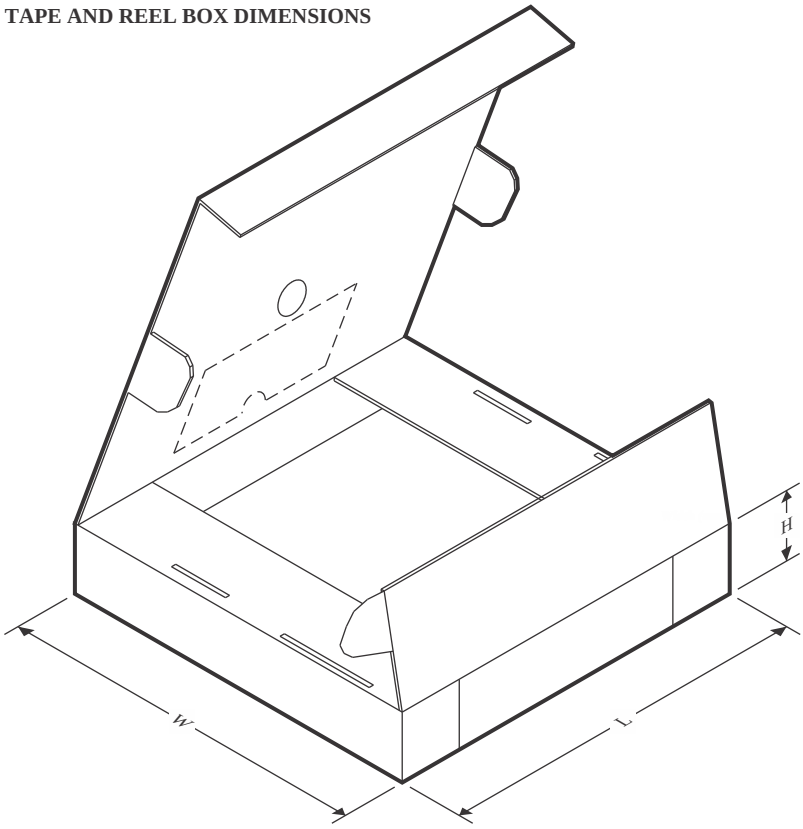
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD751DYAR	SOT-5X3	DYA	2	8000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
ESD761DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

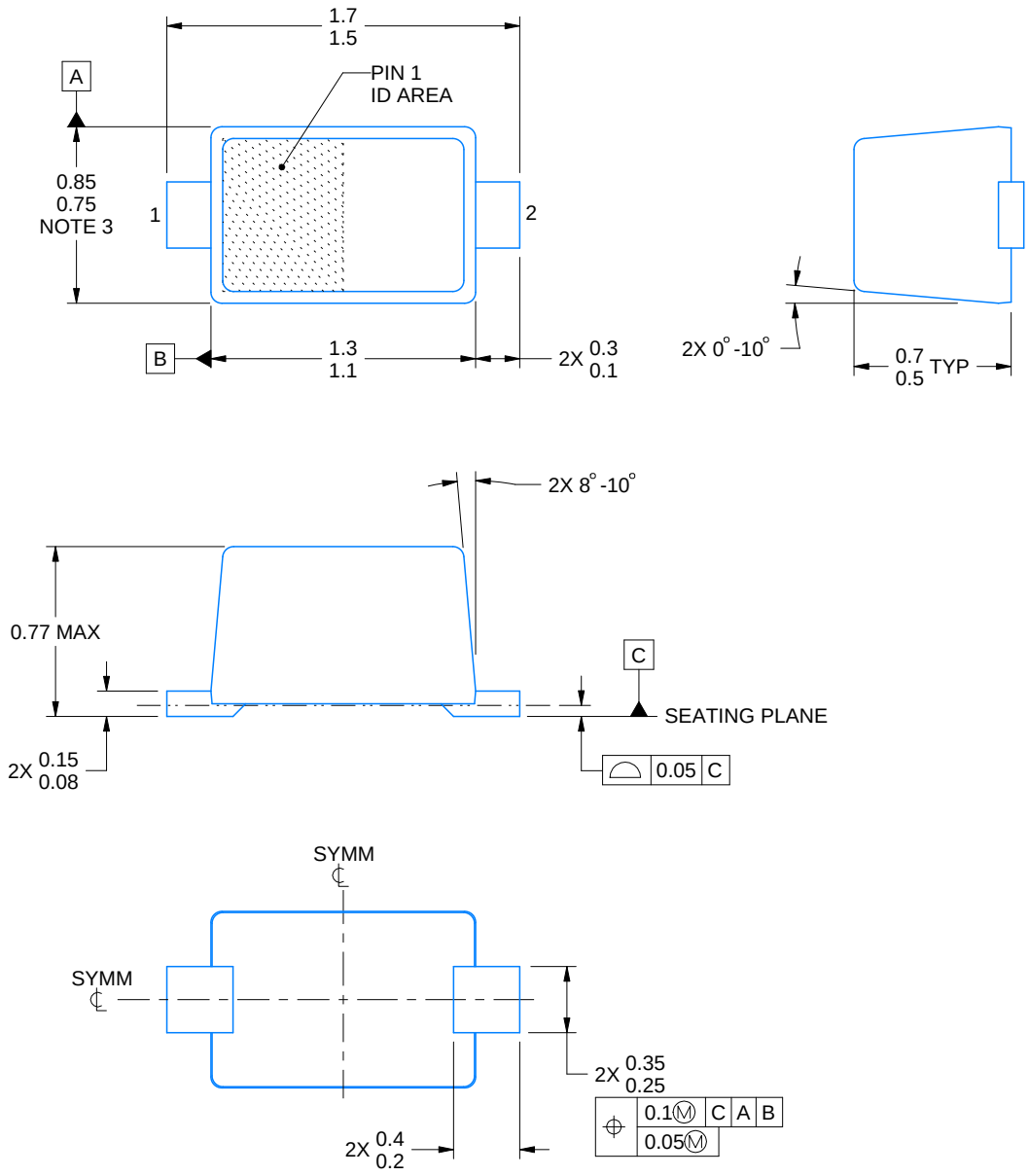
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD751DYAR	SOT-5X3	DYA	2	8000	210.0	200.0	42.0
ESD761DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



4224978/C 11/2024

NOTES:

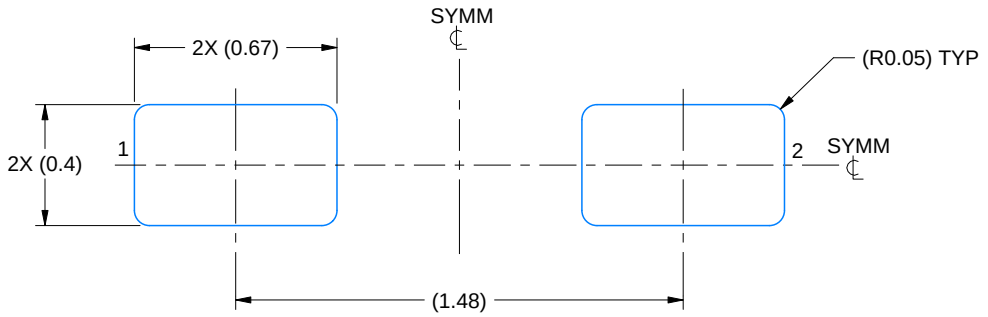
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height

EXAMPLE BOARD LAYOUT

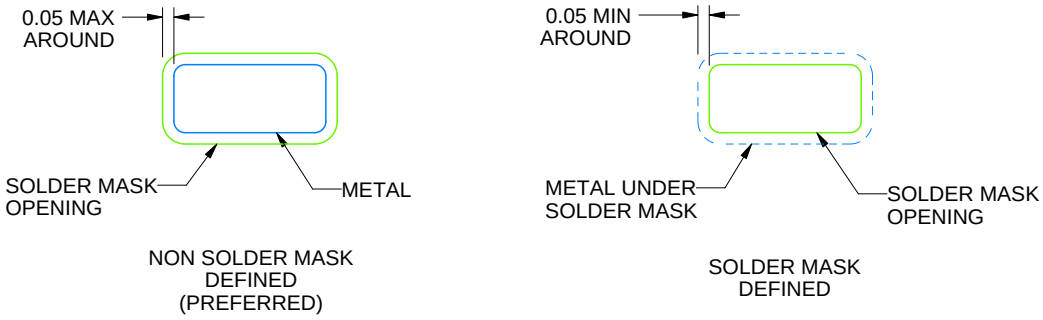
DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

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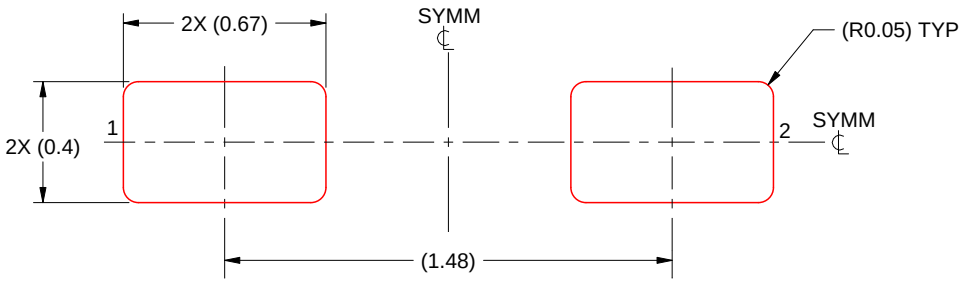
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

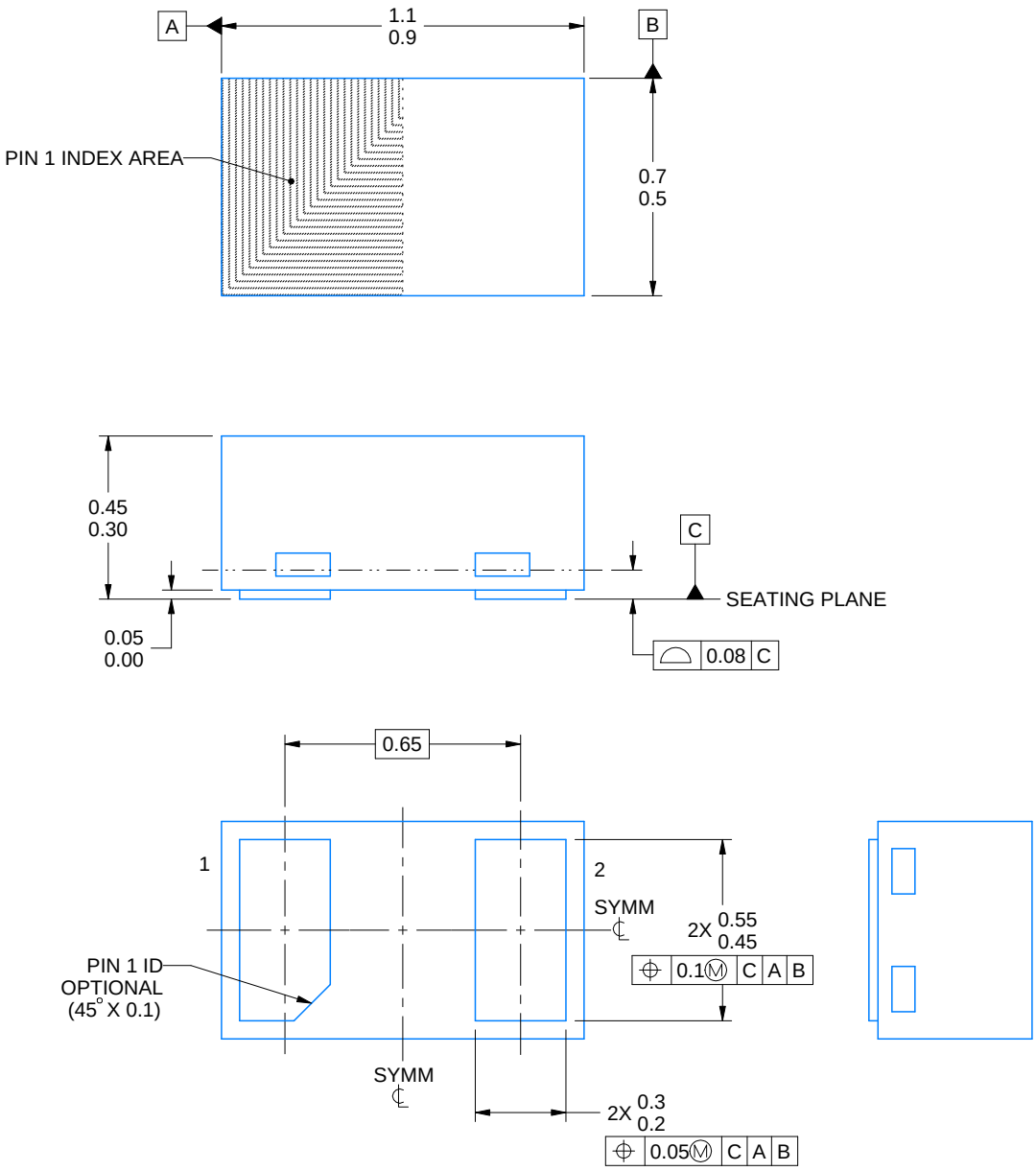
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

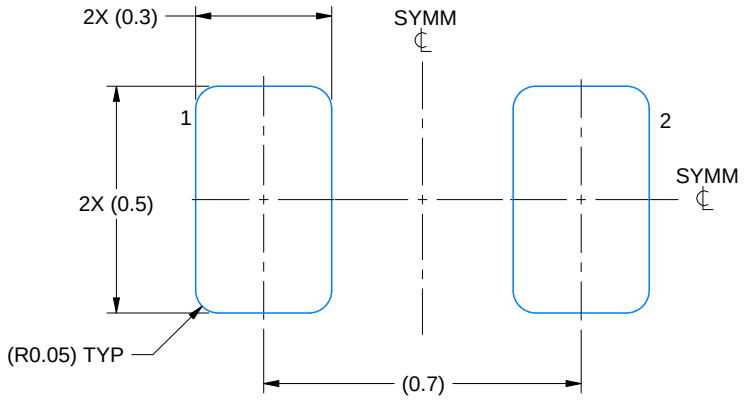
PLASTIC SMALL OUTLINE - NO LEAD



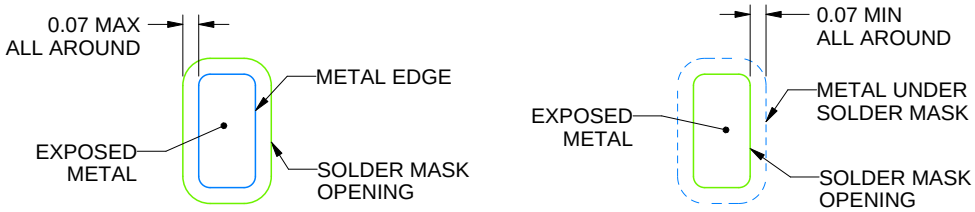
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

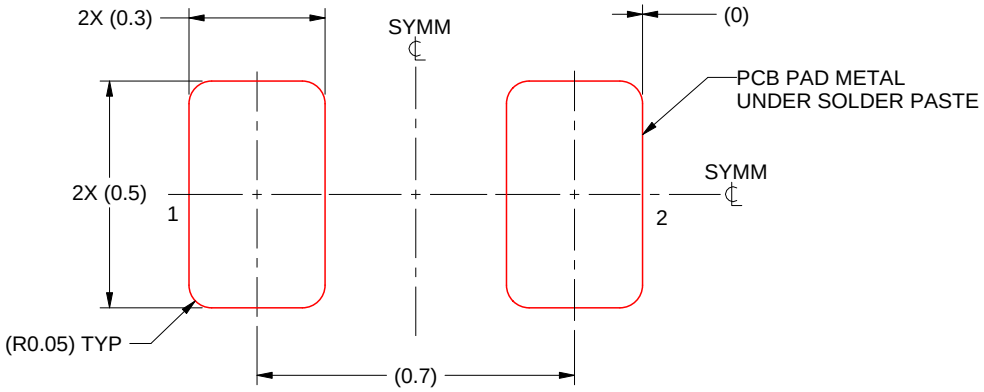


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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